

AMD1044_00192068

```

----- start of module sc count -----
testbench.top.gc.gc.sc.usc_perfmon_qm_num_quads_low,      4096
testbench.top.gc.gc.sc.usc_perfmon_qm_covered_hl6_low,    256
testbench.top.gc.gc.sc.usc_perfmon_hier_num_quads_low,    4096
testbench.top.gc.gc.sc.usc_perfmon_det_num_quads_low,     4096
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h0_low,       0
testbench.top.gc.gc.sc.usc_perfmon_det_mask_h1_low,       0
.
----- end of module sc count -----
----- start of module rb count -----
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_rb_cntx17_busy_low,      4527
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_passed_z_low,    1024
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_quads_failed_z_low,     1
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_exp_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_fills_sep_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_low, 0
testbench.top.gc.gc.rb_3.urb_perfmon_wrapper.urb_perfmon_num_8x256_depth_cache_flushes_sep, 0
.
----- end of module rb count -----

```

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AMD1044_00192070



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R400 BIOS Progress

- New-architecture based R300/R400 VGA BIOS are implemented
- BIOS ECR Status

Component	Status			Total
	Q	A	FA+	
Documentation	0	5	3	8
Build Process	0	5	4	9
Command Decoder	0	16	42	58
R400 BIOS	50	15	32	97
BIOS IKOS	46	2	2	50
BIOS Test on R300	7	6	3	16
BIOS Utility	0	21	8	29
BIOS Kit	2	1	0	3
<i>Subtotal</i>	<i>105</i>	<i>71</i>	<i>94</i>	<i>270</i>
<i>Summary</i>	<i>38.89%</i>	<i>26.30%</i>	<i>34.81%</i>	

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R400 BIOS Verification

- Command Decoder Coverage Test

Test Category	Review	PASS	FAIL	UNKNOWN	%PASS
Move/Alignment Tests	Last Review	20	4	0	83%
	This Review	24	0	0	100%
ALU Tests	Last Review	20	8	0	71%
	This Review	24	4	0	86%
Control Command Tests	Last Review	19	8	0	70%
	This Review	23	0	1	96%
<i>Summary</i>	<i>Last Review</i>	59	20	0	75%
	<i>This Review</i>	71	4	1	93%

- The new R300 BIOS passed following VGA tests:

- Amidiag 5.42 from American Megatrends Inc.
- DMU - DisplayMate Professional Utilities from Sonera Technologies
- VgaDiag from Renaissance GRX Inc.

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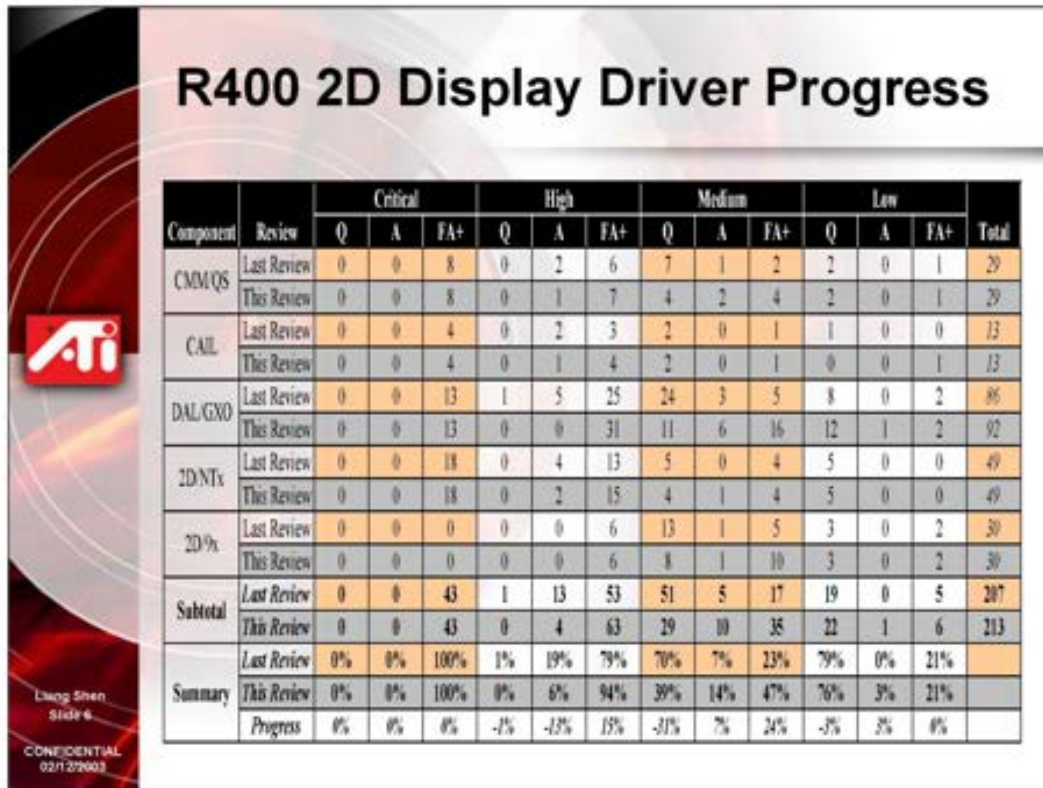
R400 BIOS Risks and Plan

- Risks
 - Amount of testing on IKOS is huge due to new BIOS architecture
 - Timing critical implementations can not be verified until ASIC back
 - Current VGA code is very old and hard to maintain
- Plan
 - Categorize R400 BIOS tasks with proper priority and verify them on IKOS in a proper order
 - Using existing ASIC (R300) to verify timing critical implementation
 - Modularize VGA code as a long term goal (may not R400 timeframe)
 - Also plan to make our new BIOS VBE3.0 compliant (nVidia claims): investigation phase

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R400 2D Driver Verification

• DDT Test Status

M	Test Group	# Cases	Test Result (0210303)		
			PASS	FAIL	UNKNOWN
1024x768x32	Draw	30	30	0	0
	DrawIcon	1	1	0	0
	GetDibits	1	1	0	0
	StretchDib	0	0	0	0
	Text	23	21	2	0
	Drawing	10	10	0	0
	Poly	6	6	0	0
	Region	6	6	0	0
	Shape	7	7	0	0
	GradientFill	0	0	0	0
	AlphaBlend	0	0	0	0
	AAFont	0	0	0	0
	Summary	84	97.62%	2.38%	0.00%

no coverage yet
emulator regression failure

no coverage yet
no coverage yet
no coverage yet

• New Packets Verification

- GradientFill: WHQL Test – PASS (detected MS DCT defect and MS just fixed it)
- AlphaBlend: WHQL Test - 384 of 495 (77%) PASS; most of the failures are result of incorrectly programming the bottom-right clipping coordinates (fixing now); the other issue is the lack of support for SRC/DST surfaces of differing sizes – John just updated microcode and PM4 spec (CL#83549)
- AAFont: feature is working, but like R300 (AAFont turned off), s/w need to resolve rendering problems with overlapping constant background characters

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R400 2D Driver Risks and Plan

- Risks
 - R400 DAL/GXO implementation can only be verified on IKOS
 - Bandwidth sensitive tasks can not be verified until ASIC back
- Plan
 - Using the small (5M) IKOS box to start DAL/GXO testing ASAP (only MC/BIF/DC/MH/SI blocks are required); in addition, we are now working on wrapping display emulator for s/w testing
 - Dump more 2D packets for h/w teams testing; 2D packets capture support is available; currently debugging playback issues
 - Profiling of 2D driver with various benchmarks for performance tuning: initial profiling results for WinBench and WinStone are available now and under analysis
- Other
 - Control Panel: R400 display related control panel features are discussed and proposed; 3D related control panel features need to be followed
 - More thorough R400 CMM/QS verification strategy is defined and is under way

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R400 3D Graphics Driver Progress

- Compiler
 - Code complete all remaining DX9 and OGL2 opcodes support (await test cases from verification team for fully testing)
 - Couple remaining render states support is under way
 - Bug fixing has been progressing well and number of open bugs has been kept small
 - Number of optimization tasks are started
- SSM
 - Updated SSM interface
 - Complete rework SSM fetch for 8/8 internal and 16/16 external allocation
 - Design of “wildcarded shaders” support
 - Debugging and fixing problems from DX SDK Apps, DX Test Suites, and Func Tests

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R400 3D Graphics Driver Progress (cont.)

- D3D
 - Completed MSAA, 3D Texture, Cylindrical Wrap, and Texture Filtering
 - Pushed through a simple n-patch triangle through the DirectX driver, SSM and the R400 emulator
 - Focus on debugging failures of DX SDK Apps, DX Test Suite, and Func Tests
- OGL
 - Render to Texture and HP_occlusion_test/NV_occlusion_query are supported
 - Shadow Buffers, 2 Sided Lighting, and Polygon Stippling are implemented and debugging with SSM/compiler
 - Focus on debugging failures of Conformance Tests, Quickcheck Test Suite, and Glut

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R400 3D Driver Verification

- SSM/Compiler

- Currently SSMClient Test Suite consists of cases with and w/o equivalent DX instructions. For the former, there are golden images available; while verification team is working on a mechanism to generate golden images for those w/o equivalent DX instructions (i.e., the UNKNOWN category).

Test Name	Review	#Cases	Test Results				
			PASS	FAIL	ERR/HANG	UNKNOWN	%PASS
SSMClient	Last Review	6734	722	221	5791	0	10.72%
	This Review	8485	945	96	4243	3201	11.14%

Note: some of ERR/HANG are those ILs not yet supported by interpreter – in other words, those are not SSM/Compiler issues; more detailed analysis is under way.

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R400 3D Driver Verification (cont.)

- D3D Driver
 - Verification Tests (DX Test Suite = SimpleD3D + DX8/DX9 Shader)

Test Name	Review	#Cases	Test Results				
			PASS	FAIL	ERR/HANG	UNKNOWN	%PASS
DX Test Suite	Last Review	3136	2923	164	49	0	93.21%
	This Review	3657	3436	220	1	0	93.96%
FuncTest	Last Review	5995	1893	2230	1872	0	31.58%
	This Review	3661	1781	1880	0	0	48.65%

A slight "accounting" issue (not "Enron" ☺) will be fixed in the incoming release

- DXn SDK Apps

DXn	Review	PASS		FAIL		ERR/HANG		UNKNOWN		Total
		#	%	#	%	#	%	#	%	
7	Last Review	14	51.85%	4	14.61%	9	33.33%	0	0.00%	27
	This Review	19	70.37%	2	7.41%	6	22.22%	0	0.00%	27
	Progress	5	18.52%	-2	-7.41%	-3	-11.11%	0	0.00%	0
8.1	Last Review	7	28.00%	9	36.00%	6	24.00%	3	12.00%	25
	This Review	21	47.73%	17	38.64%	5	11.36%	1	2.27%	44
	Progress	14	19.73%	8	2.44%	-1	-12.64%	-2	-8.73%	18
9	Last Review	6	22.22%	8	29.63%	13	48.15%	0	0.00%	27
	This Review	23	60.53%	8	21.05%	7	18.42%	0	0.00%	38
	Progress	17	38.30%	0	-8.58%	-6	-29.73%	0	0.00%	11
Total	Last Review	27	34.18%	21	26.58%	28	35.44%	3	3.86%	79
	This Review	63	57.80%	27	24.77%	18	16.51%	1	0.92%	109
	Progress	36	23.62%	6	-1.81%	-10	-18.93%	-2	-2.88%	30

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R400 3D Driver Verification (cont.)

• OGL Driver

– OpenGL Conformance Tests (with 19 ATI extensions)

Review	Passed		Not Run		Failed		Crashed		Hung		Total
	#	%	#	%	#	%	#	%	#	%	
Last Review	56	70.89%	0	0.00%	18	22.78%	1	1.27%	4	5.06%	79
This Review	65	66.33%	5	5.10%	24	24.49%	3	3.06%	1	1.02%	98
Progress	9	4.68%	5	5.18%	6	1.78%	2	1.80%	3	4.04%	16

– OpenGL Glut

Passed		Failed		Err/Hang		Unknown		Total
#	%	#	%	#	%	#	%	
46	75.41%	2	3.28%	12	19.67%	1	1.64%	61

– ATI's Quickcheck

- Clear: 30 of 31 PASS
- Frustum: PASS
- ImmediateApi: 7 of 14 PASS
- Lighting: 64 of 96 PASS
- Stipple: 8 of 19 PASS
- Xform: 287 PASS
- The remaining Quickcheck tests were run, with no valid results obtained (either software crash, emulator problem, or system lockup): ARBVertexProgram, ATIVertexShader, Fog, GlutRedbook, Materials, MiniMustPass, Primitives, RenderTex, SecondColor, Texturing, and Vertex Arrays

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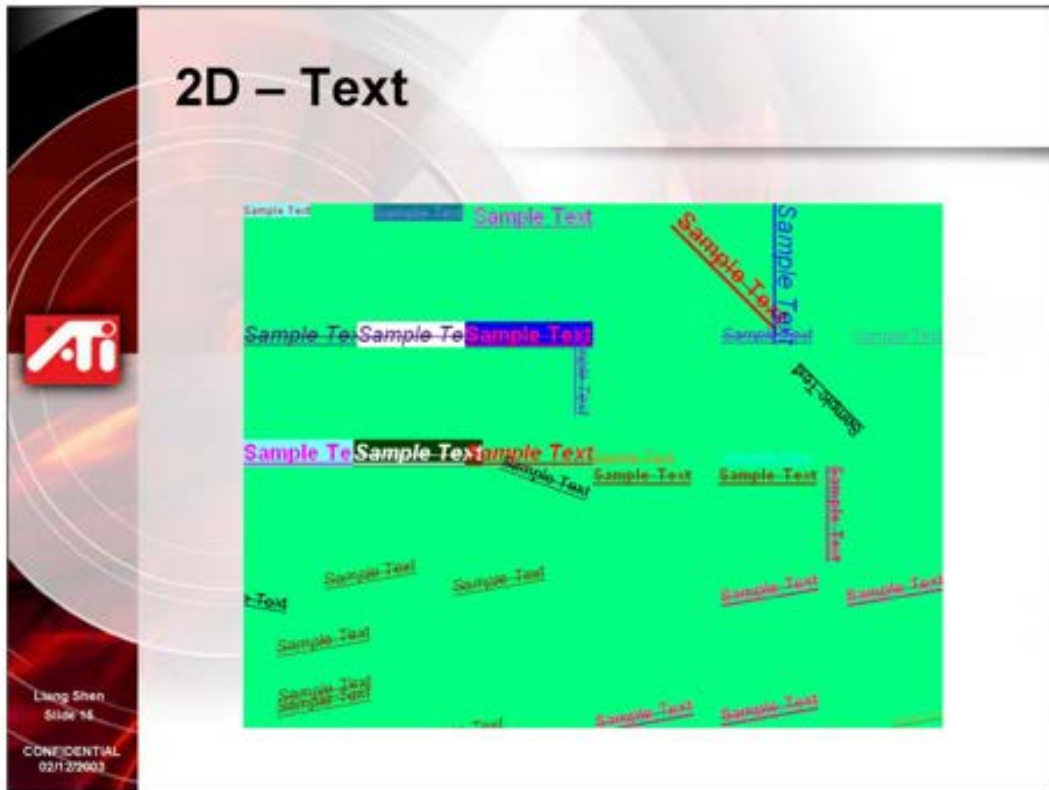
R400 3D Driver Risks and Plan

- Risks
 - Regression failure and feature completeness of emulator
 - Test Coverage of 3D Component Test Suites
 - Compiler and StateCache performance work not yet started
- Plan
 - Completing development of the following planned test suites for IKOS by 2/28
 - Emphasizing more on s/w testing and complete the following s/w verification milestone before s/w IKOS starts (3/16)
 - SSM/Compiler: pass all SSMClient test suite except for branching
 - D3D: 100% pass of DX7 and DX8 shader test suites and func tests; 90% pass of DX9 shader test suites and func tests
 - OpenGL: pass all red book apps and OGL applets; at least 80% pass of WHQL Test Set, Conformance Test Suite, and ATI's Quickcheck Test Suite
 - Developing driver optimization and performance tuning plan for delivery at end of February.
 - Complete all key features (required to verify on IKOS) in 3D drivers by the end of March
- Others
 - QS-EMU² has been released and provide significant performance improvement

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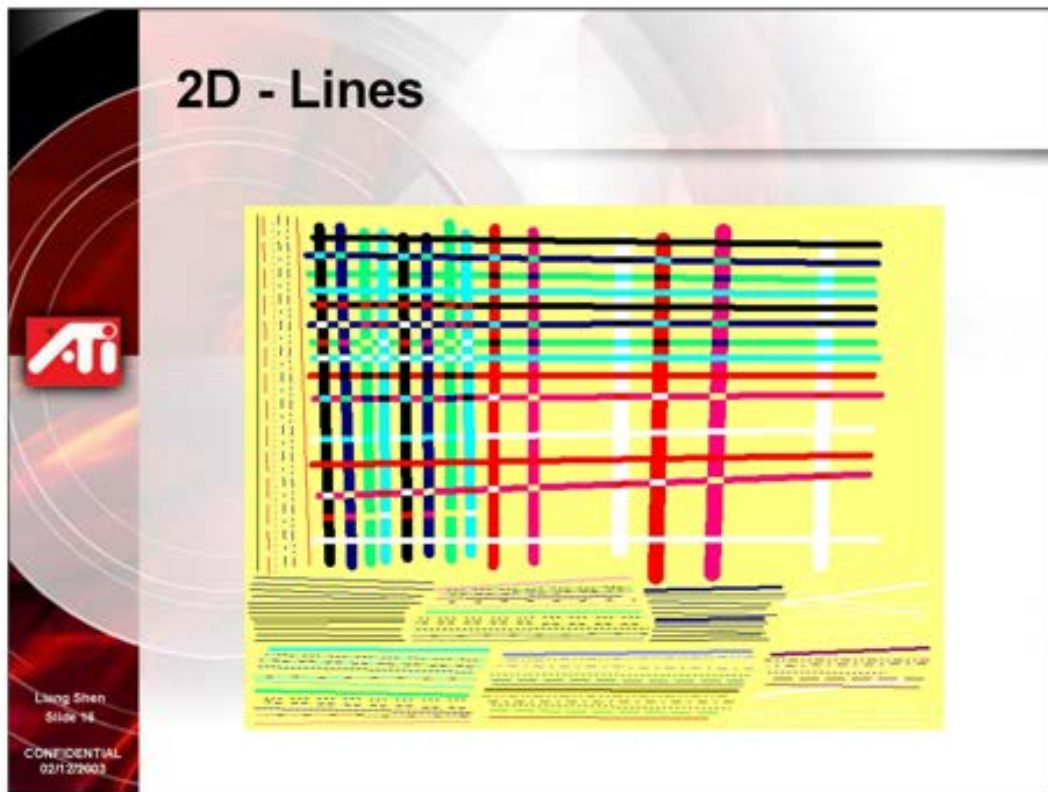
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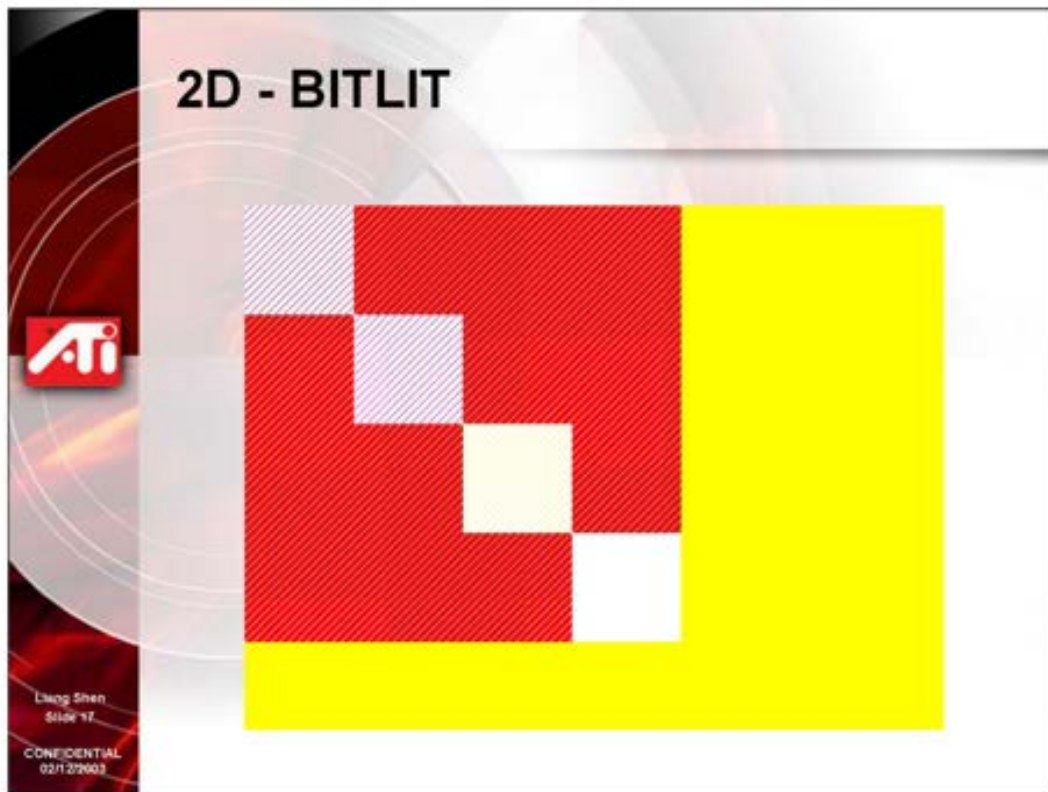
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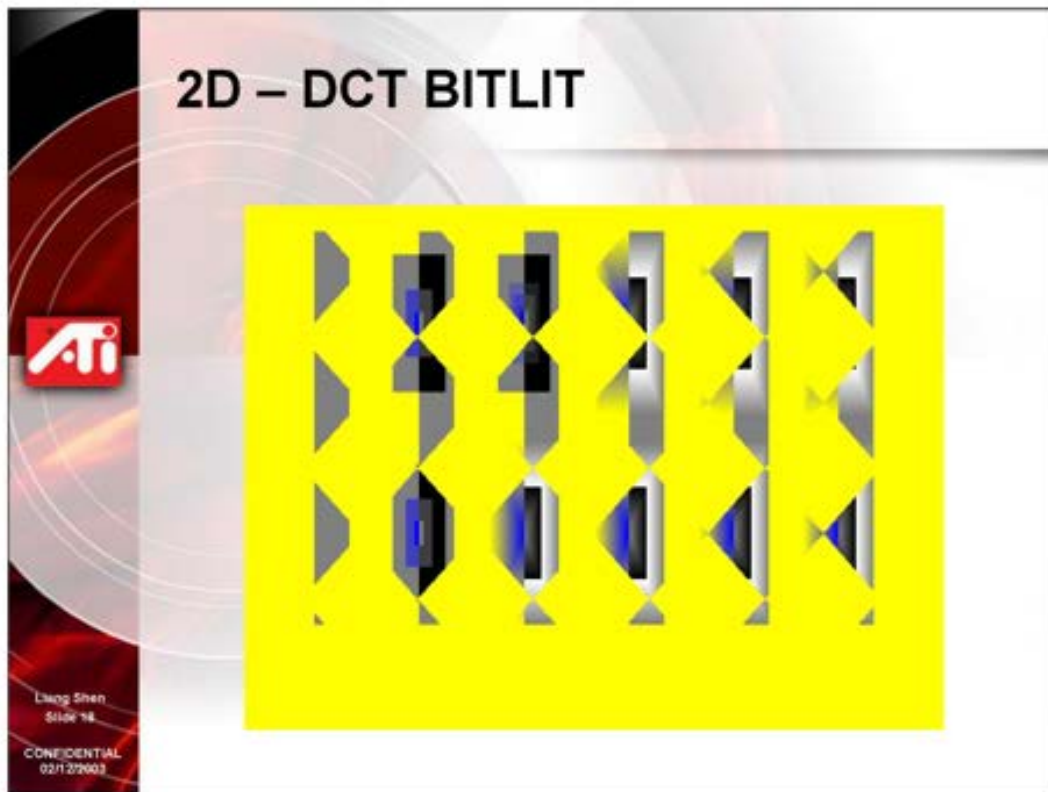
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3D WinBench 200 – Rust Valley



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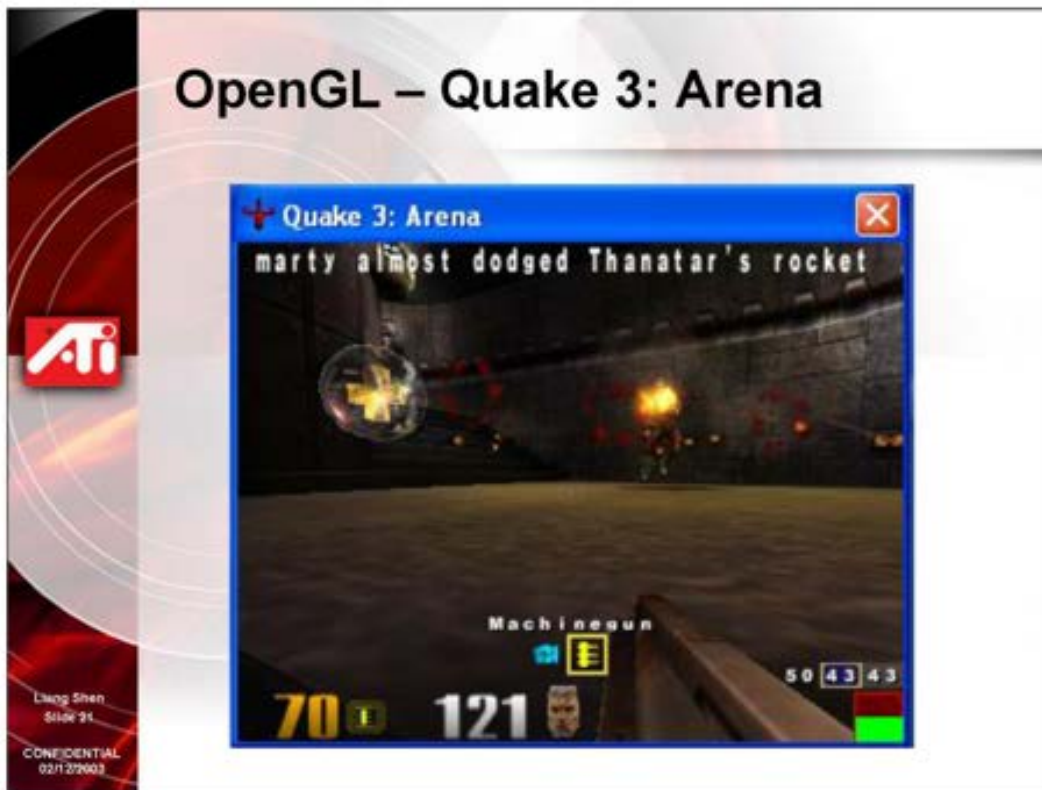
3D WinBench 2000 - Hangar



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OpenGL – Quake 3: Arena



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- Some Screenshots

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R400 BIOS Progress

- New-architecture based R300/R400 VGA BIOS are implemented
- BIOS ECR Status

Component	Status			Total
	Q	A	FA+	
Documentation	0	5	3	8
Build Process	0	5	4	9
Command Decoder	0	16	42	58
R400 BIOS	50	15	32	97
BIOS IKOS	46	2	2	50
BIOS Test on R300	7	6	3	16
BIOS Utility	0	21	8	29
BIOS Kit	2	1	0	3
<i>Subtotal</i>	<i>105</i>	<i>71</i>	<i>94</i>	<i>270</i>
<i>Summary</i>	<i>38.89%</i>	<i>26.30%</i>	<i>34.81%</i>	

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R400 BIOS Verification

- Command Decoder Coverage Test

Test Category	Review	PASS	FAIL	UNKNOWN	%PASS
Move/Alignment Tests	Last Review	20	4	0	83%
	This Review	24	0	0	100%
ALU Tests	Last Review	20	8	0	71%
	This Review	24	4	0	86%
Control Command Tests	Last Review	19	8	0	70%
	This Review	23	0	1	96%
<i>Summary</i>	<i>Last Review</i>	59	20	0	75%
	<i>This Review</i>	71	4	1	93%

- The new R300 BIOS passed following VGA tests:

- Amidiag 5.42 from American Megatrends Inc.
- DMU - DisplayMate Professional Utilities from Sonera Technologies
- VgaDiag from Renaissance GRX Inc.

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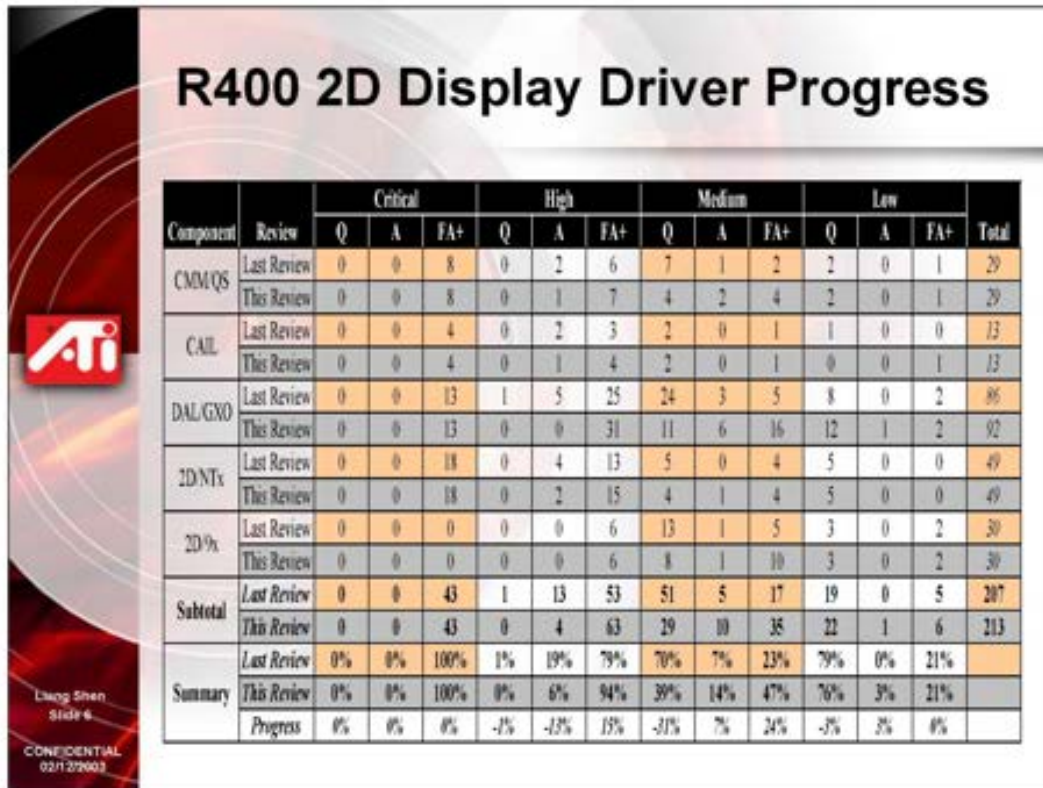
R400 BIOS Risks and Plan

- Risks
 - Amount of testing on IKOS is huge due to new BIOS architecture
 - Timing critical implementations can not be verified until ASIC back
 - Current VGA code is very old and hard to maintain
- Plan
 - Categorize R400 BIOS tasks with proper priority and verify them on IKOS in a proper order
 - Using existing ASIC (R300) to verify timing critical implementation
 - Modularize VGA code as a long term goal (may not R400 timeframe)
 - Also plan to make our new BIOS VBE3.0 compliant (nVidia claims): investigation phase

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R400 2D Driver Verification

• DDT Test Status

M	Test Group	# Cases	Test Result (0210303)		
			PASS	FAIL	UNKNOWN
1024x768x32	Draw	30	30	0	0
	DrawIcon	1	1	0	0
	GetDibits	1	1	0	0
	StretchDib	0	0	0	0
	Text	23	21	2	0
	DrawRect	10	10	0	0
	Poly	6	6	0	0
	Region	6	6	0	0
	Shape	7	7	0	0
	GradientFill	0	0	0	0
	AlphaBlend	0	0	0	0
	AAFont	0	0	0	0
	Summary	84	97.62%	2.38%	0.00%

no coverage yet
emulator regression failure

no coverage yet
no coverage yet
no coverage yet

• New Packets Verification

- GradientFill: WHQL Test – PASS (detected MS DCT defect and MS just fixed it)
- AlphaBlend: WHQL Test - 384 of 495 (77%) PASS; most of the failures are result of incorrectly programming the bottom-right clipping coordinates (fixing now); the other issue is the lack of support for SRC/DST surfaces of differing sizes – John just updated microcode and PM4 spec (CL#83549)
- AAFont: feature is working, but like R300 (AAFont turned off), s/w need to resolve rendering problems with overlapping constant background characters

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R400 2D Driver Risks and Plan

- Risks
 - R400 DAL/GXO implementation can only be verified on IKOS
 - Bandwidth sensitive tasks can not be verified until ASIC back
- Plan
 - Using the small (5M) IKOS box to start DAL/GXO testing ASAP (only MC/BIF/DC/MH/SI blocks are required); in addition, we are now working on wrapping display emulator for s/w testing
 - Dump more 2D packets for h/w teams testing; 2D packets capture support is available; currently debugging playback issues
 - Profiling of 2D driver with various benchmarks for performance tuning: initial profiling results for WinBench and WinStone are available now and under analysis
- Other
 - Control Panel: R400 display related control panel features are discussed and proposed; 3D related control panel features need to be followed
 - More thorough R400 CMM/QS verification strategy is defined and is under way

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R400 3D Graphics Driver Progress

- Compiler
 - Code complete all remaining DX9 and OGL2 opcodes support (await test cases from verification team for fully testing)
 - Couple remaining render states support is under way
 - Bug fixing has been progressing well and number of open bugs has been kept small
 - Number of optimization tasks are started
- SSM
 - Updated SSM interface
 - Complete rework SSM fetch for 8/8 internal and 16/16 external allocation
 - Design of “wildcarded shaders” support
 - Debugging and fixing problems found by OGL, MM, and D3D

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R400 3D Graphics Driver Progress (cont.)

- D3D
 - Complete 3D texture, cylindrical wrap, and texture filtering
 - Continue implementing MSAA, Z/Stencil compression, and reviewing texture format support
 - Pushed through a simple n-patch triangle through the DirectX driver, SSM and the R400 emulator
 - Focus on debugging failures of DX SDK Apps, DX Test Suite, and Func Tests
- OGL
 - Render to Texture and HP_occlusion_test/NV_occlusion_query are supported
 - Shadow Buffers, 2 Sided Lighting, and Polygon Stippling are implemented and debugging with SSM/compiler
 - Focus on debugging failures of Conformance Tests, Quickcheck Test Suite, and Glut

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R400 3D Driver Verification

- SSM/Compiler

- Currently SSMClient Test Suite consists of cases with and w/o equivalent DX instructions. For the former, there are golden images available; while verification team is working on a mechanism to generate golden images for those w/o equivalent DX instructions (i.e., the UNKNOWN category).

Test Name	Review	#Cases	Test Results				
			PASS	FAIL	ERR/HANG	UNKNOWN	%PASS
SSMClient	Last Review	6734	722	221	5791	0	10.72%
	This Review	8485	945	96	4243	3201	11.14%

Note: some of ERR/HANG are those ILs not yet supported by interpreter – in other words, those may not be SSM/Compiler issues; more detailed analysis is under way.

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R400 3D Driver Verification (cont.)

- D3D Driver
 - Verification Tests (DX Test Suite = SimpleD3D + DX8/DX9 Shader)

Test Name	Review	#Cases	Test Results				
			PASS	FAIL	ERR/HANG	UNKNOWN	%PASS
DX Test Suite	Last Review	3136	2923	164	49	0	93.21%
	This Review	3657	3436	220	1	0	93.96%
FuncTest	Last Review	5995	1893	2230	1872	0	31.58%
	This Review	3661	1781	1880	0	0	48.65%

A slight "accounting" issue (not "Enron" ☺) will be fixed in the incoming release

- DXn SDK Apps

DXn	Review	PASS		FAIL		ERR/HANG		UNKNOWN		Total
		#	%	#	%	#	%	#	%	
7	Last Review	14	51.85%	4	14.61%	9	33.33%	0	0.00%	27
	This Review	19	70.37%	2	7.41%	6	22.22%	0	0.00%	27
	Progress	5	18.52%	-2	-7.41%	-3	-11.11%	0	0.00%	0
8.1	Last Review	7	28.00%	9	36.00%	6	24.00%	3	12.00%	25
	This Review	21	47.73%	17	38.64%	5	11.36%	1	2.27%	44
	Progress	14	19.73%	8	2.44%	-1	-12.64%	-2	-8.73%	18
9	Last Review	6	22.22%	8	29.63%	13	46.15%	0	0.00%	27
	This Review	23	60.53%	8	21.05%	7	18.42%	0	0.00%	38
	Progress	17	38.30%	0	-8.58%	-6	-29.73%	0	0.00%	11
Total	Last Review	27	34.18%	21	26.58%	28	35.44%	3	3.86%	79
	This Review	63	57.80%	27	24.77%	18	16.51%	1	0.92%	109
	Progress	36	23.62%	6	-1.81%	-10	-18.93%	-2	-2.88%	30

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R400 3D Driver Verification (cont.)

• OGL Driver

– OpenGL Conformance Tests (with 19 ATI extensions)

Review	Passed		Not Run		Failed		Crashed		Hung		Total
	#	%	#	%	#	%	#	%	#	%	
Last Review	56	70.89%	0	0.00%	18	22.78%	1	1.27%	4	5.06%	79
This Review	65	66.33%	5	5.10%	24	24.49%	3	3.06%	1	1.02%	98
Progress	9	4.68%	5	5.18%	6	1.79%	2	1.80%	3	4.04%	16

– OpenGL Glut

Passed		Failed		Err/Hang		Unknown		Total
#	%	#	%	#	%	#	%	
46	75.41%	2	3.28%	12	19.67%	1	1.64%	61

– ATI's Quickcheck

- Clear: 30 of 31 PASS
- Frustum: PASS
- ImmediateApi: 7 of 14 PASS
- Lighting: 64 of 96 PASS
- Stipple: 8 of 19 PASS
- Xform: 287 PASS
- The remaining Quickcheck tests were run, with no valid results obtained (either software crash, emulator problem, or system lockup): ARBVertexProgram, ATIVertexShader, Fog, GlutRedbook, Materials, MiniMustPass, Primitives, RenderTex, SecondColor, Texturing, and Vertex Arrays

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Slide 13

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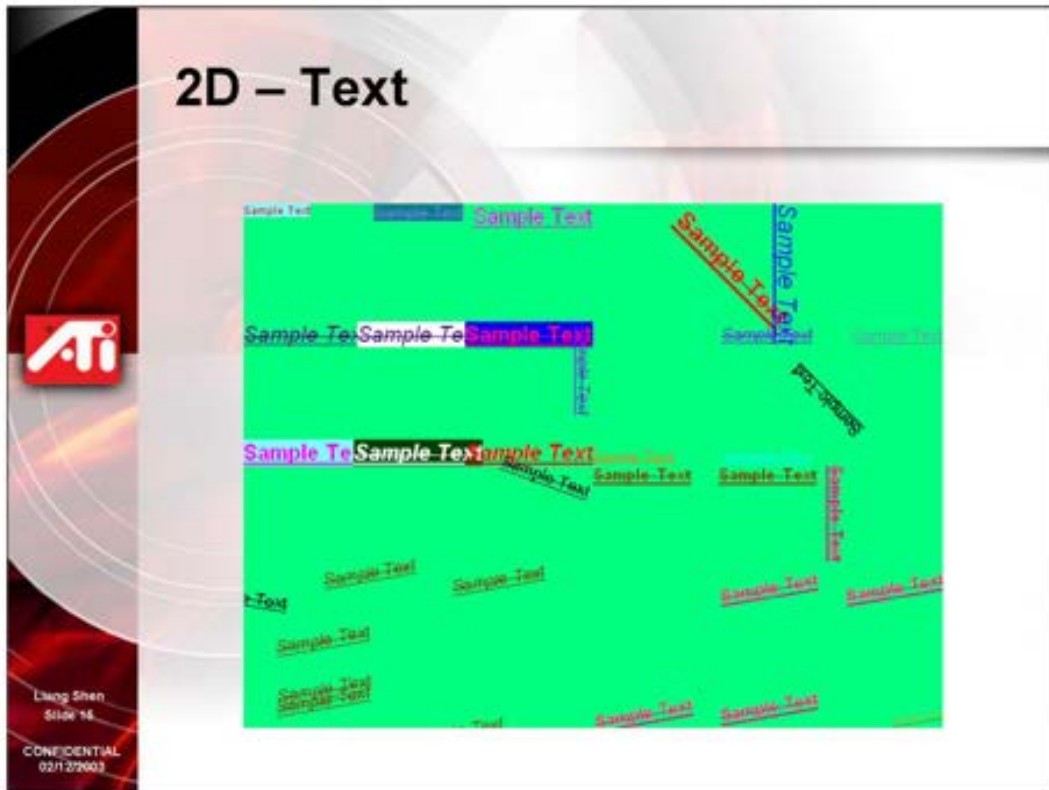
R400 3D Driver Risks and Plan

- Risks
 - Regression failure and feature completeness of emulator
 - Test Coverage of 3D Component Test Suites
 - Compiler and StateCache performance work not yet started
- Plan
 - Completing development of the following planned test suites for IKOS by 2/28
 - Emphasizing more on s/w testing and complete the following s/w verification milestone before s/w IKOS starts (3/16)
 - SSM/Compiler: pass all SSMClient test suite except for branching
 - D3D: 100% pass of DX7 and DX8 shader test suites and func tests; 90% pass of DX9 shader test suites and func tests
 - OpenGL: pass all red book apps and OGL applets; at least 80% pass of WHQL Test Set, Conformance Test Suite, and ATI's Quickcheck Test Suite
 - Developing driver optimization and performance tuning plan for delivery at end of February.
 - Complete all key features (required to verify on IKOS) in 3D drivers by the end of March
- Others
 - QS-EMU² has been released and provide significant performance improvement

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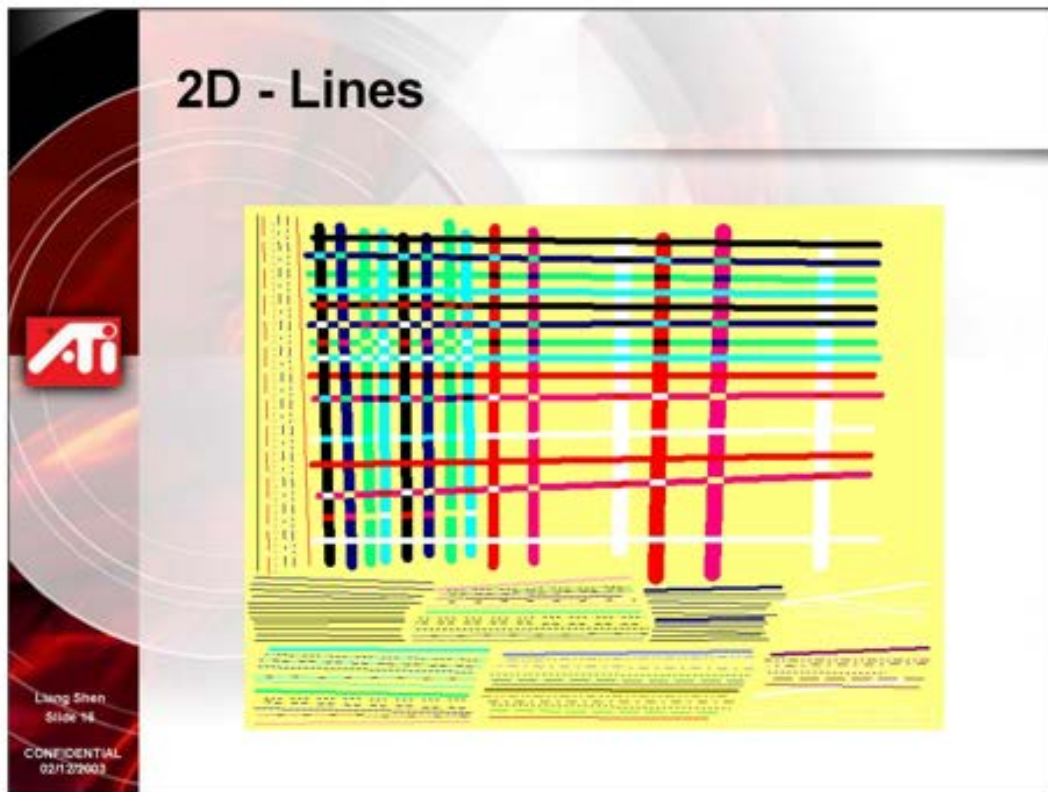
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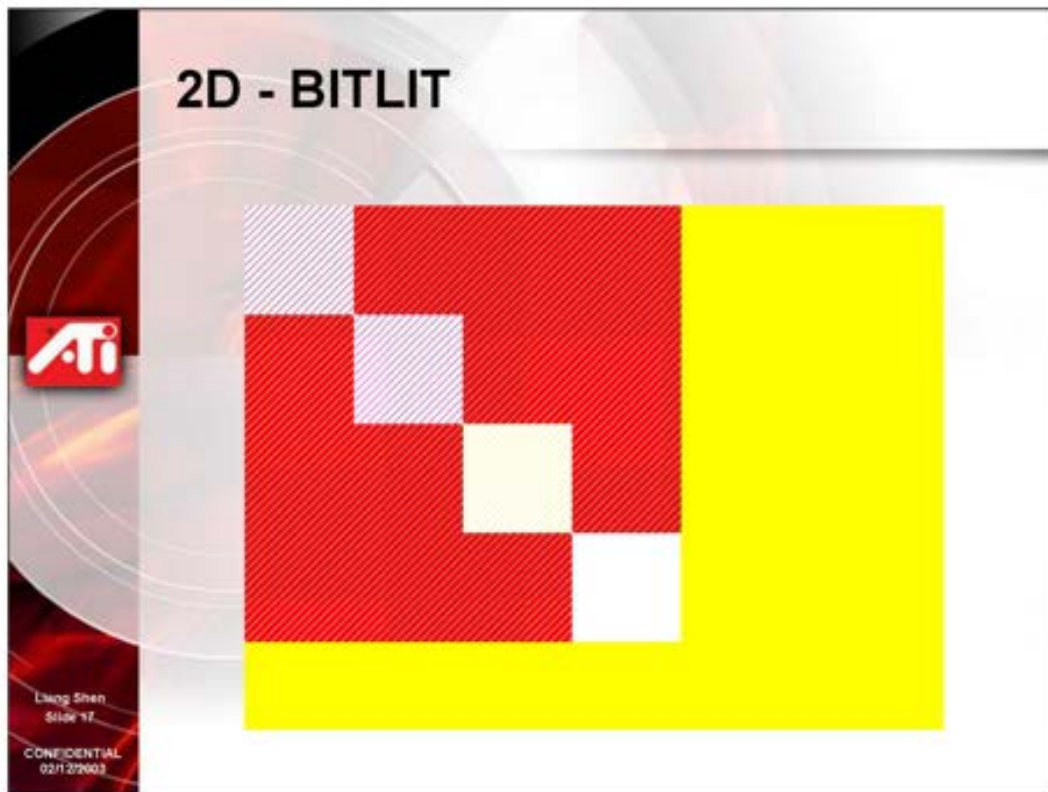
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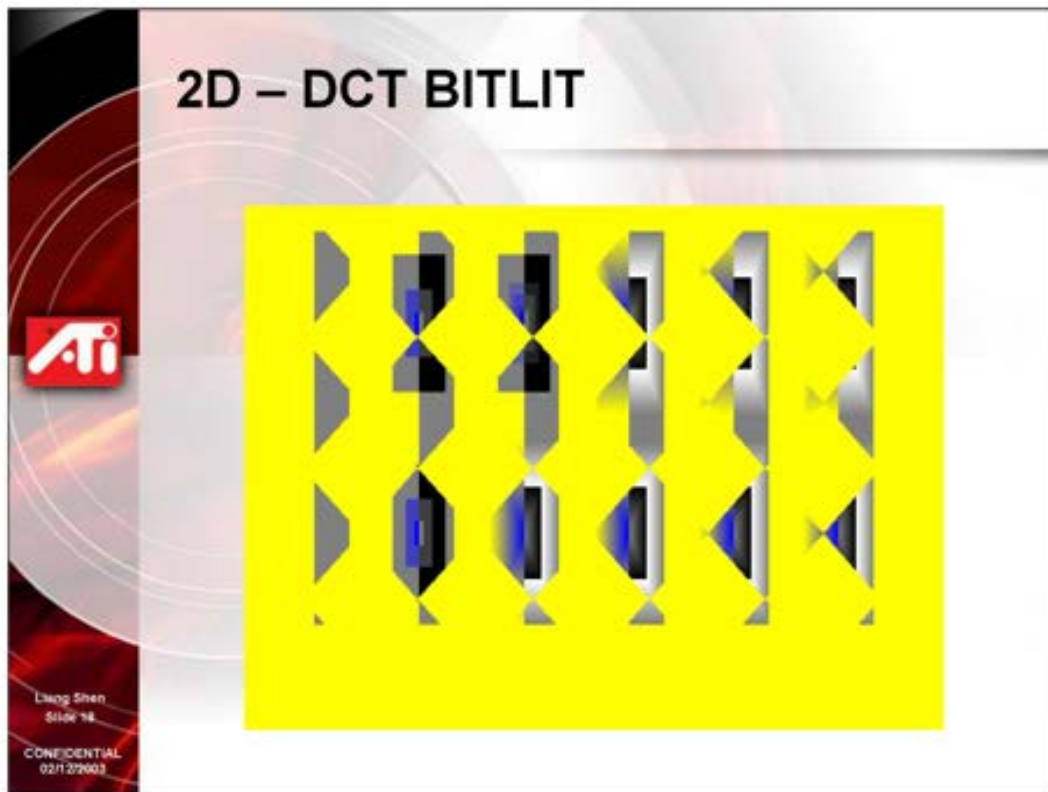
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3D WinBench 200 – Rust Valley



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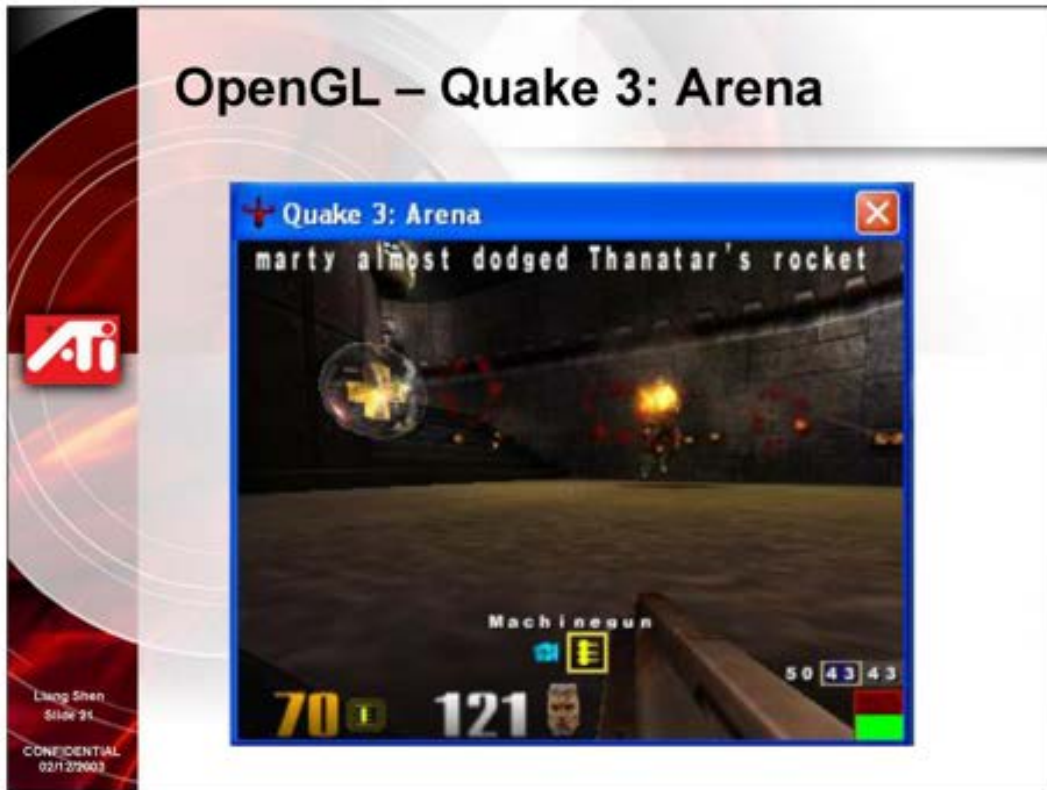
3D WinBench 2000 - Hangar



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OpenGL – Quake 3: Arena



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Staffing and Assignments

- Rahul Singh to join R400 PD team from ATI TOR
 - Physically in Silicon Valley starting 2/18
 - Already started work while in TOR
- 1 contractor rolling over from RV350 respin efforts
- Starting with rel_3.0C, all tiles (20 unique) will have owners
- R400 PD fully staffed:
 - 18 PD engineers total (not counting CAD):
 - 16 tile owners: 9 full time, 7 contractors. 4 tile owners are doubled up
 - 2 full time on top level netlisting and P&R

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Progress in the last month

- Top level netlisting
 - Did three releases based off netlist 3.0
 - Tile netlist quality much improved from rel_3.0A to rel_3.0C :
 - Tile power grid
 - Congestion based pin/ram assignments
 - Repeaters inserted
 - Tile constraints pushed down from top level constraints
 - Timing budgets used to generate tile io constraints
 - Found and fixed top level netlist bug
 - Top level netlist now of good enough quality to start top level P&R trials
 - Top level tile refinement
 - KS tile
 - 2 RB tiles
 - 2 MC tiles
 - Misc grouping (SI tile)

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Progress in the last month (cont)

- Tile P&R progress
 - Tile P&R flow in place and proceeding with refinement stage
 - some tiles have gone through the flow once already with decent timing for rel_3.0B (<1ns setup violation): AB, PA, SCB, SX, TP
 - Some tiles have already had tile reviews using a tile review template with the LD team. All tile should have their reviews regardless of progress this week.
 - Other tiles either have gone through the flow with poor timing (>1ns) or haven't completed the flow yet, but don't see any show stoppers yet (after the clock insertion workaround): BIF, CP, SC

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Top issues

- Many top level issues still need to be resolved
 - Top level power grid design being refined - moving to thin M7, need to follow up with pad, analog, TSMC, etc
 - Top level power grid needs to be implemented
 - Top level clocking needs to be implemented
 - Top level P&R started, but experiencing tool crashes
 - Run time issues for top level netlisting flow
- Some tiles having problems getting through the flow
 - DC – clocking issues, constraint issues, tool (nanoroute) crash issues. Many netlist fixes coming in netlist 4.0
 - RB/SP size issues – causing run time problems (>1 day in PKS) and tool memory footprint bloat. In netlist 3.0, RB has 490K instances, SP has 400K instances (goal was to have tiles come in < 300K instances. DC and some TC tiles also over 300K)
 - MH – currently not routable, working on tile floorplans and investigating ways to improve the tile aspect ratio in future netlist releases
 - SX – routable, but needed an area bloat, which might impact the top level floorplan.

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Top issues (cont)

- Global issues have caused tile P&R to stall/restart
 - Clock insertion strategy and clock gating structures – working around for now until fix in netlist 5.0 time frame
 - Virage memory size fluctuations – invalidated the floorplan for some tiles
- Some tiles really can't start until rel_4.0A, but will try to go through the flow using rel_3.0C:
 - 2 MC tiles, SQ, 3 TC tiles, KS
- Tile utilizations pre-repeater insertion seems on the high side

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Risks and Future Issues

- Runtime for top level netlisting flow – Currently about 5 days. Working with Cadence to bring that down (2-3 days?). Working on in house solutions to make incremental releases faster/easier
- Tile size and growth and changes – impacts top level floorplan for both 4.0 and 5.0
 - 4.0: TC split, SP getting bigger (400K → 440K?), potential MH/SQ aspect ratio change
 - 5.0: RB split – will need a new tile owner
- Top level P&R and timing closure – continue to address issues in house and work with Cadence on tool crashes
- Scan – Will get an incremental 4.0 release from LD team with DFT logic in place to start implementing scanStitching correctly. Currently just getting routing impact into the design

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R400 Review Action Summary

- Program – Next tentative review date is on March 12th
- Last Month
 - R400 Software
 - Plan support for packet dump capture – [Complete](#)
 - Quality goal needed for conformance of compression/coherency code - [Open](#)
 - IKOS Meeting with Ron White for SW – [Complete](#)
 - R400 Hardware
 - SDR 3.3V support on DVO port (requirements) – [Closing, finalizing](#)
 - RB break-up for Netlist delivery (NL4.0 vs NL5.0) – [Planned for NL5](#)
 - Code coverage analysis on all blocks – [In process](#)
 - DC dependency on MH bugs - [Ken Correll focused on support](#)
 - DC instance count – [Instance count reduced, discussing with Mark Lee](#)
 - SQ test coverage review – [Complete](#)
 - Performance
 - PA performance registers – [Complete](#)
 - GC testbench for better performance data – [Not working yet, still debugging](#)
 - Contractors to run/analyze tests – [Ko Yu, Allen G. will pursue as necessary](#)
 - Chip Integration
 - Power – [Greg S. analyzing power](#)
 - Operations – [Update meeting held with Anita Siu, working fuse process](#)
 - Pad – [Review scheduled for end of February](#)
 - Physical Design
 - Feedback from Netlist 3 needed – [Mark Lee began, PD/LD meetings in process](#)

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R400 Review Action Summary

- This review
 - R400 Software
 - Quality goal needed for conformance of compression/coherency code - [Open](#)
 - Is HW testing using Set_state or Type0 packets in tests – Mark Fowler
 - SW ran into problem recently
 - R400 Hardware
 - RB split for netlist 5 – Frank Hering
 - AB file dumps – Mike Mantor / Larry Seiler
 - Remove degamma from DXTC as a feature ?
 - Code coverage analysis on blocks – Mark Fowler
 - TC performance path – Steve Morein / Clay Taylor / Andy Gruber
 - DC instance count high – Lili S./Frank H. to close with Mark Lee
 - Assist with debug of 2D tests – Mark Earl / John Carey / Harry Wise
 - SQ/SX has risk, continue to monitor – Peter Pellenite
 - Review CP code
 - Rewrite of 2D Drivers for derivative area savings – Joe Cox
 - CP code removed, need to review – Andy Gruber / John Carey
 - Performance
 - Orlando to work more with playback – Chris Gray / Allen G.
 - GC testbench for better performance data – [Open](#)
 - Chip Integration
 - Thermal solution need overall owner
 - Boards group involvement priority (or window is lost)
 - Operations – give memory/fuse package to Anita for ASE
 - Pad – clock distribution in pads needs to be finalized with SIV
 - Physical Design
 - BIF description for R400 PD – Lili Sinclair
 - PD to LD communication mostly working (may need to expand/change list)
 - Clock insertion methodology – meeting 2/14

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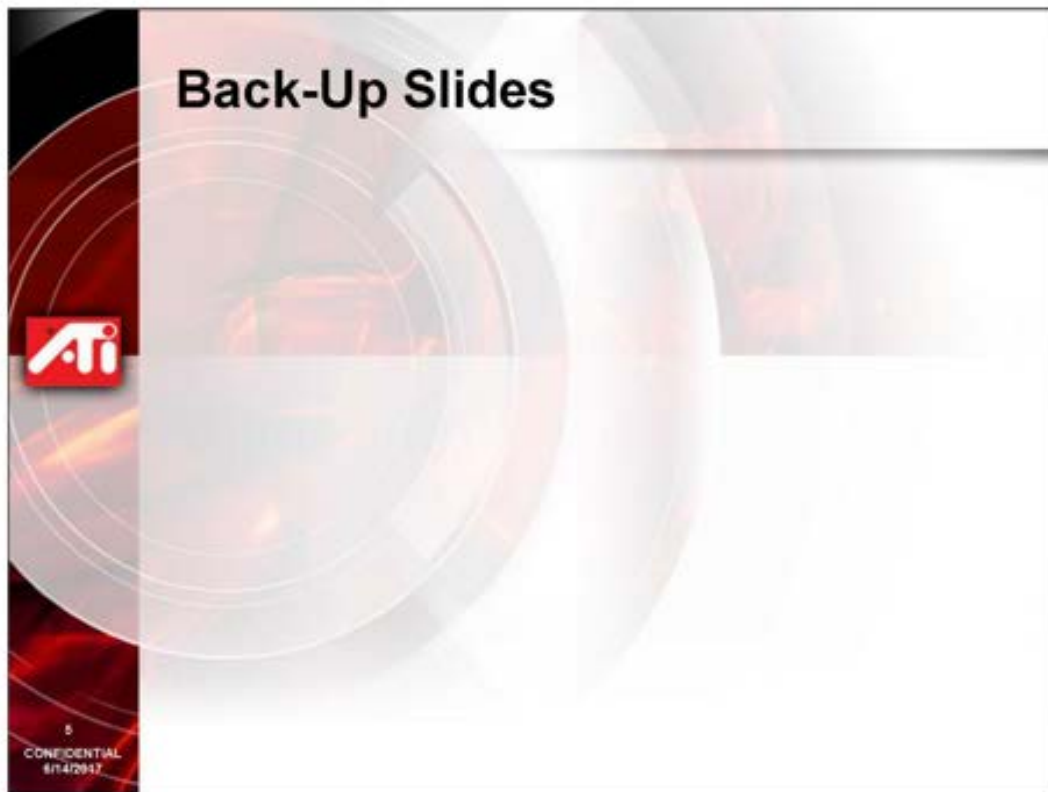
High Level Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Synthesis (n-1)	07-12-02	08-03-02	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
Netlist 4.0	02-14-03	02-07-03	02-12-03
Netlist 5.0	03-03-03	03-03-03	03-03-03
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	05-01-03
A11 Base Layers Tapeout	01-10-03	03-28-03	06-26-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	07-10-03
First Samples for Engineering		06-25-03	09-12-03
R400 First Customer Samples		07-16-03	10-03-03
A12 Tapeout		07-31-03	10-17-03
A12 Samples for Engineering		09-04-03	11-28-03
R400 Customer Samples		09-11-03	12-05-03
Product Delivery		10-04-03	12-29-03

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R400 Area Summary (2/09/03)

R400 Area Estimate (0.13)

Block	Pin Route Logic Area	Utilizatio n	Post Route Logic Unit Area	Macro Area	Total Unit Area	R400 Qty	R400 Total	Rv400 Qty	Rv400 Total	Synthesis Date
BIF (Bus Interface)	1,319,518	0.70	1,885,023	0	1,885,023	1	1,885,023	1.00	1,885,023	1/09/2003 1%
DC (Display Controller)	6,330,005	0.70	9,042,882	2,155,296	11,198,128	1	11,198,128	1.00	11,198,128	2/10/2003 5%
VIP (Video in Port)		0.70				1	0	1.00	0	2/10/2003 0%
SI (Clock Gen, T3T, D&Q, RCM)	222,089	0.70	317,242	0	317,242	1	317,242	1.00	317,242	2/10/2003 0%
CP (Control Processor)	2,433,755	0.70	3,476,790	1,586,958	5,063,748	1	5,063,748	1.00	5,063,748	2/10/2003 2%
RBBM (Register Backdoor Manager)	145,891	0.70	208,888	182,382	372,379	1	372,379	1.00	372,379	1/09/2003 0%
MB (Memory Hub)	5,383,879	0.70	7,736,541	1,270,841	8,976,482	1	8,976,482	0.75	6,732,362	2/09/2003 4%
IDCT	1,229,255	0.70	1,756,079	0	1,756,079	1	1,756,079	1.00	1,756,079	1/09/2003 1%
VDT (Vertex Group and Tessellate)	753,077	0.70	1,075,824	483,907	1,526,731	1	1,526,731	1.00	1,526,731	1/09/2003 1%
PA (Viewport X/Y/Z, Clip and Setup)	3,156,429	0.70	4,507,756	1,349,122	5,866,878	1	5,866,878	1.00	5,866,878	1/09/2003 3%
SC (Scan Converter)	3,281,794	0.70	4,688,283	1,088,714	5,786,977	1	5,786,977	1.00	5,786,977	1/09/2003 3%
SC_8 (Scan Converter)	3,483,305	0.70	4,976,150	0	4,976,150	1	4,976,150	1.00	4,976,150	1/09/2003 2%
SP (Shader Pipe)	7,143,881	0.70	10,205,230	2,724,647	12,829,877	4	51,719,508	2.00	25,868,754	2/09/2003 24%
SG (Sequences)	1,921,753	0.70	2,616,790	3,686,854	6,293,645	1	6,293,645	1.00	6,293,645	2/10/2003 3%
TP (Texture Pipe)	2,877,446	0.70	4,110,637	989,007	4,779,644	4	19,118,577	2.00	9,559,298	2/09/2003 9%
TC - TCP (Texture Periscope)	2,067,420	0.70	2,963,457	862,686	3,826,143	1	3,826,143	0.60	2,295,686	2/10/2003 3%
TC - TCR (Texture Return)	3,558,349	0.70	4,799,089	2,486,588	7,285,677	1	7,285,677	0.60	4,371,262	2/09/2003 3%
TC - TCR (Texture Return)	3,489,817	0.70	4,965,453	1,043,284	6,028,737	1	6,028,737	0.60	3,617,242	2/09/2003 3%
RB (Render Backend)	7,086,140	0.70	10,123,058	1,583,484	11,706,542	4	48,826,187	2.00	23,412,084	2/09/2003 21%
AB (Alpha Blend)	1,793,687	0.70	2,558,124	0	2,558,124	4	10,232,497	2.00	5,116,248	2/10/2003 5%
RC (Render Control)	185,091	0.70	264,287	0	264,287	1	264,287	1.00	264,287	1/07/2003 0%
SX (Shader Export)	1,268,628	0.70	1,788,042	2,307,226	4,126,271	2	8,252,541	1.00	4,126,271	2/09/2003 4%
MC (Memory Controller)	412,438	0.70	588,197	638,682	1,127,779	4	4,511,117	2.00	2,255,558	1/09/2003 2%
Analog + DFT							8,534,500		7,852,191	1/09/2003 3%
Total Core (sum)							218,258,974		140,372,314	100%

Current Pad separation (um)	50
Current Pad height (um)	350
Core inside	8.18
Core outside	14.77
Total outside	15.85
	11.85
	12.73

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