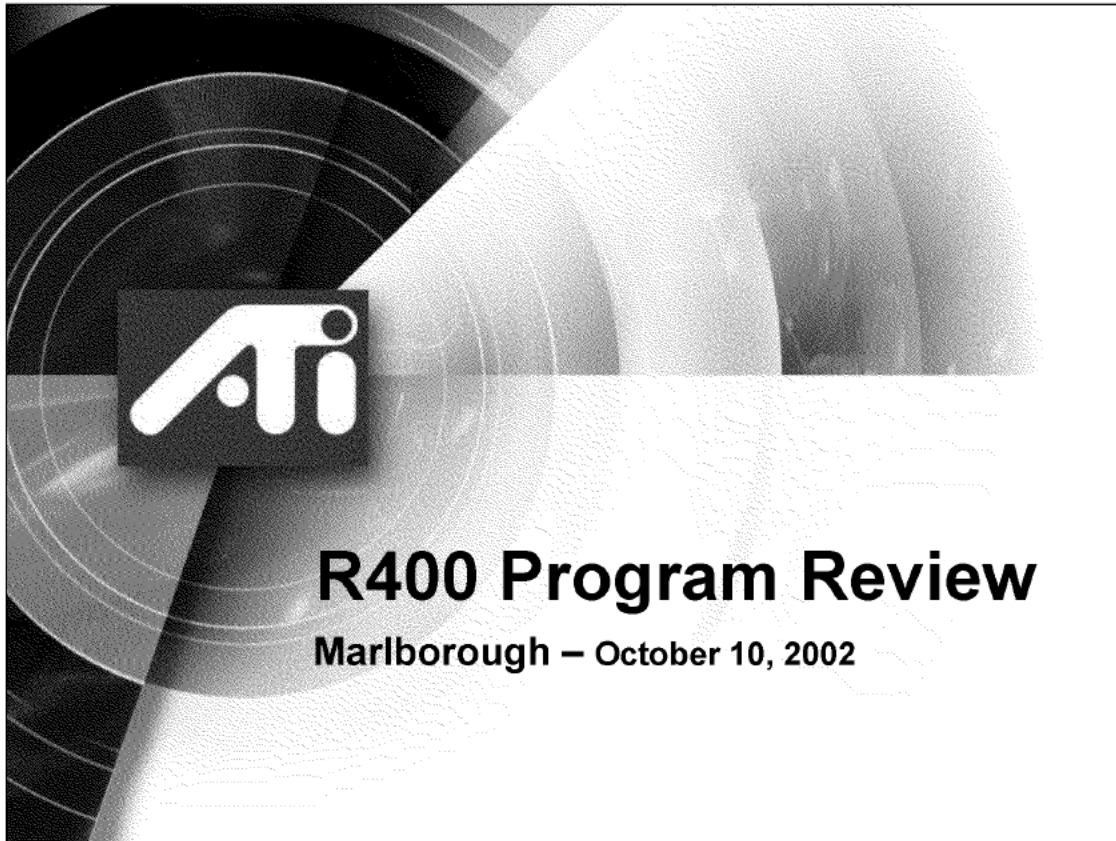




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IP – Virage HD

- ◆ Virage is under control for now
- ◆ 2.14 bit cell is out; 2.8 bit cell is in the HD memories
 - Compilers are ready because of prior customer
 - Larger RAM and it will consume more power
 - Cells design rules are less aggressive
 - Cell is not approved at TSMC, but does not appear to be a formality
 - Test chip is in the October Shuttle, but we will not see silicon till January
 - Some customization to the compiler need to be made

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IP – Virage RF

- ◆ Virage has delivered the logical views of the register file and fuse box.
- ◆ The Processor still has issues with the test and repair modes, but works in normal modes.
- ◆ Design team is beginning to enter the system into the Verilog
- ◆ We are still having issues with the compiler, but they seem to be addressed
- ◆ Virage is here tomorrow and we will review what our implementation
- ◆ Now need deal with the test and laser interface.



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IP – Virage



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STAR RF 16K		
LV-OD-LowK		
Memory FE	Shipped 19-Sep-02	
SMS Processor Shell	Shipped 19-Sep-02	
SMS Processor RTL	30-Oct-02	(pulled in from Nov 15)
Memory Compiler	30-Nov-02	

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IP – Analog

- ◆ Work has started with Toronto team to make small modifications to the cell.
- ◆ MPLL should work at 600Mhz, but 700Mhz is scary.
- ◆ Thermal Sensor was over designed to nearly a medical instrument. Going to larger increment cause the design to half its area.
- ◆ TVDAC board muxing is the path we are going and adding a pin to control the chip.

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IP - Digital

- Toronto team is looking design for the harvest fuses
- Studies about differential clocking did not pan out because of noise margin issues
- Specialized clock buffer with built in decoupling is being studied.
- Clocking will go to a wide metal with shield approach.
- Decoupling Specific cell will come out of work with done RV350. We need to find the balance between gate array and decoupling cells.
- Need a modification to the gate array cell for backside fibs.



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Pads and Pad ring

- ◆ Initial padout has been complete based on Shiva cells; this giving us a 14.2 mm die
- ◆ With the dropping of support of 2.5 volt Rams we can cut the memory cells to 65X350, which will bring the die size down to 13 ish
- ◆ The ball has been released to the board group, but the board group is to busy to comment.
- ◆ A schedule for the development of pads has been received with a final delivery date of 15-Feb-03
- ◆ John Hackenberg will working on Electrical Packaging modeling

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System Integration

- ◆ Validation of the Rom is nearly complete
- ◆ Proposal for chip personality bits and chip ids for the entire R400 family is currently under review.
- ◆ I/O ring code and pad spreadsheet is done until pad and board group.



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Netlist Generation

- ◆ Netlist was release on 3-Oct-02.
 - ◆ Synopsys ate the I/O pads, this was fixed and re-released.
 - ◆ At this point all top level functional connection should be complete.
 - ◆ Star Memories did not make it every where, but all blocks have memories
- ◆ The team is going to enter the Star memories incrementally
- ◆ 1st week of November will be the next coordinated release that includes all the DFT connections.



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DFT

- ◆ The R400 is currently 1.08M flops.
- ◆ Test Controller specification has been released is currently being implemented.
- ◆ Scan chains and pins are being assigned to blocks, looks like length will be 3500. R200 family is in the 2000's
- ◆ I/O testing is being defined.
- ◆ Virage validation of test and repair is going to be a time consuming process.



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Diagnostics

- ◆ Development and Build infrastructure is complete.
- ◆ Chip definition files have been generated off of AutoReg
- ◆ Primlib and library conversion are almost complete
- ◆ Packet Reader is currently being updated
- ◆ Base Diagnostics are just starting
- ◆ Toronto appears to be distracted on other projects currently.



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IKOS

- ◆ Non Graphic core netlist has been compiled and is 2.7 million gates
- ◆ RTL compilation seem unlikely because of problems in the IKOS compiler. Back to Gates
- ◆ Still trying to compile full chip, but held up on I/O pad problem.



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Issues

- ◆ Virage is better, but it is going to require attention throughout the program.
- ◆ Need the board group give us some cycle to deal with packaging and memory interface.
- ◆ A number of issues are not being address due lack of time and manpower.



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