

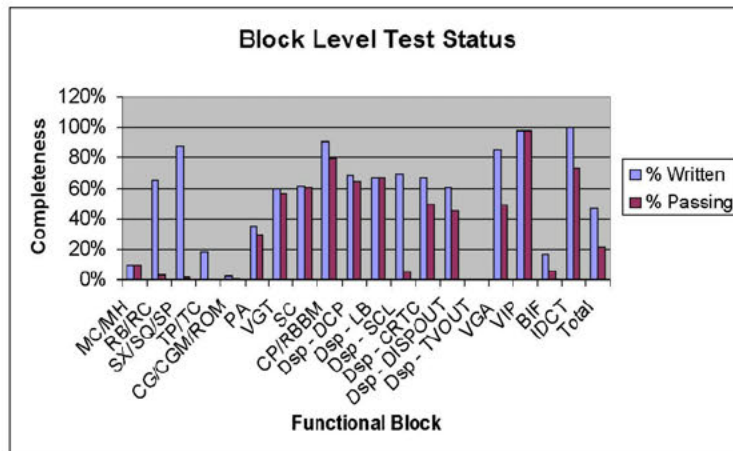
Executive Review – R400

September 16, 2002

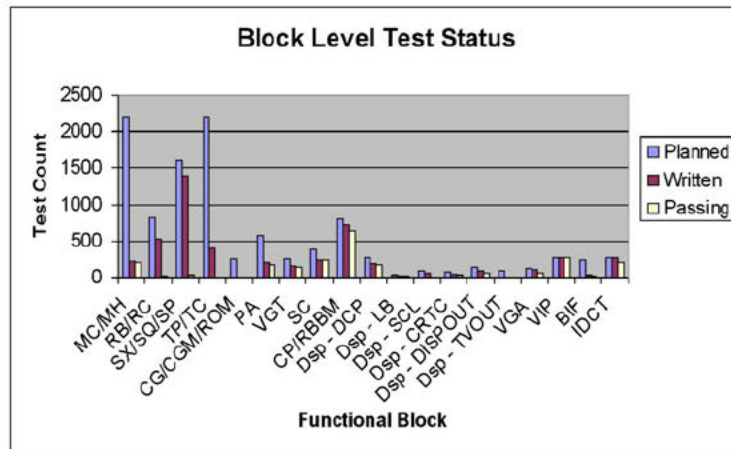
Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14.1nS)	
MC/MH	98% / 98%	9/23 - 9/16	N/A	10%	MC: 4.46; MH: 4.72	MCLK: 2.39	55 / 643
RB/RC	85% / 95%	9/30	95%	54%	RB: 8.2; RC: 2.5		16689 / 0
SX/SQ	90%	9/16 - 9/30	99%	88%	SX: 2.74; SQ: 2.5		0 / 0
SP	100%	9/16	97%		SP: 2.5		0
TP/TC	97% / 95%	9/16	92%	18%	TP: 2.55; TC: 2.5		0 / 0
CG/CGM/ROM	100%	9/16	N/A	2%	CG: 2.5; CGM: 2.5; DBG: 2.5		0
PA	100%	9/16	100%	35%	PA: 2.69		110
VGT	100%	9/16	100%	59%	VGT: 2.75		33
SC	90%	9/16	95%	61%	SC: 2.73		140
RBBM	95%	9/16	N/A	90%	RBBM: 2.95		95
CP	95%	9/16	90%		CP: 2.85		439
Display - DCP	100%	9/16	90%	65%	Display: 11	PXCLK: 2.5	8207
Display - LB	100%	9/16	100%	65%			
Display - SCL	70%	9/20	85%	65%			
Display - CRTIC	100%	9/16	80%	65%			
Display - DISPOUT	95%	9/16	65%	65%			
Display - TVOUT	100%	9/16	30%	0%			
VGA	100%	9/16	99%	85%			
VIP	100%	9/16	100%	100%			
BIF	100%	9/16	90%	15%	BIF: 4.47	BCLK: 14.1	228
IDCT	100%	9/16	97%	97%	IDCT: 4.23		2898

Block Level Test



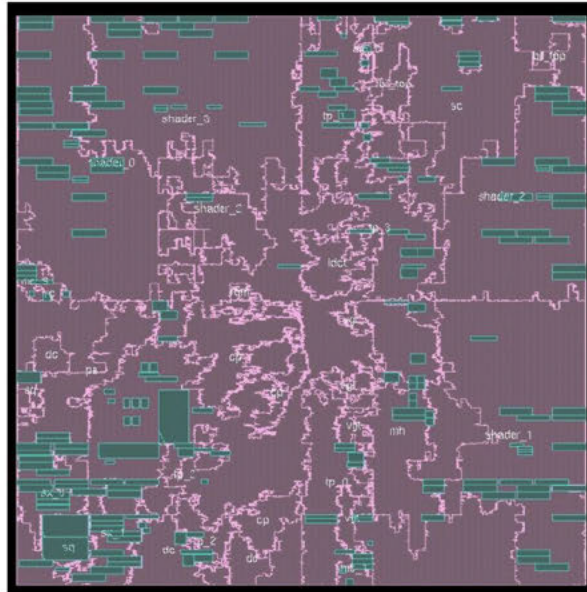
Block Level Test



Synthesis & Physical Design

- **Hardware Emulation**
 - Initial IKOS compilation has begun to attempt R400 fit into a V15M
- **Synthesis continuing ...**
 - Blocks focusing on feature complete, not timing
 - Some blocks have made significant progress
 - Working top level interconnect issues
 - Working synthesis interface into physical design
- **Physical design**
 - Working group inter-relationships SiV <=> Marlboro
 - Meeting often to synchronize teams
 - Physical Design web page under construction
- **Floorplan**
 - Initial padout done, needs to be reviewed
 - Initial netlist successfully read into SPC
 - Generated floorplan from SPC (no I/O constraint)

First R400 Floorplan - Silicon Perspectives (no I/O constraints)



Software Status (2D / MM)

- **Display Driver**

- BIOS: Design scope nearly complete, significant work identified, detailed plan is available
- CAIL: Design scope completed, ~15% implemented
- DAL/GXO: Design scope completed, significant work identified, work underway
- CMM/QS: Design scope completed, ~5% implemented
- 2D/NTx: Design scope completed, ~10% implemented
- 2D/9x: Design scope completed, ~5% implemented

- **Multimedia**

- Staffing and re-org complete; development work in progress.
- Schedule complete; under review.
- Design specs partially complete.
- MRD review meeting scheduled on Thursday.

Software Status (3D)

- **D3D**
 - BLT ~80% implemented
 - Abstract state, state cache, surface create and drawing functions ~60% implemented
 - Z/Stencil/Color ~50% implemented
 - Texture ~40% implemented
 - AA / HOS not yet begun
- **OpenGL**
 - Multiple texture and texture state 80% complete
 - IL to R400 binary translator 100% complete
 - Z, stencil and alpha operations complete
 - Vertex and fragment shaders complete
- **Compiler**
 - Compiler integrated with SSM and D3D Driver 100%
 - Triangle through compiler on emulator 100%

R400 Area Summary

R600 Area Estimate (0.13)									
Block	Pre Route Logic Area	Post Route Logic Utilization	Macro Area	Total Unit Area	R600 Qty	R600 Total	RV400 Qty	RV400 Total	
BIF (Bus Interface)	1,488,893	0 70	2,126,956	0 2,126,956	1	2,126,956	0 2,126,956	1%	
DC (Display Controller)	2,677,600	0 70	3,825,429	1,779,948	5,605,377	1	5,605,377	4%	
VIP (Video In Port)	518,393	0 70	240,527	47,892	788,419	1	788,419	1%	
CO (Clock Gen)	340,700	0 70	486,714	224,000	710,714	1	710,714	0%	
ROM (ROM and debug controller)	193,134	0 70	275,893	0 275,893	1	275,893	0 275,893	0%	
TSTC (Test Controller)	9,000	0 70	13,714	0 13,714	1	13,714	0 13,714	1%	
PC Control Processor)	3,366,639	0 70	4,802,484	1,497,341	6,306,825	1	6,306,825	4%	
REBM (Register Back Base Manager)	221,732	0 70	316,717	0 316,717	1	316,717	0 316,717	0%	
MN (Memory Nut)	3,193,174	0 70	4,591,877	875,232	5,236,909	1	5,236,909	3%	
IDC	847,452	0 70	1,216,949	84,403	1,295,040	1	1,296,049	1%	
VGT (Vertex Group and Tessellate)	816,930	0 70	1,161,129	331,693	1,498,822	1	1,498,822	1%	
PAT (Vertex Xform Clip and Stamp)	2,919,371	0 70	4,256,253	982,018	4,938,271	1	4,938,271	3%	
SC (Scan Converter)	6,558,362	0 70	9,368,074	568,187	9,937,261	1	9,937,261	6%	
SP (Shader Pipe)	3,992,420	0 70	5,043,429	2,613,709	8,317,139	4	33,269,553	21%	
SC Sequencer	1,178,584	0 70	1,683,692	2,990,049	4,094,338	1	4,094,338	2%	
TP (Texture Pipe)	2,210,219	0 70	3,165,841	881,432	3,838,973	4	15,356,881	10%	
TC (Texture Cachs)	13,014,218	0 70	18,659,739	5,322,011	23,913,761	2	23,913,761	15%	
RB (Render Backing)	3,594,000	0 70	5,125,000	1,233,000	6,358,000	2	26,432,000	16%	
CB (Render Center)	40,000	0 70	61,433	200,000	267,433	1	267,433	0%	
SX (Shader Export)	524,938	0 70	745,897	1,516,000	2,265,897	2	4,531,794	3%	
MC (Memory Controller)	543,312	0 70	776,180	426,757	1,202,937	4	4,811,056	3%	
Analog						6,545,540	2,405,934	4%	
							9,154,400		
Total Core (um)						167,108,674	102,178,849		
Current Pad separation (um)					80				
Current Pad height (um)					360				
Scribe					0.18				
Core m/mide						12.63	10.11		
Total m/mide						13.86	10.99		
RV400 in 0.09 (estimate)									
Core m/mide							8.16		
Total m/mide							9.07		

R400 Risks / Issues Summary

- **R400 Technology**
 - Proceeding with TSMC 0.13 Low-K; need to continue to monitor status
- **Chip Integration**
 - Virage STAR compiler - functional compiler delivery late
 - Impacting completeness of next netlist release
 - Chip level simulation environment stabilizing - impacting debug of non-GC blocks
- **Physical Design**
 - Resource rollovers from RV350 to R400
 - Logic Design netlist delivery to the Physical team
 - New flow will be a risk; only partially exercised on RV350
- **Software**
 - Compiler progressing (slower than planned)
 - Software MRD reviews completing; need review of integrated SW schedules
- **Overall**
 - Debug progressing slowly in some areas
 - February tapeout target.

R400 Program Schedule

<u>Task</u>	<u>Plan</u>	<u>Actual</u>	<u>Forecast</u>
Emulator Test template Complete	01-18-02	01-18-02	
GC Emulator integration – 1 triangle	02-22-02	02-21-02	
Core Emulator pixel / shader tests run	03-15-02	03-19-02	
Block Testing Begins	04-16-02	05-01-02	
GC/Chip Integration Start	05-17-02	05-15-02	
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	
First Syntheses	07-12-02	08-03-03	
Verilog Feature Complete	09-16-02		09-30-02
IKOS Emulation start	10-11-02		10-11-02
Begin early block delivery	11-08-02		11-15-02
IKOS Emulation (w/ Software) begins	11-11-02		11-11-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02		11-30-02
A11 Base Layers Tapeout	01-10-03		02-28-03
A11 Metal Layers Tapeout	01-24-03		03-14-03
First Samples for Engineering			05-23-03
A12 Tapeout			06-28-03
A12 Samples for Engineering			07-26-03
R400 Customer Samples			08-02-03
Product Delivery			09-02-03