

R400 Area Estimate (0.13)

Block	Pre Route		Post Route Logic		Macro	Total Unit	RV400		RV400	RV400
	Logic	Area	Utilization	Unit Area			R400 Qty	R400 Total		
BIF (Bus Interface)		1,488,869	0.70	2,126,956	0	2,126,956	1	2,126,956	1.00	2,126,956
DC (Display Controller)		2,677,800	0.70	3,825,429	1,779,948	5,605,377	1	5,605,377	1.00	5,605,377
VIP (Video In Port)		518,369	0.70	740,527	47,892	788,419	1	788,419	1.00	788,419
CG (Clock Gen)		340,700	0.70	486,714	224,000	710,714	1	710,714	1.00	710,714
ROM (ROM and debug controller)		193,104	0.70	275,863	0	275,863	1	275,863	1.00	275,863
TSTC (Test Controller)		9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714
CP (Control Processor)		3,366,639	0.70	4,809,484	1,497,341	6,306,825	1	6,306,825	1.00	6,306,825
RBBM (Register Backbone Manager)		221,702	0.70	316,717	0	316,717	1	316,717	1.00	316,717
MH (Memory Hub)		3,193,174	0.70	4,561,677	675,232	5,236,909	1	5,236,909	0.75	3,927,682
IDCT		847,452	0.70	1,210,646	84,403	1,295,049	1	1,295,049	1.00	1,295,049
VGT (Vertex Group and Tessellate)		816,990	0.70	1,167,129	331,693	1,498,822	1	1,498,822	1.00	1,498,822
PA(Viewport Xform,Clip and Setup)		2,979,377	0.70	4,256,253	580,018	4,836,271	1	4,836,271	1.00	4,836,271
SC (Scan Converter)		6,558,352	0.70	9,369,074	568,187	9,937,261	1	9,937,261	0.60	5,962,357
SP (Shader Pipe)		3,992,400	0.70	5,703,429	2,613,709	8,317,138	4	33,268,552	2.00	16,634,276
SQ (Sequencer)		1,178,584	0.70	1,683,692	2,380,646	4,064,338	1	4,064,338	1.00	4,064,338
TP (Texture Pipe)		2,210,279	0.70	3,157,541	681,432	3,838,973	4	15,355,891	2.00	7,677,945
TC (Texture Cache)		13,014,218	0.70	18,591,739	5,322,011	23,913,751	1	23,913,751	0.60	14,348,251
RB (Render Backend)		3,584,000	0.70	5,120,000	1,233,000	6,353,000	4	25,412,000	2.00	12,706,000
RC (Render Central)		40,000	0.70	57,143	200,000	257,143	1	257,143	1.00	257,143
SX (Shader Export)		524,928	0.70	749,897	1,516,000	2,265,897	2	4,531,794	1.00	2,265,897
MC (Memory Controller)		543,312	0.70	776,160	426,757	1,202,917	4	4,811,668	2.00	2,405,834
Analog								6,545,540		8,154,400
Total Core (um2)							157,109,574		102,178,849	

Current Pad separation (um)	80		
Current Pad height (um)	350		
Scribe	0.18		
Core mm/side		12.53	10.11
Total mm/side		13.98	10.99

RV450 in 0.09 (estimated)			
Core mm/side			8.15
Total mm/side			9.07

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14.1nS)	
MC/MH	98% / 98%	9/23 - 9/16	N/A	10%	MC:4.46; MH: 4.72	MCLK: 2.39	55 / 643
RB/RC	85% / 95%	9/30	95%	54%	RB: 8.2; RC 2.5		16689 / 0
SX/SQ	90%	9/16 - 9/30	99%	88%	SX: 2.74; SQ: 2.5		0 / 0
SP	100%	9/16	97%		SP: 2.5		0
TP/TC	97% / 95%	9/16	92%	18%	TP: 2.55; TC: 2.5		0 / 0
CG/CGM/ROM	100%	9/16	N/A	2%	CG: 2.5; CGM:2.5; DBG:2.5		0
PA	100%	9/16	100%	35%	PA: 2.69		110
VGT	100%	9/16	100%	59%	VGT: 2.75		33
SC	90%	9/16	95%	61%	SC:2.73		140
RBBM	95%	9/16	N/A	90%	RBBM: 2.95		95
CP	95%	9/16	90%		CP: 2.85		439
Display - DCP	100%	9/16	90%	65%	Display: 11	PIXCLK: 2.5	8207
Display - LB	100%	9/16	100%	65%			
Display - SCL	70%	9/20	85%	65%			
Display - CRTC	100%	9/16	80%	65%			
Display - DISPOUT	95%	9/16	65%	65%			
Display - TVOUT	100%	9/16	30%	0%			
VGA	100%	9/16	99%	85%			
VIP	100%	9/16	100%	100%			
BIF	100%	9/16	90%	15%	BIF 4.47	BCLK: 14.1	228
IDCT	100%	9/16	97%	97%	IDCT: 4.23		2898

Tests Planned	Tests Written	Tests Passing
2200	225	215
720	390	22
1600	1400	27
2200	400	0
253	5	2
584	206	175
263	156	149
389	239	236
800	722	635
280	190	179
30	20	20
97	67	5
75	50	37
150	91	68
	0	
130	110	64
275	270	270
240	40	15
279	279	204

Executive Review – R400

September 30, 2002

Block Logic Design and Timing

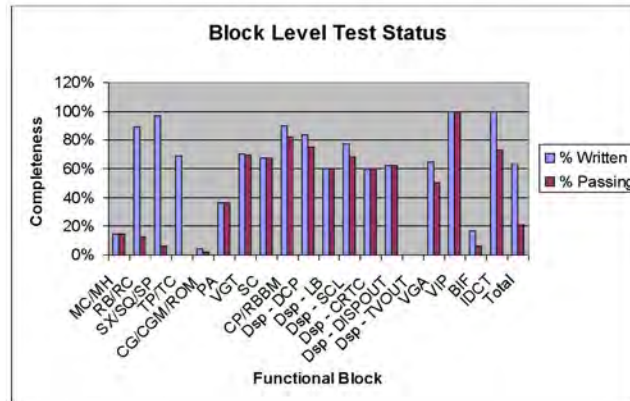
Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14.1nS)	
MC/MH*	100% / 99%	9/23 - 9/16	N/A	15%	MC: 2.5; MH: 4.41	MCLK: 2.39	0 / 14491
RB*/RC	90% / 99%	9/30	95%	89%	RB: 8.2; RC: 2.5		16689 / 0
SX*/SQ	99%	9/23	99%		SX: 2.5; SQ: 2.51		0 / 0
SP	100%	9/16	98%	97%	SP: 2.5		0
TP/TC*	99% / 95%	9/16	95%	69%	TP: 2.5; TC: 2.5		0 / 0
CG/CGM/ROM	100%	9/16	N/A	4%	CG: 2.5; CGM: 2.5; DBG: 2.5		0
PA	100%	9/16	100%	36%	PA: 2.56		143
VGT	100%	9/16	100%	70%	VGT: 2.52		0
SC*	90%	9/16	95%	68%	SC: 2.52		140
RBBM	95%	9/16	N/A		RBBM: 2.5		0
CP	95%	9/16	90%	90%	CP: 2.73		408
Display - DCP	100%	9/16	100%	84%	Display: 4.8	PIXCLK: 2.66	3608
Display - LB	100%	9/16	100%	60%	3.08		
Display - SCL	100%	9/20	90%	77%	3.94		
Display - CRTC	100%	9/16	100%	59%	2.02		
Display - DISPOUT	100%	9/16	80%	62%	2.8		
Display - TVOUT	100%	9/16	30%	0%		20.77 (TVCLK: 15ns)	
VGA	100%	9/16	99%	65%	5.12		
ViP	100%	9/16	100%	100%	2.15		
BIF	95%	10/11	90%	17%	BIF: 5.75	BCLK: 14nS; AGP: 3.5nS	242
IDCT	100%	9/16	97%	100%	IDCT: 2.52		75

Logic Design

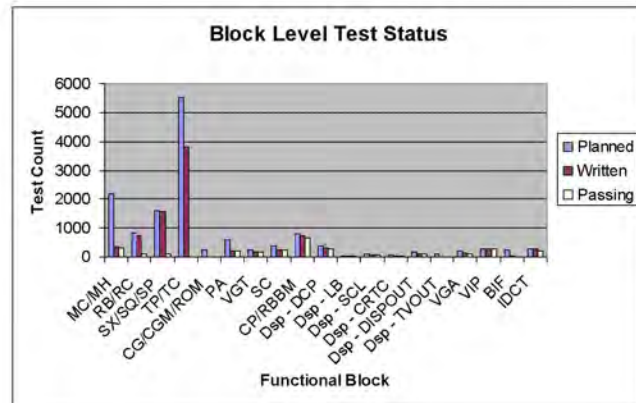
- **Virage Compilers late**
 - Impacted quality of released netlist
 - Frank Hering met with Virage last Friday
 - Expect updated schedule this week
- **Logic Design continuing ...**
 - SC/SX/RB affected by memory export architectural issue
 - TC/MH/RB affected by multisample resolve architectural issue
 - This issue resolved; working to implement
- **SQ/SX**
 - Concentrating on debug work over feature complete
 - Expecting debug to stabilize this week
 - Switching emphasis to feature complete next week

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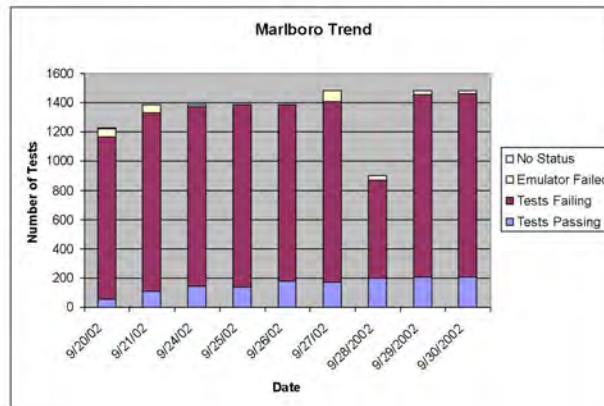
Block Level Test



Block Level Test



Marlboro Trends



Synthesis & Physical Design

- **Hardware Emulation**
 - Initial IKOS RTL compiled
 - Working on clock and display issues
- **Synthesis continuing ...**
 - RB/RC synthesis results lost due to an error
 - Expected to be delayed until Wednesday morning
- **Physical design**
 - Physical Design web page completed
- **Floorplan**
 - Next floorplan to begin this week

Software Status (2D / MM)

- Display Driver
 - BIOS: Design scope completed, BIOS and command decoder development started
 - CAIL: Design scope completed, ~28% (+13%) implemented
 - DAL/GXO: Design scope completed, ~3% (+3%) implemented
 - CMM/QS: Design scope completed, ~12% (+7%) implemented
 - 2D/NTx: Design scope completed, ~26% (+16%) implemented
 - 2D/9x: Design scope completed, ~13% (+8%) implemented
- Multimedia
 - MM sections of MRD has been reviewed and revised. Now very close to final.
 - The shader team has been having difficulty compiling code or doing blit operations in simulation. Kenneth Man and Yuri Kiselev have been sent to Marlboro for this week to work directly with the developers there.

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Software Status (3D)

- **3D Software**
 - Kevin Furrow assisted with QS-Emu setup in Toronto
 - 2D driver beginning to use emulation
 - Test coverage increasing

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R400 Area Summary

R400 Area Estimate (6.13)

Block	Pre Route Logic Area	Utilization	Post Route Logic Unit Area	Macro Area	Total Unit Area	R400 Qty	R400 Total	RV400 Qty	RV400 Total	
BF (Bus Interface)	1,488,869	0.70	2,126,966	0	2,126,966	1	2,126,966	1.00	2,126,966	1%
DC (Display Controller)	2,677,800	0.70	3,825,429	1,779,948	5,605,377	1	5,605,377	1.00	5,605,377	4%
VP (Video In Port)	518,369	0.70	740,527	47,892	788,419	1	788,419	1.00	788,419	1%
CG (Clock Gen)	340,700	0.70	485,714	224,000	710,714	1	710,714	1.00	710,714	0%
ROM (ROM and debug controller)	195,104	0.70	275,863	0	275,863	1	275,863	1.00	275,863	0%
TSTC (Test Controller)	9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714	1%
CP (Control Processor)	3,366,639	0.70	4,819,484	1,497,341	6,306,825	1	6,306,825	1.00	6,306,825	4%
RRSM (Register Backdoor Manager)	221,702	0.70	315,717	0	315,717	1	315,717	1.00	315,717	0%
MR (Memory Hub)	3,193,174	0.70	4,581,877	676,232	5,258,109	1	5,258,109	0.75	3,922,882	3%
MCJ	847,452	0.70	1,210,846	84,403	1,295,049	1	1,295,049	1.00	1,295,049	1%
VGF (Vertex Group and Tessellate)	816,090	0.70	1,187,129	331,693	1,488,822	1	1,488,822	1.00	1,488,822	1%
PA(Viewport Xform, Clip and Setup)	2,979,377	0.70	4,255,253	580,016	4,836,271	1	4,836,271	1.00	4,836,271	3%
SG (Scan Converter)	6,560,362	0.70	9,369,074	580,187	9,937,261	1	9,937,261	0.60	5,962,357	0%
SP (Shader Pipe)	3,592,400	0.70	5,103,420	2,513,709	8,317,130	1	8,317,130	2.00	16,634,276	22%
SO (Sequencer)	1,179,684	0.70	1,683,052	2,300,645	4,064,338	1	4,064,338	1.00	4,064,338	3%
TP (Texture Pipe)	2,316,274	0.70	3,293,249	506,589	3,800,238	1	3,800,238	2.00	7,600,476	10%
TC (Texture Cache)	11,382,889	0.70	16,261,266	3,766,397	20,016,682	1	20,016,682	0.60	12,010,009	13%
RI (Render Backend)	3,584,000	0.70	5,120,000	1,221,000	6,363,000	4	25,452,000	2.00	12,706,000	17%
RC (Render Control)	43,000	0.70	67,143	200,000	267,143	1	267,143	1.00	267,143	0%
SX (Shader Export)	624,908	0.70	749,887	1,516,000	2,265,887	2	4,531,794	1.00	2,265,887	3%
MC (Memory Controller)	643,312	0.70	776,160	426,752	1,202,912	4	4,811,680	2.00	2,405,840	3%
Analog							6,545,540		6,545,540	4%
Total Core (um2)							163,417,566		99,943,136	
Current Pad separation (um)							80			
Current Pad height (um)							350			
Scribe							0.12			
Core mm/side							12.39		10.00	
Total mm/side							13.90		10.00	

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R400 Risks / Issues Summary

- **Verification**
 - Tracking progress ...
- **Chip Integration**
 - Virage STAR compiler
 - Need to integrate repairable memories w/o extended disruption to design
 - Chip level simulation more stable
 - Impacting debug of non-GC blocks
- **Physical Design**
 - Resource rollovers from RV350 to R400
 - Logic Design netlist delivery delayed
- **Software**
 - Software MRD reviews completed
 - Review of SW schedules in planning

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R400 Program Schedule

Task	Plan	Actual	Forecast
Emulator Test template Complete	01-18-02	01-18-02	
GC Emulator integration – 1 triangle	02-22-02	02-21-02	
Core Emulator pixel / shader tests run	03-15-02	03-19-02	
Block Testing Begins	04-16-02	05-01-02	
GC/Chip Integration Start	05-17-02	05-15-02	
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	
First Syntheses	07-12-02	08-03-03	
Verilog Feature Complete	09-16-02		09-30-02
IKOS Emulation start	10-11-02		10-11-02
Begin early block delivery	11-08-02		11-15-02
IKOS Emulation (w/ Software) begins	11-11-02		11-11-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02		11-30-02
A11 Base Layers Tapeout	01-10-03		02-28-03
A11 Metal Layers Tapeout	01-24-03		03-14-03
First Samples for Engineering			05-23-03
A12 Tapeout			06-28-03
A12 Samples for Engineering			07-26-03
R400 Customer Samples			08-02-03
Product Delivery			09-02-03

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Executive Review – R400

October 28, 2002

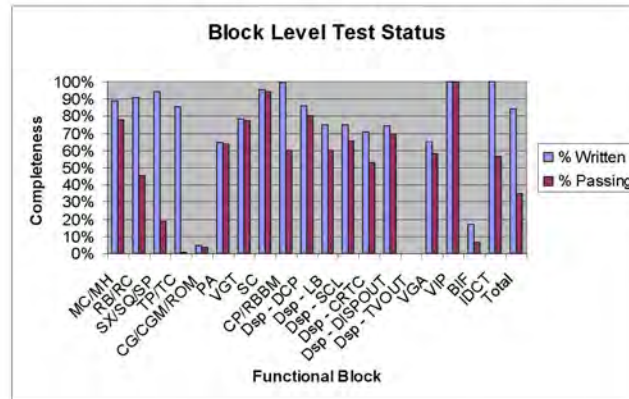
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Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	89%	MC 2.5; MH: 3.08	MC - MCLK: 1.71	0 / 1295
RB/RC	97% / 98%	10/31	95%	91%	RB: 6.3; RC: 2.5		6211 / 0
SX/SQ	Done / 97%	Done, 10/31	100%	94%	SX: 2.5; SQ: 2.51		0 / 0
SP	100%	Done	100%		SP: 2.5		0
TP/TC	95% / 95%	10/11	95%	85%	TP: 2.5; TC: 7.5		0 / ?
CG/CGM/ROM	100%	Done	N/A	5%	CG: 2.5; CGM: 2.5; DBG: 2.5		0
PA	100%	Done	100%	65%	PA: 2.79		109
VG/VT	100%	Done	100%	78%	VG/VT: 2.50		0
SC	99.44%	10/30	100%	95%	SC: 3.4		35
RBBM	100%	Done	95%	99%	RBBM: 2.5		0
CP	100%	Done	95%		CP: 3.1		408
Display - DCP	100%	Done	95%	86%	Display: 4.46	PIXCLK: 2.66	3608
Display - LB	100%	Done	100%	75%	2.6		
Display - SCL	100%	Done	90%	75%	5.01		
Display - CRTIC	100%	Done	100%	71%	2.72		
Display - DISPOUT	100%	Done	90%	74%	2.29		
Display - TVOUT	100%	Done	40%	0%		TVCLK: 22.11	
VGA	100%	Done	99%	65%	4.8		
VIP	100%	Done	100%	100%	3.47		
BIF	100%	Done	90%	17%	BIF: 2.63	BCLK: 14.53nS; AGP: 3.49nS	242
IDCT	100%	Done	97%	100%	IDCT: 2.83		

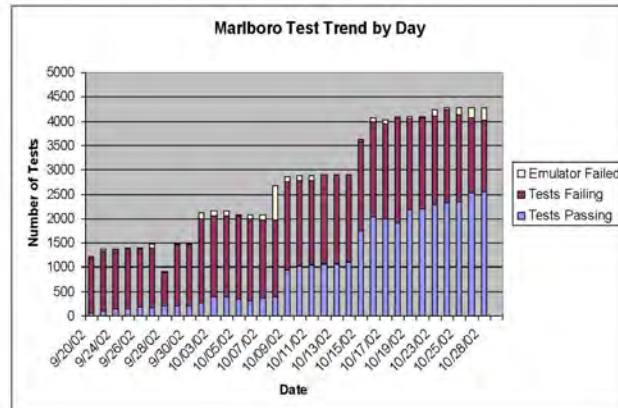
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Block Level Test Completeness



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Marlboro Blocks



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General Status

- **Full chip**
 - Full chip environment now passing tests
- **Synthesis**
 - Working through issues with netlist “N”
 - Flow and process issues are being resolved for next netlist “N+1”
 - Next netlist ...
 - STAR memories and DFT are intended to be included
 - STAR processor functionality not arriving till 10/30/02
 - Synthesis experts continually reviewing code for area optimization
 - Have identified potential areas in RB that are being pursued
- **Block Design**
 - RB currently exceeds 300K instance
 - Split into color blend unit and remainder of RB
 - Allows early delivery of RB blend for Physical Design
 - MC synthesized at 600 MHz

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General Status

- **Block delivery**
 - Stressing early block delivery to take advantage of new PD flow

Major Block	Delivery
RB (Blend)	11/18/2002
SP	11/18/2002
SX	12/2/2002
MC	12/16/2002
PA	12/16/2002
SC	12/16/2002
VGT	12/16/2002
BIF	12/20/2002
DC	12/20/2002
DCT	12/20/2002
MH	1/2/2003
CP	1/10/2003
RBBM	1/10/2003
SQ	1/15/2003
RB (Remaining)	1/15/2003
TP	1/31/2003
TC	1/31/2003

- Early block wrap-up is expected to enable physical design elements to complete sooner

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Software Status (2D)

- **CAIL**
 - Command Decoder is integrated to CAIL
- **BIOS**
 - BIOS now boots up with new command decoder and new initialization table
 - New BIOS architecture now has official name – ‘ATOM’
- **2D**
 - 8 of 12 2D legacy PM4 packets passed initial tests with Oct 22nd's QS-EMU

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Software Status (3D)

- **Compiler**
 - Compiler issues starting to clear
- **D3D**
 - Index Buffer optimization - complete
 - Polygon Offset – complete
 - Blit – complete
 - Fixed Pipe Multi-texture – complete
 - Fixed Pipe TCL – complete
 - Pixel Shader 1.0-1.4 – complete
- **OpenGL**
 - CopyPixels – complete; Drawpixels – complete
 - Cubemap and 3D Texture – complete
 - Immediate Mode – complete
 - Multi-texture – complete
 - Fragment Shader (ATI R200 Level) – complete
 - Fixed Pipe Multi-texture – complete

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R400 Risks / Issues Summary

- **R400 Technology**
 - Proceeding with TSMC 0.13 Low-K; need to continue to monitor status
- **Hardware Design & Chip Integration**
 - Validation / debug effort is the long pole
 - Virage STAR compiler - functional compiler delivery late
 - Impacted completeness netlist one; second netlist with STAR
- **Physical Design**
 - Logic Design netlist delivery continues; resolving issues
 - Early block delivery expected to realize schedule savings
- **Overall**
 - Debug progressing; full chip testing now progressing

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R400 Program Schedule

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Emulator Test template Complete	01-18-02	01-18-02	
GC Emulator integration ~ 1 triangle	02-22-02	02-21-02	
Core Emulator pixel / shader tests run	03-15-02	03-19-02	
Block Testing Begins	04-16-02	05-01-02	
GC/Chip Integration Start	05-17-02	05-15-02	
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	
First Syntheses (n-1)	07-12-02	08-03-03	
Verilog Feature Complete	09-16-02		10-31-02
Second Synthesis (n)	09-23-02	10-04-02	
IKOS Emulation start	10-11-02		11-15-02
Third Synthesis	11-01-02		11-01-02
Early block delivery	11-08-02		11-18-02
IKOS Emulation (w/ Software) begins	11-11-02		12-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02		01-31-03
A11 Base Layers Tapeout	01-10-03		03-28-03
A11 Metal Layers Tapeout	01-24-03		04-11-03
First Samples for Engineering			06-25-03
A12 Tapeout			07-31-03
A12 Samples for Engineering			09-04-03
R400 Customer Samples			09-11-03
Product Delivery			10-04-03

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Back-up Slides

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Area Summary

- Routing efficiency 70%
- Pad size (RV350) 80 μ x 350 μ
- R400 in 0.13 μ
 - Core Size 12.45mm
 - Total area (pad limited ?) ~14mm
- RV450 in 0.09 μ (estimated)
 - Core Size 8.1mm
 - Total Area 9.1mm

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CS (Clock Gen)	340,700	0.70	488,714	224,000	710,714	1	710,714	1.00	710,714
ROM (ROM and debug controller)	193,104	0.70	275,863	0	275,863	1	275,863	1.00	275,863
TSTC (Test Controller)	9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714
CP (Control Processor)	3,386,639	0.70	4,809,484	1,497,341	6,306,825	1	6,306,825	1.00	6,306,825
RBM (Register Backbone Manager)	227,702	0.70	318,717	0	318,717	1	318,717	1.00	318,717
MH (Memory Hub)	3,834,949	0.70	5,478,499	675,232	6,153,731	1	6,153,731	0.75	4,615,298
IDCT	847,452	0.70	1,210,646	84,403	1,295,049	1	1,295,049	1.00	1,295,049
VGT (Vertex Group and Tessellate)	816,990	0.70	1,167,129	331,693	1,498,822	1	1,498,822	1.00	1,498,822
PA (Viewport, Xform, Clip and Setup)	2,979,377	0.70	4,256,253	580,018	4,836,271	1	4,836,271	1.00	4,836,271
SC (Scan Converter)	6,558,352	0.70	9,389,074	568,187	9,957,261	1	9,957,261	0.60	5,962,357
SP (Shader Pipe)	3,992,400	0.70	5,703,429	2,613,709	8,317,138	4	33,288,552	2.00	16,634,276
SG (Sequencer)	1,648,958	0.70	2,355,654	2,333,799	4,689,452	1	4,689,452	1.00	4,689,452
TP (Texture Pipe)	2,305,274	0.70	3,253,249	596,989	3,850,238	4	15,560,950	2.00	7,700,475
TC (Texture Cache)	11,382,899	0.70	16,261,285	3,755,397	20,016,682	1	20,016,682	0.60	12,010,009
RB (Render Backend)	3,584,000	0.70	5,120,000	1,233,000	6,353,000	4	25,412,000	2.00	12,706,000
RC (Render Central)	40,000	0.70	57,143	200,000	257,143	1	257,143	1.00	257,143
SX (Shader Export)	524,928	0.70	749,897	1,516,000	2,265,897	2	4,531,794	1.00	2,265,897
MC (Memory Controller)	543,312	0.70	776,160	426,757	1,202,917	4	4,811,668	2.00	2,405,834
Analog							6,545,540		8,154,400
Total Core (um2)							154,959,500		101,255,888
						16,272,354			
			Current Pad separation (um)	80					
			Current Pad height (um)	350					
			Scribe	0.18					
			Core mm/side				12.45		10.06
			Total mm/side				13.33		10.94

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End

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This record has been provided in native format.

Executive Review – R400

October 15, 2002

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R400 General Information

- R400 Program Website:

http://fl_orlweb/r400/Program.html



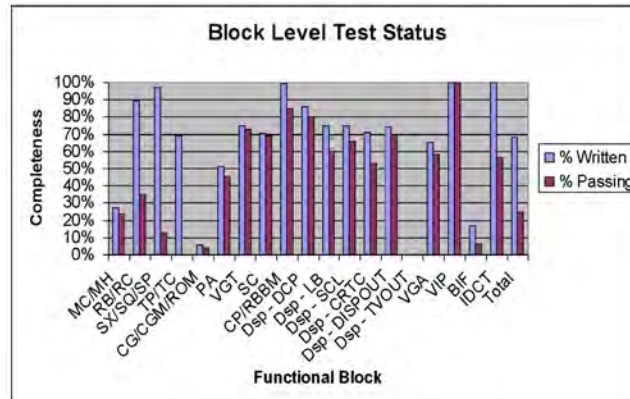
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Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (2nS) PIXCLK (2.5nS) BCLK (14nS) AGP(3.5nS) TVCLK(10nS)	
MC/MH*	100% / 99%	Done, 10/18	N/A	27%	MC: 2.5, MH: 3.30	MC - MCLK: 2.00	0 / 14491
RB*/RC	95% / 96%	10/31	95%	90%	RB: 6.3, RC: 2.5		6211 / 0
SX*/SQ	98% / 96%	10/18, 10/31	100%	97%	SX: 2.5, SQ: 2.51		0 / 0
SP	100%	Done	100%		SP: 2.5		0
TP/TC*	96% / 96%	10/18	95%	89%	TP: 2.5, TC: 7.5		0 / -
CG/CGM/ROM	100%	Done	N/A	6%	CG: 2.5, CGM: 2.5, DBG: 2.5		0
PA	100%	Done	100%	51%	PA: 2.79		109
VG	100%	Done	100%	75%	VG: 2.50		0
SC*	>95%	10/15	>97%	71%	SC: 3.4		35
RBBM	95%	10/31*	N/A	99%	RBBM: 2.5		0
CP	95%	10/31*	95%		CP: 3.1		408
Display - DCP	100%	Done	95%	86%	Display: 4.46	PIXCLK: 2.66	3608
Display - LB	100%	Done	100%	75%	2.6		
Display - SCL	100%	Done	90%	75%	5.01		
Display - CRT	100%	Done	100%	71%	2.72		
Display - DISPOUT	100%	Done	90%	74%	2.29		
Display - TVOUT	100%	Done	40%	0%		TVCLK: 22.11	
VGA	100%	Done	99%	65%	4.8		
VIP	100%	Done	100%	100%	3.47		
BIF	95%	10/11	90%	17%	BIF: 2.63	BCLK: 14.53nS, AGP: 3.49nS	242
IDCT	100%	Done	97%	100%	IDCT: 2.63		

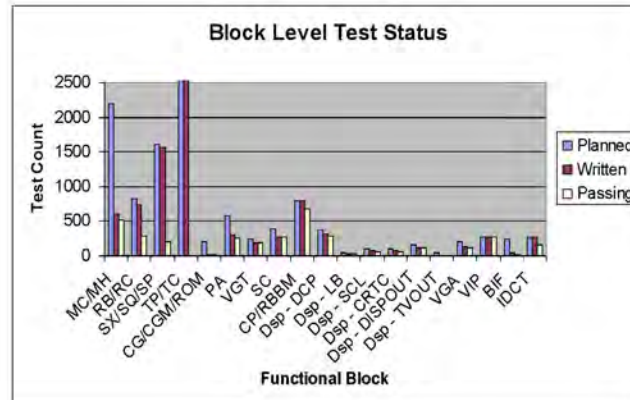
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Block Level Test Completeness



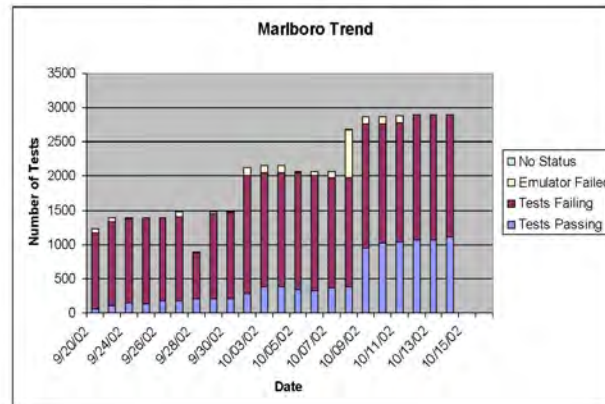
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Block Level Test Status



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Marlboro Blocks



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General Status

- **Hardware Emulation**
 - IKOS meeting this week to review status and tasks
- **Synthesis**
 - Netlist delivery completed 10/4/02
 - Next netlist target is 11/01/02
 - With STAR memories and DFT included
 - All blocks within 10% of clock speed goals
 - Synthesis experts reviewing code for area optimization
- **Physical design**
 - Reviewing instance counts and block sizes
 - 5.6 million instances in the R400; implies 18 to 20 tiles
 - Clock constraints nearly complete; expecting more info from display today
 - Preliminary Clock diagram complete

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Mitigation Plans

- Near term goals:
 - October goals for block tests passing have been set for MC/MH, RB/RC, SP/SX/SQ & TP/TC
 - Goal of 4250 tests passing by end of October (~40% of Marl direct tests)
 - Similar goals will continue for following months
- Block delivery
 - Stressing early block delivery; do not want to impact this
 - Early block wrap-up enables physical design elements to complete
 - VGT, SP, MC, MH are early candidates (3-5 weeks away)
 - Resource of completed blocks re-allocated to long pole design areas
- Freeing up senior designers from Orlando and Marlboro to help drive bug triage in Marlboro

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Software Status (2D / MM)

- QS-EMU for 2D
 - 2D Rendering is working
 - PIO Mode is working
- BIOS
 - Command decoder is successfully built and linked to CAIL
 - VGA core BIOS is ready and adding init table support is under way
- Multimedia
 - All master schedules were refreshed to include recent MRD changes and work items from MMC 8.5 MRD.
 - R300/RV250 issues caused a late start in some instances.
 - There are some synchronization issues between the MM team's schedules which need to be resolved.

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Software Status (3D)

- **D3D**
 - Index Buffer optimization - complete
 - Polygon Offset – complete
 - Blit – complete
 - Fixed Pipe Multi-texture – complete
 - Fixed Pipe TCL – complete
 - Pixel Shader 1.0-1.4 – complete
- **OpenGL**
 - CopyPixels – complete; Drawpixels – complete
 - Cubemap and 3D Texture – complete
 - Immediate Mode – complete
 - Multi-texture – complete
 - Fragment Shader (ATI R200 Level) – complete
 - Fixed Pipe Multi-texture – complete
- **Compiler**
 - Rotating single textured triangle
 - Compiler fixing a couple key bugs

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R400 Risks / Issues Summary

- **R400 Technology**
 - Proceeding with TSMC 0.13 Low-K; need to continue to monitor status
- **Hardware Design & Chip Integration**
 - Validation / debug effort is the long pole
 - Virage STAR compiler - functional compiler delivery late
 - Impacted completeness netlist one; release second netlist with STAR
 - Chip level simulation environment stabilizing - debug of non-GC blocks
- **Physical Design**
 - Logic Design netlist delivery continues, SVC needs constraint file
 - Early block delivery needs to occur
- **Software**
 - BIOS is new (re-architected)
 - DAL/GXO: new Display Controller; amount of software work is large.
 - Compiler progress / bug fixing has gated driver development
- **Overall**
 - Debug progressing slowly in some areas
 - Impact to tapeout target.

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R400 Program Schedule

Task	Plan	Actual	Forecast
Emulator Test template Complete	01-18-02	01-18-02	
GC Emulator integration ~ 1 triangle	02-22-02	02-21-02	
Core Emulator pixel / shader tests run	03-15-02	03-19-02	
Block Testing Begins	04-16-02	05-01-02	
GC/Chip Integration Start	05-17-02	05-15-02	
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	
First Syntheses (n-1)	07-12-02	08-03-03	
Verilog Feature Complete	09-16-02		10-31-02
Second Synthesis (n)	09-23-02	10-04-02	
IKOS Emulation start	10-11-02		11-15-02
Third Synthesis	11-01-02		11-01-02
Early block delivery	11-08-02		11-15-02
IKOS Emulation (w/ Software) begins	11-11-02		12-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02		01-30-03
A11 Base Layers Tapeout	01-10-03		04-30-03
A11 Metal Layers Tapeout	01-24-03		05-14-03
First Samples for Engineering			07-23-03
A12 Tapeout			08-28-03
A12 Samples for Engineering			09-25-03
R400 Customer Samples			10-02-03
Product Delivery			11-01-03

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Back-up Slides

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Area Summary

- Routing efficiency 70%
- Pad size (RV350) 80 μ x 350 μ
- R400 in 0.13 μ
 - Core Size 12.45mm
 - Total area (pad limited ?) ~14mm
- RV450 in 0.09 μ (estimated)
 - Core Size 8.1mm
 - Total Area 9.1mm

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R400 Area Summary

R400 Area Estimate (0.13)									
Block	Pre Route Logic Area	Utilizati on	Post Route Logic Unit Area	Macro Area	Total Unit Area	R400 Qty	R400 Total	RV400 Qty	RV400 Total
BIF (Bus Interface)	1,488,869	0.70	2,126,956	0	2,126,956	1	2,126,956	1.00	2,126,956
DC (Display Controller)	2,677,800	0.70	3,825,429	1,779,948	5,605,377	1	5,605,377	1.00	5,605,377
VP (Video In Port)	518,359	0.70	740,527	47,852	788,419	1	788,419	1.00	788,419
CS (Clock Gen)	340,700	0.70	488,714	224,000	710,714	1	710,714	1.00	710,714
ROM (ROM and debug controller)	193,104	0.70	275,863	0	275,863	1	275,863	1.00	275,863
TSTC (Test Controller)	9,600	0.70	13,714	0	13,714	1	13,714	1.00	13,714
CP (Control Processor)	3,386,639	0.70	4,809,484	1,497,341	6,306,825	1	6,306,825	1.00	6,306,825
RBM (Register Backbone Manager)	227,702	0.70	318,717	0	318,717	1	318,717	1.00	318,717
MH (Memory Hub)	3,834,949	0.70	5,478,499	675,232	6,153,731	1	6,153,731	0.75	4,615,298
IDCT	847,452	0.70	1,210,646	84,403	1,295,049	1	1,295,049	1.00	1,295,049
VGT (Vertex Group and Tessellate)	816,990	0.70	1,167,129	331,693	1,498,822	1	1,498,822	1.00	1,498,822
PA (Viewport, Xform, Clip and Setup)	2,979,377	0.70	4,256,253	580,018	4,836,271	1	4,836,271	1.00	4,836,271
SC (Scan Converter)	6,558,352	0.70	9,389,074	568,187	9,957,261	1	9,957,261	0.60	5,962,357
SP (Shader Pipe)	3,992,400	0.70	5,703,429	2,613,709	8,317,138	4	33,288,552	2.00	16,634,276
SG (Sequencer)	1,648,958	0.70	2,355,654	2,333,799	4,689,452	1	4,689,452	1.00	4,689,452
TP (Texture Pipe)	2,305,274	0.70	3,253,249	596,989	3,850,238	4	15,560,950	2.00	7,700,475
TC (Texture Cache)	11,382,899	0.70	16,261,285	3,755,397	20,016,682	1	20,016,682	0.60	12,010,009
RB (Render Backend)	3,584,000	0.70	5,120,000	1,233,000	6,353,000	4	25,412,000	2.00	12,706,000
RC (Render Central)	40,000	0.70	57,143	200,000	257,143	1	257,143	1.00	257,143
SX (Shader Export)	524,928	0.70	749,897	1,516,000	2,265,897	2	4,531,794	1.00	2,265,897
MC (Memory Controller)	543,312	0.70	776,160	426,757	1,202,917	4	4,811,668	2.00	2,405,834
Analog							6,545,540		8,154,400
Total Core (um2)							154,959,500		101,255,888
						16,272,354			
			Current Pad separation (um)	80					
			Current Pad height (um)	350					
			Scribe	0.18					
			Core mm/side				12.45		10.06
			Total mm/side				13.33		10.94

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End

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Executive Review – R400

November 11, 2002

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Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	91%	MC:2.5; MH: 3.08	MC - MCLK: 1.71	0 / 1295
RB/RC	100%	Done	99%	91%	RB: 6.2; RC: 2.5		12155 / 0
SX/SQ	100%	Done	100%	94%	SX: 2.5; SQ: 2.51		0 / 0
SP	100%	Done	100%		SP: 2.5		0
TP/TC	100%	Done	99%	85%	TP: 2.5; TC: 7.5		0 / ?
CG/CGM/ROM	100%	Done	N/A	5%	CG: 2.5; CGM:2.5; DBG:2.5		0
PA	100%	Done	100%	72%	PA: 3.04		142
VGt	100%	Done	100%	79%	VGt: 2.55		0
SC	100%	Done	100%	97%	SC: 3.85		1150
RBBM	100%	Done	95%	100%	RBBM: 2.5		0
CP	100%	Done	95%		CP: 3.1		408
Display - DCP	100%	Done	95%	99%	Display: 4.48	PIXCLK: 2.66	3669
Display - LB	100%	Done	100%	100%	2.6		
Display - SCL	100%	Done	90%	88%	5.01		
Display - CRTc	100%	Done	100%	98%	2.72		
Display - DISPOUT	100%	Done	90%	100%	2.29		
Display - TVOUT	100%	Done	40%	0%		TVCLK:10.4	
VGA	100%	Done	99%	100%	4.8		
VIP	100%	Done	100%	100%	3.37		
BIF	100%	Done	90%	17%	BIF: 4.75	BCLK: 14.53nS, AGP:3.49nS	242
IDCT	100%	Done	97%	100%	IDCT: 2.72		

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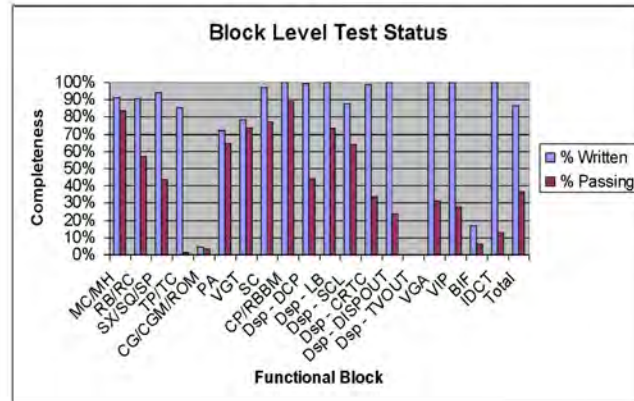
General Status

- **Verification Results**

- Regressions continuing to trend upward
 - SP/RB blender nearing end of functional verification
 - Random testing underway on memory blocks for 2 weeks
 - Randoms started on RB/RC over the weekend
 - Randoms running on PA
 - TP started to turn the corner on verification blockage
- Toronto experienced some simulation issues with Virage memory
 - Some artificial test loss
- Full chip environment passing tests
 - Beginning Real Time verification debug in full chip
 - Goal for this month is to get a wider spectrum of tests passing at GC and full chip

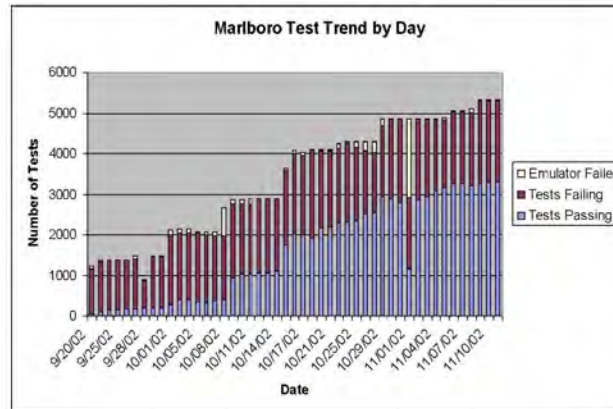
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Block Level Test Completeness



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Marlboro Blocks



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General Status

- **Synthesis**

- Maneesh Bhide working with with netlist “N”
 - Incorporate learnings and PD feedback into netlist delivery
 - STAR processor and fusebox functionality delivered 10/31/02
 - Working through learning curve with SMS
- Maneesh will travel to Marlboro for R400 SPC collaboration this week
- Synthesis experts reviewing code for area optimization
 - Area bloat identified in SP and RB
 - Reviews last week identified many area optimizations
 - These are being put in as we progress through next few weeks
 - Reviews continue, not yet complete

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General Status

• R400 Pads

- Met with with Joe Macri at SVC 11/07/02
 - Most memory pad to MC interface questions resolved.
 - The few remaining issues will be resolved as work progresses.
- Reviewed memory specifications for GDDR3
 - Required clarifications and updates for the spec discussed and identified.
 - Joe will resolve these issues with DRAM vendors this week
 - RAM models to be delivered from Joe Macri
- Reviewed RV350 to R400 pad modifications (at circuit level)
 - Resolved which portions of the design belong in or out of the pads
- Reviewed Memory Controller
 - Continuing with asynchronous MC to pad interface
 - Detailed implementation reviewed
- System modelling and timing methodology reviewed and discussed

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Software Status (2D)

- **CAIL**
 - Continuing integration with BIOS (using R300)
 - Waiting for R300 BIOS with new ATOM header
- **BIOS**
 - Cleaning up R400 base source
 - New BIOS architecture now has official name – ‘ATOM’
- **2D**
 - Initial run of DCT GDI with QS-EMU is done
 - 32bpp, 16bpp and 8bpp
 - Various issues are under investigation
 - Implementation of AAFONT and AlphaBlend 2D packets is delayed

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Software Status (3D)

- **Compiler**
 - Assembler complete, into bug fixing
- **D3D**
 - Z stencil and fast clear 50% complete
 - Fast color clear 50% complete
 - Blit – complete
- **OpenGL**
 - GL Read Pixels 30% complete
 - Multi Sample AA 50 % complete
 - Line stipple complete

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R400 Risks / Issues Summary

- **Hardware Design & Chip Integration**
 - Validation / debug effort is the long pole
 - Virage STAR compiler
 - Continue to work through implementation issues
 - Test strategy in definition
- **Physical Design**
 - Working through initial floorplanning over next couple weeks
 - Feedback and incorporation of learnings into process
- **Software**
 - Work through staggered netlist delivery and IKOS functionality

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R400 Program Schedule

Task	Plan	Last	Current
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration ~ 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-03	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	11-15-02	11-15-02
Third Synthesis	11-01-02	11-15-02	11-15-02
Early block delivery	11-08-02	11-18-02	11-18-02
IKOS Emulation (w/ Software) begins	11-11-02	12-16-02	12-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	01-31-03
A11 Base Layers Tapeout	01-10-03	03-28-03	03-28-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	04-11-03
First Samples for Engineering		06-25-03	06-25-03
A12 Tapeout		07-31-03	07-31-03
A12 Samples for Engineering		09-04-03	09-04-03
R400 Customer Samples		09-11-03	09-11-03
Product Delivery		10-04-03	10-04-03

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Executive Review – R400

November 25, 2002

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Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	94%	MC 2.5, MH 2.78	MC - MCLK 1.71	0 / 1295
RB/RC	100%	Done	99%	90%	RB 6.2, RC 2.25		12155 / 0
SX/SQ	100%	Done	100%		SX 2.5, SQ 2.51		0 / 0
SP	100%	Done	100%	94%	SP 2.5		0
TP/TC	100%	Done	99%	85%	TP 2.5, TC 7.5		0 / 7
CG/CGM/ROM	100%	Done	N/A	6%	CG 2.5, CGM 2.5, DBG 2.5		0
PA	100%	Done	100%	74%	PA 2.79		142
VG/VT	100%	Done	100%	88%	VG/VT 2.5		0
SC	100%	Done	100%	97%	SC 2.88		1150
RBBM	100%	Done	95%		RBBM 2.25		0
CP	100%	Done	95%	100%	CP 2.83		408
Display - DCP	100%	Done	95%	100%	Display 4.57	PIXCLK 2.66	3669
Display - LB	100%	Done	100%	100%	2.6		
Display - SCL	100%	Done	90%	99%	5.01		
Display - CRTIC	100%	Done	100%	99%	2.72		
Display - DISPOUT	100%	Done	90%	100%	2.29		
Display - TVOUT	100%	Done	40%	10%		TVCLK 10.4	
VGA	100%	Done	99%	100%	4.8		
VIP	100%	Done	100%	100%	3.37		
BIF	95%	?	90%	17%	BIF 2.5	BCLK 14.53nS, AGP 3.49nS	242
IDCT	100%	Done	97%	100%	IDCT 2.5		

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General Status

- **Design/Synthesis**

- Reviews have identified area optimizations in SP/RB
 - Progress being made implementing reductions
 - Area reduction work has added ~ 7 –10 days on SP and RB Blender

- **Verification Results**

- Regressions continuing to trend upward
 - SP/RB blender nearing end of functional verification
 - Random testing continues on MC/MH, RB/RC and PA blocks
 - Running ~19 days behind plan
- Toronto experienced simulation issues with Virage memory implementation
 - Delayed regressions; working through issues

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SP / RB Blend Blocks

- **SP Block**

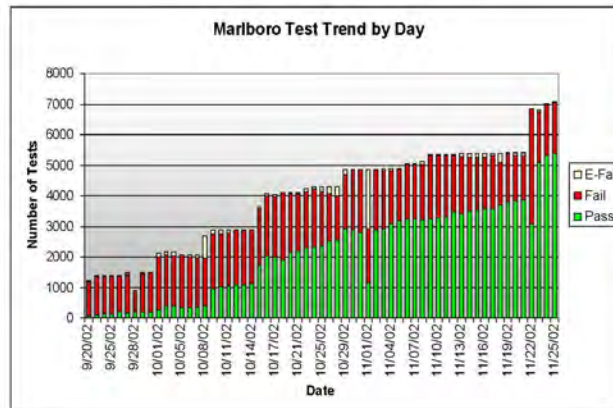
- Review of test plan last week for thoroughness
- Team identified ~300 additional tests
- Added over the weekend – most new tests passed
 - Corner cases and NaN tests all that remain
- Area reduction work has added ~ 7 days to SP schedule

- **RB Block**

- Regressions passing except for Fog, Stencil and Z tests
- Blender is done except for a few individual tests
- RB had largest area bloat
 - Much time spent last two weeks to recover area
 - One third area reduction incorporated, one third in-flight and the balance is identified but not implemented
 - Area reduction opportunities still being examined

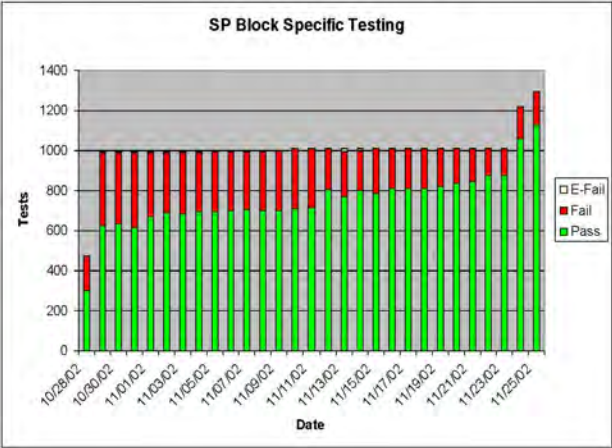
ATI Confidential and Proprietary

Marlboro Blocks



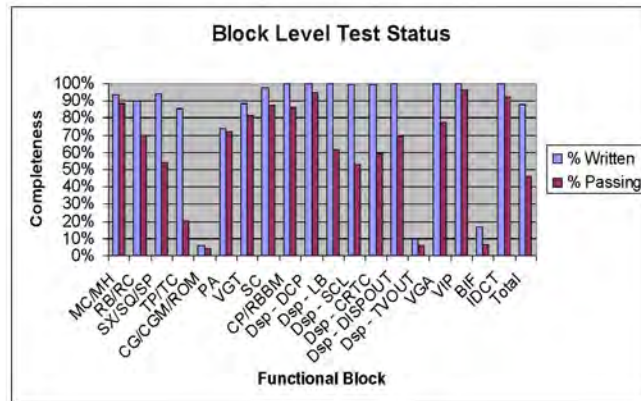
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SP Block Level Test



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Block Level Test Completeness



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General Status

- **Floorplanning**
 - Generated first floorplan with SPC last Friday
 - Congestion driven placement used
 - Found problems with I/O pads
 - Work will continue through this week
 - SiV team in Marlboro this week to work jointly
- **PD laying out blocks w/out floorplan**
 - Generating improved wireload models
 - Learning block characteristics

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General Status

- **Block delivery**
 - Stressing early block delivery to take advantage of new PD flow

Major Block	Plan	Last	Current
RB (Blend)	11/18/2002	11/18/2002	12/2/2002
SP	11/18/2002	11/18/2002	12/2/2002
SX	12/2/2002	12/2/2002	12/16/2002
MC	12/16/2002	12/16/2002	12/16/2002
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
BIF	12/20/2002	12/20/2002	1/15/2003
DC	12/20/2002	12/20/2002	1/15/2003
DCT	12/20/2002	12/20/2002	1/15/2003
MH	1/2/2003	1/2/2003	1/2/2003
CP	1/10/2003	1/10/2003	1/10/2003
RBBM	1/10/2003	1/10/2003	1/10/2003
SQ	1/15/2003	1/15/2003	1/15/2003
RB (Remaining)	1/15/2003	1/15/2003	1/15/2003
TP	1/31/2003	1/31/2003	1/31/2003
TC	1/31/2003	1/31/2003	1/31/2003

- Early block wrap-up is expected to enable physical design elements to complete sooner

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R400 Risks / Issues Summary

- **Hardware Design & Chip Integration**
 - Validation / debug effort is the long pole
 - Virage STAR compiler
 - Continue to work through implementation issues
 - Impacting block completion because of lack of clarity in documentation and engineering “on the fly”
 - Impact from RV280 has been substantial in the last two weeks
- **Physical Design**
 - Working through initial floorplanning with SPC tool
 - Delivery of early blocks critical
- **Software**
 - Worked through staggered netlist delivery and IKOS functionality

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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration ~ 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-03	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	11-15-02	TBD
Third Synthesis	11-01-02	11-15-02	12-06-02
Early block delivery	11-08-02	11-18-02	12-02-02
IKOS Emulation (w/ Software) begins	11-11-02	12-16-02	12-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	01-31-03
A11 Base Layers Tapeout	01-10-03	03-28-03	03-28-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	04-11-03
First Samples for Engineering		06-25-03	06-25-03
A12 Tapeout		07-31-03	07-31-03
A12 Samples for Engineering		09-04-03	09-04-03
R400 Customer Samples		09-11-03	09-11-03
Product Delivery		10-04-03	10-04-03

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Executive Review – R400

December 9, 2002

[DateTime]

R400 Executive Reviews
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Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.5nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	94%	MC 2.5, MH 2.78	MC - MCLK 1.71	0/1285
RB/RC	100%	Done	99%	90%	RB 6.2, RC 2.25		12155 / 0
SX/SQ	100%	Done	100%		SX 2.5, SQ 2.51		0 / 0
SP	100%	Done	100%	100%	SP 2.5		0
TP/TC	100%	Done	99%	85%	TP 2.5, TC 7.5		0 / 7
CG/CGM/ROM	100%	Done	N/A	6%	CG 2.5, CGM 2.5, DBG 2.5		0
PA	100%	Done	100%	78%	PA 2.79		142
VG/VT	100%	Done	100%	88%	VG 2.5		0
SC	100%	Done	100%	81%	SC 2.88		1150
RBBM	100%	Done	95%		RBBM 2.25		0
CP	100%	Done	95%	100%	CP 2.83		408
Display - DCP	100%	Done	95%	100%	Display 4.57	PIXCLK: 2.66	3669
Display - LB	100%	Done	100%	100%	2.6		
Display - SCL	100%	Done	90%	100%	5.01		
Display - CRTIC	100%	Done	100%	100%	2.72		
Display - DISPOUT	100%	Done	90%	100%	2.29		
Display - TVOUT	100%	Done	40%	100%		TVCLK 10.4	
VGA	100%	Done	99%	100%	4.8		
VIP	100%	Done	100%	100%	3.37		
BIF	95%	?	90%	17%	BIF 2.5	BCLK 14.53nS, AGP 3.49nS	242
IDCT	100%	Done	97%	100%	IDCT 2.5		

[Date/Time]

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2

General Status

- **Design/Synthesis**
 - BIF resource continues to be on RV280 work
 - Focused on debug over the last two weeks
 - RB Blender split out as a new top level block
 - SC block split into SC and SC_B top level blocks
 - Timing and area reduction work continuing
- **Verification Results**
 - Regressions continuing to trend upward
 - Many changes are being processed
- **Physical Design**
 - SiV Team in Marlboro 11/25, 11/26 for discussions
 - MC logic design lead in SiV 12/3, 12/4
 - Finalized pad interface
 - Logic Design and Physical Design working out respective issues
 - PD team working on netlist 2 of the following blocks: CP, SC, MH, SP, DC
 - Floorplan proposal generated, R400 architect working with PD team today
 - Netlist 3.0 candidate on 12/11
 - Expect to identify and work out netlist problems with PD and IKOS teams
 - Expected clean by 12/18

[DateTime]

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SP / RB Blend Blocks

- **SP Block**

- Code coverage analysis completed, all tests written and released
- Debug of corner cases has revealed architectural issues with mathematical corner cases
 - Microsoft WHQL and IEEE are in contention at times
 - Architectural evaluations today for resolution
 - R400 program requires this evaluation
- Other than above issues, verification complete
 - Remaining failing tests are emulator issues

- **RB Blend (AB Block)**

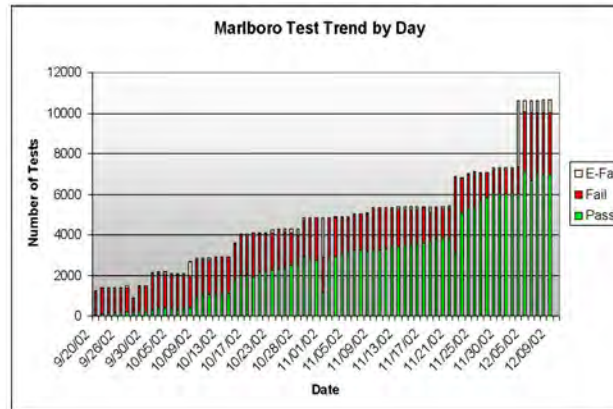
- Split completed from original RB Block this weekend
- Working through clean-up issues
- Release will occur with Netlist 3.0
- Passing in block regressions
 - Fog tests expected to pass in this night's release

[DateTime]

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Marlboro Blocks

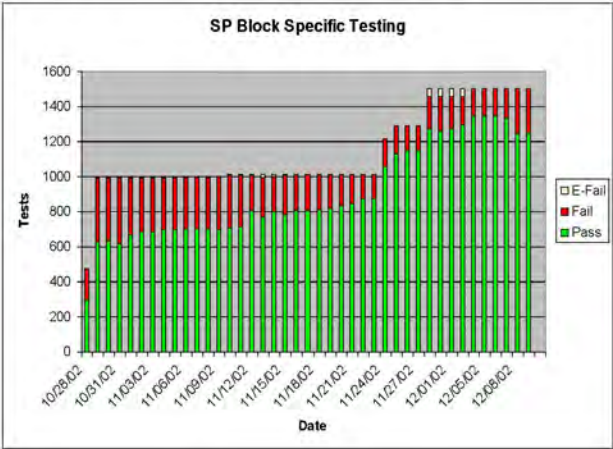


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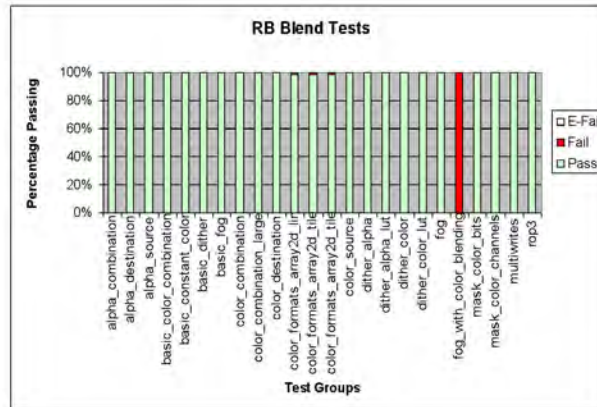
SP Block Level Test



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RB Blend

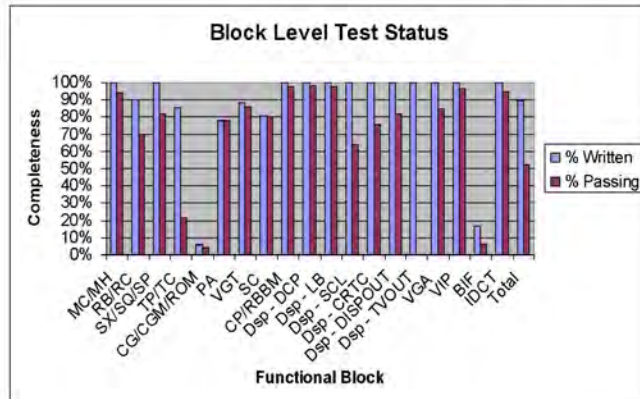


[DateTime]

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Block Level Test Completeness



[DateTime]

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General Status

- **Block delivery**
 - RB Blend (now the AB block) is day to day, complete with Netlist 3.0
 - SP resolving corner case issues, SX delayed behind SP

Major Block	Plan	Last FC	Current FC
RB Blend (AB Block)	11/18/2002	12/2/2002	12/18/2002
SP	11/18/2002	12/2/2002	1/3/2003
SX	12/2/2002	12/16/2002	1/3/2003
MC	12/16/2002	12/16/2002	12/16/2002
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
BIF	12/20/2002	1/15/2002	1/15/2002
DC	12/20/2002	1/15/2002	1/15/2002
DCT	12/20/2002	1/15/2002	1/15/2002
MH	1/2/2003	1/2/2003	1/2/2003
CP	1/10/2003	1/10/2003	1/10/2003
RBBM	1/10/2003	1/10/2003	1/10/2003
SQ	1/15/2003	1/15/2003	1/15/2003
RB (Remaining)	1/15/2003	1/15/2003	1/15/2003
TP	1/31/2003	1/31/2003	1/31/2003
TC	1/31/2003	1/31/2003	1/31/2003

[DateTime]

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R400 Risks / Issues Summary

- **Hardware Design & Chip Integration**
 - Validation / debug effort continue to be the long pole
 - SP issues to be resolved (meeting this afternoon)
 - Impact from RV280 still being felt on BIF
- **Physical Design**
 - Delivery of netlist 3.0 to physical design team by logic design
- **Software**
 - Netlist 3.0 planned for IKOS work

[DateTime]

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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-03	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	11-15-02	01-04-02
Third Synthesis	11-01-02	11-15-02	12-18-02
Early block delivery begins	11-08-02	11-18-02	12-16-02
IKOS Emulation (w/ Software) begins	11-11-02	12-16-02	01-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	01-31-03
A11 Base Layers Tapeout	01-10-03	03-28-03	03-28-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	04-11-03
First Samples for Engineering		06-25-03	06-25-03
A12 Tapeout		07-31-03	07-31-03
A12 Samples for Engineering		09-04-03	09-04-03
R400 Customer Samples		09-11-03	09-11-03
Product Delivery		10-04-03	10-04-03

[DateTime]

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Executive Review – R400

December 16, 2002

[DateTime]

R400 Executive Reviews
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1

Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.25nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	96%	MC 2.5, MH 3.01	MC - MCLK 1.71	0 / 218
AB/RB/RC	100%	Done	100%	91%	AB 2.69, RB 5.38, RC 2.25		247 / 10275 / 0
SX/SQ	100%	Done	100%	97%	SX 3.47, SQ 3.21		1918 / 254
SP	100%	Done	100%		SP 4.54		16604
TP/TC	100%	Done	100%	85%	TP 3.79, TC 7.5		337 / 2
CG/CGM/ROM	100%	Done	N/A	95%	CG 2.25, CGM 2.25, DBG 2.25		0
PA	100%	Done	100%	78%	PA 2.35		26
VGT	100%	Done	100%	89%	VGT 2.42		15
SC / SC_B	100%	Done	100%	81%	SC 2.39 / SC_B 2.26		41 / 1
RBBM	100%	Done	100%		RBBM 2.40		10
CP	100%	Done	100%	100%	CP 2.30		4
Display - DCP	100%	Done	100%	100%	3.72	PIXCLK 2.66	3669
Display - LB	100%	Done	100%	100%	3.25		
Display - SCL	100%	Done	100%	100%	3.23		
Display - CRTIC	100%	Done	100%	100%	2.25		
Display - DISPOUT	100%	Done	100%	100%	3.13		
Display - TVOUT	100%	Done	80%	50%		TVCLK 10.76	
VGA	100%	Done	99%	100%	4.43		
VIP	100%	Done	100%	100%	2.38		
BIF	95%	?	90%	30%	BIF 2.78	BCLK 12.39nS, AGP 3.50nS	242
IDCT	100%	Done	100%	100%	IDCT 2.9		

[Date/Time]

R400 Executive Reviews
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General Status

- **Design/Synthesis**

- BIF resource continues to be on RV280 work
- Focused on re-synthesis to 2.25nS cycle time and debug over the last week
 - AB Block split (had a few issues to work)
 - PA, VGT, SC and SC_B release
- Real Time Streams implemented
 - Passed RTS and mixed NRTS/RTS test

- **Verification Results**

- Regressions continuing to trend upward, experienced some instability
- Fullchip progress is slow but steady

- **Physical Design**

- Floorplan proposals under review
- Netlist 3.0 release expected 12/18

[DateTime]

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SP / AB Blocks

- **SP Block**

- Known timing issue understood; will be fixed this week
- Architectural precision issue identified
 - Fixes will have little area and no timing impact
- This has impacted the SP freeze

- **AB Block**

- AB block complete except for timing issue
 - Timing issue understood and is being worked
- Release will occur with Netlist 3.0

[DateTime]

R400 Executive Reviews
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PA, SC, VGT Blocks

- **Block Level Test Regressions**

Test Bench	Tests Run	Tests Pass	% Pass	Report Date
VGT	2308	2308	100%	12/09/02
SC	2308	2198	95%	12/10/02
PA	2309	2201	95%	12/10/02

- **Block Level Random Testing**

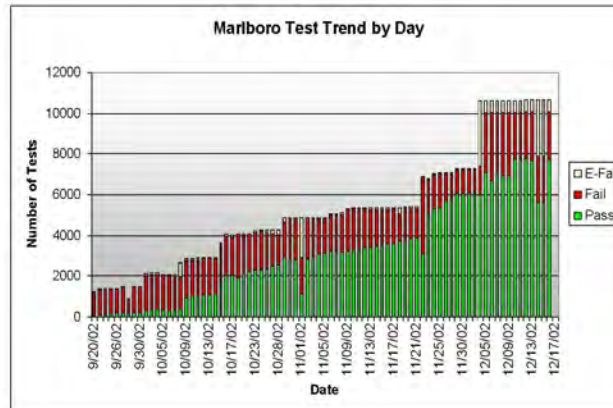
- VGT / PA / SC Block Randoms coded & passing 100%
- PA / SC Chip Randoms passing
- VGT / CP Chip Randoms started

[DateTime]

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Marlboro Blocks

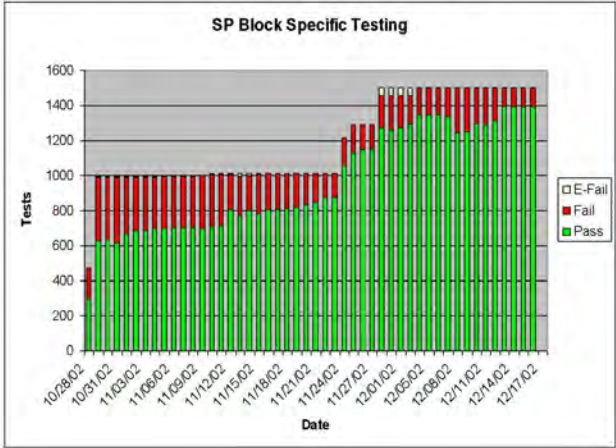


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SP Block Level Test

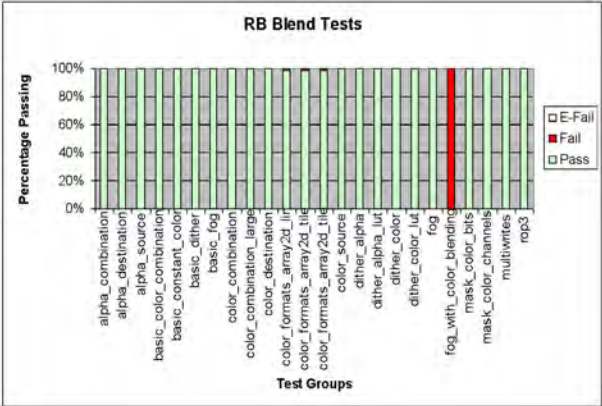


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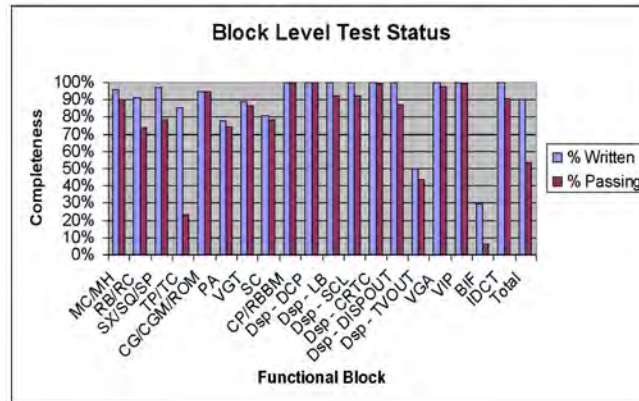
RB Blend (AB Block)



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Block Level Test Completeness



[DateTime]

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General Status

- **Block delivery**
 - AB, PA, SC, VGT blocks complete, delivery with Netlist 3.0
 - SP resolving corner case issues, SX delayed behind SP
 - MC delayed
 - Pad interface definition
 - Test plan review found test coverage holes

Major Block	Plan	Last FC	Current FC
RB Blend (AB Block)	11/18/2002	12/18/2002	12/18/2002
SP	11/18/2002	12/18/2002	1/5/2003
SX	12/2/2002	1/3/2003	1/11/2003
MC	12/16/2002	12/18/2002	1/2/2003
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
BIF	12/20/2002	1/15/2003	1/15/2003
DC	12/20/2002	1/15/2003	1/15/2003
DCT	12/20/2002	1/15/2003	1/15/2003
MH	1/2/2003	1/2/2003	1/2/2003
CP	1/10/2003	1/10/2003	1/10/2003
RBBM	1/10/2003	1/10/2003	1/10/2003
SO	1/15/2003	1/15/2003	1/15/2003
RB (Remaining)	1/15/2003	1/15/2003	1/15/2003
TP	1/31/2003	1/31/2003	1/31/2003
TC	1/31/2003	1/31/2003	1/31/2003

[DateTime]

R400 Executive Reviews
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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-03	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-04-02	01-04-02
Third Synthesis	11-01-02	12-18-02	12-18-02
Early block delivery begins	11-08-02	12-16-02	12-16-02
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	01-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	01-31-03
A11 Base Layers Tapeout	01-10-03	03-28-03	03-28-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	04-11-03
First Samples for Engineering		06-25-03	06-25-03
A12 Tapeout		07-31-03	07-31-03
A12 Samples for Engineering		09-04-03	09-04-03
R400 Customer Samples		09-11-03	09-11-03
Product Delivery		10-04-03	10-04-03

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Executive Review – R400

December 23, 2002

[DateTime]

R400 Executive Reviews
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1

Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.25nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	96%	MC 2.5, MH 2.37	MC - MCLK 1.71	0 / 1121
AB/RB/RC	100%	Done	100%	91%	AB 2.69, RB 5.38, RC 2.25		247 / 10275 / 0
SX/SQ	100%	Done	100%	97%	SX 3.47, SQ 3.21		1918 / 254
SP	100%	Done	100%		SP 4.54		16804
TP/TC	100%	Done	100%	85%	TP 3.78, TC 3.78		1345 / 16282
CG/CGM/ROM	100%	Done	N/A	95%	CG 2.25, CGM 2.25, DBG 2.25		0
PA	100%	Done	100%	78%	PA 2.35		26
VGT	100%	Done	100%	89%	VGT 2.42		15
SC / SC_B	100%	Done	100%	81%	SC 2.39 / SC_B 2.26		41 / 1
RBBM	100%	Done	100%		RBBM 2.40		10
CP	100%	Done	100%	100%	CP 2.30		4
Display - DCP	100%	Done	100%	100%	3.72	PIXCLK 2.66	3669
Display - LB	100%	Done	100%	100%	3.25		
Display - SCL	100%	Done	100%	100%	3.23		
Display - CRTIC	100%	Done	100%	100%	2.25		
Display - DISPOUT	100%	Done	100%	100%	3.13		
Display - TVOUT	100%	Done	80%	50%		TVCLK 10.78	
VGA	100%	Done	99%	100%	4.43		
VIP	100%	Done	100%	100%	2.38		
BIF	95%	?	90%	30%	BIF 2.78	BCLK 12.39nS, AGP 3.50nS	242
IDCT	100%	Done	100%	100%	IDCT 2.9		

[Date/Time]

R400 Executive Reviews
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General Status

- **Design/Synthesis**

- Focused on re-synthesis to 2.25nS cycle time and block releases
 - AB block split completed
 - PA, VGT, SC and SC_B released in Netlist 3.0

- **Verification Results**

- Regressions continuing to trend upward, experiencing some instability
- Fullchip progress is slow but steady

- **Physical Design**

- Architect working on floorplan proposals past week
- Netlist 3.0 release completing top level

[DateTime]

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SP / AB Blocks

- **SP Block**

- Known timing issue understood; fix is implemented
- Architectural precision issue identified
 - Fixes will have little area and no timing impact
 - Impacting the SP freeze

- **AB Block**

- AB block completed except for timing issue
 - Timing issue understood and is being worked

[DateTime]

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PA, SC, VGT Blocks

- **PA, SC and VGT blocks released**
- **Block Level Test Regressions**

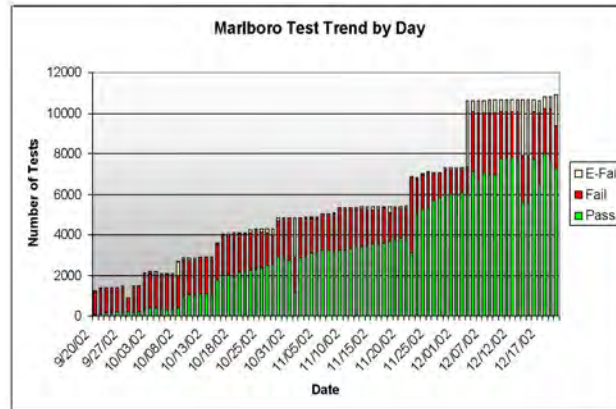
Test Bench	Tests Run	Tests Pass	% Pass	Report Date
VGT	2308	2308	100%	12/09/02
SC	2308	2198	95%	12/10/02
PA	2309	2201	95%	12/10/02

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Marlboro Blocks

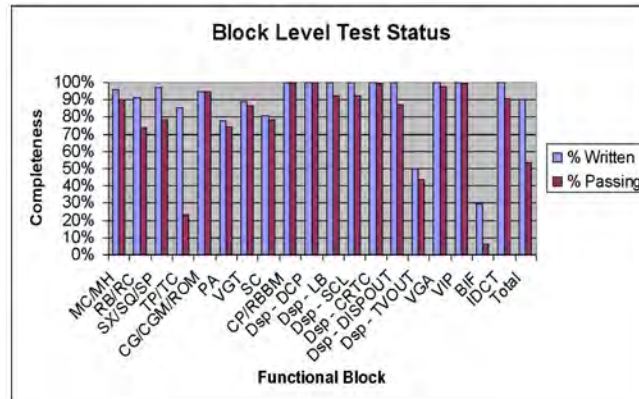


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Block Level Test Completeness



[DateTime]

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General Status

- **Block delivery**
 - AB, PA, SC, VGT blocks complete, delivery with Netlist 3.0
 - SP resolving corner case issues, SX delayed behind SP
 - MC delayed
 - Pad interface definition
 - Test plan review found test coverage holes, working through these

Major Block	Plan	Last FC	Current FC
RB Blend (AB Block)	11/18/2002	12/18/2002	12/18/2002
SP	11/18/2002	12/18/2002	12/18/2002
SX	12/2/2002	1/3/2003	1/1/2003
MC	12/16/2002	12/18/2002	12/18/2002
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
BIF	12/20/2002	1/15/2003	1/15/2003
DC	12/20/2002	1/15/2003	1/15/2003
DCT	12/20/2002	1/15/2003	1/15/2003
MH	1/2/2003	1/2/2003	1/2/2003
CP	1/10/2003	1/10/2003	1/10/2003
RBBM	1/10/2003	1/10/2003	1/10/2003
SQ	1/15/2003	1/15/2003	1/15/2003
RB (Remaining)	1/15/2003	1/15/2003	1/15/2003
TP	1/31/2003	1/31/2003	1/31/2003
TC	1/31/2003	1/31/2003	1/31/2003

[DateTime]

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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-03	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-04-02	01-04-02
Third Synthesis	11-01-02	12-18-02	12-23-02
Early block delivery begins	11-08-02	12-16-02	12-16-02
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	01-16-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	01-31-03
A11 Base Layers Tapeout	01-10-03	03-28-03	03-28-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	04-11-03
First Samples for Engineering		06-25-03	06-25-03
A12 Tapeout		07-31-03	07-31-03
A12 Samples for Engineering		09-04-03	09-04-03
R400 Customer Samples		09-11-03	09-11-03
Product Delivery		10-04-03	10-04-03

[DateTime]

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Executive Review – R400

January 6, 2003

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Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.25nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	100%	MC:2.5, MH: 2.37	MC - MCLK: 1.71	0 / 1121
AB/RB/RC	100%	Done	100%	100%	AB: 2.25, RB: 5.38, RC: 2.25		0 / 10275 / 0
SX/SQ	100%	Done	100%	100%	SX: 3.42, SQ: 3.11		1974 / 271
SP	100%	Done	100%	100%	SP: 2.70		1580
TP/TC	100%	Done	100%	85%	TP: 3.33, TC: 3.35		1345 / 16282
CG/CGM/ROM	100%	Done	N/A	95%	CG: 2.25, CGM: 2.25, DBG: 2.25		0
PA	100%	Done	100%	79%	PA: 2.27		3
VGT	100%	Done	100%	89%	VGT: 2.42		15
SC / SC_B	100%	Done	100%	83%	SC: 2.32 / SC_B: 2.25		9 / 0
RBBM	100%	Done	100%	100%	RBBM: 2.28		1
CP	100%	Done	100%	100%	CP: 2.30		4
Display - DCP	100%	Done	100%	100%	3.72	PIXCLK: 2.66	3669
Display - LB	100%	Done	100%	100%	3.25		
Display - SCL	100%	Done	100%	100%	3.23		
Display - CRTIC	100%	Done	100%	100%	2.25		
Display - DISPOUT	100%	Done	100%	100%	3.13		
Display - TVOUT	100%	Done	90%	100%		TVCLK: 10.76	
VGA	100%	Done	99%	100%	4.43		
VIP	100%	Done	100%	100%	2.38		
BIF	95%	?	90%	30%	BIF: 2.78	BCLK: 12.39nS, AGP: 3.50nS	242
IDCT	100%	Done	100%	100%	IDCT: 2.66		76

[Date/Time]

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Design / Verification

- **Design/Synthesis**

- Netlist 3.0 synthesis at 2.25nS cycle time; released 1/02/03.
- SP Block
 - Architectural precision issues:
 - HW fixes implemented
 - Some additional timing work still to be done
 - Some regression failures remain – thought to be emulator issues to be worked this week

- **Verification Results**

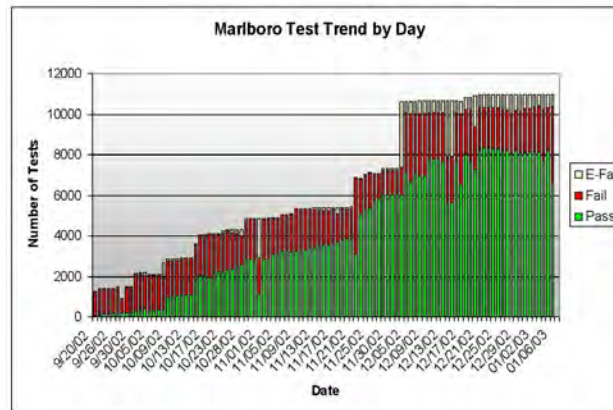
- Three blocks not progressing as planned: Texture, Sequencer, Bus Interface
- Fullchip progress is slow but steady

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Marlboro Blocks

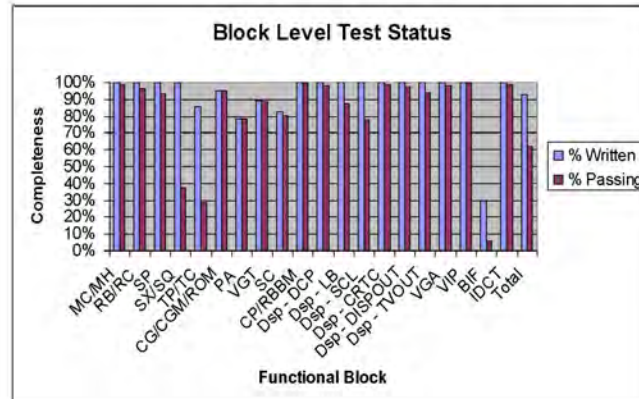


[DateTime]

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Block Level Test Completeness



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Design / Verification

- **Two problem graphics blocks exist (SQ and Texture)**
 - Orlando is essentially complete and has resources available
 - Plan is to have Orlando take responsibility for validation of SQ
 - Move three resources from Orlando to SQ
 - Second part of plan is for Marlboro to focus additional resources on Texture Unit (TP/TC)
 - TP verification debug is currently a bottleneck
 - Moving resource from TC to TP for debug
 - Moving verification resource to TC design
 - Using synthesis contractor for TC block split
- **BIF is expected to progress as RV280 issues wane**

[DateTime]

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General Status

- Chip area
 - Currently estimated at 15.8mm²/side
 - Re-synthesis for Netlist 3.0 was targeted for 2.25nS cycle time
 - Approximately 5 – 10 % area increase depending on block
 - Design priorities have been set:
 - 1) Functional debug
 - 2) Timing
 - 3) Area reduction as blocks complete 1 and 2.

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Physical Design

- Netlist 2.0:
 - Generated 11 floorplans
 - Ran most through SPC - 20hr+ runtime each
 - Rejected all but two based on SPC routed congestion results (net2.0plan0.80 and net2.0plan1.11)
- Netlist 3.0:
 - Built floorplan candidate based on netlist 3.0, using net2.0plan0.80 as guide
 - SiV is generating tiles, and running through SPC for congestion report

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Physical Design

- Blocks:
 - As an experiment, running individual blocks through SPC
 - VGT
 - 1hr runtime for: Place/FE-ClkTree/TrialRoute/Extract/Time/IPO -high/
IPO -High
 - Results:
 - Worst path 2.436 ns (with clock skew), no manual IPO
 - 70% initial utilization to < 72% after clock + IPO
 - Future work
 - Validate SPC results with real route and extract
 - Plan to generate custom wireload models for next netlist
 - Do bigger more complex blocks

[DateTime]

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General Status

- **Block delivery**
 - AB, PA, SC, VGT blocks complete, delivery with Netlist 3.0
 - SP resolving corner case issues, SX delayed behind SP
 - MC delayed
 - Pad interface definition being discussed today in Marlboro with SiV team
 - Test plan review found test coverage holes, working through these

Major Block	Plan	Last FC	Current FC
RB Blend (AB Block)	11/18/2002	12/18/2002	12/18/2002
SP	11/18/2002	12/18/2002	12/18/2002
SX	12/2/2002	1/3/2003	1/17/2003
MC	12/16/2002	12/18/2002	1/20/2003
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
BIF	12/20/2002	1/15/2003	1/15/2003
DC	12/20/2002	1/15/2003	1/15/2003
DCT	12/20/2002	1/15/2003	1/15/2003
MH	1/2/2003	1/2/2003	1/2/2003
CP	1/10/2003	1/10/2003	1/10/2003
RBBM	1/10/2003	1/10/2003	1/10/2003
SQ	1/15/2003	1/15/2003	1/15/2003
RB (Remaining)	1/15/2003	1/15/2003	1/15/2003
TP	1/31/2003	1/31/2003	1/31/2003
TC	1/31/2003	1/31/2003	1/31/2003

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Executive Review – R400

January 13, 2003

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Design / Verification

- **SP**
 - Last few bugs, ironing precision out, updated SQRT today
 - Plan is to freeze with Netlist 4.0 release
- **TP**
 - Working LOD logic, expect wrap-up this week
 - Belief is LOD is a major blockage to tests passing
- **TC**
 - Performance improvements designed and released
 - Break-up in progress, expected done for Netlist 4.0
 - Full verification impacted by TP bugs
- **SQ**
 - Orlando ramp-up started, Division of labor identified
 - Regular meetings start today to coordinate Orlando-Marlboro

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Design / Verification

- **RB**
 - Random testing continues with a high failure rate
 - RB requires division to fit in physical design tools
 - Timing has improved from 5ns to 1.7ns violation over the Holidays
- **MC/MH**
 - MC Pad interface logic design in progress, completed 1/31.
 - Gates Netlist 4.0
 - MH chip level tests continue to find bugs, working through issues
- **SX**
 - Bugs are being fixed – behind SP in priority
- **CP/RBBM**
 - Directed testing to be completed this month
 - Freeze is gated by chip level testing (requires 8 weeks)

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Design / Verification

- **BIF**
 - Resource conflict with RV280 resolved
 - Requires 2 months to complete
- **IDCT**
 - Complete by end of month
- **DC**
 - Timing fixes being identified
 - Freeze gated by chip level simulations
 - Current dependency is on resolution of MH bugs

[DateTime]

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General Status

- Block delivery

Major Block	Plan	Last FC	Current FC
RB Blend (AB Block)	11/18/2002	12/18/2002	12/18/2002
SP	11/18/2002	1/9/2003	2/14/2003
SX	12/2/2002	1/11/2003	2/28/2003
MC	12/16/2002	1/20/2003	3/15/2003
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
BIF	12/20/2002	1/15/2003	3/15/2003
DC	12/20/2002	1/15/2003	2/28/2003
DCT	12/20/2002	1/15/2003	1/31/2003
MH	1/2/2003	1/2/2003	3/15/2003
CP	1/10/2003	1/10/2003	3/31/2003
RBBM	1/10/2003	1/10/2003	3/31/2003
SQ	1/15/2003	1/15/2003	5/1/2003
RB (Remaining)	1/15/2003	1/15/2003	4/10/2003
TP	1/31/2003	1/31/2003	4/30/2003
TC	1/31/2003	1/31/2003	4/30/2003

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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration – 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
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Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	05-01-03
A11 Base Layers Tapeout	01-10-03	03-28-03	06-26-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	07-10-03
First Samples for Engineering		06-25-03	09-12-03
A12 Tapeout		07-31-03	10-17-03
A12 Samples for Engineering		09-04-03	11-28-03
R400 Customer Samples		09-11-03	12-05-03
Product Delivery		10-04-03	12-29-03

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Block Logic Design and Timing

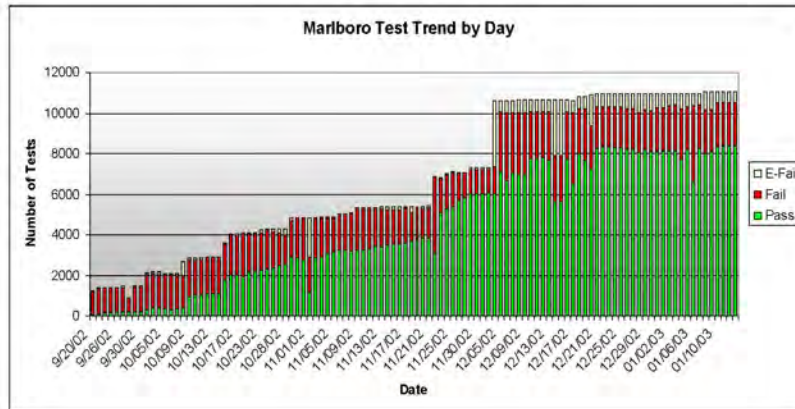
Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.25nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	100%	MC:2.86; MH: 2.37	MC - MCLK: 1.71	36 / 1121
AB/RB/RC	100%	Done	100%	100%	AB: 2.25; RB: 3.95; RC:2.25		0 / 14450 / 0
SX/SQ	100%	Done	100%	100%	SX: 3.42; SQ: 3.11		1974 / 271
SP	100%	Done	100%	100%	SP: 2.70		1580
TP/TC	100%	Done	100%	85%	TP: 3.33; TC: 3.35		1345 / 16282
CG/CGM/ROM	100%	Done	N/A	95%	CG: 2.25; CGM:2.25; DBG:2.25		0
PA	100%	Done	100%	82%	PA: 2.27		3
VG	100%	Done	100%	96%	VG: 2.42		15
SC / SC_B	100%	Done	100%	83%	SC: 2.32 / SC_B: 2.25		9 / 0
RBBM	100%	Done	100%	100%	RBBM: 2.28		0.5
CP	100%	Done	100%	100%	CP: 2.29		5
Display - DCP	100%	Done	100%	100%	3.13	PIXCLK: 2.66	2178
Display - LB	100%	Done	100%	100%			
Display - SCL	100%	Done	100%	100%	2.51		
Display - CRTC	100%	Done	100%	100%			
Display - DISPOUT	100%	Done	100%	100%			
Display - TVOUT	100%	Done	80%	100%		TVCLK:10.76	
VGA	100%	Done	99%	100%	3.35		
VIP	100%	Done	100%	100%	2.26		
BIF	95%	3/15	90%	48%	BIF: 2.86	BCLK: 12.36nS; AGP:3.50nS	148
IDCT	100%	Done	100%	100%	IDCT: 2.85		117

[Date/Time]

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Marlboro Blocks

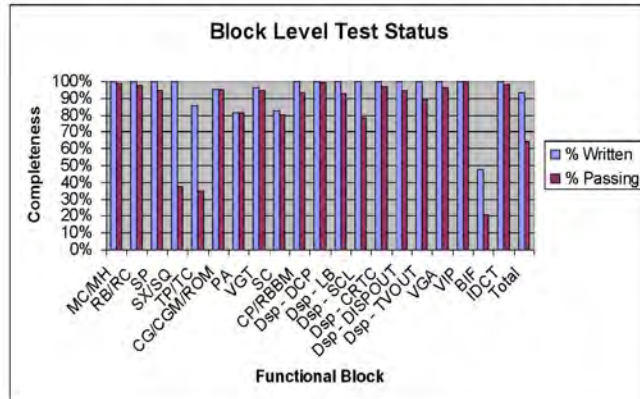


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Block Level Test Completeness



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Executive Review – R400

January 20, 2003

[DateTime]

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1

General Status

- **Putting together a general mitigation plan**
 - Portions of plan in today's discussion
 - Pulling resources from Orlando
 - Planning to use resources from SiV team
 - Re-focusing local resources on troubled areas
 - Trying to pull all blocks into early April timeframe

[DateTime]

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Design / Verification

- **SP**
 - Working through last precision bugs and an SQ bug affecting SP
 - Directed/Randoms passing at 95%
 - SQRT updated last week, some fine tuning underway
 - Expect last SQRT fixes by 1/22
 - FRACT emulator issue understood and being corrected
 - Plan is to freeze with Netlist 4.0 release
- **SQ**
 - Closure rate of SQ debug was not sufficient for schedule
 - Recovery plan
 - Orlando has resources available
 - Six engineers assisting with RTL validation, test bench generation, test suite review and performance analysis / validation
 - ORL assuming synthesis responsibilities to free up Marlboro SQ resource for other work
 - Individuals coming on line & starting to be productive
 - Performance enhancements made this past week, debugging Control flow in process
 - **ORL driving validation, trying to improve overall delivery to a very aggressive target of 3/31**
 - Initial test plan review occurred 1/15
 - Will not know ORL affect for a couple more weeks (may not be long pole with ORL assistance)
- **SX**
 - Moving export allocate counter to SQ to solve performance issue
 - Debug remainder of export features (dependent on SQ debug)
 - Add ORL resource to speed debug of SX
 - Timing improved by 0.8ns over last week, expect to meet timing this week

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Design / Verification

- **RB**
 - Random testing improving (85% passing up from 52% the previous week)
 - 2D register fix in RB is complex
 - Being fixed in conjunction with other architectural register consolidation efforts
 - RB needs division to fit in physical design tools
 - Will not gate Netlist 4.0 (plan for Netlist 5.0)
 - Resource added to address timing issues
 - Fixes in process for RB sub-blocks
 - Adding ORL resource for RB long pole areas (stencil & depth)
- **AB**
 - Performance analysis is complete and satisfactory
 - Block awaiting PD feedback
- **MC/MH**
 - MC Pad interface logic design in progress, completion 1/31
 - Planned for Netlist 4.0
 - MC/MH Block level test complete, identified verification coverage holes that are being addressed
 - Moving resource to test writing
 - Adding resource to implement MC/MH testbench enhancements
 - Starting significant stress and random verification
 - MH corrected a number of chip level bugs this past week

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Design / Verification

- **TP/TC**

- Recovery

- Senior resource focusing on TP/TC debug
 - Resource added for test bench focus
 - Plan to ask R300 team for assistance
 - Architectural, RTL code and emulator review
 - Discussion with Bob Drebin later today
 - Trying to pull towards 4/2

- **TP**

- Worked on LOD logic through last week
 - Making precision adjustments that are continuing
 - Tests passing last week experienced a jump

- **TC**

- Break-up completed last week: TCM, TCF, TCR
 - Simulating against original TC
 - Study and identify AGP vertex performance issue
 - Repair not yet fully understood
 - Expect some area/schedule impact for TC
 - Architectural deadlock issue
 - Identified and fix being implemented (expected complete this week)

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Design / Verification

- **CP / RBBM / VGT / PA / SC / SC_B**
 - Gate Level simulations of all blocks in progress
 - Code coverage results used to improve random and stress test coverage
 - Real Time Streams, Pipe Disable, 2D Validation in progress
 - Moving to GC/Full chip testing
 - CP/RBBM gated by chip level testing progress
 - VGT / PA / SC / SC_B awaiting physical design feedback

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Design / Verification

- **BIF**

- BIF team focusing on verifying AGP fast write changes.
- Porting existing tests from R300
 - 108 out of 150 tests passing now in emulator
 - 20% of the progress since Wednesday.
- BIF's timing issues are due to design changes that are in review
- Emulation work on track for 2/7 complete.

- **IDCT**

- Complete by end of month

- **DC**

- DC still has some violations caused by a few improper constraints
 - Most timing violations in DC will be corrected through iterative synthesis
- Emulation work on track for 1/24 for tvout
 - SDTV tests in tvout fully released. HDTV tests are on track for this week
- Completion gated by chip level simulations
 - MH bugs resolved

[DateTime]

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General Status

- Block delivery

Major Block	Plan	Last FC	Current FC
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
AB	11/18/2002	12/18/2002	12/18/2002
DCT	12/20/2002	1/15/2003	1/31/2003
SP	11/18/2002	1/9/2003	2/14/2003
SX	12/2/2002	1/11/2003	2/28/2003
DC	12/20/2002	1/15/2003	2/28/2003
MC	12/16/2002	1/20/2003	3/15/2003
BIF	12/20/2002	1/15/2003	3/15/2003
MH	1/2/2003	1/2/2003	3/15/2003
CP	1/10/2003	1/10/2003	3/31/2003
RBBM	1/10/2003	1/10/2003	3/31/2003
RB	1/15/2003	1/15/2003	4/10/2003
TP	1/31/2003	1/31/2003	4/30/2003
TCM/TCF/TCR	1/31/2003	1/31/2003	4/30/2003
SQ	1/15/2003	1/15/2003	5/1/2003

[DateTime]

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Chip Integration

- **Final memory compliers received from Virage on 1/14/03**
- **Pad Ring**
 - Final Pad Ring is being created; all major issues resolved
- **Packaging**
 - R400 will use the same 40X40 ball package as R300
 - Stiffener is not expected to be part of the package
 - Corner ball will be removed
 - Routing experiments to begin after final padout
 - Laser fuses on package for device “personality”
 - This allow final test to determine speed, workstation, etc.
- **Operation and Test Flow**
 - Operation, Test, and Engineering met with Virage
 - Virage discussed previous customer issues and flow
 - ASE has been selected to take on the repair
 - The are suggested vendor of Virage and one of ATI’s primary vendors
 - Operations will be providing a plan and schedule in early February

[DateTime]

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Chip Integration

- Pushing Netlist 4 early (1st week of Feb.)
 - Final Memory Controller Pad interface for DDR3
 - PD team wants to begin looking at this as early as possible
 - Split of the TC into 3 blocks
 - First pass look at DFT coverage over whole chip
- Netlist 5 (1st week of March)
 - Final Top Level interconnect, logically correct, including test
 - Split of RB block (instance count too high)
 - Final Tile configurations
 - Feedback from netlist 3.0 used in synthesis

[DateTime]

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Physical Design

- **Rick Hagen / Frank Hering will be in SiV this week**
 - Work through dependencies
- **Debug new tile flow: estimate is 2 weeks**
- **Netlist 3.0 tile P&R: 2 – 3 weeks depending on tile**
 - Push tiles through the flow, goal is to get as many tiles routed, extracted, and timed as possible.
 - Provide FE team with feedback (local congestion problems, timing, routability, etc)
- **Debugging top level flow**
 - Fallbacks for most areas of the flow
 - Cadence tool issue (commitPartition) delayed work
 - Incremental release (rel_3.0B) this week
 - Runtime and reuse are risks
- **Start toplevel P&R activities**
 - dependent on getting top level flow clean
 - Release_3.0B is a starting candidate
- **Floorplan efforts for netlist 3.0 underway**

[DateTime]

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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration – 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-02	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	05-01-03
A11 Base Layers Tapeout	01-10-03	03-28-03	06-26-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	07-10-03
First Samples for Engineering		06-25-03	09-12-03
A12 Tapeout		07-31-03	10-17-03
A12 Samples for Engineering		09-04-03	11-28-03
R400 Customer Samples		09-11-03	12-05-03
Product Delivery		10-04-03	12-29-03

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Backup Slides

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Block Logic Design and Timing

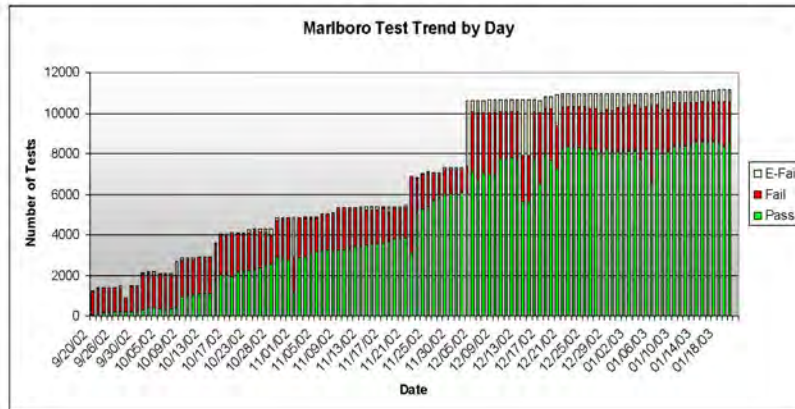
Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.25nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	98%	MC:2.86; MH: 3.37	MC - MCLK: 1.71	36 / 1688
AB/RB/RC	100%	Done	100%	78%	AB: 2.46; RB: 3.91; RC:2.25		0.3 / 9989 / 0
SX/SQ	100%	Done	100%	96%	SX: 2.57; SQ: 3.09		36 / 136
SP	100%	Done	100%	100%	SP: 2.70		1580
TP/TCM/TCF/TCR	100%	Done	100%	85%	TP: 3.11; TCM: 2.25; TCF: 3.10; TCR:3.02		486 / 0 / 12347 / 752
CG/CGM/ROM	100%	Done	N/A	95%	CG: 2.25; CGM:2.25; DBG:2.25		0
PA	100%	Done	100%	94%	PA: 2.29		6
VG	100%	Done	100%	98%	VG: 2.27		1
SC / SC_B	100%	Done	100%	86%	SC: 2.42 / SC_B: 2.25		28 / 0
RBBM	100%	Done	100%	100%	RBBM: 2.28		0.4
CP	100%	Done	100%	100%	CP: 2.25		0
Display - DCP	100%	Done	100%	100%	3.58		2178
Display - LB	100%	Done	100%	100%			
Display - SCL	100%	Done	100%	100%	2.52		
Display - CRTC	100%	Done	100%	100%	2.6	PIXCLK: 2.66	
Display - DISPOUT	100%	Done	100%	100%	3.88		
Display - TVOUT	100%	Done	100%	68%	2.29		
VGA	100%	Done	100%	100%	3.59		
VIF	100%	Done	100%	100%	2.92		
BIF	98%	2/15	90%	64%	BIF: 2.83	BCLK: 14nS; AGP:3.50nS	203
IDCT	100%	Done	100%	100%	IDCT: 2.38		21

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Marlboro Blocks

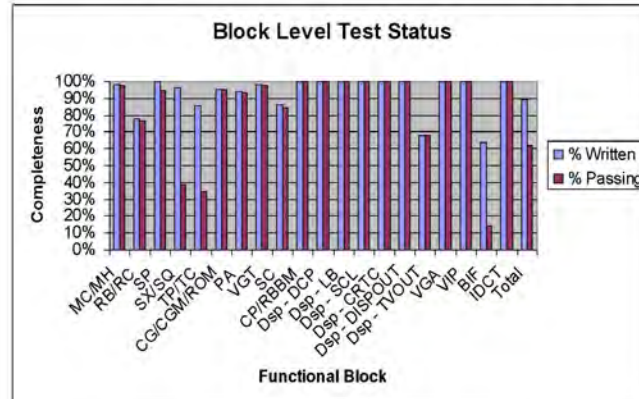


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Block Level Test Completeness



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Executive Review – R400

January 27, 2003

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1

General Status

- **R400 Tapeout frequency**
 - Is 400 MHz an adequate tapeout frequency ?
- **General mitigation plan**
 - Resources from Orlando in place
 - Re-focusing of Marlboro resources has started
 - Still planning to use resources from SiV team as possible
 - Konstantine Iourcha is engaged and is reviewing the texture cache
 - Still pursuing additional resources from SiV

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Design / Verification

- **SP**
 - Last corner case bugs persist in addition to an SQ bug affecting the SP
 - SQRT hardware and emulator updates were completed last week (some fine tuning continues)
 - SQRT directed & random testing hit 100% passing last week
 - Added interface checking to frame buffer comparisons
 - Graphics core testbench interface checkers are showing failures not necessarily related to the SP block
 - Emulator mismatches
 - Other smaller issues being addressed
 - Remaining SP hardware and emulator failures being rectified
 - Architect and Block Lead to focus on this for next 2 days
 - SQ bug affecting MOVA functionality partially corrected, expect full fix this week
 - Plan is to freeze with Netlist 4.0 release
- **SQ**
 - Debug and repair of MOVA functionality major focus last week
 - Recovery plan - ORL driving validation to a very aggressive target of 3/31
 - Orlando has been ramping on the SQ and contributing to debug
 - Fixed bugs within the pixel input controller
 - Beginning emulation/RTL debug work on sequencer operation and predication
 - Ramping up understanding of control flow, starting to work bugs
 - Performance enhancements made this past week
 - » Export buffer counters
 - » Improvement made to prevent fetching of unnecessary control flow instructions
 - » Interface improvements
- **SX**
 - Orlando ramping up to assist with SX
 - Identified and fixed hang
 - Continuing debug of remainder of export features (dependent on SQ debug)
 - Working through synthesis, still 0.3ns violation over 2.25ns.

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Design / Verification

- **RB**
 - 2D register fix and architectural register consolidation in RB nearly complete
 - Also added 2D endian register
 - RB analyzing memory performance bandwidth
 - Excellent at 32bit pixels (64 bit pixels will need some work, not a priority)
 - Resources have implemented many fixes to address timing issues
 - Added resource in place to assist with timing and synthesis
 - Orlando resource is ramping and has begun to assist with debug
 - Existing RB resource now focusing on multi-sample debug
- **AB**
 - Block awaiting PD feedback
 - PD team is using the block for re-use flow analysis
- **MC/MH**
 - MC Pad interface logic design completed, debugging continuing in local area testbench
 - Ready to release today into general environment
 - First MC synthesis with new pad interface completed
 - MC/MH Block level coverage holes
 - Debugging multi memory architecture tests in testbench
 - Resource added and ramping to implement MC/MH testbench enhancements
 - Finalized GMB arbitration enhancements to assist with single/multiple client debug
 - MH continues to address and fix chip level bugs from chip level regressions

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Design / Verification

- **TP/TC**

- Recovery

- Senior resource focusing on TP/TC debug
 - Resource added for test bench focus
 - On board and being productive
 - Still planning on R300 team for assistance
 - Konstantine Iourcha is reviewing the Texture Cache (TC)
 - Still pursuing an additional resource from SiV for TP/TC debug

- **TP**

- Team worked through and released the LOD hardware fixes
 - These precision changes were released into the test environment with no adverse affect
 - Matching emulator changes for LOD are in the queue

- **TC**

- **Simulating** TCM, TCF, TCR in place of **original TC**
 - Completion and release this week for Netlist 4.0
 - AGP vertex performance issue
 - Repair understood
 - About 2 days into a 2 week task to correct
 - Architectural deadlock issue
 - Fix implemented and released last week

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Design / Verification

- **CP / RBBM / VGT / PA / SC / SC_B**
 - Gate Level simulations of all blocks continue
 - SC_B has run through the PD flow with Rel_3.0a
 - First tile to receive feedback from the Physical Design team

[DateTime]

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General Status

- Block delivery

Major Block	Plan	Last FC	Current FC
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VGT	12/16/2002	12/16/2002	12/16/2002
AB	11/18/2002	12/18/2002	12/18/2002
IDCT	12/20/2002	1/15/2003	1/31/2003
SP	11/18/2002	1/9/2003	2/14/2003
SX	12/2/2002	1/11/2003	2/28/2003
DC	12/20/2002	1/15/2003	2/28/2003
MC	12/16/2002	1/29/2003	3/15/2003
BIF	12/20/2002	1/15/2003	3/15/2003
MH	1/2/2003	1/2/2003	3/15/2003
CP	1/10/2003	1/10/2003	3/31/2003
RBBM	1/10/2003	1/10/2003	3/31/2003
RB	1/15/2003	1/15/2003	4/10/2003
TP	1/31/2003	1/31/2003	4/30/2003
TCM/TCF/TCR	1/31/2003	1/31/2003	4/30/2003
SQ	1/15/2003	1/15/2003	5/1/2003

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Chip Integration

- **Chip Level Test**

- We are seeing progress in chip level simulations
 - Tests (in general) have gone from hanging to running to completion
 - Simple graphics tests are passing
- DMA of 2 MB from AGP to Local Memory passed
- IKOS register backbone has been verified
 - Working on memory initialization with old pads

- **Packaging**

- R400 will use the same 40x40 ball package as R300
 - Plan in place from the Package Engineering team
 - Vincent C is aware of concerns from R300
 - Will be running experiments to validate enhancements

- **Operation and Test Flow**

- Operations will be providing a plan and schedule (early February)
- Planning a meeting for early February for further discussions

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Chip Integration

- **Pad ring is completed**
 - Memory clock pads are an exception
 - Require input from SiV pad designers
- **First pass feedback from the P & R tools is being analyzed**
 - Investigating an error with resistance extractions
- **First pass DFT and coverage checks run against MC, BIF, SI and DC**
- **SOCBist is being used on first stable blocks (SP, AB, SC, SC_B, PA)**
- **Pushing Netlist 4 early (1st week of February)**
 - Final Memory Controller Pad interface for DDR3
 - PD team wants to begin looking at this as early as possible
 - Split of the TC into 3 blocks
 - First pass look at DFT coverage over whole chip
- **Netlist 5 (1st week of March)**
 - Final Top Level interconnect, logically correct, including test
 - Split of RB block (instance count too high)
 - Final Tile configurations
 - Feedback from netlist 3.0 used in synthesis

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Physical Design

- **Netlist 3.0**
 - Net 3.0a – released for PD
 - Packaged up tiles for PD team to process
 - First results back to SC_B block
 - More tile results are coming this week
 - Net 3.0b – Corrects for deficiencies from 3.0a
 - Metal 6 obstructions, power grid, repeaters, toplevel influence pins and RAM placements
 - Net 3.0c – re-process with timing driven placement
 - First Feedback (SC_B) from Rel_3.0a
 - Initial utilization: 70.8%
 - Worst case post P&R internal setup violation: 767ps (from 10ps violation pre-layout)
 - Worst case post P&R I/O setup violation: 855ps
 - 7 routing violations in final nanoroute run
 - Final utilization is 70.5%
- **Meeting last week**
 - Planned out Logic/Physical design deliverables for next 10 weeks
 - Incremental release (Rel_3.0b) this week
 - Runtime and reuse are risks
- **Timing feedback**
 - First set of blocks will be available first week of February (possibly this week)
 - More complex blocks the following week
- **Starting on toplevel P&R activities**
 - Release_3.0b is the starting candidate

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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-02	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
Netlist 4.0	02-14-03	02-14-03	02-07-03
Netlist 5.0	03-03-03	03-03-03	03-03-03
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	01-31-03	05-01-03
A11 Base Layers Tapeout	01-10-03	03-28-03	06-26-03
A11 Metal Layers Tapeout	01-24-03	04-11-03	07-10-03
First Samples for Engineering		06-25-03	09-12-03
A12 Tapeout		07-31-03	10-17-03
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R400 Customer Samples		09-11-03	12-05-03
Product Delivery		10-04-03	12-29-03

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Block Logic Design and Timing

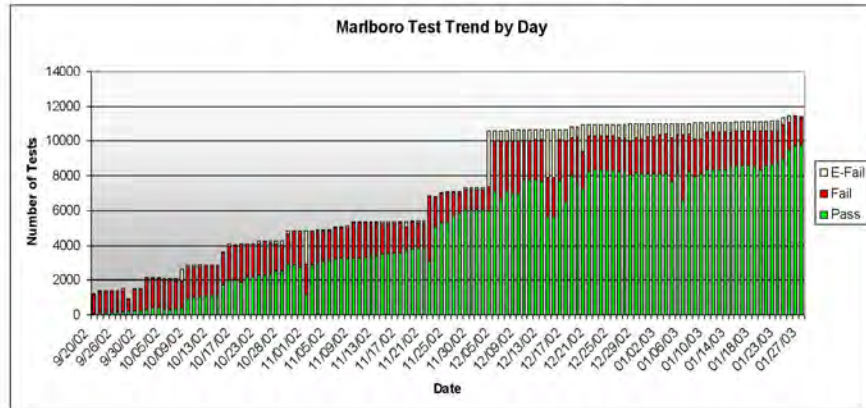
Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.25nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MCMH	100%	Done	N/A	100%	MC: 2.84; MH: 2.40	MC - MCLK: 1.71	44 / 93
AB/RB/RC	100%	Done	100%	80%	AB: 2.46; RB: 3.79; RC: 2.25		0.3 / 7983 / 0
SX/SQ	100%	Done	100%	96%	SX: 2.57; SQ: 3.09		36 / 136
SP	100%	Done	100%	100%	SP: 2.70		1580
TP/TCM/TCF/TCR	100%	Done	100%	86%	TP: 3.13; TCM: 2.25; TCF: 4.24; TCR: 3.32		523 / 0 / 18168 / 2225
CG/CGM/ROM	100%	Done	N/A	95%	CG: 2.25; CGM: 2.25; DBG: 2.25		0
PA	100%	Done	100%	97%	PA: 2.27		2
VG	100%	Done	100%	98%	VG: 2.29		2
SC / SC_B	100%	Done	100%	87%	SC: 2.34 / SC_B: 2.26		35 / 0.1
RBBM	100%	Done	100%	100%	RBBM: 2.28		0.4
CP	100%	Done	100%	100%	CP: 2.25		0
Display - DCP	100%	Done	100%	100%	3.58		212
Display - LB	100%	Done	100%	100%			
Display - SCL	100%	Done	100%	100%	2.52		
Display - CRT	100%	Done	100%	100%	2.6	PIXCLK: 2.66	
Display - DISPOUT	100%	Done	100%	100%	3.86		
Display - TVOUT	100%	Done	100%	68%	2.29		
VGA	100%	Done	100%	100%	3.59		
VIP	100%	Done	100%	100%	2.92		
BIF	98%	2/15	90%	64%	BIF: 2.92	BCLK: 14nS; AGP: 3.50nS	142
IDCT	100%	Done	100%	100%	IDCT: 2.30		2

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Marlboro Blocks

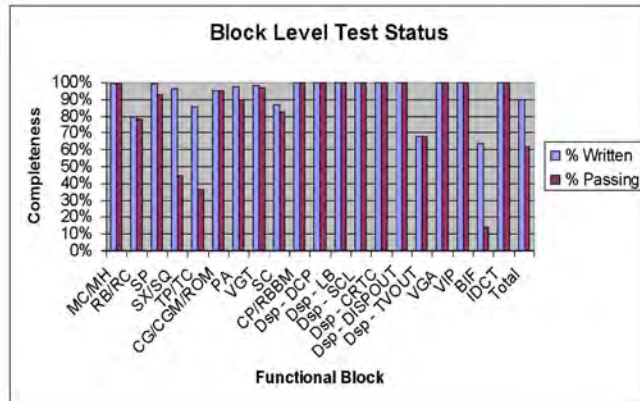


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Block Level Test Completeness



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Executive Review – R400

February 10, 2003

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General Status

- **R400 area constant (past 4 weeks), TNS down 55%**
- **R400 Tapeout frequency**
 - R400 Marketing input
 - Given the R400 schedule, Marketing wants the high end sku to be >450 MHz
 - Synthesizing to 2.25ns (444MHz)
 - Not yet achieved...3 blocks still having trouble – TC, SP, RB
 - Tapeout expected at 2.5ns (400MHz) or better
 - If we do 2.5ns or better, we should get some yield at 450+ MHz
- **General mitigation plans**
 - Focusing Toronto resources on IKOS
 - TP/TC mitigation
 - Discuss this more later ...

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Design / Verification

- **SP**
 - Released HW / Emulator corrections through last week
 - Precision errors mostly corrected
 - MOVA bug causing majority of failures
 - Progress made in timing
 - More effort required
 - Requires this week to complete (originally planned)
- **SQ**
 - Concentrated on MOVA bug
 - Corrected, investigation in other blocks: SX and/or RB
 - Predication tests expected to start passing
 - Expect release today from Orlando
 - General debug progressing in parallel
- **SX**
 - Debug progressing with SQ work
- **RB / AB**
 - 2D register fixes released
 - Implemented many timing fixes
 - Improved timing but caused some unstable periods
 - Orlando resource focused on failing randoms
 - Progressing with multi-sample debug
 - Planning RB split for PD

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Design / Verification

- **MC/MH**
 - MC
 - Pad interface logic design released
 - Caused only minor issues in general environment
 - Released refresh checker in the DRAM model for MC
 - MH
 - Focused on single client randoms debug
 - Solving multiple client bugs in the process
- **TP/TC**
 - TP
 - LOD emulator fixes
 - Delayed behind TP formatter corrections
 - TC
 - Release of divided TCM, TCF, TCR completed
 - Vertex fetching performance issues
 - Inadequate handling of AGP Vertex fetching latency
 - Poor sizing of cache lines for Vertex data
 - » Architectural solution not yet complete
 - Left alone, this set of problems is likely to have a 1 month schedule impact
 - Mitigation plans have started:
 - » Resources from SiV, Orlando and Marlboro will be re-assigned.
 - » Impact of mitigation plan not yet understood

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Design / Verification

- CP / RBBM / VGT / PA / SC / SC_B
 - CP/RBBM gate level sims running/passing at 99%
 - Randoms found 12 bugs in CP
- IDCT
 - Validated for closure
 - Release with Netlist 4.0
- DC
 - Closure on track
 - Risk: Does not include split of DC for PD tools
- BIF
 - Feature coding complete
 - Test writing and debug progressing
 - Risk: Architecture changes may affect timing closure

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Block closures

- Delivery targets

Major Block	Plan	Last FC	Current FC
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VG	12/16/2002	12/16/2002	12/16/2002
AB	11/18/2002	12/18/2002	12/18/2002
IDCT	12/20/2002	1/31/2003	1/31/2003
SP	11/18/2002	2/14/2003	2/14/2003
SX	12/2/2002	2/28/2003	2/28/2003
DC	12/20/2002	2/28/2003	2/28/2003
MC	12/16/2002	3/15/2003	3/15/2003
BIF	12/20/2002	3/15/2003	3/15/2003
MH	1/2/2003	3/15/2003	3/15/2003
CP	1/10/2003	3/31/2003	3/31/2003
RBBM	1/10/2003	3/31/2003	3/31/2003
RB	1/15/2003	4/10/2003	4/10/2003
TP	1/31/2003	4/30/2003	4/30/2003
TCM/TCF/TCR	1/31/2003	4/30/2003	4/30/2003
SQ	1/15/2003	5/1/2003	5/1/2003

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Chip Integration

- **Netlist 4**
 - All blocks have been released and the chip level processed
 - Pad Ring done (with the exception of VREF and Power in GPIO sections)
 - Release will happen today
- **DFT**
 - The PA, SC, SC_B, SP and MH have all passed through SOCbist
 - High stuck-at coverage >99.5% and short patterns sets
 - Scripting developed for scan insertion of MC, and DC, BIF, SI, and CGM
 - Plan to release this scripting into the synthesis flow has been developed
- **Chip Level Test**
 - Disruption in past week but have recovered
 - Concentrating on 2D tests
- **IKOS progressing**
 - Register R/W working
 - Memory writes working, memory reads working on one channel
 - Basic Display test are ready for IKOS
- **Operation and Test Flow (meeting this past week)**
 - Initial feedback on process from ASE
 - Supplying info on memories and fuses for review

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Physical Design

- **PD/LD tile reviews on rel_3.0A/B**
- **Rel_3.0C released last week**
 - Tile owners starting (now have an owner for each tile)
 - Major top level netlist fix identified and implemented
 - 2 MC / 2 RB types for re-use
- **Tile P&R flow issues occurring (nothing major)**
 - Most tiles making progress (through at least one pass)
 - Problematic tiles
 - DC: understanding clocks
 - RB: size - 500K instance tile
 - MH: currently not routable, iterating on floorplans
 - SX: routable (but need more X direction area), could impact top level floorplan
- **Top level P&R currently problematic**
 - Working with Cadence
 - Tool crashes, strange tool behavior
 - Some issues fixed, more to be addressed
 - Impacting ability to complete 1st iteration of toplevel P&R

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R400 Program Schedule

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Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
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Netlist 5.0	03-03-03	03-03-03	03-03-03
IKOS Emulation (w/ Software) begins	11-11-02	01-16-02	03-16-03
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Block Logic Design and Timing

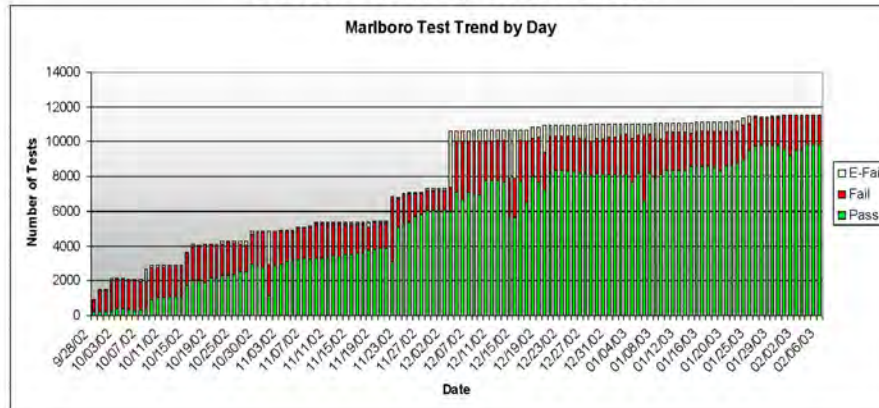
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MC/MH	100%	Done	N/A	100%	MC: 2.25; MH: 2.48	MC - MCLK: 2.35	59 / 258
AB/RB/RC	100%	Done	100%	81%	AB: 2.31; RB: 3.03; RC: 2.25		0.1 / 3557 / 0
SX/SQ	100%	Done	100%	100%	SX: 2.59; SQ: 3.25		53 / 335
SP	100%	Done	100%	100%	SP: 3.44		5810
TP/TCM/TCF/TCR	100%	Done	100%	86%	TP: 3.22; TCM: 2.25; TCF: 4.26; TCR: 2.79		485 / 0 / 5516 / 185
CG/CGM/ROM	100%	Done	N/A	95%	CG: 2.25; CGM: 2.25; DBG: 2.25		0
PA	100%	Done	100%	97%	PA: 2.28		2
VGT	100%	Done	100%	98%	VGT: 2.31		7
SC / SC_B	100%	Done	100%	89%	SC: 2.32 / SC_B: 2.25		19 / 0
RBBM	100%	Done	100%		RBBM: 2.34		1
CP	100%	Done	100%	100%	CP: 2.25		0
Display - DCP	100%	Done	100%	100%	DC: 2.62		152
Display - LB	100%	Done	100%	100%			
Display - SCL	100%	Done	100%	100%			
Display - CRTIC	100%	Done	100%	100%		PIXCLK: 2.55	
Display - DISPOUT	100%	Done	100%	100%			
Display - TVOUT	100%	Done	100%	100%			
VGA	100%	Done	100%	100%			
VIP	100%	Done	100%	100%			
BIF	100%	Done	90%	64%	BIF: 2.81	BCLK: 14nS; AGP: 3.50nS	140
IDCT	100%	Done	100%	100%	IDCT: 2.48		69

[Date/Time]

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Marlboro Blocks

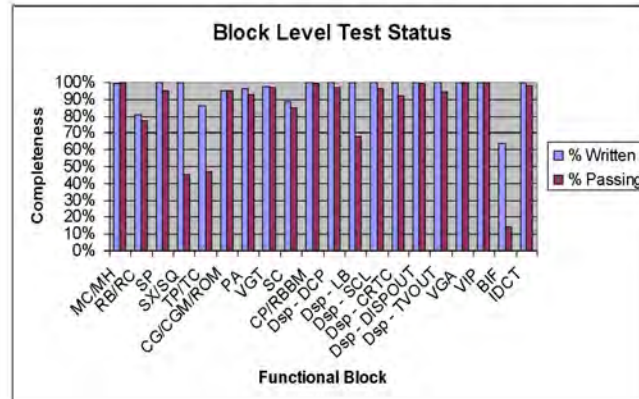


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Block Level Test Completeness



[DateTime]

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Executive Review – R400

February 24, 2003

[DateTime]

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Progress over past week was a disaster

- **Expected to show improvement in next couple days ...**
 - **Environment problems ...**
 - Testbench issues
 - With a snowstorm
 - **Netlist 4.0 delayed by 4.1 confusion**
 - **Emulator / RTL releases delayed**
 - Lost a motherboard on a fileserver
- **R400 Tapeout frequency**
 - R400 Marketing input
 - Given the R400 schedule, Marketing wants the high end sku to be >450 MHz
 - Synthesizing to 2.25ns (444MHz)
 - Not yet achieved...3 blocks still having trouble – TC, SP, RB
 - Tapeout expected at 2.5ns (400MHz) or better
 - If we do 2.5ns or better, we should get some yield at 450+ MHz

[DateTime]

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Design / Verification

- **SP**
 - Closed a substantial number of bugs on both hardware and emulator.
 - Problems were related to corner, boundary, special IEEE float values
 - Propagation of NaN values and last DOT opcodes fixes in flight
 - Remaining issues are believed to be emulator, SQ related and/or environment failures
 - Corrected three timing paths
 - Split the adder unit in scalar engine in two modules - a major timing fix that was required
 - Investigating new failing path
- **SQ/SX**
 - Identified SQ-SX open issues
 - Improving Orlando-Marlboro task organization, communication & coordination of these issues
 - Additional testbench development in process
 - More emulator data dumps with trackers are planned
 - MOVA tests caused by a known SQ issue (pixel vector export ordering)
 - Examining out of order completion
 - Reviewed feature focused testing
 - Some areas not covered in SQ test suite are covered in other block tests
 - Orlando and Marlboro team will create tests for any non-covered areas
 - SQ/SX may need an extra 4 weeks
- **RB / AB**
 - One resource dedicated to debug of multisample tests
 - Identified and corrected new architectural issues relating to precision
 - Debugging design and environment issues with compressed depth.
 - Timing has improved
 - Planning RB split for PD

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Design / Verification

- **MC/MH**
 - MC
 - Created architecture descriptions for GDDR2 and GDDR3.
 - Debugging GDDR3 in the MC and DRAM models.
 - Completed MC pad ring changes requested by SiV
 - Release pending for pad ring spreadsheet update.
 - Synthesized the latest MC for netlist 4.1. Checked in the netlist.
 - MH
 - Maintaining focus on single client randoms debug
 - Multiple client debug has started
 - Most effort spent on HI/VGA interaction
- **TP/TC**
 - TP
 - TP formatter verification nearly complete
 - Focus back on general TP debug
 - TC
 - TC performance issues
 - **Inadequate handling of AGP Vertex fetching latency**
 - **Poor sizing of cache lines for Vertex data**
 - » Architectural solution in review
 - **Still understanding impact ...**
 - » Simulations underway in Orlando
 - » Konstantine examining cache

[DateTime]

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Design / Verification

- CP / RBBM / VGT / PA / SC / SC_B
 - Focusing on 2D debug
- IDCT
 - Validated for closure
 - Released with Netlist 4.x
- DC
 - Target 2/28 for final netlist
 - Examining some design changes and system test issues
 - May be impacted 2 weeks for us to resolve issues.
- BIF
 - Feature coding complete
 - Test writing and debug progressing
 - Some dependency on MH debug

[DateTime]

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Block closures

- **Delivery targets**

Major Block	Plan	Last FC	Current FC
PA	12/16/2002	12/16/2002	12/16/2002
SC	12/16/2002	12/16/2002	12/16/2002
VG	12/16/2002	12/16/2002	12/16/2002
AB	11/18/2002	12/18/2002	12/18/2002
IDCT	12/20/2002	1/31/2003	1/31/2003
SP	11/18/2002	2/14/2003	2/14/2003
SX	12/2/2002	2/28/2003	5/30/2003
DC	12/20/2002	2/28/2003	2/28/2003
MC	12/16/2002	3/15/2003	3/15/2003
BIF	12/20/2002	3/15/2003	3/15/2003
MH	1/2/2003	3/15/2003	3/15/2003
CP	1/10/2003	3/31/2003	3/31/2003
RBBM	1/10/2003	3/31/2003	3/31/2003
RB	1/15/2003	4/10/2003	4/10/2003
TP	1/31/2003	4/30/2003	4/30/2003
TCM/TCF/TCR	1/31/2003	4/30/2003	6/15/2003
SQ	1/15/2003	5/1/2003	5/30/2003

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Physical Design

- **Tile P&R progressing on rel_3.0C**
 - **Some tiles still having problems making progress:**
 - DC - clock problems, constraints - most expected fixed in 4.0
 - SP - size makes turn times long
 - MH - routability issues - asking for some netlist changes, although not agreed upon yet
 - RB1/2 - size makes turn times long
 - BIF - many routing violations, not sure yet why
 - TC's - too "hacky" in netlist 3.0 timeframe to make good progress
 - **Other tiles go through the flow OK with approximately < 1ns timing violation**
 - Too early to call (KS, MC1, MC2, SI)
- **Top level P&R problems**
 - **First Encounter crashes**
 - **Currently doesn't route in nanoroute**
 - **Some fixes**
 - Repeater pin spacing problem
 - Missing grout area between core and pad due to manual die bloat in physical domain
 - New FE version from Cadence coming next week
 - Playing with grout width
 - Asking TSMC if thin M7 is a possibility or not
- **Continued flow refinement/enhancements**

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R400 Program Schedule

Task	Original	Last FC	Current FC
Emulator Test template Complete	01-18-02	01-18-02	Complete
GC Emulator integration - 1 triangle	02-22-02	02-21-02	Complete
Core Emulator pixel / shader tests run	03-15-02	03-19-02	Complete
Block Testing Begins	04-16-02	05-01-02	Complete
GC/Chip Integration Start	05-17-02	05-15-02	Complete
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	Complete
First Syntheses (n-1)	07-12-02	08-03-02	Complete
Verilog Feature Complete	09-16-02	10-31-02	Complete
Second Synthesis (n)	09-23-02	10-04-02	Complete
IKOS Emulation start	10-11-02	01-13-03	Complete
Third Synthesis	11-01-02	01-02-03	Complete
Early block delivery starts	11-08-02	12-16-02	Complete
Netlist 4.0	02-14-03	02-12-03	02-24-03
Netlist 5.0	03-03-03	03-03-03	03-24-03
IKOS Emulation (w/ Software) begins	11-11-02	03-16-02	TBD
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02	05-01-03	06-15-03
A11 Base Layers Tapeout	01-10-03	06-26-03	08-07-03
A11 Metal Layers Tapeout	01-24-03	07-10-03	08-21-03
First Samples for Engineering		09-12-03	10-24-03
R400 First Customer Samples		10-03-03	11-14-03
A12 Tapeout		10-17-03	11-28-03
A12 Samples for Engineering		11-28-03	01-10-04
R400 Customer Samples		12-05-03	01-16-04
Product Delivery		12-29-03	02-09-04

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Backup Slide

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Block Logic Design and Timing

Block	Percent Feature Complete	Forecast Feature Complete	Emulator Complete	Directed Tests Written	Synthesis W/C		TNS (nS)
					SCLK (2.25nS)	MCLK (1.67nS), PIXCLK (2.5nS), BCLK (14nS), AGP(3.5nS), TVCLK(10nS)	
MC/MH	100%	Done	N/A	100%	MC:2.25; MH: 2.47	MC - MCLK: 2.29	49 / 345
AB/RB/RC	100%	Done	100%	81%	AB: 2.29; RB: 2.89; RC:2.25		0.1 / 1657 / 0
SX/SQ	100%	Done	100%	100%	SX: 2.59; SQ: 2.83		53 / 531
SP	100%	Done	100%	100%	SP: 2.97		4679
TP/TCM/TCF/TCR	100%	Done	100%	86%	TP: 2.59; TCM: 2.25; TCF: 4.26; TCR:2.79		309 / 0 / 5516 / 185
CG/CGM/ROM	100%	Done	N/A	95%	CG: 2.25; CGM:2.25; DBG:2.25		0
PA	100%	Done	100%	96%	PA: 2.26		1
VGt	100%	Done	100%	99%	VGt: 2.27		0.2
SC / SC_B	100%	Done	100%	89%	SC: 2.31 / SC_B: 2.25		5 / 0
RBBM	100%	Done	100%		RBBM: 2.34		1
CP	100%	Done	100%	100%	CP: 2.25		0
Display - DCP	100%	Done	100%	99%	DC: 2.30		11
Display - LB	100%	Done	100%	92%			
Display - SCL	100%	Done	100%	100%			
Display - CRTc	100%	Done	100%	97%		PIXCLK: 2.50	
Display - DISPOUT	100%	Done	100%	100%			
Display - TVOUT	100%	Done	100%	100%			
VGA	100%	Done	100%	95%			
VIP	100%	Done	100%	100%			
BIF	100%	Done	90%	65%	BIF: 2.83	BCLK: 14nS; AGP:3.50nS	110
IDCT	100%	Done	100%	100%	IDCT: 2.25		0

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Executive Review – R400

March 10, 2003

[DateTime]

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What's happened on R400 ...

- **R400 Spring '04 production was at risk**
 - **Architectural performance problems were found in the Texture Cache**
 - Latency of Vertex fetching from AGP memory was not adequately handled
 - L2 Cache architecture was not well matched to vertex data
 - Net result – very noticeable performance degradation
 - **These problems are solvable, but would have schedule impact**
 - A re-architecting of the cache is required (which is in progress)
 - Completion of the re-design would have the following effects:
 - extend RTL freeze beyond June, 2003
 - push tapeout beyond October, 2003
 - push volume ramp beyond March, 2004
 - **ATI needs a new high end product in Q1, 2004**
 - R390 will be pushed quickly to a tapeout in September, 2003
 - The R400 will be reconstituted as the R500 with a new tapeout date
 - Establishing new schedule - estimated for January/February 2004
 - There is schedule pressure for a December tapeout

[DateTime]

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Where does R400 go next ?

- **R400 broke new ground**
 - Unified shaders & DX9 with Shader Model 3.0 support
 - It has a rich and valuable feature set
 - The current design will form the basis for the R500
- **The R500 differences will be limited**
 - The new tape out target must be hit
- **How will the R500 differ from the R400?**
 - The R500 will have a re-architected cache, optimized for vertex data and for texture data
 - The R500 will have 8 shader pipes (32 ops/cycle)
 - R400 had 4 (16 ops/cycle)
 - The R500 will be a PCI Express part rather than an AGP8X part
 - The R500 will be 90nm rather than 130nm process technology ?

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Process readiness is a problem

- TSMC will be able to accept initial tape out in their G process in 3Q03 (wafer out)
- Currently, there are not enough wafer starts for 4Q03 through 2Q04 (2-3K/Quarter)
- 3Q04 would be the first time enough slots to launch
- 110 nm LV+ could be a potential fallback, but it does not provide area reduction
 - There is limited availability of Low K dielectric material starts this year

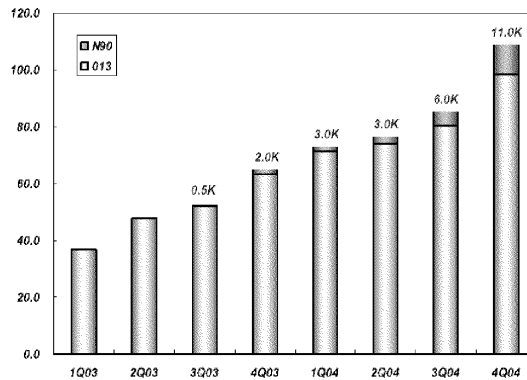
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TSMC 0.13um and 90nm Wafer Capacity (Unit: K pcs, 12" Equivalent)



PTM/JCHuang

Security - TSMC Confidential

Empowering Innovation

Date: 2/27/2003

1

[DateTime]

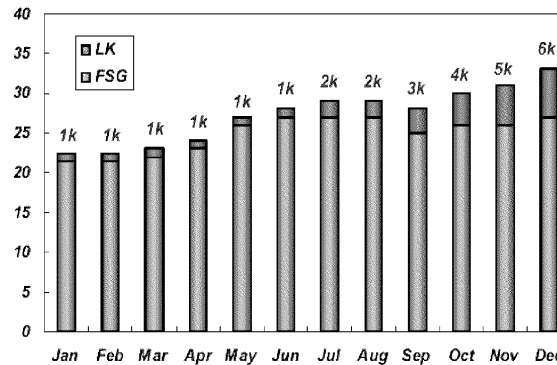
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Potential Low-K Capacity in Fab6

(Unit: K pcs, 8" Equivalent)



• Fab6 can maximize Low-K capacity to 6K/month in Q4/2003, however, we will need a 3-month lead time to make it happen.
• If needed, Fab12 Low-K capacity can also be made available for 0.13um production.

PTM/JCHuang

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Empowering Innovation

Date: 2/27/2003

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R400 moving forward ...

- The R400 will be the foundation for the new plan:
 - We need to complete as much of the R400 as we can as soon as we can.
 - This provides a stable code base to modify for the R500
- The Software team has requested a continuance of support for IKOS with the R400 code base
 - Much of the driver has been re-written to support the R400
 - Extended emulator and IKOS time allows the driver to be in a better state when the chip is ready for bring-up.
 - A higher quality driver at the time of bring-up should help shorten time to volume production.
 - This will likely impact the BIF, TC and SQ teams...they may have to support the R400 in IKOS while starting work on the R500.

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R400 moving forward ...

- Process changes
 - Examining closely the block status in R400
 - Including the additional work for R500
 - Added shader pipes, PCI express, new IP, etc.
 - Developing a detailed task list
 - Load will be balanced among sites
 - Investigating improvements with emulation/simulation
- Planning a schedule from this effort
 - Goal is a tapeout in January '04 (± 1 month)

[DateTime]

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Executive Review – R400

March 24, 2003

[DateTime]

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Overview of today's discussion

- **Schedule Development**
- **Major Block Summary**
- **Schedule Summary**
- **IKOS**
- **Silicon Process (90nm)**
- **Projected Area / Cost**

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Progress on R400/R500 schedule analysis

- **Analysis of the issues and process of R400**
 - **Management Structure**
 - Team and Block management will be restructured
 - Responsibilities will be more vertically integrated
 - This will be rolled out to the team this week
 - **More human resources were needed on Marlboro Blocks**
 - Have been working with each block lead
 - Listing tasks and effort to complete R400
 - Developing tasks and impact of changes for R500 completion
 - **Reviewing test plans and methods of reporting**
 - Review blocks for proper coverage
 - Use smaller testbenches (in some cases) and reporting of results
- **Load balancing of work is underway with Orlando**
 - **Work has been shifted**
 - SQ work has been pushed to Orlando
 - SX tasks to simplify the SQ implementation are also shifted
 - In addition the new VC block is being designed in Orlando

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Progress on R400/R500 schedule analysis

- **Resource balancing in Marlboro**
 - **Identified holes in the staffing plan**
 - Some solutions identified, more work required
 - **Original R400 plan called for shared resources**
 - Two resources on SP and MH were to be shared
 - One to assist TP to completion and the other to assist RB to completion
 - However, changes for R500 impacted this
 - It will be too long before they can contribute useful work on either TP or RB
 - **RenderBackend**
 - The RB requires an additional senior resource to assist Jay Wilkinson
 - One lead to drive the RB_depth logic on schedule
 - The other to drive the RB_color logic on schedule
 - Currently planning on this to be Mark Sprague
 - Impact: Creates another hole in 90 nm synthesis and libraries
 - Risks
 - one resource may be impacted by the yearly personnel review cycle
 - one is contractor who's contract will expire (may not be able to retain him)

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Progress on R400/R500 schedule analysis

- **Resource balancing in Marlboro (continued)**

- **Texture Units**

- Shifted verification resource to full time on TP (originally shared with TC)
 - TC verification hole backfilled with another resource
 - TP was expecting a resource from the SP (knowledgeable in math operations)
 - A hole exists for a senior resource to drive to this conclusion
 - No identified solution for this problem, may need to hire

- **Memory**

- Reallocated Frank Hering to drive MC/MH to closure
 - Created a hole for leading the chip integration effort
 - No solution identified yet, may need to hire

- **Software Team assistance**

- **Verification thoroughness**

- Capturing packets from SW stress tests for hardware playback
 - Will write additional tests as identified

- **Emulator assistance**

- Build process
 - Speed

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R500 Blocks are progressing

- **Major Block Summary**

- **MC/MH**

- Complete by end of July
 - MH work includes R500 changes for PCI Express
 - MC will need to adjust to pad changes and any new memories that arise

- **RB**

- Complete by mid-September
 - Past week showed good progress on tile and depth logic

- **SP**

- R500 complete by end of June
 - Random test time is an additional 8 weeks
 - SP is passing 97% of directed (last 3% tracked to SP/SX or RB issues)
 - Infinity propagation precision issues persist in random tests

[DateTime]

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R500 Blocks are progressing

- **Major Block Summary**

- **SQ/SX**

- R400 features to be stable by mid-May with a month of random debug
 - R500 schedule under development
 - Schedule development slowed by R390 work

- **TP**

- Estimated complete by October (assumes adding a resource)
 - Adding six sub-block test benches to aid debug
 - Schedule acceleration from new sub-block testbenches has not been taken into account

- **TC**

- Estimated complete by mid-September
 - Old TC will be replaced by new TC in GC/Chip level sim by mid-June

- **VC: Vertex Cache (new block)**

- VC schedule expected in two weeks

- **Remaining blocks are not the long pole items**

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IKOS

- **Netlist 4.1 is the final R400 synchronized netlist**
 - RTL compilations of blocks will continue as needed (e.g. MH)
 - In parallel, work will continue on full chip RTL compilation
 - BIOS team will use this netlist first
 - Diagnostics, VGA and Display will use thru June
 - Switch to new SQ and TC (R500) in mid-June
 - Availability for IKOS approximately mid/late July
 - Allowing time to work through issues
- **IKOS progress on 4.1**
 - Memory reads/writes working
 - Register reads making progress
 - Display is up and working !

[DateTime]

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Silicon Process (90nm) Issues

- Currently planning December for 90nm IP ready
 - Raj Verma is developing the plan to get there
 - Test chip and IP development objectives
 - This plan is expected imminently
 - Part of this plan could be outsourcing IP
- Most importantly ...
 - Need to pick a process
 - At a minimum, TSMC needs a faster transistor

[DateTime]

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Current projected schedule / cost

- Schedule

- Chip Level Randoms Start July '03
- RTL Freeze October '03
- Tapeout (in 90nm) February '04

- Cost Estimates (*need to validate cost model used*) 8in. Wafer

- R500 in 130 nm
 - 17.86 mm/side
 - \$144 (2004Q3)
- R500 in 90 nm (assumes DD is 0.5 and wafer costs similar with 130)
 - 13.80 mm/side
 - \$156 (2004Q3) / \$85 (2005Q1)

[DateTime]

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Executive Review – R400

April 7, 2003

[DateTime]

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1

Overview of today's discussion

- **Major Block Summary**
- **Block Schedule Summary**
- **Schedule Risks**
- **High Level Schedule**

[DateTime]

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Progress on R400/R500

- **Restructuring and load balancing complete**
 - **Management Structure rolled out**
 - Team and Block management has been restructured
 - Responsibilities are now more vertically integrated
 - **Restructuring based on block tasks and R500 impact**
 - Reallocated resources to blocks
 - **Reviewing test plans and methods of reporting**
 - Block reviews beginning
 - Smaller testbenches coming online
 - **Vertex Cache (VC) is being designed in Orlando**
 - SQ/SX tasks also have been shifted Orlando

[DateTime]

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R500 Blocks are progressing

- **Block Summary**
 - **MC/MH**
 - Debug of randoms continues, at 82% passing
 - Updated MH released to IKOS for RTL compilation
 - Display client performance issue known, to be addressed next week
 - MC pad interface validation progressing well
 - **RB**
 - RB depth system under review
 - Color and Tile system fairly stable
 - **SP**
 - SP is passing 99.8% of directed and 92% of Randoms
 - (last errors tracked to SQ/SX or RB issues)
 - R500 work has begun to split out interpolators
 - Open issues with TC and VC interface need to be resolved
 - **TP**
 - Added a resource to TP starting 4/21/2003
 - TP is investing time developing more solid block level test bench strategy
 - Schedule acceleration from new sub-block testbenches has not been taken into account
 - **TC**
 - TC is partially stable and progressing well

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R500 Blocks are progressing

- CP/RBBM
 - Considering adding minimal risk changes (previous requests that were denied due to schedule)
 - Validation: Block tests at 100%
 - Synthesis: Completed (feedback from PD team open)
 - Performance: No known issues
- PA
 - Design: 2X Shader Pipes, Subpixel precision increase TBD
 - Validation: 99% for R400, randoms running and passing
 - ~20 new tests for R500
 - Synthesis: Meet 2.25ns for R400
 - Performance: 100 % for R400
- VGT
 - Design: 2X Shader Pipes (est. 2 week + 1 week validation)
 - Validation: 99 % for R400, Randoms running and passing
 - Meet 2.25ns for R400
 - Performance: 100 % for R400

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R500 Blocks are progressing

– SC

- Design: 2X Shader Pipes, Subpixel precision increase, HiZ Reject - TBD
- Validation: 99 % for R400, randoms running and passing
 - ~20 new tests for R500
- Synthesis: Meet 2.25ns for R400
- Performance: 100 % for R400

– SQ

- Built block level testbench (SQ/SP)
- Validation starting, 25% tests passing

– SX

- Block test bench has been creating, regressions starting this week
- Will start reporting status next week
- Missing timing by .50 ns (-22%)

[DateTime]

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R500 Blocks are progressing

- VC: Vertex Cache (new block)
 - Architecture 70% complete
 - Performance model and real app data used to architect design
 - Meeting scheduled 4/7 to wrap up open issues
 - this is critical for RTL coding to start next week
 - Requires schedule issues to be worked
- DC
 - Cleaning up system stress tests
 - Splitting DC
 - Beginning
- BIF
 - Continuing support of AGP8x

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Block Summary

Block Description	Current Status		
	BCP-A	BCP-B	BCP-C
SQ R400 Base	4/30/03	6/30/03 (goal) 7/30/03 (>80%)*	8/30/03 (goal)
SQ - R500 changes - 2X ALU's	5/30/03	7/30/03 (goal) 8/30/03 (>80%)*	9/30/03 (goal)
SX	5/15/03	6/30/03	8/30/03
PA - R500 changes - Increase subpix accuracy	5/7/03	5/30/03	6/30/03
SC - R500 changes - Increase subpix accuracy	5/7/03	5/30/03	6/30/03
VC	6/30/2003 (goal)	8/30/03 (goal) 9/30/03 (>80%)*	10/30/03 (goal)
VGT - R500 changes - 2X ALU's	5/7/03	5/30/03	6/30/03
RBBM - R500 changes	Complete	Complete	6/30/03
CP - R500 changes	Complete	Complete	6/30/03
RB	5/15/2003 - 5/29/2003	6/30/2003 - 7/7/2003	9/30/03
TC	5/15/03	6/30/03	9/30/03
TP	5/15/2003 - 5/29/2003	6/30/2003 - 7/7/2003	9/30/03
SP	Complete	6/30/2003 (possibly early)	9/30/2003 (possibly early)
DC	Complete	5/30/03	7/30/03
DCT	Complete	5/30/03	7/30/03
BIF - PCIExpress	Complete (as IP)	8/30/03	9/30/03

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Risks/Issues

- Change for 2x/4x Hi-Z discard not considered
- Orlando blocks need to hit goal targets
 - 2x ALUs not a major impact
- Long Pole is Vertex Cache (VC)
 - Need to work on the scheduling of this outlier
 - Full chip validation to start in earnest in late July
 - Need discuss coordination of TC covering vertex fetches
 - Temporary until VC available in late August
 - Late VC availability affects vertex performance testing
 - Allows about 1 month prior to RTL freeze (similar to R300)
 - Can begin with pixel performance testing
 - R400 SQ base can be used for Full Chip Validation
 - Cut in R500 changes after tested in local test bench
- TP block is a risk for completion; it needs to hit its goals
 - Mitigation: adding new TP resource but ramp time required
- 90nm technology and IP delivery
- PD schedule in discussion

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R500 Schedule

Task	Plan	Last FC	Current FC
Preliminary Netlist NL0 (Top Level)	5/30/2003	5/30/2003	5/30/2003
Block Checkpoint B	6/30/2003	6/30/2003	6/30/2003
Physical Floorplanning Netlist NL1	7/15/2003	7/15/2003	7/15/2003
IKOS start on R500 Netlist	7/30/2003	7/30/2003	7/30/2003
Netlist Delivery - NL2	TBD	TBD	TBD
Netlist Delivery - NL3	TBD	TBD	TBD
RTL frozen (Gate ECOs only)	10/1/2003	10/1/2003	10/1/2003
Final NetList	10/15/2003	10/15/2003	10/15/2003
IP Ready for integration (90nm)	12/30/2003	12/30/2003	12/30/2003
A11 Base Layer Tapeout	2/13/2004	2/13/2004	2/13/2004
A11 Metal Layer Tapeout	2/27/2004	2/27/2004	2/27/2004
First Samples for Engineering	4/13/2004	4/13/2004	4/13/2004
First Samples for Customers	5/4/2004	5/4/2004	5/4/2004
A12 Tapeout	5/18/2004	5/18/2004	5/18/2004
A12 Samples for Engineering	6/29/2004	6/29/2004	6/29/2004
R500 Customer Samples	7/13/2004	7/13/2004	7/13/2004
Product Delivery	8/15/2004	8/15/2004	8/15/2004

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Back-up slides

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High Level BCP definitions

- BCP – A (5/15/03)
 - 40% tests passing
 - Test plan complete / Testbenches functional
 - 90% area accurate
- BCP – B (6/30/03)
 - Block Design 100% complete
 - 80% tests passing
 - Synthesis within 5% of timing target
- BCP – C (9/30/03)
 - RTL frozen, 100% Block level passing
 - 100% Gate sims passing
 - 100% line and clause coverage
 - Meets timing, PD review and issues addressed

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