

Change 85595 on 2003/02/20 by scamlin@scamlin_crayola_unix_orl

added testreg

Change 85139 on 2003/02/18 by grayc@grayc_crayola_linux_orl

changed path to gfxcore in vgttracker
fixes for tracker checking

Change 83338 on 2003/02/10 by hartogs@fl_hartogs2

Changed/added ifdef SIM code to prevent error messages that are a result of changing the programmable FIFO depth.

Change 82868 on 2003/02/07 by hartogs@fl_hartogs2

Changed testbench to cause "wait for idle" before allowing a write to the VGT_VTX_VECT_EJECT_REG.

Change 82847 on 2003/02/07 by hartogs@fl_hartogs2

Added grep for error messages even when test passes.

Change 82200 on 2003/02/05 by scamlin@scamlin_crayola_unix_orl

forgot these fuseboxes

Change 81602 on 2003/02/03 by smoss@FL_REGRESS_P4L_crayola_win

changed netlist from vgt.cot.v to ks.cot.v

Change 81502 on 2003/02/03 by hartogs@fl_hartogs2

Added vgt_tb/vgttbtrk_inf.v to makefile

Change 81153 on 2003/01/31 by viviana@viviana_crayola_linux_orl

Tracker added to check the vgt interfaces and use it at the chip, gc and block levels.

Change 81152 on 2003/01/31 by viviana@viviana_crayola_linux_orl

Changed the vgt_tb.v and buildtb to pull out of the testbench the vgt interface trackers so
that they could be used at the Chip and GC level.

Change 80854 on 2003/01/30 by bbuchner@fl_bbuchner_r400_win

add configuration file for VGT perfmon

Change 80569 on 2003/01/29 by hartogs@fl_hartogs2

Added VGT_DEBUG_CNTL, VGT_DEBUG_DATA, VGT_PERFCOUNTER[0-3]_SELECT, VGT_PERFCOUNTER[0-3]_LOW, and VGT_PERFCOUNTER[0-3]_HI registers to the emulator and vgtbtrk_rbbmrd. In the tracker, separated non-GFX registers into two groups: test read back data and don't test read back data.

Change 79929 on 2003/01/28 by hartogs@hartogs_crayola_unix_orl

Added signal missing from sensitivity list.

Change 79892 on 2003/01/28 by hartogs@fl_hartogs

Fixed yet another erroneous 'x' assignment found by Randy.

Change 79665 on 2003/01/27 by hartogs@fl_hartogs

Moved 'end' to be outside `ifdef SIM block.

Change 79635 on 2003/01/27 by hartogs@fl_hartogs

Fixed VGT_SQ continued flag to match spec description.

Change 79374 on 2003/01/24 by hartogs@fl_hartogs2

Dummy files for vgt RTL testbench.

Change 79141 on 2003/01/24 by smoss@smoss_crayola_linux_orl_regress

changed atipli to tb_utils

Change 78670 on 2003/01/22 by smoss@FL_REGRESS_P4L_crayola_win

Placed vsim arguments into a variable and added +notimingchecks argument.

Change 78296 on 2003/01/21 by smoss@FL_REGRESS_P4L_crayola_win

Removed grouper tracker for gate sims.

Change 78003 on 2003/01/20 by hartogs@fl_hartogs2

Removed rbbmRd.dmp

Change 78001 on 2003/01/20 by scamlin@fl_regress_p4j_crayola_win

mod for a04

Change 77995 on 2003/01/20 by hartogs@fl_hartogs2

"Fixed" valid bit for quad-composition case so that grouper tracker would not mis-match

Change 77932 on 2003/01/20 by hartogs@fl_hartogs2

Removed fusebox

Change 77534 on 2003/01/17 by scamlin@fl_regress_p4j_crayola_win

update for A04

Change 77508 on 2003/01/17 by scamlin@scamlin_crayola_unix_orl

need to move fusebox to TST block

Change 77501 on 2003/01/17 by scamlin@scamlin_crayola_unix_orl

A04

Change 76875 on 2003/01/15 by bbuchner@fl_bbuchner_r400_win

genperfcode changed, so regenerated this file

Change 76810 on 2003/01/15 by fhsien@fhsien_r400_linux_marlboro

Change MES_ALL parameter to OFF

Change 76595 on 2003/01/14 by bbuchner@fl_bbuchner2_r400_win

improve vgt te output timing

Change 76432 on 2003/01/14 by smoss@smoss_crayola_linux_orl_regress

removed vgtgrpout dump

Change 76406 on 2003/01/14 by smoss@smoss_crayola_linux_orl_regress

added dummy file

Change 76218 on 2003/01/13 by smoss@smoss_crayola_linux_orl_regress

increased idle_clocks timeout

Change 76107 on 2003/01/13 by bbuchner@fl_bbuchner2_r400_win

convert state machine to one-hot

Change 75944 on 2003/01/10 by hartogs@fl_hartogs

Moved mh_vgt_tag_7_q from rbiu readback bus to debug read bus because rbiu test was failing.

Change 75839 on 2003/01/10 by viviana@viviana_crayola_linux_orl

Added a test to write and read all context registers and changed the vgtbtrk_rbbmrd to handle
all contexts.

Change 75582 on 2003/01/09 by scamlin@scamlin_crayola_win

minor update

Change 75516 on 2003/01/09 by viviana@viviana_crayola_linux_orl

Changed the GetVec function to get rbbm.dmp instead of rbbmRd.dmp.

Change 75493 on 2003/01/09 by hartogs@fl_hartogs

Re-ordered three case statements for better coverage results.

Change 75460 on 2003/01/09 by viviana@viviana_crayola_linux_orl

Changed the file so that the rbbm reads can be compared from rbbm.dmp instead of rbbmRd.dmp.

Change 75313 on 2003/01/08 by hartogs@fl_hartogs2

Added stuff related to new grouper tracker.

Change 75268 on 2003/01/08 by scamlin@scamlin_crayola_win

virage rf test

Change 75224 on 2003/01/08 by hartogs@fl_hartogs

Added signal missing from sensitivity list. Added default assignment for input of new register.

Change 75212 on 2003/01/08 by hartogs@fl_hartogs

Cleaned-up previous change.

Change 75211 on 2003/01/08 by hartogs@fl_hartogs

Hooked-up PA_SU_SC_MODE_CNTL bit for provoking vertex to the pass thru block.

Added code to cause the passthru block to perform index re-ordering for tri-strips.

Change 75065 on 2003/01/07 by bbuchner@fl_bbuchner_r400_win

modified for vcs coverage

Change 75057 on 2003/01/07 by bbuchner@fl_bbuchner_r400_win

added more perf monitor values

Change 74837 on 2003/01/06 by hartogs@fl_hartogs

Added a tracker at the output of the grouper. This tracker is currently only enabled by a command line switch.

Change 74836 on 2003/01/06 by hartogs@fl_hartogs

Added signal missing from sensitivity list.

Change 74834 on 2003/01/06 by hartogs@fl_hartogs

Removed stride==0 conditions. Situation avoided with new grouper programming rules.

Change 74525 on 2003/01/04 by smoss@smoss_crayola_linux_orl_regress

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Change 74333 on 2003/01/03 by hartogs@fl_hartogs2

Found bug where first grouper vector has stride == 0, but the grouper, because of backpressure, cannot extract the first

vector immediately after loading the draw initiator. In this case, the shifter was pre-loading (because of the load

of the draw_initiator) but the data was not needed. This messed up the shift calculation. The fix was to prevent

pre-loading of the shifter with the draw_initiator if the first vector (vect 0) for that draw_initiator has a stride of zero.

Change 74299 on 2003/01/03 by hartogs@fl_hartogs2

Added ability to supply random seed as third argument in single-test mode.

Change 74202 on 2003/01/02 by hartogs@fl_hartogs

Added rbbmRd.dmp to list of vgt_tb files copied.

Added ability to handle changes to ROM_BAD_PIPE_DISABLE_REGISTER including a test_bench stall untill VGT is idle before changing the pipe disable bits.

Change 74155 on 2003/01/02 by hartogs@fl_hartogs

Removed "DEBUSSY" compile directive.

Change 74143 on 2003/01/02 by hartogs@fl_hartogs2

Changed dealloc size (in vertices) to be based on number of active pipes.

Change 74090 on 2003/01/02 by hartogs@fl_hartogs

Turned of coverage for an available configuration that will not be tested.

Simplified condition for "second_pass_rl_q" block that could not be reached (discovered by VCS coverage). Added error detection for un-reachable path.

Change 74087 on 2003/01/02 by hartogs@fl_hartogs

Turned-off VCS coverage for a case statement default.

Change 72974 on 2002/12/20 by hartogs@fl_hartogs2

Set default to behavioral memory models.

Change 72921 on 2002/12/20 by hartogs@fl_hartogs2

Changed testbench to ignore indx1 and indx2 for points and indx2 for lines.

Change 72792 on 2002/12/20 by hartogs@fl_hartogs

Connected grp_dma_read and dma_grp_valid signals to the top level of the VGT.

Change 72762 on 2002/12/20 by hartogs@fl_hartogs2

More filter changes for gate-level simulation.

Change 72742 on 2002/12/20 by hartogs@fl_hartogs2

Changed warning filter for gate-level simulations.

Change 72711 on 2002/12/20 by hartogs@fl_hartogs2

Chaged default to GATES=0

Change 72648 on 2002/12/19 by dclifton@dclifton_r400

a few changes to run gate sims.

Change 72490 on 2002/12/19 by hartogs@fl_hartogs

Turned off VCS coverage analysis for `ifdef SIM code.

Change 72372 on 2002/12/19 by smoss@smoss_crayola_linux_orl_regress

works better for coverage

Change 72030 on 2002/12/18 by smoss@smoss_crayola_linux_orl_regress

added rbbmRd dump file

Change 71999 on 2002/12/18 by hartogs@fl_hartogs

Made change so that VIZQUERY_START event will mark the state context active in the testbench.

Change 71860 on 2002/12/17 by hartogs@fl_hartogs

Connected MH_VGT_tag[7] to the register readback bus to prevent the gate-eater from deleting the register and then the port.

Change 71731 on 2002/12/17 by hartogs@hartogs_crayola_unix_orl

Reverted back to revision 76.

Change 71730 on 2002/12/17 by hartogs@hartogs_crayola_unix_orl

Reverted back to revision 97.

Change 71727 on 2002/12/17 by hartogs@hartogs_crayola_unix_orl

Reverted back to revision 39.

Change 71439 on 2002/12/16 by bbuchner@fl_bbuchner_r400_win

typo

Change 71433 on 2002/12/16 by bbuchner@fl_bbuchner_r400_win

flop unused bit 7 of MH_VGT_TAG bus.

Change 71149 on 2002/12/13 by hartogs@fl_hartogs

Timing change.

Change 71130 on 2002/12/13 by hartogs@fl_hartogs

Connected programmable FIFO depth for draw_initiator FIFO and for dma_request FIFO.

Change 71121 on 2002/12/13 by hartogs@fl_hartogs

Hooked VGT_PA_clip_v_stalled and VGT_PA_clip_s_stalled to the vgt_perf_cntl block.
Changed expression for stall condition for VGT_SQ_stalled and VGT_PA_clip_p_stalled.

Change 71096 on 2002/12/13 by hartogs@fl_hartogs

Added signals missing from sensitivity list.

Change 71090 on 2002/12/13 by hartogs@fl_hartogs

Fixed random FIFO depth values to dis-allow zero depths.

Change 71046 on 2002/12/13 by hartogs@fl_hartogs

Moved a computation to the other side of the prim fifo for timing.

Change 71026 on 2002/12/13 by hartogs@fl_hartogs2

Added ability for testbench to randomize depths of FIFOs whose depths are programmable.

Change 70972 on 2002/12/13 by hartogs@fl_hartogs

Timing changes. Should be no functional change.

Change 70880 on 2002/12/12 by hartogs@fl_hartogs2

Switched files used to detect "NOFILE" case.

Change 70878 on 2002/12/12 by hartogs@hartogs_crayola_unix_orl

Added missing signal to sensitivity list.
Fixed port names for STAR signals going to vgt_dma block.

Change 70873 on 2002/12/12 by hartogs@hartogs_crayola_unix_orl

Added missing signal to sensitivity list.

Change 70872 on 2002/12/12 by hartogs@hartogs_crayola_unix_orl

Fixed a ',' that should have been a 'or' in a sensitivity list

Change 70870 on 2002/12/12 by hartogs@hartogs_crayola_unix_orl

Fixed ',' that should have been 'or' in sensitivity list.

Change 70865 on 2002/12/12 by hartogs@fl_hartogs2

Moved the DMA engine to be within the grouper. This was done to help synthesis timing problems between the DMA engine and the grouper.

Change 70864 on 2002/12/12 by hartogs@fl_hartogs2

Fixed again.

Change 70844 on 2002/12/12 by hartogs@fl_hartogs2

Fixed some simulation only check code.

Change 70812 on 2002/12/12 by hartogs@fl_hartogs2

Changed grouper to ignore major mode zero packets with prim type 0.

Change 70788 on 2002/12/12 by bbuchner@fl_bbuchner_r400_win

updated to match tessellator engine changes (addition of null prim)

Change 70787 on 2002/12/12 by bbuchner@fl_bbuchner_r400_win

reduce critical timing path of OKAY_TO_ADVANCE in walker unit
and of 19 bit subtractors in the output unit

Change 70677 on 2002/12/12 by hartogs@fl_hartogs2

Moved updated Virage STAR memory files from src/gfx/vgt to src/gfx/vgt/vgt_tb

Change 70672 on 2002/12/12 by hartogs@fl_hartogs2

Added vgtbtrk_rbbmrd module to Makefile.

Added "register_addr.v" include file to vgtbtrk_rbbmrd.v.

Change 70566 on 2002/12/11 by viviana@viviana_crayola_linux_orl

Added vgtbtrk_rbbmrd.v to the testbench to track rbbm bus reads.

Change 70446 on 2002/12/11 by viviana@viviana_crayola_linux_orl

Added VGT_ENHANCE register select to read strobe equation.

Change 70394 on 2002/12/11 by hartogs@fl_hartogs

Moved resource statements into separate labeled "begin-end" blocks

Change 70381 on 2002/12/11 by hartogs@fl_hartogs

Specified particular DW multipliers for two operators.

Change 70314 on 2002/12/11 by dclifton@dclifton_r400

Initial check-in of gate rep of vgt rams-Dec 9 compile

Change 70276 on 2002/12/11 by bbuchner@fl_bbuchner_r400_win

signal was incorrectly labelled as input

Change 70126 on 2002/12/10 by bbuchner@fl_bbuchner_r400_win

regenerated vgt_perfmon.v after change to genperfcode program

Change 70042 on 2002/12/10 by hartogs@fl_hartogs

Updated some port widths for sub-block ports to clean-up synthesis lint messages.
This change requires a corresponding vgt.blk file change.

Change 69937 on 2002/12/10 by hartogs@fl_hartogs

Moved local variable declarations out of the always blocks.

Change 69687 on 2002/12/09 by scamlin@scamlin_crayola_unix_orl

update vgt memories

Change 69686 on 2002/12/09 by scamlin@scamlin_crayola_unix_orl

update vgt memories

Change 69674 on 2002/12/09 by hartogs@fl_hartogs

Wired-up the busy signals for the VGT_CNTL_STATUS register.
Changed width of p1500 bus from 6:0 to 5:0.

Change 69624 on 2002/12/09 by hartogs@fl_hartogs

Changed TST_VGT_rf_star_p1500 from 6:0 to 5:0

Change 69573 on 2002/12/09 by bbuchner@fl_bbuchner_r400_win

corrected use of I/O for debug/perf blocks

Change 69352 on 2002/12/06 by hartogs@fl_hartogs

Fixed multi-prim reset enable state arriving at wrong time.

Change 69338 on 2002/12/06 by hartogs@fl_hartogs

Fixed erroneous load of packet data.

Change 69308 on 2002/12/06 by hartogs@fl_hartogs

Fixed cut-and-paste typo.

Change 69266 on 2002/12/06 by bbuchner@fl_bbuchner_r400_win

corrected instances where I/O signals were being used.

Change 69224 on 2002/12/06 by hartogs@fl_hartogs

Changed new signal name to match naming convention for temps.

Change 69219 on 2002/12/06 by hartogs@fl_hartogs

Added code to handle 2-vector group where first vector has stride of zero.
Also added condition to prevent shifter preload for zero stride groups.

Change 69193 on 2002/12/06 by hartogs@fl_hartogs

Added VGT_CNTL_STATUS register.

Deleted VGT_PASS_THRU_CNTL register.

Wired up debug reads for vgt_grouper and vgt_output block.

Change 69052 on 2002/12/06 by smoss@smoss_crayola_linux_orl

mem on

Change 68866 on 2002/12/05 by bbuchner@fl_bbuchner_r400_win

fixed bug with validation null_verts from walker to output unit.
Fixes r400vgyt_hos_multiprim_reset_index_01 test.

Change 68777 on 2002/12/05 by scamlin@scamlin_crayola_unix_orl

add fusebox

Change 68331 on 2002/12/04 by grayc@chip_regress_orl

removed define

Change 68313 on 2002/12/04 by smoss@smoss_crayola_linux_orl_regress

removed all pass-thru instances!!

Change 68215 on 2002/12/03 by bbuchner@fl_bbuchner_r400_win

fixed perf monitoring bugs. Created new vgt_perfmon.v after update to genperfmon.

Change 67816 on 2002/12/02 by hartogs@hartogs_crayola_unix_orl

Moved the perf monitor block onto the registered version of the RBBM bus.

Change 67554 on 2002/11/29 by smoss@smoss_crayola_linux_orl_regress

removed coverage

Change 67235 on 2002/11/27 by scamlin@scamlin_crayola_unix_orl

fusebox

Change 66371 on 2002/11/22 by smoss@smoss_crayola_linux_orl_regress

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Change 66321 on 2002/11/22 by hartogs@fl_hartogs

Added delay chain stuff.

Change 66320 on 2002/11/22 by hartogs@hartogs_crayola_unix_orl

Added delay chain.

Change 66051 on 2002/11/21 by hartogs@fl_hartogs

Tie-off the Virage STAR processor signals.

Change 66048 on 2002/11/21 by hartogs@fl_hartogs

Virage Memory Chain-- Star processor hookup

Change 66035 on 2002/11/21 by smoss@smoss_crayola_linux_orl_regress

update

Change 65255 on 2002/11/19 by smoss@smoss_crayola_linux_orl_regress

update

Change 65216 on 2002/11/19 by viviana@viviana_crayola_unix_orl

Virage Memories System file.

Change 65179 on 2002/11/19 by bbuchner@fl_bbuchner_r400_win

changed performance clock to be the permanent clock
fixed two incorrect signal names

Change 65170 on 2002/11/19 by viviana@viviana_crayola_unix_orl

Virage memory processor and all the new Virage memories.

Change 65145 on 2002/11/19 by viviana@viviana_crayola_unix_orl

Deleted old Virage memory files.

Change 63572 on 2002/11/12 by hartogs@hartogs_crayola_unix_orl

Fixed some synthesis errors in new code.

Change 63078 on 2002/11/11 by viviana@viviana_crayola_unix_orl

Added configuragion files for the Virage memories and new rtl generated.

Change 62956 on 2002/11/08 by grayc@grayc_crayola_linux_orl

added 4 new files

Change 62870 on 2002/11/08 by bbuchner@fl_bbuchner_r400_win

new modules for performance monitoring and debug register

Change 62810 on 2002/11/08 by bbuchner@fl_bbuchner_r400_win

Added debug register and control.
Added performance monitoring logic.

Change 62125 on 2002/11/06 by viviana@viviana_crayola_unix_orl

Models for the virage memories.

Change 61262 on 2002/11/03 by hartogs@hartogs_crayola_unix_orl

Added (again) the vgt_reset block to the vgt.v and vgt.syn files.
Changed clock period from 2.5ns to 2.25ns in vgt.io.scr.

Change 61243 on 2002/11/02 by smoss@smoss_crayola_linux_orl_regress

new input directory for linux

Change 61130 on 2002/11/01 by smoss@smoss_crayola_linux_orl_regress

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Change 60809 on 2002/10/31 by hartogs@fl_hartogs2

Added second level of reset registers.

Change 60673 on 2002/10/31 by smoss@smoss_crayola_win

using link instead

Change 60532 on 2002/10/30 by smoss@smoss_crayola_linux_orl_regress

updated for coverage

Change 60490 on 2002/10/30 by hartogs@fl_hartogs

Added programmable depth state registers for draw initiator fifo, dma request fifo, and dma data fifo. Increased size of draw initiator fifo and dma request fifo from 8 to 32 entries.

Added register "LAST_COPY_STATE" to read back the source and destination context ids from the last GFX_COPY_STATE command.

Change 60127 on 2002/10/29 by smoss@smoss_crayola_linux_orl_regress

Coverage for VGT

Change 59903 on 2002/10/29 by smoss@smoss_crayola_linux_orl_regress

update

Change 59804 on 2002/10/28 by bbuchner@fl_bbuchner_r400_win

allow writes to index fifo even for null prims.

Change 59803 on 2002/10/28 by bbuchner@fl_bbuchner_r400_win

Change to named, rather than positional, ports

Change 59759 on 2002/10/28 by hartogs@fl_hartogs2

Added some error checking code. No functional change.

Change 59466 on 2002/10/25 by hartogs@fl_hartogs2

Changed ROM_SPx_disable signals.

Change 58721 on 2002/10/22 by hartogs@fl_hartogs

Added missing sensitivity list signals.

Change 58671 on 2002/10/22 by hartogs@fl_hartogs

Correct 2 vector compound index shifting for bug found by Vineet's adaptive test.

Change 58335 on 2002/10/21 by hartogs@fl_hartogs

Hooked Virage memory RST pin to hard reset.

Change 58311 on 2002/10/21 by hartogs@fl_hartogs

Hooked up Virage STAR bus to registered version of reset.

Change 57675 on 2002/10/17 by hartogs@fl_hartogs

Added Virage memory simulation models.

Change 57561 on 2002/10/16 by hartogs@fl_hartogs

Fixed some typos.

Change 57546 on 2002/10/16 by scamlin@scamlin_crayola_unix_orl

first cut at STAR test bus. Have not tried to compile it!!!

Change 57395 on 2002/10/16 by hartogs@hartogs_crayola_unix_orl

Fixed some latch inferences that resulted from localizing the temp variables.

Change 57237 on 2002/10/15 by hartogs@fl_hartogs2

Fixed error caused by localizing temp variable declarations.

Change 57236 on 2002/10/15 by hartogs@fl_hartogs2

Enhanced

Change 57235 on 2002/10/15 by hartogs@fl_hartogs

Made all temp variables (blocking assignments) local to their respective always block.

Change 56462 on 2002/10/10 by hartogs@fl_hartogs2

Change corresponding to 2D compound index change in the emulator.

Change 56286 on 2002/10/10 by hartogs@hartogs_crayola_unix_orl

Corrected accidental use of un-registered reset inputs.

Change 56206 on 2002/10/09 by hartogs@fl_hartogs

Added missing signal in sensitivity list.

Change 56196 on 2002/10/09 by hartogs@fl_hartogs

Yet another correction.

Change 56193 on 2002/10/09 by hartogs@fl_hartogs

Fixed typo.

Change 56190 on 2002/10/09 by hartogs@fl_hartogs

Recoded to control timing problem.

Change 56113 on 2002/10/09 by hartogs@fl_hartogs2

"Fixed" RBBM_regclk_active timing.

Change 56112 on 2002/10/09 by hartogs@fl_hartogs2

Updated.

Change 56006 on 2002/10/09 by hartogs@hartogs_crayola_unix_orl

Deleted sclk_mem port on instance of vgt_dma.

Added block_busy_extender to vgt.v.

Change 55944 on 2002/10/08 by hartogs@fl_hartogs

Deleted infer_mux synthesis directives that were ignored by the synthesizer anyway.

Change 55943 on 2002/10/08 by hartogs@fl_hartogs

Deleted infer_mux synthesis directive because they wer ignored anyway.

Change 55928 on 2002/10/08 by hartogs@fl_hartogs

"FInalized" clock gating.

Change 55319 on 2002/10/04 by hartogs@fl_hartogs2

Added DI_PT_2D_TRI_STRIP prim type to major mode 0 for John Carey.

Change 55214 on 2002/10/03 by hartogs@hartogs_crayola_unix_orl

Fixed clock name on memory port.

Change 55167 on 2002/10/03 by hartogs@hartogs_crayola_unix_orl

Changed instance names of clock gaters for synthesis scripts.

Change 55115 on 2002/10/03 by hartogs@hartogs_crayola_unix_orl

Removed paramters from fifo containing Virage memories.

Change 54902 on 2002/10/02 by hartogs@fl_hartogs2

Implemented clock gating using the SC as a template. For most blocks this means that the sclk_global input signal changed to sclk_vgt.

Change 54844 on 2002/10/02 by bbuchner@fl_bbuchner_r400_win

modified sensitivity lists to include null_prim