UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

Before The Honorable MaryJoan McNamara
Administrative Law Judge
INVESTIGATION NO. 337-TA-1044

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IN THE MATTER OF :
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CERTAIN GRAPHICS SYSTEMS, COMPONENTS :
THEREOF, AND CONSUMER PRODUCTS :
CONTAINING THE SAME, :

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AUDIO-VISUAL DEPOSITION OF LAURENT LEFEBVRE, a witness called on behalf of the Respondents, LG Electronics, Inc., LG Electronics U.S.A., Inc. and LG Electronics MobileComm U.S.A., Inc. pursuant to 19 C.F.R. 210.27 and 210.28 and Rule 3.4.1 (Order No. 2), before Lisa McDonald Valdario, (CSR #130093), a Registered Professional Reporter, Certified Realtime Reporter, and Notary Public in and for the Commonwealth of Massachusetts, at the Offices of Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., One Financial Center, 38th Floor, Boston, Massachusetts 02111, on Wednesday, June 28, 2017, commencing at 9:00 a.m.

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P R O C E E D I N G S

VIDEO OPERATOR: Good morning. We are now recording and on the record. My name is Marissa Demonte representing Veritext Mid Atlantic Region. The date today is June 28, 2017. The time is 9:00 a.m. This deposition is being held in the Office of Mintz, Levin located at One Financial Center, Boston, Massachusetts.

This deposition is being taken In the Matter of: Certain Graphics Systems Components Thereof, and Consumer Products Containing the Same, filed with the United States Trade Commission.

The name of the witness is Laurent Lefebvre. At this time, the attorneys will identify themselves and the parties they represent, after which our court reporter, Lisa Valdario, will swear in the witness and we can proceed.

MR. ELENGOLD: Scott Elengold with Fish & Richardson on behalf of the LG Respondents.

MR. LOWERY: Justin Lowery with McGuire Woods on behalf of the MediaTek and Sigma Respondents.

MR. RENAUD: Michael Renaud on behalf of the Complainants, Advanced Micro Devices Inc. and ATI Technologies along with Adam Rizk, both of Mintz,

Levin.

LAURENT LEFEBVRE

A witness called for examination, having been duly sworn, testified as follows:

DIRECT EXAMINATION

BY MR. ELENGOLD:

Q Good morning, Mr. Lefebvre.

A Good morning.

Q Could you please state your full name for the record.

A Laurent Lefebvre.

Q And I'll try my best to get that name correct today as we go, sir. What is your current home address?

A My current home address is

Q Mr. Lefebvre, what is your current employment?

A I am currently employed by ATI, a subsidiary of AMD, as a hardware fellow.

Q What is a hardware fellow?

A It is a title we give to engineers at AMD.

Q What is your current responsibilities in your employment?

A Currently, my responsibilities are to configure and plan the future products of AMD, and also

scope the performance area and power that said products would use.

Q What types of products do you work with?

A I work on GPUs, which are graphics processers, APUs, which are integrated graphics processers on SOCs, as well as scope -- SCBUs, semi-custom business unit products to be embedded in various customer products.

MR. RENAUD: I'm going to designate the transcript as highly confidential under the protective order and I would just say to Laurent, just go a little bit slower.

Q Have you ever been deposed before, Mr. Lefebvre?

A Yes, I have been deposed twice.

Q Do you remember approximately when each of those depositions were taken?

A I remember the most recent deposition was taken in December of last year, and the one before occurred some time before that, but I don't exactly recall when.

Q What was the subject matter of your December 2016 deposition?

A If memory serves, it was about the unified shader patent and some specifications on the R400 products, as well as my previous deposition.

Q What was the subject matter of your previous deposition?

MR. RENAUD: Objection.

A So my memory is more fuzzy on that one, but it was also on some form of unified shader patent. I think it did include another patent which was more directed to the sequencer itself, and my testimony was also part of that deposition, and again, various specifications of the R400 product.

Q Have you ever testified at a trial before?

A No, I have not.

Q And are you represented by counsel here today, Mr. Lefebvre?

MR. ELENGOLD: Objection.

A I am represented by counsel today, yes.

Q So I know you've been deposed twice now, but I just wanted to go over a couple ground rules with you if that's okay. Do you understand that you've sworn to provide truthful and complete responses to my questions today as if you were in a court of law?

A Yes, I understand.

Q Are you aware of any reasons why you cannot give truthful and complete testimony today?

A No, I'm not aware of any reason.

Q As we're going through the day, please ask for any clarification you have with regard to my question, and if you answer it, I'll assume you understand it. Is that okay?
A That is okay.
Q And if at any time you need to take a break, don't hesitate to ask. If there is a question pending, I'll ask that you try to answer the question to the best of your ability, but if you need a break at any time, please just let me know.
A I will.
Q And finally, please try your best to answer my questions audibly as we go through the day just so the court reporter can get a clean record to your responses to my questions.
A I understand.
Q Earlier, when we were talking about the products that you're currently working with, you mentioned I believe GPUs, APUs and SOC, is that correct?
A That's what I remember my answer was, yes, but we can go through the transcript if you want.
Q I'm just trying to bring you back to there so I can ask a follow-up question if that's okay.
A That is okay.
Q And really what I would like to ask you is what is

the difference between each of those three types of products?

MR. RENAUD: Objection.

A Can we restate the three types of products so I get my answer as clear as possible?

Q Why don't we take them one at a time. What is GPU?

A Okay. So the GPU acronym stands for graphics processing unit. This is typically a distinct device that you put into a computer that is responsible for performing graphics on the computer, that is generating images that you see on your computer.

Q What is an APU?

A APU is an internal acronym at AMD we use that stands for accelerated processing unit. It's similar to a GPU, but the main difference is that all of the components of the computer are integrated on a single chip; that is, the CPU and the GPU are integrated on a single chip, which is why we call it an APU versus a GPU.

Q So GPU is dedicated to graphics processing, is that right?

MR. RENAUD: Objection.

A A GPU is a piece of hardware that performs

graphics that does not contain a CPU.

Q What is an SOC?

A An SOC is the fabric, if you will, that allows us to integrate multiple IPs on a single chip. The acronym stands for system on chip, so it's the fabric that allows to connect and integrate everything on a single piece of silicon.

Q Does an SOC contain a GPU?

A SOC stands for system on a chip. It can contain whatever you want it to contain.

Q Can an APU contain a GPU?

MR. RENAUD: Objection.

A An APU and a GPU are different products, so an APU can contain graphics processing, a graphics core, but it doesn't have to have all the capabilities of a discrete GPU.

Q Are they different chips, an APU and a GPU?

A Can you define what you mean by chip? Do you mean different pieces of silicon?

Q Yes.

A So yes, they would be specific different pieces of silicon.

Q And an SOC would be a different piece of silicon or a different chip too?

A An SOC is really the process by which we generate

an APU, so it can be used by an APU, but it can also be another piece of silicon if you want it to be.

Q And approximately how much of your current time is spent working on graphics?

A Can you define what you mean by graphics? It's a pretty generic term.

Q Sure. Why don't we come back to that, and first let me ask you a couple questions about today.

So when did you find out you were going to be deposed today?

A So again, I'm speaking from memory here so excuse if my dates are not exact. I remember late 2016 or early 2017 receiving a call from Adam.

MR. RENAUD: And you can -- instruct you not to provide any content of the call.

THE WITNESS: Sure.

A And that made me aware of this pending litigation, and then I met with counsel several times since that date.

Q Do you have an understanding of what this case is about?

MR. RENAUD: Objection. You may answer so long as you don't reveal any attorney/client communications.

A I understand it's some kind of litigation between third parties and AMD.
Q Do you understand what kind of litigation?
MR. RENAUD: Same instruction. You may answer so long as you do not reveal any attorney/client communications.
A So I am not an attorney so I don't exactly know what the complaints or litigation is all about. I know that the R400 is part of that.
Q Approximately when was your first discussion with counsel about this investigation?
A I think I already answered that question previously. You can go back to the log, I said I believe around January -- late 2016 to early 2017.
Q Do you remember any, with any more detail approximately when it occurred?
MR. RENAUD: Objection.
A No, I do not. I'm sorry.
Q When was the first time that you met with counsel regarding this investigation?
A By meeting, you mean in person, or what do you mean by meeting?
Q Earlier you said you met with counsel several times. Do you recall that?
A Okay. So I'm assuming you meant, you mean met in

person.
Q Do you recall saying you met with counsel several times earlier?
A I do, yes.
Q What did you mean by that?
A So I meant taking calls and also meeting in person. So which one of the two?
Q So after your first call with, I believe you said it was Mr. Rizk, when was your next communication with counsel regarding this investigation?
A Again, I'm speaking from memory. It is fairly fuzzy, but I recall another instance of a call and then a meeting in person in Montreal.
Q Do you recall who you spoke with on your second call?
A From memory, I believe Mr. Rizk was present on the call. I don't recall who else was on these calls.
Q Do you recall if there were other people on the call?
A There were at least another person from AMD but I don't remember more.
Q Do you remember who that other person was from AMD?
A Yeah, that person was Pam Horn.
Q Who is Pam Horn?

A My understanding is she works for the legal team for AMD.
Q Do you know if Pam Horn is an attorney?
A I do not know, no.
Q Without getting into specifics, what generally was the subject matter of your call?
MR. RENAUD: Instruction not to answer.
A I'm going to follow my counsel and not answer that question.
Q Approximately, when was your first meeting with counsel in Montreal?
A It was some time in spring because it wasn't cold anymore, but I don't remember the specific dates.
Q Do you recall who you met with?
A I met with Mr. Rizk and one of his colleagues that I don't remember the name.
Q Anyone else?
A No, not in that meeting.
Q Where did you meet?
A We met at the Hilton Hotel in Laval, which is north of Montreal.
Q Approximately how long did you meet for?
A If I remember correctly, that was about, I would say three-quarters of a day.
Q Did you talk to anyone at AMD that day?

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A You mean if I talked to anyone at AMD that day of the meeting or --
Q Yes.
A And by -- you know, let me rephrase correctly to make sure I understand your question. Did I talk to anyone at AMD that I was going to a meeting, or about the content of the meeting, or talk to anyone at AMD during that day?
Q Let's take all of those. So first, did you talk to anyone at AMD about the content of the meeting?
A Not that I remember, no.
Q Did you talk to anyone from AMD at the meeting?
A I was the sole person of AMD present at the meeting.
Q Did you call anyone at AMD during the meeting?
A During the meeting itself, no, I did not talk to anyone at AMD.
Q When was your next conversation with counsel regarding this investigation?
A My next -- again, if I recall correctly, my next verbal conversation with counsel was here in Boston.
Q When was that?
A That was, started Monday morning up until today.
MR. ELENGOLD: I ask the court reporter to

please mark Exhibit 1.

(Document marked Exhibit 1 for identification.)

Q Mr. Lefebvre, have you seen Exhibit 1 before?

A I believe I've seen this piece of paper or collection of piece of paper in a bigger document before, yes.

Q Do you know what Exhibit 1 is?

A It reads: Respondents' Notice of Deposition of Laurent Lefebvre, so.

Q Do you understand that you are noticed to be deposed today in your personal capacity?

MR. RENAUD: Objection.

A Yes, I do understand that.

MR. ELENGOLD: And I'm going to ask the court reporter to please mark Exhibit 2.

(Document marked Exhibit 2 for identification.)

Q Mr. Lefebvre, have you seen Exhibit 2 before?

A I have seen a document that looks very much like this. It was not exactly in the same form, but it contains the same number of items than this document.

Q Do you know what Exhibit 2 is?

A Again, it reads: Respondents' First Notice of

Deposition to Complainants Advanced Micro Devices Inc. and ATI Technologies, ULC.

Q Do you understand that you have been designated by complainants AMD and ATI to testify today on their behalf for certain topics?

A Yes, I understand that.

Q And Mr. Lefebvre, if you'll refer in that document in front you in Exhibit 2, my understanding is that you have been identified for topics one, seven, eight, nine, 17, 18, 33, and 86; with respect to two of the patents in this litigation, and those two patents both have you listed as a named inventor. We generally refer to them as the Morein patents because he is the first listed inventor.

Do you understand the two patents I'm referring to if I say the Morein patents at issue in this investigation?

A For the sake of precision, I would like you to refer to them by number so I can tell which patent exactly you're talking about, but I generally am aware of the field, yes.

Q Okay. And do you understand that you've been designated for those topics for the two patents for which you're a named inventor to testify today

on behalf of AMD and ATI?

MR. RENAUD: Objection, and you may answer, but I'm just going to insert in the record that all of those subjects are subject to objections that have been made in writing, but sorry, please answer the question.

A Yes. I can testify to the facts related to those patents with the understanding I'm not an attorney so I can't really go, you know, beyond my knowledge.

Q You're prepared to testify today though on those topics we just identified.

A Yes.

MR. RENAUD: Same objection. He's prepared subject to the objections.

Q What did you do to prepare for today's deposition?

A Okay.

MR. RENAUD: And you may answer that question without revealing any attorney/client communications.

THE WITNESS: Yes.

A So I met with counsel in person, like I said before, once in Montreal and then here in Boston extensively for two days prior to this deposition, and I reviewed a wealth of specifications, as well

as my prior depositions, my prior testimonies. I browsed through the patents, I had discussion with AMD representatives, and reviewed some presentations and the various elements that were Exhibits in my previous depositions.

Q Let's try and take those one at a time.

What documents did you review during your meeting in Montreal?

A In Montreal, I don't recall reviewing any particular documents. We had more discussions about the subject that I was about to be deposed on, but I don't recall reviewing particular documents per se.

Q What documents did you review during your preparation here in Boston?

A I'm going to give you the best list I can tell with the understanding it's probably not going to be exhaustive because there was a wealth of documents, and so like I said before, we could go back to the log, but they involve my depositions, my testimonies and various Exhibits, and presentations that were held on the AMD Perforce server, P E R F O R C E.

Q Starting with the specifications, what specifications did you review?

A Again, speaking from memory here, I recall reviewing at least the sequencer specification of the R400 chip versions 0.4 and version 2.0. And I believe for that particular deposition, the specification that I reviewed, that was it.

Q Those were the only two specifications you've reviewed in preparation for your deposition today, is that correct?

A These are the depositions I recall being reviewed. So I know for sure I reviewed those. I may have reviewed other documents. There was a big binder. At least those.

Q You said you reviewed your depositions. Is that referring to the two depositions we discussed earlier?

MR. RENAUD: Objection.

A Yes, that is referring to the two depositions that I did before, yes.

Q And you reviewed both transcripts this week?

MR. RENAUD: Objection.

A I read both transcripts, yes.

Q You said you reviewed testimony. What testimony did you review to prepare for today's deposition?

A So as best I recall again, and if you have the documents we can look at them, there were

testimonies that were made on how the R400 implemented the unified, the various unified shader patent, and those are at least the testimonies that I've been reviewing that were part of the big binder of documents.

Q What is a unified shader?

MR. RENAUD: Objection.

A Can you be more precise about what you mean? Are you talking about the unified shader in the R400 project?

Q You just mentioned how the R400 implemented the unified shader patent, right? Do you recall that?

MR. RENAUD: Objection.

A Can you give me back my answer exactly?

Q Why don't I just ask again.

A Okay.

Q Did the R400 implement the unified shader patents that you referred to?

MR. RENAUD: Objection.

A So again, I'm not an attorney so I can't talk how the patent and everything interlocks, but the R400 product had a unified shader, yes.

Q What was the unified shader in the R400?

A So the particular unified shader that the R400 implemented was a shader that was able to operate

on pixels and vertices using the same piece of hardware.

Q Is there a name for that piece of hardware?

A We call it the unified shader, but you know, with the understanding this is just one definition of the term in that particular product.

Q Did you work on the unified shader in the R400?

A In the R400, I was the main architect for the sequencer, which is effectively the block that allows -- one of the block that allows the unified shader to operate. It is the block that sequences the instructions and makes various decisions about how the work is split between pixels and vertices, and so in that respect, and many discussions I had with the lead architects, Steve Morein and Andy Gruber, yes, I worked on the unified shader.

Q Is the sequencer a part of the unified shader?

A I did not get that question. Can you restate, please?

Q Sure. Is the sequencer a part of the unified shader?

A The sequencer is a block of the R400 that is inside the unified shader that allows the shaders or the programs to operate, and makes decision about the workload balance between pixels and

vertices.

Q You mentioned reviewing some Exhibits this week. Were you referring to the Deposition Exhibits from your prior depositions?

MR. RENAUD: Objection.

A Yes, I meant -- I was referring to some of the Exhibits of my previous depositions.

Q What presentations did you review to prepare for your deposition?

A While I don't recall the specifics, some of the presentations I reviewed were part of the Exhibits of my previous depositions, and I also reviewed other presentations to refresh my memory and prepare me to testify on behalf of AMD on certain topics.

Q Do you recall any details regarding any presentations you reviewed to prepare for today?

MR. RENAUD: Objection.

A So I mean, I recall two specific presentations that were new, at least not part of the Exhibits before, that related about what Netlist 3 was in terms of the R400 product and how that particular netlist was ported on a hardware simulator named IKOS.

Q Do you recall the author of that presentation?

A No, I do not.
Q Were you already personally familiar with that presentation before your review?
A I must admit, I did not remember it. It was a long time ago. I might have been familiar with it way back when, but when it was re-presented to me, it was new. It did not ring any bells, put it that way.
Q Do you recall the date of that presentation?
A As I stated before, there were two presentations I believe, and they were, one of them was in January and the other one, February. I don't recall the particular year unfortunately, but I'm sure if you can -- these were produced, so if you can find them, I can review them with you and can give you more definition as to the date.
Q How do you know they were produced?
A Because counsel told me that they were produced.

MR. RENAUD: While that answer is fine, I remind you, Laurent, any conversations with counsel are off limits. Saying what was produced, if you know it, I'll allow, but just be careful. Okay.

THE WITNESS: Yes, sir.

Q Did both presentations relate to the netlist for

the R400?

A Again, you have the documents so we can review them and I can give you more details. I'm talking from memory. I recall one presentation was about telling what Netlist 3 was, and the other presentation was saying how that list was used or when it was ported to IKOS.

Q Any other presentation you recall reviewing?

A Again, do you mean new presentations or presentations that were part of the previous Exhibits?

Q Both. Any presentations that you recall reviewing in preparation for your deposition today.

A So there was a presentation in, at least in my previous testimony about the one tri, triangle, that was part of the Exhibits that I recall, and there was some slides about the AMD's roles and responsibilities of various people in the R400 project.

Again, I'm talking from memory. You can bring up the slides and we can look at them. This is a non-exhaustive list of the presentations that I recall.

Q Any new presentations other than those two netlist presentations that you recall reviewing in

preparation for your deposition today?

A There were a wealth of PDF documents -- not PDF, power points presentations on the table that I looked at, but I don't recall the specifics on them unfortunately. So I know there were more, but --

Q Did you review the patents in preparation for your deposition today?

MR. RENAUD: Objection.

A Yeah, we can go back to the record again. I think I stated that before, yes, I did browse through two patents in preparation for this deposition.

Q Do you recall any details about those two patents you reviewed?

A They were both unified shader patents on which I was listed as an inventor, and they had numbers on them distincting them but, you know, if you bring them up, I'm sure I can tell you which ones and confirm that they were the patents I reviewed.

Q Did you review any other documents that we haven't discussed in preparation for your deposition today?

A Like I said, there were a wealth of documents that I reviewed. I recall one of them was the IKOS User Manual. I recall it because it was very

thick. And there might be more. Like I said, it was a lot of documents that were browsed through.

Q Did you speak with any AMD or ATI people to prepare for your deposition today?

A I recall having phone calls with a few people from AMD. Yes.

Q Who did you speak with from AMD?

A I remember David Christie and a few other people that I don't remember the names of. They are not the -- I mean, I understand that they were gathering information on behalf of AMD, and documents, but I don't recall the specific names. They are not people I work with very often.

Q The only person you remember speaking with in preparation for your deposition today at AMD is David Christie, is that correct?

MR. RENAUD: Objection.

A Yes, and but Pam Horn was also on the call. I mean she always is typically.

Q Who is David Christie?

A My understanding is that he is a hardware engineer that works for AMD legal teams to help accumulate documents and reviews them for litigation purposes and whatnot. I don't exactly know what he is doing in that role though.

Q Why did you talk with David Christie to prepare for your deposition today?

MR. RENAUD: Instruct you not to answer that question if it can't be answered without revealing attorney/client communications.

A Yeah, I don't think I can answer that question directly.

Q Is Mr. Christie an attorney?

A He is, I believe he is an engineer. Not an attorney.

Q Did you speak with him on the instruction of counsel?

MR. RENAUD: Instruct you not to answer that question.

A I can't answer that question.

MR. ELENGOLD: Why do you believe that his discussion with Mr. Christie is privileged?

MR. RENAUD: Because it is. Attorney/client communication. I was on the phone with him. I'm not going to pry into that. If you want to take a break and talk about it, we can.

MR. ELENGOLD: Okay.

MR. RENAUD: I'm also happy to ask the witness to go back and find out who the other AMD people are that he spoke with so you can get them

by name, but my memory is there are some non-attorneys that were part of the conversations.

MR. ELENGOLD: I think for now, in interest -- as you wanted to get through the day quickly, it's fine if you want to take break and do more sort of work on prep, but I think it might be faster for us to go forward with the deposition. But that's up to you.

MR. RENAUD: That's fine. Let's go forward.

Q Who else was on the call with Mr. Christie?

A Again speaking from memory, I believe for that particular call, it was just Mr. Christie and Pam Horn.

Q How many times did you speak with Mr. Christie to prepare for your deposition today?

A I recall only that one phone call. There might have been emails between that I don't remember.

Q Is there anyone else that you recall speaking with to prepare for your deposition today?

A Well, if by "else" you mean other than the ones that I named you, yes. I mean, there were, like I said, other parties on the phone call. I don't remember them by name but they were there.

Q Was there always an attorney on the line whenever you spoke with people, or Miss Horn?

A Either on the line or in the room, yes, because I had these conversations from my counsel's office, so --
Q In the last two days?
A In the last two days, yes.
Q Was your conversation with Mr. Christie in the last two days?
A Yes, it was.
Q Other than the documents reviewed, you reviewed, and your call with David Christie, is there anything else you did to prepare for your deposition today?
MR. RENAUD: Objection.
A I personally searched the Perforce database for evidence of what Netlist 3 was, and you know, like I said before, read documents, and I had another call with other parties of AMD, like I already stated, but that's the extent of what I remember.
Q Was that a single other call with other people at AMD that you're referring to?
A Yes. That's what I remember, single other call.
Q When did you search the Perforce database?
A I did it in the last two days.
Q Why did you search the Perforce database to prepare for your deposition?

MR. RENAUD: Objection. You may answer that to the extent you do not reveal any attorney/client communication.

A Yeah, we can go back to the log again. I think I answered that question already. It was to find evidence of what Netlist 3 was, if I recall correctly.

Q What is Netlist 3?

A So a netlist is a list of synthesis files, which are the output of synthesis, so they're basically a list of gate level files that implement a hardware device.

Q What do you mean by "implement a hardware device"?

A I mean, it's the source file that is used to generate silicon. So either the input of an FPGA simulator or the input to the PD team to generate a chip, a silicon device.

Q So did you say FPGA simulator?

A FPGA.

Q What is an FPGA simulator?

A So FPGA is an acronym, and I know it's present in the IKOS User Manual, so we can go look there to remind myself what the letters actually mean, but it is a system of programmable gates that you can program by pushing a netlist to it, to implement

any hardware device that would fit on the number of gates that the hardware simulator supports.

Q Is that the same as a tapeout?

A A tapeout is a separate process that enables the creation of a silicon piece. So they're similar but different at the same time.

Q How are they different?

A So a tapeout is really a manufacturing step where we send the design to silicon manufacturers, versus a netlist, which is the information in a tapeout would be what we use to initiate or program, if you will, an FPGA simulator.

Q And an FPGA simulator allows you to simulate how the hardware would function?

A Yes. So basically, an FPGA simulator is a way to build a prototype of a given hardware device.

Q Does it simulate a prototype or does it actually build a chip?

MR. RENAUD: Objection.

A So an FPGA device is a programmable hardware device. So in that sense, once a netlist or design is pushed onto that, it becomes that device. It has limitation as to how fast it can operate, but effectively, it is the device.

Q So when you say an FPGA simulator, just so I'm

clear, is that a computer program or is that a hardware device?

A So an FPGA simulator is a hardware device. It's a big programmable hardware device which you can use to simulate another product that, you know, would become a chip in the end. It's a way to a means to get a prototype early of the device that you want to build.

Q What is the PD team?

A PD stands for physical device, so it's the team that takes a netlist, or takes the output of synthesis, and place and routes them in order to make a floor plan of a chip that is going to be built.

Q Is there a name for that floor plan once the PD team has completed its work?

A Well, I believe a floor plan is a floor plan. I mean, once everything is complete and done, I believe the technical term is, we have a GDS database, and that's what is used to do a tapeout.

Q So when the PD team is done, that's -- the result of their work is what would go to a tapeout, is that correct?

A Yes. The result of the work of the PD team would result in a tapeout, yes.

Q And the PD team gets a netlist to start their work?
A The PD team gets a netlist to start their work, yes.
Q And at the same time, that netlist is also used with an FPGA simulator, is that right?
A Yes. So that same netlist that can be used by the PD team can also be compiled or sent to an FPGA simulator to establish a prototype of the chip.
Q And is that for testing that you would do that at the same time you're doing the tapeout?
A Yes. Well, it is for testing, and it also is used, as best I can tell -- and remember, it was a long time ago, so forgive me for inaccuracies here -- to bring up the software stack, the driver, because it's a much more convenient machine to use to run more extensive complete applications than what you can run on an RTL simulator.
Q Other than the conversations we've discussed and the documents we've discussed, is there anything else that you did to prepare for your deposition today?
A Not that I recall.
Q Do you know what patent prosecution history is?
A I am vaguely familiar with the term but I don't

know the details of it. Again, I'm not a lawyer, so I mean it's not something I looked at very much, no.

MR. RENAUD: I'll object as being outside the scope, and I'm not sure, Mr. Elengold, how you want to handle the personal versus the Rule 30(b)(6). We can live with having them kind of be back and forth and not having a rigid line, but I'll just state for the record that any questions directed to file histories I believe are outside the scope of the subject matters that he's being asked to testify on, but so please proceed.

Q Sure I was just laying a foundation for a question, which is, did you review any prosecution histories in preparation for your deposition today?

A Not that I recall.

Q About how much time did you spend total on your preparation for your deposition?

A I believe this question was already answered. Like I said before, three-quarters of a day, personal meeting in Montreal, some phone conversations, and then full two days here in Boston. That's what I remember.

Q By full days, do you mean nine to five?

A For the first one, probably nine to six. The second one, somewhere more around nine to seven or eight. So pretty long days.

Q Were there any employees or documents that you planned on reviewing but didn't before coming to be deposed today?

MR. RENAUD: You may answer that yes or no.

A No.

Q Do you feel you're the most qualified person at AMD to testify on their behalf for the corporate topics you're discussing today?

MR. RENAUD: Objection.

A I believe I qualified and I prepared adequately to testify today, yes.

Q Are you being paid for your testimony today?

MR. RENAUD: Objection.

A I am paid my normal salary by AMD.

Q Do you get any additional compensation for testifying?

MR. RENAUD: Objection.

A No, I did not.

Q Does AMD have any policies regarding employee participation in litigation?

MR. RENAUD: Objection. You may answer that yes or no.

A I don't know.
Q For this investigation, did you personally search for any documents in your files?
MR. RENAUD: Objection.
A So my understanding is that a team of people at AMD did that investigation. That investigation included my files, and like I stated before, I did a Perforce search of documents yesterday and the day before.
Q Prior to those two searches in the last two days, did you personally do any work collecting documents for this investigation?
MR. RENAUD: Objection.
A No. I did not, but like I said, I had the understanding a team at AMD did that work, and that work included my documents.
Q Did you discuss your deposition today with anyone other than counsel?
MR. RENAUD: Objection.
A I did not discuss the contents of my deposition but, you know, at least my manager, Mike Mentor is aware that I'm doing depositions today because I had to get away from work for these days, so.
Q And where is your work currently located?
A I officially report to the Markham office of ATI,

and I mostly work from my home in Montreal, or I'm actually in Mascouche to be exact, and my manager is Mike Mentor from the Orlando office, so.

Q All over.

A Pretty much.

Q What is the relationship between ATI and AMD?

A My understanding, and again, talking from memory and I don't have all the specifics, is that AMD acquired ATI some time ago.

Q But you're an ATI employee, is that correct?

A So I was not. At the time of the AMD acquired ATI, I was actually a contractor working for ATI but working in my own name effectively. So I was working for but not as an employee.

Q What about right now?

A So right now, I am again speaking from memory and this is a lot of -- I understand that I'm an employee of AMD but through what they call ATI Technologies ULC, which is the Toronto office.

Q Do you have a formal employment agreement, like a written agreement?

A A formal -- I don't know what you mean by that.

Q Do you have a written employment agreement?

A A written employment agreement. I'm just -- I don't know. I'm just a normal employee, so full

time. Is that what you mean by this question?

Q I don't know. I don't know if you have a written employment agreement or not. I'm just trying to -- you said you -- I understand you're an employee of AMD but through ATI, and I'm trying to understand what that means. Who actually is your employer?

A Okay. So because I'm Canadian, to simplify tax matters and everything, I'm paid through the Toronto office, and so my paychecks and my actual employer is the Markham office, which I understand is ATI ULC because that's what it says on my paychecks and tax records and what not. That's pretty much the extent of what I know about this. I don't know what relationship is, but as far as I know, I work for AMD but it goes through this.

MR. RENAUD: And all of the answers regarding corporate structure or purported corporate structure are obviously outside the scope of the designation, although you're free pursue them.

MR. ELENGOLD: Yeah, that's fine.

Q Your personal employment is not something you need to be designated for right now. I was just trying to understand who your employer is.

MR. RENAUD: Yeah, and that corporate structure relationships, I think there is a witness coming up on that because I understand that might be an area of inquiry.

Q Yeah, I don't know if that's true or not, but again, this is just limited to your employment right now.

MR. RENAUD: Thank you.

Q Can you please describe for me your education since high school.

MR. RENAUD: Objection.

Q Where did you go to college?

A I went to the Ecole Polytechnique de Montreal where I got an electronic engineering degree, and I followed that immediately with a master's in computer graphics from the University of Montreal.

Q When did you get your initial engineering degree?

A If memory serves, that would have been June 1998.

Q When did you get your master's in computer graphics?

A That would have been somewhere in the summer of 2000. Can't be exact on the date because it involves, you know, giving the thesis and having it reviewed and whatnot.

Q What was the subject matter of your thesis?

A If I remember correctly, it was about the analysis of and synthesis of textures through photograph trying to get a procedural model for those.

Q Do you have any other degrees?

MR. RENAUD: Objection.

A I have a high school degree and primary school diploma, but to my knowledge, that's it.

Q That's it.

Did you attend any other schools after receiving your master's degree?

A No, I did not. I went to conferences and such but not schools, that I remember.

Q Where did you first work after obtaining your master's degree?

MR. RENAUD: Objection.

A I started working for ATI Technologies, the Boston office. Or actually, to be more accurate, the Marlborough office at the time.

Q What was your initial title at ATI?

MR. RENAUD: Objection.

A If I recall correctly, it was something like engineering level one.

Q What were your initial job responsibilities?

A So again, thinking, talking from memory, 17 years ago, it was, the very first thing I did was to

work on something loosely related to my master's, was to try to do pearl and noise on hardware, then I moved to the scan converter of the R400. All of these topics were related to the R400 project by the way. And then I started working on the actual sequencer of the R400.

Q When did you join ATI?

MR. RENAUD: Objection.

A If memory serves, it would have been around September of 2000. So right after my master's or thereabouts.

Q And you said you initially started working on the R400, is that correct?

A That is correct, yes.

Q What is the R400?

A The R400 is a GPU that ATI was working on at the time, their newest GPU.

Q When did you start working on the scan converter for the R400?

A That would have been maybe a few months after I started with ATI. I'm somewhat fuzzy on the transition between the pieces of work, but it was fairly soon after I started working at ATI.

Q Approximately how many people were working on the R400 at that time?

MR. RENAUD: Objection.

A You mean as I started working for ATI, right at the beginning of my employment?

Q Sure. Yeah.

A As I recall, again it's a long time ago, that was a fairly small team then. You know, maybe a few architects and myself. So something like 10, 15 people at the beginning.

Q Is there a difference between an architect and an engineer at ATI?

A An engineer is a job title or job rank, if you will. An architect means what you are doing. So it specifies what the engineer is doing. It has no real relationship with your rank within the company.

Q What does an architect do?

A So my best understanding is that, and again at the time, for the R400, an architect was responsible to develop the specifications for the block that he owned or the system that he owned, as well as developing a model, which we call the C sim or emulator, that would serve as a reference to the designers.

Q What is a block?

A A graphics chip is composed of subsystems or

sub-functionalities, and we call those blocks.
Q What blocks make up a graphics chip generally?
A So I'm going to answer here in the scope of the R400 to, you know, constrain the problem. So for example, in the R400, and we could go to the spec if you really want me to give you the exhaustive list of blocks, I'm talking from memory, I remember there has to be a CP, which is a command processor first block; then some kind of vertex block, which you a call the VGT; the PA, which is a primitive assembly; the scan converter, which is the SC, then the shader, which in the R400 case was a unified pixel and vertex shader. And then you have some texture blocks or texture cache, some form of memory controller and memory connection, and render back ends, which are, you know, the color and the depth blocks.
Q And each block is implemented in separate hardware, is that correct?
A What do you mean by "separate hardware"?
Q What is the distinction between the different blocks?
A The blocks allow parallelism in the development of a GPU. They define boundaries, and so they define like a functional entity, if you will, of the chip

and they're surrounded by interfaces with strict protocols that define the need to communicate with the other blocks. And the sum of all blocks make up the GPU, or whatever you want to call, you know, whatever chip or device you're trying build.

Q Will those functional boundaries be physical boundaries on the final chip?

MR. RENAUD: Objection.

A I don't understand what you mean by physical boundaries.

Q You said there is input and outputs for each of the blocks, correct?

A Yes, there are interfaces for the blocks, which could -- or wires, but that is just, you know. A block is a logical structure. It's not, each block is not going to be a different chip, if this what you're asking.

Q No, what I'm asking is whether it will be a different section of the chip.

A Different section of the chip. So again, a block is a logical entity. Once you put it in silicon, it can be intermingled with other blocks as the PD team sees fit. It doesn't mean that if you have a block, a logical block on RTL that you use for development, that it's going to be its own little

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bubble in the silicon. It can be intermixed, depending on the various constraints that you have when you're placing and routing the chip.

Q And that's what the PD team does, is that correct?

A Yes, that is correct.

Q The PD team actually figures out how all of the different logical blocks or functional blocks will interface together on silicon?

A No. The interface connections between the various blocks are defined by the designers and the architects in RTL and in the spec. So that's fixed by the code. How these are placed on the actual silicon device, that's what the PD team does.

Q Is that a hard process?

A It depends on the complexity of each block. Obviously the more cells you have to place, the more complex it can be.

Q What is RTL?

A I'm talking from memory here, and I always get this acronym wrong, I think it stands for registered transfer layer, but that's the source code of the synthesis tool that generates the netlist.

Q You mentioned C sim; is that the code that's used

with C sim?

A What do you mean by "the code that's used with C sim"?

Q You just said the RTL is the source code that's used, right? Earlier? Is that correct?

A Yes. I said that it was the source -- that is the source used by the synthesis tool to generate gates. The C sim, as I refer to it, is the C code which is C plus plus, it's a program, that serves as a reference model to compare this RTL structure against a golden model so to make sure that it performs the right operation.

Q What is a golden model?

A I guess it depends, in the scope, I mean in AMD and in the R400 project, for example, the golden model is, you know, what is used to generate pictures on the screen with the program that is supposed to emulate the chip, and to make sure that outputs the pictures we expect it to output. It's a reference model if you will.

Q It's a simulator or -- I'm sorry, strike that.

It's a simulated model programmed in C, is that correct, or C plus plus?

A Yes. It's a behavioral model of the chip we want to build that serves as a reference.

MR. ELENGOLD: We've been going to about an hour. Would you like to take a break?

MR. RENAUD: You know, in order to make the day work, while I think later we'll need shorter windows, maybe we go another 15 or so, if everyone's comfortable with that?

MR. ELENGOLD: That's fine.

MR. RENAUD: But thank you for asking.

Q What is the process that was used to design and implement the R400 into the netlist, starting from I guess the C model?

A Okay. So let me rephrase the question, make sure I understand correctly. What you are asking is, the way AMD conceived or built the R400 chip from start to finish, in a general sense, is that what you're asking?

Q Yeah, was the R400 ever built?

MR. RENAUD: Objection.

A The R400 was prototyped on the IKOS box, yes.

Q What is IKOS?

A It's the name and/or the company, I don't remember, of the FPGA device.

Q So yes, can you please describe for me the way AMD or ATI conceived of the R400 chip from start to finish.

A Okay.

So the process for the R400 was to start with a system level specification, which describes the various interactions expected between each of the blocks of the chip as described before. And then you have another tier of work that goes into the creation of these block level specification which describes in more detail what each block is supposed to do.

Then typically, you have the creation of the C model, which is the reference model that we described before, and at that time, the development or the RTL starts. We typically do the validation from the block level up, whenever we can, so try to start small and then grow. And at some point later when the RTL is mature enough, we start generating netlists which we give to a PD team so they can start working on the place and route, and at this point, there is a loop between PD and the RTL to close timing and fix issues, and once that loop completes, in the middle of that loop you can have a prototype being done to shortcut the process and have your software team starting working on the device, and the very end of the loop is where the tapeout takes place to

initiate manufacturing of the silicon device.

Q You mentioned doing the validation at the block level. Is that done on the C model or the RTL?

A Okay, some blocks, not all of them, have what we call a block level test bench. And typically, what this does is it's a closed environment around the block that stimulates the block with inputs and gets the output of the block, and then what we do is we use the gold model or the C sim to compare the outputs of the RTL against those we get from the C sim.

Q How do you know that the outputs from the C simulator are correct?

A So you'll know that for sure. The C sim, the way we validate it is to use it to generate the final pictures that we're expecting, and so the assumption there is if you get the final picture correct, then the interfaces in between will also be correct. However, you know, as you run this process, it's possible that you're going to get mismatches between the RTL and the C sim and sometimes, you know, the C sim is wrong and so you just work on it until they agree, and you keep the final image correct.

Q So you mentioned you started your work originally

on -- I'm probably going to get this wrong, but -- I'm sorry, just to make sure I don't mess up the -- I think you said pearl and noise, is that correct?

A Yes, that's what I said.

Q What is pearl and noise?

A Pearl and noise is a specific continuous noise function that is used typically to introduce or simulate natural environments, or like turbulence or such. So if you want to do a cloud, cloud doesn't have a very definite form, and so some kind of noise needs to be introduced to create the randomness.

So pearl and noise is a procedural manner to generate said turbulence so that you can then introduce it into graphic models.

Q Was your work on pearl and noise at a specification level or were you already working in C and/or RTL?

A It's been a long, long time, but I believe I did both, a model of the pearl and noise on C, as well as specifications of what it would have been. So both. Again, kind of an architect role on it too.

Q What about RTL?

MR. RENAUD: Objection.

A At AMD, we tried not to have the same person that defines the architecture and writes the C model also writes the RTL, for the obvious reason that if you have one person doing that, if he does an error on one, he's likely to do the error on the other. So we try to have the architect do the C sim and another person under the direction write the RTL, so that you have more chances of finding errors and issues.

Q You said your next role I believe was with the scan converter, is that correct?

A Yes, that is correct.

Q What is a scan converter?

MR. RENAUD: Objection.

A The scan converter in the R400 is the hardware block that takes triangles or primitives and rosterizes them. So it creates pixels or identifies which pixels on the screen would belong to that primitive, whether it's a triangle or some other primitive. That's what we call scan converting.

Q Were you an architect for the scan converter?

A I worked on the scan converter in both the specification and the C sim. I don't know if I was given, you know, formally the architect title,

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but I think you can assume that it was very close to that, yes.

Q Did you write any RTL for the scan converter?

A No, I did not, for the same reasons stated before.

Q Are you experienced with reading and writing RTL?

A I had RTL classes as part of my formation. I can read RTL. I can debug RTL. I can read waves, but I did not write any RTL, I mean any significant portions of RTL in my career.

Q And not for the R400?

MR. RENAUD: Objection.

A And for the R400, you know, as best as I remember again, I mean, I may have written here bits and pieces and small fixes in RTL, but I did not create modules from scratch, no.

Q At what point did you switch from working on the scan converter to working on a different block?

A So as best I recall, it was around September 2001, and the reason I recall that, it was I supposed to go to Orlando to give the scan converter design to the Orlando team so that I could focus on the sequencer. So I know because of the events that occurred, that the transition occurred somewhere around that date. Not before, let's put it that way.

Q Was the scan converter block completed at that point?
A No, it was not, and that's the reasons why we had to travel to Orlando to give that work to them so they can complete it while I would focus on other blocks.
Q And you mentioned you were going to focus on the sequencer block next, is that correct?
A That is my recollection, yes.
Q Why were you switching to the sequencer?
MR. RENAUD: Objection.
A So when we started doing the R400 project, we thought of reusing some of the concept of the sequencer that was used in the R300, but the unified shader between vertex and pixel shaders of the R400, made the process complex, and so the workload assumed by the sequencer became too big to be handled by, you know, one engineer already assigned to another block. I believe that, if I recall correctly again, that's one of the reasons why this occurred.
Q What is the R300?
A The R300 is another GPU that was done by ATI, so it's the predecessor, if you will, to the R400 which was a good part mostly done by the time, or

at least in development by the time I switched over to the sequencer work.

Q What do you mean by "in development"?

A Well, as you may or may not know, the graphics processers are not done in one day, so takes an extensive time to build a GPU, and so what I mean by "in development," I mean it was in that development period.

Q The R300 was still in development is what you're saying, is that right?

A At the time I switched to the R400 sequencer, yes, I believe that was the case, but talking from memory. Again, I'm sure we can find public records or what not to put the dates on the calendar, but that is my recollection.

Q Did the R300 ever get commercialized?

MR. RENAUD: Objection.

A Yes, I believe it did.

Q What was the name of the commercial chip?

A I am very bad with commercial names. I have no idea. I only know the internal names. Even today actually, so. I'm terrible with these. They have these weirdest nomenclatures.

Q What public records would you look at to determine when the R300 was finished with development?

A It's a good question. I think I would rely on the product names and then also try to find internal documents within AMD that ties these product names to the internal project names.

Q But you do believe the R300 was put into a commercial graphics chip, is that correct?

A Yes, that is my recollection.

Q Did the R300 project, just by name I'm guessing, precede the R400 project into development?

MR. RENAUD: Objection.

A Yes, that's my understanding.

Q Do you know approximately when the R300 finished development?

A I don't recall. I mean, it wasn't done by the same team that I was working on. It's a completely different program, different team. I know it was before 400 and after R200, but where exactly, it's just too far away.

Q So you don't know when it went into manufacturing?

MR. RENAUD: Objection.

A I do not recall that information, no.

Q What were the differences between the R300 and the R400?

MR. RENAUD: Objection.

A So I haven't prepped or anything on the R300.

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It's been a long time ago. But my understanding is that that product was more typical in the sense that it had a more normal or natural flow of graphics processing than the R400. It did not have, for example, a unified pixel and a vertex shader.

Q It had separate vertex and pixel shaders?

MR. RENAUD: Objection.

A Again, not having fully prepped for that, and knowing the intimate details of the R400, can only talk from memory, but this is why I remember, yes, it had a different vertex and a different pixel shader.

Q Is that what you mean by a typical product at the time, having separate vertex and pixel shaders?

MR. RENAUD: Objection.

A This is my recollection of what a natural GPU at the time was, yes.

MR. RENAUD: Let me just state for the record that the R300 is outside the scope, and I'd remind Laurent to be careful when he's answering, because I think the prior answer you said you hadn't been prepped on the R400. I think you meant the R300.

THE WITNESS: R300, sorry, yes.

MR. RENAUD: So, and I don't want to provide testimony for the witness, but he is prepared exhaustively on the R400.

MR. ELENGOLD: I think you are providing testimony for the witness, so it's fine. Let's have him answer the questions, and if he feels like something is outside of the scope, you're welcome to make a scope objection.

MR. RENAUD: My problem is, if you're going to move between the 300 and the 400 --

MR. ELENGOLD: I'm not moving. I asked him what the differences were.

MR. RENAUD: Hang on. Let me just state my piece. You're going to ask whatever you want obviously. I just want to make sure the record is clean; the 300 is outside the scope, the 400 is inside scope. And just go slow so you can pay attention to what he's asking and what the answers are, okay?

MR. ELENGOLD: Why don't we take a break.

MR. RENAUD: That's fine by me.

VIDEO OPERATOR: The time is 10:30 a.m. This concludes tape one. We are off record.

(Recess taken.)

VIDEO OPERATOR: The time is 10:48 a.m.

This is the beginning of tape 2. We're back on the record.

Q Mr. Lefebvre, before the break we were talking about the unified shader and the R400, do you recall that?

A I recall conversations about the R400 unified shared, yes. I mean, if you want to talk about specifics, we can pull back my previous answers and discuss about them.

Q What is a shader?

MR. RENAUD: Objection.

A In the context of the R400, a shader is the block that runs the pixel in all the vertex programs.

Q What is a pixel program?

A So again, in the context of the R400, the R400 is what we call the programmable device, so you can start running small programs on the pixels that the chip generates to perform effects. This is what I referred to as a program, these small, well, programs, shaders; programmable pieces of a GPU.

Q Is a program in that context a set of instructions?

A In the R400 was a set of ALU, control flow and memory operations of some kind.

Q What is an ALU operation?
A An ALU operation in the R400 context is an arithmetic operation. Can be anything you want; an add, subtract, multiply, any kind of an arithmetic operation.
Q Were there logical operations that were supported in the R400?
A If you give me the specification, I can answer decisively, but my memory, according to my memory, yes, there were logical operations in the R400 supported.
Q By the ALU.
MR. RENAUD: Objection.
A If memory serves, it was more done by what we call the scalar unit.
Q What is a scalar unit?
A So the scalar unit is the unit that does anything that the ALU unit could not do; so more involved functions like exponentials, and you know, bit manipulation and logical operations of sort. And typically, not all the time, scalar operations apply to a whole vector of elements versus ALU operations that operate on a specific thread within that vector of elements.
Q When you say scalar, is that scalar with an A or

scalar with an E at the end? Actually, strike that. Can you spell scalar in this context, please?

A To me, that would be S C A L A R.

Q When you say "to me," have you seen it both ways before?

MR. RENAUD: Objection.

A I vaguely remember having seen it both ways, but English is my second language and I get some words wrong, and so I'm not your best reference in the English literature.

Q So you say scalar operations apply to a vector versus ALU operations on a specific thread; are you just talking about the number of either vertices or pixels that are getting affected by the operation?

A The R400 is operating on -- typically, a single instruction applies to multiple elements, and so when I say a vector, I mean -- I'm representing the elements on which each thread or sub element of that vector can have different data, but then the instruction is the same for all of them.

Q And for a scalar operation, the data would be the same for all of them?

A Yes. For the scalar operation, my understanding

is that you would be operating on a single bit of element, and then applying that result on the whole vector. You can use this, for example, for control flow operations of some sort.

Q Was the scalar processer separate from the ALU's?

MR. RENAUD: Objection.

A In the R400, there was separate piece of hardware that was doing the scalar processing, but they don't have to be in different blocks. I mean, they can even have -- they can be or they can be -- there can be some overlap between the ALU and the scalar. The main distinction is that the scalar is doing other kinds of operations than the ALU processer can be doing. And typically, applies to the whole vector.

Q Are the scalar and ALU part of the same unified shader?

MR. RENAUD: Objection.

A In the scope of the R400, they are both pieces of the unified shader, but one can envision any kind of implementation.

Q In the R400, are they part of the same processer?

A Can you define what you mean by processer?

Q Well, let me rephrase that then. What is a processer in the context of the R400?

MR. RENAUD: Objection.

A Processer. Yeah, you have -- I mean, if you give me the specification -- I don't recall exactly what this word was used for in the R400 specification itself, but talking from memory, a processer to me would mean the collection of ALU's that perform arithmetic operations.

Q Does that include the scalar?

MR. RENAUD: Objection.

A Again, I'm not seeing the specs and it's been a long time, but thinking from memory, yes, it would include -- it could include scalar operations as well.

Q What is a control flow operation?

MR. RENAUD: Objection.

A Control flow operation is an operation that prevents the executions of -- conditionally, prevents the execution of some instructions in the shader. It can be a loop, an if then else condition.

Q Is a branch a control flow operation?

A Yes. Branch is typically the operation you use to implement an if then else condition.

Q In the R400, where were the control flow operations executed?

MR. RENAUD: Objection.

A Again, it would be helpful if I had the spec over me, but best I recall, the operations were executed by the sequencer itself.

Q What spec would be helpful?

A Any kind of R400 sequencer spec would be fine with version two.

Q This is part of the sequencer logic?

MR. RENAUD: Objection.

A Can you say what do you mean by this?

Q Sure. Our discussion right now about the three different types of operations that you identified, is that part of the sequencer logic in the R400 and that's why the sequencer specification would have the information?

A So the scalar processer -- well the scalar unit, the L unit, they're in the SP, the shader pipe. The sequencer controls the control flow operations mostly, especially those that are applying to the whole vector. The reason why I'm asking for a sequencer spec is that I don't remember at what level and at what point we implemented a possible data dependent control flow instructions.

Q I will try and find that spec for you in a little bit. Just to follow-up on the last one, what is a

memory operation?

A A memory operation in the R400 scope is any kind of operation that involves writing to or reading to memory devices, D rams or system memory.

Q What's the difference between D rams or system memory?

MR. RENAUD: Objection.

A D ram are the memories that we typically put on a board along with a GPU or an APU, and the system memory is the memory that can also be accessed by the CPU.

Q When you say "put on a board," do you mean put on a chip?

A No. Typically when you have a GPU or a discrete graphics chip, the chip sits on a PCB board, which is then inserted into a PCI controller, so what I mean by board is the physical support that the chip is applied to.

Q Is there any memory on the chip?

MR. RENAUD: Objection.

A There are integrated memories on the R400 device, yes.

Q Are those D rams?

MR. RENAUD: Objection.

A Those are not what I would qualify -- well,

they're not the ones that pertain to what I described as the memory operations. When I was talking about memory operations, I was really talking about the memories that are outside the chip on the board.

Q And what in the R400 is responsible for processing those types of memory operations?

A That's an ambiguous question. I would like you to be more precise. I don't understand what you mean by processing.

Q How is a memory operation performed in the R400?

A Do you mean in the context of the shader of the R400 or -- because there is many blocks on the R400 device and some of these blocks have memory connections. So what are you asking about?

Q In the context of the shader of the R400, how are memory operations performed?

A Okay. The R400 shader contains options to, or instructions that allows either a pixel or a vertex shader to read data from memory, and so these instructions would be issued by the sequencer and executed by the SB to read the source GPRs, and then they could go through what we call the texture unit and then to the memory controller, and eventually the memory system.

Q Okay. There was a lot there so I'm going to ask you some follow-up questions.

What is the difference between instructions and operations?

MR. RENAUD: Objection.

A An instruction is the control that is in the program that tells the hardware how to -- what to fetch and how to fetch it, and the operation, again in my own definition and in the R400, is how this instruction gets executed on the hardware, the steps.

Q What is the role of the sequencer with regard to instruction execution?

MR. RENAUD: Objection.

A So in the R400, the sequencer had the role to choose which instructions would be executed next between pixels and vertices because of the unified nature of the shader as well as the ordering of the instruction within each shader type.

Q Does shader type refer to vertex and pixel?

A When I say "shader type" in the R400, I refer to pixels and vertices, yes.

Q Are there any other kinds of shader types with regard to the R400?

A At the time, those were the only two types that I

remember.

Q How did the sequencer order the instructions?

A What is your question? Can you repeat the question, please.

(Question read back.)

A The instruction order per type is defined by the program itself which is written by the programmer, and the sequencer has to follow that order. So it then forces that order per shader type, but it also gets to pick where to apply the machine between vertex and pixels, and that, that can be done many different ways.

Q What different ways are you referring to?

A So in the R400 again, remember we have a shader that is able to operate both pixels and vertices, and so depending on the workload that a chip gets, you can do more pixel work and less vertex work, or vice versa, or have a mix of the two types. That's what I mean by any type.

Q Did the sequencer order which instruction will get executed within each shader type?

A I think I already answered that question. I said that the execution was fixed by the programmer, and the sequencer is enforcing the instruction order within each shader type.

Q So the sequencer can only handle one instruction set per shader type at a time, is that correct?

MR. RENAUD: Objection.

A I am not clear on your question. I don't understand what you're asking.

Q I think what you said was that the sequencer did not have any responsibilities with regard to determining which instruction was next within, say, the possible set of pixel instructions. Is that correct?

MR. RENAUD: Objection.

A So in the R400, you can have, potentially, several pixel vectors all at once in a shader. Within a pixel vector, you have to use the ordering as instructed by the program, but you can choose to execute the next instruction of any of the pixel vectors that are on the system.

Q And is the sequencer responsible for that decision?

MR. RENAUD: Objection.

A The R400 sequencer is responsible for making that decision, and the decision of whether or not it wants to execute a vertex or a pixel execution, yes.

Q You said that within each, let's say pixel vector,

the sequence of instructions is determined by the programmer, is that correct?

A It -- within -- so again, I answered that already, so we could go back to the answer, but my recollection is that for one pixel wave, yes, you have to execute the program as it's specified by the shader.

Q Does the sequencer have any role with regard to enforcing that the instructions are executed in the correct order with regard to timing?

MR. RENAUD: Objection.

A What do you mean by "timing"?

Q For example, if one instruction had a dependency on another instruction, is it the sequencer that's responsible for determining that the first instruction is done executing before the next instruction begins?

MR. RENAUD: Objection.

A The R400 sequencer had that capability, yes. Although I could envision a hardware device where its responsibility is enforced by the compiler or software.

Q The compiler could put some sort of instructions in that require waiting, is that what you're saying?

MR. RENAUD: Objection.

A The -- there are many ways to enforce this. The R400 had specific controls to allow for that, and those were enforced by the R400 sequencer.

MR. ELENGOLD: I ask the court reporter to please mark Exhibit 3.

(Document marked Exhibit 3 for identification.)

MR. ELENGOLD: I'll note for the record that Exhibit 3 is Bates labeled AMD1044_175470 through 175485.

Q Mr. Lefebvre, have you seen Exhibit 3 before?

A Yes. This is the R400, or this looks to be like it is the R400 Architecture Proposal version one by Steve Morein. I just want to say that my versions are underscore 0175470 and not underscore 17, so I don't know if it makes any difference to you, but I have a zero.

Q Mine are the same. So yeah, that will be part of the actual record. Sometimes I'm leaving out zeros when I say the number, but that's fine. Just so we're clear for the record, it's underscore 0175470 through 485.

When was the first time you saw Exhibit 3?

A I don't recall the exact date at which I saw this

proposal. I mean, must have been around the creation date. I remember having discussions with Steve about this particular spec, but as to exactly when I first saw this, I don't recall the specifics.

Q Who is Steve?

A Steve Morein is or was an architect at ATI and is also the author of the spec as stated here on the first page.

Q What was the purpose of the R400 Architecture Proposal?

A I believe the purpose is stated on the page and I'm going to read, "This is a proposal for the overall architecture of the R400. It's just a proposal and nothing is decided yet." So it's to initiate discussions about the R400 project.

Q Do you know when this document was created?

A I don't have memories as to when it was created, but it states an originate date of 2000-11-13. And I have no reason to believe those are wrong.

Q And you started working on the R400 you said in September of 2000, is that correct?

A I said that I started working on pearl and noise, which you know, we were investigating for the R400, yes, around that timeframe.

Q So do you know when the first discussions around the R400 began at ATI?
A Discussion about what part, I mean, of the R400? Like I said, the R400 is a very broad subject. So are you asking specifically about what part?
As a whole?
Q I mean, do you know when the first planning for the R400 started at ATI?
A I don't remember exactly when it occurred, but you know, given I was working, at the very least I was working on the FC prior to September 11, 2001, and this dates from November 13, 2000. That must have been in this vicinity.
Q Around November of 2000?
A Around November 13, 2000, yeah.
Q Was this the first document to your knowledge that described the R400 architecture?
MR. RENAUD: Objection.
A I recall having seen diagrams from Steve. I don't know if you call them documents. This is one of the documents that describes the R400. Whether it's the first one or not, I don't recall exactly.
Q Are there others from the same time period?
A There might have been. I don't recall them if there were.

Q Do you know if ATI searched for those documents for this investigation?

MR. RENAUD: Objection.

A I know that a team of people searched for it, but I also know that this time period, we were using a separate source revision control than Perforce, which made the search much harder for that time period because of it being antiquated and not available.

Q When did Perforce start being used?

A I don't remember exactly but, you know, we could go back to the logs, and obviously, the first submissions to the depot would point as to a pretty good idea of when the date was established, effectively.

Q So you're not sure whether there were or were not other documents in this time period regarding the R400 architecture, is that right?

MR. RENAUD: Objection.

A Like I said, I recall at least diagrams from Steve. There's definitely this one. Whether or not there are others available, I don't know.

Q Do you recall any others?

A Well, I was working on the pearl and noise, so you know, I have every reason to believe there would

be a pearl and noise specification somewhere, as well as some time later, a scan converter specification in my name, and so forth. But as to when exactly, I don't know.

Q So going back to the Architecture Proposal which is Exhibit 3, is this a document that you reviewed in your preparation for your deposition?

A I don't recall specifically reviewing this document for this particular deposition, but I did review it many times over, as it was part of my two previous depositions as you can see by Exhibit 5 on 12/9/16.

Q At the time of the Architecture Proposal that's Exhibit 3, had you already discussed with Mr. Morein the idea of using a unified shader in the R400?

MR. RENAUD: Objection.

A So you mean at the time of the spec was published did I --

Q At the time of November 2000, had you already discussed with Mr. Morein the idea of using a unified shader in the R400?

A I know I had discussions with Steve Morein on the subject matter. When exactly these occurred versus this particular specification, I don't

remember. I mean, I did discuss this before in my previous testimonies and deposition. We could go grab the records, but that's my recollection. I had discussions with Steve.

Q Whose idea was it to combine the vertex and pixel shaders into a unified shader?

MR. RENAUD: Objection.

A So Steve came up, as best I can understand, came up with the original concept, but both myself and Andy Gruber all worked on blocks and issues and systems within that unified shader, so as such, it's a collective effort, I would say.

Q Are you referring to the patented invention now, the patents, or are you talking about the idea of putting a unified shader into the R400?

MR. RENAUD: Objection.

Q Strike that. You said, just so it's clear for the record, you said Andy -- sorry, what was his last name?

A So there were two Andys, Andi Skende and Andy Gruber. Or Andy Gruber also goes by Andrew Gruber, and Skende is Andi with an I.

Q So Exhibit 3, which is in front you, discusses the idea of using a unified shader for vertex and pixel operations in the R400, is that correct?

MR. RENAUD: Objection.

A Well, the spec actually calls for, and I quote on page 6 of 16, that "the most ambitious feature in this design is the 'truly unified pipe': a single programmable pipeline is used for 2D, video, 3D vertex, and 3D pixel," so it would apply more than just pixels and vertices, but inclusive of, yes.

Q So the idea at the time ,in November of 2000 ,was to unify 2D, video, 3D vertex, and 3D pixel operations into a single shader, is that correct?

MR. RENAUD: Objection.

A According to the spec, yes, it was the original concept.

Q And did you just say that prior to Mr. Morein putting together this document, you, Mr. Skende -- is it Mr. Skende or Mrs. Skende?

A Mr. Skende.

Q Mr. Skende, Mr. Gruber, and Mr. Morein all collectively talked about that idea, is that correct?

MR. RENAUD: Objection.

A I didn't say that prior to the spec. I said I remember collectively working on the unified shader. I don't know exactly when all these occurred versus through the creation of this spec.

Q Do you know who first suggested the idea of combining vertex and pixel operations into a single shader?

MR. RENAUD: Objection.

A Like I previously stated in my prior depositions, I believe I said that I thought that Steve Morein came up with the original idea, or the original concept, and then we worked collectively to further the idea into a design.

Q Do you recall having contributed to this document, the R400 Architecture Proposal that's Exhibit 3?

MR. RENAUD: Objection.

A Can you define what you mean by "contributed"? You mean typing words into the spec or do you mean having --

Q Did you write any parts of Exhibit 3?

A I don't recall writing personally any part of Exhibit 3, no.

Q When did you first start working with Mr. Skende on the R400?

MR. RENAUD: Objection.

A So best I can recall, Mr. Skende was working on the R200 at the very, very onset of my beginning to work at ATI. And again, if I recall correctly, and I'm talking from very, very long time memory,

the interactions really started in earnest when we were developing the sequencer and the shader pipe for the unified shader, so would have been somewhere around the September 2001 timeframe.

Q What is the R200?

A The R200 is the chip that preceded the R300 in nomenclature and was developed by the, in part by the Orlando -- not the Orlando office -- well, the Orlando office, yes, but also the Marlborough office, which I was part of.

Q Was the R200 ever manufactured into a chip?

A Yes, my recollection is that it was, yes.

Q Do you recall the name of that chip?

A I don't recall the name. I know the internal project name was Chaplain, and probably was called something like Radeon, but like I said, I'm terrible with marketing names. We never use them in engineering.

Q When did you first start working with Mr. Gruber?

A Can you refine the question please because Mr. Andy Gruber was my manager right from the onset, so --

Q When did you start working on the R400 with Mr. Gruber?

A On the R -- I mean I've been always working on the

R400 project, so Andy Gruber was my manager and engaged in technical discussions right from the beginning on the various topics that were assigned to me, so as far as I know, I've been working with Mr. Gruber for the whole time that I was employed in the Boston office.

Q September 2000?

MR. RENAUD: Objection.

A From my initial employment day, yeah; September 2000 to, until I moved back to Montreal.

Q What was Mr. Gruber's title at the time you worked with him on the unified shader?

A I believe I already answered that question in a previous deposition, so you must already know the answer to that, but I don't recall what his title was. I didn't recall it then, I don't recall it now.

Q What was Mr. Skende's title when you worked with him on the unified shader?

MR. RENAUD: Objection.

A Some kind of engineer. Again, I don't recall exactly.

Q Do you recall Mr. Morein's title when you worked with him on the unified shader?

MR. RENAUD: Objection.

A No, not directly either. Again, these are all questions that I'm pretty sure I answered previously in depositions.

Q You understand this is a different case from your prior depositions, correct?

A I do understand, and you have every right to ask your questions, but I also understand you have all that documentation, so it is available to you and they are the exact same questions. As far as I remember.

Q Is all of your prior testimony, do you believe, correct as you sit here today?

MR. RENAUD: Objection.

A So as I read through them, I found a few typos and filed a errata sheet for both, and could not find other discrepancies as best as I can tell, but if you want to bring them up and discuss them, I'm more than welcome to comment on them if you want to.

Q To your point, it seems rather than walk through some of the stuff you believe you already answered, do you still stand behind all of your prior deposition testimony as being accurate and correct?

MR. RENAUD: Objection.

A I could not find any inaccuracies in my previous testimonies other than those noted in the errata sheets.

Q And did you review them earlier this week?

MR. RENAUD: Objection.

A I did read through both of my depositions earlier this week, yes.

MR. ELENGOLD: I'll ask the court reporter to please mark Exhibit 4.

(Document marked Exhibit 4 for identification.)

MR. ELENGOLD: I'll note for the record that Exhibit 4, the first page is Bates labeled AMD1044_0012459 through 12617.

Q Mr. Lefebvre, have you seen Exhibit 4 before?

A Yes. This appears to be my deposition that I did in Montreal. It's missing the errata sheet though.

Q This is the deposition, the first deposition you referred to earlier that appears to have occurred in November of 2015, is that correct?

MR. RENAUD: Objection.

A Yes. And at the time, I did not remember the date but looks to be right. Again, it is missing the errata sheet that was filed late.

MR. ELENGOLD: I'm not aware of us having received a copy of the errata sheet, so I'll just note for counsel that if you guys have that and want to make sure that's produced, that would be helpful.

MR. RENAUD: Okay.

Q So other than the errata sheet, is this a complete and accurate copy of your testimony from November 2015?

A Yes. This looks to be.

Q You were under oath during this deposition, is that correct?

A Yes, I was under oath during the deposition.

Q Is there anything, sitting here now, other than the errata sheet, that you wish to correct from your prior deposition transcript?

MR. RENAUD: Objection.

A You want me to reread it in light of everything that we discussed today? I can do so now, I mean --

Q That's up to you. You know, I know you said you just reviewed it and that, you know, it appeared to me that you were expressing a lot of frustration with getting asked questions that you felt like you had previously answered, so I'm

offering you an opportunity to say that you believe that this deposition transcript is still true and accurate with regard to your answers. Is that the case? Is this deposition transcript true and accurate to your knowledge?

MR. RENAUD: Objection.

A To the best of my knowledge. I mean, there could be dates here and there that I got wrong or anything, but the generic sense when I read through it yesterday -- it was yesterday, it was not just now -- looked to be accurate. Yeah.

MR. ELENGOLD: I'll ask the court reporter to please mark Exhibit 5.

(Document marked Exhibit 5 for identification.)

Q Before we turn to Exhibit 5, one more question for you, Mr. Lefebvre, what was the subject matter of your deposition in Exhibit 4?

MR. RENAUD: Objection.

A Well, the first date -- the first page, sorry, states that this was related to case IPR-2015-00325, Patent 7,742,053 B2; Case IPR-2015-00326, Patent 6,897,871, and Case IPR-2015-00330, Patent 7,327,369 B2. So I don't know.

Q You just read the case caption, correct?
A Yes.
Q Do you recall what the subject matter was of the deposition -- or strike that. Do you recall why you were deposed in that case?
MR. RENAUD: Objection.
A I recall talking in this deposition about the R400 sequencer and multi-threaded patent which was -- and also the unified shader patent, but specifically, what was the purpose, I don't recall exactly.
Q When you say the "unified shader patent," is that your understanding of the same family of patents that's at issue in this investigation?
MR. RENAUD: Objection.
A So my recollection is one of these patents, yes, was from that family.
Q Turning now to Exhibit 5, which is Bates stamped AMD1044_0175035 through 175187.
Mr. Lefebvre, have you seen Exhibit 5 before?
A Yes, I have seen this Exhibit before.
Q What is Exhibit 5?
A This is the videotape deposition that I did on December 9, 2016.

Q Do you recall the subject matter of that deposition?

MR. RENAUD: Objection.

A So I recall some, again, some subjects that were discussed in this deposition, and they included the '871 unified shader patent, as well as you can see from the Exhibits, several specifications from the R400 and some presentation program reviews.

Q Did you review this deposition yesterday in your preparations?

A Yes, I read through this deposition.

Q Do you believe your testimony in this deposition to still be true and accurate?

MR. RENAUD: Objection.

A I didn't find any inaccuracies that I'm aware of. I mean, doesn't mean that there aren't any, but I couldn't find them while reading through these.

Q Is there anything you wish to correct in Exhibits 4 or 5 for this deposition?

A Not that I know of, but you know, if you want to point me to specifics, which I'm sure we'll do, we can discuss them. I don't know anything wrong offhand right now with these depositions.

MR. RENAUD: And just to clarify the record, counsel, I believe there is an errata sheet.

A There is also an errata sheet.

MR. RENAUD: We're going to confirm it's either been produced or produce it.

MR. ELENGOLD: That would be great. Thank you.

Q So, you know, just to make sure the record is clear then on that point, so other than the two errata sheets, is there anything in Exhibits 4 and Exhibit 5 that you wish to correct today for this deposition?

A Again, I'm human, but from reading through those, they sound correct. So they sounded correct when I read through them.

MR. ELENGOLD: I'll ask the court reporter to please mark Exhibit 6.

(document marked Exhibit 6 for identification.)

MR. ELENGOLD: For the record, Exhibit 6 is Bates stamped AMD1044_0011617 through 11682.

Q Mr. Lefebvre, have you seen Exhibit 6 before?

A Yes, I have seen Exhibit 6 before.

Q What is Exhibit 6?

A This is, and I quote "Declaration of Inventor Laurent Lefebvre Regarding the Invention Date of U.S. Patent 6897871.

Q Did you author Exhibit 6?
A I prepared Exhibit 6 with the help of counsel, yes.
Q Who wrote Exhibit 6?
MR. RENAUD: Objection.
A Exhibit 6 was written by counsel upon my instructions and guidance.
Q And not your counsel here today, but prior counsel you worked with, is that correct?
A Yes. This is what I remember, correct.
Q Why did you work with counsel to prepare the declaration in Exhibit 6?
MR. RENAUD: And I'll instruct you not to answer if that calls for revealing any attorney/client communication.
A My understanding is that this declaration was created to establish a date of invention, or of creation, if you will, of the R400.
Q Do you mean a date of invention of creation for the patent at issue that's on the front page, or for the R400?
MR. RENAUD: Objection.
A I meant establish an earlier date than the patent was issued.
Q An earlier date for what?

MR. RENAUD: Objection.

A An earlier date for the creation or, you know -- to show that we had a product prior to having filed the patent.

Q A product that you believe practices the patent?

MR. RENAUD: Objection.

A I am not a lawyer so I can't really exactly understand what practice means in terms of the law, but my understanding is that yes, to show that we had a product that was working and was performing the operations of a unified shader prior to the date of the patent being issued, or at least show that the work started well before the patent issuance date.

Q Did you review this declaration that is Exhibit 6 in your preparation for today's deposition?

MR. RENAUD: Objection.

A Yes, I browsed through this deposition for preparing to this deposition.

Q Was that yesterday?

A I don't remember if it was yesterday or the day before, but it was in between these two dates.

Q This declaration, like your depositions, was sworn under oath, is that correct?

MR. RENAUD: Objection.

A This is correct. I mean, there is my electronic signature here on the last page. I have no reason to believe it's wrong.

Q Do you still believe that the statements you made in your declaration are true and accurate?

MR. RENAUD: Objection.

A At best I can recall, yes. I mean, I did not see any inaccuracies as I browsed through this document for preparing to this deposition.

Q Is there anything you wish to correct in this document?

A No. Not that I know of.

Q So I'll ask you to turn to paragraph 6, please, on page 3. And do you see where it says in the second sentence, "We collectively conceived of the graphics-processing system claimed in the '871 patent no later than early 2002, while working on the R400"?

A Yes. I see.

Q What did you mean by that statement?

A So again, the specific wording is not mine. It was written by counsel, but reading this, to me it means that the -- we conceived or we made a product called the R400, and it was operating to perform pixel and vertex functions, no later than

early 2002.

Q What did you mean by the graphics-processing system claimed in the '871 patent?

MR. RENAUD: Objection.

A So again, these are not my words. They're the words of my counsel, but the graphics-processing system is the graphics core of a GPU. So the whole graphics infrastructure.

Q And did you intend to offer testimony regarding when you conceived of the actual claimed system in the patent, or were you trying to just refer to the R400 in your statement?

MR. RENAUD: Objection.

Q You can strike that.

And I know I'm going to ask you some general question, but I wanted to have these documents in front you, so please feel free to reference them if you would like to as we go through the day since I know you mentioned that you wanted to ensure your accuracy across the documents so --

A I appreciate that.

Q Is that helpful to have those in front you now?

A Yes. I will, as, if I remember more, refer to these documents.

Q So now -- and I'll tell you, looking at your

declaration on page 4, you said, "The R400 includes a unified shader -- the R400 includes a unified shader that performs both pixel operations and vertex operations," do you see that?

A Yes, I see in this proposal, the R400 includes a unified shader that performs both pixel operations and vertex operations. That's what's written here.

Q What are pixel operations?

A Pixel operations in the R400 context would mean pixel shader operations in my opinion; the instruction that you execute in a pixel shader, the programmable section of the pixel pipeline.

Q Does that determine pixel color?

MR. RENAUD: Objection.

A That is part of the process that determines pixels colors, yes, in the R400.

Q What are the other purposes of pixel operations other than color?

A I don't have the R400 sequencer specifications, so I don't recall exactly, but one of the other operations that I know is feasible in a pixel shader is what we call a kill operation, which would just plain remove a pixel from being generated. So this is one other example of an

operation that you can do in a pixel shader that does not affect color.

Q Any others?

A Offhand, not that I can remember from the pixel shader side, no.

Q What is a vertex operation?

MR. RENAUD: Objection.

A In the R400 context, and assuming by "vertex operation" you mean vertex shader operation, that would be the instructions executed on the vertex shader.

Q What types of operations are instructed on -- sorry, strike that.

What types of operations are executed on a vertex shader?

MR. RENAUD: Objection.

A On the R400, the vertex shader supported, I believe -- again, you give me the R400 sequencer specification I can be more precise, but my recollection is that it allowed for memory fetch operations as well as scalar operations, ALU operations, and control flow.

Q What were the benefits of using a unified shader in the R400?

A Okay, so that's one I know I answered already.

Q Do you know of any as you sit here today or do you need to look at your prior testimony?

MR. RENAUD: Objection.

A I can give you my recollection of what I recall in my testimony, but I can guarantee it's going to match word for word. I have a pretty good idea of what was said, so if that's satisfactory to you.

Q Yeah. So as a general rule, as we go through, I wanted you to have these available since you asked frequently about your prior testimony, but you know, let me ask this: Do you plan to offer any testimony at the hearing in this investigation?

MR. RENAUD: Objection.

A I don't know. I mean, that's not my call or anything.

Q Right. So for those purposes, when I ask you questions, you know, if there is anything you can think of as you sit here today, I would like you to try to answer the questions today, and if you need to refer back to prior testimony, then you're welcome to say that you need to look it up because you don't recall.

A Okay.

Q Okay. So as you sit here today, do you know, were there any benefits to using a unified shader in

the R400?

A Okay. The benefits of the R400 unified shader are two fold. The first one is that it is an area reduction benefit by which you can only have one shader instead of two. So it's by definition smaller.

The second benefit is that it can operate on both pixels and vertices dynamically and assign the shader to either or both pixels and vertices depending on the workload, and the third benefit is that having only one shader core to validate, it simplifies the validation purposes.

Q By "validation," you mean testing for commercialization?

A By validation, I mean testing, yes.

Q What kind of validation is done to make sure that GPU works successfully?

MR. RENAUD: Objection.

A Do you mean the classes of verification? I am not -- this is a pretty broad question. I want to make sure that I answer it very directly.

Q That's fine.

A So what are you concerned about?

Q Well, you mentioned that validation is a benefit of using unified shared, correct?

A I said that the -- one of the benefits of having a pixel and vertex shader unification like in the R400 is that you only have one shader core, thus it reduces the amount of verification that is needed because you don't have to test two separate pieces of hardware.

Q Is that a lot of work, the testing process?

MR. RENAUD: Objection.

A I would say that the verification of a chip is substantial work, yes.

Q What's involved in that verification?

A When we had to validate the R400 design, we had to basically verify all of the features of the chip, as well as the general operation of the device, and what makes it hard in silicon design is the fact that until you have a prototype of the chip on the FPGA or something, the simulation infrastructure that we have to use is very slow, and so that makes it for a very long period of time to walk through all the sub-features required by commercial product.

Q Is that the C simulator you're referring to that's much slower?

A No. The C plus plus model, which I am assuming is what you're referring to by the C sim, like

discussed before, is relatively, relatively-speaking, fast.

The RTL simulation itself, when you run the RTL code, then you're trying to compare it with the golden C simulator. That is the thing that takes a lot of time.

Q Is it -- does it take a lot of time because you're fixing errors in the RTL, or does it take a lot of time because it's just slow to run tests?

MR. RENAUD: Objection.

A It takes a lot of time because it's just very slow to run anything. I mean, for example, you can't imagine running a few frames of a game on an RTL simulator. It just -- it would take months.

Q And the FPGA simulator lets you run those tests faster?

MR. RENAUD: Objection.

A Yes, the FPGA device, hardware device lets you run tests much, much faster.

Q Why is that?

A In part, because it is a hardware device, so it's not an emulation of the system. It is the system in some hardware form and it can run the system -- it doesn't have to emulate the system. It just, you know, runs as if it was a chip just at a much

reduced clock speed that you would be able to operate the silicon at.

Q I'm a little confused about what you said because I think earlier you said that it is emulating what the chip will look like, but now you said it's not an emulation, it's not an emulation of the graphic system, but it is a emulation of the chip, is that correct?

MR. RENAUD: Objection.

A So the FPGA device is a hardware device that can be configured any way you want. So you can push a netlist on it, and effectively, it becomes that device. The gates are configured in the same way as you would have on an actual silicon piece that would you commercialize.

Q It's programmed to act like what the gates will look like when they're actually created in silicon, is that right?

A So I am not an expert on the actual IKOS device itself, but my understanding is FPGAs are gates, and what you can do is connect them any way you want. And so by pushing a netlist on them, you connect them in the same way they would be connected as on the actual silicon device. So in all essence, it becomes that device, but it's not

something obviously you can commercialize because it's very expensive, it's very big.

Q And so in order to do that, it's already been laid out at that point, like the F -- I'm sorry, I keep getting the -- P --

A FPGA.

Q No, no, I'm sorry, the team we were talking about earlier.

A PD.

Q The PD team. So it's already been laid out in order to see how all those interconnections will work by the PD team?

MR. RENAUD: Objection.

A Not being on the IKOS, you know, team, I don't have the, in great details exactly how that process works, and AMD can bring in the experts if you want more details on that. We have some people, but I don't know to what extent it needs to be floor plan to be able to operate on the FPGA.

Q Did you -- sorry, go ahead.

A It starts from the same netlist, that is what I was wanting to say.

Q Did you work on the netlist?

MR. RENAUD: Objection.

A Can you define what you mean by "work on the netlist"? I mean --

Q Did you have any responsibilities with regard to creation of the netlist?

MR. RENAUD: Objection.

A The creation of the netlist is an automated process by which we call synthesis. It takes in the RTL and, you know, outputs the netlist. So that would have been the responsibility of the RTL designer, but effectively, it's our design, so I'm not directly connected to the netlist, but in a sense, I've worked on the netlist. I mean --

Q Your specification results in a netlist.

MR. RENAUD: Objection.

A The work that I've done in specifying the R400 sequencer, as well as the models that we created, the C sim model to validate the RTL, they all turn into eventually the netlist because they are used to generate that netlist, indirectly.

Q Some of this is new because I don't think you described the FPGA simulator in your declaration, is that correct?

MR. RENAUD: Objection.

A That is correct. I don't think that I described these in my previous declarations because I was

not aware at the time that we did FPGA simulations, or I did not recall at the time that we did FPGA simulation, or FPGA prototyping would be a better word, on the R400. I mean, it is common practice, but again, it's been so long, I was not aware when exactly we started doing that process.

Q And when did you start looking into that?

MR. RENAUD: Objection.

A The legal -- I mean not the legal team, but the team at AMD that collected the document brought to me evidence that the IKOS machine was used in the R400 project.

MR. RENAUD: I don't want you to give any communications with that team, but you can continue your answer.

THE WITNESS: Yes, sir.

A And so those were the two presentations that I divulged before that, you know, describe the netlist, what they were, and the progress on IKOS, and so that is when I got aware of the IKOS prototyping effort.

Q When was that?

A These documents were disclosed to me over the last two days.

Q And were they disclosed to you by counsel or someone from AMD?

MR. RENAUD: You can answer that with either of those answers, counsel or AMD.

A Counsel.

Q Were you involved in any work with the FPGA system?

MR. RENAUD: Objection.

A Again, in the R400 it's the same thing. I was not directly involved into the work of pushing the netlist on the FPGA prototype, but I was involved in the design of the R400, so indirectly, you know, you can involve me with any given step of the way, but I did not directly work on the IKOS machine, no.

Q Who did?

A So during the break, I browsed through some documents we had, and at least there was a person named Colin Stuart that was named in the logs, and by the way, he is the one that I spoke on the phone with for preparation.

There was another name, but unfortunately, I lost it again. But it's in --

MR. RENAUD: I can tell you what that name is if it's helpful.

MR. ELENGOLD: That's okay. Let's let him testify.

A I forgot about it. I knew the names coming in but then we discussed things.

Q Did you talk to your counsel about the substance of your deposition during the break? Just a yes or no question.

A No.

Q You reviewed these documents on your own?

MR. RENAUD: You can answer that yes or no.

A Yes.

Q What documents did you review during the break?

A There was an IKOS log file document that listed all the interactions and steps involving IKOS. I mean, it's probably not an all inclusive document, but at the very least, it had a few names and information that were helpful into establishing the IKOS work.

Q What do you mean by "establishing the IKOS work"?

A I mean which netlist was ported to the IKOS and when that netlist was pushed on the IKOS machine.

Q Is a netlist tied to a version of RTL?

MR. RENAUD: Objection.

A Okay. This is a tricky answer. A netlist is a collection of synthesis files, and the collection

of synthesis and/or verilog files can come from different change lists. So you can tie a netlist to the list of synthesis files, and through that, establish a range of dates for which the RTL was used to generate the netlist.

Q Okay. What you're referring to with the FPGA system, when did that occur, the first time the R400 was put into the IKOS machine?

A So there is a presentation, like I said, that is dated February of 2003, if memory serves, that states that by that time, according to the presentation again, it said that the IKOS work was progressing rapidly or quickly, I don't exactly remember, I'm paraphrasing, but so you could say that no later than that date, the work had been done on the IKOS machine prototype.

Q And it started before that date because it was progressing?

MR. RENAUD: Objection.

A State again, please.

Q You're saying it started before February 2003, correct?

MR. RENAUD: Objection.

A I'm saying that the netlist was on the IKOS machine prototype no later than that date because

that presentation states that the work was progressing well on IKOS, which infers that the netlist was present and it's actually working rapidly.

Q So what kind of work was being done?

MR. RENAUD: Objection.

A So as best I can tell from the presentations, and the various documents that I've seen, and this is fairly new information so I'm sure you have more questioning and they can provide more substance to that matter, the work that was done at the time was at the very least registered reads and writes, and there was another topic too that was stated in that presentation. So if you bring it up, we can just look at it and I can point you to it exactly.

Q Registered read writes. Anything else you know of that was being done at the time with respect to IKOS work?

A There is a -- so like I said, there is another topic that escapes my memory. And also, some other presentations that I saw in both these actually depositions, the program reviews, they talk about IKOS with software, so those would be dates of establishment of when the driver was expected to run on the IKOS prototype.

Q What is the driver?
A For the R400 GPU, in order to connect an application which is, you know, a game or anything to the hardware system, the application goes through what we call an API which defines the operations that the application can perform, but that API defines broadly what applications can do, and has to be vendor independent so that applications can work on any graphics device.

What sits under that API is a driver which is a software piece of code that interprets the API commands and translates them to hardware commands.

Q So do you know when the driver first ran on the FPGA system?

MR. RENAUD: Objection.

A From what I could gather at this point, I couldn't -- I don't have a conclusive date. I mean I see, like I said, see some projection dates in these program reviews. This is all very fresh. Like I said, I'm sure if you want to dig into that more, AMD can provide more information, but at this point I cannot give you any dates.

Q And is all your information regarding the IKOS system from the documents you've reviewed in the

past two days?

MR. RENAUD: Objection.

MR. ELENGOLD: Sorry, strike that.

Q Is all your knowledge regarding the IKOS system in the R400 from the documents you've reviewed in the past two days?

MR. RENAUD: Objection.

A I would say most of my knowledge, you know, as I stated, there are some indications in the program reviews about some IKOS dates in there which I didn't pay attention to before, but the information was there. So to be fair, it was there, not to a great extent though.

Q Is all your knowledge regarding the IKOS system from documents that you have reviewed, or do you have any personal recollections regarding any of the IKOS testing?

MR. RENAUD: Objection.

A No, not having worked directly on the IKOS prototype device, I don't have any personal recollection of such.

Q Did you talk to anyone about the FPGA system in the IKOS testing?

A One of the phone calls that we had yesterday or the day before, I don't remember, was about that

topic, yes.
Q Who did you talk to?
A That Colin Stuart, and that other person which my counsel can give you the name to. It's also in that, in the documents so --
Q Who is Colin Stuart?
A Colin Stuart, as I understand it, is a manager; at least at the time, he was managing the IKOS effort.
Q Is Mr. Stuart still at AMD or ATI?
A To the best of my knowledge, since I talked to him yesterday or the day before, yes.
Q So he was still when you talked to him?
A Yes.
Q Do you know Mr. Stuart's current position?
A No. Unfortunately not, but I can find that out if you want to.
Q How long did you talk to Mr. Stuart for?
A My recollection was in the vicinity of half an hour to 45 minutes.
Q What did you learn with regard to the FPGA system and the IKOS testing from Mr. Stuart?
A Mostly the timelines and what was on the IKOS machine at the time. That kind of information.
Q What timelines did you learn?

A So again, I don't recall the specifics, but Mr. Stuart is named into file log and that file log that the dates of the entries, and so while I don't remember the exact dates and stuff, I could tell, you know, what was going on, and that file log also was stating which netlist -- because each netlist has a number -- was used for IKOS.

So you know, we just had the opportunity to discuss that and make sure we were aligned.

Q What do you mean? What do you mean aligned?

A Aligned on the, that the data that I was seeing in the log was consistent with his memory because, you know, he was much more hands-on than I would have been on the IKOS machine.

Q So what timelines do you recall learning from Mr. Stuart?

A I mean corroborating evidence that the work on IKOS was, you know, at least done to some extent prior to that presentation.

Q February 2000?

A February 2000, yeah, making sure the presentation and the logs were consistent.

So I wouldn't say that I learned any new dates from the discussion. It was more to, as best as we could, make sure that everything was

connected because again, this is a long, long time ago, a lot of people left the company, so you know, due diligence as much as we could.

Q So you asked Mr. Stuart if he remembered the log entries that had his name in them, is that correct?

A Yes, I did.

Q Did he remember them?

A No, he didn't from my discussion with him.

Q As far as what was on the machine, you said you also discussed that with Mr. Stuart; what did he tell you was on the machine?

A Not much more than what was in the log because unfortunately, he did not remember much from that era, it was too long ago. So we just tried to discuss with him the various evidence we had and best we could piece the puzzle together, but I don't remember any loud insight he has, he had, sorry, over the IKOS prototyping effort.

Q Were you able to, with Mr. Stuart in your discussions, identify exactly which RTL versions would have been involved in what was on the machine?

MR. RENAUD: Objection.

A No, and actually, that was the subject of the

second phone discussion that I had with Mr. Christie to try to establish that link, and we ran out of time, but my understanding is that he is continuing on that endeavor, and there is a lot of information on the Perforce server. It's sometimes poorly labeled, so I tried to gather as much as I could within the time constraints.

Q But as of right now, you're still not sure what RTL went into the netlist that went into the IKOS machine, is that correct?

MR. RENAUD: Objection.

A So what I can tell you is because the netlist was created according to the presentations no later than February 2003, it would have been a version of the RTL prior to that date. I cannot give you the specifics, but you have to have the RTL prior to have the netlist, and so it has to be a collection of these RTL files, and it has to be before that date.

And also, typically -- and this is like from more recent. I'm going to talk to you from the recent ways we do it at AMD. Typically now we try to freeze and branch the RTL into a branch a month before the netlist so it's stable.

So I don't remember if it was the practice

back then, but, you know, that should give you -- those are the guidelines I can provide.

Q You're not aware of any frozen set of RTL that represents what was put on the IKOS machine, correct?

MR. RENAUD: Objection.

A So I am aware of Netlist 3, and that there is evidence that these files are -- eventually came from a branch, and so the question is, yes, there is evidence of freezing the RTL. What we could not assess yet is what RTL files were pulled into that branch and eventually pushed onto the Netlist 3. That's the part what we're missing right now.

Q Why do you refer to it as Netlist 3? Was there a Netlist 2?

A There is evidence on the Perforce server of many netlist numbers; some poorly named, some well named, but the reason why I'm referring to Netlist 3 is that this is a number that we could find that is consistent across netlist generation and documentation and presentation, so that we can establish a link on what went on when, where.

Q When was the first netlist created?

MR. RENAUD: Objection.

A I don't recall directly, but I believe it's in one

of the executive presentation calendar that are parts of the Exhibits that were already discussed. I don't know that there was a question to that regard. I don't exactly recall. And if you want me to dig through I could look at it, but I know this information is at least in part in these calendar slides.

Q Do you have an idea of when the first netlist is generally created out of RTL in a project?

MR. RENAUD: Objection.

A The R400, I mean we try to do it as soon as the RTL is stable enough.

Like I said, I mean, these dates are readily available in the documentations that you have and that we discussed. So if you want us to look at that calendar, we can. I don't recall the specific dates.

Q Do you know when the RTL was stable for the R400?

MR. RENAUD: Objection.

A Yeah, I also don't recall the specifics on that.

Q What does it mean for the RTL to be stable?

MR. RENAUD: Objection.

A My definition of stable, which might be different than other people's, is that it is when, when you start a project, there are going to be a lot of

changes as designers implement new features, and so that process eventually stabilizes, and the code -- basically, once you have one tri test passing, which is the test that can run both vertex and pixels through the shader and the whole chip, we have a way to guarantee that any new RTL changes will not break the database.

Typically, that milestone is the time where the RTL starts to get stable and you can start doing PD efforts and prototyping and all that because you have a way to test every submission of RTL.

Q Did you say first triangle test, or one triangle test?

A Yeah. I mean, can you --

Q For the reporter I wanted to -- I don't know that the reporter got it, that's why I'm asking you what you said.

MR. RENAUD: Do you want to read the question and the answer back?

A Yeah, why don't you do that.

Q Well, let me ask you this: Can you recall a second ago saying that the RTL code is stable once a test is passed?

MR. RENAUD: Objection.

A So I said that the RTL code gets stable when -- and I don't remember if I called it first tri or one tri, but there is this one test which is a single triangle that we tried to run first, and that establishes proof of life, and once that test gets working, we keep it working, and we make sure that all the designers have to run it after they make any change to make sure they did not break anything. And so, you know, I think in this -- where is it.

Q Are you looking at your declaration?

A I am looking at Exhibit No. 6, page 30, where you have an example of that first triangle. And in this particular declaration, it is labeled that, for the successful first triangle. This is what I am referring to.

Q Just make sure I heard you correctly and the court reporter got it too. First triangle, not first try? Or does it mean the same thing?

A First tri is a contraction of first triangle. So when we -- when I said first tri, I meant first triangle, and it's just a contraction.

Q Which is fine, but you understand, just for purposes of the records, that's why I'm asking you to clarify to make sure your testimony is

accurate.

A Okay.

Q So earlier you were referring to the first triangle test that's on page 30 of Exhibit 6, is that right?

A That is correct. Yes.

Q And what type of work is done on the RTL after it's stable?

A So the first triangle test establishes what we call a proof of life, meaning that the hardware can operate from top to bottom on what it's supposed to do, but as you can imagine, to have a commercial product, you need to test all the sub features and, you know, various instructions and what not that might not be needed for first triangle.

So from that point on, all the work that goes through is really to verify and complete all the sub feature work to make sure you have a commercial product, and there's also performance testing that comes along after that point.

Q How is performance testing done on the RTL?

MR. RENAUD: Objection.

A So on the R400 project, what we have is the set of tests, and we measure the number of clocks it

takes to process, you know, a triangle, two triangles, 10 triangles and what not, and knowing the through-put that the chip is capable of, let's say that the chip can do four pixels per clock, I'm making up a configuration, then we make sure that if you have a triangle that is 10,000 pixels, then the chip does not take more than 10,000 divided by four, that kind of performance testing.

Q And is that kind of testing done on an IKOS machine, or is it done on the C sim, or is it done on, I think you said VCS simulator for the RTL?

MR. RENAUD: Objection.

A What we did for the R400, that type of testing on that project occurred on the VCS simulator because this is representation of the hardware. It did not occur on the IKOS machine as far as I know, which was more used for software bringing up purposes, and it can also -- it cannot really occur on the C sim because the C sim is a functional model. It doesn't have a good understanding of the clocks.

Q Okay. Let's go off the record.

VIDEO OPERATOR: The time is 12:27 p.m. This concludes tape two. Off the record.

(Lunch recess taken.)

VIDEO OPERATOR: The time is 1:11 p.m. This is the beginning of tape three. We are back on the record.

A Before you ask a question, do you want me to go on the record? I went downstairs and did find the name of the person that I talked to over the phone for the IKOS, and his name is Ron White, and both he and Colin Stuart are SMTS's. You asked me for their titles so I went and looked it up.

Q What's SMTS?

A SMTS is senior member of technical staff.

Q Do they work for AMD or ATI?

A They now work for AMD and they are employed by the Toronto office, so they must have -- their work employment is probably through ATI Technologies ULC as well.

Q And you mentioned Mr. Christie as well earlier?

A David Christie, yeah.

That was the other conversation I had.

Q And those are the only three people you've talked to, to prepare for today, is that correct?

A Along with Pam Horn, but yes, this is my recollection, correct.

Q Earlier there were some people you couldn't remember their names. I just want to make sure

we're done with the sort of list of people you can't remember. So are those the three people that you spoke with, other than counsel and Pam Horn, to prepare for your deposition today?

A As best as I can remember, this is correct.

Q Okay. And during the break, your counsel located some errata sheets I presume from you, is that correct, with regard to your prior depositions?

A Yes, I did provide two errata sheets for my previous two depositions.

Q And so I believe they were just Bates stamped and produced right now, so to put them into the record, we will mark them as Exhibit 7 and Exhibit 8.

(Documents marked Exhibit 7 and Exhibit 8 for identification.)

MR. ELENGOLD: For purposes of the record, Exhibit 7 is Bates stamped AMD1044_0252730 through 733, and Exhibit No. 8 is Bates stamped AMD1044_0252728 through 729.

Q Starting with Exhibit 7, Mr. Lefebvre, have you seen this before?

A Yes.

Q What is Exhibit 7?

A As best I can tell, this is the errata list that I

provided after my first deposition on November 13, 2015.

Q And did you just provide this to your counsel during the lunch break?

A I signed and provided that errata to the counsel that did the -- that helped me with this testimony, but counsel came with -- I don't know who gave them to him.

Q So putting aside that you gave this to your counsel in that case back in 2015, did you just provide it to your counsel in this case during the lunch break?

A No. I did not.

Q Okay. Other than this errata sheet for your deposition, which I believe, and let me make sure I get it clear for the record, is Exhibit 4, other than this errata sheet, are there any other corrections or changes you would want to make to Exhibit 4 to make it complete and accurate testimony?

A Not that I'm aware of.

Q Okay. And what is Exhibit -- sorry, strike that. Mr. Lefebvre, have you seen Exhibit 8 before?

A Yes.

Q What is Exhibit 8?

A Best I can tell, this is the errata sheet for the deposition that I did on December 9, 2016.

Q And did you just provide this errata sheet to your counsel that's sitting here today during the lunch break?

A No, I did not.

Q Other than the errata sheet in Exhibit 8, are there any other changes, corrections or additions to your testimony in Exhibit 5 that you would want to make in order to make it a complete, true and accurate set of testimony?

A Not that I'm aware of.

Q Okay. And before the break for lunch, we were talking about the first triangle test. Do you recall that?

A Yes. Let me bring back the relevant document to make sure.

Okay. I brought back Exhibit 6 and I'm now at page 30.

Q Is the first triangle test an industry standard test for graphics processing?

MR. RENAUD: Objection.

A I can't speak about the industry. I mean I've only been employed through AMD, but I can tell you that this is a very standard process at AMD, and

even to this day we still do it. That is still the test we use. I mean, obviously, we changed it slightly to adapt to the newer chips which need more pixel, but still the same concept.

Q What's involved in the first triangle test from an actual emulation perspective?

A Can you refine what you mean by emulation?

Q Sure.

A You talking about the C sim or the RTL?

Q Which is the first triangle test performed on, the C sim or the RTL?

A Okay. So in R400 and other chips that I worked on, this test is first performed on the C sim to bring up the reference model to a level to which it is able to support the RTL development, and then we run the test on both the RTL and VCS and the C sim, compare the output image to make sure they match.

Q Is the first triangle test also run on the IKOS machine?

A Nothing precludes it from being run. I don't know if it was run, but certainly, if it can work on the RTL, it should also work on the IKOS machine.

Q But it's not part of the standard. I believe you suggested it was sort of the standard procedure

every time a change is made with regard to the RTL; is that true, to then run the first triangle test again?

MR. RENAUD: Objection.

A So it is standard procedures for the developers and the architects to run this test prior to making any changes to the RTL; however, the thing that is being applied to the IKOS prototype is a netlist, and that doesn't get refreshed on every change list. It only gets refreshed at fixed periods.

Q How many netlists were there for the R400?

MR. RENAUD: Objection.

A At least three, given that we have a netlist number three. There is evidence that there were more, but I can't tell you conclusively how many iterations that project went through so --

Q Approximately how many? Earlier you mentioned there were a bunch that didn't have correct naming, and some that did have correct naming? Are we talking dozens, hundreds?

MR. RENAUD: Objection.

A I've seen evidence of up to, you know, maybe eight or nine but without deeper search, I can't give you a better answer than that.

Q Am I correct that it's not standard procedure to run the first triangle test every time there is a new netlist?

A So given that we run the one triangle test on the VCS emulator, which is the RTL, the netlist is a reflection of that. So if the one triangle test work on the RTL simulation, then we have a tool that performs an equivalence test between the netlist and the RTL. It's not truly needed to run the one triangle test on the netlist because they are the same and it works on the RTL.

Q If the netlist matches with the frozen set of RTL, correct?

MR. RENAUD: Objection.

A That is the correct assumption, yes.

Q Otherwise, you wouldn't know for sure whether it would work.

MR. RENAUD: Objection.

A I don't know how the netlist would not match to the RTL, but you know, when we freeze the RTL, it is typical policy to make sure that the frozen set of RTL files work as intended on RTL, and that would be the first test that would be run, so.

Q Right. I believe earlier you said that Netlist 3 at least was made up of portions of different sets

of RTL over time, correct?

A Correct. So the -- we are -- the process is that we freeze files block by block into a branch, and every time new sets of code is ported to that branch, regressions are being run, and at least this test is being run.

So while it is fair to say that a netlist is a collection of multiple sets of RTL, I have every reason to believe that whatever set was used was regressed against at least this test and potentially many more.

Q Do you know that for sure?

MR. RENAUD: Objection.

A It has been so long ago I can't conclusively say, but this is general policy so I have no reason to believe it not to be.

Q Do you know of any documents to show that it was performed?

A It could have been in the program reviews that you have documents for. I'm not a hundred percent positive. Most of these regression results unfortunately are usually kept on servers and not in a Perforce depot, so some of the information is probably lost.

MR. ELENGOLD: I'm going to ask the court

reporter to please mark Exhibit 9.

(Document marked Exhibit 9 for identification.)

MR. ELENGOLD: For the record, Exhibit 9 is Bates labeled AMD1044_0175191 through 196.

Q Mr. Lefebvre, have you seen Exhibit 9 before?

A Yes, I have.

Q What is Exhibit 9?

A This is a presentation by Peter Pellerite that occurred on August 30, 2002, and I am reading from the presentation to say that, that is called the R400 August Program Review, which also incidentally happened to be an Exhibit for my previous depositions.

Q Is this the program review you were just referring to?

A This is one of such presentations, yes.

Q Do you know if there's others that exist?

A Yes, there are others that exist.

Q What other program review summaries are you aware of for the R400?

A I don't recall the specifics but I know, I mean at least in the preparation there were several other program reviews, and these program reviews are typically held at regular time intervals. This

one is August. I'm expecting there's going to be others earlier, later.

Q Do you recall any that you've looked at that -- in preparing for today's deposition, other than the August?

A I recall reviewing other presentations, yes, where probably would have been a later one because the actual column on page Bates number AMD1044_0175196 had a more complete actual description.

Q Is the IKOS emulation start what you were referring to with regard to the FPGA and IKOS machine?

MR. RENAUD: Objection.

A The IKOS simulation start is, yes, the process by which we are starting prototyping, if you will, the netlist on the IKOS machine.

Q And when, to your knowledge, do you know when that occurred, that prototyping or emulation occurred?

A Like I said before, there's a very similar program review presentation that has a lot more actual dates, and that would state the record properly. I think, if my memory serves, that it occurred slightly after the plan date, but you know, we can find for sure because that information is readily available.

Q But you don't know yourself?
MR. RENAUD: Objection.
Q You're just saying you have to look at a document to tell you, is that correct?
A I said I don't remember. Correct.
Q What does "begin early block delivery" mean?
A Begin early block delivery?
Q It's right under "IKOS emulation start."
A Yeah. I believe this has to deal with initial efforts to deliver blocks to physical design, so through the PD team, so they can start as early as possible the floor plan effort, so that when they get the later blocks, they can focus their effort on those.
Q Then what is an IKOS emulation with software?
A This is exactly the topic that we broached on a little bit earlier where I said the hardware emulator would be running with the software infrastructure. This is what this line refers to.
Q The RTL freeze/Final Netlist, what does that step represent?
A In the R400, as with many other silicon devices, at some point you have to freeze the design in order to submit the GDS or the netlist to the manufacturing process. So this date is the date

by which we were intending to freeze the design completely for fabrication.

Q What is "base layers tapeout"?

A Silicon chip contains several layers. The first layer is the silicon layer in which the gates are etched in, and then it follows by several metal layers, which are the wires that connect the gates together.

So that base layer tapeout is taping out that baseline, the first layer of where the gates are etched, and then the metal layers are the subsequent layers that you lie on top of that base layer to establish the connections.

Q What is the "First Samples for Engineering" step?

A This, again, in the R400 concept is when we expect to get the first chips back from the manufacturer.

Q How many samples are usually returned for engineering purposes?

MR. RENAUD: Objection.

A I don't recall the number specifically for the R400, but you know, for product like we would do today, we just do a few wafers, which would be, I don't know, around a thousand chips or so. I mean, that vicinity. We're not talking millions of parts. It's really a small number of parts.

Q Then what occurs between the first Samples of Engineering and the A12 Tapeout?

A So the samples are going to go to the software team for what the process we call bring-up, which is, you know, starting to run applications on the chip. Sometimes you have issues and, you know, small problems that you have to reconnect the gates differently. This is what we call an ECO or an A12. It's just a -- so A12 means it's -- a metal mask is just released. So you don't change the base layer, just one of the metal layers, which is a much faster turnaround time to fix any possible issues that one might have encountered in one application.

Q And then is that same sort of thing done with the A12 samples for engineering, are they then also tested for minor or other problems?

A So in this R400 concept, the A12 Samples for Engineering is really -- so we were -- this program was planning for one -- was expecting or planning for one metal layer in the schedule, and so this is just testing again to make sure the chip works before the production is, you know, enlarged to millions and millions of parts, at which point you can't fix anything anymore.

Q So far in this program schedule, did the R400 program make it before it was ended?

MR. RENAUD: Objection.

Q I remember the -- my memory recalls that the R400 was never really taped out because at some point in time, this transitioned into the Xenos program. So I believe it ended in between IKOS simulation and RTL freeze. It didn't make any more progress than that.

Q What is the Xenos program?

A The Xenos program is a program that ATI initiated with Microsoft to provide the graphics core for the X box 360 console.

Q Do you know if the R400 ever started the tapeout process?

MR. RENAUD: Objection.

A To the best of on my knowledge, and the documents I've reviewed, I could not see any evidence that it ever did start the tapeout process.

Q At what point did you stop working on the R400 program?

MR. RENAUD: Objection.

A That's another question I already answered in my previous depositions, but my memory is fairly vague on this because the transition for my block

was very transparent. It's really the same kind of product. So I don't exactly recall when I stopped working on one and started working on the other because they're one, one and the same kind of blur in my memory.

Q Is it approximately fall 2002, based on these dates?

A These dates are stating, like, the back end blocks, the back end efforts, or the PD efforts which I'm not really involved in. I can't tell from this when the front end designers and architect would have transitioned from one program to the other. I mean --

Q So it could have been before August 2002, is that right?

A Could have been before August -- so August 2002, that was the first synthesis date, is that the point you're referring to or?

Q Well, that's when this is from, right?

The program schedule is dated August 2002, I believe --

A So --

Q -- according to your testimony?

A So at the time of this presentation, because people were still, you know, inactive, this is the

first synthesis, so it's still undergoing active RTL development. So I have every belief that at that time, I probably would still have been involved in the R400 program itself. Maybe the Xenos program also started, but there would still be work on the R400 at that time.

Q Was there overlap between the R400 program and the Xenos program?

A To the best of my memory, yes, there was, and so that's why it contributed to making it even more of a blur.

Q What kind of overlap?

A So at AMD, we use Perforce server and depositories, so the depositories are directories, and you can integrate files from one depot to the other. Typically, a depository has the name of a given project, and so you can start working on the Xenos program and then start back integrating changes as you see fit to the R400 and back and forth. It's like, it kind to working with two different directories.

Q Are you talking about changes to specifications, or changes to C code, or changes to RTL, or all of the above?

A Any kind of changes can be back integrated, but

any binary files -- like unfortunately, our specifications are binary because they're Word documents. These -- you can copy them from one depot to the next, but you cannot integrate them. And by "integrate," I mean when you have code, the Perforce tool itself is intelligent enough to find exactly what change between the two files and merge them into one file, where you can't do that with binary files.

Q Does that work for both C code and for RTL code, in Perforce?

A Yes, it does. It works with anything that is not binary.

Q What is the difference between the R400 program and the Xenos program?

A The R400 program was meant to be a PC GPU, meant to operate on Windows; whereas, the Xenos program is, was meant to be a console program. So a specific piece of silicon delivered to a customer with some specific features potentially to be used in a console.

Q Why didn't it have an R500 or R600 name?

A The Xenos program you mean?

Q Yes.

A At AMD, we tried to distinguish the semi-custom

programs versus the GPUs so that people know what they are working on. Typically, the -- our names, at the time, we reserved for our GPU line of products, our PC products, whereas, whenever you had a -- an SCBU program, or a dedicated piece of silicon for, dedicated for a specific customer, it would have a program name to obfuscate also who the customer might have been.

Q Xenos was specifically being designed for Microsoft, is that right?

MR. RENAUD: Objection.

A The Xenos chip was specifically designed for Microsoft, but the RTL, at least during the overlap, was -- at least a portion of the RTL for the graphics core existed on both the R400 and Xenos program, as was very similar if not the same in some respect.

MR. RENAUD: Just so the record is clear, the Xenos subject matter, you're testifying in your personal capacity.

MR. ELENGOLD: Okay.

So this witness is only testifying on the R400 on behalf of AMD and ATI.

MR. RENAUD: No, he's testifying consistent with the subjects, but I don't believe the Xenos

is within to the scope of the subject matters. Do you have a different point of view on that?

MR. ELENGOLD: I don't know. That's why I'm trying to clarify your objection --

(Court reporter interruption of overlapping colloquy)

MR. ELENGOLD: -- trying to understand where you're trying to draw the line with your objection so I make sure it's clear for the record.

MR. RENAUD: My memory is, the Xenos is outside the scope, but I would be happy to go back and take a second look at it during a break.

MR. ELENGOLD: It's up to you.

Q For now, we're going to treat this testimony as personal testimony, just for yourself, as far as your recollection regarding Xenos.

So I think the last question -- I'm sorry, I think we got a little derailed there, was just regarding whether or not this was specifically designed for Microsoft, and I believe you said the chip was specifically designed for Microsoft, is that correct?

A So if I remember correctly my statement, I said that the Xenos chip itself was a product specifically designed for Microsoft, but then a lot of the graphics blocks and infrastructures, at

least during the time of the overlap, were the same or very similar between the R400 and the Xenos program.

Q Was the Xenos chip a graphics chip?

MR. RENAUD: Objection.

A The Xenos chip was a dedicated graphics chip. It was not a PC product, but it was able to perform graphics functions.

Q It wasn't an APU or an SOC.

MR. RENAUD: Objection.

A I mean, I believe, I believe at the time it was a graphics processor, stand-alone graphics processor, but it's kind of fuzzy. I only worked on the graphics subsection of it, so I don't even remember if we made it an APU or not.

Q What is the period of overlap you're referring to for the R400 and the Xenos chip?

A So we should really go back down -- I don't know if it's readily available or not, but in Perforce, we have all the dates. So I remember it being an overlap because I remember when I was searching for, you know, documents, that there were integrations back and forth between R400 and Xenos. I can't really tell you how long that period of overlap took, but I know there was some

overlap.

Q And at some point, everyone stopped working on the R400 program and either were working on Xenos or other projects at ATI, is that correct?

A So at some point, yeah, the R400 program got cancelled, and so everyone who was working on R400 at the time transitioned to Xenos and possibly some other program. I mean -- but --

Q Did everybody transition to Xenos, is that correct?

A Are you asking me --

MR. RENAUD: Objection.

A -- everyone at AMD transitioned?

Q Well, I think you just said, at some point everyone stopped working on the R400 program and were either working on Xenos and possibly other projects at ATI. I just wanted to make sure I understood your testimony for both of us to make sure it's accurate.

So was everyone that was working on R400 project when it was cancelled, transitioned to the Xenos program?

A Yeah, when I meant everyone, I didn't mean everyone at ATI because there were another team working on the R300. That team never worked on

the R400 or the Xenos program.

But once we transitioned to the Xenos program, and the project got, the R400 project got cancelled, I can't say for sure if everyone that was working on the R400 transitioned to the Xenos program, but my recollection is that at least most of the people transitioned over.

Q Was there an R500 program?

A Again, to the best of my recollection, the R500 program was a derivative from the R300, so the team that was working on the R500 was actually the R300 team.

Q What was the next computer chip -- sorry, strike that. What was the next general purpose computer chip program to follow the R400?

MR. RENAUD: Objection.

A So to the best of my knowledge, that would have been the R600, also known as Pele.

Q P E L E?

A Like the football person, yes. P E L E, yes.

I think it has an accent, but let's not get picky.

Q Approximately, when did the R600 program start?

A I really don't recall. I mean after the R500 and then the Xenos program, and there could also be,

have been overlap because I'm sure some integration occurred.

Q That was going to be my next question, is whether the Xenos program overlapped with the R600 to your knowledge.

A It may have. You know, again, we can check the Perforce log. I think that would really be the conclusive proof of, if any overlap occurred, and what kind of data bled from one project to the next, but I can't answer these questions from memory. It's just too far back.

Q Do you know what blocks reported from the R400 program to the Xenos program?

A To the best of my knowledge, again speaking from memory here, it was pretty much all the blocks except the render back ends, which are the blocks that take the output of the pixel shader. And the reason for that was that the Xenos program had a dedicated memory on board for the frame buffer which necessitated custom-made render back ends.

Q What is the output of the pixel shader that goes into the render back end?

MR. RENAUD: Objection.

A So in most cases, the output of the pixel shader is the color elements that you want each pixel to

have. We now have capabilities to also export the Z values and what not. I don't recall, and again I can look it up in the specification if you give them to me, but there can be more than just a color, but it is at least the color information.

Q What's a Z value?

A As you render primitives into 3D space, the Z value is the third coordinate, if you will, that will say if a triangle is on top of one another or not. So it's used to compute occlusions between primitives.

Q And you said the Xenos chip had a dedicated memory for the frame buffer, is that correct?

MR. RENAUD: Objection.

A So as best I can recall, again, the Xenos had a big onboard memory to use as the frame buffer, and the RBs were directly connected to that memory, and as such, did not need a cache because they did not need to hide the latency going to actual system memory and what not, could operate directly from that dedicated memory, and that's why they needed to be custom made.

Q So it didn't need a cache because the memory was on board, is that right?

A The Xenos program did not need a cache because it

did not need to amplify or hide the latency because the memory was on board, super low latency, and very high bandwidth, so you could operate right off that memory instead of having to use a cache to amplify the internal traffic versus the external traffic to memory.

Q What's the difference between a cache and a memory?

MR. RENAUD: Objection.

A A cache -- and again, this is my definition of the term -- is a structure that is very often used in GPUs to amplify the bandwidth by storing temporal data that is also in memory, so that if multiple blocks or customer of the chip want to access the same data, it's going to be able to provide that data to all of these customers without having to go to the main memory to retrieve it all the time.

Q So it's a way to access the memory? Temporarily store certain things closer for faster access?

A Again, it is a way to amplify the memory bandwidth so to satisfy more customer than the bandwidth provided by a memory device would be allowed to provide.

So let's say you need, you know, 10 gigabytes of bandwidth to provide a task, and your

memory is only five gigabytes because of the bus width and so forth, you need a cache to amplify that so that in most cases, the clients that need 10 gigabytes of bandwidth can operate inside the chip without having to always use the small narrow bus going to system memory or D rams onboard.

Q Are there any other differences between the R400 and the Xenos chip that you recall?

A Without going into specifics that I can't divulge because of customer relationships, I mean proprietary information from Microsoft, the only other difference that I can remember is that Xenos had a slightly different configuration than the R400 program.

Q So we're under a protective order in this case which keeps things confidential, so I believe you can speak freely to the extent that you want to testify to this issue on behalf of AMD or ATI.

MR. RENAUD: We may need to take a break on that. Let me just see if I can solve it quickly, counsel.

Is this something, Laurent, that you think you need specific permission from Microsoft to disclose that we don't have?

A So this subject matter came up in one of my

previous testimonies and we had this issue where I would -- I was not able to divulge Microsoft proprietary information, and so we can read the transcript. I mean, I sent most of the information in that. I mean, it's really just a configuration difference between the two chips, and last time I could not tell you what the Xenos configuration was because of these protective, or I don't know how you call them in English. I can't tell you how many pixels the Xenos can process per clock, but I can tell you, it is a different number than on the R400, but my understanding is everything else is the same.

Q How much additional work was done on the Xenos chip from when the integration started from the R400 into the Xenos chip becoming commercialized?

A How much work?

Q Let me rephrase that. How much time did it take to make the Xenos chip into a customer-ready chip?

MR. RENAUD: Objection.

Q From when the R400 program was ported over.

A Is your question pertaining to the Xenos chip as a whole or on the shader section?

Q Let's start with the Xenos chip as a whole.

A So on the Xenos chip as a whole, like I said, most

of the work had to deal with the render back ends which were brand new pieces of hardware. I don't recall exactly how long they took, but that was the bulk of the effort. Everything else kind of followed right through.

Q Were any changes required to the other hardware blocks?

MR. RENAUD: Objection.

A Because the configuration was different, we had to tweak a few parameters, but I don't recall the extent of any of the changes, but you know, I can tell you that the two chips are very similar, and the only main difference that I can remember, again, is the render back ends and then the configuration to change a number of pixels.

Q So you're not sure of any other differences that might exist? That's not something you prepared for, for today's deposition?

MR. RENAUD: Objection.

A I did not prepare, you know, or review the Xenos program extensively. So no, I'm not -- I don't remember any other changes.

Q Did you review any Xenos documents in preparing for today's deposition?

MR. RENAUD: Objection. Let me make one

clarification just because I refreshed my memory. Xenos is outside the scope for any domestic industry stuff, but to the extent it's within the reduction of practice, it would be within the scope, so.

MR. ELENGOLD: I don't think it is. Well, I don't know, you said it's not, so I don't want to put words in your mouth.

MR. RENAUD: But I just looked at a record here that says the scope objection was to the extent it was related to domestic industry since we're not relying on it, but that to the extent it was related to reduction of practice, it is. So whether that makes sense to you or not, I just wanted to make sure I wasn't leaving you ambiguous.

So the questions about the Xenos, to the extent they reflect the reduction of the practice, he will be the designee, but he's not going to be a designee as to domestic industry use.

MR. ELENGOLD: Okay. So all of our questions then with respect to Xenos, and then we might have to go back, I apologize, now to revisit those if you are being designated, questions with respect to Xenos to the extent it's relevant to

production or not reduction to practice --

MR. RENAUD: He will be the designee.

MR. ELENGOLD: -- you're saying he is designated, right?

MR. RENAUD: And apologies for the ambiguity.

Sorry. Do you want to read the question back?

MR. ELENGOLD: No, I can ask the question. Thank you.

Q Did you review any Xenos documents in preparing for your deposition today?

A I recall there was this source code computer that counsel had, and there were some files of Xenos on there. I browsed through them. That's the extent of it.

Q Do you know when the Xenos program passed the first triangle test for the first time?

A I don't recall that information. I mean we can -- if you have Xenos specific documents with you, we can review them, but unfortunately, I don't know.

Q Do you know if it passed it?

MR. RENAUD: Objection.

A So the Xenos was made into a commercial program, and so it's in millions of consoles, or was at

least, so yes, I have a very good feeling that it passed it.

Q Do you know when the Xenos chip went into IKOS emulation?

A No, I do not know.

Q Do you know if it did?

A No, I don't.

Q Do you know when the tapeout was for the IKOS chip?

A There is no tapeout.

Q Sorry, strike that. I apologize. I said it wrong. Do you know when the tapeout was for the Xenos chip?

A Okay. Again, having not reviewed anything, I can talk from memory. I recall it vaguely being around 2004, but this is very vague.

Q Do you know when the first products were delivered to customers for the Xenos chip?

A No, I don't recall any specific dates, no.

Q So turning back to the first triangle test that we were discussing earlier, which you're free to reference either the presentation in Exhibit 9 or your declaration, which I believe is Exhibit 6, how was the first triangle test performed?

A On the R400, you mean how this test is being run?

Q I assume it's the same for all of the programs since you said it's sort of part of standard for ATI.

A Okay. Yes. So the base process by which we run functional test on hardware at AMD, and at the time on the R400, was that we create, like, a low level API which allows us to write small C programs that describe the test and what it's supposed to do, and by such, energize the hardware in a similar manner of which it would have been stimulated by the driver.

I know, you know, again, upon my review to prepare for this deposition, that in the source computer, there is the source code for such a test, which we can walk through so you can get appreciation of exactly what is being driven to the hardware, but effectively, it is a small C program that describes what you want the test to do.

Q Is it a static image of the triangle? Is it a single picture?

A In this particular case, it is a single picture of a triangle, yes. The test is render, triangle, and terminate. Finish.

Q I believe in your declaration, you said it's a

Gouraud shaded triangle, is that correct?

MR. RENAUD: Objection.

A It is a Gouraud shaded triangle, yes.

Q I thought maybe counsel was objecting to my pronunciation on that one.

What is Gouraud shading?

A So a Gouraud shaded triangle is a triangle that has three different colors for each of the vertices of the triangle. So in this case, if you had a color picture for this triangle, one of the vertex, which is one of the extremities of the triangle, would be blue, the other one would be red, and the third one would be green, and then the inside of the triangle varies slowly from one color to the next, and it is to ensure that the interpolation structure that determines the color for each of the pixels within the triangle is working effectively.

Q Is it just one set of vertices that are used for the test?

A For this test because it was one triangle, it is, yes. It's three vertices and one primitive, which we call the triangle.

Q And how many pixels are used?

A If your picture was better, we could count them,

but the pixels in this case are the big squares that you see here. It's not a very big triangle.

Q The picture is a little better here. This is how it gets produced to us, so I apologize.

A It is hard to see, especially at the top, but you can see these big squares are the pixels, so I mean, there are one, two, three, four, five, six, seven, eight, nine, 10, 11; 11 by 11 divided by two.

Q So to draw the triangle in the triangle test, you would make sure all the vertices shaded correctly, and then you would rosterize the pixels and make sure the pixels are shaded correctly, is that correct?

MR. RENAUD: Objection.

A So the way the API works is that the test sends the three vertices and the connectivity information, say, by this vertex connected to this one and to this one to form the triangle. The hardware does the rest.

So the hardware makes sure that the vertices are first passed through the shader, operates the right positions, as well as the attributes, which are the color in this case, and then subsequently runs the pixel shader on those attributes.

Q Okay. We'll come back to that. I wanted to turn to talking about the R400 specification that you've been mentioning. I don't know, would you like to take a short break now before we transition topics?

MR. RENAUD: My thought is maybe we go another 15 or 20, if that's comfortable for you. I think it ensures that we'll keep tracking toward getting a full seven hours.

A I'm fine. We can do another 15, 20. I'll let you know if it changes.

Q Okay. Thank you. Give us as much warning as we can and we'll wrap it up.

So earlier you mentioned, a couple times I believe, sequencer specification, is that correct?

A I believe I did, yes.

MR. ELENGOLD: I'd ask the court reporter mark Exhibit 10.

(Document marked Exhibit 10 for identification.)

Q Mr. Lefebvre, have you seen Exhibit 10 before?

A Yes, I have seen it. This appears to be the R400 Specification Version 0.4.

Q Is this the R400 Sequencer Specification you were referring to earlier?

A In fact, I was hoping to get Version 2.0, which had the control flow structures, to answer any of your questions about the control flow, but this is one version of the sequencer, yes.

Q I think I have that one too and I'll bring that out next, but I wanted to ask you a couple questions about this first.

So do you remember approximately the date of when this document was completed in the current form that it is in Exhibit 10?

MR. RENAUD: Objection.

A So the date, I have no reason to believe that it would be wrong. This document, by myself, if you look at the revision changes on page 3 of 20, or Bates number AMD1044_0175218, it's dated by myself, or what appears to be me, on August 24, 2001.

Q Do you recall making that entry in this document?

A I don't recall directly having made that entry, but I have no reason to believe that it's incorrect. I mean --

Q Do you know why the Edit Date on the document says September 4, 2015?

A I don't know why, but I can tell you that these fields up there are usually automatic fields, and

so this Edit Date is going to be changed whenever anyone opens the document to read it or what not.

So I suspect somebody read this document and either formatted it to include, you know, revision change control which wasn't there before or not. I can only assume that's what it is.

Q Is that the same for the date in the bottom right-hand corner on the front of Exhibit 10, that that auto updates, to your knowledge?

A Yeah, it looks like that could also have been automatically generated.

Q Because it says September 4, 2015.

A Yeah, it matches, but yeah, so.

Q But you're not sure, with regard to this general structure of the document, whether or not the edit date, and the bottom right corner date, auto update or not?

MR. RENAUD: Objection.

A It looks like a new entry because it's not stricken like the other text, but conclusively to say to you, whether or not this actually was typed in or was auto generated -- we could -- if I had the electronic version of it, we could check in the electronic version if this is an automated field or not. From a paper, I can't tell you

conclusively.

Q You don't know how those dates got there, is that right?

MR. RENAUD: Objection.

A Well, I told you that I know that these dates here on page 3 of 20 are typed in. So these are typed in by the author, which just happens to be me. So I'm confident in these. How these on the first page got changed or not, yeah, I don't remember exactly what form we used at the time.

Q Did you create Exhibit 10?

MR. RENAUD: Objection.

A By "create," you mean did I write this specification?

Q Did you write Exhibit 10?

A I am the author, at least according to this document, of this specification, and this is also my recollection, yes.

Q Did anyone make edits to Exhibit 10 other than you, to your knowledge, other than the date field we're talking about?

MR. RENAUD: Objection.

A According to this log, which is on, again, page 3 of this Exhibit, I'm the sole contributor to this specification.

Q Did ATI have a policy regarding logging in the Revision Change section of specifications at the time that you edited Exhibit 10?

MR. RENAUD: Objection.

A I think AMD has a relatively loose policy on that. It's the responsibility of the author to make the entries. However, I will say that once the document is in Perforce, the Perforce server itself records the dates and the name of each and every person that interacts, writes any document, and so if you have the Perforce change list revisions for this file, it would be much more tangible and accurate than anything that would be present here.

Q Does the Perforce log file identify each change that was made within the document?

MR. RENAUD: Objection.

A In the case of a binary file, it does not because it's just -- it cannot, you know, do the merge and the comparison. But it's going to maintain all of the versions of every single file that was submitted to the depot, so having all the changes, you can manually do the comparisons, and for all of the source check-ins, C plus plus, or RTL, the Perforce does make the record.

Q So the management of the dates and the revision changes is left to the authors and may not be a hundred percent accurate, but the Perforce logs you believe are always maintained to be accurate, is that correct?

MR. RENAUD: Objection.

A That is my understanding, yes.

Q Do you know approximately the date of Exhibit 10?

A Well, like stated before, this is dated on the page 3 by myself as of August 24, 2001. No reason to believe it not to be accurate.

Q Is that because you, every time you made a change to a document, put a note in the Revision Change log?

MR. RENAUD: Objection.

A It is because I personally, whenever I change a revision number on the first page, try to put a revision change list in the Revision Changes. So I know I have not been a hundred percent accurate, and I could have made changes to this document without changing the rev number, but if I change the rev number, again, it's my recollection and my work practice, I would make an entry in the Revision Change.

Q So this could have some changes that occurred

after August 24, 2001 in this document, but any of those changes would have occurred prior to you creating Version .5, is that correct?

MR. RENAUD: Objection.

A That is a possibility, yes, and if we go to the Perforce log, we can say conclusively whether it is the case here or not.

Q Why did you create this document that's Exhibit 10?

A This document is the architecture document that is meant to describe the way the sequencer is supposed to operate in the R400 unified pixel and vertex shader.

Q Whose idea was it to put a sequencer in the R400 shader?

A Everyone, at least of the architecture team, knew that a sequencer was needed because you need, maybe not the name sequencer, but you need a module that controls the operation of the shader, and so, you know, I can't tell you -- I don't know that anyone had an idea to put a sequencer in the R400. The idea is how to make it work in that context.

Q Was the R400 the first ATI program to use a sequencer in a shader?

MR. RENAUD: Objection.

A To my knowledge, the R300 had a pixel shader sequencer, meaning the sequencer was only operative on the pixel shader side of things, and this is, to my knowledge, the first time ATI created a sequencer that able to operate on either or both pixels or vertices.

Q Do you know when the R300 sequencer was created?

MR. RENAUD: Objection.

A So your question is when it was created?

Q Do you know when?

A No, I don't know the date, I mean, and I recalled it being named into the overview, and so I just went to read back through it to see if there was any date, but there's no date. It just states that the sequencer is based on the R300 design, where we used it as a baseline and then modified it in order to operate in a unified vertex and pixel shader environment.

Q Is that a true statement, that the R400 sequencer is based on the R300 sequencer?

MR. RENAUD: Objection.

A This is what page 4 of 20 of this specification is stating. I mean, it is to the best of my knowledge, we use some concepts of the R300. We

use the clause concepts. But the R400 sequencer is still significantly different than the R300 sequencer. It has to deal with the two types of elements, which the R300 did not have to deal with, and I also know we upgraded it to have more clauses or more flexibility.

Q What are clauses?

A If you refer to the figure which is not named on page 5, or Bates number AMD1044_0175220, you have a Top Level Diagram of the Version 0.4 sequencer. The clauses are effectively the trips between the various reservation stations. So the more clause you have, the more opportunities you have to do what we call dependent fetches, which is go to memory, fetch an element, do some ALU map on them, and then do another fetch based on that, so forth.

Q Can each clause support one instruction?

MR. RENAUD: Objection.

A Each clause supports a number of instructions, but they have to be all of the same type; so either all textures or all ALU. Whenever you had to transition from an ALU to a texture or fetch operation, you had to go to a new clause.

Q What is the purpose of supporting ALU clauses and eight texture clauses?

A Like I just stated, it's to support what we call dependent fetches. So let's say in the first texture clause, you go to memory, you fetch a number, and you want to operate on that number on the ALU clause, and then use that number as an address to the next memory fetch you want to do. Having eight levels of clauses allows you to have eight levels of indirections. That gives you the opportunity to read memory, operate on it, and go back to memory and back and forth.

Q Why do you need eight levels, or I'm sorry, strike that.

What is a level of indirection?

MR. RENAUD: Objection.

A So a level of indirection, at least in the R400 concept, is a dependent fetch; like I said, a fetch to memory, an operation on the ALU, and then another fetch that is dependent on the result from the first fetch. That is one level of indirection.

So eight fetches gives you seven levels of indirections effectively.

Q So looking at the diagram you were just referring to on Bates 175220, what is the first block, the vertex/pixel vector arbitrator used for?

A So this block is meant to represent -- and by the way, in these specs, I would say that whenever you see arbitrator, you can treat it as arbiter. It's a remnant of my being French. And so this is the block that the sequencer is operating on to decide what is the next piece of data elements allowed into the shader; is it going to pick a group of vertices or a group of pixels?

Q And whose idea was it for -- sorry, strike that. Who came up with the idea to design the design of the pixel/vertex arbitrator that was used in the sequencer?

MR. RENAUD: Objection.

A Best as I can remember, that part was something we needed and, you know, the details I came up with effectively.

Q What did you come up with?

A On this version of the 0.4, I came up with this idea of having an input block that would decide between the two, and it went into various gyrations of the rules that we could put in that block, and in order to give you details about that, you know, I would need to go and check the code because I don't remember exactly what kind of code we had in place at the time of this

specification.

Q With regard to your coming about, just sort of the control structure here, on Bates number 175227, there is a section heading: 1.3 Control Graph. Do you see that?

A Yes, I see that picture.

Q What does that picture show?

A This picture, best I can tell, and again, this is a long time ago, it's the exploded view of all the various communication buses between the sequencer and the other units of the unified shader.

Q What does IS stand for?

A IS stands for instruction store. This is where the instructions that the shader -- the sequencer, sorry, is to execute for either pixels or vertices.

Q That's where they're stored, in the instruction store?

MR. RENAUD: Objection.

A That is where they are stored in the R400 program.

Q A what does SEQ stand for?

A SEQ is the acronym for the sequencer.

Q What is CST?

A CST in the R400 project stands for the constant, or the constant buffer. That's where the values

that are the same across a whole vector of pixels or vertices are stored.

Q What kind of values are stored in the constant store -- sorry, strike that. What kind of values would be the same across a series of vectors or pixels that would be stored in the constant store?

A So I'm going to give you one use-cases for this. It's by, not a long shot, the only use-case, but one of the use-case for this is so that software or the driver can use the same shader and apply it to two different conditions.

So you can use a constant to direct your control flow and skip over whole segments of code by just having one bit change in the constant, so that allows you to use the same shader and have completely different behaviors without having to resend over a whole new program to the GPU.

Q So it gains additional efficiencies during the execution?

MR. RENAUD: Objection.

Q Is that right?

A It's a gain of CPU power because you don't have to recompile all the time. It's a control that the driver likes to have so that it can be more nimble. It doesn't have to be. You can have a

sequencer without a constant store if you want it, but it's a nice tool in your tool box.

Q Could you have a sequencer without an instruction store?

MR. RENAUD: Objection.

A You can have a sequencer without an instruction store, yes.

Q How would that work?

MR. RENAUD: Objection.

A The way I would envision this to work is to have a sequencer coupled to system memory and it fetching the instructions as needed.

Q So it would be slow but it would work?

MR. RENAUD: Objection.

A It can be as fast as you want it to be because if you imagine instead, you have an instruction cache, then you can make it very fast and very flexible. It's a more complex design than having a buffer, an instruction store.

Q You could do a cache instead of a store, would be one way to do it?

MR. RENAUD: Objection.

A So like I said before, you can do a cache, you can do nothing at all and couple it to memory, you can do a store. There are many ways one can do it.

Q Could you have a sequencer without the vertex/pixel vector arbitrator block?

MR. RENAUD: Objection.

A Can you be more precise in your question because sequencer generically is very generic, so what is the scope of your question?

Q Sure, as far as I understand your R400 sequencer, the components included vertex/pixel vector arbitrator, and instruction store, and a constant store based on our discussion so far of this specification. Is that right?

A So the R400 sequencer included all of these modules, yes. You don't have to have all of these modules to have a unified shader. It's just an implementation of, and it just happened to have these blocks.

Q Are any of these necessary to have a unified shader?

MR. RENAUD: Objection.

A One could envision having a unified shader with, you know, for example, an instruction store dedicated to vertices, and instruction store dedicated to pixels, and then just shared resources on the GPRs which are the SPs. You can do any level of unification that you want. This

is just one example, one implementation.

Q You mean the sequencer is just one implementation, or this implementation of the sequencer is one implementation?

MR. RENAUD: Objection.

A The implementation here of the sequencer is the sequencer we used in the R400, and the R400 itself as a program is an implementation of what we call a unified shader.

Q What I'm trying to understand is what parts are necessary for, you know -- so strike that.

You understand that AMD and ATI are contending that there is an invention of a specific kind of unified shader that's embodied in your patent, is that correct?

MR. RENAUD: Objection.

A So I understand that there is contention, and again, I'm not a lawyer, so there is contention about the specifics of the unified shader. All I can tell you is from a technical point of view, I can tell you what can and cannot be a unified shader, and so all I've said so far, I believe, is that this particular R400 sequencer, and the R400 as a whole, is an implementation of the unified shader. It does not preclude other kinds of

designs.

Q And to that point, what I'm trying to understand is what is required in order to build a unified shader of what you claim you invented?

MR. RENAUD: Objection.

A Unified shader means unification of some degree, and so I think at a minimum, to have a unified shader, you would need to have unification of the most expensive part of the shader, which is the GPRs and the ALUs. The rest is not, not necessary. You can build it with or without it, but you would lose most of the benefits of the unified shader if you did not have a unified ALU coupled with GPRs.

Q What are GPRs?

A The GPRs are the general purpose registers. These are the small embedded memories that serve as source and destinations for ALU operations or fetches. They're the stored -- the data, the intermediate data as you run your shader.

Q Why are they called general purpose registers?

A Because they can store any data you want. They're generic memories that you can use as source or destination and they store any information you want to store.

Q So unification of GPRs and ALUs, you believe, is all that's required in order to have the unified shader that you believe was invented and as part of the R400 project, is that right?

MR. RENAUD: Objection.

A I believe that in order to get benefits great enough to go to the burden of unifying everything and, you know, have the area and savings, that is, you know, the one piece you need to have. Obviously, the more you add on top of that, the more you can maximize your savings, but you know, they're not strictly necessary.

MR. RENAUD: Good time for a break, counsel?

MR. ELENGOLD: Sure, let's take a break. Go off the record.

VIDEO OPERATOR: The time is 2:31 p.m. This is the end of tape 3. We are off the record.

(Off the record.)

VIDEO OPERATOR: The time is 12:51 p.m. This is the beginning of tape four. We are back on the record.

Q Mr. Lefebvre, before the break we were talking about Exhibit 10. Do you recall that?

A Yes.

Q And I'd like to turn to page 175232 which at the

top says: 13. Examples of program executions. What is this section of the document used for?

A This section of the spec, as best I can tell, in the R400 is meant to provide an example of an execution of a vertex shader program so that the designer can refer to it and understand with an example the kind of steps expected to be run when we are running an exemplary program on vertices.

Q Okay. In step 2 -- you see step 2? What does that say?

A Step 2 reads as follows, "SEQ arbitrates between the Pixel FIFO and the Vertex FIFO - basically the Vertex FIFO always has a priority. At this point, the vector is removed from the Vertex FIFO; the arbiter is not going to select a vector to be transformed if the parameter cache is full unless the pipe has nothing else to do (i.e. no pixels are in the pixel fifo)."

Q And is that the operation of the pixel/vertex arbiter block we were talking about earlier?

MR. RENAUD: Objection.

Q That's on page 220.

A You mean the R400 vertex/pixel arbiter -- arbitrator?

Q We can use the terms interchangeably, that's fine.

So yes. Yes, that's exactly. Is that the operation of that block?

MR. RENAUD: Objection.

A So in this R400 example, it would appear to be that the policy was to pick vertices; if there were space enough for vertices, else, picks pixels.

Q When you say "example," is that because the actual functioning of the arbiter hadn't been determined at the time of August 21, 2001 when you -- sorry, August 24, 2001 when you last think you edited this document?

MR. RENAUD: Objection.

A So this document states, and again, I quote, "Basically, the Vertex FIFO always has priority." That seems to infer that the arbitration rule or threshold was decided at that date, and it was decided that the vertices would have priority over pixels.

Q Do you recall when that rule was decided?

MR. RENAUD: Objection.

A I don't recall the specific dates, but from the date of the specification, that would have been, you know, making sure I'm stating the correct date, before or on August 24, 2001.

Q And is that how the arbitration occurred in the R400 as it progressed through revisions leading to the RTL?

MR. RENAUD: Objection.

A I don't recall the specifics of the arbitration rule in the R400 program. Like I said, there are multiple, multiple revisions of the SQ source code, and the input arbiter is one of the such source codes. So this likely was the initial rule. Whether or not it stuck to be the one rule after, you know, at the end of the program, I don't recall.

Q Do you know what the rule was in the RTL?

MR. RENAUD: Objection.

A I don't recall what it was, or whether or not there was RTL at the time of the specification or not, but again, this is something we can easily go look at if you're interested into that. It is in the source code, and all the revisions are tied so we can see any change that occurred.

Q Who was in charge of determining what arbitration scheme to use for the sequencer?

MR. RENAUD: Objection.

A I believe as the architect, I would be the one providing the initial assessment as to what I

thought the policy ought to be, and it could have been a concerted effort between all the architects, but you know, at some point, if you run a test and you realize it doesn't work as intended or anything, we could have changed it based on the results of that test too.

Q Do you know if there is any reason why you chose at this time to have vertex get priority?

MR. RENAUD: Objection.

A So I can't speak about what I may or may have not thought of at the time. I can give you an answer based on my current knowledge of graphics, if that's satisfactory in reading that document.

Q Okay. So you're not sure at the time why this was vertex. Based on your current knowledge, why would one prefer vertex as being the priority for arbitration?

MR. RENAUD: Objection.

A So what you want to do most of the time, unless you have the design that is very different, and that I don't know the intrinsics is, you don't want to have a bubble of latency between your vertex and pixel stages because that would infer slower performance because you have to wait.

So basically, in the R400, we wanted to

always make sure that the parameter cache, which is the storage for the attributes of the vertex shader, was always full or as full as possible, enabling the pixel flow to be as continuous as possible, and in that sense, have as good performance as possible.

Q Because vertices always have to get processed before pixels?

MR. RENAUD: Objection.

A In the R400 program, yes, that was the case. The vertices, since they are the input to the pixel flow, they had to be processed before the pixels.

Q When you say "in the R400 program," is that not the case for graphics processing in general, that you do your vertices before you do your pixels?

MR. RENAUD: Objection.

Q Sorry, strike that. Is it not the case in graphics processing in general that you shade your vertices before you shade your pixels?

MR. RENAUD: Objection.

A It is my understanding that in all the AMD products, that is the way we are doing it, and in some other products that I'm aware of in the literature, that is also the case, but I can't talk to everything that I may or may not know. I

mean, that is, in my opinion, a generic way of doing things, but if someone finds a way to do it otherwise.

Q Do you know of a way to do it otherwise?

MR. RENAUD: Objection.

A No. I basically cannot think of another way of doing it. That's the way I would have done it, vertices first.

MR. ELENGOLD: Going to ask the court reporter to please mark Exhibit 11.

(Document marked Exhibit 11 for identification.)

Q Mr. Lefebvre, have you seen Exhibit 11 before?

A I don't think I've seen this Exhibit, no.

Q Do you know what Exhibit 11 is?

MR. RENAUD: Objection.

A It reads, and I quote: The Complainants Notice of Patent Priority Dates, In the Matter of Certain Graphics Systems, Component Thereof, and Consumer Products Containing the Same.

Q I'm going to ask you to turn to page 2 and look at Section C. Can you read the title of Section c of this document?

A U.S. Patent No. 8,760,454.

Q Mr. Lefebvre, are you familiar with that patent

number?

A I have seen this patent number in the past. I believe this is one of the unified shader patents.

Q Do you understand you've been designated to testify today about the conception and reduction to practice regarding the patent 8,760,454?

MR. RENAUD: Objection.

A Yes.

Q If I call that the '454 patent moving forward, will you understand what I'm referring to? Is that okay?

A Yes. It would be even better if you had it so that, you know, we would know what exactly you're talking about.

Q I do have it. Do you not know what I'm talking about right now?

MR. RENAUD: Objection.

A I know it's one of the unified shader patent, but exactly what -- which one it was, I mean, I can't remember these patents by numbers only.

Q Okay. Sure. Can you look at Section D, please. Can you read section D.

A The title?

Q Yes.

A U.S. Patent No. 9,582,846.

Q Do you know what that patent number is?

MR. RENAUD: Objection.

A '846. Yeah. I think that's another one of these unified shader patents.

Q Do you know if you've been designated to testify today on complainants' behalf for conception and reduction to practice regarding that 9,582,846 patent?

A So the assignment for the -- sorry, the first notice of deposition says that I am assigned to testify on the reduction to practice to any alleged acts of diligence in reduction of practice of each of the asserted claims and asserted patents. However, not being a lawyer, I don't exactly remember which patents were asserted and which were not.

Q Okay, I'll ask the court reporter to please mark Exhibit 12.

('454 Patent marked Exhibit 12 for identification.)

Q Mr. Lefebvre, have you seen Exhibit 12 before?

While you're looking, I'll note for the record, it is AMD1044_0000165 through 176.

And I'm sorry, Mr. Lefebvre, have you seen Exhibit 12 before?

A Yes, I have.
Q What is Exhibit 12?
A This is the Graphics Processing Architecture Employing a Unified Shader patent, and I quote: Patent No. 8,760,454 B2.
Q And that's the patent we were just discussing with regard to Section C of Exhibit 11, is that correct?
A Well, the text says on Exhibit C that it's 8,760,454. This one is 454 B2, so without being a lawyer, I don't know if there's any difference between the two, but there seems to be at least two letters of mismatch.
Q Okay. Well, let's presume for the moment that the B2 is not important, and this is the patent I'll represent to you that was produced, as you see at the bottom, by AMD, as being a certified true copy of the patent, according to the front.

So with that clarification, do you understand this to be your patent that is listed in Section C of Exhibit 11?
A Yes. This is a patent for which I am one of the named inventors.
Q And do you understand that you're here today to testify on complainants' behalf about Exhibit 12,

this patent?

A Yes, my understanding is that I've been designated to testify about the facts pertaining to this patent.

Q Going forward, are you comfortable now if we refer to this as the '454 patent?

A Yes, I am comfortable.

MR. ELENGOLD: I will ask the court reporter to please mark Exhibit 13.

(Document marked Exhibit 13 for identification.)

MR. ELENGOLD: For the record, Exhibit 13 is AMD1044_0000177 through 195.

Q Mr. Lefebvre, have you seen Exhibit 13 before?

A Yes.

Q What is Exhibit 13?

A Exhibit 13 is or appears to be U.S. Patent 9,582,846 B2, title: Graphics Processing Architecture Employing a Unified Shader, for which I am a named inventor.

Oh, wait a minute. There is a typo in my town name, but.

Q So other than that, which I don't know how that got there, but does this otherwise appear to be correct with regards to the patent that we were

discussing earlier that's identified in Section D of Exhibit 11?

A Section B?

Q D.

A D. Yes. With the same caveat as before, that it has a B2 at the end, which this Section D does not.

Q If we refer to this as the '846 patent going forward, is that okay with you?

A That is okay with me, yes.

Q Okay. So turning back now to Exhibit 11, if you look at Section C, can you read the first full sentence on page 3 in that, beginning with, "The Asserted claims."

A "The asserted claims of the '454 Patent were conceived at least as early as August 24, 2001."

Q Mr. Lefebvre, do you understand that to be AMD and ATI's contention in this case?

MR. RENAUD: Objection.

A I am not a lawyer, so I don't even -- I can't interpret contention for you. I can read the English, and it says, "asserted claims of the '454 Patent," which appears to be this one, and "were conceived at least as early as August 24, 2001."

Q Do you agree with that statement?

MR. RENAUD: Objection.

A Agreeing with that statement in the sense of the law would mean interpreting the word "conceived," which I'm not an attorney. I'm an engineer. I can talk to the facts, and talk to the R400 and what it did at that date or did not do.

Q What did the R400 do as of that date?

MR. RENAUD: Objection.

A So in order to answer that conclusively, I guess I need to refer to some documentation because my memory is not clear enough to exactly pinpoint the single date in time. So let me see if this information is present.

There is a lot of paper here.

MR. RENAUD: And for purposes of scope, I believe that the parties agreed that contention based deposition topics under Rule 30(b)(6) were withdrawn, so to the extent that this question is intended to go beyond the scope, it would be my understanding it's outside the scope, but he can obviously proceed in his personal capacity.

MR. ELENGOLD: Okay. So you believe the question, "What did the R400 do as of that date," is outside of the scope?

MR. RENAUD: I believe that your entry

point, which was about the contentions of this document, are outside the scope on a question by question --

MR. ELENGOLD: So you're objecting to the prior questions.

MR. RENAUD: That's right. On a question by question basis, I think facts related to any contentions are fair game, although he may know one way or another whether they support or don't support contentions.

MR. ELENGOLD: Are you objecting to the question, "What did the R400 do as of August 24, 2001"?

MR. RENAUD: To the extent you're relating it to the contentions, I am. To the extent it's standing alone, I'm not.

A Okay. So the August 24, 2001 is a date that is after the date of this specification here, Exhibit 10, that says -- well, actually, it's the date of that specification. So if by "conception," you mean writing the specification of the sequencer that describes how the R400 unified shader works, then yes, I agree with this statement.

Q So I think my question was, just so we're clear for the record, because I'm not sure you answered

my question at all, my question said, "What did the R400 do as of August 24, 2001."

MR. RENAUD: Objection.

A Okay. I don't recall what the actual R400 did at that time. The one thing that I can point to is the fact that the specification, which I wrote, was available on that date and described the functioning of the sequencer or -- of the R400.

Q Do you know if that specification by itself supports conception of the claims of the '454 patent on August 24, 2001?

MR. RENAUD: Objection.

A I am not a patent attorney, again. I don't have any law background. I can attest to the facts, and the facts are that the specification existed at that date according to the entries in the file.

Q Are you aware of any facts other than that document to support conception of your unified shader invention on August 24, 2001?

MR. RENAUD: Objection.

A I am aware of at least that other specification, which is Exhibit 3, that you gave me, that is the proposal for the R400 architecture that is also dated well ahead of the August 24, 2001 date. So that would be another proof or fact behind the

fact that this chip or this idea was conceived on or before that date.

Q Anything else?

A Sure. We can go to the Perforce server again and do a search of the files that existed then. I must have written some portion of the C simulator which described the R400 functions. That would be another thing we can look at.

Q Do you know if that exists? Have you reviewed that code to see if it exists?

A I know that I reviewed the Perforce submission as part of doing this Declaration, which has a calendar, and so if we look at this calendar and pinpoint August 24, unless it goes all the way down -- yes, I think it does.

So by August 24, 2001, the only entry in this calendar on page 33 is the sequencer specification, and from that point on, there is a list of code and changes that occurred that showed that we worked on the R400 project from that point on.

MR. RENAUD: Just so the record is clear, all of the documents that he's referring to regarding Perforce have been either produced or made available to respondents.

MR. ELENGOLD: When you say "made available," I'm not sure what you're referring to.

MR. RENAUD: The source code is on a source code computer.

MR. ELENGOLD: Yeah, and the documents have been produced?

MR. RENAUD: Yes.

Q So I believe you discussed this August 24th date in your Declaration as well. Do you recall that?

MR. RENAUD: Objection.

Q I'll direct you to page 8.

MR. RENAUD: Can you just state the Exhibit number because there are multiple declarations in the case?

MR. ELENGOLD: I think there is only one that we're using today, but it is Exhibit 6.

MR. RENAUD: Thank you.

A Yes. So in this Declaration -- sorry, making sure I get the words right. I did describe that the Version 0.4 of the R400 Sequencer Specification was dated on August 24, 2001.

And furthermore, to qualify our previous discussions, it says here that this date was corroborated by the Perforce log. So I think it is a true and accurate date because you had some

contention to the day before, you said it could be this or after. This can conclusively prove that it is actually this date and not another one.

Q The documents that are cited in your Declaration prove that?

A The fact that the log entry meant that, when I did this Declaration, and I do remember reviewing the calendar events against the Perforce logs, so I'm confident that this is a true and accurate date, and it came from the Perforce log and not only the written version on page 3 of Exhibit 10.

Q And the purpose of your Declaration was to similarly establish a conception date and to a reduction of practice date with regard to the prior proceeding, is that correct?

MR. RENAUD: Objection.

A Can you rephrase your question? I got confused.

Q Sure. When you put together this Declaration, it was to try to talk about your work on the R400 with regard to the unified shader patents, correct?

MR. RENAUD: Objection.

A I believe this Declaration that I did was to show work on the R400 project and when each of the elements occurred. I mean, it is obviously, the

R400 is an implementation of the patent, so by extension, it is loosely related to the patent, but this is really more a collection of facts about the R400.

Q So beyond the facts that you gathered for your Declaration that you submitted on this topic, are there any other facts you're aware of today regarding the R400 that support your August 24, 2001 conception date?

MR. RENAUD: Objection.

A I mean, again, on the Perforce server, I mean, we can check again and re-corroborate, and that will point to that date I'm very confident, but you have, like, both the written date on the spec as well as an automated lead generated date on Perforce. I don't know what else would be needed to prove the date on the specific specification of the R400 Sequencer.

Q So more broadly, are there any facts regarding the work on the R400 that you're aware of today beyond those that you discussed in your Declaration?

MR. RENAUD: Objection.

A In my declaration here, I am not talking at all about the IKOS prototype effort. So this is one case that is not recorded in this Declaration and

has been done by AMD. I'm only human. I mean, there's probably more things, but I can't offhand think of anything else.

Q And that's the IKOS system we talked about with regard to Exhibit 9?

MR. RENAUD: Objection.

Q Is that correct?

A Yes. This is the similar -- this is the same IKOS, and we did touch on this subject when this Exhibit was brought up.

Q Are there any other facts you're aware of beyond those in your Declaration and the IKOS device regarding the R400?

MR. RENAUD: Objection.

A Can you describe, like, what facts --

Q Sure.

A -- you want me to, because this is a very, very broad subject on a very broad --

Q You told me earlier that you're here to testify about facts related to topics including conception and reduction to practice, is that correct?

A Yes, that is correct.

Q Beyond the facts that you put into your written testimony and what we've discussed regarding the IKOS device, are there any other facts that you're

aware of to support those topics?
A I see.
MR. RENAUD: Objection.
A No, as of today, there are no other facts that I can remember being aware of.
Q For conception and for reduction to practice.
A Again, I'm not an attorney. I don't know what conception, reduction to practice means. I can speak about the dates of the R400, and timeline, and the specifications. If this was your question, then yeah.
Q Okay. Turning back to Exhibit 11.
A Yes.
Q Staying in the same paragraph we were in, the third full sentence begins, "The asserted claims of the '454 patent were actually also reduced to practice," do you see that sentence?
A The asserted claims. Yeah, so you're referring to page 3, line five?
Q Yes.
A Okay, "Asserted claims of the '454 Patent were also actually reduced to practice, in the form of physical embodiments, at least as early as April 20, 2003 and June 26, 2003." Yes, I see those lines.

Q What happened with regard to the R400 project on April 20, 2003?

MR. RENAUD: Objection.

A I don't recall this exact date. It might be the date on which the -- there was some evidence of IKOS implementation, but let me check the calendar to see if this date is present in the calendar to refresh my memory.

April 28, 2003.

So I see some check-ins on that date from the calendar, I don't know, some RTL check-ins and a test. I don't know why that date got picked up in this notice here, but, you know -- "form of physical embodiment."

I don't quite understand the physical embodiment nomenclature, if you will. But so I don't know.

Q What happened with regard to the R400 program on June 26, 2003?

MR. RENAUD: Objection.

A June 26, 2003. Again, from the calendar there were some check-ins to the Perforce depot. And the first synthesis of the R400, at least according to Exhibit 9, page AMD1044_0175196 said that the first synthesis occurred on, I guess it

is August 3, 2003, or on or before August 3, 2003. Other than that, I can't really remember or tell from the documentation that you have here in front of me what actually occurred on that date. I don't recall.

Q For the R400 program, what activities were occurring between August 24, 2001 and the third quarter of 2002?

MR. RENAUD: Objection.

A Can you restate the question, please.

(Question read back.)

A August 24. So that's initial.

And the third quarter of?

Q 2002.

MR. RENAUD: Objection.

A And by "third quarter," you mean up until what, August? September? What do you mean by third quarter?

Q Let's go with July.

A July.

Q What was occurring with regard to the R400 program between August 24, 2001 and July 2002?

MR. ELENGOLD: Objection.

A Again, I am referring to my Declaration, which is Exhibit No. 6, calendar, Diligence Calendar. On

page AMD1044_0011651, shows that on August 24, the sequencer specification was created or at least checked in, and I believe this was Version 0.4, which was Exhibit No. 10.

After that, I can see that on pretty much every day that was not a weekend day, there were work and things checked in into the various directories of Perforce on a day-to-day basis, and all the way until July 2002.

So I can tell you that work was occurring everyday by a large party of people, which are listed again on the same Exhibit, page AMD1044_0011641; we can see that there was substantial group of people and making a substantial amount of changes to the R400 program.

Q Were all of these people working on the unified shader?

MR. RENAUD: Objection.

A In the R400 timeframe, the sequencer, because it was at the center of the chip, was one of the blocks that did not have a block level test bench, meaning it could not be tested in isolation from the other blocks.

As such, in order to make forward progress on the sequencer, we needed what we call the GC

environment, which is the graphics core; that is, all the blocks of the graphics domain to be working and energizing. And so all of these persons are all, as far as I can tell, and again, a lot of them left AMD, but at the time were all graphics designers or graphics architects; might not have directly worked on the unified shader blocks per se, but all their work was relevant to the unified shader because of the reason that in order to enable testing of the unified shader, and the sequencer and the SP, we needed the whole graphics core block to be working.

Q So is it true then that the sequencer was never tested until November 2003?

MR. RENAUD: Objection.

A I fail to understand why you're making that comment.

Q Well, your Diligence Calendar shows work occurring on R400 through November 2003, is that correct, and that's on page 175547.

A 175. Which date did you say, sorry?

Q November 2003. So is it correct that your Diligence Calendar that you put into your Declaration shows work occurring on the R400 until November 2003?

MR. RENAUD: Objection.

A This Diligence Calendar shows that there is work, yes, occurring on either the tests infrastructure, which are used to test the sequencer or the emulator or the RTL. But it doesn't mean that the SQ, or the sequencer, the R400 Sequencer, was not tested before then. It means that the testing or the, you know, the work progressed all the way to that November 20th date.

Q When was the sequencer first tested?

A So you can say that effectively the sequencer -- and again, it depends on your definition of "tested." Can you refine exactly what you mean by tested?

Q Well, you just said there was no block level test bench, so everything affected the sequencer because it couldn't be tested until the other people did their work, is that correct?

MR. RENAUD: Objection.

A I did say there was no sequencer test bench, and thus by definition, the sequencer was affected by the other blocks. That is correct.

So for example, if one of the other blocks were to break or stop working, this would affect temporarily at least the sequencer because the

test would be broken momentarily. It doesn't mean that the sequencer was not tested and, you know, in fact of the matter is, if you find that a given change to another block broke the graphics core test bench, you could just revert that locally on your machine so that work can continue on the sequencer on the R400.

Q And those kinds of changes were occurring at least through November, 2003, is that correct?

MR. RENAUD: Objection.

A From this calendar of event, I can't really tell you what kind of changes occurred. We would need to go to the Perforce depot and look at each and every change and see what was modified.

This just says that some work occurred all the way up until November 20, 2003. And this Exhibit here, which is Exhibit No. 9, shows that by August 30 of 2002, the single triangle test was working on the sequencer, and this was a GC test bench, which is the same test bench that we are referring to here.

Q And additional problems were getting fixed until November 2003, is that correct?

A Additional issues, or problems or, you know, new features requested by Microsoft or whatnot, were

being addressed all the way up to November 20, 2003.

Q And why do you say "being addressed" by Microsoft? Is the calendar not specific to the R400 program?

A The calendar is specific to the R400 program. However, as I stated before, the R400 is a PC graphics processor. As such, it is affected by any changes that Microsoft does to the API and, you know, one clear change that occurred for us was, the release of an API called Direct Text 9 caused us to have to redesign the sequencer and is one of the main reasons why we had to move from the simpler version of a sequencer that was doing the unified shader on the -- as described on the August 14 specification onto a more evolved sequencer that was supporting unlimited clauses in order to obey new Microsoft API restrictions.

Q When did you start working on that new sequencer, do you recall?

MR. RENAUD: Objection.

A That would have been, and I quote here in my Declaration, Exhibit No. 6, page AMD1044_0011636, Sequencer Specification Version 2.0, April 19, 2002. So given that this specification was checked in on that date, I would have worked on

the Sequencer Version 2.5 at least on or before that date.

Q Were there any revisions to the sequencer specification after 2.0?

A Yes, there were. In fact, if you refer to again Exhibit 6, page AMD1044_0011679, you're going to see a table there that lists a collection, and I don't think if it's an exhaustive list of all the specifications ever released, but you can clearly see that beyond 2.0, we went to 2.1, and then all the way to revision number 2.11, all of which I believe were provided as part of this written testimony as Exhibits.

Q Do you know if the 2.11 sequencer specification was the last version of the specification?

MR. RENAUD: Objection.

A I do not recall that information, no.

Q When did you stop working on the R400 sequencer?

A Again, the work for me from the R400 to Xenos transition was seeming -- I mean, it was very fluid, and so I don't really remember how and when I transitioned to Xenos, and how and when documents got imported over.

The fact of the matter is the Xenos program, as far as the sequencer and the unified shader is

concerned, is the R400 program, and such, you know, it was just one big continuous for me.

Q So the R400 sequencer could have continued changing even after version 2.11 was complete, is that right?

MR. RENAUD: Objection.

A So it could. What it could also mean is by that time the R400 program got cancelled and we started working on the specification in the Xenos depot, but like I said, to me it's just a location for a file, and so I would have continued working on the sequencer, almost as if it was the R400 because they were so similar.

Q Was the sequencer always getting modified up until when Xenos chip was netlisted for production?

MR. RENAUD: Objection.

A So while I know a lot about what's inside Xenos because it's the same design for me as the R400, I'm not as familiar with the Xenos dates, and so I don't know and remember how this would line up with my work on the R400, or my work on Xenos per se.

Q Was the R400 sequencer constantly being changed until the end of the R400 program?

MR. RENAUD: Objection.

A I can tell you. Let me look at the calendar again. So the R400 -- so the calendar is not precise enough because the -- the R400 sequencer would have been under Arch, which is, if you look at AMD -- sorry, Exhibit 6, page AMD1044_011651, the Arch -- sorry, I'm going to give you time to go to it.

All right. The Arch category as noted here is the architecture folder history which contains more than just the sequencer. So any day here where you see "Arch" in the calendar could mean that there was a sequencer change, and we could map that, again using the Perforce server, can tell you exactly when the last revision of the R400 sequencer specification got checked in. I just don't have this information readily available.

Q Is that what would have been in the Arch folder?

A Yes, it would have been an Arch change, so for example here, the last Arch change that I see in this calendar occurred on Monday, October 6, 2003, unless I missed an entry.

Q So outside of what we've discussed with regard to the calendar in your Declaration, which is Exhibit 6, are there any other activities you're aware of

that were going on with regard to the R400 program from August 2001 to July, 2002?

MR. RENAUD: Objection.

A Again, there was this IKOS activity, which is the hardware prototype, which was, you know, at least planned, and if you give me another presentation which has more complete dates, we could get a better refine date on this, but it was at least planned to be occurring around 11, October 11 of 2002.

Q And you think that took place before July 2002?

A Sorry, so July 2000 -- no, of course. Well, I mean, it was planned to be. Whether or not, you know, things got started on that machine before that, you know, I would have to --

Q That's the IKOS emulation start you're talking about that's in Exhibit 9?

A Yes. That is it.

Q So if that emulation had started before the August 30, 2002 presentation, do you think it would have said it in the presentation?

MR. RENAUD: Objection.

A So this is saying whether or not we were -- so effectively, my understanding of this IKOS emulation start line is that we would have been

successful into porting a netlist on the IKOS server. It doesn't mean that tries before did not occur. I can't know that conclusively, and there could be evidence on the Perforce server or elsewhere of that effort before the date that we discussed.

Q So you believe the IKOS emulation start means a successful emulation on the IKOS machine on that day.

MR. RENAUD: Objection.

A I mean a successful implementation of the netlist on the IKOS hardware.

Q That day. To be a start, that would be a successful implementation, not the start of trying to get a successful implementation.

A Can you define to me what you mean by implementation? I mean --

Q I believe that's what you -- the word you used so I'm sorry if I didn't -- for the IKOS emulation start, whatever it is that is involved with on the IKOS device testing the netlist, it's not the start of that testing. You believe this start is the successful date, is that right?

MR. RENAUD: Objection.

A I believe the date here is the date on which we

were able to push the netlist on the IKOS machine. Once a netlist is on the IKOS machine, you can start trying to run things on it.

Q Is that the IKOS emulation with software date, when you start running things on it?

MR. RENAUD: Objection.

A No. The IKOS emulation with software, in my opinion, refers to trying to use the IKOS hardware with the driver versus trying to energize it manually, if you will, with simple tests.

Q Okay. So other than what's identified in Exhibit 9 and the calendar in your Declaration, what other activities are you aware of that were going on with regard to the R400 program from August 2001 to July of 2002?

MR. RENAUD: Objection.

A That is the extent of what I remember.

Q Other than your Declaration, Exhibit 6, and Exhibit 9, what activities are you aware of that occurred from July 2002 to April 2003 with regard to the R400 program?

MR. RENAUD: Objection.

A I mean there's a bunch of other presentations that we have as Exhibit that I've seen. Without seeing them again to refresh my memory, I can't really

remember of any other activities offhand.

Q What about from April 2003 until November 2003, what activities are you aware of that were occurring with regard to the R400 program?

MR. RENAUD: Objection.

A April 2003. April 2003 to?

Q November 2003.

A November 2003. Okay.

Other than the work described here, I mean, of all the change list that occurred in the R400 depot, I can't think of anything else offhand.

Q When you say the work described here, you're referring to the work identified in your calendar in Exhibit 6?

A Sorry, yes, I am referring to Exhibit 6, page AMD1044_0011671 to AMD1044_0011678.

MR. RENAUD: Counsel, this might be a good time for a break. We've been going about an hour.

MR. ELENGOLD: It's up to you if you want to break. I thought you wanted to try and power through.

MR. RENAUD: I do, but I can tell the witness is tired and I'm getting tired, so I thought a break might make sense.

MR. ELENGOLD: Okay. Let's go off the

record.

VIDEO OPERATOR: The time is 3:49. We're off the record.

(Recess taken.)

VIDEO OPERATOR: The time is 4:20 p.m. This is tape five. We're back on the record.

MR. RENAUD: Counsel, during the break, we called in to AMD to clarify some issues that were asked during the deposition on a subject matter, so the witness has some additional information to supply regarding one or more of your questions.

MR. ELENGOLD: Yeah, so it's up to you, if you want to, you know -- it's late in the day, and I don't want to have this go another four hours, but we can, if you want to introduce new information now or if you want to redirect him or however you'd like.

MR. RENAUD: I'm not redirecting him. You were asking questions about what the complement of knowledge was of the company. He is an individual trying to represent a company and --

MR. ELENGOLD: He's still getting knowledge is what you're saying.

MR. RENAUD: Yeah, he is.

A Okay, so basically --

Q Just let me ask questions. We'll go from there.
A Okay.
Q Earlier you mentioned that you identified during the first break, that the individual you talked to is Ron White, do you recall that?
A One of the persons I talked to was Ron White, yes.
Q You identified him as the name you couldn't remember earlier, right?
A That's correct, yes.
Q And then Mr. White, you said was an SMTS, is that right?
A That is what the AMD People Finder Repository says.
Q And what is his role at AMD?
A My understanding is that he's part of the product team. That's what his record says. I don't know what he does in that role on top of that, and I saw his name on the, on R400 IKOS status list, if you will, which means that he was involved in the IKOS support in some respect for the R400 program.
Q And what information did Mr. White give you regarding your investigation?
A Well, again, it was trying to assert that the presentations that we had on the topic of the hardware IKOS simulation were coherent with his

memory of the activities that occurred on the IKOS hardware machine, same as we'd done with my other colleague, which his name escapes me again. Colin? Colin Stuart. Sorry.

Q Was there any other additional information you learned from Mr. White other than what we've already discussed today regarding the IKOS machine?

A Well, regarding the IKOS machine and otherwise, because this is all tied to the same subject, I did review, re-review actually, a number of documents that were in the room, the break room we had.

Q With Mr. White?

A No, not with Mr. White. But I did review them with -- on a call with Pam Horn and Dave Christie to see exactly the amount of information AMD provided as far as the --

Q Just to be clear --

MR. RENAUD: Let him finish.

Q -- this is at Mr. White's suggestion?

MR. RENAUD: Let him finish the answer. Finish your answer, sir.

MR. ELENGOLD: No, it's okay. I --

MR. RENAUD: You're not going to interrupt

his answer.

MR. ELENGOLD: I'm not intending to interrupt. I just want to make sure he understood my question. I don't have to strike his answer, but --

A Your question pertained to the IKOS program, and the IKOS program as I understand --

Q What you learned from Mr. White with regards to the IKOS program.

MR. RENAUD: Are you going to let him answer?

A I learned from Mr. White -- we tried to record from Mr. White the amount of recollection he had on the IKOS program. What I'm trying to tell you is that on that subject matter, which is the whole implementation of the R400 on a hardware machine, looking at the other documentation that was present in the room, I saw that there was a bunch of document that were likely not in the Exhibit 6 agenda because they were in directories that were not covered by this particular investigation, and they were, you know, provided, as I understand, by Pam Horn in AMD, and Dave Christie, to you to describe the amount of work that went in, into the IKOS server, as well as other activities of AMD

during that timeframe, and these include, like, extensive Perforce logs as I understand, and extensive presentations that are not covered in this detailed agenda that only covers a subsection of the directories of the Perforce server and not the whole database.

And furthermore, I also saw some other Xenos presentations that were laying on the table, and that reminded myself that this is, although not -- also, sorry, not covered by Exhibit No. 6, and I understand, because it was on the table down there, that it was provided as information to you guys.

So there is a wealth of document that are available that show work that are not covered by the scope of this particular agenda which is definitely inclusive -- well, not inclusive, but it's -- all the work here is included in the document, but this is not exhaustive as to the amount of information that AMD has on the work that went in.

Q The documents you're referring to, did you review them yesterday?

A They were on the table all day but, you know, honestly, the table is covered with documents so

we reviewed them briefly. I remember seeing the Perforce log, don't remember going through it, but since you kept asking questions about, in particular, this agenda, then I decided to go ahead and talk to Pam to see if it really was the extent of what we presented, and then she said to me, no, I mean, there's more to it than that, and she pointed me back to the log.

So when I started looking at the log in more details, I realized that this is not the complete list. There is way, way more than that, and you know, just forgot about it when I was talking about this.

Q Did you review the documents on Monday?

A Which -- I mean --

Q The documents you're referring to, did you review them on Monday?

A The document, the Perforce log was on the table. I glanced at it but, you know, I didn't pay attention as to exactly what directories were described in the whole Perforce log, and so I didn't pay attention to the content itself of the logs, and didn't realize how extensive it was compared to the logs that are described here in this Exhibit.

Q So you reviewed them Monday, yesterday, and today, is that correct, these Perforce logs that you're talking about?

MR. RENAUD: Objection.

A So the logs were on the table. I saw them. I did not, you know, go through them one by one on Monday and Tuesday. I did go and look at them today after I talked to Pam because, you know, she reminded me we have all these logs, and so you make sure that you explain to them that this is more than just what you did on the sequencer. There's all of the MAS, so they are not just the sequencer and the SP. All of the presentations that we provided are not in these directories that you have in your Declaration because some of them are on servers, and she told me -- and Dave actually told me that we also provided, you know, tests, and test descriptions, and test logs, which would also not be on the, on these particular directories in Perforce.

Q When did you talk to Pam Horn?

A I just did during the break with Dave Christie as well.

Q How long did you talk for?

A If memory serves, about 10 minutes or so. 10

minutes with Pam, maybe six minutes with Dave Christie because he joined in after she had her -- she called him basically to complement her answers.

Q Was it your idea to call Pam Horn during the break?

A So it was after I sought wealth of document on the table and realized that I was not talking here on my behalf but on behalf of AMD, that I decided to go forward and make sure that I was covering everything because this particular declaration is somewhat -- well, it's exhaustive, but it only pertains to the sequencer, which is not the whole R400, so I wanted to make sure that, because I'm not talking in my name, I got all the bases covered.

Q Was it your idea to call Pam Horn during the break?

A Well, I mean, again, I was looking at the specification, and so that was my idea to look more and then find more, but the actual idea of calling came from counsel.

Q Which counsel?

A The present counsel.

Q Do you know their names?

A Well, I mean the counsel Adam Rizk and --
Q So Adam and Michael suggested that you call Pam, is that correct?
A Well, they called her and put her on the line, yeah, but --
Q So they just called her.
A They opened the line to Pam, is all they did.
Q Did you ask Pam questions?
A Yes.
Q What was the first question you asked Pam?
A I asked Pam to tell me if the Perforce log on the table that was sitting next to me was part of the evidence that was sent to the counsel team and if there were more, because I was concerned that, you know, there was not enough information here to cover everything or every activity that occurred at the AMD. I'm only human. I can only know so much.
Q What was the name of the Perforce log?
A That Perforce log did not have a name. It's just a thick book of paper with all of the Perforce entries in both the Xenos repository and the R400 repository. It's just a big stack of paper with a big paper binder attached to it.
Q Did you ask Pam any other questions?

A I said -- well, I asked her about the other evidence produced, and then she offered to call Dave Christie, which is the person that actually did the data collection, I understand, on AMD's behalf, and he pointed me to the other evidence and, you know, for that matter, on the IKOS server, he just offered me during the phone call that he found a netlist that was pushed on IKOS and that was containing the whole graphics core that was dating around April of 2003. So that is new information that he just gave me on that phone call.

Q Just 20 minutes ago you learned that there was a netlist that was pushed on IKOS in April 2003, and that that netlist had been found, is that correct?

A Like I said before, I talked to Dave Christie yesterday to initiate, like, a search for the netlist, and so I guess he went ahead and did that over the last -- I mean yesterday, and some of it today, and so because he was on the phone with me, he just offered to say okay, well, by the way, I found this new piece of evidence, and I'm telling you now so you can say it or not.

Q Was that netlist the first netlist that was used with the IKOS emulator in April 2003?

A I don't know if it's the first netlist because he told me that he found a netlist called 4 point something, and the IKOS log that is on the table down here was referring to Netlist 3. So there might be -- it might not be the very first netlist that got pushed onto the IKOS hardware emulator.

Q Is Netlist 3 the list that he located today?

A No, like I said, the netlist he told me he located today was called Netlist 4.

Q Netlist 4?

A And he told me it was dated around May of 2003, and he told me he found a bunch more, but I don't remember all the names and I don't want to mislead you in any way, so please, that -- there is at least one more, and there's probably a couple more.

Q Did you ask any other questions of Pam or David?

A Let me think. I asked the -- what kind of -- so the Perforce log, what directories in Perforce it was covering, the thick book that was on the table; that's when I realized there was a mismatch between that and the dates here, and after that, the presentations that were submitted, the test logs that were submitted, the name and the MAS specifications and which ones, and they told me

they submitted pretty much every MAS, architecture MAS of the R400 and Xenos, and also, some Microsoft presentations were apparently submitted.

And I'm sure there's much, much more, but if you want me to describe them to you, I mean, we would have to put them here on the table to look at them.

Q What Microsoft presentations are you referring to?

A There was at least one presentation sitting in the middle of the table that was -- that had a title called: Xenos, so I assumed it was a Microsoft presentation.

Q To Microsoft or from Microsoft?

A This was on an ATI template with Xenos, so I am assuming it was a presentation from ATI to Microsoft about the status of Xenos. It was a program review presentation, and there were also a few more presentations sitting on that table too.

Q When was the first discussion with Microsoft regarding the Xenos chip?

A I can't tell without, you know, looking at the documents.

Q Is there a document that shows the first time anyone from AMD discussed with Microsoft the Xenos chip?

A I'm sure there will be some kind of document that show the communications, and from those documents, we can infer which was the first, you know, discussion to Microsoft, but I can't remember all of these dates on all this wealth of documents. If you want to talk about these, I mean, just bring the documents on the table and we can sort them and look which one is the first one.

Q Do you know if the first discussion of the Xenos chip between Microsoft and ATI has been produced in this case?

A I don't know if the first one got produced or not, but I know that from discussions with Dave and from the document I saw, that presentations were disclosed, and so you know, I can't say conclusively from those presentations whether or not the first presentation would have been here or not, but there were a wealth of presentations, and some of these presentations were to Microsoft.

Q Did you do any investigation as to when the first offer of the Xenos chip to Microsoft was?

A Can you rephrase the question, please.

Q Sure.

A When you say "first" --

Q In preparing for your deposition, did you do any

investigation into the first communications between ATI and Microsoft regarding the Xenos chip?

MR. RENAUD: Objection.

A So I did not personally do this but, you know, again, I am very aware that documents exist out there, and I'm sure that between the Perforce log and all the presentations that exist, if you put them on the table, we could look at them, and I am knowledgeable about -- sorry, knowledgeable enough to figure it out and, you know, discuss it with you.

Q Do you know when the first offer of the R400 was made to Microsoft?

A I don't know if the R400 ever was offered to Microsoft or not. I mean, again, if you want to discuss these topics, we have a wealth of documents, a lot of presentations. I'm sure we can find it. It's just, you know, it was all submitted apparently, according to Pam and Dave Christie. So put it on the table and we can look at it and discuss the facts.

Q You understand you were designated today to talk about certain topics, correct?

A Yes.

MR. RENAUD: Objection.

A But you know, I'm only human. There's like, like I said, the table downstairs is covered, literally covered with documents. There is like thick books and papers of presentations and logs and whatnot. So I can talk about any of these if you bring them on the table so I can look at them. I can't talk to them from memory.

Q Any other questions you asked Pam or David through your call today?

A Not that I recall, no. It was really about trying to figure out what, you know, what was disclosed by AMD to make sure I was not misrepresenting the amount of information and the amount of work that went in to, you know, the development of both the R400 and Xenos, and you know, the only conclusion so far is, this is not exhaustive and there's way more than just this Exhibit 6.

Q I believe you testified earlier that other than that, and Exhibit 9 and the IKOS work, the IKOS emulator work that's discussed in Exhibit 9 -- sorry, let's strike that.

Other than the work described in Exhibit 9 which includes the planned IKOS emulator work, and your Exhibit 6, is there any other work of which

you're now aware of regarding the R400 based on your discussion with Pam and David?

MR. RENAUD: Objection.

A Yes, like I said, there is a ton of documentation that I -- I mean, there's a ton more presentations like this that are on this declaration that are available, and apparently were submitted, which we can discuss. There is the test logs, which would not be on the Perforce server because they're just, you know, logs, and apparently those were submitted as well, as well as the tests, and we discussed before the source machine, the source code machine. So there was also code published on that machine that can be reviewed to see the amount of work that went in the RTL.

You can see the difference, you know, between the two file revisions at different states to see how much work went in. There's MAS specifications. There's the Perforce log of the whole depot which, you know, includes all the change that went into that depot and not just the Sequencer and Arch subdirectory.

Q In addition to the first triangle test that we discussed earlier, what other tests were conducted on the R400?

MR. RENAUD: Objection.

A So there is like a lot of unit level testing that was done on the R400. I mean hundreds and hundreds of tests. My understanding is also that this got produced, the test name, test subdirectories. I've seen them on the code machine when I reviewed the code machine yesterday. So we can look at that. I mean there's just a lot of them.

And also, I know that on the -- sorry, the web server that apparently Joe Cox provided, that's another nugget that Pam gave me, that was provided, and that included the regression results and summaries of these tests at some dates and time, and apparently, that also got submitted, according to Pam and Dave, so we could look at that as well.

Q Is it still your opinion that the graphics system of the R400 was functionally complete when it passed the first triangle test?

MR. RENAUD: Objection.

A Can you define what you mean by "functionally complete"?

Q Did it work?

MR. RENAUD: Objection.

A I believe it -- I mean, the purpose of the shader, the unified shader, unified pixel and vertex shader is to process pixels and vertices, and so I think that the one triangle, admittedly, it -- sorry, it is a fairly simple test, but it shows that the shader is able to process both vertex and pixels, and as such, it shows that it can work in the simplest form. It doesn't mean that all the corner cases are, you know, figured out and everything, but to me, the test passes, the test worked. The hardware generates a picture, the right picture.

Q Can you please turn to Exhibit 12.

A Yes. I am on Exhibit 12.

Q Do you know what a patent claim is?

MR. RENAUD: Objection.

A Pardon me, can you repeat?

Q Do you know what a patent claim is?

A I know where to find the patent claims. I know how to read them in English. I can't really interpret them in the sense of the law because, you know, I'm not equipped to really tell you what they mean in the sense of the law.

Q Were you involved in drafting the claims of the '454 patent?

A The way I recall it working at AMD is what we filed, what we call an IDF, which is Invention Disclosure Form to the attorneys, or an attorney in that particular case, and we describe and work with the attorney to describe the machine, in that case, the R400, and then the claims are -- were worded by the attorney retained to write this patent, and that's my understanding on how it went.

Q Do you have an opinion on whether or not the R400 uses claim 2 of the '454 patent?

MR. RENAUD: Objection.

A So not being an attorney, I don't have an opinion on the claims per se. I can't break down the product down to a set of claims. I have not done the regression, the, you know, the study to see what exists and what not. What I can tell you is I believe the R400 and the unified shader in that R400 are implementing in the general sense what is described in this patent, yes.

Q Can you look at Figure 4A please on page 171. Have you looked at this figure before?

A Yes, I have looked at this figure. This is a figure in the patent, so having read the patent, I've seen this figure before, yes.

Q Does this figure look like an accurate representation of the R400 to your knowledge?

MR. RENAUD: Objection.

A This figure looks like, yeah, an implementation of the R400 that we had.

Q When you say "an implementation of the R400," what do you mean?

MR. RENAUD: Objection.

A I mean, first, this picture is very high level, so it's hard to really map it directly to the R400 hardware device, and I know that we went back and forth as to whether or not to include the texture vertex cache on the R400. So I don't remember in the end, if the product had such a device or not, but generally speaking, it looks like it, you know, maps to some degree to the R400 product.

Q Why do you say "to some degree"?

A Because like I said, this is a very high level picture and so -- and I'm also working from memory, so if you want to go into the details and go and compare the R400 product, we could just go and look at the verilog code and make sure that the connections are accurate, and the modules that are listed here exist or not, and so forth and so on.

Q Have you done that?
A I have not done that personally, but you know, put the code on and we can do it right now.
Q Has anyone at AMD to your knowledge compared the RTL code of the R400 to the Figures of the '454 patent?
MR. RENAUD: Objection.
A So I know the code got produced. I don't know if anyone at AMD did or did not do it. I mean, I know there is a lot of evidence that was produced, and somewhere in there, there is probably a mapping of that nature. It's just -- you know, again, I can't, I can't remember, if you don't put the -- it's too far away. You have to put some documents in front of me for me to conclusively say one way or another.
Q What about Figure 5. Can you turn to Figure 5, please. It's on page 172. Does Figure 5 look like an accurate representation of the R400 architecture?
MR. RENAUD: Objection.
A By "R400 architecture," what do you mean exactly? Can you refine your question?
Q Sure. Do you remember any documents that referred to the R400 architecture that we looked at

earlier?

Q And you don't have to look. I'm asking if you remembered, but I'm taking it you don't, so let me ask it a different way. Looking at Figure 5, does Figure 5 look like the R400?

A Figure 5 looks like, yes, something we would have implemented in a similar fashion from the R400. I mean, assuming the GPRs would be block 92, and then the sequencer would be block 99, it looks, you know, fairly familiar as to what the R400 unified shader would have looked like.

Q Why do you say that block 99 looks like the sequencer?

A Well, for one, it contains the instructions store in the constant, which is where these things are located in the R400, and for two, in the specifications, column 4, line 52, it states, "The sequencer 99 includes constants block 91 and instructions store 98," so.

Q Anything else?

A Anything else about what?

Q Why you say block 99 looks like the sequencer. Any other reason?

A Well, I mean, it's connected to the SP, or the ALU unit by line 94. And I can go and read the spec

to give you more. The constants block 91 contains the transformation matrices used in conjunction with vertex manipulation operations. Those are all the, you know, operations that would have occurred on the sequencer. "Instruction store 98 contains the necessary instructions that are executed by the processor 96."

So you know, the whole paragraph here describes it in some detail.

Q So turning back to claim 2, having now looked at the figures and the specification, do you know whether the R400 practices claim 2 of the '454 patent?

MR. RENAUD: Objection.

A Again, I mean, claims are patent verbiage for me, and I'm not equipped to discuss the claims. I'm not an attorney. I can tell you again that this patent, like the Exhibit 12, the patent '454, is based on the R400 design, and as such, I think the R400 is an implementation of this patent.

But further than that, I mean, can't really tell you.

Q So you don't have an opinion with respect to whether the R400 practices any claims of the '454 patent, is that correct?

MR. RENAUD: Objection.

A I just said that the R400 chip or graphics core is an implementation or is a hardware implementation of the patent. I mean, how it maps to the claim and which, I'm not equipped to answer that question.

Q So no, you don't have an opinion whether the R400 practices the claims of the '454 patent, is that correct?

A I have said that I am not equipped to answer that question. I did not say yes or no.

Q You don't have an opinion.

A I said that I'm not equipped, I don't have the right knowledge, right background. I haven't worked through all the claims and worked through all the litigation to understand that question and answer it in any way.

Q Do you know what a processor unit is?

MR. RENAUD: Objection.

A In the scope of the R400, as it is described, I believe, one of these specs, I believe it is described in some amount of details in one of the specs that were given, but I don't have it in front of me. If you ask me in the scope of the R400 -- what was the question?

Q Processor unit?
A Processor unit would then be one of what we call the shader pipeline.
Q What's a shader pipeline?
MR. RENAUD: Objection.
A R400 shader pipeline is, according to Steve's specs here, which is Exhibit 3, page AMD1044_0175479, is -- sorry. That's not what I was looking for. So it is a -- it says the shader pipeline operates -- on page, sorry, 1044_0175478 is the module that operates on vectors of 16 -- "vector of four 2 by 2 pixel footprints. A total of 16 pixels," in the case of pixel, "for vertex processing," and I continue reading from the spec. "Each of the pixels is replaced by a vertex." So it is, you know, the block that performs the ALU operations, if you will, on vertices or pixels.
Q Do you know, outside of Exhibit 3, what a shader pipeline is?
MR. RENAUD: Objection.
A If I know outside --
Q Well, let me -- I asked you what a shader pipeline is, and you had to refer to a document. Does that mean you don't know what a shader pipeline is with respect to the R400 without referring to a

document?

MR. RENAUD: Objection.

A No. The reason why I referred to this specification is to try to be precise in my answer in terminology. My understanding is, in the R400, in the pipeline, and the chip in general, the shader is the part that executes the ALU instructions.

Q So the shader is inside of the shader pipeline; is that what you're trying to say in that distinction?

MR. RENAUD: Objection.

A In the R400, the shader pipeline contains the ALU modules and it is the block that executes the ALU operation.

Q The shader pipeline is the block, is that what you're saying?

A The shader pipeline, or I mean, in one -- it's terminology, but the shader pipeline can be seen as a block, yes. That includes the GPRs and the ALU units.

Q Are shader pipeline and the shader synonymous for purposes of the R400 documents?

MR. RENAUD: Objection.

A So again, in the scope of the R400, I believe I've

said before that shader is the program that you run on your vertex or pixel shaders, and the shader pipeline is the block that operates on the ALU instructions.

Q Is the sequencer inside of the shader pipeline?

MR. RENAUD: Objection.

A The sequencer is inside the shader complex, I would call it, so but it's outside of the shader pipeline. So if you go to Exhibit 10, the Sequencer Specification, there is a picture on page 11 that shows the shader pipe, and so you can see that the docs states, "the grey area represents blocks," and I read, "that are replicated four times per shader pipe."

So this is what I would refer to as the shader pipe, and you can see that from that picture, the sequencer is just sitting next to it and ordering instructions into the shader pipe.

Q And this started with us discussing where the processor unit was in the R400, do you recall that?

A Correct. And started with the fact that, you know, we don't really use the term processor unit in the R400. So I was trying to map that word on our terminology to better understand your

question, which was not very clear to me.

Q And were you able to identify the processor unit in the R400?

MR. RENAUD: Objection.

A So to me, I think the processor unit in the R400 design -- and again, it's not directly tied in the specification that I'm seeing -- would be the shader pipeline, which is this block on the left side of the picture.

Q Can you please look at Exhibit 13. And Exhibit 13 do you recall is the '846 patent?

A Yes.

Q Have you reviewed the claims of the '846 patent?

A As stated, I read the patent, so I read the claims as well, yes.

Q Do you have an opinion on whether the R400 practices the claims of the '846 patent?

MR. RENAUD: Objection.

A Again, I am not an attorney. I am not equipped to answer how and when and why the R400 maps to any of the claims. Again, my answer is the same. The R400 is an implementation of this patent. As such, it is, you know, implementing the patent from a high level.

Q Was the R400 a graphics processor?

MR. RENAUD: Objection.

A The R400 is a GPU, or was a GPU, so it's a graphics processor, but it's not -- I mean, it's a graphics engine. It's not limited to a GPU. This graphics processor can be used in APUs, and in fact, it's being used in the Xenos program, which is a specialized piece of silicon as well, and those are all the same product, as far as I'm concerned, the same entity of graphics, if you will.

Q So the 400 can be used in a variety of different kinds of chips.

MR. RENAUD: Objection.

A I'm saying -- the 400 -- the R400 is a project name. The graphics core inside the 400 can be applied to, could be applied to any kind of other chips, whether it is an APU, or semi-custom unit, or any kind of device that uses graphics in any way.

Q Is there a unified shader in the R400?

MR. RENAUD: Objection.

A In the R400, there is what we like to call a pixel and vertex unified shader, which is a unified shader that shares the load or shares the work between pixels and vertices.

Q And we talked about that a lot earlier with regard to the sequencer specification, correct?

MR. RENAUD: Objection.

Q And other R400 documents that we discussed.

MR. RENAUD: Objection.

A So restate the question, please?

Q Sure. Strike that.

Is there a arbiter circuit in the R400?

A There are multiple arbiter circuits in the R400. Some of them are in the unified shader pixel/vertex of the R400, and I'm sure there's many others elsewhere.

Q So the pixel/vertex arbiter is in the unified shader in the R400?

MR. RENAUD: Objection.

A The pixel/vertex shader input arbiter is in the R400 design. Correct. That's the way we implemented it.

Q And that was what you worked on inside the sequencer, is that correct?

MR. RENAUD: Objection.

A I worked on the R400 sequencer as a whole, not only the input arbiter, and I defined the way the sequencer was supposed to be working as a whole. This is just a subsection of the R400 sequencer.

Q The arbiter is the subsection of the R400 sequencer, correct?
A I missed the beginning of your question.
Q I'm sorry. The pixel/vertex arbiter, you just said is a subset of the sequencer, is that correct?
A The pixel or vertex input arbiter is a sub-block of the sequencer, of the R400 sequencer as we implemented it, yes.
Q And I believe in your Declaration, which is Exhibit 6, you identified some RTL with regard to the sequencer on page 31. Do you recall that?
A Can you remind me the page number, please.
Q 31, or 0011649.
A Okay. Yes, so according to this, to my Declaration, it says that it is an example of the RTL code that arbitrates between vertices and pixels. And, but I do not recall effectively if this, and we could again look at the RTL code, to make sure if it was indeed the input arbiter or some other arbiter inside the sequencer further down.
Q You mean this code we're looking at right here?
MR. RENAUD: Objection.
A Let me check the -- do you have the Exhibit with

the whole code files so that I can look at it, because without context it's hard to say whether or not if it's the input arbiter or some other arbiter.

Q How many arbiters in the sequencer were responsible for arbitrating between vertex and pixel?

MR. RENAUD: Objection.

A In the -- well, are you referring -- what version of the sequencer are you referring to when you ask that question?

Q Did it change across versions of the sequencer?

MR. RENAUD: Objection.

A The arbitration points changed slightly. I think the concepts stayed the same, but in order for me to give you an accurate answer, I would like to phrase it in terms of a specific version of the sequencer. Is it 0.4 that you want to address?

Q Do you know which version this RTL code came from?

MR. RENAUD: Objection.

A This here says that the RTL code file in question is on page 63 of the Declaration, the SQ thread arbiter, which would indicate to me that this is not the input sequencer. This is some kind of other arbiter further down in the RTL that chooses

between pixels and vertices as the sequencer is trying to execute instructions, either pixel or vertex instruction, of something already loaded into the shader core.

Q And that's why you said in your Declaration that this is just one example in the RTL code, is that correct, on page 30?

A I believe that -- I can't remember exactly what I was thinking at the time. But reading that now, yes, I mean, I can -- like I said, I know of at least three arbitration points in the sequencer, and this is one of them, and in this particular case, this is the thread arbiter which is inside the sequencer, not the input.

Q Is the thread arbiter, the arbiter on the side that we were looking at earlier with regard to the .4 spec? I believe you said there was, inside the sequencer there is -- and I'm referring now to page 175220 of Exhibit 10, which is a top level diagram. Earlier you said the vertex/pixel vector arbitrator was the first step inside the sequencer and that there were two additional arbitrators that were on the sides of that diagram?

MR. RENAUD: Objection.

Q Do you recall that?

A I don't recall specifically saying that, but I mean this picture here, as well as the picture in Exhibit 6, shows all the various levels of arbitration. So on page 11, you have a more clear picture of the sequencer operation because there is actually two of these pictures as it sets here, one for pixels and vertices, and so there is both an arbitration across all of the clauses as stated here, and then the final level of arbitration, and I read from the Declaration here, SEQ arbitrates between the pixel and vertex FIFO, so those are the kinds of arbiters that I believe, if I remember correctly, are described in -- on page 31 of that Declaration.

Q I see. So inside the sequencer there is an initial vertex/pixel vector arbitrator which is shown in Exhibit 10, and then there is also arbitrator at the bottom of the sequencer essentially, which is shown on page 11 of Exhibit 6. Is that correct?

MR. RENAUD: Objection.

A These arbiters can be anywhere in the design basically, but yeah, they are steps of arbitration. Effectively, the sequencer must pick one vertex -- one, sorry, one texture winner, and

one ALU winner, and in order to do that, it needs, in this particular design, which is .4, pick a winning clause of all of the texture clauses, and a winning clause of all of the ALU clauses, and this is showing the hierarchy of how it could do this, but you know, you could presumably also look at all the texture clauses in parallel, and pick one of them, and that would give you the same winner.

Q Was this -- I'm sorry, strike that. Earlier you mentioned the Sequencer Version 2.0, is that correct?

A I believe I mentioned it quite a few times, yes.

Q Is the Sequencer Version 2.0 the same with regard to this arbitration scheme?

MR. RENAUD: Objection.

A Sequencer Version 2.0 had -- has the same goal. It has to pick a winner out of the pixels and the vertices for both the ALU and the texture. The arbitration, however, as you can see in Declaration Exhibit 6, page 19, was done in one arbiter, at least according to this diagram, that was looking at the collection of the reservation stations at the time, and picked an ALU and a texture winner amongst the waves that are on the

vertex reservation station or the pixel reservation stations. So the end result is the same. The implementation defers slightly.

Q What about the Xenos sequencer, does it use the same arbitration scheme?

MR. RENAUD: Objection.

A So I would love to get the Xenos specifications to confirm. They are available, but my recollection is that they are very similar, yes.

MR. ELENGOLD: I will ask the court reporter to please mark Exhibit 14.

(Document marked Exhibit 14 for identification.)

Q And I'll note for the record that Exhibit 14 is AMD1044_226797 through 226851.

Mr. Lefebvre, have you seen Exhibit 14 before?

A Yes, I have seen Exhibit 14 before.

Q What is Exhibit 14?

A Exhibit 14 is, and I read, Xenos Sequencer Specification SQ Version 3.0.

Q Is this the specification you were referring to a second ago that you said would be helpful to confirm whether the Xenos sequencer used the same arbitration scheme as the R400?

A Yes. This is one of the specifications that would be very helpful.

Q Did the Xenos chip use the same sequencer arbitration scheme as the R400?

A So as you can see, on page 8 of 55, or AMD1044_0226804, you can see the picture here is identical as the picture that, for Sequencer Version 2.0 as stated in Exhibit No. 6, the deposition, so that confirms for me the Xenos sequencer was indeed having a very, very similar arbitration schemes than what was used on Version 2.0 of the R400.

Q Why do you say that?

A Because it matches my recollection, and the two pictures are identical, the pictures that are meant to describe the -- the top level pictures that are meant to describe the various operation points of the Xenos Sequencer and the R400 Version 2 Sequencer.

Q So based on comparing the two top level diagrams, you can determine whether or not the two sequencers use the same arbitration scheme?

MR. RENAUD: Objection.

A To give you a much more detailed information, we would need to go and look at the RTL, which I

understand you have, and compare them to guarantee that they are identical. I mean, I only have the specifications right now. You're not giving me a whole lot of documents to work with. Obviously, comparing pictures is not sufficient proof that they're identical, but it is my recollection that they are similar, and also, you know, the pictures are also very similar. So I have no reason to believe that they're different.

Q Earlier you said the R400 was never taped out, is that correct?

MR. RENAUD: Objection.

A That is my recollection, that the R400 was never taped out. Again, you know, I'm sure in the wealth of documents you have, we can go and find strong evidence one way or another. But I don't recall it being ever taped out in my personal knowledge.

Q Do you think there is a document that says somewhere, this was never taped out?

MR. RENAUD: Objection.

A I think it would have probably shown somewhere in some logs that the tapeout occurred on the R400, and so there would have been a trace of at least a GDS netlist present somewhere in the Perforce

depot or otherwise in the Perforce server of the company.

Q Is it hard to tape out from a netlist?

MR. RENAUD: Objection.

A Can you -- what -- I don't understand.

Q Is it a lot of work to complete a tapeout once you have a netlist?

A I see.

MR. RENAUD: Objection.

A In order to do a tapeout from a netlist, you need to have a PD team in place and floor plan the chip.

There is work involved definitely, but it is -- I wouldn't say it's easy, but it's like common in silicon devices. That work is no different for GPUs or for any other kinds of access device, so it's common knowledge as to how to take a netlist and make it into a GDS tapeout file.

Q Do you know approximately how long it would take to tape out product from a netlist?

A What product are you --

Q The R400?

A The R400. So it again, you have all the Perforce logs so you have all the informations back and

forth. I'm sure there's many more presentations like this one, program reviews that would give you insights as to the dates and the process involved. This particular one is kind of stopping short, but --

MR. RENAUD: What Exhibit are you referring to?

A Sorry, Exhibit 9. Page AMD1044_0175196 can give you an appreciation of the planned time period from RTL freeze, which is effectively your netlist, and the first tapeout, which would be the base layer tapeout. Though, you know, here it's stating, forecasting 12/15. So December 15 of '02, and the tapeout would have occurred around February 14 of '03. So roughly two, two months and a half of work planned.

Q At the time you started your work on the R400, were you aware of any other graphics processing systems that used a unified share for both vertex and pixel shader?

MR. RENAUD: Objection.

A At the time I started working for ATI, I was not aware of any other designs that were using a unified shader being able to operate on pixel and vertex, no.

Q When did you first learn of the idea of using a unified shader for both vertex and pixel?

MR. RENAUD: Objection.

A I stated before, I don't recall the exact date. I know discussion took place between myself Andy Gruber, Andi Skende, and Steve Morein, and there is evidence of the first specification proposal produced by Steve around November 13, 2000 or thereabouts.

So again, there's probably a lot more documents that we could dig to refine these dates, but that would have been around these dates that a discussion occurred on the subject.

Q What was the first company or person that you were aware of outside of ATI to discuss the idea of having a unified shader for both pixel and vertex shading?

MR. RENAUD: Objection.

A What do you mean? Can you say what you mean by "discuss"?

Q Sure. Are you aware of anyone outside of ATI having had an idea to use a unified shader for both vertex and pixel?

A Having ideas. I know, for example, that Qualcomm has a unified shader because they license it from

us. I think there is another company too. I am not, you know, going at the literature to try to find which products may or may not have a unified shader, so I don't really know which ones would or would not have one.

Q What's the first product you know of that was available commercially in the marketplace that used a unified shader for both pixel and vertex shading?

MR. RENAUD: Objection.

A First products that I know of is the Xbox 360 which was manufactured by Microsoft. Well, the IP was given to Microsoft by AMD, and Microsoft, I understand, actually manufactured the chip.

Q Do you know why the R400 program was cancelled?

A Again, there is probably a wealth of information that can be derived that is available, and that would be very helpful to refresh my memory.

Q Do you know?

A I was a junior engineer back then, but I knew there were some problems with the render back end blocks not meeting performance and schedule. And also, a large amount of work was needed to enable the Xenos chip. So I guess at some point a resource call got made and positioned the teams

over to the Xenos program to make sure that the customer for which we had a contract with, was satisfied with the product.

Q Do you know whether others copied the unified shader idea that you, and Mr. Morein, and Mr. Gruber, and Mr. Skende had back in 2001?

MR. RENAUD: Objection.

A I have never searched for, you know, any products outside of AMD, so I don't know. And can you define what you mean by "copy"? I mean --

Q I mean -- let me come at this a different way then for you.

Are you aware of the first public disclosure by ATI of the idea of using a unified shader for graphics processing?

A So I am aware that one former employee, Mike Dogget, did a presentation on the R400 unified shader at a conference. Whether or not this was the very first public announcement of the unified shader of the R400, I am not sure, but there is at least that.

Q Do you know when that presentation was?

A No, I do not, but it's probably -- I know it was delivered to you, so if we want to look at the date, and again, look, put the document in front

of me, we'll look at it, we'll confirm.

Q Have you ever received any awards or praises for your work that led to the unified shader patents?

A Awards? I mean there is -- at AMD there is an inventor award whenever you publish a patent. And that is the extent of what I received as far as this particular patent.

Q What is that award?

A It changed over the years. I believe it's around a thousand dollars to be spread amongst the inventors.

Q Do you still receive that award each time a new patent issues with you listed as the inventor?

A I still receive an award. I don't even check what the amount of money is because it's not really relevant to me, but there is still an award for every patent filed by inventors to be, again, amount of money to be spread amongst the inventors.

Q Do you receive any other compensation with regards to being an inventor at AMD?

A You receive a small flag that you can put on your desk, but that's the extent of the awards that I can think of.

Q Does the flag say "Inventor" on it?

A The flag used to say Date and Patent Granted, white flag, and then black flag said Date and Patent Issued. They don't issue the flags anymore, as far as I know.

Q Are you a named inventor on any patents other than the unified shader patents?

A Yes.

Q How many other patents approximately?

A Do you count all of the derivatives and -- because for example, this patent, which we -- the initial patent was the '871, then it turned into the 486 -- the '846. It turned into another number here, the '454. So what --

Q So if we broadly classify all of the ones that share the '871 specification --

A As one?

Q -- as the unified shader patents, are you a named inventor on any other patents?

A Yes. Quite a few of them.

Q Have any of them been involved in litigation?

A I'm not typically aware, but I can say that at least another one of mine was involved in litigation because I was deposed on it by Mr. Nese. It was the patent -- let me find the actual.

I believe, if my memory serves, I think it was the patent, as stated here on Exhibit 4, page 3, the 7,742,053 patent. And I can go into the deposition to make sure and to -- let me just check that actually.

Q Any other patents that you know of that you were a named inventor on that have been in litigation other than the '053 patent?

MR. RENAUD: Objection.

A I only got deposed on that one other patent. I am not -- I don't know if there is any other litigation or otherwise on the other patents that I have been named inventor on.

Q When you first talked to Steve Morein about using unified shader in the R400, did you think it was a surprising idea to use a unified shader?

MR. RENAUD: Objection.

A It was definitely new. I mean, that was the first time that anybody would be trying to do something like that, and actually, even inside AMD it caused a lot of friction as to whether or not it was a good idea or not, at the inception.

Q Why?

A Because it was so novel and so unusual basically.

Q What were the down sides?

A So at least one of the issues we had to work with, or make sure that we did not degrade the performance on, was the fetching of the vertices. In the initial inception, if I remember correctly again, and we should definitely bring the specs here so we can look and take a deeper look, I believe the vertices were supposed to be fetching directly from the texture cache size, and there was an issue, a possible issue where the two types of traffic could trash one another, and so we decided to mitigate that by having a separate vertex cache dedicated to vertices to make sure that we had the best chances of having a very good product in the sense of the performing product and a small product.

Q How did a vertex cache solve that issue?

MR. RENAUD: Objection.

A The vertex cache, by having a separate cache for the vertices, prevented any kind of cache trashing, meaning a line from the vertices evicting a line from the pixels, and so mitigated the issue of the two types of traffics colliding into one another going to memory.

Q Are there any other problems you ran into with implementing to a unified shader?

MR. RENAUD: Objection.

A Well, I mean, the R400 is a product, so we ran into all sorts of, you know, possible issues. I can't really recollect them all. Again, you have all the Perforce logs. We can go and look at all the changes. I mean, all of these changes are to address a particular issue or to fix a small problem. I can't -- there definitely were issues, and if it was easy, everyone would do it immediately. I mean --

Q Any other substantial issues that you can remember other than the vertex cache?

MR. RENAUD: Objection.

A No, I don't remember any, you know, substantial issues. I mean most of the -- most of the things we worked on were like small nitpicks and trying to get to the machine to really operate flexibly to the best it could.

Q So I know earlier when you came in from the break, we talked afterwards about the call you did with Pam and David. I just wanted to make sure I gave you a chance. Was there anything else you wanted to add to your testimony today with regard to things you've learned during the breaks with your counsel?

MR. RENAUD: Objection.

A So I mean the things I learned during the break were based on discussions with Pam and Dave Christie, not with counsel. Counsel was in the room, but I did the discussion and I did the learning, and I looked at the specification.

Q And I don't mean to cut you off, but I believe earlier your counsel mentioned, when we were talking about your other conversations when Pam and/or David was involved, they were with the legal department and it was at the direction of counsel, is that correct? I just don't want to push you into a place where you're breaching a privilege.

MR. RENAUD: Yeah, let's put it simply. I allowed a lot of latitude to explore what was done to collect documents and to enhance his awareness today.

MR. ELENGOLD: During the break.

MR. RENAUD: During the break, but there are things that both Dave and Pam do that are privileged and confidential. Shouldn't say privileged and confidential. Privileged or work product.

In this instance, I made the decision that

his inquiries as to the documents that they produced were not privileged and should be the subject matter of the deposition.

MR. ELENGOLD: I appreciate all that. Just for purposes of time, that wasn't my question. But just so you understand, when I say counsel, I'm including people within the AMD legal department just so you understand.

MR. RENAUD: Oh, I understand now what you're saying. Sorry, go ahead.

MR. ELENGOLD: Yeah.

Q So you distinguish them from counsel, and I just wanted to make sure for you to understand for purposes of privilege, that I'm not intending to exclude your people in the legal department at AMD from counsel, when I say, you know.

A Okay, so --

Q So going back again, is there anything you would like to add to your testimony today based on other things that you may have learned?

A So like I said, I mean, as a designated witness from AMD, I learned during that break that there was a wealth of documents that was available and, you know, I misrepresented that the only document of relevance was Exhibit 6 which was -- it is a

document, and it does provide a view of the Perforce depot, but not an exhaustive view, but I was also made aware by Dave and Pam that there were many more documents submitted that were outside of the Perforce depot, such as the test logs, the test names, the source code -- well, actually, the source code was in the depot, but it got provided in various snaps, presentations which were not in the directories that I described in my Exhibit 6 testimony, as well as all of the IKOS initiative, which is definitely not in that testimony.

Q So I believe you've now testified about all those things, correct?

A Well, to the extent --

Q Is there anything else that we haven't talked about today that you would like to add to supplement your testimony?

A There is probably way more, yes. There is a wealth of documents, and I can't remember them all. I mean, if you want to talk about them, I know that there's hundreds and hundreds of documents that were provided. There's also hundreds and hundreds of people at AMD that worked on the R400 project. So --

Q Are there any in particular that are still at AMD that you think would be knowledgeable about the subject matter we talked about today?

MR. RENAUD: Objection.

A You want me to name people that were working? Okay. Sure. I mean, I know of at least Mark Fowler, Mike Mentor, which were senior architects back then. There's a lot of other people, like Randy Ramsey, which is an RTL designer that works in Orlando that still works at AMD. I mean --

Q Why did you not talk to those people in preparing for your testimony today?

MR. RENAUD: And I'll instruct you not to answer to the extent that reveals an attorney/client communication, but you can otherwise answer.

A So I am aware of the specifications and the design of the R400. I know what they are. I am knowledgeable in that respect, and so I personally don't need to talk to Mike Mentor or Mark Fowler about the R400 design, which I know. I needed to talk to Dave Christie and Pam to get an appreciation of the documents that were submitted but, you know --

Q Is there anyone else at AMD that you would want to

talk to, to get additional information to supplement your testimony today?

MR. RENAUD: Objection.

A There's hundreds and hundreds of people at AMD that worked on this program, so you know, we can talk to each and every one of them. They would probably have each their own view of what occurred at any of these dates. You know, at this point, I could talk to everyone that was involved and that probably would help me, but in the interest of time, do you really want to do this? I mean --

MR. ELENGOLD: Okay. Let's go off the record.

MR. RENAUD: Sure.

VIDEO OPERATOR: The time is 5:38 p.m. We're off the record.

(Off the record.)

VIDEO OPERATOR: The time is 5:53 p.m. We're back on the record.

Q I'm going to hand the witness Exhibit No. 15.

(Document marked Exhibit 15 for identification.)

Q Mr. Lefebvre, have you seen this document before?

A I don't remember having seen this document before, no.

Q Do you know what Exhibit 15 is?
A Can you point me to it? I mean where is it --
Q Sure, if you look at the title, and if you read the title into the record, that might help.
A Yeah, okay. Complainants Advanced Micro Devices, Inc. and ATI Technologies ULC's First Supplemental Responses and Objections to Respondents LG and Vizio's First Set of Joint Interrogatories (Nos. 5-8, 12, 18, 34, 49, 51-52, 55, 65-66, 70-71.
Q Do you know what that means?
A Talks about joint interrogatories, but further than that --
Q Do you know what an interrogatory is?
A Not really. Can you educate me?
Q Sure. You were designated today on topic 86 which is just respondent's -- responses, complainants' responses, so ATI and AMD's responses to discovery requests, written discovery from LG and the other respondents, and so I just wanted to ask you a couple quick questions about this document which -- let's try, if you can turn to page 95, I'm going to ask you to look at Interrogatory number 49.

Again, you are only designated, my understanding is, this topic with regard to your

other topics; so conception, reduction to practice.

A Okay. What part of the --

Q Look at Interrogatory number 49, do you see that?

A Yes, I see that.

Q And you're welcome to read it. But my question is going to be, do you understand Interrogatory number 49 to be asking for the information regarding conception and reduction to practice for the patents that are at issue in this case?

A Okay. I read through it.

Q Can you look at the response on pages, bottom of page 96 and top of 97 which says, Response No. 49, and then in parentheses (6/5/2017). I think you just said you read that. Do you see that this is the most recent response to Interrogatory number 49?

A So 6/5, okay. I did not read that paragraph, so can I read that paragraph?

Q Absolutely. Response no. 49.

A You want me to read it out loud?

Q No, you can just read it to yourself.

A Okay.

Okay. I read through it.

Q Okay, do you understand that response to be an

accurate reflection of the facts that AMD and ATI have identified with regard to Interrogatory 49?

MR. RENAUD: Objection.

A I see a lot of text with AMD prefix and numbers, and I don't know what they are, what these involved.

Q Sure. Well, just because you were designated on the subject. Do you have any reason to believe that Response no. 49, 6/5/2017 on this document, is not a complete and accurate response from AMD and ATI?

MR. RENAUD: Objection.

A Well, not knowing who made that comment and what these files are, I don't know if it's accurate or not, or what it contains. I mean.

I have a hard time understanding what I can tell you on this.

Q So you don't know.

A No, I don't know. I don't know. I don't know what these files are, if they're even files and what they represent and -- I don't know.

Q Let's look at Interrogatory number 51 on page 98. After you've read that, my question is, do you understand Interrogatory number 51 to be asking for the facts regarding conception and reduction

to practice for the patents at issue in this case.

A That's what it says, yes. As far as understanding per se what actual, these terms really mean in the sense of the law, again, I'm an engineer, so I can read the text. I see, I see the text on the page, yeah.

Q Okay. And then if you look at page 100, you'll see similarly a response, number 51, 6/5/2017, do you see that?

A This, okay. This was the response to --

Q Interrogatory number 51.

A -- the question.

Q Yes.

A Okay.

Q I have the same question as before, do you understand this to be a complete and accurate response from AMD and ATI?

A Well, yeah, so from my conversation with Pam and Dave Christie, I understand that there is indeed an investigation going, and people are looking into that subject.

Q Okay. And for Interrogatory number 52, which is right below that on page 100, please go ahead and read that, and do you understand that to be asking for additional facts regarding conception and

reduction to practice?

A Is there a response you want me to read?

Q Well, for my question, do you understand what Interrogatory number 52 generally says, and that it relates to conception and reduction of practice to the patents?

A Yeah. "Identify all persons involved in conception, reduction to practice, prosecution of the patent application, preparation of the patent application or any part thereof, custodian," which I don't know what it means, "keeper of the record related to the same, including name, title, current employer, current contact information of persons, descriptions of the dates and the substance of their involvement, and specify who is most knowledgeable regarding the same."

Q Okay. Can you turn to page 102 where there is the response to number 52, 6/5/2017.

A Yes, I am on that page.

Q And you see that response?

A Again, big list of AMD numbers and --

Q We call those Bates numbers.

A Page.

Q Yeah, page numbers, that's right, that's what they are.

A Okay.
Q Do you understand the Response no. 52 to be accurate and complete?
A I can't really comment on, again, on the completeness of all this not knowing what is being discussed here. It's way too summarized for me to provide any kind of opinion.
Q And you didn't do any preparation to testify today with regard to those responses, is that correct?
A Well, I mean, I prepared for today's testimony as far as the steps or the amount of work that went in on the R400 to prove that it was, you know, diligently working and trying to make a product for a date, and talked about, you know, various people which we discussed; Dave Christie and Pam Horn, and reviewed the Perforce logs, the documents. So this is the, the preparation that I did for this, right.
Q I meant specific to these discovery responses, did you do any preparation to testify on those today?
A I don't know what these are, so no.
Q So if I represent to you that this is the most recent set of discovery responses that we've received from AMD and ATI, which is Exhibit 15, so for Interrogatory number 49, 51 and 52, you have

no reason to doubt that AMD and ATI's responses are wrong, right, or I'm sorry, you have no reason to doubt that they're accurate and correct, right?

MR. RENAUD: Objection.

A These response -- I mean, I can't tell what these are, so I mean, unless you put in front of me what these documents are, and I can look at them, I can't formulate an opinion either way. I don't know what this is.

Q Well, these are the documents that AMD and ATI have represented that that list are relevant to these topics as of today or, you know, until they supplement it again, so as of 6/5/17. My question was, do you understand or do you have any reason to believe that these are incorrect, these responses?

MR. RENAUD: Objection.

A Well, I mean, if they were provided by AMD, and you know, counsel reviewed them and appended them to this document, I don't have any reason to believe these are not correct and accurate, but I really want to state that I have no idea what these are, so I can't really formulate a personal opinion on this. I mean, I'm relying on AMD and counsel.

MR. ELENGOLD: Okay. And so I have no further questions, and sort of per our earlier discussion where I said I would try to keep it to seven hours in light of your need to have an appointment tonight, Mr. Lefebvre, so I understand that and we'll cut it off; although I will say that, you know, with regard to the information that was disclosed, an hour and a half left in the day, on the deposition, that changed your prior testimony, we reserve the right to, once we learn more about that, recall this witness on those subjects, limited to those subjects that changed prior testimony and came up late in the day.

MR. RENAUD: All right. Well, we'll certainly take that under advisement. I will say that the witness throughout the day had requested documents to help him answer questions of which there are quite a few, and during the day, it was a few hours in the depo before they were put on the table. You can use that time any way you'd like, but my point of view is you had ample opportunity to question the witness, but we're open to further dialogue about the subject matter, and appreciate you respecting the seven hour limit on the deposition. Thank you for your time.

MR. ELENGOLD: Per the parties' agreement, I'm happy to do the seven hours, like I said, but again, just to note, I don't think any of those documents that we went through during the day, to your point, are relevant to this subject of changing testimony late in the day in the deposition.

MR. RENAUD: Look, the open-ended questions you were asking about, are there any other documents, does the company have any awareness --

MR. ELENGOLD: I think now you're testifying. So I don't think we really need to go through that.

MR. RENAUD: I'm just going to say on the record that I think you mischaracterized the change in testimony. There was no change in testimony. Like any other 30(b)(6), the witness has the burden to produce information for an entire corporation, and on more than one occasion during a break, he tried to go complement his earlier testimony on subject matters you asked about for which he said he did not have full awareness, so at the end of the day, if you'd like to talk about additional time with this witness or another witness to manage the issue you've

addressed, we're happy to have that conversation.

MR. ELENGOLD: Well, that's my question, is I don't know that it's necessary because again, I think we have a complete record based on what has been put in to date. I guess my point again is just that, to the extent that we're trying to keep it to seven hours, I'm just noting for the record that we're doing that, and we're doing that in light of your request and the parties' agreement to do that with individual deponents, but you know, again, I think you're mischaracterizing things quite a bit there, but I appreciate if you want to represent there was no change in testimony, I think that's fine, and I'm happy to, you know, let that go and we both said our piece.

MR. RENAUD: Okay. We're happy to take it up off the record. Thank you.

VIDEO OPERATOR: The time is 6:08 p.m. This concludes the deposition of Laurent Lefebvre. We're off the record.

(Whereupon the deposition concluded at 6:08 p.m.)

C E R T I F I C A T E

COMMONWEALTH OF MASSACHUSETTS
MIDDLESEX, SS.

I, Lisa McDonald Valdario, Registered Professional Reporter and Notary Public, in and for the Commonwealth of Massachusetts, do hereby certify that:

LAURENT LEFEBVRE, the witness whose deposition is hereinbefore set forth, was duly sworn by me, that I saw a picture identification for him in the form of his NEXUS government issued ID, and that the foregoing transcript is a true and accurate transcription of my stenotype notes to the best of my knowledge, skill and ability.

I further certify that I am not related to any of the parties in this matter by blood or marriage and that I am in no way interested in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand and notarial seal this 1st day of July, 2017.

_____
Lisa McDonald Valdario, RPR, RMR
Notary Public
My commission expires: June 15, 2018

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In The Matter Of Certain Graphics Systems v. Laurent Lefebvre

ACKNOWLEDGMENT OF DEPONENT

I, _____, do hereby certify that I have read the foregoing pages and that the same is a correct transcription of the answers given by me to the questions therein propounded, except for the corrections or changes in form or substance, if any, noted in the attached Errata Sheet.

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