

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

REALTEK SEMICONDUCTOR CORP.,

Petitioner

v.

ATI TECHNOLOGIES ULC

Patent Owner

Case No.: IPR2023-00922

U.S. Patent No. 8,760,454

Issue Date: June 24, 2014

Title: Graphics Processing Architecture Employing a Unified Shader

**PETITIONER REALTEK SEMICONDUCTOR CORP.'S REPLY TO
PATENT OWNER'S PRELIMINARY RESPONSE**

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PETITIONER’S EXHIBIT LIST

Exhibit #	Reference Name
1001	U.S. Patent 8,760,454 to Morein et al.
1002	Prosecution History of U.S. Patent 8,760,454
1003	Declaration of Hanspeter Pfister, Ph.D.
1004	Curriculum Vitae of Hanspeter Pfister, Ph.D.
1005	U.S. Patent 7,038,685 to Lindholm et al. (“Lindholm ’685”)
1006	U.S. Patent No. 7,015,913 to Lindholm et al. (“Lindholm ’913”)
1007	John Amanatides and Edward Szurkowski, <i>A Simple, Flexible, Parallel Graphics Architecture</i> , In Proceedings of Graphics Interface at 155-160 (Canadian Information Processing Society 1993) published in Proc. Graphics Interface ’93 in May 1993 (“Amanatides”)
1008	Les Kohn and Neal Margulis, <i>Introducing the Intel i860 64-bit Microprocessor</i> , IEEE, Volume 9, Issue 4, pages 15-30, August 1989 (“Kohn”)
1009	Harald Selzer, <i>Dynamic Load Balancing within a High Performance Graphics System</i> , In Proceedings of Rendering, Visualization and Rasterization Hardware (Eurographics' 91 Workshop) at 37-53 (Springer-Verlag 1993) published in 1993 (“Selzer”) [Library of Congress]
1010	Stuart Fiske and William J. Dally, <i>Thread prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors</i> , In Proceedings of First Symposium on High-Performance Computer Architecture, 1995 at 210-221 (IEEE 1995) published in 1995 (“Fiske”)
1011	IEEE Xplore bibliography page for Fiske, <i>Thread prioritization: A Thread Scheduling Mechanism for Multiple-Context Parallel Processors</i> , visited on May 11, 2023
1012	Declaration of Gordon MacPherson re Authentication of Fiske (May 11, 2023)
1013	IEEE Xplore bibliography page for Kohn, <i>Introducing the Intel i860 64-bit Microprocessor</i> visited on May 11, 2023

1014	Declaration of Gordon MacPherson re Authentication of Kohn (May 11, 2023)
1015	Initial Determination on Violation of Section 337, <i>Certain Consumer Electronics and Display Devices With Graphics Processing and Graphics Processing Units Therein</i> , 337-TA-932 (October 9, 2015)
1016	Harald Selzer, <i>Dynamic Load Balancing within a High Performance Graphics System</i> , In Proceedings of Rendering, Visualization and Rasterization Hardware (Eurographics' 91 Workshop) at 37-53 (Springer-Verlag 1993) published in 1993 (“Selzer”) [University of California, Berkeley, Library]
1017	Redacted Deposition Transcript of Andrew E. Gruber, taken March 17, 2015, in ITC Case No. 337-TA-932

Pursuant to the Board’s authorization of October 6, 2023, Petitioner submits this Reply to Patent Owner’s Preliminary Response (“POPR”) to address the material deficiencies and omission of key evidence from the POPR. Once the withheld evidence is properly considered as part of the record, the POPR and Mangione-Smith declaration clearly do not show prior invention relevant to Ground 1 of the Petition.¹ The subject matter in the omitted ATI 30(b)(6) deposition transcript also makes clear that a previous Federal Circuit decision did not decide the relevant issue here regarding whether the register allocation scheme in the Challenged Claims was conceived and reduced to practice. Much like the Mangione-Smith declaration filed with the POPR, it was not addressed.

Petitioner’s Reply addresses three points: 1) irrelevance of the prior Federal Circuit decision, 2) deficiencies in the Mangione-Smith declaration related to the omitted evidence and differences between the Challenged Claims and claims in related patents, and 3) the omitted inventor and 30(b)(6) deposition transcript that contradicts the POPR and declaration and dooms Patent Owner’s position.

I. The Previous Federal Circuit Decision Is Not Controlling

The Challenged Claims include elements that were not addressed by the

¹ Patent Owner’s alleged prior invention argument has no bearing on Grounds 2 and 3, which are not addressed in this Reply.

Federal Circuit’s decision of a related patent (U.S. Patent No. 6,897,871) in *ATI Techs. ULC v. Iancu*, 920 F.3d 1362 (Fed. Cir. 2019). In addition, the Federal Circuit and the PTAB did not address conception in that case because it was not challenged. Accordingly, the Federal Circuit decision does not dictate, much less address the issues presented in, this proceeding.

First, the Challenged Claims (using claim 1 as an example below) include limitations related to the allocation of register blocks to be used for performing either vertex or pixel operations:

'871 Patent

1. A graphics processor, comprising:
an arbiter circuit for selecting one of a plurality of inputs in response to a control signal; and
a shader, coupled to the arbiter circuit, operative to process the selected one of the plurality of inputs, the shader including means for performing vertex operations and pixel operations, and performing one of the vertex operations or pixel operations based on the selected one of the plurality of inputs, wherein the shader provides a appearance attribute.

Challenged Claim 1 – '454 Patent

1. A method carried out by a unified shader comprising:
performing vertex manipulation operations and pixel manipulation operations by transmitting vertex data to a general purpose register block, and performing vertex operations on the vertex data by a processor within the unified shader unless the general purpose register block does not have enough available space therein to store incoming vertex data; and
continuing pixel calculation operations that are to be or are currently being performed by the processor based on instructions maintained in an instruction store until enough registers within the general purpose register block become available.

The '871 patent claims and the Federal Circuit decision mention nothing about allocation of or use of register space as a predicate for determining which type of operation to perform (*e.g.*, vertex or pixel operations). *See also* Ex. 1017 at 168:5-23 (ATI witness confirming that the '871 patent did not cover dynamic register allocation). Nor do the '871 patent claims or the Federal Circuit decision address the failure of ATI to conceive of or reduce to practice the “dynamic register allocation” in the R400. Importantly, Patent Owner’s Preliminary Response does

not address the differences in the claims, and to the extent it attempts to do so in its Sur-Reply, this factual dispute should be resolved through a full proceeding.

Second, conception was not contested in the '871 patent IPR proceeding, and therefore, it was not addressed by the PTAB or the Federal Circuit. This is a critical distinction because ATI did not conceive of the use of register allocation in the context of the R400 or any other project, as recited in the Challenged Claims, prior to their effective filing date. Patent Owner failed to address this distinguishing factor in its Preliminary Reply. At most, ATI identified a problem, as confirmed by its witness testimony, but it did not identify a solution, which is required to establish prior inventorship. *Singh v. Brake*, 317 F.3d 1334, 1341 (Fed. Cir. 2003) (finding no conception for an unworking embodiment because “[e]ven if the entry expressed the problem, it did not provide the solution.”).

The only court decision to address the lack of conception and reduction to practice related to the R400’s register allocation was the determination of the International Trade Commission in 337-TA-932. *See* Petition at 15-16. Indeed, the very evidence that Patent Owner withheld from its Preliminary Reply is the same evidence relied upon by Judge Pender in the 932 Investigation to find the lack of an “operative and complete invention” that is required to prove conception. Patent Owner withheld that testimony because it contradicts any argument it could attempt regarding conception and reduction to practice.

Accordingly, any attempted reliance on the Federal Circuit decision would fall short of addressing the specific, and different, claim elements at issue here.

II. The Mangione-Smith Declaration Does Not Address the Differences Between the Challenged Claims and the '871 Patent IPR Decision

Patent Owner relies upon a declaration from Dr. Mangione-Smith to support its claim to previous conception and reduction to practice. Specifically, Dr. Mangione-Smith asserts that the ATI “inventors...created an implementation of the R400 in source code, e.g., emulation code and RTL.” Ex. 2001, ¶196. But the Mangione-Smith declaration does not perform any analysis of the R400 RTL code and relies only on the '871 IPR proceeding and a declaration from Dr. Wolfe. Ex. 2001 at ii (citing Ex. 2002, the Wolfe Declaration). This leaves the Mangione-Smith declaration deficient for at least three reasons.

First, the Mangione-Smith declaration relies solely on draft specifications for the R400 while ignoring the corresponding RTL code and omitted inventor testimony. As ATI’s witness, Andrew Gruber, previously testified, “RTL is probably the best guide” and “anything not in the RTL code is not in the GPU.” Ex. 1017 at 52:11-53:3 (testifying that RTL is more definitive than the draft ATI specifications relied upon by Dr. Mangione-Smith). And Dr. Mangione-Smith cannot credibly claim ignorance of this prior testimony. That is, Dr. Mangione-Smith was one of ATI’s experts in the 1318 Investigation, and therefore, had access to the Gruber deposition transcript because it was marked as an exhibit and

produced by ATI. Dr. Mangione-Smith's declaration in this IPR proceeding puts on blinders and presents an expert opinion that knowingly contradicts the sworn testimony of an ATI inventor on the '454 patent. The Mangione-Smith declaration should be given no weight, especially in the absence of a more complete evidentiary record that may be developed following institution.

Second, Dr. Mangione-Smith's reliance on the R400 as being continuous with the R500 and Xenos projects at ATI is flatly contradicted by Mr. Gruber. His testimony confirmed that there was no "seamless extension" from the R400 to the other projects and that there were "substantial changes" in the R500 and R600, which became Xenos. Ex. 1017 at 7:23-8:22; *compare with* Ex. 2001 at 208 (Mangione-Smith labeling R400 to Xenos as "seamless extensions."). Indeed, the "sequencer," which is the component claimed in the '454 Challenged Claims, "had substantial changes" and even had different teams working on it. Ex. 1017 at 9:1-10. Even worse, as Mr. Gruber testified, the R400 was never taped out and the dynamic register allocation never worked. Ex. 1017 at 104:20-25. Dr. Mangione-Smith ignored all of this testimony, which flatly contradicts the conclusions set forth in his declaration citing cherry-picked documents.

Third, while the Mangione-Smith declaration ignored the contents of the R400 RTL code (as it needed to do in order to contradict the Gruber testimony), the Wolfe declaration from the '871 proceeding actually reviewed RTL code and

concluded that the R400 had a **fixed** vertex priority scheme that did not depend on any amount of data in storage. But that is the opposite of what is required by the claims of the '454 patent. Accordingly, to the extent the Mangione-Smith declaration was incorporating by reference the opinion from Dr. Wolfe in the '871 IPR proceeding (which the declaration purports to do), then Patent Owner's expert testimony conclusively establishes that ATI did not previously conceive of or reduce to practice what is required by the Challenged Claims.

III. The Withheld Gruber Transcript Demonstrates a Lack of Prior Conception and Reduction to Practice

All the Challenged Claims require a form of memory allocation that dictates whether vertices or pixels will be processed by the claimed shader. AMD's 30(b)(6) witness, and co-inventor on the '454 patent, Andrew Gruber, provided testimony in the 932 ITC investigation—which was not considered in the '871 IPR proceeding or by the Federal Circuit—demonstrating that the claims of the '454 patent were not conceived or reduced to practice as part of ATI's R400 project. Ex. 1017. Petitioner discussed Judge Pender's ruling that relied on Mr. Gruber's testimony in the Petition at pages 15-16. ATI is well-aware of Mr. Gruber's testimony and is in possession of Mr. Gruber's deposition transcript from the 932 Investigation, as it was produced and cited as an exhibit by ATI in a recent ITC Investigation. Yet, ATI produced over 200 exhibits with its Preliminary Response,

including *another* deposition transcript from Mr. Gruber, but conspicuously omitted Mr. Gruber's testimony from the 932 Investigation. This was no mistake.

The Challenged Claims require a register allocation method that was never conceived of in the R400 project and never made functional for use in Xenos. Ex. 1017 at 103:11-104:25. Indeed, Xenos used a fixed register system that is *not* the dynamic method in the Challenged Claims. *Id.* at 14:18-15:10. Mr. Gruber's testimony could not be clearer that, *even years after the filing of the parent application to the '454 patent in 2003*, the register allocation scheme did not work:

20 Q. So when the first silicon was made
21 for the Xenos chip, the dynamic register file
22 allocation method did not function properly,
23 correct?
24 MR. PAIGE: Object to the form.
25 A. Correct.

Ex. 1017 at 104:20-25 (discussing the first tapeout of Xenos in late 2004/2005).

Mr. Gruber went on to explain how this “aspirational” dynamic register allocation method included flaws that prevented it from being functional and may have never come close to working in any form until the later R600 (years after the patent filings). *Id.* at 104-107 (further testifying that the R400 “never got to the point” of even testing the flawed dynamic register allocation). Instead of being functional, the R400 and Xenos used a “fixed” register space widely available in the prior art that simply dedicated 50 percent of the register space to vertices and 50 percent of the register space to pixels. *Id.* at 107:10-16. With respect to the date that ATI

(including Mr. Gruber as a co-inventor) allegedly conceived of the register file allocation in the '454 patent, Mr. Gruber testified that “I cannot provide a date” and it may have been in 2002. *Id.* at 115:115:19-116:8. Again, Mr. Gruber’s testimony contradicts the Mangione-Smith declaration and POPR.

Mr. Gruber’s testimony regarding the RTL code, which the Mangione-Smith declaration ignores and does not analyze, further demonstrates that the R400 (and Xenos) cannot be an operative conception, much less a reduction to practice, of the Challenged Claims. That is, Mr. Gruber testified that in the R400, the dynamic register allocation mode was nonfunctional and the “static mode” did not utilize any priority and could not utilize any allocation of shared resources as required by the Challenged Claims. *Id.* at 167:13-21. Thus, there was no priority given to vertex or pixel threads based on the allocation of register space as required by the Challenged Claims. Dr. Mangione-Smith again ignores this relevant testimony and his declaration is contradicted by the unsubmitted evidence.

By producing a different Gruber deposition transcript that did not address the register allocation scheme of the Challenged Claims, the POPR sought to hide ATI’s failure to invent earlier than Petitioner’s Ground 1 prior art from NVIDIA. The Federal Circuit also did not have this Gruber transcript, but also did not need to decide the issue of whether ATI conceived of the claimed register allocation method. ATI did not, and the Petition should be instituted as to Ground 1.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

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