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ATI and NVIDIA Proclaim Different Graphics Processors Architecture Goals

ATI Says Unified Rendering Engine – the Way to Go, NVIDIA Disagrees

by **Anton Shilov**
12/23/2004 | 07:55 AM

While particular approaches in graphics processing units design have been pretty different for leading computer visual companies ATI Technologies and NVIDIA Corp., in future the architecture of GPUs from the firms may be fundamentally different, as executives from both companies proclaim different approaches for chip internal architectures.

NVIDIA Disagrees with ATI Technologies

ATI Technologies' developer relations manager Richard Huddy said last month during a conference in London, UK, that the company's future visual processing units will feature unified pixel and shader processing. While he declined to elaborate on the timeframes for such chips, he said unified pixel and vertex data processing is a required capability for Windows Graphics Foundation 2.0 that comes out together with Microsoft's next-generation operating system called Windows Longhorn. On of the benefits the unified approach brings is ability to dynamically allocate chip resources depending on the demand for pixel and vertex processing, Mr. Huddy said. Another one is simplified software development.

NVIDIA Corp.'s chief architect David Kirk called the unified graphics engines as an implementation detail, not a feature, but admitted the unified architecture would be nice for programmers, who would have one instruction set for vertex and pixel shaders.

"It's not clear to me that an architecture for a good, efficient, and fast vertex shader is the same as the architecture for a good and fast pixel shader. A pixel shader would need far, far more texture math performance and read bandwidth than an optimized vertex shader. So, if you used that pixel shader to do vertex shading, most of the hardware would be idle, most of the time. Which is better – a lean and mean optimized vertex shader and a lean and mean optimized pixel shader or two less-efficient hybrid shaders? There is an old saying: 'Jack of all trades, master of none'," Mr. Kirk said in an interview with [ExtremeTech](#) web-site.

ATI: Bridging Today and Tomorrow

Not much is known about the architecture and capabilities of the code-named R520 product scheduled for release in Q2 2005 that was initially referred as the R500. What is clear now is that the new graphics chip will

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sport Shader Model 3.0 – pixel shaders 3.0 and vertex shaders 3.0 – bringing additional programming capabilities to ATI's future graphics processors as well as some other innovations.

ATI's R5xx architecture will not resemble that of the previous generation products and NVIDIA's GeForce 6 architecture known as NV4x, particularly ATI will implement efficient flow-control, a crucial feature for pixel shaders 3.0, that will not bring speed penalty it does on existing SM3.0 hardware, according to sources. The future of the graphics hardware lies in higher number of ALUs ops per texture ops, unified pixel and vertex shaders as well as some other requirements of Microsoft Windows Longhorn operating system, such as virtualisation and context switches. While ATI agrees on the long-term goals for its roadmap, it does not name feature-set of actual products and says all the architectural changes will be implemented gradually, not at once.

Some sources claim that the R500 is a code-name of ATI's graphics processor that will be submitted for Microsoft's next Xbox console. The shader core of the R500 was reported to have 48 Arithmetic Logic Units (ALUs) that can execute 64 simultaneous threads on groups of 64 vertices or pixels. ALUs are automatically and dynamically assigned to either pixel or vertex processing depending on load. The ALUs can each perform one vector and one scalar operation per clock cycle, for a total of 96 shader operations per clock cycle. Texture loads can be done in parallel to ALU operations. At peak performance, the GPU can issue 48 billion shader operations per second, it was said.

The R520 is also expected to feature advanced memory interface, presumably supporting GDDR4 memory.

NVIDIA: Plans Unclear

While NVIDIA remains extremely tight-lipped over its future products, it is known that the company is readying its code-named NV47 visual processing unit, a massively revamped GeForce 6 architecture with 24 pixel pipelines. The NV47 is expected to be released sometime in Spring, 2005, but it is unknown whether NVIDIA is ahead, or behind ATI's R520 product. NVIDIA also reportedly plans to release a chip called NV48 in Q2 2005.

The status of NVIDIA's future architecture code-named NV50 is also uncertain: some reported recently that the chip had been cancelled, but officials decline to confirm or deny the information.

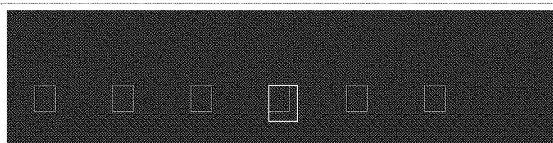
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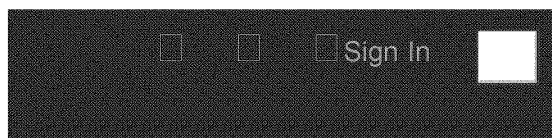
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