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Transcript of William Mangione-Smith, Ph.D.

Date: May 10, 2024

Case: Realtek Semiconductor Corp. -v- ATI Technologies ULC (PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

Transcript of William Mangione-Smith, Ph.D.
Conducted on May 10, 2024

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3	3	EXAMINATION BY:	PAGE NO.
4	4	MR. JOHNSON	4
5	5	EXHIBIT INDEX	
6	6	EXHIBIT NO. DESCRIPTION	PAGE NO.
7	7	(No exhibits marked for identification.)	
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2	1	BE IT REMEMBERED that on Friday,	
3	2	May 10, 2024, at 9:09 a.m., before Terilyn Simons,	
4	3	Certified Court Reporter, CCR, RMR, CRR, CLR, appeared	
5	4	WILLIAM MANGIONE-SMITH, PH.D., the witness herein;	
6	5	WHEREUPON, the following proceedings	
7	6	were had, to wit:	
8	7	<<<<<< >>>>>>	
9	8	WILLIAM MANGIONE-SMITH, PH.D., having been first duly	
10	9	sworn by the Certified Court	
11	10	Reporter, testified as follows:	
12	11	EXAMINATION	
13	12	BY MR. JOHNSON:	
14	13	Q Good morning, Dr. Smith, Dr. Mangione-Smith--	
15	14	A "Mangione-Smith," please.	
16	15	Q "Mangione-Smith," okay, I'll do my best.	
17	16	A Thank you.	
18	17	Q I don't think I have ever deposed you before, so it's	
19	18	nice to meet you.	
20	19	Are you ready to begin today?	
21	20	A I am.	
22	21	Nice to meet you as well, and I don't recall being	
	22	deposed by you as well.	

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5 1 Q So since we haven't met before, I'll just go over a few 2 basic things that I'm sure you're very well aware of 3 because I know you've been deposed many times. 4 Is there any reason you can't give me truthful 5 answers today? 6 A Not that I'm aware of. 7 Q Are you on any kind of medication that will impair your 8 ability to understand my questions or give answers today? 9 A No. 10 Q Okay. I see that you've brought some papers with you 11 today. 12 Can you tell me what those are? 13 A Sure. 14 Printouts of my report and some of the materials 15 that are cited. 16 Q Can you just go through them and identify each one for 17 me? 18 A Sure. 19 The first one is ATI Exhibit No. 2071, and I know 20 there is an issue with some of them having two exhibit 21 numbers, so I'm going to do my best to get the right 22 exhibit number.	7 1 were made to various circuitry. In this case I believe 2 it's all focused on the SQ circuitry. 3 Next is ATI Exhibit No. 2099. This is a document 4 that has estimates for the area required for different 5 circuit blocks in the R400. 6 Next is ATI Exhibit 2111. It's titled, "ATI 7 Technologies Incorporated R400 program." 8 Then I have Realtek Exhibit 1001. This is the '454 9 patent. 10 Then Realtek Exhibit 1009. This is a reprint of 11 the— this is what I have referred to as the Selzer 12 reference, S-E-L-Z-E-R, titled, "Dynamic load balancing 13 within a high performance graphics system." 14 Next is Realtek 1008. It's a magazine article 15 titled, "Introducing the Intel I860 64-bit 16 microprocessor." 17 Next is Realtek Exhibit 1007. This is a reprint of 18 the article, "A simple flexible parallel graphics 19 architecture," where the lead author is John Amanatides, 20 A-M-A-T-I-D-E-S. 21 Next is Realtek Exhibit No. 1010 titled, "Thread 22 prioritization, a thread scheduling mechanism for
6 1 Do you want me to characterize it as well? 2 Q Can you just tell me briefly what it is? 3 A Sure. 4 This is what's called a regression log of testing 5 various circuits, and it looks like it's got a date of 6 being run on January of 2004. 7 Q And do you know what it was testing? 8 A In my notes I probably do. 9 There is a comment at the top that it's— oh, it's a 10 regression report for the SQ on the R400 project. 11 Q Okay. All right. And the next one? 12 A The next one is titled, "R400 Top Level specification, 13 Version 0.2," and it's got an exhibit number of ATI 14 Exhibit 2013. 15 Q Okay. 16 A The next one is titled, "Shader processor, Version 0.1," 17 and the exhibit number is ATI Exhibit 2012. 18 The next is "R400 sequencer specification," and then 19 below that it says, "SEQ, Version 0.4," Exhibit ATI 2010. 20 Q Okay. 21 A Then there is ATI Exhibit 2095, which is what is often 22 referred to as a change log. It's a log of changes that	8 1 multi-context parallel processors," and this is typically 2 referred to by me as the "Fiske reference," F-I-S-K-E. 3 Then I have a printout of my declaration, which is 4 ATI Exhibit 2121. 5 Q Thank you. 6 Are those clean copies or do you have any notes or 7 marks in them? 8 A I have not made any notes or marks on any of these. 9 I didn't print them out, so I couldn't swear that 10 they were clean, but I know of no markings in them. 11 Q So somebody else gave them to you? 12 A Yes. 13 Q I assume that was Counsel? 14 A Yes. 15 Q Okay. So did you ask for printouts of those or they 16 provided those at their own discretion? 17 A They were provided to me yesterday while we were doing 18 preparation for the deposition today. 19 Q Okay. And did you make that selection or did Counsel 20 make it, in terms of which documents to print? 21 A Well, I think— it's hard to say. 22 Which ones to print, I certainly didn't direct any

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9 1 printing. 2 Counsel came with a large box. He may have printed 3 everything that was an exhibit. I just don't know. 4 Q Okay. And so you met with Counsel yesterday to prepare 5 for your deposition? 6 A Yes. 7 Q And did you do anything else to prepare for your 8 deposition, other than meet with Counsel yesterday? 9 A Certainly. I did some reviewing this morning and over 10 the last couple of weeks. 11 Q Okay. Did you have any other meetings with any other 12 individuals? 13 A No. 14 Q Any phone calls, conversations with any other individuals 15 to prepare for your deposition? 16 A Not that I can recall, not specifically to prepare for my 17 deposition. 18 Q And Counsel was Reza or were there other attorneys 19 present? 20 A No, it was just he. 21 Q Okay. So I was going to mark the patent and your 22 declaration, but I'm not going to do that.	11 1 had, you know, typed up different sections and said, you 2 know, "What do you think of this," or I said, "We need to 3 argue X, Y, and Z," and somebody said, "Well, then I'll 4 take a crack at that," and then I reviewed it. 5 Q Okay. So maybe, as we go through today, you can identify 6 portions where you think you might have made the initial 7 draft and others where they were provided to you, if 8 possible. 9 Would that be okay? 10 A Sure. 11 Q Okay. Once the declaration was finalized but before you 12 signed it, did you review it? 13 A Yes. 14 Q And after you signed it and submitted it in this case, 15 have you reviewed it again? 16 A Yes. 17 Q Have you found it to contain any errors or mistakes, 18 anything you want to correct on the record before we get 19 started? 20 A Nothing that occurs to me as I sit here today. 21 Q I'm sure there's typos in any document. I am not talking 22 about those, just any other kind of mistakes that you
10 1 You already have a copy. 2 (Discussion off the record.) 3 Q (By Mr. Johnson) With respect to your declaration, which 4 is Exhibit No. 2121, did you prepare that declaration on 5 your own? 6 A It contains-- the opinions expressed in there are my 7 opinions. 8 I certainly had assistance in discussion with other 9 individuals along the process of me developing the 10 declaration. 11 Q That was a bad question. 12 Did you write the initial draft of the declaration? 13 A Even that's a little hard to answer because some of it, 14 for example, is my background and an explanation of my 15 understanding of the law, I believe. That's typically in 16 there. 17 Those sections have been developed over many years 18 with many different clients. 19 Furthermore, there have been two declarations in 20 this matter, and I looked at the technology over the 21 years, working previously in the context of an ITC 22 matter, so, sure, it's possible that different people	12 1 might have noticed. 2 A Nothing that occurs to me. 3 Q Okay. Thank you. 4 In your declaration you refer to the transcripts of 5 some other individuals, like Mr. Gruber and others, 6 Dr. Watson-- I mean, Mr. Watson. 7 Did you have any conversations with those 8 individuals, where you cite to their transcripts, in 9 preparing for your declaration? 10 A I don't believe so, not that I recall. 11 Q So to the extent that you cite to them or rely on them in 12 your declaration, you are basing that solely on the 13 documents that you reviewed, correct? 14 A That's my recollection. 15 It's my practice, if I'm relying on a personal 16 discussion, I will cite it that way, but I don't recall 17 any such conversations. 18 Q And you can feel free to look at any of the documents 19 that you brought with you today as you need them. It 20 doesn't bother me at all, okay? 21 If you need a break or anything, just let me know. 22 I am very flexible.

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13 1 I try to take breaks as quickly as I can when you 2 ask for them. If I'm asking a question, and I want to 3 finish one or two things, I will try to do that quickly, 4 but feel free to ask, okay? 5 A That sounds good. 6 I prefer to take a break, a brief one, every hour, 7 just to stretch my legs. 8 Q I will do my best. 9 I am sure your counsel will remind me often. 10 Do you recall that there's a term in the '454 patent 11 claims that says, "Vertex manipulation operation"? 12 Have you heard of that term before? 13 A It seems familiar. 14 Can you point me to the section where that appears? 15 Q Sure. 16 You can just look at Claim 1 in Exhibit No. 1001. 17 Claim 1 appears in Column 6. 18 A Yes, I see that. 19 Q Is "vertex manipulation operation" a term of art? 20 A I don't recall hearing exactly that sequence of words 21 previously, but certainly the-- I think that there's a 22 clear understanding to a person of ordinary skill in the	15 1 A So outside of the context of the '454, a vertex operation 2 would be an operation that works on vertex data. 3 Q Okay. And then a little later in Claim 1 it refers to 4 "vertex calculation operation." 5 Do you see that? 6 A I don't doubt it's in there. I'm just not seeing it. 7 Q Sorry, I think I said "Vertex." 8 I meant "pixel," "pixel calculation operation." 9 Do you see that? 10 A I see "pixel calculation" but not "pixel operation 11 calculation." 12 Q Let me restart. Sorry. 13 In the continuing clause of Claim 1, there's a 14 reference to "pixel calculation operations." 15 Do you see that? 16 A Yes. 17 Q Was that a term of art that you were aware of before 18 encountering the '454 patent? 19 A I would say the concept is. 20 I don't recall with great confidence seeing exactly 21 that sequence of words. 22 Q Is there a difference between a vertex manipulation
14 1 art. 2 Q So we'll get to that. 3 I just want to know, in your experience as a person 4 of ordinary skill in the art and an expert in the field, 5 whether or not you had heard the term "vertex 6 manipulation operation" before. 7 A It's possible. 8 The concept I certainly had heard of, but I don't 9 recall exactly hearing that sequence of words previously. 10 Q Is-- and then a little later in Claim 1 it refers to a 11 "vertex operation." 12 Is that a term of art? 13 A I think that's a little bit closer to a term of art, so I 14 would say yes. 15 Q Okay. And so you have encountered that term in your past 16 experiences prior to the '454 patent? 17 A I believe so, but I am not suggesting that I have a 18 reference to point to. 19 Q That's fine. I just want to know what your general 20 understanding was outside of the context of the '454 21 patent as to what a vertex operation would have been. 22 Can you give me that understanding?	16 1 operation, a vertex operation, and a vertex calculation 2 operation? 3 A Sure. 4 Q Okay. Can you explain to me the difference between those 5 three terms? 6 A Well, there are a number of different types of 7 operations. 8 I think "operation" was in all three of those terms. 9 "Vertex manipulation operation" would be an 10 operation that manipulates, I would say, the vertices, 11 and the third one was a vertex, I think, calculation-- 12 just "vertex operations"-- 13 Q Yes. 14 A No-- 15 Q Okay. Let me ask the question just to make sure you're 16 not floundering around. 17 So you've already identified what you believe is a 18 vertex manipulation operation. I appreciate that. 19 What I would like to know is, how is that different 20 from just a general vertex operation? 21 Let's start there. 22 A It is an instance of a vertex operation.

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17 1 Q But I take it that vertex operations are broader, they 2 may include more things? 3 A I believe so, yes. 4 Q Okay. And then I'm asking you if you have ever heard of 5 the term "vertex calculation operation." 6 A Yeah, I believe that was in here, right? 7 Q Well, they have a "pixel calculation operation," but I'm 8 just asking in the terms of vertex. 9 A Oh, okay. That explains why I couldn't find it. 10 "Vertex calculation operation," sure, that would, 11 again, be an example of a vertex operation. 12 Q But it would be different than a vertex manipulation 13 operation? 14 A It could also be an instance of a vertex manipulation 15 operation. 16 Q So how would you define the "vertex calculation 17 operation"? 18 A I would understand that a vertex calculation operation is 19 an operation that does a calculation based on vertex 20 data. 21 Q Do you believe those three terms have a plain and 22 ordinary meaning outside of the context of the '454	19 1 A Yes, I do. 2 Q Are these the legal principles that you used to conduct 3 any claim construction that you felt needed to be done in 4 forming your opinions for your declaration? 5 A These are the legal principles that have been explained 6 to me, as I understand them, regarding claim 7 construction, yes. 8 Q Were you provided any other legal principles that you 9 relied on in conducting any claim construction that you 10 felt needed to be done? 11 A I guess the answer would be no, I don't recall conducting 12 any claim construction in this matter, but it's a long 13 report. Maybe it's in there. 14 Q Okay. In Paragraph No. 53 and 54, I am just going to 15 summarize, but I think you identify that there are two 16 possibilities for claim construction. 17 One is that a term could be given its ordinary and 18 customary meaning, and the other is that it could be 19 given a special definition in the patent, which would 20 supersede any plain and ordinary meaning; is that 21 correct? 22 A That is generally my understanding.
18 1 patent? 2 A I haven't really considered it. 3 Q Do they have a plain and ordinary meaning inside the 4 context of the '454 patent? 5 A I think a person of ordinary skill in the art certainly 6 understands those terms without requiring a construction, 7 so I think that means "yes," but I'll stick with that 8 answer. 9 Q Did you formulate an opinion as to what those terms meant 10 when forming your opinions in your declaration? 11 A Yes, I would say so, although not explicitly, as far as I 12 recall. 13 Q Okay. And you can turn, if you want to, to Page 22 of 14 your declaration, which is Exhibit No. 2121. 15 A Okay. I am there. 16 Q On Page 22 of your declaration you have a subheading 17 entitled, "Claim construction." 18 Do you see that? 19 A Yes, I do. 20 Q And underneath "Claim construction" are two paragraphs 21 numbered 53 and 54 that spill over to Page 23. 22 Do you see that?	20 1 Q Okay. If a term that's recited in a patent claim doesn't 2 have a plain and ordinary meaning, and it was given no 3 special definition in the patent, how would you go about 4 construing that term? 5 A Well, it's my understanding that a term in a patent 6 claim-- the claim should be presumed to be valid, and the 7 meaning of any term should be interpreted as it would be 8 understood by a person of ordinary skill in the art at 9 the time of invention, in the context-- in the whole 10 intrinsic-- in the context of the entire intrinsic 11 evidence. 12 Q Okay. So if I had a term in a patent, let's say, 13 "widget," that has no plain and ordinary meaning in the 14 art, and it turns out that the patent didn't give a 15 special definition for "widget"-- do you understand that 16 assumption? 17 A I do. 18 Q Is it your opinion then that you would then just construe 19 the term "widget" in the context of the intrinsic record? 20 A That's my understanding, it should determine whether 21 there is-- given the entire context, whether there is a 22 reasonable understanding of what a widget would be.

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21 1 Q And in that circumstance would that be considered the 2 plain and ordinary meaning of that term? 3 MR. DOKHANCHY: Objection; calls for a 4 legal conclusion. 5 THE WITNESS: Yeah, I don't really 6 know. 7 Q (By Mr. Johnson) Okay. Now, I noticed in your 8 declaration, which is Exhibit No. 2121, that other than 9 these two paragraphs, 53 and 54, there is no other 10 specific claim construction section in your declaration. 11 Is that correct? 12 A I don't recall for sure, but it would not surprise me if 13 that was the case. 14 Q And so I take that to mean that you did not feel the need 15 to specifically construe any particular term recited in 16 any of the '454 patent claims, correct? 17 A I think that's generally correct. 18 In the past there have been instances where I've 19 been asked to provide a construction where I didn't feel 20 it was necessary, so it's not-- so I would say it's 21 likely two-pronged: I wasn't asked, and I didn't, on my 22 own, feel the need to provide a construction.	23 1 your declaration? 2 A So my recollection is that likely in my first declaration 3 the construction had not come out. 4 I have voiced opinions regarding some of the art not 5 being unified shaders. 6 I don't recall for sure if those are all missing 7 from 2121, but I understand that for purposes of the 8 proceedings, that is the construction that now needs to 9 be applied. 10 Q Okay. So it sounds like at some point you did review the 11 institution decision that was issued by the board; is 12 that correct? 13 A Yes, that's correct. 14 Q Okay. So I want to turn to Page 28 of your declaration, 15 Exhibit No. 2121. 16 A Okay. I am there. 17 Q On Page 28 there is a Section 8 with the title, 18 "Conception." 19 Do you see that? 20 A Yes, I do. 21 Q Just by way of paraphrasing, I think in this section you 22 address what you are asserting as evidence of conception
22 1 Q Do you recall whether or not you came to the conclusion 2 that any recited term in any of the claims of the '454 3 patent had a special definition, as that term is 4 understood by you in Paragraph No. 54 of your 5 declaration? 6 A So my recollection is that my opinion was and is that the 7 term "unified shader" has a particular meaning to a 8 person of ordinary skill in the art. 9 However, my recollection is that the PTAB, I 10 believe, had offered up a construction, and so moving 11 forward I have endeavored to apply that construction. 12 Q Okay. I am happy to give you a copy of the PTAB's 13 decision, but I'm just going to read it and see if you-- 14 if this sounds familiar to you. 15 On Page 17 of the institution decision, the PTAB 16 writes, "We construe the claimed unified 'shader' to mean 17 a shader that is configured to perform both vertex and 18 pixel operations." 19 Do you recall that? 20 A Yes, I do. 21 Q And is that the construction that you applied when 22 reviewing the prior art and formulating your opinions in	24 1 of the unified shader that's disclosed in the '454 2 patent, correct? 3 A Yes, throughout the remainder of this section of my 4 report. 5 Q And your opinion, with respect to conception, is based on 6 the documentation that you cite throughout this section, 7 related to something called the R400 project; is that 8 correct? 9 A I think that's broadly correct. 10 The documentation is certainly some of the 11 engineering technical specifications, as well as some of 12 the related but different types of documents, 13 particularly that I mentioned I brought in today. 14 Q So just to set the stage, I just want to-- I want you to 15 tell me what is the R400 project. 16 A So my understanding was that the R400 was a development 17 project at ATI to build a new graphics processor or 18 "GPU," it's sometimes referred to for "graphics 19 processing unit," and they developed the design. 20 I think I would assume that initially it was 21 anticipated to be sold fairly broadly. 22 My understanding is that it was used in the

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25 1 Microsoft Xbox, but I don't know of use other than that. 2 Q All right. And this GPU that you referred to included a 3 unified shader, correct? 4 A Yes, that's correct. 5 Q As well as some other components to make out the overall 6 GPU architecture, correct? 7 A I would say that's correct. 8 It's a little bit tricky in that as VLSI Technology 9 has gotten denser and denser, other stuff on the system 10 has gotten put on the chip, so whether-- I think the R400 11 was considered the entire chip, but ATI might have 12 considered that just the main part of the chip with other 13 peripherals around the edge. 14 So exactly what they would consider the boundary of 15 the GPU, it certainly is the R400. It may have been 16 other components as well. 17 Q Okay. The '454 patent claims are directed to a unified 18 shader, correct? 19 A Yes, that's correct. 20 Q So my only desire in my question was to just make sure 21 that the GPU included a unified shader. 22 That's all I was trying to get at.	27 1 You are basing your opinions on this AMD 2 documentation in the 2001 timeframe, correct? 3 A Yes, I think that's correct, although I don't recall if 4 in some of the-- I'm basing it on the AMD documentation. 5 I did my best to only consider documentation with 6 regards to diligence. 7 I don't-- let me take a step back and try to be a 8 little clearer. 9 I am not sure if it was restricted-- if my analysis 10 was restricted to documentation in the 2001 timeframe. 11 I think that certainly was the starting point. 12 Q Let me refresh your recollection just a little bit and 13 see if we can clear it up. 14 I think you addressed two things in your report, and 15 feel free to correct me. One is conception and the other 16 is diligence. 17 Do you recall that? 18 A Yes. 19 Q And I believe your opinions related to conception are 20 that it was conceived of in the 2001 timeframe, but then 21 there was diligence that lead up to the reduction in 22 practice in the 2003 timeframe, correct?
26 1 A Got it. 2 The GPU in the R400 project included a unified 3 shader. 4 Q Okay. And it included some other things as well, but it 5 absolutely included a unified shader, correct? 6 A Yes, sir. 7 Q Okay. And then starting on Page 30 of your report, there 8 is a subsection entitled, "454 patent," and for the next 9 many pages you walk through each claim on an 10 element-by-element basis and identify where you believe 11 those elements are present or disclosed within the 12 documentation you reviewed, correct? 13 A Yes, I think that's a generally accurate assessment. 14 Q And if we look at Paragraph No. 76 on Page 31 of Exhibit 15 No. 2121, there is a statement in the second sentence 16 that says, "The AMD documentation in the 2001 timeframe 17 describes a unified shader performing the same steps as 18 the unified shader of the '454 patent." 19 Do you see that? 20 A Yes, I do. 21 Q So you repeat this sentence throughout your analysis in 22 this conception section, and my question is:	28 1 A That is my recollection, yes. 2 Q So it would not surprise me that you did look at some 3 documents after 2001, at least with respect to diligence, 4 but my question is: 5 For conception, since you are asserting it in 2001, 6 did you rely on documents in the 2001 timeframe? 7 A Yes. 8 Q Okay. Do you believe that documents beyond 2001 would 9 show conception in 2001? 10 A I guess it's possible if they included references or data 11 or cited data that was from 2001, but I'm not sure. 12 Q And the documents that you refer to in this sentence in 13 Paragraph No. 76, they all relate to the R400 project, 14 correct? 15 A I believe so. 16 I don't know why I would have cited anything not 17 related to the R400. 18 Q And do you recall whether or not there was a product in 19 the 2001 timeframe that was reflected in the R400 20 documentation? 21 A I don't recall for sure. 22 Some of the documentation referred to a product or

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29 1 referred to a previous design, which I believe was turned 2 into a product, but I don't recall for sure as I sit 3 here. 4 For example, my recollection is that there was an 5 R300, an earlier design, and elements of the R400 early 6 documentation talked about changes or advancements 7 compared to earlier products and designs. 8 Q It is not your opinion that the R300 is evidence of 9 conception of the invention described in the '454 patent, 10 correct? 11 A I don't recall relying upon that. 12 I am not sure that it could not have served such a 13 purpose, but I don't think I used it for that purpose. 14 Q Did you inspect any of the products that might have been 15 available in the 2001 timeframe that were related to the 16 documentation you reviewed? 17 A Not that I recall in the process of my work for this 18 matter. 19 Q Have you ever seen any of the products from the 2001 20 timeframe related to the R400 project? 21 A Likely. 22 I'm a computer nerd. I see lots of different kinds	31 1 A It depends. 2 I do quite a bit, but different companies oftentimes 3 have their own proprietary language for source code that 4 is not available outside of the company. 5 Q And have you heard the term "RTL code"? 6 A Yes, I have. 7 Q Can you tell me what that is? 8 A "RTL" stands for "registered transfer language." 9 Q And do you recall there was a reference to "RTL code" 10 related to the R400 project? 11 A I recall there being quite a bit of discussion of RTL. 12 I recall reviewing RTL, as well as discussions of 13 net list files, which are closely related. 14 Q And was that RTL code, code that existed in the 2001 15 timeframe that you reviewed? 16 A I believe so, but I'm not sure. 17 Q Do you recall whether or not there's, for lack of a 18 better term, a schematic diagram of the overall layout or 19 circuitry architecture for the GPU related to the R400? 20 A I certainly recall a number of high-level schematics, 21 block diagrams at different levels of abstraction. 22 Q So, for example, on Page 31 there is a block diagram,
30 1 of products. 2 I've had lots of different kinds of processors and 3 GPUs from-- some of them from AMD, some of them from ATI, 4 but I don't recall any particular one at this moment. 5 Q So you have no specific memory of ever inspecting a 6 product related to the R400 project that was available in 7 the 2001 timeframe, correct? 8 A Not that I recall as I sit here. 9 Q Within the AMD documentation that you reference in your 10 declaration, did that include any source code? 11 A My recollection is that it did, but I'm not 100 percent 12 certain where. 13 My recollection could be wrong. 14 It's also-- part of the issue is what constitutes 15 "source code." 16 I have seen documentation where there will be just a 17 couple of lines cited to make it clear to an engineer 18 what sort of function should be there, but I don't 19 believe that the documentation, as far as I recall, 20 contained, for example, large blocks of source code or 21 complete source code files. 22 Q Do you read and understand source code?	32 1 schematic at the bottom of the page. 2 Do you see that? 3 A Yes, I do. 4 Q And is that a block diagram for the overall GPU related 5 to the R400? 6 A It's titled, "R400 Top Level block diagram." 7 Q And would you understand that to be a block diagram for 8 the overall GPU architecture? 9 A Well, again, it depends. 10 For example, I don't know if the Xbox had-- 11 contained-- if the chip used in the Xbox contained one 12 R400 or two. That's the sort of scaling that typically 13 gets done in this area. 14 Let's say it had two. 15 I think a person of ordinary skill in the art could 16 look at that and say, "The whole thing is one GPU" or it 17 could say, "No, it's got two GPUs that operate somewhat 18 independently." 19 I think it's perfectly reasonable to look at this 20 and say, "That's a GPU." 21 Q And within that block diagram that's on Page 31, is there 22 a unified shader within that?

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33 1 A I believe so, but my—let me rephrase that. 2 Since it's my opinion the R400 has a unified shader, 3 I believe there is a unified shader in this block 4 diagram. I am just having trouble reading the blocks as 5 printed. 6 Q I believe that you told me earlier that you have with you 7 the Top Level specification, which is Exhibit No. 2013. 8 A I believe that is the case as well, but let me look. 9 I found the patent that I couldn't find before. 10 Yes, I have the Exhibit No. 2013. 11 Q So feel free to look at that, and maybe that document has 12 a clearer picture of that block diagram. 13 A Not much clearer. 14 Let me see. 15 Sorry, I still can't read these blocks. 16 On the other hand, there is a Section No. 7, which 17 is below the block diagram in this document, as well as 18 reproduced next in my report, that has a list of blocks, 19 and I would expect that list corresponds to the labels on 20 the different blocks we are looking at here. 21 Q Is unified shader listed as one of the blocks? 22 A Does the word, literally, "unified shader" appear? Is	35 1 Claim 1 is a method claim. It does certainly refer to 2 operating upon that component, but it's not defined-- 3 Q Sure, I can clear that up. 4 We can go to Claim 2, that's fine. 5 You agree that Claim 2 is an apparatus claim? 6 A Yes. 7 Q And it is directed to a unified shader comprising-- 8 A Yes-- 9 Q --correct? 10 A Yes. 11 Q And one of the components within that unified shader is 12 recited as a general purpose register block, correct? 13 A Yes. 14 Q Within the R400 documentation were you able to find a 15 general purpose register block? 16 A Yes. 17 Q And can you identify that in the Top Level diagram that 18 we were looking at from Page 31? 19 A Well, perhaps. Let me look back at the diagram 20 discussion. 21 Well, there is a reference to a registered interface 22 manager, the RBBM.
34 1 that what you're asking? 2 Q Yes. 3 A No. 4 Q Okay. Is it your opinion that the GPU as a whole is the 5 unified shader or that there is a unified shader within 6 the GPU of the R400? 7 A So let me refer just to the R400 Top Level block diagram 8 that we have talked about, setting aside the question of 9 whether the GPU is the whole chip, for example. 10 It's my opinion that the R400 Top Level block 11 diagram contains within it a unified shader. 12 Q Does it contain within it something other than a unified 13 shader? 14 A Sure, I believe it does. 15 Q The claims in the '454 patent, they recite a few 16 components of a unified shader, correct? 17 A Yes. 18 Q For example, in Claim 1 there is a general purpose 19 register block that's recited. 20 Do you see that? 21 A Yes, I see that. 22 My only caveat, again, not being an attorney, is	36 1 I can't tell, looking at this block diagram, where 2 that is, but one place that I would look to is where that 3 unit connects to, but, I guess, that being said, as I sit 4 here today, looking at this diagram, I cannot point you 5 to what would qualify as a general purpose register. 6 Q So if you look at Page 45 of your declaration in Exhibit 7 No. 2121-- 8 A Yes. 9 Q At the top of the page you write, "The R400 includes a 10 general purpose register block." 11 Do you see that? 12 A Yes, I do. 13 Q And then it goes on. 14 Does that refresh your recollection? 15 A Yes, and it's, for the most part, certainly easier to 16 read than that block diagram. 17 Q So I am trying to figure out where within that block 18 diagram those GPRs are going to be located. 19 A Okay. Let me turn to-- there's a reference to the 20 sequencer at the bottom of Page 45. 21 I believe that means they are going to be in the 22 sequencer, but let me turn to that reference, the design

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37 1 document for the sequencer. 2 Yes, so at a minimum it would be within the 3 sequencer or the SQ unit, and I see, for example— it 4 just occurs to me on Page 4 of Exhibit No. 2010 is one of 5 those references that I had to the previous design, the 6 R300. 7 Q Okay. So the general purpose register block is within 8 the sequencer of the R400, correct? 9 A I have identified that, yes. 10 Q Okay. And then the next component that's recited in 11 Claim 2 is a processor unit. 12 Do you see that? 13 A Yes, I do. 14 Q And do you agree with me that the term "processor unit" 15 is a generic term? 16 A I don't know. 17 It's fairly broad. 18 Q Would "processor unit" be a term of art outside the '454 19 patent? 20 A I would think so, yes. 21 Q Okay. Is there a difference between a processor and a 22 processor unit?	39 1 I don't know that that's not redundant. 2 Q You don't-- 3 A But I think the language certainly matches the convention 4 in the field. 5 Q You don't know if it's redundant because you didn't 6 formulate an opinion or do any analysis within the 7 context of the '454 patent as to whether or not the term 8 "unit" created some additional requirement in the claims, 9 correct? 10 A I am not sure how to answer that. 11 I think a person of ordinary skill in the art, 12 looking at "processor unit," would certainly have an 13 understanding and not feel the need to parse whether 14 "unit" further constrained a processor. 15 It's certainly possible that in some context, and 16 maybe in the context of the '454 patent -- I haven't done 17 this analysis -- one could argue that a processor could 18 be implemented in, simply, software, and so perhaps the 19 inventors were attaching "unit" to make it clear that it 20 was a physical structure. 21 Q We are about to take a break, but I'm just going to 22 finish this last one.
38 1 A I haven't really considered that. 2 Q In the context of the '454 patent claims, what does the 3 term "unit" add to the claim? 4 A I don't know. I haven't really considered that. 5 Q When evaluating the R400 documentation and looking for 6 something to satisfy the term "processor unit," what did 7 you look for? 8 A I looked for a unit that would be understood to be— in 9 my opinion, to be a processor unit that would also match 10 any of the other constraints in the various claim 11 limitations. 12 Q Did you just look for a processor that carried out the 13 functions recited in the claim? 14 A This was quite some time ago. I don't recall exactly 15 what my process was. 16 Q But as you sit here today, you can't tell me what the 17 difference is between a processor and a processor unit, 18 correct? 19 A I don't know that there is a difference. 20 Typically, in my experience, engineers working in 21 this field refer to graphics processor units, GPUs, and 22 central processor units, CPUs.	40 1 The next component in Claim 2 is recited as a 2 sequencer. 3 Do you see that? 4 A I do. 5 Q And as we've already discussed, you were able to find 6 something called a sequencer in the R400 documentation, 7 correct? 8 A Correct. 9 MR. JOHNSON: Okay. Why don't we go 10 ahead and take a break. 11 (Recess 10:12 to 10:24 a.m.) 12 Q (By Mr. Johnson) Okay. Are you ready to proceed? 13 A Yes, I am. 14 Q When we left, we had just identified the sequencer in the 15 claims, and I wanted to ask you whether or not you found 16 that the sequencer in the R400 was within the unified 17 shader of the R400. 18 A Yes. 19 Q And how did you come to that conclusion? 20 A Well, I came to that conclusion based on my experience 21 and my reading of the '454 patent as well as the R400 22 documentation.

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41 1 This is— well, I guess I'll end with that. 2 Q So did you see within the diagrams of the documentation 3 where the sequencer was located relative to the 4 boundaries of the unified shader in the R400? 5 A I don't recall the R400 showing— identifying the 6 boundaries of a unified shader, but it certainly may 7 have, and I may have recited that. 8 Let me go back and look. 9 So yes, I identified the Top Level as a unified 10 shader, but I don't recall the documentation specifically 11 doing that. 12 It may have. 13 Q Okay. So let's turn to Page 35 of your declaration, 14 Exhibit 2121, and look at Paragraph No. 82. 15 A Okay. 16 Q And just to put you within context, we are still within 17 your discussion of Claim 1 in the conception portion of 18 your declaration, and specifically with respect to 19 Paragraph No. 82, you are addressing Element C of Claim 20 1, which is, "Performing vertex manipulation operations 21 and pixel manipulation operations by transmitting vertex 22 data to a general purpose register block."	43 1 used by the arbitration scheme in the R400? 2 A I know further what's described in the sequencer 3 documentation, as well as the source code I reviewed, but 4 in particular I'm aware of the further passages that I 5 cited here in Paragraph No. 82. 6 For example, it says, "The arbiter is not going to 7 select a vector to be transformed if the parameter cache 8 is full, unless the pipe has nothing else to do; i.e., no 9 pixels are in the pixel FIFO," and then furthermore I 10 cite the passage that says, "Sequencer SEQ arbitrates 11 between pixel FIFO and vertex FIFO when there are no 12 vertices pending, or there is no space left in the 13 register files for vertices, the pixel FIFO is selected," 14 and then there is a final citation coming from Page 5 of 15 that documentation, saying, "The rasterizer always checks 16 the vertices FIFO first, and if allowed by the sequencer 17 sends the data to the shader. If the vertex FIFO is 18 empty, then the rasterizer takes the first entry of the 19 pixel FIFO"— which it says is a vector of 16 pixels 20 —"and sends it to the interpolators. Then the sequencer 21 takes control of the packet. The packet consists of 22 three bits of state, six to seven bits for the base
42 1 Do you understand that? 2 A Yes. 3 Q In Paragraph No. 28 you state, "Based on the arbitration 4 scheme implemented by the sequencer," and then it goes 5 on. 6 Do you see that sentence? 7 A Yes, I do. 8 Q Can you tell me what you understand the arbitration 9 scheme to have been in the R400? 10 A Well, it is largely described in the citations that 11 follow. 12 For example, I cite to 2010 on Page 17, where it 13 says, "The SQ arbitrates between the pixel FIFO and the 14 Vertex FIFO. 15 "Basically the vertex FIFO always has priority." 16 Q So do you agree that the arbitration scheme in the R400 17 is based on priority? 18 A I would not characterize it that way. 19 It literally says, "Basically the vertex FIFO always 20 has priority," it does say that, but then there's also a 21 discussion of the priority scheme in more detail. 22 Q And do you know what the priority scheme was that was	44 1 address of the shader program, and some information on 2 the coverage to determine texture LOD," which stands for 3 "level of depth." 4 "All other information (2x2 addresses) is put in a 5 FIFO (one of the pixels and one of the vertices) and 6 retrieved when the packet finishes its last clause." 7 Q Do you believe that the arbitration scheme that was used 8 in the R400 was based on priority? 9 A I would not characterize it that way. 10 As I said, they say it's basically the vertex FIFO 11 always has priority, but the vertex FIFO doesn't always 12 have priority based on the other discussion, some of 13 which I've cited and the rest of which resides within the 14 specification. 15 Q Did you review the priority scheme for the sequencer? 16 A I reviewed the arbitration scheme for the sequencer. 17 Q And is there a priority scheme within the arbitration 18 scheme? 19 A I haven't thought to look. 20 I haven't considered that. 21 There are elements of priority used in the 22 arbitration scheme.

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45 1 Q If you look on Page 32 of your declaration, you cite to 2 Exhibit No. 2013. 3 A I see that. 4 Q At Page 11. 5 There is a box there with some text in it that 6 starts, "Before starting the processing." 7 Do you see that box? 8 A Yes. 9 Q And the last two sentences of that paragraph state, "I 10 think it will be sufficient for the real time stream to 11 have a priority over the vertex stream, which has a 12 priority over the pixel stream. This will meet the real 13 time demands, and keep the vertex cache filled." 14 Do you see that? 15 A Yes, I see that. 16 Q So you agree that there is some sort of priority scheme 17 involved, correct? 18 A No. This is in reference to the Top Level design. This 19 doesn't come from the sequencer documentation or from the 20 engineers designing the sequencer. 21 The author is saying he thinks that will be 22 sufficient, but he's not sure, and as we see from the	47 1 data. 2 I will also point out-- I'm taking a step back for a 3 moment. 4 If I recall previously, you had asked, I think, 5 where the sequencer was in the overall block diagram, and 6 when we looked at Page 32, it refreshed my memory that 7 the sequencer is within the raster engine, and the raster 8 engine is one of the blocks in the overall block diagram. 9 Q Okay. Thank you. 10 So going back to my question, did you review all of 11 the criteria used by the sequencer to make the 12 determination about what is allowed and not allowed to be 13 sent to the shader? 14 A I would say yes. 15 Q And did you put into your declaration anywhere an 16 analysis of the criteria, the full criteria, that was 17 used by the sequencer to make that determination? 18 A I believe I endeavored to do that; for example, in my 19 discussion of-- at Paragraph No. 82, that we were just 20 looking at. 21 Q Okay. I will just jump to Page 49 of your declaration. 22 A All right. I'm there.
46 1 materials we just reviewed, it is not the case. 2 Q So is it your opinion that this statement about priority 3 has nothing to do with the sequencer? 4 A No, I wouldn't say that. 5 It's referring to the sequencer, so it does have 6 something to do with the sequencer. 7 Q So the sequencer does involve some sort of priority 8 scheme, correct? 9 A I think I've answered this question before. 10 I wouldn't say that. 11 The sequencer has an arbitration scheme. 12 Q Earlier you referred to a statement on Page 35 of your 13 declaration that's in the last box on the page that says, 14 "The rasterizer always checks the vertices FIFO first, 15 and if allowed by the sequencer sends the data to the 16 shader." 17 Do you see that? 18 A Yes, I do. 19 Q And what are the criteria used by the sequencer to make 20 that determination about what is allowed and not allowed? 21 A I don't recall the full set of requirements. 22 One issue is whether there is space to receive the	48 1 Q And I believe on Page 49 we are within your analysis of 2 Claim 2 with respect to conception, based on the R400 3 documentation, and specifically you are addressing the 4 limitation that is directed to the sequencer in Claim 2, 5 correct? 6 A Yes, I see that. 7 There's a section heading on the previous page, Page 8 48, which has Limitation D, as I have identified it, the 9 third element of Claim 2. 10 Q Okay. And as you stated earlier, in Paragraph No. 109 11 you have identified that the sequencer is part of the 12 rasterizer or raster engine, correct? 13 A Yes, that's correct. 14 Q In Paragraph No. 108 you have a sentence that says, "The 15 AMD documentation, as of August 24, 2001, describes a 16 sequencer having the same characteristics as the 17 sequencer described in the '454 patent." 18 Do you see that? 19 A Yes, I do. 20 Q So when looking for a sequencer in the R400 21 documentation, were you looking for a sequencer as 22 described in the '454 patent specification?

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49 1 A Ultimately, yes, because I was focused, at this point, on 2 the third limitation of Claim 2 from the '454 patent, but 3 certainly I started by looking at blocks that are 4 identified as sequencers. 5 There likely are other elements throughout the R400 6 that would also be considered sequencing various 7 operations. 8 Q Paragraph No. 111 on Page 53, you state, "The operations 9 are performed on data that is stored in the general 10 purpose registers." 11 Do you see that? 12 A I do. 13 Q And I assume that we are talking here about the 14 operations being carried out by the processing unit; is 15 that correct? 16 A Ultimately, yes. 17 The limitation we're looking at refers to the 18 sequencer maintaining instructions operative to cause the 19 processor to execute vertex calculations and pixel 20 calculation operations. 21 Q So how did the processing unit perform these operations 22 on data that is stored in the general purpose registers?	51 1 "Well, the processor just has it already and gets the 2 particular data." 3 It's possible that AMD is thinking of the general 4 purpose register set, which is big and more complex than 5 in a non-GPU processor, as its own block separate from 6 what they're considering the processor. 7 I don't recall exactly how they drew the box. 8 Q So in the first example you gave, where you said that the 9 sequencer makes the data available to the processor unit, 10 in that case the processor unit would then just access 11 that data in the registers and take what it needs to 12 operate on, correct, or retrieve, I think that's the word 13 you used? 14 A So the data is stored for any thread that is in operation 15 at a particular point in time. 16 The data for that is already stored in the general 17 purpose register set. 18 It's just a question of whether that's viewed as 19 being forwarded to the processor or whether it's viewed 20 as being part of the processor. 21 The processor box is drawn to include the GPR or 22 not.
50 1 A Well, the data is retrieved from the general purpose 2 registers. 3 The processor unit does whatever the calculation is 4 that is required by the operation; for example, it could 5 be something as simple as adding two sets of numbers 6 together. 7 Q How is the data retrieved from the general purpose 8 register? 9 A Over data buses. 10 Q Would the processor unit simply be given access to the 11 general purpose registers and go in and take what it 12 needs? 13 A So what happens is the sequencer is arbitrating from 14 instructions and operations that-- multiple instructions 15 and operations that might be pending, and it causes the 16 data required for the selected operation to be made 17 available to the processor unit. 18 To some extent, in the context of the R400, it 19 depends on a process of box drawing, I would say. 20 I would typically consider a processor to comprise a 21 general purpose register set or the register set that it 22 operates on, in which case I would be inclined to say,	52 1 It doesn't change the design or the functionality, 2 but for management purposes or from their perspective, 3 they may have thought of these as two separate units. 4 Q Did you make any evaluation as to how the data was 5 retrieved by the processing unit? 6 A Yes. 7 Q Okay. So that's all I'm trying to get at. 8 How is the data retrieved by the R400 processor? 9 A In a way consistent with the claims. 10 Q Sorry, but that just really doesn't give me any detail. 11 What I want to know is: 12 I want you to identify in your declaration, or based 13 on your understanding as you sit here today, how the 14 processing unit retrieved the data that it then performed 15 the calculations on. 16 A Well, I focused on the claims. 17 Can you point me to-- I don't recall a claim 18 limitation talking about the processor receiving-- I'm 19 sorry, retrieving the data. 20 Q Well, that's the word you used earlier, so I'm just 21 repeating your language. 22 What did you mean when you said that?

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53 1 A I don't believe I said the R400 does that. 2 Q So in the R400 there is data that is stored in the 3 general purpose registers, correct? 4 A Yes, there is, both vertex data and pixel data. 5 Q And in Paragraph No. 111 of your declaration you state 6 that "Operations are performed on data that is stored in 7 the general purpose registers," correct? 8 A Yes. 9 Q And those operations are performed by the processing 10 unit, correct? 11 A Yes. 12 Q And how does the processing unit get that data to perform 13 those operations, as you stated in Paragraph No. 111 of 14 your declaration? 15 A So the design document, and in particular I am going to 16 talk about the passage cited at the top of Page 54, talks 17 about the GPR, the general purpose register file, holding 18 data for multiple programs that are in operation. It 19 could be multiple geometry operations, multiple pixel 20 operations, or a combination of both. 21 It makes reference to-- it makes reference to 22 something that's called "microthreading" -- that's one	55 1 actually be using data in registers eight, nine, and ten, 2 for example, or nine, ten, and 11, depending on whether 3 the registers are addressed starting at zero or one. 4 That's part of how the data is retrieved from the 5 GPR and made available for use by the operations. 6 Q So it's placed into a different source register then, 7 correct? 8 A Different from what? 9 Q From the general purpose register block. 10 A It may be put into a different register. 11 I don't think those details are provided. 12 The processor-- the processing unit is pipeline, 13 which will require some registers between different 14 pipeline segments, but those registers are not 15 addressable. They're not the type of registers that 16 we're talking about here or as referred to in the claims. 17 Q I think we are getting bogged down in something I really 18 wasn't trying to get bogged down in. 19 I was trying to ask a much simpler question. 20 I just want to know, does the processor unit go and 21 retrieve the data that it needs to operate on, "yes" or 22 "no"?
54 1 word -- which was being introduced at that time into 2 CPUs, although it's an old concept going back to the 3 peripheral processor unit of the CDC 6600 back in the 4 '60s. 5 What they say here is that "The management of the 6 shader register file is automatic and not visible to a 7 program executing on a vector, except that a program is 8 required to declare the number of GPRs," so what this 9 means is that, for example, the thread might require-- 10 might say it requires eight registers, and for that 11 thread there will be another register that holds an 12 offset that points into the GPR, so in order-- from the 13 point of view of the executing thread, it would have an 14 instruction that says something like, "Add register one 15 to register two, stick the result in register three." 16 In order to actually get access to that information, 17 the offset for the particular thread needs to be added to 18 the value of one, two, and three, so if the offset is 19 zero, it would look into GPR at one, two, and three, but 20 if the offset was set to-- for the thread, was set to 21 eight, even though the thread thought it was accessing or 22 using data in registers one, two, and three, it would	56 1 A I tried to answer that question as best I could. 2 It depends on how the block is drawn. 3 If the processor unit includes the GPR, which is 4 typically the case, then it has access to-- it has the 5 operation, it knows it wants to use registers one, two, 6 and three, it provides that data into the GPR, and the 7 information in it gets pulled out. 8 Now, if the box is drawn such that the processor 9 doesn't include the GPR, then I could imagine one of two 10 things happens: 11 As the operation flows from the sequencer into the 12 processor, those fields are used to access the GPR, and 13 the data is forwarded to the processor; or, when the 14 operation is received by the processor, then it sends the 15 register references sort of back out to the GPR and 16 receives them. 17 Q And which of those embodiments that you just described is 18 used in the R400? 19 A I don't know exactly how they decided to draw their 20 boxes. 21 Neither one of them changes my analysis. 22 Q So I am jumping up to Page 77 in your report.

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57 1 I'm sorry-- strike that. 2 I am moving to Page 77 in your declaration, which is 3 Exhibit No. 2121. 4 A All right. I am there, and I will tell you that I'm not 5 sure what the distinction is between "reports" and 6 "declarations" as well, but I'm with you. 7 Q In this part of your report you are addressing Claim 5 8 and specifically the sequencer limitation of Claim 5. 9 Do you see that? 10 A Yes. 11 Q And that limitation recites a term called "selected 12 data." 13 Do you see that? 14 A Yes. 15 Q Is "selected data" a term of art outside of the '454 16 patent? 17 A I don't know. 18 The understanding-- the meaning of "selected data" 19 would be clear to a person of ordinary skill in the art. 20 Depending on the context, it may be considered a 21 term of art. 22 Q So within the context of the '454 patent, what makes data	59 1 essentially a thread startup. 2 Q Okay. So when selecting data to place it into the GPR, 3 if there's going to be other data there, is there 4 something that identifies the selected data as being 5 selected as it sits in the GPR? 6 A Yeah. It's whatever data is being written into the GPR. 7 Q Well, maybe I'm just not asking it correctly, but how 8 would I distinguish between selected data and 9 non-selected data that is stored in the general purpose 10 register block? 11 A Well, in this context, in the example I provided, the 12 sequencer is going about the process of setting up a new 13 thread, so there is data, presumably, in the GPR. 14 Granted, when the chip first starts, there is no 15 meaningful data in there, but during general operation, 16 there will be data in there, and as this element says, if 17 the amount of space available in the store is sufficient, 18 the sequencer can select the data to start up a thread 19 and place it in the GPR. 20 Q Okay. So by placing it into the GPR, every data that's 21 placed into the GPR, based on that criteria, would be 22 selected data, correct?
58 1 selected? 2 A That it has been selected. 3 Q Is there criteria used to select data in the '454 patent? 4 A Sure. 5 Data is selected, for example, when it's picked from 6 multiple possible data elements related to multiple 7 possible pending threads and placed into the GPR. 8 It is also selected, for example, when the sequencer 9 decides to pick a particular operation, and that 10 operation will have associated with it data that needs to 11 be used. 12 Q Okay. So I think I heard two things in that response. 13 One is it's selected and placed into the GPR; is 14 that correct? 15 A Yes, that's correct. 16 Q And so under that context, all of the data placed in the 17 GPRs would be selected data, correct? 18 A No. 19 Q So is there data that's in the GPR that was not selected 20 from a larger group to be placed in it? 21 A Sure. 22 Not in the way that I was discussing about	60 1 A No. 2 Q Well, if data is selected based on available space-- I 3 think that's what you just said, right? 4 A In this claim limitation, yes. Yeah. 5 Q So if data is selected based on available space and 6 placed into the GPR, everything placed into the GPR under 7 that criteria would be considered selected data under 8 this claim limitation, correct? 9 A Whenever the sequencer goes to start up a thread, the 10 thread indicates how many-- how much storage it needs and 11 if there is-- well, there-- I think there always is 12 initial data associated with that storage, it will place 13 that selected data into the GPR. 14 Now, that data may not cover all of the storage 15 required. 16 Q What makes data maintained in the store, according to 17 Claim 5, selected data? 18 A Well, the data-- as I mentioned, the selected data gets 19 written into the GPR, and what a register file does, in 20 general, and particularly a general purpose register 21 file, is that it's there to maintain data. 22 It's a particular kind of memory. That is its

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61 1 purpose. 2 Q I want to clear something up because we've been using 3 this term "GPR," but the claim refers to the "general 4 purpose register block," and so when you refer to "GPR," 5 are you intending that to mean the "general purpose 6 register block" according to the '454 patent claims? 7 A In this context, yes. 8 I don't recall if-- in some cases it's also referred 9 to-- well, here it's referred to as "the store." 10 When I said "here," I'm referring to the limitation 11 that we're looking at on Page 77. 12 The store it's talking about, I believe, maps to the 13 R400 GPR. 14 Q Okay. And what I'm trying to figure out is there's-- 15 strike that. 16 You agree with me that there is, at some point in 17 time during operation, data maintained in the store, in 18 the R400, correct? 19 A Yes. 20 Q And what I'm trying to determine is, as that data sits in 21 the store, is it already designated as selected data 22 according to the claim?	63 1 We're talking about data that's stored and 2 maintained in the store, correct? 3 A Yes. 4 Q So it is physically already sitting and being maintained 5 in the store, okay? 6 A Yes. 7 Q What I want to know is: 8 As it sits there, is it selected data or will it 9 become selected data because the sequencer chooses it 10 later? 11 A I've identified here as it being the selected data when 12 it's selected and placed into the store. 13 Q Okay. I am going to jump to Page 85 of your declaration. 14 A Okay. I'm there. 15 Q On Page 85 you begin to address Claim 7 of the '454 16 patent, correct? 17 A Yes. 18 Q And Claim 7 states, "The shader of Claim 5, further 19 including a selection circuit"-- do you see that? 20 A I do. 21 Q And I believe that you have identified that the selection 22 circuit is the sequencer in the R400, correct?
62 1 A Well, my understanding is that-- I guess it depends. 2 I wonder if it's possible, although it would be 3 exceedingly rare, for a thread to have no input data but 4 require storage, although I guess that's still selected 5 data, it's just selected data with the empty set. 6 There is data maintained in the store that is 7 selected by the sequencer for thread startup. 8 There is also data maintained in the store that is 9 not that sort of selected data. 10 Q And what I'm trying to get at is whether or not there is 11 a temporal issue in your opinion as to whether or not the 12 data sitting in the store, being maintained in the store, 13 is something that is going to be selected or that has 14 already been selected. 15 A I think it's-- according to this limitation, it's at 16 least selected by the sequencer, so it's already in 17 there. It's already in there at the point when the 18 register file is set up to allow the execution of 19 operations from a particular vertex or pixel thread. 20 Q Right. 21 I understand that it's already there. That's a 22 given.	64 1 A Let me be sure. 2 Q If you want, I can direct you to Paragraph No. 159 of 3 your declaration. 4 If you just look at the second sentence, it states, 5 "The R400 sequencer, as explained above, is the arbiter, 6 or selection circuit." 7 Do you see that? 8 A Yes. 9 Sorry, I was looking further to the control signal. 10 Yes. 11 Q So your opinion, with respect to the R400, is that the 12 selection circuit of Claim 7 is satisfied by the 13 sequencer; is that correct? 14 A Yes. 15 Q And that's the same sequencer that you identified as 16 satisfying the sequencer limitation in the-- in Claim 5, 17 correct? 18 A Yes, I believe that is the case. 19 Q So in your opinion does-- strike that. 20 I take it then that your opinion is that the 21 selection circuit of Claim 7 does not have to be a 22 separate component from the sequencer recited in Claim 5,

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65 1 correct? 2 A Sure, and my experience, depending on how claims are 3 written, it's possible for a particular block to satisfy 4 two different claim limitations. 5 Q Okay. And in Claim 5 the memory that's being used, I 6 believe you said, is being referred to as a store, 7 correct? 8 A Yes. 9 Q And Claim 6 comes from Claim 5 and states, "Wherein, the 10 sequencer further includes circuitry operative to fetch 11 data from a memory." 12 Do you see that? 13 A Yes, I do. 14 Q And for Claim 6 you also identify the sequencer as being 15 the circuitry that satisfied Claim 6; is that correct? 16 A The additional circuitry of Claim 6 is included within 17 the sequencer. 18 Q Okay. And what is the memory that you believe satisfies 19 the memory recited in Claim 6 for the R400? 20 A I believe that would be the GPR, but let me review 21 further. 22 So in this case, in this context for Claim 6, in	67 1 Whether, you know, in claim construction it would be 2 construed that it has to be separate or could be 3 together, I'm not sure, but it suggests to me that it 4 certainly could be separate. 5 THE WITNESS: Is this a good break? 6 I think it's been maybe an hour, but maybe we're-- 7 MR. JOHNSON: Sure, that's fine. 8 (Recess 11:21 to 11:32 a.m.) 9 Q (By Mr. Johnson) Are you prepared to go forward now? 10 A Me? Yes. 11 Q Okay. Let's see, when we broke, I believe we had just 12 finished talking about the selection circuit. 13 We can move to a new topic. 14 I would like to jump to Page 97 of your report. 15 A Okay. I am with you. 16 Q Page 97 begins your analysis of Claim 10 correct? 17 A Yes. 18 Q Claim 10 recites, "The shader of Claim 7, wherein the 19 control signal is provided by an arbiter." 20 Do you see that? 21 A Yes, I do. 22 Q Again, you point to the sequencer as satisfying the
66 1 Paragraph No. 156, I say, "The specification of the '454 2 patent discloses this element of Claim 6"-- okay. 3 Then I go on and specifically refer to fetching 4 texture data and other types of data from a memory. 5 Q Is the memory that you identified part of the store? 6 A So in this case one of the examples identified is texture 7 reservation stations. 8 That would not be generally considered part of the 9 store. 10 The texture memory is usually separate. 11 It's a larger memory from the GPU-- I'm sorry, from 12 the GPR, the general purpose register file. 13 Q So you used the term "usually." 14 Does that mean that it could be, in some instances, 15 part of the store? 16 A I haven't really considered it, just focused on the 17 patent claims as well as the R400 documentation. 18 Q Okay. Does the memory recited in Claim 6 have to be 19 separate from the store or could it be part of the store 20 that's recited in Claim 5? 21 A It suggests to me that it's separate from a legal point 22 of view.	68 1 arbiter of Claim 10, correct? 2 A Yes, the sequencer has an arbitration scheme, for 3 example, that we discussed earlier. 4 Q So in your opinion the arbiter recited in Claim 10 does 5 not have to be a separate component from the sequencer 6 recited in Claim 5, correct? 7 A I haven't really thought of it. 8 In general a sequencer doesn't have to include an 9 arbiter, and perhaps an arbiter doesn't have to include 10 sequencing, but in this case I have indeed identified the 11 arbiter as being the sequencer or the sequencer doing the 12 arbitration scheme. 13 Q Okay. And then jumping to Page 103 of your declaration, 14 Exhibit No. 2121-- 15 A All right. I'm there. 16 Q Here you are addressing Claim 11 of the '454 patent, and 17 specifically the limitation that states, "A processor 18 unit flexibly controlled to perform vertex manipulation 19 operations and pixel manipulation operations based on 20 vertex or pixel workload." 21 Do you see that? 22 A I do.

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69 1 Q And what did you understand the term "flexibly 2 controlled" to mean? 3 A My understanding is that it's-- the processor unit is not 4 rigidly controlled. 5 Q What would be the difference between flexibly and rigidly 6 controlled? 7 A Well, it could be the case that-- and in earlier designs 8 I have seen situations where the control would simply 9 alternate between a vertex operation and a pixel 10 operation. 11 A flexible control-- flexibly controlled, rather, 12 would allow a different sort of alteration. Maybe there 13 could be-- I'm sorry, a different sort of sequence; for 14 example, if there were more vertex operations, it could 15 respond by executing more vertex by actually performing 16 more vertex operations. 17 Q Does "flexibly controlled" refer to the configuration 18 within the processing unit? 19 A It might. It depends on, again, partially a box drawing 20 exercise, what is identified as-- what is considered in a 21 particular situation to be the processor unit. 22 There could be flexible control both within and	71 1 A Yes, I do. 2 Q And my understanding, from your declaration, is that you 3 construe that phrase to mean "unfinished"; is that 4 correct? 5 A Yes, or, I guess, at least to include unfinished. 6 Whether a finished instruction is in some degree of 7 completion, it may include that as well, but it must 8 include unfinished. 9 Q Okay. And is that the understanding that you applied 10 when forming the opinions in your declaration? 11 A Yes. 12 Q I am going to go backwards a little bit to Paragraph 13 No. 29 of your declaration. 14 A I am there with you. 15 Q The first sentence of Paragraph No. 29 mentions vertex 16 and pixel threads. 17 Do you see that? 18 A Yes, I do. 19 Q Do you agree with me that the '454 patent never uses or 20 mentions the word "threads"? 21 A No, I wouldn't agree with that. 22 Q Okay. So let's look at the citation you give, which is
70 1 without. 2 Q Well, for example, some of the claims require a sequencer 3 that does things to cause the processor unit to perform 4 operations, correct? 5 A Yeah, I think that's generally accurate. 6 Q And so my question to you is: 7 When reading this limitation, "a processor unit 8 flexibly controlled," did you construe that to mean that 9 it was configured in such a way within the processor or 10 that it was being controlled by some other component, 11 such as the sequencer? 12 Where is the flexibility coming from? 13 A I would say yes. 14 Q Is it both? 15 A It's "or." 16 It's flexibly controlled. It could be inside the 17 processor. It could be inside, for example, in the case 18 of the R400, the sequencer. 19 Q Okay. And then the next limitation, which is identified 20 on 104 of your declaration, has a phrase in it that says, 21 "Various degrees of completion." 22 Do you see that?	72 1 in Exhibit No. 1001 at Column 2, starting at Line No. 58 2 and going to Line No. 61, which states, "Briefly stated, 3 the present invention is directed to a graphics processor 4 that includes a unified shader that is capable of 5 performing both the vertex operations and the pixel 6 operations in a space saving and computationally 7 efficient manner." 8 Did I read that correctly? 9 A Yes. 10 Q And that sentence doesn't have the word "threads" in it, 11 right? 12 A That's correct. 13 Q So can you point me to some other sentence in the '454 14 patent that uses the term "threads"? 15 A Perhaps. 16 I think the concept is there and, in fact, was just 17 discussed, but if you're seeming to look for literally 18 the word "thread," I couldn't agree with your question 19 earlier because I simply don't recall. 20 Q Paragraph No. 30 of your declaration states, "The unified 21 shader's sequencer stores the individual instructions 22 that, when sequenced together, comprise the vertex and

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73 1 pixel threads that the unified shader will use to 2 manipulate and transform the stored vertex and pixel 3 data," correct? 4 A Yes. 5 Q And so is it your opinion that individual-- strike that. 6 Is it your opinion that sets of sequenced individual 7 instructions are what comprise a thread? 8 A It's my opinion-- no, I wouldn't characterize it that 9 way. 10 Q So what's the definition of a "thread"? 11 A Well, a thread is, for example, sometimes referred to as 12 a process. 13 A thread is a particular sequence of instructions 14 that corresponds to an element of a program while 15 executing, so a thread must be associated with execution 16 context. 17 Q Can a single instruction be a thread? 18 A Possibly. 19 It seems unlikely, but it really depends on what the 20 particular instruction set comprises. 21 It's likely the case that a single instruction could 22 be a useless thread, but it may, in fact, be able to do	75 1 questions of, I would say, subtlety that make it 2 impossible to answer completely. 3 Q What questions are you referring to? 4 A Well, for example, a person might think of 5 multi-threading-- a person of ordinary skill in the art 6 might think of multi-threading simply meaning that a 7 processor is able to execute more than one thread. I 8 think by its nature it would require some condition in 9 which it operated on more than one thread. 10 However, that operation might be closely interleaved 11 within hardware control. It may be less closely 12 interleaved under software control. It may be completely 13 not interleaved under software control, probably hardware 14 as well. 15 Q So I want to turn to Page 16 of your declaration. 16 I am looking at Paragraph No. 32. 17 In this section of your declaration you are no 18 longer talking about the R400, but you are actually 19 describing the unified shader that is disclosed within 20 the '454 patent itself, correct? 21 A I believe that's correct. 22 Q And in the second sentence of Paragraph No. 32 you state,
74 1 useful processing, in general. 2 Q All right. Later in Paragraph No. 30 there is a sentence 3 that says, "The resulting threads are called vertex and 4 pixel 'manipulation operations.'" 5 Can you explain that sentence to me? 6 A Sure. 7 The threads, which is-- a thread is going to be 8 either a vertex program or a pixel program that happens 9 to be executing in the context of a particular set of 10 data. 11 For example, the sequencer will select data 12 associated with a vertex thread, and that will be the 13 vertex information, and when conditions are appropriate, 14 it will write that data, having selected it, into the 15 GPR, and then at some point in the future it will start 16 to direct the processor to execute the instructions 17 associated with that thread. 18 Q Is it your opinion that the '454 patent discloses a 19 unified shader that is multi-threaded? 20 A I would say I believe so. 21 However, I don't believe that term is used in 22 context here, and multi-threading-- there's some	76 1 "The arbiter's selection criteria, or 'arbitration 2 scheme,' includes at least the capacity to store 3 particular types of data." 4 Do you see that? 5 A Yes, I see that. 6 Q So what is the arbiter's selection criteria within the 7 '454 patent specification? 8 A It is the arbiter that determines generally, based on 9 available storage of one sort or another, whether to pick 10 the-- whether to select the data associated with the 11 start of a particular vertex thread or a particular pixel 12 thread. 13 Q And that selection being done by the arbiter is for the 14 purpose of placing that data that is selected into the 15 general purpose register block, correct? 16 A That is one of the purposes of the arbiter, yes. 17 Q Is there another purpose stated in the '454 patent? 18 A There might be. 19 I don't recall. 20 Q So the arbiter is evaluating the available space in the 21 general purpose register block, and then based on that 22 evaluation making some determination about what type of

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77 1 data to place into the general purpose register block, 2 correct? 3 A Yes, based, at least in part, on that information. 4 Q And then after it makes that determination, it will then 5 cause that selected data to be transferred into the 6 general purpose register block, correct? 7 A Yes, after determining what type of data should be 8 selected, it will pass that on to— it will pass that 9 data on to the various claims, I think— call it a store 10 or a general purpose register. 11 Q I want to look at Figures 4A and Figure 5 in the '454 12 patent, which is Exhibit No. 1001. 13 A Okay. 14 Q So let's just sort of get on the same page to begin with. 15 Do you agree with me that Figure 4A is a block 16 diagram showing the overall graphics processor 17 architecture for the '454 patent? 18 A That seems accurate. 19 Let me just take a quick look at how they describe 20 4A. 21 Yeah, on Column 2 it says, "4A is a schematic block 22 diagram of the graphics processor architecture, according	79 1 I was just going to say this is in accordance with 2 the claims, but there are other embodiments of the— I'm 3 sorry, in accordance with the inventions disclosed in the 4 '454 patent, but it doesn't have to be representative of 5 all such inventions. 6 Q And just to place Figure 5 into context of Figure 4A, at 7 the top of Figure 5 is something that says, "From MUX" 8 with a Line 65 coming down, so that's where we can see 9 where it would be placed into Figure 4A, correct? 10 A That's correct. 11 Q All right. And then within Figure 5, I just want to get 12 all the terminology down so later when we're referring 13 back, we are on the same page, Item 92 within Figure 5 is 14 what is referred to as the general purpose register block 15 that may other times be referred to as the store, 16 correct? 17 A That seems right. 18 Is there a particular location you could point me to 19 just to confirm that? 20 Q Sure. 21 A I certainly believe that's accurate. 22 Q So if you look at Column 4, starting on Line No. 29, it
78 1 to the present invention." 2 Q Okay. And as indicated in Figure 4A, there's a unified 3 shader designated as Item 62, correct? 4 A Yes. 5 Q And there's also an arbiter 64? 6 A Yes. 7 Q And a MUX as Item 66, correct? 8 A Yes. 9 Q And can you just tell me what a MUX is? 10 A Yeah. "MUX," M-U-X, stands for "multiplexer." 11 That is a circuit that will take more than one input 12 and then, using a control signal, select well less than 13 the number of inputs-- usually it just selects one 14 output. 15 Q Okay. And then Figure 5 is, according to Column 2, an 16 exploded schematic block diagram of the unified shader 17 employed in the graphics processor illustrated in Figure 18 4A that we were just looking at, correct? 19 A Yes, I believe that's accurate. 20 Q So Figure 5 will show the various components of the 21 unified shader of the present invention, correct? 22 A Yes.	80 1 says, "Referring briefly to Figure 5, the unified shader 2 62 will now be described. As illustrated, the unified 3 shader 62 includes a general purpose register block 92." 4 A Yes, I see that. 5 Q Okay. So I believe you asked me also to show you where 6 it's referred to as the store, but I don't see that. 7 Do you? 8 A Oh, I don't know. 9 I don't recall asking that. 10 I do believe that in the nomenclature of— a person 11 of ordinary skill in the art would understand a memory of 12 this sort to also be a store. 13 Q Within the context of Claim 5, which refers to a 14 sequencer that maintains instructions and they're 15 maintained in a store, is that referring to Item 92 in 16 Figure 5 or is that referring to the instruction store 98 17 in Figure 5? 18 A It is talking about a store that holds data, not a store 19 that holds instructions, Claim 5. 20 So that would be— well, it wouldn't be 98, but it 21 would be— it could be 92, sure. 22 Q Okay. So that's what I was just trying to get back to.

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81 1 I think the store referred to in the claims is also 2 called the general purpose register block in the patent, 3 correct? 4 A I don't know if they're always used interchangeably, but 5 there certainly is significant overlap. 6 Q Okay. 7 A I could think-- I know of stores that would not be called 8 a general purpose register file. I don't know if they 9 would fit the other claim limitations. 10 Q Okay. While we are at it, Box 99, in Figure 5, you 11 understand that to be the sequencer, correct? 12 A Yes, that's my understanding. 13 Q And Box 96, that's labelled, "CPU," you would understand 14 that to be a processor? 15 A Yes, and this would be an example where I discussed where 16 the box for the processor would be separate from the box 17 for the GPR. 18 Q Okay. And in the context of the claims, did you 19 understand Box 92 to be the processor unit? 20 A I am sorry, could you repeat the question? 21 Q Sure. 22 Let me just piece it out for you.	83 1 A Well, one example of shared resources, and I think one 2 that's relevant to the claims, are the storage space in 3 the register file 92. 4 For example, you will see it indicates 64 available 5 registers of some size, and those are shared among all of 6 the threads that are, at any particular point in time, 7 configured such that instructions from them can be 8 executed by the arbiter. 9 Q Are instructions stored in Item 92 or is just data? 10 A Generally just data. 11 In this context it's just data. 12 There are situations where instructions are operated 13 upon as if they were data, but we're not talking about 14 situations like that. 15 Q I was just trying to clarify your statement because you 16 said, "Instructions from the registers could be 17 executed," and so I just wanted to make clear that we're 18 talking about data in the registers. 19 A Yeah, typically instructions are not coming out of 20 element 92. 21 Q Okay. And what about the registers 93, 95, and 97, would 22 you consider those to be shared resources within the
82 1 Some of the claims refer to a processor unit, 2 correct? 3 A Yes. 4 Q Not just a processor? 5 A Yes. 6 Q And so all I'm asking is: 7 When you look to Figure 5, would you understand 8 Box 92 to be that processor unit-- I'm sorry, Box 96. 9 A Okay, that was my confusion. 10 Yeah, in this exemplar of the claimed inventions, it 11 is my understanding that Box 96, marked "Central 12 processing unit," is the processing unit or processor 13 unit. 14 Q And then there are some additional registers that are 15 shown as Boxes 93, 95, and 97, correct? 16 A Yes. 17 Q Now, some of the claims refer to something called share 18 resources. 19 For example, that's cited in Claim 3. 20 A Yes. 21 Q What would you identify in Figure 5 of the shared 22 resources?	84 1 context of Claim 3? 2 A Not really, not as I recall them being utilized here. 3 Q Could shared resources, within the context of Claim 3, be 4 resources outside of the unified shader? 5 A Not that I see. 6 I don't know how that would work or how the 7 arbiter-- how it would fit the other claim limitations, 8 for example, how the arbiter would know what shared 9 resources were available. 10 Q Okay. So if you would turn to Page 17, Paragraph No. 34 11 of your declaration in Exhibit No. 2121-- 12 A I'm there. 13 Q And the first sentence says, "The claims require this 14 functionality in a variety of different ways, with 15 different levels of specificity." 16 What functionality are you referring to in that 17 sentence? 18 A I believe it's referring to the functionality discussed 19 in the immediately-- at least in the immediately 20 preceding paragraph; i.e., Paragraph No. 33, which is 21 talking about, for example, pixel calculation operations 22 that are to be or are currently being performed by the

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85 1 processor based on instructions maintained in the 2 instruction store until enough registers within the 3 general purpose register block become available. 4 So this is getting back to the issue of doing 5 arbitration control, to some extent, and selection, to 6 some extent, based on how much space is available to be 7 used in the GPR or the store. 8 Q And then Paragraph 34 goes on to give some examples, 9 starting with Claim 1, correct? 10 A Yes. 11 Q And you state that Claim 1 requires two evaluations: 12 first, that there is no longer room for additional vertex 13 data; and then, second, that at a later point in time 14 there is once again room for additional vertex data in 15 the general purpose register block, correct? 16 A Yes, I see that. 17 Q So those two evaluation steps are requirements of Claim 18 1, under your interpretation, correct? 19 A It certainly seems to say that, yes. 20 Q And is that based on a particular construction-- strike 21 that. 22 Are those two required evaluation steps based on	87 1 Do you see that? 2 A I do. 3 Q And then there is an "unless" clause, and if that 4 "unless" clause is met, then there is a continuing step 5 to the method, correct? 6 A Yes. 7 Q But whether it's called by "evaluation" or some other 8 word, there's no evaluation steps recited in Claim 1, 9 correct? 10 A No, that's incorrect. 11 Q Okay. Where is the evaluation step recited, in your 12 opinion, in Claim 1? 13 A Well, at a minimum where it says, "Unless the general 14 purpose register block does not have enough available 15 space therein to store incoming vertex data," that is an 16 evaluation step. It is evaluating whether there is 17 enough available space to store incoming vertex data. 18 Q Okay. So in your opinion then, this phrase, the "unless" 19 phrase, is what must be construed to require both of 20 those evaluation steps that we talked about earlier, 21 correct? 22 A No. I would say that requirement comes from, likely, the
86 1 your construing any particular term or phrase within 2 Claim 1? 3 A Not any one in particular. 4 It relies upon my understanding, and I guess it's 5 construction of all of the terms and all of the 6 limitations, but not an explicit construction. 7 Q So then you would say that those two claim requirements 8 are just inherent in the plain language of the claim 9 itself? 10 A I think that's generally accurate. That's how I 11 understand the claims to operate. 12 Q You would agree with me that Claim 1 doesn't specifically 13 recite any evaluation steps, correct? 14 A Give me a moment. 15 In my review here, I certainly would agree that the 16 word "evaluation," let alone the term "evaluation steps," 17 does not appear in Claim 1. 18 Q So Claim 1 is a method claim, correct? 19 A Yes, it is. 20 Q And there is a performing step in which the unified 21 shader must perform vertex manipulation operations and 22 pixel manipulation operations.	88 1 entire claim, but perhaps only the first limitation 2 that's listed, the entire limitation titled, "Performing 3 vertex manipulation operations," et cetera. 4 Q So looking at the first step, which is "Performing vertex 5 manipulation operations and pixel manipulation 6 operations," does the claim require that those two 7 operations be carried out or executed at the same time? 8 A "At the same time" is a concept that is not-- I'm not 9 sure what you're asking, let's put it that way, because 10 instructions can be at various-- operations, rather, can 11 be at various stages of completion. 12 Q Could I perform a vertex manipulation operation, have it 13 completed, and then perform a pixel manipulation 14 operation, let it be completed, and would that two-step 15 process satisfy the performing vertex manipulation 16 operations and pixel manipulation operations of a claim? 17 A That would be an example of performing vertex 18 manipulation operations and pixel manipulation operations 19 in the context of Claim 1, yes. 20 Q Okay. What do you understand the phrase "by transmitting 21 vertex data to a general purpose register block" to mean 22 in that first clause of Claim 1?

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89 1 A Well, I think "by transmitting vertex data to a general 2 purpose register block" means that the vertex data needs 3 to be sent, written into the general purpose register 4 block. 5 Q So the phrase, "Performing vertex manipulation operations 6 and pixel manipulation operations by transmitting vertex 7 data to a general purpose register block"-- it's all one 8 phrase, correct? 9 A Yes, although it's not clear to me-- that is one phrase. 10 I think that the next phrase, "And performing vertex 11 operations, et cetera," would generally be understood to 12 be an example of performing vertex manipulation 13 operations. 14 Q I see. 15 So the phrase, "by transmitting vertex data to 16 general purpose register block" is just the setup to do 17 the "performing operations" in the next clause, correct? 18 A That's generally my understanding, yes. 19 It's certainly in the case where-- I don't recall if 20 it comes up here, but there is a discussion of the 21 arbiter selecting data or a sequencer selecting data. 22 Q Okay. And then there's this phrase, "Unless," and then a	91 1 alleged infringing device, one has to point to the 2 operations actually being practiced. 3 Q Okay. And if I was looking at an alleged infringing 4 device, and it never ran out of enough available space in 5 the store, then I would satisfy this claim by simply 6 performing vertex manipulation operations and pixel 7 manipulation operations, correct? 8 A I'm sorry, could you repeat the question? 9 Q Sure. 10 So there's an "unless" clause, right? 11 A Yes. 12 Q And that "unless" identifies a condition that needs to be 13 met in order to move to the next part of the method 14 steps, correct? 15 A It's required in order to do-- execute pixel operations, 16 yeah. 17 Q Okay. So-- well, let me just unpack your statement. 18 Are you saying that prior to the "unless" condition, 19 the claim does not require any pixel operations? 20 A That seems to be the case. 21 It's only talking about performance vertex 22 operations unless there's no more room for vertex data.
90 1 bunch of stuff that comes after it, correct? 2 A Yes. 3 Q And what does the term "unless" mean to you in the 4 context of Claim 1? 5 A I think it means the general description prior to 6 "unless" is operable, unless the conditions following the 7 "unless" are met. 8 Q Okay. So this is a conditional transition in the claim, 9 correct? 10 A It's a conditional step, yes. 11 Q So if the condition is not met, then this limitation is 12 not necessary for the claim, correct? 13 MR. DOKHANCHY: Objection; vague, 14 calls for a legal conclusion. 15 THE WITNESS: No, I think that's 16 wrong. 17 This is-- yeah, this is a legal interpretation, but 18 my understanding with method claims-- yeah, I guess I'll 19 leave it there. 20 I don't-- yeah, I'll leave it there. 21 Q (By Mr. Johnson) It's a method claim, correct? 22 A It's a method claim, so if one wants to point to an	92 1 Q Okay. So the condition that is identified by the 2 "unless" clause is that there is not enough available 3 space in the store for incoming vertex data, correct? 4 A That's correct. 5 Q And if I had, for example, a large enough store, and I 6 had not-- and I did not run out of available space, then 7 I would not have to move to these conditional steps, 8 correct? 9 A Perhaps, in which case you would never do any pixel 10 operations. 11 Q Okay. So under that scenario, where the condition is not 12 met, then the only thing I would have to do for this 13 method claim is perform the steps that are identified 14 prior to the "unless" clause, correct? 15 MR. DOKHANCHY: Objection; calls for a 16 legal conclusion. 17 THE WITNESS: Yeah, to be honest, I'm 18 not sure about that, but it's also premised on the notion 19 that there's an unlimited amount of vertex storage, which 20 is not practical, and also the preamble says it's a 21 unified shader, and shading involves both vertex and 22 pixel operations, arguably pixel operations even more

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93 1 than-- I think I might have mispronounced that. 2 It involves both vertex operations and pixel 3 operations, and pixel operations are arguably more 4 shading than vertex operations, to a certain degree. 5 Q (By Mr. Johnson) When forming your opinions, did Counsel 6 provide you with any legal principles about how to 7 interpret claims that have conditional limitations? 8 A In the context of the condition that we see in Claim 1, I 9 do not recall having any specific discussion of that. 10 Q Okay. 11 A Actually, now that I think about it, the first limitation 12 says, "Performing vertex manipulation operations and 13 pixel manipulation operations," and then it goes on to 14 describe one aspect of that, and then the "unless" is 15 used to describe another aspect of that, but it is saying 16 that you have to do vertex manipulation operations and 17 pixel manipulation operations, and that requires that 18 both sides of the "unless" be operable. 19 Q Okay. So let's keep looking at this "unless" phrase in 20 Claim 1. 21 It refers to "enough available space," correct? 22 A Yes.	95 1 Q And you said, "at least to start execution." 2 Is it possible that you could place just enough data 3 into two registers out of four for it to start and then 4 later fill the other two registers? 5 A No. If it's indicating it requires four registers to 6 start, you need to have four registers available. 7 Q I am trying to distinguish what "to start" means. 8 Are you trying to say that you can somehow have 9 enough space just to start the operations but not have 10 enough space for the entire vertex operation set of data? 11 A I'm just thinking hypothetically one could imagine a very 12 long-running thread that required a certain amount of 13 storage to start, and at some later point may or may not 14 require additional storage, but I haven't seen any 15 examples of that either in the '454 patent or the 16 materials reviewed. 17 Q How does space become available in the general purpose 18 register block? 19 A Well, a thread that has been allocated that space 20 terminates, and so whatever space was allocated to it is 21 now for re-use, so it's available to other threads. 22 Q And forgive me for my crude discussion, this is not going
94 1 Q And what is the meaning of "enough" in the context of 2 this claim? 3 A Well, let me start with "available space." 4 That means that the store, the general purpose-- I'm 5 sorry, the general purpose register block has storage 6 locations within it that are not currently allocated to 7 threads. Nobody is depending upon them maintaining data. 8 Then "enough available space" means that the 9 particular vertex operation thread that's being 10 considered requires a certain amount of space, and there 11 has to be that much space available within the general 12 purpose register block. 13 Q Okay. So there has to be enough space to put in a 14 complete set of data for a particular vertex operation; 15 is that what you're saying? 16 A Well, at least whatever size block of vertex data is 17 required to start execution of the vertex program or the 18 vertex thread, yes. 19 The vertex thread will indicate-- for example, it 20 requires four registers. Well, then there must be four 21 registers available before it gets placed in. It may 22 also indicate that it only required one register.	96 1 to be very technical, but I imagine that-- let's say the 2 registers are all full, something gets-- a thread gets 3 terminated in use, so a little bit of space becomes 4 available, so now I can place a new incoming set of 5 vertex data into that available space, but immediately 6 doing that, I'm now out of available space again, 7 correct? 8 A It depends. 9 It could be the case-- that may very well be what 10 happens in a particular instance. 11 The thread that ended might be a pixel thread, and 12 maybe all pixel threads use the same amount of space and 13 all vertex threads use the same amount of space, but 14 they're different. Pixels use four and vertices use two. 15 If you allocate a vertex thread to it, you would 16 still have two entries available. 17 Q So if I don't have enough space available in my general 18 purpose register block, such that I'm now within this 19 "unless" conditional part of the limitation, does the 20 claim require that I then cease performing vertex 21 operations and only do pixel operation? 22 A Well, certainly any vertex operation threads that are

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97 1 currently in execution will continue to execute, but my 2 understanding is that new vertex threads couldn't be 3 selected and allocated to the GPR and activated. 4 Q Okay. Just so I can clear that up, so any vertex data 5 that's already in the general purpose register block can 6 be executed; is that what you're saying? 7 A Can be executed upon by whatever the vertex threads are 8 that are in the middle of processing. 9 Q Whether they had been started already or whether they're 10 about to be started, correct? 11 As long as it's already in the general purpose 12 register block, it could be executed, correct? 13 A Yeah, in general, that's my understanding of Claim 1. 14 Q Okay. And then, likewise, the next step in the method 15 says, "Continuing pixel calculation operations that are 16 to be or are currently being performed." 17 I take that to mean that anything already within the 18 general purpose register block can be executed in terms 19 of pixel operations. 20 A I wouldn't—I think I know what you're saying. 21 I wouldn't phrase it that way. 22 For example, if there were four vertex threads that	99 1 about various aspects of Claim 1, and we mentioned or we 2 were discussing the two evaluation step requirements that 3 you identify in Paragraph No. 34 in your declaration. 4 Do you recall that? 5 A Yes. 6 Q With respect to the '454 patent specification, what 7 component carries out those two evaluation steps? 8 A Well, in the context of Claim 1, it's a method claim, so 9 there doesn't have to be a particular—at least as I 10 understand it, a particular component identified. There 11 just has to be a determination made. 12 Q Right. 13 I'm just trying to find the disclosure of those 14 steps in the specification. 15 If you could, just point me to where those things 16 happen in the specification, and that would be great. 17 A I will give it a look. 18 I don't recall, as I sit here, but I'll also say 19 that it's not something that would allude or challenge a 20 person of ordinary skill in the art. 21 So in Column 4, around about Line No. 22, it says, 22 "The arbitration scheme employed by the arbiter 64 is as
98 1 were currently active in the processor, their input data 2 had been selected and written to the GPR, then likely one 3 of them is currently executing an operation. 4 The other ones are all ready to execute operations 5 in the future, and so both of those scenarios are allowed 6 to go forward. 7 Q Okay. The phrase "maintained in the instruction store," 8 I assume that "maintained" just means it's stored there, 9 correct? 10 Is there any further meaning to the word 11 "maintained"? 12 A I don't think so. 13 Okay. Yeah, I don't think there's any further 14 meaning. 15 It strikes me as a little odd that it doesn't have 16 the same element in the first clause, but I don't think 17 it matters. 18 MR. JOHNSON: All right. Do you want 19 to break now? 20 THE WITNESS: Sure. 21 (Lunch recess 12:35 to 1:17 p.m.) 22 Q (By Mr. Johnson) Before the lunch break we were talking	100 1 follows: The vertex data on the first input of the 2 multiplexer is transmitted to the unified shader 62 on 3 Line 65 if there is enough resources available in the 4 unified shader to operate on the vertex data." 5 I read that to suggest that they anticipate it being 6 done-- the determination to be done by the arbiter, which 7 makes sense to me, given the rest of the elements of the 8 system. 9 The processor, for example, seems to only operate on 10 what it perceives as its available registers. The GPR 11 just has its registers allocated. 12 The sequencer or arbiter would be the most likely 13 place to keep track of what threads were currently 14 running and what resources they were currently using. 15 Q Okay. So the arbiter 64 would then be the one that 16 evaluates or monitors the available space, and then when 17 it determines that there's enough available space, it 18 will select data to fill that space? 19 A Sure, that seems like the most reasonable place to 20 implement that. 21 Now, it's possible, for example, that some other 22 portion, which wouldn't be identified as the arbiter,

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101 1 does the determination— tracks the available space, and 2 then the arbiter itself makes a determination of "Well, 3 is there enough space available to start the next 4 thread?" 5 I mean, it seems to me it has to be in the arbiter 6 because the arbiter is the place that knows what 7 resources are needed for a thread that it might have 8 available to start. 9 Q I think there's another sentence that probably tracks 10 with what you're saying as well, and that's in Column 5 11 around Line No. 41. 12 It says, "However, if the general purpose register 13 block 92 does not have enough available space therein to 14 store the incoming vertex data, such information will not 15 be transmitted as the arbitration scheme of the arbiter 16 is not satisfied." 17 A Yeah, I can imagine it may be a situation where the GPR 18 itself reports actively what space is free, but that's 19 pretty complicated. 20 It's just much easier for the arbiter to keep track 21 of it. 22 As it starts up a thread, it keeps track of which	103 1 of which ones are available and the arbiter just makes 2 the determination, "Of the ones available, is it big 3 enough to start the vertex?" 4 Q I didn't see any disclosure of that embodiment either in 5 the '454 patent, did you? 6 A No. 7 Q Okay. Earlier I think we were talking, in the context of 8 Claim 1, about the conditional statement and whether or 9 not it meant that vertex operations had to cease before 10 we started pixel operations, and you said that wasn't the 11 case, correct? 12 A That's right, I believe it's not the case. 13 Q I just want to clarify that you believe that's also true 14 for the remainder of the claims as well? 15 A I am not sure I understand the question. 16 Q Sure. 17 For example, in Claim 3, the processor unit clause-- 18 do you see that? 19 A Yes, I do. 20 Q It says, "The processor unit operative to use the shared 21 resources for either vertex data or pixel information and 22 operative to perform pixel calculation operations until
102 1 registers are free and which are not. 2 Q I didn't find anything in the '454 patent specification 3 in which the arbiter was informed by some other 4 component, say the register blocks themselves, that they 5 had available space or didn't have available space. 6 Did you? 7 A By the register blocks themselves, no. 8 I wouldn't expect that to be the case. 9 Q The only disclosure I found was that the arbiter-- to the 10 extent any evaluation is being done, the arbiter seems to 11 be the one that's monitoring the space and then making a 12 determination on what to select and put into the 13 registers based on that evaluation. 14 A Yeah, I think the arbiter at least has to do the second 15 part. It's looking at a thread that might be able to run 16 and determines whether there's available space. 17 It wouldn't be unreasonable to perhaps have the 18 sequencer— the sequencer and the sequence functions in 19 the arbiter work very closely together, and as we talked 20 about, maybe they're the same physical unit, maybe their 21 box is drawn so that they are separate. 22 It could be the case that the sequencer keeps tracks	104 1 enough shared resources become available and then use the 2 shared resources to perform vertex calculation 3 operations." 4 Do you see that? 5 A Yes, I do. 6 Q So do you interpret that last phrase where it says, 7 "until," to mean that it's going to shift from pixel to 8 vertex operations or do you interpret that to just mean 9 it can now start vertex operations at the same time or in 10 parallel with pixel operations? 11 A So it's my understanding that, for example, if there is 12 no space available for vertex operations, it will execute 13 pixel operations. 14 Let's imagine it's currently executing what I would 15 call three different pixel threads, and one of them 16 terminates, and now there is enough space to accept a 17 vertex thread. 18 So the vertex thread would be started, but the pixel 19 threads will be allowed to— they won't be stopped. They 20 will be allowed to finish their work. 21 Q Okay. I'm just going to jump to Page 238 for a second. 22 A Okay.

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105 1 Q You have a sentence in the middle of Page 238 that says, 2 "For example, the specification explains." 3 Do you see that sentence? 4 A I do. 5 Q Can you tell me what that sentence means? 6 A Okay. 7 Q Because it doesn't look like to be a real sentence to me. 8 A Okay. Let me review. 9 I think that probably the "and" in the middle of it 10 is superfluous. 11 Q Okay. So still looking in that little section of your 12 report, you're discussing Claim 5. 13 Claim 5 is up above that. 14 Do you see that? 15 A Yes. 16 Q And you state, "There is no process in Amanatides or Kohn 17 for selecting data from a data store." 18 Do you see that? 19 A Yes, and I meant selecting it in the way discussed in the 20 claim. 21 Q Okay. So I think we discussed earlier that in the '454 22 patent the selection that is talked about with the	107 1 Q So if I execute data from the register block, and I 2 happen to execute some of the selected data, then I would 3 be satisfying the claim limitation to execute selected 4 data, correct? 5 A Maybe. 6 Let me see. 7 Sure. If the processor executes vertex calculation 8 and pixel calculation operations on selected data, it 9 will have done those operations on the selected data. 10 Q Okay. There is a phrase that's repeated in many of the 11 claims of the '454 patent that says the words "operative 12 to." 13 Do you recall that? 14 A Sure. 15 Q So, for example, in Claim 2, in the sequencer limitation, 16 there is a phrase that says, "The sequencer maintaining 17 instructions operative to cause the processor unit to 18 execute"-- various operations. 19 Do you see that? 20 A I do. 21 Q Did you formulate an opinion as to what the phrase 22 "operable to" meant in the '454 patent claims?
106 1 selected data is the selection by the arbiter from a 2 bunch of data to then place that data into the store or 3 the general purpose register block, correct? 4 A Yes, but under the other limitations that has to be done, 5 for example, depending upon an amount of space available 6 in the store. 7 Q Understood. 8 But Claim 5 doesn't have any recitation of an 9 arbiter, right? 10 A It does not use the word "arbiter." 11 Q So we had discussed earlier that data sitting in the 12 general purpose register block has already been selected, 13 correct? 14 That's how it got into the block? 15 A Some of the data in the general purpose register block 16 was selected and placed there by the sequencer or the 17 arbiter, as part of starting up the thread, not all of 18 the data in the general purpose register file though. 19 Q All right. So some of it is selected and some of it may 20 not be selected, but it's all just sitting in the 21 register block, correct? 22 A Sure.	108 1 A I did not conduct an independent claim construction for 2 that term. 3 Q Okay. 4 A I think it just means-- well, I think its meaning is 5 clear. 6 Q Do you think that just means "capable of"? 7 A That, I'm going to be careful of because I know that 8 there's a distinction, for example, between "capable of" 9 and "configured to," and "configured to" is not at issue 10 here, but I'm just leery of stepping into some other 11 distinction among those terms that is made outside of the 12 context of this matter that I may not be aware of. 13 Q Sure. 14 If you look at Column 6, Line No. 29-- 15 A I'm there. 16 Q It says, "As discussed above, the graphics processor 60 17 of the present invention incorporates a unified shader 62 18 which is capable of performing both vertex manipulation 19 operations and pixel manipulation operations based on the 20 instructions stored in the instruction store 98." 21 Do you see that? 22 A Yes, I do.

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109 1 Q A little bit further on, in Line No. 36, there is another 2 sentence that says, "In addition, as the unified shader 3 62 is capable of alternating between performing vertex 4 manipulation operations and pixel manipulation 5 operations"-- and it goes on. 6 Do you see that? 7 A Yes. 8 Q Again, both of those sentences are disclosing "capable 9 of," correct? 10 A Yes. 11 Q And if you were to look at Column 2, Line No. 58, it 12 says, "Briefly stated, the present invention is directed 13 to a graphics processor that employs a unified shader 14 that is capable of performing both the vertex operations 15 and the pixel operations in a space-saving and 16 computationally efficient manner." 17 Do you see that? 18 A I do. 19 Q Again, it's disclosing this conception of "capable of," 20 correct? 21 A Yes, it's talking about-- using the word "capable of," 22 yeah.	111 1 the processing unit, might be outside the processing 2 unit, and if it was outside the processing unit, it could 3 just have access and go and retrieve the data. 4 I think that's the word you used earlier? 5 A Mm-hm. 6 Q Or it could be sent the data, correct? 7 A Yes. 8 Q We talked about three or four different embodiments 9 around that situation. 10 Do you recall that? 11 A I do. 12 Q And I believe your testimony was that the '454 patent 13 wasn't express about any one of those particular 14 embodiments, other than the fact that it does not show 15 the general purpose register block as being within the 16 processing unit, correct? 17 A I'm not sure I follow the question. 18 Q Sure. 19 So you agree with me that the general purpose 20 register block, as described in the '454 patent, is not 21 described as being integrated within the processing unit, 22 correct?
110 1 Q Let's go back to Claim 2 and turn to Paragraph No. 41 on 2 your report, which starts at Page 19 of-- sorry, your 3 declaration. 4 A Okay. I'm there. 5 Q So in Paragraph No. 41 you discuss how the '454 patent 6 provides for receipt of selected data, correct? 7 A Yes. 8 Q And then in Paragraph No. 42 you talk about this phrase, 9 "In response to selected data." 10 Do you see that? 11 A Yes. 12 Q So is it your opinion that the phrase "in response to 13 selected data" in Claim 2 requires the steps of receiving 14 selected data by the processing unit? 15 A Yes. You can't start a thread-- you can't start 16 execution for any operation related to a particular 17 vertex or a particular pixel until it has received that 18 data that was selected as input related to the vertex of 19 the pixel. 20 Q Earlier we had a discussion about the processing unit, 21 and you mentioned several different types of embodiments 22 where the general purpose register block might be inside	112 1 A I think that's accurate with regards to Figure 5. 2 I don't recall if it's consistent throughout the 3 rest of the specification. 4 Q And so in that situation the data either has to be sent 5 to the processing unit or it can simply be retrieved by 6 the processing unit, correct? 7 A Yes, I think that's generally accurate. Yeah. 8 Q Okay. And the '454 patent is silent as to which way is 9 required, correct? 10 A I think that's probably the case, yeah. 11 Q Okay. 12 A Figure 5 seems to suggest to me-- well, I guess I'll just 13 leave it at that. 14 It's a little bit-- yeah. 15 Q I am just trying to understand whether or not you believe 16 that there's some statement or teaching in the '454 17 patent that disclaims the processing unit retrieving its 18 own data and operating on it, from the general purpose 19 register block. 20 A I don't recall any such disclaimer. 21 Q Thank you. 22 I also wanted to understand-- I think we were

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113 1 looking at Figure 5, and in terms of the registers 93, 2 95, 97-- 3 A Mm-hm. 4 Q --does the processing unit operate on data that is placed 5 into those registers or does it operate it on data that's 6 still in the general purpose register block? 7 A I believe the answer is it does both. 8 Q Okay. Why would some of the data be moved to the 9 registers 93, 95, and 97, and others not? 10 A So you'll see there's one line coming out of 92 at the 11 bottom. There's no arrows on it to make it completely 12 clear as I would prefer it, but that pretty clearly 13 indicates to me that data comes out of GPR 92, but 14 there's only one line. 15 That's the simplest way to build a register file. 16 There's circuitry that will allow you to get one 17 piece of data out at a time. 18 Most instructions in general operate on at least two 19 pieces of data, and particularly for graphics, many of 20 them will use three pieces of input data, and that's what 21 they're showing here. 22 In that case, there's two possibilities.	115 1 I mean, we can go back in the description and see 2 how they define 93, but, yeah, I think that's just an 3 error. 4 Q Okay. So I agree with you, but you would understand that 5 the CPU is-- has access to those three registers to get 6 data from them, as needed, correct? 7 A Yes, but those are not general purpose registers, they're 8 not addressable, but it does have access to all three of 9 them. 10 Q And there is a line that goes from 92 down around, 11 bypassing those registers, to something called the 12 scaler. 13 Do you see that? 14 A I do. 15 Q And what is the scaler? 16 A That's for doing, I believe, integer operations as 17 opposed to what we call floating point operations. 18 Q And it's in a dotted box. 19 Is that supposed to indicate that it would-- under 20 some circumstances, the CPU would include a scaler? 21 A I don't recall for sure, but that's my understanding as I 22 sit here, yeah.
114 1 You could build what's called a three-ported 2 register file, which basically means repeating-- making 3 three complete copies of this large register file and 4 adding some additional circuitry, so you can immediately 5 get access to all three of those pieces of data at the 6 same time. 7 A simpler approach and more affordable in hardware 8 is to first get access to the first piece, but it's got 9 to be waiting around because you're not ready to do the 10 operation, so you stick it in register source A, then you 11 read the second piece, then you stick it in source B, and 12 then you read the third piece, and you stick it in source 13 C, and now the CPU has immediate access to all the input 14 data that it needs, so it does its operation. 15 Q And I am just curious, from source B to the CPU, there's 16 a line connecting them. It's not numbered. 17 A Yes. 18 Q And then from source C to the CPU there appears to be a 19 pathway to that as well, although it's not numbered. 20 There's no pathway from source A to the CPU. 21 Why is that? 22 A I think that's just an error.	116 1 Q Is that the way a person of ordinary skill would 2 understand, that a scaler would just be part of a 3 processor? 4 A Often it is, but there are plenty of designs that don't 5 have-- where that's not the case. 6 Q I am going to walk through some passages in the patent, 7 starting with Column 4, Lines 38 and 39. 8 A Okay. 9 Q It says, "The data present in the general purpose 10 register block 92 is transmitted to the plurality of 11 source registers via Line 109," correct? 12 A Yes, it does. 13 Q And those source registers are the registers 93, 95, and 14 97 that we were talking about earlier? 15 A Yes. 16 Q And then in Column 5, starting on Line No. 6, this 17 paragraph says-- I don't want to read the whole thing, so 18 I am just going to read portions, "The sequencer 99 19 causes the appropriate operands to be transferred from 20 the general purpose register block 92 into the 21 appropriate source registers -- 93, 95, 97 -- for 22 execution," correct?

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117 1 A I believe so, and that's consistent with my review of 2 Figure 5. 3 I am just having trouble-- this is Column 5, which 4 line? 5 Q We are talking about the first full paragraph, which 6 starts at Line No. 6. 7 A Okay. 8 Q So you can take your time and read it and let me know 9 when you're ready. 10 A Yeah, I see that. 11 This is talking about the condition where the 12 sequencer is causing the input data to be forwarded. 13 Q To the source registers, correct? 14 A Yes. 15 Q And then it says, "What happens next is an appropriate 16 signal is sent to the processor 96 on Line 101." 17 Looking at Figure 5, Line 101 is the connection 18 between the sequencer and the processor, correct? 19 A Yes. 20 Q So going back to Column 5, it says that that signal 21 "Indicates what operation or series of operations are to 22 be executed on the several operands present in the source	119 1 Q Because what I've been trying to talk about for a while 2 is whether or not the processor receives it, as in some 3 component sends it to it, or it can just simply access 4 the data. 5 Now let me restate my question. 6 A Okay. 7 Q Nothing in what we just read in Column 5 expressly tells 8 us whether the data was sent from the source registers to 9 the processor or whether the processor simply accessed 10 the data in the source registers, correct? 11 A As I understand Figure 5, it's suggesting both. 12 The sequencer is indicated to the GPU, and the 13 source registers retrieve an operands, stick it in source 14 A, source B, source C, then at that point the processor 15 has immediate access to it. 16 It doesn't go out and say, you know, "I need what's 17 in register seven." It just knows, "I need what's now in 18 those three source registers," and it uses that 19 information. 20 Q Okay. Is the signal that gets sent to the processor from 21 the sequencer on Line 101, that we just talked about, 22 what triggers the processor to begin execution?
118 1 registers," correct? 2 A Sure. 3 Q Does that indicate to you that the processor is going to 4 execute the data that's sitting in the source registers? 5 A Well, it's going to execute an operation on the data in 6 the source registers. 7 Q Okay. And then it says, "At this point the processor 96 8 executes instructions on the operands present in the 9 source registers," correct? 10 A Sure. 11 It's executing on the operands that were fetched 12 from 92, which may or may not be the selected data. 13 Q Okay. But none of that language tells us how the data 14 gets from the source registers into the processor, 15 correct, it leaves it silent? 16 A I don't think so. 17 I mean, Figure 5 is showing a connection. There's 18 nothing more that's needed, other than connecting the 19 outputs of source B, for example, to the source B input 20 of the CPU-- 21 Q Agreed. I think it's a bad question on my part. 22 A Okay.	120 1 A Well, if that signal is not sent, the processor doesn't 2 know what operation to execute, let alone when to start 3 it, but the triggering also happens as a result of those 4 three operands being loaded into the source registers, 5 and then you can continue back and say it's triggered by 6 the selected data being placed in the GPR. 7 Q But if the processing unit is never made aware that the 8 data is now in the source register, it won't do anything, 9 right? 10 A I mean, it's not really-- well, we don't know exactly 11 what bits are there. 12 I would anticipate-- it's not really told that there 13 is data in the source registers. It's just told "Execute 14 an add instruction," which might only use source A and 15 source B, so then it would just go and read whatever is 16 in those two registers, or it might be told, "Execute 17 what's called a 'multiply and accumulate instruction,'" 18 which uses three operands, so it would just use what's in 19 source A, source B, and source C. 20 You don't need to tell it explicitly that those 21 source registers are populated. It is implicitly 22 understood by being given the command, "Execute this."

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121 1 Q Sure, but it has to be given a command to execute 2 something, correct? 3 A Yes. 4 Q Is the general purpose register block a form of memory? 5 A Yes. 6 Q Could it be a collection of FIFOs? 7 A No. 8 Q Why not? 9 A A FIFO is not a general purpose register file. 10 Q Okay. Is there some limitation as to what can be stored 11 in a general purpose registry file, in terms of, say, 12 type of data? 13 A Not that I know of, no. Yeah, not that I know of. 14 Q Could I store instructions in the general purpose 15 registry block? 16 A So you can only store information in the general purpose 17 register file that will, while it's in there, be 18 processed and treated as data. 19 You can't pull an instruction out of the GPR and 20 then execute it. 21 You can, however, and I don't think this applies to 22 graphics, that I can think of, but you could write a	123 1 Q Okay. And what are those? 2 A Well, it has to maintain data, so there are instruction 3 stores as well. 4 It's got to-- there has to be a determination of how 5 much space is available in the store. 6 In a FIFO, you don't know how much space is 7 available in the store. 8 Q Okay. And-- but outside of those restrictions, it could 9 be any type of memory that could store data or 10 instructions? 11 A I would have to look at any particular-- that's too broad 12 a question for me to answer. 13 Q You didn't determine, when forming your opinion, whether 14 the term "store" in Claim 5 was restricted to any type of 15 memory? 16 A I did my best to determine if it was restricted in the 17 context of Claim 5, for example, yeah. 18 Q And did you form an opinion? 19 A Yeah, it's restricted in at least those ways that I 20 talked about. 21 The store has to store data, and it has to be able 22 to-- there has to be a-- it has to be capable of having a
122 1 program that generates a second program, so you could 2 produce instructions, for example, write them into the 3 GPR, and then store them back into memory and then bring 4 them back in, and instead of sending them to the GPR, 5 have the sequencer stick it in its instruction buffer. 6 That sort of operation is pretty uncommon but 7 certainly understood and known, like I said, not really 8 in the context of graphics. 9 Q In Claim 5 it doesn't use the words "general purpose 10 register block," it uses the word "store," correct, with 11 respect to maintaining this selected data? 12 A Yes, that's correct. 13 Q And would you understand that the term "store" is broader 14 than the general purpose registry block? 15 A Yes. 16 Q So a store could be any type of memory, correct? 17 A Off the top of my head, I can't think of a restriction of 18 a particular type of memory that couldn't be considered a 19 store of some sort or another. 20 However, there are other limitations that the claim 21 enforces that bars it from being certain types of store, 22 in my opinion.	124 1 determination made of the amount of space available. 2 Q But does that prevent it from also being able to store 3 instructions? 4 A I don't know. 5 Do you mean data that as a result of where it's 6 stored will be used as an instruction or data that at 7 some time in the future in a different context can be 8 used as an instruction? 9 Q Either one. 10 A Well, as I suggested, there are situations where a piece 11 of information is processed or manipulated as data and 12 then gets moved into a different context and is treated 13 as an instruction. 14 Q Okay. In Claim 6 there is language that says, "The 15 circuitry operative to fetch data from a memory," 16 correct? 17 A Yes. 18 Q What data is being fetched there, in your opinion? 19 A That's the data that-- presumably that's data that's 20 fetched by the sequencer, yeah. 21 Q Is there-- 22 A I think one of the things that's being-- one aspect of

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125 1 that, I believe, is— if we look back at Figure 5— well, 2 it's not really clearly shown there. 3 There are things called texture caches, and I think 4 that that's one example of what they are anticipating. 5 Q Is there anything in Claim 5 or 6 that would prevent that 6 type of data from being maintained in the store? 7 A Well, 5 only refers to storage in a store. 8 6 uses a term "memory" separately, which certainly 9 suggests that they could be separate. 10 I don't know and haven't thought about whether they 11 have to be separate or not. 12 Q Right. 13 My question was a little different. 14 What I'm asking you is: 15 Is there anything in the claim language that would 16 restrict "store" in Claim 5 from being able to store 17 either the data that is talked about in Claim 5 or the 18 fetch data that's being talked about in Claim 6? 19 A Yeah, and that's why— that's what I was trying to get 20 at. 21 I'm sorry if it wasn't clear. 22 I don't know that there's anything that precludes	127 1 the store holding the selected data. 2 Claim 6 is talking about also having a memory from 3 which data can be fetched. 4 It strikes me that would not be the selected data. 5 Now, it could be the case that, for example, both of 6 them might qualify as pixel data or geometry data, but I 7 don't think it's— when they're separate, I don't think 8 it's the selected data, but I get the sense I didn't 9 answer your question here. 10 Q I think that's fine. I don't care if it's selected data 11 or not. 12 I just want to know, can both types of data, whether 13 they're selected or not, be stored in the store or is 14 there something that restricts the memory recited in 15 Claim 5 to being a type of memory that cannot store the 16 fetched data? 17 A No, I don't think there's anything that restricts it in 18 such a way that it cannot store the fetched data. 19 MR. JOHNSON: Let's go ahead and take 20 a break. 21 (Recess 2:12 to 2:24 p.m.) 22 Q (By Mr. Johnson) Welcome back from your break.
126 1 them from being the same thing, the same memory, the same 2 store. 3 Q I think my question is still bad, so let me try one more 4 time. 5 A Okay. 6 Q I am setting aside the issue-- the legal issue that you 7 said earlier, you don't know whether or not it should be 8 separate or the same, okay? 9 I am just trying to take that out of the equation, 10 all right? 11 A Mm-hm. 12 Q All I'm asking is: 13 With respect to the term "store" in Claim 5, we were 14 talking about what types of memory could satisfy that 15 term, okay? 16 A Okay. 17 Q And my question is just: 18 Is there anything in Claim 5 or 6, apart from 19 whether or not memory has to be separate or the same, 20 that would restrict the memory in Claim 5 from being able 21 to store both types of data? 22 A Okay. So if they're separate, Claim 5 is talking about	128 1 A Thank you. 2 Q Are you ready to proceed? 3 A Yes, I am. 4 Q Earlier today you were discussing the R400. 5 Do you recall that? 6 A Yes. 7 Q And I asked you whether or not you had had conversations 8 with the various people that you cite from their 9 testimony in your declaration. 10 Do you recall that? 11 A Yes. 12 Q And so as I recall, you had not had conversations with 13 them, but you had read their transcripts or reports or 14 whatever documents that they provided. 15 Is that correct? 16 A Yeah, to the best of my recollection. 17 Q And in general, did you find anything in their testimony 18 that you disagreed with? 19 A I don't recall seeing anything that I disagreed with that 20 was material to my consideration, not that I recall. 21 Q Okay. And in particular, there was a Mr. Gruber. 22 Do you recall him?

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129 1 A I do. 2 Q And in the institution decision, there's some discussion 3 about Mr. Gruber's testimony in several places, but one 4 of those is on Page 31 of the institution decision. 5 Do you have a copy of that with you? 6 A I do not have that. 7 Q Okay. I am just going to hand you a copy of the 8 institution decision in this case. 9 It's indicated as Paper 10 on the document. 10 If you go to Page 31, the first full paragraph is 11 what we are going to be looking at. 12 It starts with, "Patent owner argues there is 13 substantial evidence of conception." 14 Do you see that? 15 A I do. 16 Q The second sentence says, "According to patent owner, 17 Mr. Gruber's testimony demonstrates that the basic design 18 was proven to work even if it had bugs and was not 19 completely functional." 20 Do you see that? 21 A I do. 22 Q Do you recall whether or not in your review of	131 1 functional? 2 A I certainly believe that when they shipped the R400 3 ultimately to the Xbox-- for production in the Xbox, one 4 would call it completely functional. 5 Microsoft sold many of those, which is not to say 6 that it didn't-- as I say, that it didn't have bugs. 7 Q Do you know when that took place? 8 That wasn't in 2001, correct? 9 A No. I don't recall when that was. 10 Q Later in this paragraph it says, "Mr. Gruber also 11 acknowledged that when the first silicon was made for the 12 Xenos chip, the dynamic register file allocation method 13 did not function properly." 14 Do you see that? 15 A I do. 16 Q Do you have any reason to disagree with that statement? 17 A No. 18 Q So I don't want you to have to answer questions in the 19 blind, so I have a copy of the transcript of Mr. Gruber 20 if you want it and want to see it. 21 A Sure, if there's something in particular-- 22 Q It's just for your benefit because I am asking you to
130 1 Mr. Gruber's testimony there was any indication that the 2 basic design of the R400 had bugs in it? 3 A I recall, as it says here, that it may have had bugs in 4 it. 5 I don't recall if he said that it did. 6 It's a very large, complex design. From my 7 experience, it had bugs in it. They just might not have 8 identified them. 9 Q So you have no reason to disagree with his statement that 10 even if it had bugs, it was not completely functional? 11 MR. DOKHANCHY: Objection; misstates 12 the document and the testimony. 13 MR. JOHNSON: Sorry, did I misread it? 14 MR. DOKHANCHY: I think so. 15 I think you said it was not functional. I think he 16 said it was functional. 17 THE WITNESS: Yeah. He said, "Even if 18 it had bugs and it was not completely functional"-- he 19 didn't say, "Even if it had bugs and it was completely 20 functional"-- 21 Q (By Mr. Johnson) Let me ask a better question. 22 Do you know whether or not the R400 was completely	132 1 agree or disagree with statements in the decision, but I 2 want you to have the opportunity to look at it. 3 I will hand you a copy of that, and it is marked as 4 Exhibit No. 1017 in this case. 5 A Okay. 6 Q If you look at, for example, Page 104, Line 20 to 25, you 7 should be able to confirm Mr. Gruber's testimony. 8 A Which lines? I'm sorry. 9 Q 20 to 25. 10 A Yes, I see his discussion there. 11 Q And so do you have any reason to disagree with his 12 testimony? 13 A No. 14 I don't know exactly what it was and how it failed. 15 I assume he's talking about the allocation step 16 where the arbiter allocates some registers, but there are 17 also other-- I'm not sure that's what he was referring 18 to. 19 Q I think the general point of the discussion here is that 20 it was not completely functional, and I'm just asking you 21 whether or not you believe, in 2001, it was completely 22 functional.

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133 1 A My understanding is that there were bugs in the chip as a 2 whole, and-- let me go back to 104. 3 The first silicon for the Xenos chip, the dynamic 4 register file allocation method did not function 5 properly, and he agreed with that, yeah. 6 Q And do you know the timeframe for when they sent the 7 silicon for the Xenos chip? 8 A No, I don't. It might be mentioned probably somewhere in 9 my declaration, but I don't recall. 10 Q Did you undertake any evaluation, independent of 11 Mr. Gruber's testimony, as to what the bugs were in the 12 R400 in the 2001 timeframe? 13 A No, other than there were bugs-- I didn't undertake any 14 effort to find bugs. 15 There were references to bugs in many of the 16 documents that I did review from that time period. 17 Q So even when they sent their first silicon for the Xenos 18 chip, it still was not operable, correct? 19 A I wouldn't say that. 20 I don't know. 21 There was a set of-- as I recall, there were 22 triangle tests, they called them, a set of very small	135 1 Q Okay. 2 A But that's just a small part of the whole system, which 3 is what I was suggesting. 4 Q Sorry, I didn't mark this properly, so I'm having to find 5 it. 6 So looking back to the institution decision, Page 7 40, which is Paper 10 in this case, down at the bottom of 8 Page 40 it says, "As Petitioner points out, Lindholm 685 9 discloses determining thread execution priority based on 10 the amount of sample data in the pixel and vertex input 11 buffers and recognizes that the maximum number of threads 12 that can be executed simultaneously depends on the size 13 of storage for thread state data." 14 Do you see that? 15 A I am sorry, I missed it. 16 You started at the very bottom of 40? 17 Q Very last sentence on 40 that spills over into the top of 18 41. 19 A Gotcha now. 20 Q Go ahead and read it at your convenience. 21 A Okay. 22 Q Do you agree with that statement?
134 1 tests from early on. 2 I would be shocked if those-- I would be quite 3 surprised if those didn't work. 4 Does that make it operable? To the engineers? 5 Maybe. Maybe that was too limited. 6 Maybe it could execute, you know, five of the most 7 popular Xbox games, but the sixth and seventh one failed. 8 Is that operable? Well, it's operable in many situations 9 or "functional" I think maybe was-- maybe was what you 10 said. 11 My Tesla, soon after I got it, had a sensor fail, so 12 when I walk up to it, the charging port doesn't open up. 13 You can push a button on the charger, and it opens 14 up. 15 I mean, that's a bug, but as far as I'm concerned, 16 the car is functional and operates for everything I want 17 it to do. 18 Q But the charging port itself wouldn't be operable, right? 19 A It charges my car. 20 The sensor to determine whether I've walked up 21 holding the charger and thus it should open the charging 22 port, yeah, that part was buggy, that was not operable.	136 1 A I don't recall. 2 I don't disagree with it as I sit here. 3 Q Okay. Did you review Lindholm 685 in preparing for this 4 deposition? 5 A Not really, no. 6 Q Okay. Do you recall Lindholm's disclosure of 7 prioritization of thread execution? 8 A I do, to some extent, but I would have to review it to 9 answer any further. 10 Q Do you recall whether or not that priority was based on 11 available storage? 12 A This statement certainly seems to suggest that the 13 petitioners made that statement and that the PTAB-- it 14 suggests to me that the PTAB agreed, but I don't recall 15 in any great detail. 16 Q Okay. Do you have a copy of the Lindholm 685 reference? 17 A No. 18 Q Okay. I am going to give you a copy of that reference, 19 and it is marked as Exhibit No. 1005 to this action. 20 If you go to Column 4, Line No. 34-- 21 A Okay. 22 Q It says, "Each execution pipeline 240 signals to vertex

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137 1 input buffer 220 when a sample can be accepted or when a 2 sample cannot be accepted." 3 Then in Column 5, starting at Line No. 24, it says, 4 "Each execution pipeline 240 signals to pixel input 5 buffer 240 when a sample can be accepted or when a sample 6 cannot be accepted as described further herein." 7 Do you see that? 8 A I do. 9 Q Do you recall whether or not, when making those 10 determinations about whether or not something can be 11 accepted or not accepted, if that decision was based on 12 available storage? 13 A I think that it must have been. 14 If you don't have-- if you need storage and there is 15 no storage available-- I don't know how it would use 16 storage that was not available. 17 Q So if you could look at Figures 8A and 8B in Exhibit 18 No. 1005. 19 A That's Lindholm? 20 Q Yes. 21 A Okay. 22 Q In Figure 8A it shows that the system receives a sample	139 1 Q A control signal is just a voltage, right? 2 A Typically, yeah. 3 Q Whereas data is represented by ones and zeros, correct? 4 A Yeah, I mean, those are just voltages as well, but, yeah 5 there is-- I agree, there is a distinction there for 6 sure. 7 Q When I receive that one or a zero, I just look at the 8 voltage, and then I determine whether it's a one or a 9 zero based on the voltage, correct? 10 A Not necessarily. 11 I mean, the control signal might have multiple bits 12 associated with it, so it could be a digital address, 13 which is used to control which register inside the GPR is 14 accessed. 15 It could also be an analog signal with useful values 16 beyond zero and one, but I can't think of a situation, in 17 the context of our discussion, where that had come up. 18 Q In your declaration what was your definition for "control 19 signal"? 20 A I don't recall providing an explicit definition for 21 "control signal." 22 I did, I believe, identify "control signal."
138 1 and assigns a thread, correct? 2 A Yes. 3 Q And in Figure 8B it receives a sample 850, assigns a 4 thread 875, it checks resources in 877, and then it 5 executes the thread in 880, correct? 6 A Yes, I see that. 7 Q So would it be fair to say that the execution of the 8 instructions in those threads in Lindholm depends on 9 receiving a selected data? 10 A If after analysis of Lindholm in the context of the '454 11 patent the received sample satisfied the selected data, 12 then I would agree with that. 13 Q Okay. So I want to talk about Claim 7 in the '454 14 patent. 15 A Okay. 16 Q Claim 7 requires a control signal, correct? 17 A Yes. 18 Q If I was to send data versus sending a control signal, 19 what would be the difference? 20 A Data conveys information that can be operated upon, used 21 in a calculation. 22 Generally that is not the case for a control signal.	140 1 Q Do you recall citing to the dictionary definition of 2 "control signal"? 3 A Not that I recall, sitting here. 4 I may have. I just don't recall. 5 I should probably look at my discussion of Claim 7 6 and see if there's anything that pops up. 7 Does anybody know what page that would likely be on? 8 Q I thought I had it marked, but I don't, so-- 9 A I am getting closer. 10 Okay. I am looking at Page 85. 11 Yeah, there's a discussion around-- starting around 12 Paragraph No. 161 saying the sequencer generates control 13 signals in the form of control packages for either vertex 14 operations and instructions or pixel operations and 15 instructions, and these packets then get sent forward, 16 and the packets include information like a pointer to the 17 start of the executing thread. 18 This discussion is all in the context of the R400, 19 so there must be, I believe, parallel discussion earlier. 20 I could flip back to that if you want. 21 Q No, I was just trying to let you get done. 22 I will refer you to Page 222 of your declaration.

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141 1 A Okay. All right. I'm there. 2 Q And down in Paragraph No. 321 there's a discussion of 3 control signals and a reference to a Microsoft computer 4 dictionary. 5 Do you see that? 6 A I do. 7 Q And so is it your opinion that "control signal" in the 8 '454 patent should be given its plain and ordinary 9 meaning? 10 A Yes, and I think this is an example of the plain and 11 ordinary meaning. 12 Q Okay. And so in this example of the plain and ordinary 13 meaning, it would mean an electrical signal that is used 14 to control internal or external devices or processes, 15 correct? 16 A Yes. 17 Q And you agree with me that if I send priority 18 information, that's going to be an electrical signal? 19 A Not necessarily. 20 Q It could involve an electrical signal, couldn't it? 21 A It could, yeah. 22 Q And if I was to send that priority information, it's	143 1 Q As a person of ordinary skill in the art, would you 2 understand that Lindholm's multi-threaded processor could 3 switch between instruction? 4 A I wouldn't necessarily call that a multi-threaded 5 processor. 6 It's a processor for multi-threaded execution. 7 One example of multi-threaded, of what is often 8 referred to as multi-threaded, is what I suggested 9 previously, where the operating system keeps track of 10 multiple threads and activates one or another, but only 11 one thread is active on the processor at any point in 12 time, so the whole system can be multi-threaded without 13 the processor itself being something that I would call 14 multi-threaded. 15 Q Is that what your opinion is of Lindholm? 16 A I don't recall. 17 Q So if you look at Figure 7A in Lindholm in Exhibit 18 No. 1005, in Box 720 it says, "Execute first program 19 instructions," and then it says, "Execute second program 20 instructions"? 21 A Yes. 22 Q Do you see that?
142 1 certainly going to control some sort of process by 2 placing a priority, something above something else, 3 correct? 4 A It may. 5 I would assume that that information is sent, and it 6 is eventually used someplace, but that's not always the 7 case. 8 Q Okay. Do you recall whether or not Lindholm discloses a 9 multi-threaded processor? 10 A I don't recall. 11 NVIDIA was certainly one of the companies that early 12 on invested or tried to make use in GPUs of such 13 technology, but I don't recall if that was in Lindholm or 14 not. 15 Q Okay. You have the Lindholm reference, correct? 16 A Yes. 17 Q Do you mind just scanning over it and just seeing if it 18 refreshes your recollection as to whether or not it 19 discloses a multi-threaded processor? 20 A The abstract says, "A programable graphics processor for 21 multi-threaded execution of program instructions, 22 including a thread control unit."	144 1 Do you agree that Lindholm shows sequential and 2 simultaneous processing capabilities? 3 A The Figure 7A shows sequential. It's not clear that it's 4 showing simultaneous. 5 Q So in sequential though, is it executing the first set of 6 instructions and then switching to execute a second set 7 of instructions? 8 A Yes, that's what 7A appears to be indicating. 9 Q Okay. If you look at Column 13, starting on Line 11, it 10 says, "In Step 775 a third number of threads determined 11 for allocation to a first sample type are allocated to 12 the first sample type. The third number may be allocated 13 prior to rendering an object within a scene, a portion of 14 a scene, a new scene, or the like. Alternatively, the 15 third number of threads may be allocated to a third 16 sample type." 17 Do you see that? 18 A I do. 19 Q Do you understand what "sample type" means here? 20 A I believe that's referring to a vertex or a pixel that 21 needs to be rendered. 22 Q And as a person of ordinary skill in the art reading

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145 1 this, would you have understood it to include the 2 possibility of simultaneous execution of threads for 3 different sample types? 4 A I don't think it precludes that. I just don't recall 5 whether it discloses that. 6 Q Would you agree that rendering a portion of a scene 7 describes operations at different degrees of completion? 8 A No, not on its own. 9 Q Why not? 10 A It's not clear that any particular instruction-- well, 11 that would be-- rendering a portion of a screen-- 12 Q "Portion of a scene." 13 A "Portion of a scene," thank you. 14 That's rendering a portion, one. 15 It could be done with-- it could involve overlapped 16 execution of operations in multiple stages of completion. 17 It may not. 18 The easiest form, as an engineer, is to start 19 something and finish it before moving on, so the easiest 20 implementation would be for it not to have operations in 21 multiple stages of completion. 22 Q But it is one of the possibilities implicated, correct?	147 1 be the first person to get tickets. The last person in 2 line will be the last person to get tickets. 3 Q And do you agree that this-- strike that. 4 Do you agree that Amanatides checks the storage 5 space in the output FIFO? 6 A I think implicitly, but I don't know that it checks the 7 storage space in the context-- any context that we've 8 discussed before. 9 Any hardware FIFO that I've seen has to have a way 10 to indicate that it is full and so that some other entity 11 won't try to load new data into it when there is no space 12 available. 13 Q Okay. Do you know what the reference to "GM" and "RM" 14 packets are in Exhibit No. 1007? 15 A Yes. 16 Q And what are they? 17 A So "GM" is a reference to geometry packages. 18 I think "M" is "message," but I'm not sure. 19 "RM" is a reference to, I think, rasterization. 20 It is, in essence, talking about pixels. It is 21 geometry and pixel messages. 22 Q So just to refresh your memory, if you look on Page 159,
146 1 A It doesn't seem to talk about it at all, so I would say I 2 don't see how this passage precludes that, but it also 3 doesn't enable it. 4 Q Do you have a copy of the Amanatides-- 5 A I do. 6 Q Okay. So this kind of prior art is difficult to pinpoint 7 you to a place because there's no line numbers, it's just 8 page numbers. 9 A Yeah. 10 Q So I'm looking at Page 158 of the article, which is Page 11 8 of 11 of the exhibit. 12 The exhibit number is 1007. 13 A All right. I am oriented. 14 Q Okay. And this article talks about FIFOs on this page, 15 correct? 16 A Yes. 17 Q And we've talked a little bit about FIFOs today, but can 18 you just remind me, what kind of a storage device is a 19 FIFO? 20 A A "FIFO" stands for "first-in, first-out," and it's just 21 like keeping, in a computer system, data elements in 22 line, like the first person to line up for tickets will	148 1 in the right-hand column, the third paragraph, it refers 2 to "geometry messages" and "rendering messages." 3 Do you see that? 4 A Yes. 5 Q And so does that refresh your memory as to what "GM" and 6 "RM" are? 7 A Where "GM" and "RM" come from, yeah. 8 It doesn't change my opinion about that they do, but 9 yes, it does help refine it. 10 Q Sure. 11 Do you agree that Amanatides assigns priorities to 12 GM and RM packets? 13 A Amanatides, as I recall, works with an arbitration scheme 14 or a prioritization scheme where they say-- the system 15 starts with no messages in the system, and graphics 16 begins with geometry instructions, and so it sends 17 geometry messages across and interconnect to the various 18 processors. 19 Those processors execute the GMs, and I think it's 20 anticipated, if not in most cases, as a result, begins to 21 generate RMs, which go to their output queues. 22 Once the system starts to generate RMs, it is my

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149 1 understanding that the host, which is the-- or the main 2 controller, which is the source of GMs, will stop 3 generating GMs, I believe, until there are no more RMs to 4 be processed, in which case it will switch back. 5 It's sort of modal. 6 Q You see on Page 159 of Exhibit No. 1007, which is Page 9 7 of 11 of the exhibit, there is a sentence in the second 8 paragraph that says, "The host busy waits until its 9 output FIFO has space and then starts sending packets 10 containing polygons." 11 Do you see that? 12 A Yes, I do. 13 Q And so as a person of ordinary skill in the art, would 14 you understand that in order for the host to know whether 15 or not there's space, there must be some sort of either 16 monitoring of the space or signal to indicate that 17 there's space available? 18 A Well, as I said, a FIFO hardware structure has got to 19 have an indication if it's full, so that would match my 20 understanding. 21 The host may not know how much space is available, 22 but it will know if there is any space available.	151 1 There's no disclosure of two packets being-- if we 2 look at the figure-- well, I guess maybe that works since 3 there's two buses. 4 One can think of it that they're saying, "If we 5 model it as high priority and low priority," so sure. 6 Q I'm sorry, are you done? 7 A Yes, I am. 8 Q So I guess I'm just not entirely clear of your response. 9 The sentence I read to you at the bottom of 9 says, 10 "Packets on the bus have two priorities: low and high," 11 correct? 12 A It does say that, yes. 13 Q So I took your earlier response to mean that they are not 14 using priorities, but how do you reconcile that with this 15 sentence? 16 A I was focusing on the second half where it says, "If we 17 map," and looking at GM and RM packets. 18 They are saying packets have two priorities, low and 19 high, and the low-priority packets get blocked from the 20 bus if high-priority packets are waiting. 21 Q Okay. So the packets are either assigned a high or a low 22 priority, correct?
150 1 Q And then down at the bottom of 159, Page 159 of the 2 article, Page 9 of 11 of the exhibit, 1007, the final 3 paragraph says, "As we mentioned earlier, packets on the 4 bus have two priorities: low and high. The low-priority 5 packets cannot get onto the bus if high-priority packets 6 are waiting. If we map GMs to low-priority packets and 7 RMs to high-priority packets, then the solution is in 8 site." 9 Do you see that? 10 A I do. 11 Q So does that refresh from your recollection as to whether 12 or not GM or RM packets are assigned priorities? 13 A They are saying if they do that in the context of doing 14 deadlock avoidance. 15 There's actually no hardware that's disclosed that 16 does that, but there is a discussion of how to manage the 17 generation of GM packets and RM packets-- well, yeah, I 18 guess implicitly RM packets. 19 Q Do you agree with me that the packets are assigned 20 priorities of either low or high at some point in the 21 process? 22 A No, I don't.	152 1 A Sure. 2 Q Okay. So we talked a little bit about shared resources 3 earlier. 4 Do you recall that? 5 A Yes. 6 Q And I recall that your testimony was that at least the 7 general purpose register block in Figure 5 of the '454 8 patent was a shared resource. 9 Is that-- 10 A Yes. 11 Q And I can't recall whether or not you indicated that the 12 source registers that sat in-between the general purpose 13 register block and the processing unit were also possible 14 shared resources. 15 A We got close to that discussion. I don't think we hit 16 upon it. 17 They are shared in that sense that only one thread 18 or only one operation, as shown in the '454 patent, can 19 make use of them at one point in time, but that doesn't 20 mean that they're shared in the sense that their usage 21 needs to be coordinated. 22 They're designed such that they're basically known

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153 1 to be available when an instruction is ready to execute. 2 Q And what about the buses that connect between the general 3 purpose register block and the processing unit, is that a 4 shared resource? 5 A I wouldn't say so, at least as disclosed in the '454 6 patent because, again, the connection from the GPR to the 7 processing unit is only going to be carrying data related 8 to one thread at any point in time. 9 If it reads out source A and then source B and then 10 source C, all three of those are used for one thread. 11 Over time they're used by different threads, but 12 there can't really be contention for them at any 13 particular point in time. 14 Q So what is your definition of a "shared resource"? 15 A I don't think I have offered one. 16 I have discussed "shared resource" in the context of 17 the claims, and we can go back and look at that-- 18 Q But you seem to be making some sort of distinction that 19 the resource has to be in contention for two different 20 things in order to be shared. 21 A That's typically the case. 22 I would agree that there's probably situations	155 1 because we never contend for it. I have it on Mondays 2 and you have it on Tuesdays. 3 Q So your opinion for shared resource means that there must 4 be some tension on the resource to be shared at the same 5 time? 6 A Yeah, at least in the context of the '454 patent, that's 7 certainly how I understand it. 8 For example, the GPRs have limited amount of space, 9 and the sequencer and arbiter considers which threads are 10 available to be started, how much space is available, how 11 much space each one requires. 12 In essence, it's arbitrating between two different 13 choices and deciding which one-- or more than two, which 14 one to activate. 15 Q But isn't a bus sometimes-- well, maybe-- I'm going to 16 say it unartfully, and then we'll try to clean it up. 17 A Yeah. 18 Q Isn't there times when two different things are trying to 19 put stuff on a bus? 20 A Yeah, so, for example, we do see that in Amanatides where 21 he mentions the two different things having priority, 22 which is presumably so that you can decide, when faced
154 1 where-- I can think of, where it can be shared by two 2 different parties or entities without necessarily being 3 in contention. 4 For example, the-- I don't know, the processors are 5 shared among all threads. Only one thread can have an 6 operation executing on it at one time, but that's a bad 7 example. I am going to-- I don't know if I can ask you 8 to strike that, but that was a bad example I was coming 9 up with off the top of my head. 10 My point was that I think when a POSITA thinks of a 11 sharing resource, it usually involves managing 12 contention, "How do you share that resource?" 13 That being said, there are trivial ways to manage 14 that contention, such that they're not-- like if no two 15 parties are asking for it at the same time, are they 16 really sharing it or not? 17 Q Okay. 18 A If we have one cell phone between the two of us, and I 19 have it on Mondays and you have it on Tuesdays, we're 20 sharing it, there's no real arbitration or contention, we 21 can't share it at the same time, is it a shared resource? 22 It kind of is, but I would say it also kind of isn't	155 1 with two at the same time, in contention, which one is 2 allowed to move forward. 3 I am contrasting that, for example, with the bus 4 coming out of the register file. 5 Now-- it's going to the processor. 6 It's true that every thread that wants to operate on 7 selected data has to use that bus, and so in that sense 8 it's a shared resource, but the scheduler and the arbiter 9 don't need to keep track of "Well, is it in use now," 10 because when it picks an instruction to go, it knows-- 11 like that bus is not in use, that bus just gets used at 12 the beginning of executing an instruction, so by the time 13 it comes around to pick the next instruction, that bus 14 will be available. 15 Similarly, it doesn't need to keep track of if the 16 registers for source A and source B and source C are 17 available. It just will be the case that they will be 18 available when it selects the next instruction. 19 My point being, is that a shared resource? Yes, 20 from one perspective. It's shared in a very different 21 way because it doesn't need to be managed. 22 Q And in your opinion for the claims of the '454 patent, in

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157 1 order to be a shared resource, it has to be something 2 that must be managed? 3 A I think that's probably the case for most of the claims 4 if not all of the claims. 5 Certainly the ones that say a flavor of doing this 6 "If there is space available for that type of operation," 7 that is an example of managing the resource to me. 8 Q But isn't-- even in the example where you and I are 9 sharing a cell phone on different days, hasn't that been 10 managed, I've decided I'll have it on Mondays and you've 11 decided you'll have it on Tuesdays? 12 A I don't know, maybe that's not the best example. 13 Q Figure 5 of the '454 patent, isn't the bus that comes out 14 of the general purpose register block and heads toward 15 the CPU sharing inputs from the sequencer and the 16 register sources? 17 I mean, it's connected to several different things. 18 It is not just a direct line from the general purpose 19 register to the processing. 20 A Sure, that's right, it's a direct line to the source 21 input, so it's out-- it's not reading from the source 22 inputs, but its output is going to the source registers,	159 1 file 92 doesn't need to check and see if its output bus 2 is available. It will be available because any previous 3 instruction that had made use of it has finished, or at 4 least it has moved past the stage where it needs to read 5 registers. 6 Similarly, the source registers can be updated 7 because any earlier instruction that would have made use 8 of them has gotten past the stage where it makes use of 9 them. 10 MR. JOHNSON: Let's take a break. 11 (Recess 3:28 to 3:35 p.m.) 12 Q (By Mr. Johnson) I think you said you had a copy of 13 Selzer there? 14 A Yes. 15 All right. 16 Q So I just want to ask a question or two about the Selzer 17 reference, which is Exhibit No. 1009 in this case. 18 Specifically I want to ask about something that's on 19 Article Page 47, which is Page 20 of 26 of the PDF. 20 A Okay. I'm oriented. 21 Q There's a sentence or two there that says, "After 22 rendering an object, any processor may run into an idle
158 1 I think. 2 Q But also the sequencer is using that same bus, right? 3 A Not directly, but indirectly sure, yeah-- 4 Q Well, there's a Line 94 that makes a direct connection to 5 the bus that's in-between 92 and, say, 95. 6 A Yeah. 7 Is that saying that 63 sends-- well, 92, the 8 register file, sends its results and stores them in the 9 constant memory, 91? Or is it saying that the constant 10 memory gets-- has a value read and that gets sent and 11 tied into the same physical output lines of the GPR that 12 the GPR is not then using? I don't know. It would help 13 if they put an arrow on it. 14 Q Yeah, you are the expert. I'm asking you. I don't know. 15 I'm just asking, is it possible that the buses are 16 shared resources? 17 A They are shared resources over time. They're not 18 explicitly managed because the sequencer will pick one 19 instruction and say, "Send off a"-- I think they called 20 it a packet, to have that instruction or that operation 21 executed. 22 Now as a result of that, the output-- the register	160 1 state if there is no rendering data in its input buffer. 2 Performing a task switch, it will request new unprocessed 3 geometry objects and continue geometry calculations." 4 Do you see that? 5 A Yes. 6 Q Isn't it true that Selzer's processors switch from 7 rendering to geometry calculations based on the 8 availability of data in input buffers? 9 A Not exactly. 10 It says it will request new unprocessed geometry 11 objects and continue geometry calculations, so it's not 12 beginning-- it's not just moving on and doing a 13 calculation. It's requesting it. 14 Q But it makes that switch based on the availability of 15 data in input buffers, correct? 16 A Well, it makes that switch not when there is space 17 available in the input buffer for a new input but when 18 there is no rendering data in the input buffer. 19 When that input buffer for rendering data is empty, 20 then it makes that switch. 21 Q Is this discussion in Selzer what you would call context 22 switch for a multi-threaded processor?

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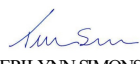
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161 1 A Yeah, most likely, a task switch and a context switch or 2 a thread switch. Depending on the terminology used by a 3 particular engineer, it might be something different, but 4 in general they're referring to the same sort of 5 operation. 6 Q Why would you want to perform this sort of context 7 switch? 8 A They discuss— they claim that this achieves automatic 9 load balancing, although I don't see that, but that's why 10 they say— seems to be why Selzer says he wants to do it. 11 Q And is one reason to do a context switch because of 12 stalls? 13 A Oftentimes, but not in this situation. 14 Q Okay. Let's also take a look at Fiske, which-- 15 A Okay. 16 Q Do you recall whether or not Fiske discloses context 17 switching as well? 18 A Yes, and in response to your last question, I think I 19 agreed that context switching on a stall is not uncommon. 20 It is actually pretty uncommon. It requires specialized 21 hardware, but not surprisingly Fiske is an example of a 22 design with that sort of specialized hardware. That's	163 1 Q Okay. 2 A The storage has already been assigned to the thread. 3 It's just that the information from memory that the 4 thread wants loaded into the storage space is not yet 5 available. 6 Q And would you agree with me that if a thread is stalled, 7 then it is unfinished? 8 A Yes. Typically, certainly in this context, there might 9 be some other definition of "stalled" that includes it 10 being done, but that would be uncommon. 11 MR. JOHNSON: All right. I will pass 12 the witness for now, subject to any redirect. 13 MR. DOKHANCHY: No questions from me. 14 MR. JOHNSON: All right. We're done. 15 (Deposition concluded at 3:46 p.m.) 16 (Signature reserved.) 17 18 19 20 21 22
162 1 why it was on my mind. 2 Q Just to clear that up, you agree then that Fiske 3 discloses context switching in the face of a stall? 4 A Yes, that's correct. 5 Q And do you agree that Fiske discloses context switching 6 of threads based on storage capacity? 7 A I don't think so, but I would be happy to review 8 something if you want me to consider it. 9 Q Well, let's see, let's look at Page 211 of the article, 10 which is Page 2 of 12 of the PDF of the Exhibit No. 1010. 11 A Okay. 12 Q Okay. And so it's in the right-hand column, and the 13 third paragraph down that starts with the word "second"-- 14 A Okay. 15 Q And then about the third sentence it says, "If a thread 16 is waiting for a memory reference to be satisfied, then 17 it is stalled and is not considered for scheduling until 18 the memory reference is satisfied." 19 A Yes. 20 Q And so does that indicate to you that it's possible that 21 the context switching is based on storage capacity? 22 A No.	164 1 CERTIFICATE 2 STATE OF WASHINGTON) 3) ss. 4 COUNTY OF KING) 5 I, the undersigned Washington Certified Court 6 Reporter, pursuant to RCW 5.28.010, authorized to 7 administer oaths and affirmations in and for the State of 8 Washington, do hereby certify: That the foregoing 9 deposition of the witness named herein was taken 10 stenographically before me and reduced to a typed format 11 under my direction; 12 That, according to CR 30(e), the witness was 13 given the opportunity to examine, read, and sign the 14 deposition after same was transcribed, unless indicated in 15 the record that the review was waived; 16 That I am not a relative or employee of any 17 attorney or counsel of participant and that I am not 18 financially or otherwise interested in the action or the 19 outcome herein; 20 That the deposition as transcribed is a full, 21 true and correct transcript of the testimony, including 22 questions and answers and all objections, motions, and 23 examinations, and said transcript was prepared pursuant to 24 the Washington Administrative Code 308-14-135 preparation 25 guidelines. 26  27 TERILYNN SIMONS, CCR, RPR, RMR, CRR 28 State of Washington CCR #2047 29 My CCR certification expires on 7/7/24 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

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