

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; TCL
CHINA STAR OPTOELECTRONICS TECHNOLOGY CO., LTD.; TIANMA
MICROELECTRONICS CO. LTD.; AND VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

U.S. Patent No. 7,414,599

Inter Partes Review No. IPR2023-00941

DECLARATION OF DR. DANIEL FOTY

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I. INTRODUCTION

1. I have been retained by counsel for Mianyang BOE Optoelectronics Technology Group Co., Ltd. (“BOE” or “Petitioner”) in the above-captioned matter as an independent consultant to offer opinions regarding the patentability of the claims in U.S. Patent No. 7,414,599 (“the ‘599 patent” or “the challenged patent”).

2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration – supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary Declarations to the extent necessary to address any such newly-introduced items.

3. If requested, I am prepared to explain (in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”)) the technology disclosed in the challenged patent – including the state of the art in the relevant timeframe. Similarly, I am prepared to explain the technology disclosed in the Kimura reference (EX1002, U.S. Pat. Pub. 2003/0132931 (“Kimura”)), and in any other prior art references cited herein. This may include, among other things, background information on driver circuits and OLED displays.

II. QUALIFICATIONS

4. My qualifications to testify as an expert in electronics technology are set forth in my *curriculum vitae* attached as Appendix A – which includes a listing of cases in which I have provided expert testimony. I have more than thirty years of experience as an engineer, scientist, and consultant in the electronics industry, including in the areas of integrated circuit (IC) design, layout, structure, and operation, in the design and analysis of transistor-based digital and analog circuits, in RF technology for wireless communications, in technology development, and in technical and business development.

5. My curriculum vitae contains further details regarding my experience, education, publications, and other qualifications which allow me to render expert opinions in connection with this proceeding.

III. COMPENSATION

6. I am being compensated for my work in this matter at an hourly rate of \$425 for consulting services. My compensation does not depend on the content of my opinions or the outcome of this investigation.

IV. MATERIALS CONSIDERED

7. In preparing this declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my declaration:

Exhibit	Description
EX1001	U.S. Pat. 7,414,599 (Chung)
EX1002	U.S. Pat. Pub. 2003/0132931 (Kimura)
EX1004	U.S. Pat. 6,362,798 (Kimura '798)
EX1005	File History for U.S. Pat. 7,414,599
EX1006	U.S. Pat. Pub. 2001/0022565
EX1007	U.S. Pat. Pub. 2003/0030603
EX1008	Excerpts from <i>Analog Integrated Circuit Design</i> , David A. Johns et al., John Wiley & Sons, Inc., 1997.
EX1009	<i>Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits</i> , Harold Shichman et al., IEEE Journal of Solid-State Circuits, Vol. SC-3, No. 3, September 1968.
EX1010	Excerpts from <i>Physics and Technology of Semiconductor Devices</i> , A. Grove, John Wiley & Sons, 1967.
EX1011	Excerpts from <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (third edition), S. Kang et al., McGraw-Hill, 2003.
EX1012	U.S. Pat. 6,229,506
EX1013	U.S. Pat. 5,666,046
EX1014	TFT AMOLED Pixel Circuits and Driving Methods, J. Stanford, SID 03 Digest, pp. 10-13 (2003))
EX1015	A New Pixel Circuit for Active Matrix Organic Light Emitting Diodes, J. Goh, IEEE Electron Device Letters vol. 23, pp. 544-546 (2002)
EX1016	A Novel Pixel Circuit for Active-Matrix Organic Light-Emitting Diodes, J. Goh et al., SID 03 Digest, pp. 494-497 (2003)
EX1017	Current-Writing Active-Matrix Circuit for Organic Light-Emitting Diode Display Using a-Si:H Thin-Film-Transistors, R. Hattori et

Exhibit	Description
	al., IEICE Transactions on Electronics vol. E83-C, pp. 779 – 782 (2000).

8. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

9. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and circuit design principles in forming my opinions.

V. UNDERSTANDING OF THE LAW

A. Legal Standards

10. I am not an attorney, but I have been informed of several legal principles, which I have employed in forming my opinions in this declaration. I have been informed that each patent claim is considered separately for purposes of patentability and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

1. Claim Construction

11. I have been informed that the claims of the challenged patents in this proceeding are to be construed using the same claim construction standard applied

in district court. I have been informed the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art as of the effective filing date of the patent. I have also been informed that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic evidence.” I have been further informed that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises, as well as the testimony of technically-skilled witnesses such as myself.

2. Burden of Proof

12. I have been informed that the petitioner in an *inter partes* review bears the burden of establishing unpatentability by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

3. Anticipation

13. I have been informed that a patent claim is unpatentable if it is “anticipated” by prior art. I have been informed that a reference anticipates a claim if the reference discloses each limitation of the claim at issue, either expressly or

inherently. I have been informed that a prior art reference may anticipate a claim without disclosing a feature of the claimed invention if that missing characteristic is necessarily present, or inherent, in the single anticipating reference as would have been understood by one of ordinary skill in the art.

14. I have been informed that material not explicitly contained in a single prior art document may still be considered for purposes of anticipation if that material is incorporated by reference into the document.

4. Obviousness

15. I have been informed that a patent claim is unpatentable if it would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the claimed invention. I have been further informed that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” or objective indicia of non-obviousness.

16. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have

been known or obvious to a POSITA at the time of the invention. That is, if the POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.

17. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

18. I have been informed that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references, or multiple teachings of the same prior art reference.

19. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be

considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

20. Copying: evidence that others, including the accused infringer, copied the patented invention.

21. Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.

22. Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.

23. Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.

24. Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.

25. Praise: evidence of praise directed to an invention by others in the field.

26. Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

27. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed that the patentee bears the burden of showing a “nexus” between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

B. Priority Date

28. I have been informed that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled – and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis, and that claims in the same patent may have different priority dates. I have been instructed to use July 7, 2003 as the priority date for all of the challenged claims in the challenged patent.

C. Level of Skill in the Art

29. I have been informed that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

30. I have been informed that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) rapidity with which innovations are made; (4) sophistication of the technology; and (5) education level of active workers in the relevant field. I have been further informed that a POSITA is also a person of ordinary creativity.

31. The challenged patent pertains generally to the field of OLED displays, and more particularly to the circuitry used to drive and control the pixels that comprise the light-generating elements of the display – though, as will be discussed below (in Section XII.1), circuitry of this type could be used in other applications to provide the same cited benefits. A person of ordinary skill in the art (“POSITA”) in the technology field of the ’599 patent at the time of the alleged invention would have had a Bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of circuit design/analysis experience. A Master’s or Ph.D. degree in a relevant field may substitute for some work experience and vice versa. I was at

the time of the alleged invention at least a POSITA in the art relevant to the challenged patent. Further, based on my experience, I understand and know of the capabilities of a POSITA in 2003 – and I am familiar with how a POSITA would have understood and used the terminology found in the challenged patent at the time of its filing, and with the state of the art at that time.

VI. SUMMARY OF OPINIONS

32. I have been asked to compare the Kimura reference to Claims 1-18 of the '599 patent (the “Challenged Claims”). In my opinion, the Challenged Claims are all unpatentable as obvious based on Kimura combined with the knowledge of a POSITA.

33. My substantive analysis in §XII provides examples of why Kimura renders the Challenged Claims unpatentable. I reserve the right to cite and rely on additional portions of Kimura in any future declarations or depositions.

VII. TECHNOLOGY BACKGROUND

34. Before considering the '599 patent in detail, some background on the technology of the '599 patent should be considered. This involves both the basic notions of transistor-based circuits, and of light-emitting elements (and their use in display screens).

A. Fundamental Concepts of Transistor-Based Circuit Design

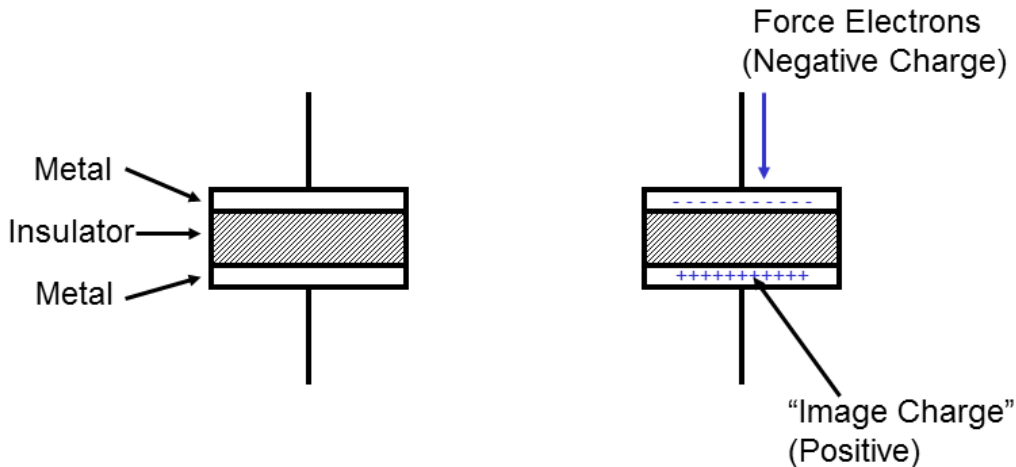
35. Ever since the invention of the first transistor in 1947, transistors have been used as fundamental building-blocks for the design of electronic circuits. Although a variety of transistor types have appeared over the years, by 2003 the transistor space was overwhelmingly dominated by a type of transistor that is known as the “field-effect transistor” (for reasons that will be described below). The circuitry disclosed in the ‘599 is based on the use of field-effect transistors as the fundamental building-blocks – with that particular type being known as a “thin-film transistor” (TFT); the TFT can be readily-understood, due to its strong similarity to the better-known (and extremely-ubiquitous) silicon-based metal-oxide-semiconductor field-effect transistor (MOSFET).¹

36. Thus, before considering the ‘599 patent (and similar prior art), it is helpful to provide a brief overview of the basics of field-effect transistors and their usage in circuitry.

1. Field-Effect Transistors (FETs)

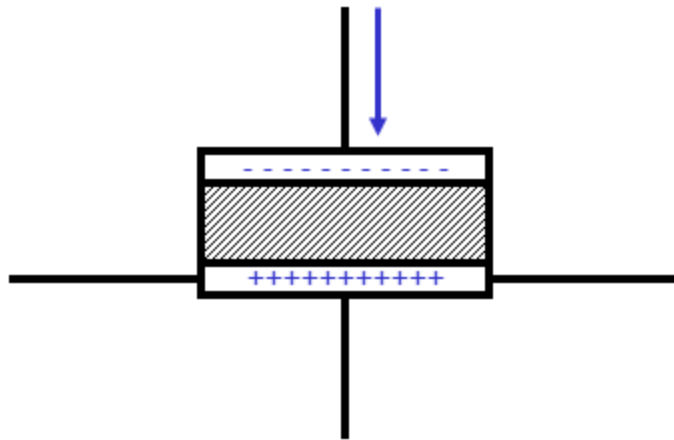
37. The field-effect transistor (FET) is actually based on a charge control mechanism that has long been known in the art – which is, the simple charge control inherent in a basic capacitor.

¹ It is the silicon MOSFET that has been the specific transistor type that has made “Moore’s Law” possible.



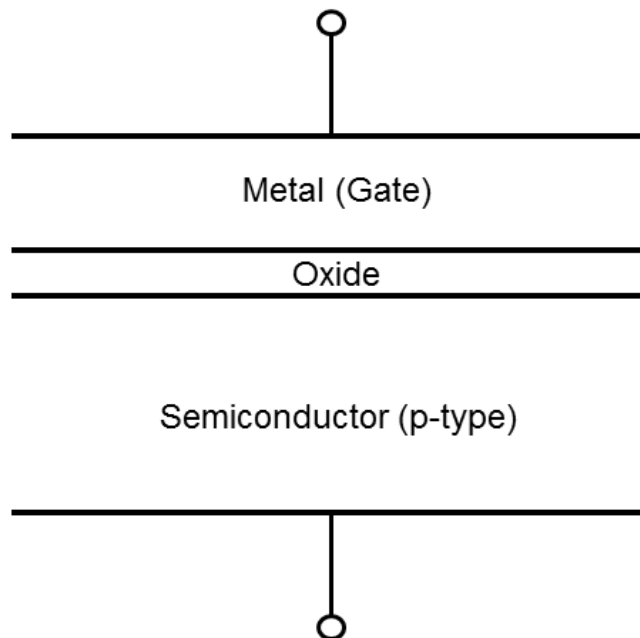
When a negative charge (electrons) is forced onto one plate of the capacitor, basic electromagnetic theory requires that a corresponding “image charge” (of an equal-but-opposite charge) appear on the other plate of the capacitor. In the same way, if a positive charge is forced onto one plate of the capacitor, an equal-but-opposite negative charge appears on the other plate of the capacitor. A capacitor will store charge and maintain a voltage until discharged.

38. A field-effect transistor is based on using this ability (to create or remove a charge layer on the other plate of a capacitor as a charge-control mechanism – combined with the addition of lateral contacts that allow current to flow when the image charge is present and to *not* flow when the image charge is absent.



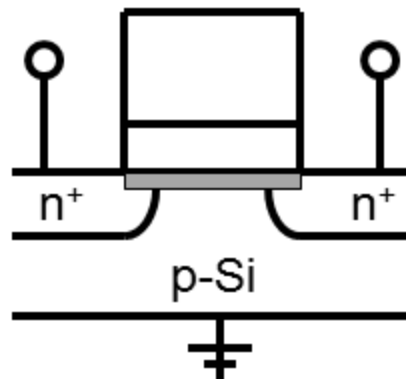
This, of course, indicates the possibility of using this type of structure as an on/off switch (with no moving parts).

39. In 1955, it was discovered (accidentally) that an insulating silicon dioxide layer can easily be grown on top of a silicon semiconductor substrate; by depositing a metal layer (such as aluminum) on top of the oxide, a simple capacitor is formed.



40. The silicon semiconductor layer is described as “p-type” – as it has (intentionally) been infused with a concentration of atoms of a species (usually boron) that contributes free positive (hence “p-type”) charge to the silicon; these introduced impurity atoms are called “dopants,” and the process of infusing them into silicon (or another semiconductor material) is known as “doping.” When a positive charge is applied to the metal contact layer (i.e., the upper plate of the capacitor), a negative image charge forms at the surface of the silicon (as in a simple capacitor) – and is trapped there by the silicon dioxide insulator layer.

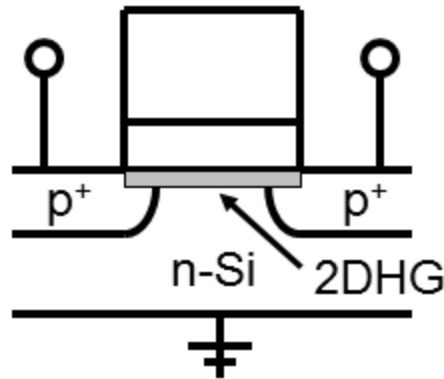
41. It was also long-known in the art that if other particular types of atoms (such as phosphorous and arsenic) are used as dopants, these atoms will cause negative-polarity free-charge to appear in the silicon – and it will be known as “n-type.” If a very large amount of phosphorus or arsenic is infused into silicon that is already p-type, the n-type atoms will simply overwhelm (by sheer numbers) the p-type atoms – and the silicon so-infused will become selectively n-type. By infusing a small pocket of n-type atoms (in such a high concentration that the silicon becomes so strongly n-type that is often called “n⁺”), it is possible to create the sought-after two lateral contacts.



This structure provides the capacitor-with-lateral-contacts discussed earlier – so that the gate voltage controls the presence (shown in the figure) or absence of charge in the capacitor structure; meanwhile, the n^+ pockets provide the lateral contacts – so that current can flow (or not flow) based upon the presence of (or absence of) the induced charge layer; when the charge layer is present, applying a voltage difference between the lateral contacts will cause current to flow in the device. This type of transistor is known as an “nMOS transistor.”

42. Also, while the MOS transistor clearly can be used as a simple on/off switch, it should be noted (for future reference herein) that the MOS transistor is a voltage-controlled current source – as the voltage on the gate controls whether-or-not (and to what degree) current flows between the lateral terminals.

43. Returning to the basic MOSFET structure, it is possible to reverse the polarities of the dopant atoms – so that the silicon substrate is n-type and the contact pockets are p^+ .

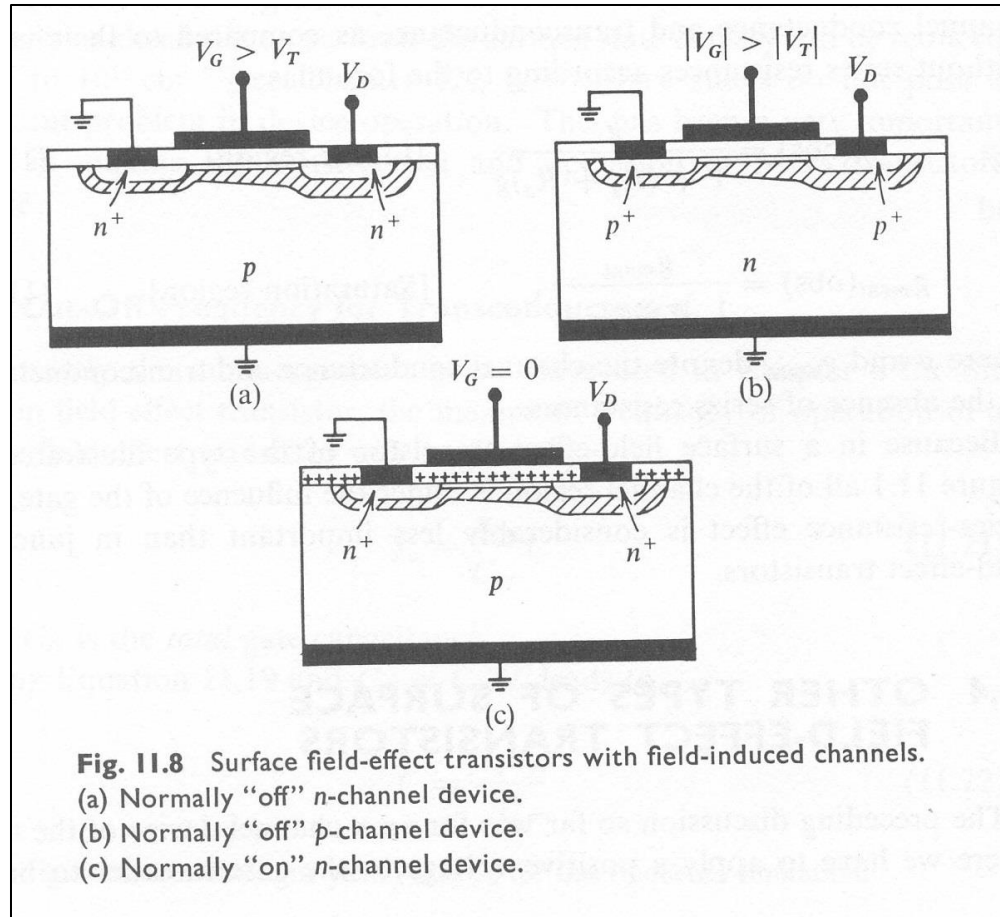


Here, a negative voltage on the control terminal will cause a positive charge layer to appear in the silicon, and current will flow a voltage is applied between the two lateral terminals. This type of transistor is known as a “pMOS transistor.”

44. It has long been known in the art that these two types of transistors (nMOS and pMOS) are not only structurally mirror-images of each other – they are also electrical mirror-images of each other. Writing in 1967, Andy Grove² (at pp. 329 – 330) described this situation for the two types of transistor:

The preceding discussion so far was for an *n*-channel device of the type where we have to apply a positive voltage to the gate in order to bring about the onset of channel conduction. By complete analogy, the discussion could have been applied to a *p*-channel where a negative gate voltage would have been required to bring about channel conduction. Because with zero gate voltage applied neither of these devices conducts, such devices are called *normally “off”* MOS transistors. (Emphasis in the original.)

² EX1010, A. Grove, *Physics and Technology of Semiconductor Devices*, John Wiley & Sons, 1967.



The MOS transistor was new at the time, and so this was the physics-based state of the art at the time.

45. However, it was soon realized that nMOS transistors and pMOS transistors could be made to be “complementary” (a word-usage that will be explained momentarily) by changing the substrate bias that is applied to the pMOS transistor. As a more-recent textbook³ on digital design states (at p. 71) the situation,

³ EX1011, S. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design* (third edition), McGraw-Hill, 2003.

“Notice that in order to be biased properly, the n-well region must also have a VDD contact.” As is well-known in the art, the n-well provides the substrate contact (via which the substrate bias is applied) for a pMOS transistor in a typical silicon fabrication process.

46. However, as they are fabricated in (as the name indicates) a thin film (rather than in a silicon substrate), thin-film transistors are unable to have a substrate contact (of the type shown above, in the figure from Grove 1967); only a gate contact and the two lateral contacts (for the current flow) are available.

47. Thus, thin-film transistors will not be able to use the type of complementarity that is fundamental to silicon-based transistor technology (such as the ubiquitous complementary MOS (CMOS) technology that dominates the semiconductor landscape today). Instead, nMOS thin-film transistors and pMOS thin-film transistors must be operated as per the discussion in Grove 1967 that was quoted above – that in order to induce conduction in an nMOS transistor a positive voltage must be applied to the gate, while in a pMOS transistor a negative voltage must be applied to the gate. In this way, nMOS and pMOS transistors are able to provide simple on/off switches – which turn on-or-off under mirror-opposite control voltages.

48. Further, the “complementary” situation also led, in the art, to the following simple circuit symbols for nMOS and pMOS transistor types.



An analog CMOS textbook⁴ (from 1997) also shows commonly-used nMOS and pMOS transistor symbols. See EX1008 at 18 (especially Figure 1.7(a) and Figure 1.8(c)). The pMOS symbol in particular is notable for its inclusion of a small circle on the gate contact; this symbol is used in electronic circuitry (and logic circuitry) to indicate “NOT” – which is a way of denoting a pMOS transistor as behaving in the opposite (i.e., “NOT”) way as behaves an nMOS transistor.

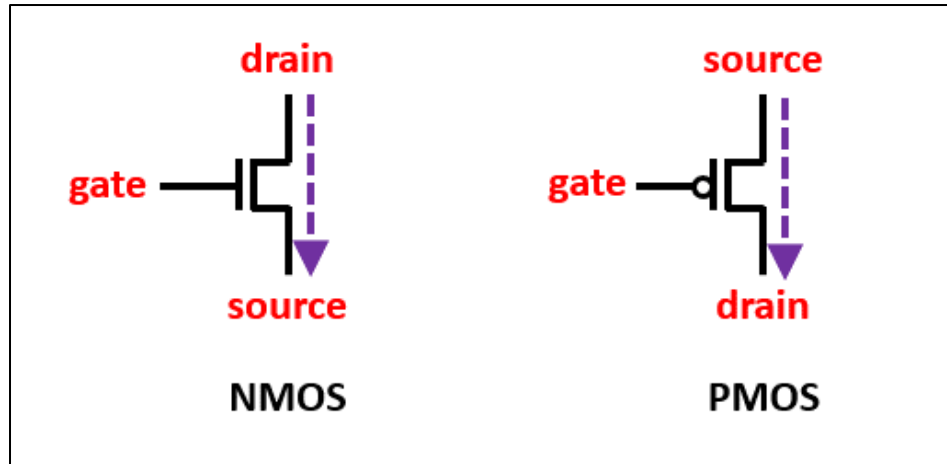
49. Even though a pMOS thin-film transistor is not able to be rendered “complementary” (as it lacks a substrate contact), the use of the pMOS symbol depicted above is still commonly used in the art to represent a pMOS TFT.

50. Further, although the MOS transistor is inherently a symmetric device, some way of separately identifying the two lateral terminals is required. For historical reasons, the side that provides the entry point for carrier flow came to be known as the “source,” while the side that provides the exit point for the current flow

⁴ D. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, 1997.

came to be known as the “drain.” However, defining the “direction” of the current flow is slightly problematic – as “current” is defined in the art (and has been for centuries) as the direction in which what would be positive charge flows; thus, for example, if there is a flow of negatively-charged electrons moving in some direction, the defined direction of the current flow is the *opposite* of the direction in which the electrons are actually moving.

51. This situation can be depicted graphically:



This methodology allows the “source” and the “drain” to be defined via the direction of the current flow (which is determined by the relative voltages on the lateral terminals) in any particular transistor (of either type). This is explained succinctly in Chapter 1 of Johns & Martin 1997:

It should be noted that there is no physical difference between the drain and the source. *The source terminal of an n-channel transistor is defined as whichever of the two terminals has a lower voltage.* For a p-channel transistor, the source would be the terminal with the higher voltage. When a transistor is turned on, current flows from the drain to

the source in an n-channel transistor and from the source to the drain in a p-channel transistor. In both cases, the true carriers travel from the source to the drain, but the current directions are different because n-channel carriers (electrons) are negative, whereas p-channel carriers (holes) are positive.

EX1008 at 16-17 (emphasis in original).

52. In most circuit applications, the flow of current through any transistor during circuit operation is one-way – that is, current flows through any particular transistor in only one of the two possible ways⁵; this allows the current flow to define what are the “source” and the “drain” of any transistor based on this operational characteristic. However, the MOS transistor is inherently a symmetric device – where the current can be induced to flow in either direction by the application of different voltage differences between the two lateral terminals; a prominent example of this situation is the single transistor which controls the charge-storage node of a DRAM memory cell – where different lateral voltages (i.e., positive or negative) are used to put charge into the storage node and to take charge out of the storage node. In theory, the “source” and the “drain” would be swapped back-and-forth during these different circuit operations – even though there is (obviously) no material change in the transistor itself. Further, when a circuit “netlist” is created (usually

⁵ This is the case for the circuitry disclosed in the ‘599 patent, and for the prior art to be considered in this Declaration.

for purposes of describing the circuit to a circuit simulation CAD tool, such as a SPICE circuit simulator), the four terminals of a MOS transistor (the drain, the gate, the source, and the substrate) must be explicitly specified – and will not be changed “on the fly” based on the voltages applied to a particular transistor; however, in this type of situation, if the sign of the voltage between the drain and source is reversed, the circuit simulator will simply cope with this – since, as mentioned above, the MOS transistor is inherently symmetric (and can be “operated” in either direction).

53. Fortunately (as mentioned above) this complex issue need not be of concern here – since (as also mentioned above) the circuitry described in the ‘599 patent (and in the prior art to be discussed later in this Declaration) operates such that current will only flow through any MOS transistor in one direction only. Thus, the scheme discussed above (and depicted in the figure above) of defining the “source” and the “drain” in terms of the current flow in the type of device in question (nMOS or pMOS) is workable here; thus, the working definition of “source” and “drain” will be used in this Declaration.

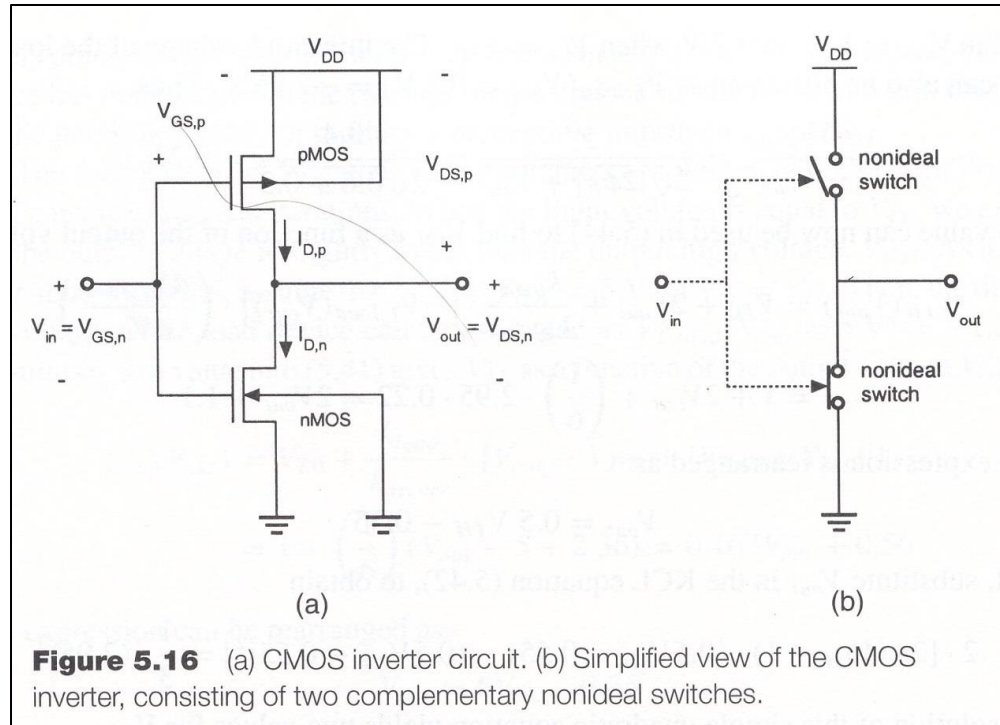
54. Finally, with respect to field-effect transistors in general and the ‘599 patent in particular, as was noted above the field-effect transistors in the ‘599 patent are of type known as a thin-film transistor (TFT). A TFT is sufficiently similar to a MOSFET (or, basically, any other type of field-effect transistor) to allow the basic understandings and descriptions (both qualitative and quantitative) associated with

the ubiquitous MOSFET (as detailed above) to be applied to the TFT. The patentee was aware of this basic relationship (as would be a POSITA) – and used it (as will be detailed later) to describe the TFTs that appear in the '599 patent.

55. TFTs are very advantageous in display applications – as they can be fabricated directly on the glass that is used in the display; however, TFTs (as just noted) are still field-effect transistors – and operate in the same way as do silicon-based field-effect transistors (as described above).

2. nMOS/pMOS Interchangeability

56. As detailed above, the nMOS transistor and the pMOS transistor are essentially mirror-images of each other. Furthermore, as was detailed earlier, a field-effect transistor, in its simplest usage, provides an electronic on/off switch with no moving parts – and this statement applies to both nMOS and pMOS transistors. This has long been well-known in the art – as can be seen in Kang and Leblebici 2003 (EX1011 at 198):



57. If the design need is for a transistor to be used as a simple on/off switch, then either an nMOS transistor or a pMOS transistor can be chosen – since, as shown in the figure from Kang and Leblebici 2003 above, each can function as a simple on-off switch. As the primary operational difference between nMOS and pMOS (when a simple switch is desired) is that the on/off characteristics are the opposite of each other – and the on-off signals to be applied must be altered (i.e., reversed as it were) to account for this. In particular, as described in Section VII.A.1, nMOS devices turn on in response to a “high” voltage on the gate terminal and turn off when a “low” voltage is applied. This is known in the art as “active-high” signaling. pMOS transistors are just the opposite – they turn on when a “low” voltage is applied to the gate terminal and turn off in response to a “high” voltage on the gate. This is known

in the art as “active-low” signaling. Changing the polarity of a switching transistor (from nMOS to pMOS or vice versa) would require changing the polarity of the gate signal to achieve the same functionality, but doing so was easy and well-known to a POSITA. In contrast, swapping an nMOS transistor that performs an analog-like function for a pMOS transistor (or vice versa) may be more difficult, no such change is proposed in this IPR.

58. Finally, there is another consideration in play – that of cost and complexity. As has long been known in the art, when the dominant silicon logic technology changed from NMOS to CMOS, about the only downside of this change was the expanded complexity of the manufacturing process involved. As noted in Kang and Leblebici 2003 (EX1011 at 198), in NMOS only nMOS transistors need be fabricated, while in CMOS both nMOS transistors and pMOS transistors must be fabricated together. (“Since nMOS and pMOS transistors must be fabricated on the same chip side-by-side, the CMOS process is more complex than the standard nMOS-only process.”) This situation also arises with TFTs, if both nMOS transistors and pMOS transistors are to be fabricated together; if only one species (nMOS or pMOS) is used exclusively in a circuit, then the process complexity and the cost will be lower.

3. The Transistor Threshold Voltage

59. In Section VII.A.1, the basic notions of field-effect transistors were presented. In particular, for the simplified case of the use of such transistors as simple on/off switches, the operational considerations for the transistors involved are also rather simple.

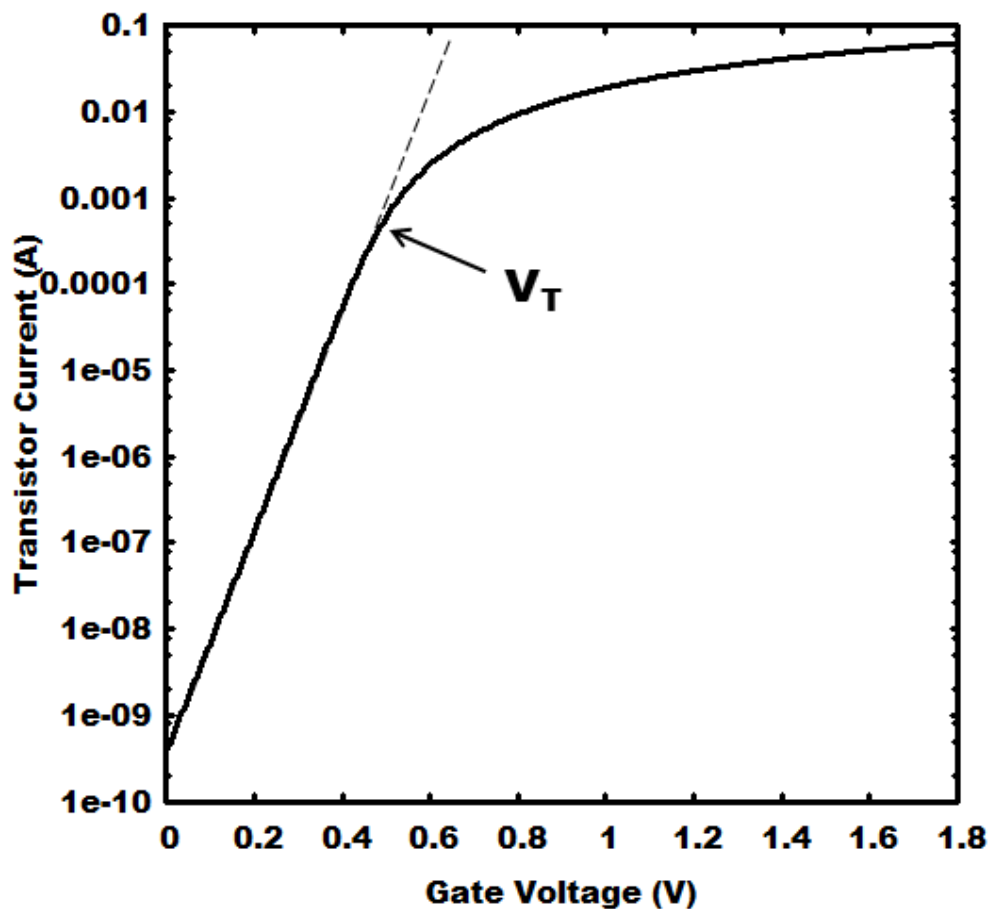
60. However, one issue that was glossed over is how the “off” state and the “on” state are differentiated from each other – other than that these two operational states actually exist. The only other consideration (to be discussed below) is to make sure that the “on” state is really on, and (obviously more challenging) that the “off” state is really off.

61. In Section VII.A.1, it was described how a field-effect transistor is turned on or off by changing the gate voltage from either high-to-low or low-to-high). That the “change” must occur at *some* particular (and identifiable) gate voltage value (for a particular transistor); that particular voltage value has long been known in the art as the “threshold voltage.” See EX1008 at 20.

62. In an ideal transistor, for a gate voltage below the threshold voltage, the transistor would simply be completely off (i.e., absolutely *no* current flowing through it), while for a gate voltage above the threshold voltage, the transistor would be in a completely-on state (i.e., for any gate voltage above the threshold voltage, the current is constant at the “on” current level). In fact, in this situation, the actual

value of the threshold voltage would essentially not matter – as long as it was somewhere between the low voltage level and the high voltage level (of the on/off logic voltage levels).

63. However, the field-effect transistor is not so simple a structure – and the threshold voltage behavior is much more complex. This is readily illustrated by an exemplary depiction of the device current (in logarithmic scale) versus the applied gate voltage.



In this figure, the threshold voltage can be defined via the point where the straight line at low gate voltage changes (as the gate voltage increases) to the more-slowly increasing curve.

64. This curve shows that the MOS transistor does not, in detail, operate explicitly as a simple on/off switch; rather, the behavior of the current as a function of the gate voltage shows what was stated earlier – that in detail, the MOS transistor (like all field-effect transistors) is a voltage-controlled current source. In addition, this curve, in-and-of itself, highlights the two critical issues that revolve around the “threshold voltage” *not* being able to exist as a simple dividing point between (as described above) all-off and all-on.

65. First, it can be easily seen that for gate voltages above the threshold voltage, the current is not a constant with gate voltage – but, rather, increases notably for higher gate voltages. As circuit switching speed is (among other things) a direct function of the current, it is desirable (in the on state) to have as much current as possible flowing through the transistor – which indicates that the threshold voltage should be as low as possible.

66. Second, though, it can also be seen that the characteristic behavior of a field-effect transistor is not ideal – in that the transistor current does not go to zero just below the threshold voltage, but rather decreases (exponentially) as the gate voltage decreases below the threshold voltage. As a result, the threshold voltage has

to be chosen (during manufacturing-process design) to be somewhat higher than the desired near-zero gate-voltage value.⁶

67. In sum, the value of the threshold voltage should be as low as possible – but not lower; otherwise, even though the transistor will be to some degree “off,” there will be too much current flowing in the “off” state – which is something that can have serious-and-unpleasant consequences in most circuit applications.

4. Process Variability

68. In an ideal world, when many different units of some type are manufactured (cam shafts for engines, grinding equipment for the manufacture of powdered cement, transistors, etc.), each-and-every unit manufactured would be

⁶ As will be discussed later, the ‘599 patent makes use of a current model for field effect transistors that is known in the art as the “Shichman-Hodges model” (see EX1009, *Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits*, H. Shichman and D. Hodges, IEEE Journal of Solid State Circuits vol. SC-3, pp. 285 – 289 (1968)). As the MOS transistor was disclosed in 1963, the Shichman-Hodges model was introduced shortly thereafter (in 1968) – to allow the MOS transistor to more-effectively used in circuit design, and also to provide a model that could be used for circuit simulation. Notably, the Shichman-Hodges model describes the first of these two features (that the transistor current increases as the gate voltage increases above the threshold voltage), but does not describe the second feature (i.e., the model treats the transistor current as zero for gate voltages below the threshold voltage).

absolutely identical with every other unit manufactured. However, even for well-controlled, stable manufacturing processes, there will be statistical variability in the defining characteristics – with a well-defined constant (with time) mean (average) value of the quantifiable characteristics, and a Gaussian (i.e., “bell-curve”) distribution of those statistical variations around that mean value.

69. Transistors, being objects that are mass-produced in well-controlled processes that exhibit these kinds of expected statistical behaviors, are subject to such statistical variabilities in their various characteristics. In field-effect transistors, one of the most prominent-such characteristics subject to such statistical variability is the transistor threshold voltage; the transistor threshold voltage will show a statistical mean and a Gaussian distribution of variabilities (from transistor-to-transistor) around that mean value.

70. In the case described above, this has effects on the on/off usage scenario. If the threshold voltage varies (in a particular transistor) to the high side, then the “on” value of the current will be somewhat reduced – and the transistor will be slower than the mean operation speed. If threshold voltage varies (in a particular transistor) to the low side, then the current flow in what is supposed to be the “off” state will be higher – and the transistor will be “less off” than would be expected from the statistical mean case. This latter situation actually tends to be the more-problematic one in practice – as excessive (vs. expectations) off-current causes

numerous problems (such as excessive battery drain in a mobile device for circuits that are supposed to be “off”). Further, circuit design must be done not against the statistical-mean case – but rather, against the worst-case scenario; thus, this type of statistical variability forces designers to be less-aggressive – and to accept slower circuit performance as a way of avoiding potentially-catastrophic troubles.

71. The above description is basically “digital” in nature – in that with the transistors being treated as on/off switches they will still work; their performance will be reduced; this is because in logic circuitry situations, the logic nodes in the circuit are being charged to well-defined “high” and “low” levels – with variability largely being a concern due to the aforementioned slowing-down of that charging (which slows down overall circuit switching speed).

72. However, in some applications, the concern is the variability of the actual current level across different instances of “identical” transistors. For example, in analog circuit design, current mismatch between two transistors in a particular circuit (such as a current mirror) is problematic – and specific techniques in how the transistors are actually drawn on-wafer (i.e., at the physical design level) are employed to minimize the difference in the current between two adjacent transistors.

73. It has long been known that this current mismatch problem is caused (for the most part) by mismatch between the (ideally-identical) threshold voltages of two transistors. Obviously, while the “current mirror” gets its name from being a

circuit that will (ideally) take a current in one circuit branch and exactly reproduce in another branch, this current-mirroring will deviate from an exact match due to this inter-device variability in the threshold voltage.

74. Thus, in any circuitry that uses numerous instances of what are supposed to be (ideally) identical transistors, and where those ideally-identical transistors would all ideally be producing the exact same output current, this variability among the threshold voltage of numerous transistors will induce variability among the current outputs of those numerous transistors; the degree of the problems thus induced depends on the particular manufacturing process in use – but also upon the degree to which the particular circuit application is vulnerable to degradation of some sort due to this real-world reality.

5. Threshold Voltage Compensation

75. In circuit design, compensation is best thought of as being a generalized approach in which parts of the circuitry are designed so that they can automatically adjust the operation of the circuit – so that the variability of certain aspects of the circuitry are greatly reduced (or completely eliminated). Thus, “compensation” generally involves feedback, which is used to achieve such a stated goal.

76. A number of compensation techniques, which serve to address a number of circuit-variability challenges, are known in the art. A prominent and well-known example is the use of compensation techniques that serve to cause the voltage

that is output by a voltage reference circuit to be largely independent of temperature over a wide range of temperatures; a good example is provided by U.S. Patent No. 5,666,046 (EX1013) issued to Mietus, “Reference Voltage Circuit Having a Substantially Zero Temperature Coefficient.”

77. However, the compensation technique that appears in the ‘599 patent is a threshold-voltage-compensation technique. A known problem in the art is that for some number of transistors that are supposed to (ideally) be identical to each other, there will in fact be some degree of statistical variability of the threshold voltage (discussed in Section VII.A.3) across those transistors; due to this threshold voltage variability, the magnitude of the output current across these transistors will also vary from transistor to transistor – an occurrence that is problematic in many circuit situations.

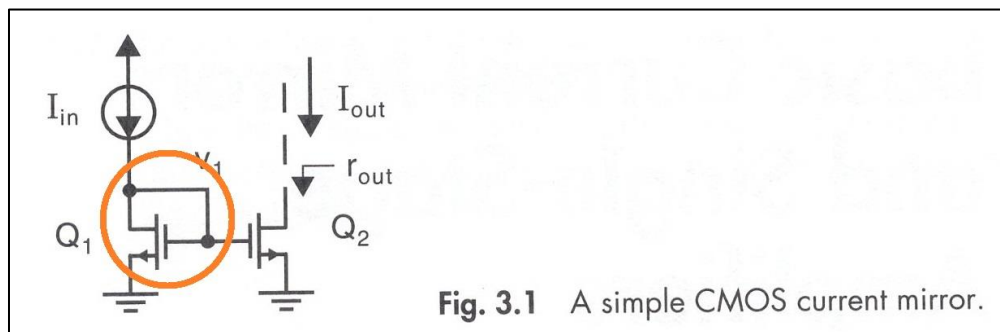
78. A good example of a threshold-voltage compensation technique is provided in a conference paper — J. Sanford and F. Libsch, *TFT AMOLED Pixel Circuits and Driving Methods*, SID 03 Digest, pp. 10 – 13 (2003) (EX1014). Further examples include J. Goh, *A New Pixel Circuit for Active Matrix Organic Light Emitting Diodes*, IEEE Electron Device Letters vol. 23, pp. 544 – 546 (2002) (EX1015); J. Goh and C. Kim, *A Novel Pixel Circuit for Active-Matrix Organic Light-Emitting Diodes*, SID 03 Digest, pp. 494 – 497 (2003) (EX1016); and R. Hattori et al., *Current-Writing Active-Matrix Circuit for Organic Light-Emitting*

Diode Display Using a-Si:H Thin-Film-Transistors, IEICE Transactions on Electronics vol. E83-C, pp. 779 – 782 (2000) (EX1017).

79. As can be seen from these examples, various solutions to the problem of inter-transistor threshold voltage variability – and its effect on TFTs – have been well-known in the art for some time.

6. The Diode-Connected Configuration of a Field-Effect Transistor

80. To connect a transistor “in the form of a diode” is something that is well-known in the art – and refers to a configuration of a field-effect transistor⁷ in which the gate of the transistor is directly connected to either the source or the drain of that same transistor. For example, Johns and Martins 1997 illustrates this well-known configuration being used in a current mirror:⁸



⁷ For completeness, it should be noted that other types of transistors (such as the bipolar transistor) can also be connected in the form of a diode.

⁸ The diode-connected portion of the current mirror is circled in orange.

EX1008 at 125-126; annotation added. Referring to this figure, this text states (on p. 125): “Note that Q1 is diode-connected (i.e., its drain and gate are connected)....”

As can be seen, in this configuration, the gate and the drain are directly connected together – so that the voltages on these two transistor terminals will always be the same in this configuration. As the gate/drain voltage is increased above the threshold voltage, the output current increases in a form that strongly resembles the current-voltage characteristic of a forward-biased diode – and hence the name of this structure, even though the transistor is not actually functioning explicitly as a diode does.

81. This very simple configuration has a very large number of useful applications – particularly in analog circuit design.

B. Electro-Optics

82. The ‘599 patent concerns driving circuitry that (in the patent) is specifically intended for use in the circuitry that drives the light-emitting element that provides light for a display screen. It should be noted (as will be discussed later) that while the circuitry described in the ‘599 patent is described as being used for display applications, the circuitry could equally be used for other applications where the same difficulties described in the ‘599 patent (the non-uniformity of the current output by different instances of a driving circuit due to inter-transistor variations in the threshold voltage) need to be addressed.

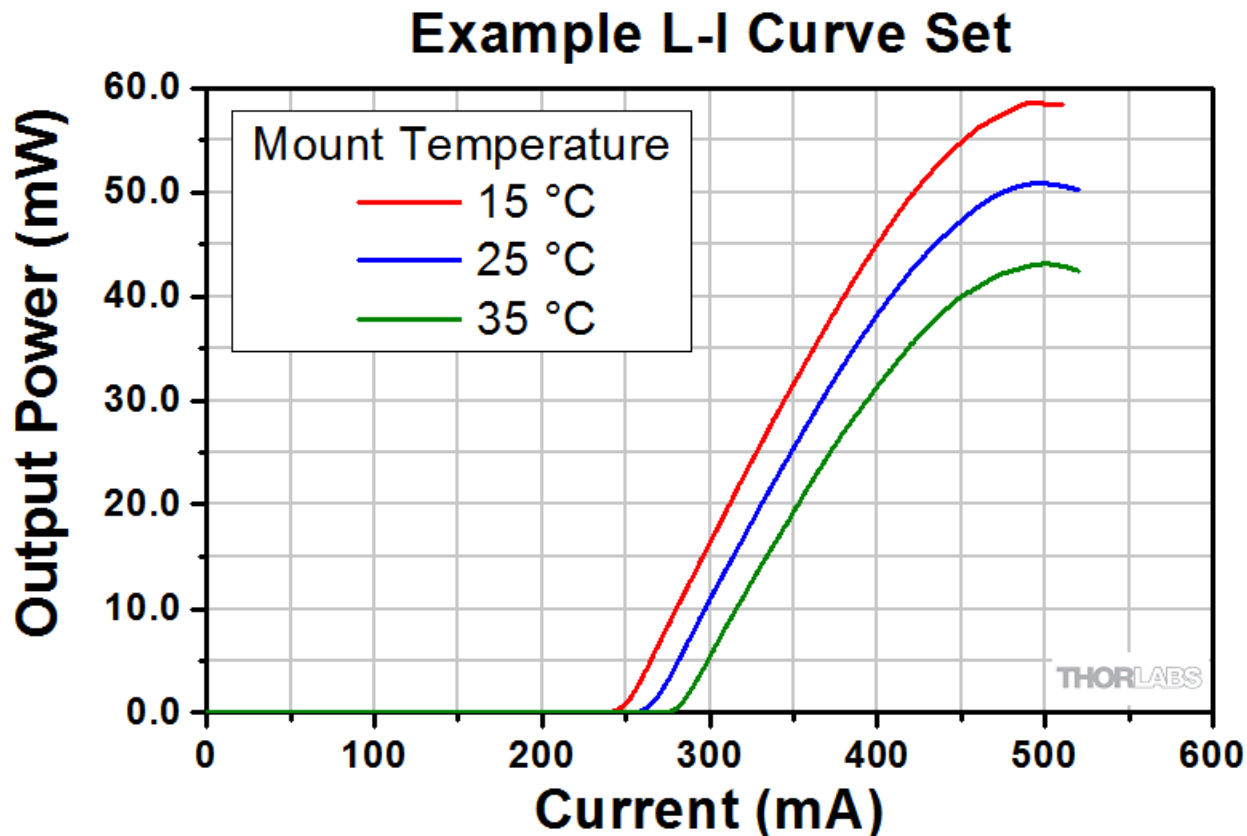
83. Therefore, the general nature of the constituent electro-optic components (light emitters and display pixels) will be discussed with respect to their utility to the disclosed circuitry, and for the clarification of display technology language that appears in the ‘599 patent.

1. Light-Emitting Devices

84. Electro-optics (as the name implies) involves conversions between the electrical domain and the optical domain – with electrical signals being converted to optical signals, and vice-versa. With respect to the ‘599 patent, the only electro-optic component that appears is the light-emitting unit that is turned on or turned off – so as to either illuminate or not-illuminate a particular pixel that is part of a display screen of some time; the details of such display screens will be considered below – while here, the light-emitter itself will be considered.

85. A rather-ubiquitous type of electrically-based light emitting device is what is known in the art as the light-emitting diode (LED). An LED is a diode that emits light when a forward bias is applied to that diode. The brightness (i.e., luminosity) of an LED is a strong function of the current that is flowing through the LED – which is not a surprise, as the forward bias current of a diode increases

exponentially as the forward-bias voltage is increased. A typical luminosity-current (L-I) curve for an LED is⁹:



86. As can be inferred from this exemplary L-I curve, the output power of the emitted light is a very strong function of the input current – so that the output power is very sensitive to small changes in the driving current. It can also be readily-inferred that for numerous instances of the same LED, if different driving circuitry has variability (between different instances of that driving circuitry), then the light output by different instances of LEDs will similarly vary considerably – with, again,

⁹ www.thorlabs.de/images/tabimages/QCL_LI_Curve_Set_General_A2-780.gif.

small differences (across instances) in the current leading to notable variabilities in the output power of the light.

87. The '599 patent in particular uses organic light-emitting diodes (OLEDs) as the light-emitting device. OLEDs function in basically the same manner as do conventional LEDs – but they have come into wide use in displays, for a variety of reasons. Among the noted advantages¹⁰ of OLEDs (particularly when used in displays) are the lighter materials involved (which are plastic), flexibility (again, because OLEDs use plastic material), greater brightness, lower power consumption, and ease of manufacturing (as they can be produced in sheet form rather than as individual LEDs).

2. Pixels and Pixel Arrays

88. A pixel is the basic unit of a light-based display screen – with that display consisting of row and columns of pixels – with a higher pixel density leading to a higher resolution in the display. This row/column structure of a display is well-known in the art by the use of the number of rows and columns that a display has – such as 1280 x 720, 1920 x 1080, and so forth. Note that these numbers provide the total number of pixels in a display – irrespective of the physical size of the display. In general, it is the areal density of pixels in a display that defines the quality of the

¹⁰ <https://electronics.howstuffworks.com/oled5.htm> .

image that can be produced by a display. Each pixel includes driving circuitry that provides current to the diode; further, each pixel typically includes a “driving transistor” to provide current for the light emitting diode, and various “switching transistors” that act as on/off switches to control the operation of the pixel.

89. Further, as the numbers above indicate (and as mentioned in association with them), in a display, the pixels are arranged into rows and columns – and these row and columns of the display are activated sequentially to produce images on a display screen.

90. In addition to pixel density, the quality of a display image is also a function of the brightness of the pixels – with brighter pixels generally leading to better image quality.

3. Scan Lines and Control Signals in a Display

91. As noted above, in a display based on pixels, the pixels are typically arranged in a row-and-column fashion. In operation, the individual pixels are generally not all “fired” simultaneously – that is, as individual pixels must change (i.e., turn on or off) when the image to be displayed changes, the individual pixels typically do not all change together at the same time.

92. Rather, a technique that has been used since the invention of screens that create non-fixed images using some form of light (that is, going back to the earliest days of cathode-ray tubes (CRTs), such as those used in the first televisions)

has been adopted. In this technique, the rows (sometimes called “lines”) of the display are treated as the basic units for changing pixel output as the display image changes – with all the pixels of a single row being changed as needed, and then the same process being applied to the next row, etc. In the context of an OLED display, a “scan signal” or “scan line signal” generally refers to the aforementioned control signal that is used for programming a line/row of pixels. This process continues until the entire display has been refreshed – via this sequential refreshing of each row; further, once the entire display has been refreshed in sequence, the next overall refresh sequence can begin.¹¹ As long as the speed of the refresh rate is faster than the ability of the human eye to detect it, the viewer will perceive the entire image changing fluidly upon the screen.¹²

93. As can be inferred from this discussion, a significant amount of behind-the-scenes control circuitry is required to manage this rather-intricate sort of screen-

¹¹ There have long been variations on this basic theme – such as, for example, refreshing every other row in one refresh pass, then refreshing the previously-unrefreshed row in the next refresh path; however, the basic approach of refreshing the display by sequentially (in one form or another) refreshing rows of pixels remains essentially the same.

¹² If the refresh rate is “too slow,” the human eye will perceive a noticeable (and unpleasant) flicker in the display.

refresh operation; it is this sort of control circuitry that is the main topic of the ‘599 patent.

VIII. THE CHALLENGED PATENT

94. U.S. Patent No. 7,414,599 (“the ‘599 patent” or “the challenged patent”) is entitled “Organic Limit Emitting Device Pixel Circuit and Driving Method Therefor.” The listed inventors are H. Chung, Y. Kim, C. Oh, O. Kwon, and S. Choi. The ‘599 patent claims priority to a Korean application (No. 10-2003-0045610) which was filed on July 7, 2003.

95. There are various aspects that merit a well-organized review of the ‘599 patent – so that this detailed overview can be provided here, and cited later in various locations in this Declaration.

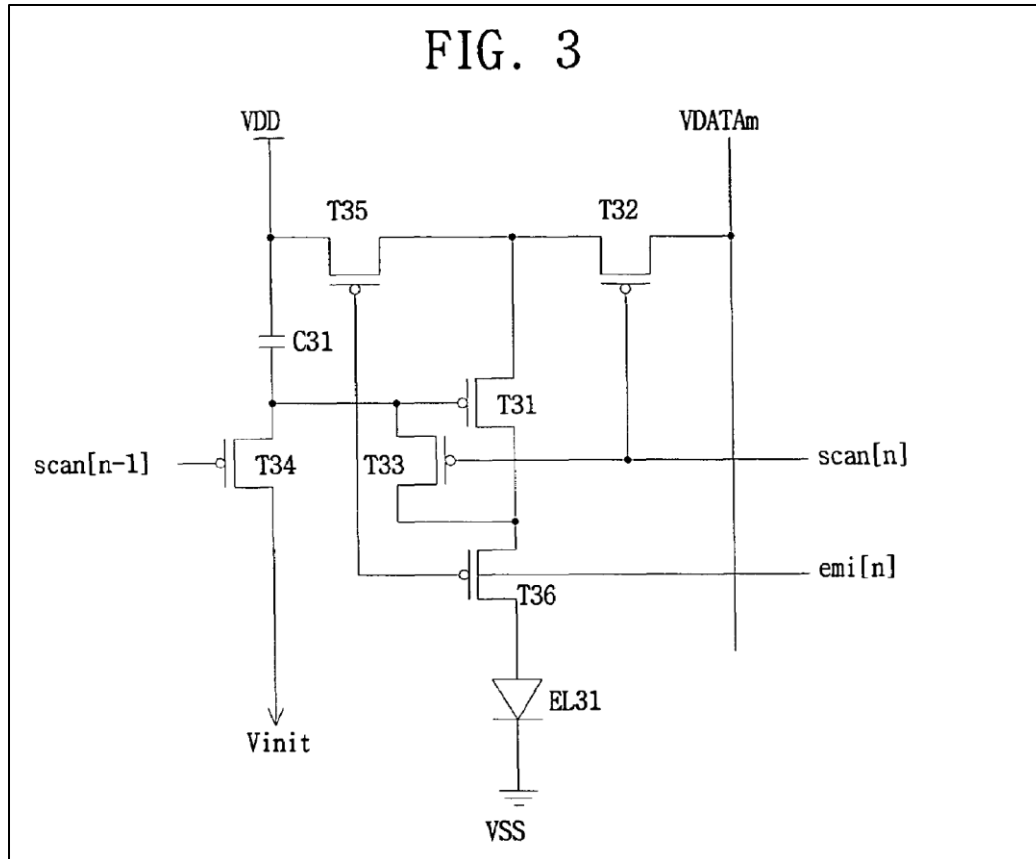
A. General Overview

96. As its title indicates, the ‘599 patent discloses a circuit – which is used in particular to provide current to an organic light-emitting diode (OLED) in a pixel of a display. As is well-known in the art (and as discussed in Section VII.B.1), the brightness of any LED is a strong function of the amount of current that is passing through it. The patent addresses the problem of variability of this current from transistor to transistor – which causes brightness to vary noticeably from pixel to pixel; the patent teaches an approach whereby the circuitry self-corrects against the cause of this interpixel variation in brightness.

97. According to the patent, the prior art example identified (and depicted in Figure 1) did not allow for correction of the problem of threshold voltage variations between the transistors of the individual pixel driver circuits associated with each pixel of a display; this causes the driving current level (which induces a pixel to emit light) to vary from pixel to pixel – which reduces the quality of an image that is being presented on a display. The ‘599 patent teaches a circuit whereby this threshold voltage variability (and resulting current variability) is overcome, so that the same current level will be provided to every pixel; by this approach, each pixel will emit light with the same brightness – thus improving the quality of an image on the display.

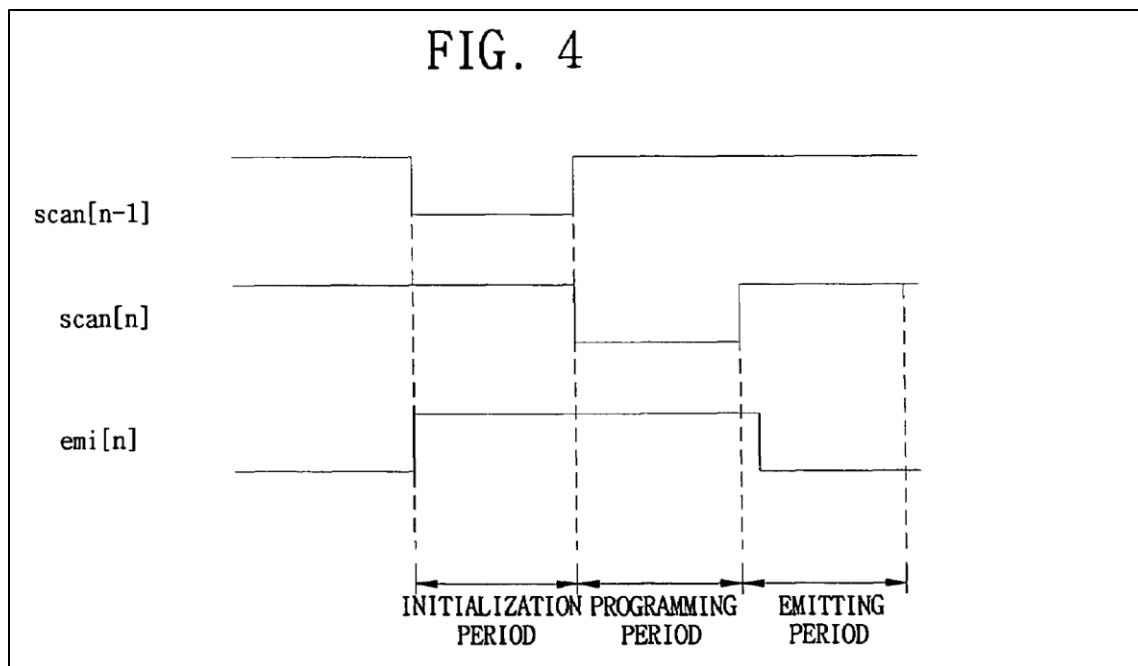
B. Circuit Operation

98. The ‘599 patent discloses a primary embodiment – which is contained in Figure 3 of the patent.



As noted above, it is useful to provide a more-detailed description of the operation of this circuit – as is detailed in the specification of the ‘599 patent.

99. The way that the circuit in Figure 3 is operated is detailed in the signal-waveform diagram of Figure 4:



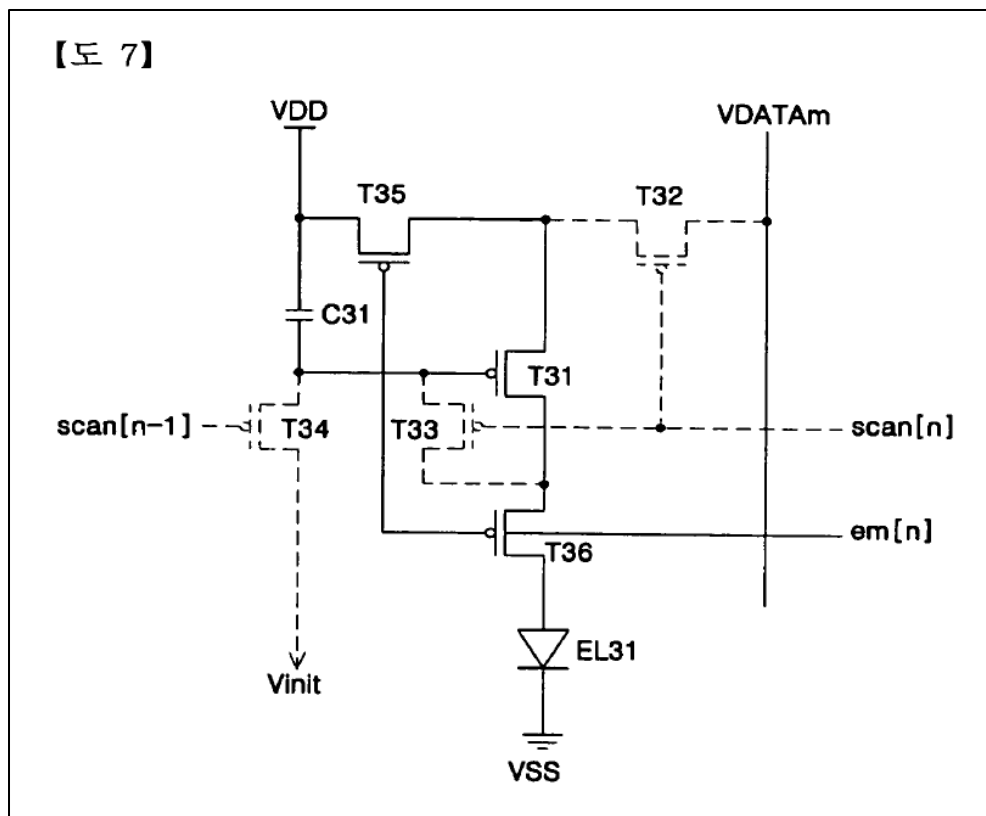
Note that as the transistors of the circuit in Figure 3 are all pMOS transistors, as per the discussion in Section VII.A.1, any of these transistors will be turned on when a waveform (of Figure 4) is pulled low, while any of these transistors will be turned off by pulling the waveform high. This is referred to in the art as an “active-low” signaling scheme.

100. Figure 4 shows that the circuitry depicted in Figure 3 will be operated in a manner (repeatedly – as the pixel rows of the display are refreshed) that involves the three stages of operation (i.e., the three periods) identified at the bottom of Figure 4. As it is drawn, Figure 4 provides a degree of continuity that is naturally built into this recurring usage of the three stages – such as the left-hand side of Figure 4 actually representing an “emitting period” prior to the one that is labeled on the right-hand side of Figure 4; this allows Figure 4 to be interpreted from left-to-right, as per

the continual pixel-refresh cycles that are provided to the display. In addition, the first identified operating period is the initialization period; however, the initialization period is somewhat difficult to understand without already having understood the programming period and the emitting period – and thus, below, the initialization period will be briefly described during the first encounter with it, then described in more detail following the detailed description of the programming period and the emitting period.

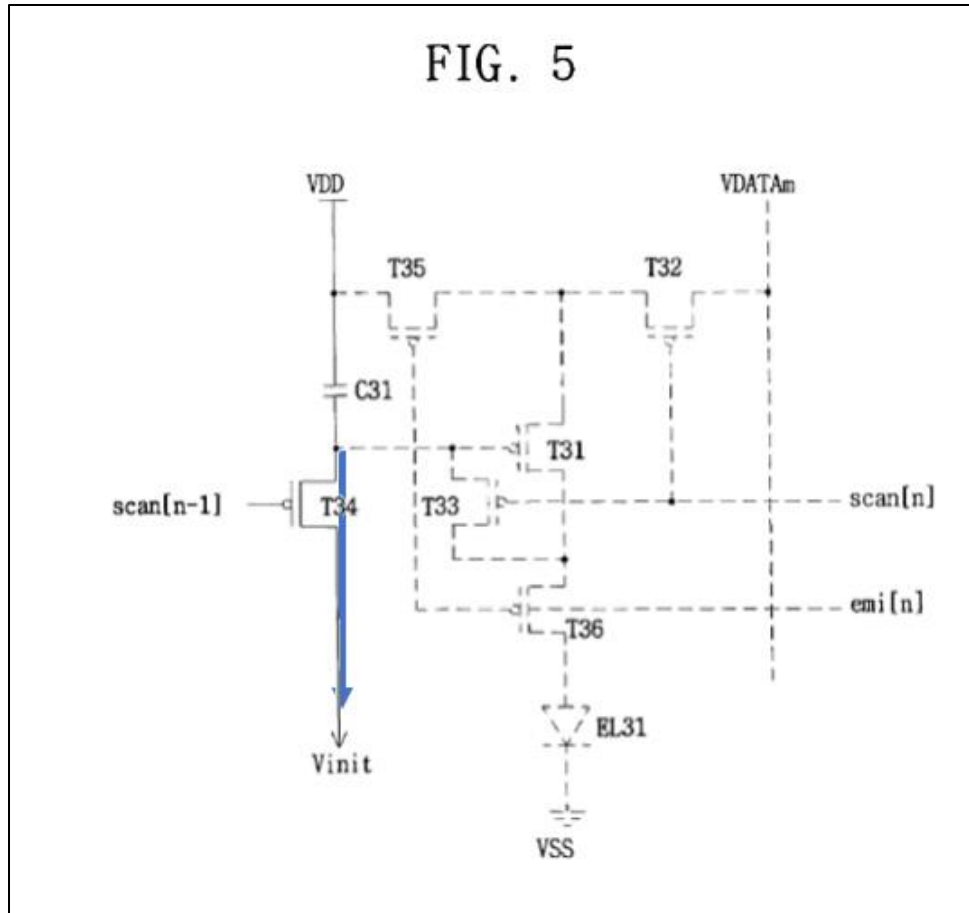
101. To begin on the left-hand side of Figure 4, although it is not labeled in the figure, the waveforms indicated that the waveform set begins in Figure 4 in an emitting period; the operation of this mode of the circuit of Figure 3 is provided in the patent, in what is supposed to be Figure 7.¹³

¹³ In the ‘599 patent, what is listed as “Figure 7” is erroneously a copy of Figure 6; however, the proper Figure 7 appears correctly in the Korean patent application mentioned above. Thus, in this Declaration, when “Figure 7” needs to be presented, the figure from the Korean patent application will be used.



102. As can be inferred from the waveforms, only the $emi[n]$ signal is held low – so that this signal turns on transistor T35 and T36, while transistors T32, T33, and T34 are held off, and transistor T31 is in a special state that will be explained below; for reasons that will be explained in more detail below, this creates a current flow path from VDD to VSS – in which current flows through transistor T35, transistor T31, transistor T36, and the light-emitting element EL31; this current flows through the electroluminescent element as forward-bias current to the light-emitting diode, causing it to emit light.

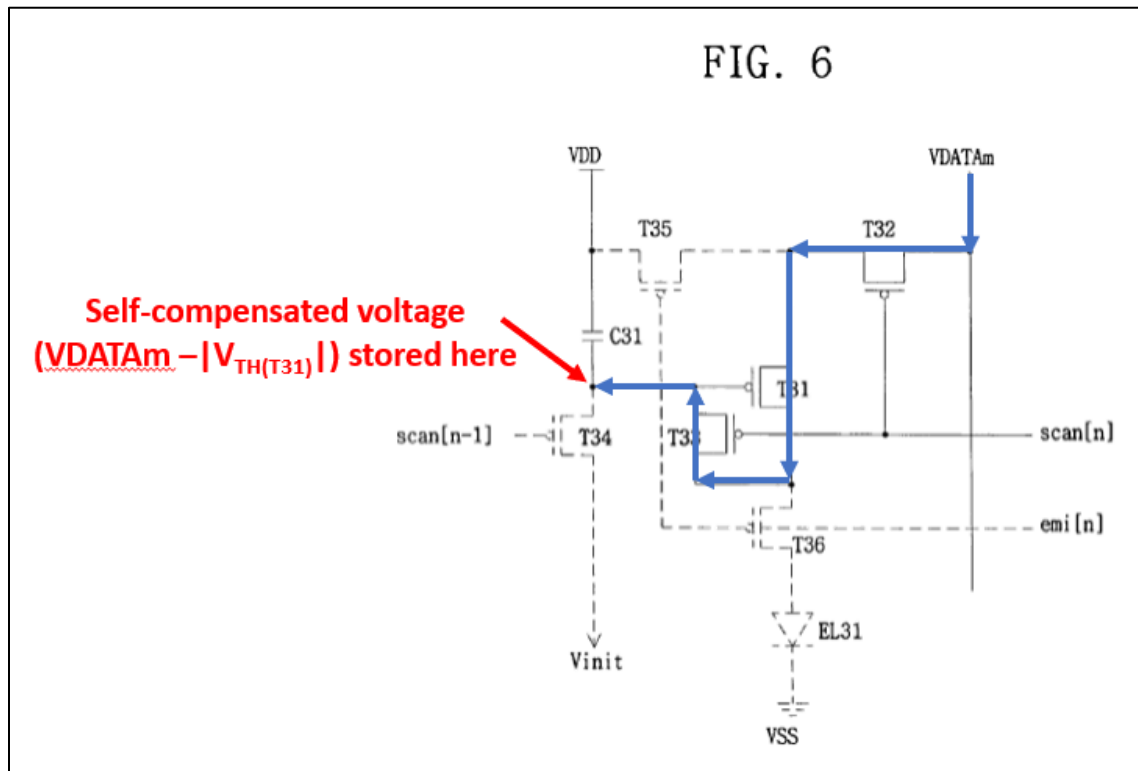
103. The emission period is ended by a transition to the initialization period; this is depicted in Figure 5 of the patent.



The change to this period (from the emitting period) involves changes to two control signals. First, the $emi[n]$ signal is pulled high; this turns off transistor T35 and transistor T36, causing the current flow that induces light emission from the emitter (as described above) to cease. Second, the prior scan line signal $scan[n-1]$ is pulled low, which turns on transistor T34. For reasons that will be explained below, this drains charge from the node that connects to the gate of transistor T31, pulling the voltage of that node down to V_{init} .

104. When the initialization period is completed, the programming period begins. This is the most intricate and complicated operating mode of the circuitry

of Figure 3, and requires a careful explanation. The programming period is depicted in Figure 6 of the patent.



105. As can be inferred from the waveforms of Figure 4, there are two control signal changes when the shift is made from the initialization period to the programming period. First, the scan[n-1] line is pulled back to high, turning off transistor T34; the draining of the aforementioned node was completed during the initialization period, and thus this transistor can be turned back off. Second, the scan[n] signal is pulled low, which turns on transistor T32 and transistor T33; this initiates a somewhat-complex circuit ballet that is described in the annotations added to the figure above – and which in particular requires a careful explanation. As is apparent, the scan[n] signal (called the “current scan [line] signal” in the claims) is

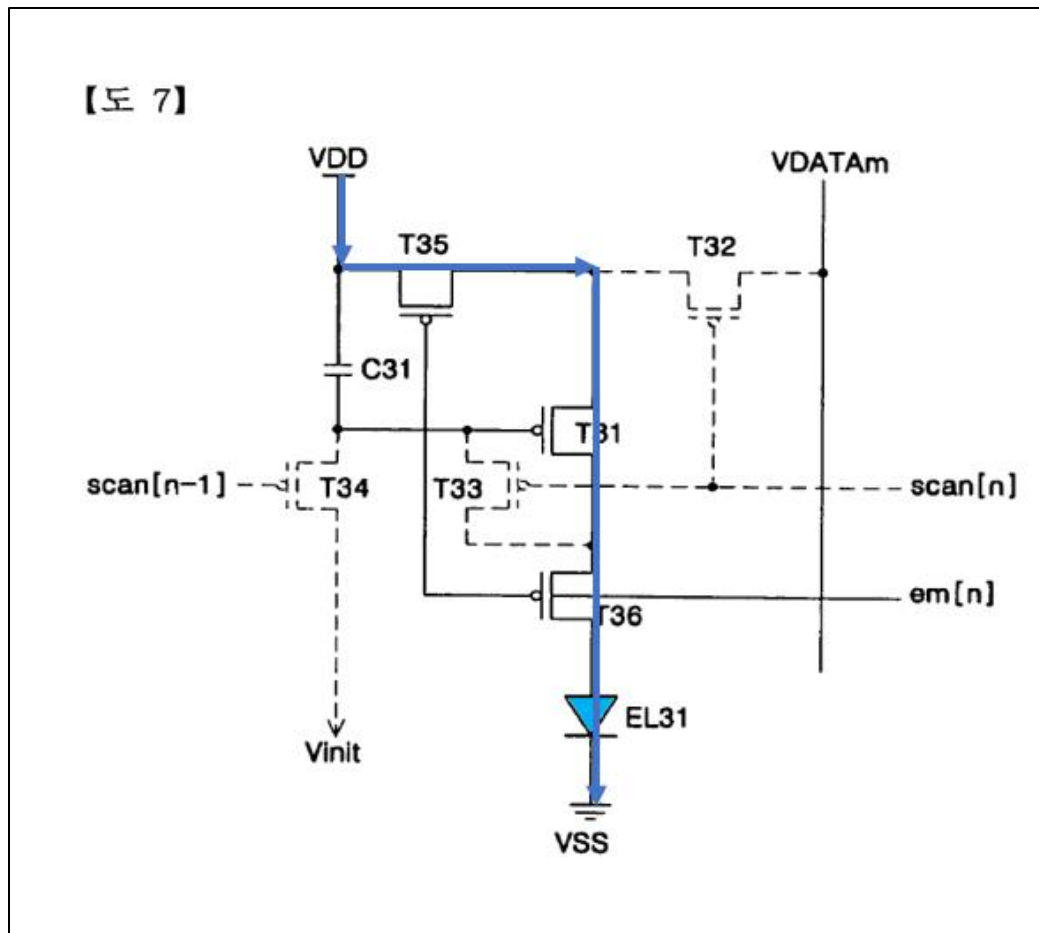
shown as a shared control signal that simultaneously (1) activates the first (T32) and third (T33) transistors so that the capacitor (and thus the node connected to the gate of transistor T31) can be charged, and (2) otherwise turns them off.

106. During the initialization period, as was described above, the node connected to the gate of transistor T32 has been pulled to a lower voltage (i.e., V_{init}) – so that transistor T31 has been turned on; however, as transistors T32, T35, and T36 are all turned off, there is no current-flow path through transistor T31, and thus no current will flow through that transistor. When the programming period begins, as described above, transistor T32 and transistor T33 are turned on; as shown in the annotated Figure 6 above, this causes current to flow through (in sequence) transistor T32, transistor T31, and transistor T33. This current path is in fact a “dead end” path to the node that connects to the gate of transistor T31 – and this node will begin to charge up, and its voltage level will rise. This charging will continue until the voltage on this node reaches a value of $(V_{DATAm} - |V_{TH(T31)}|)$ – at which point this induced voltage will turn off transistor T32. When this has been achieved, the programming phase is terminated – by pulling the scan[n] signal back to high, which turns off transistor T32 and transistor T33. At this point, the node that is connected to the gate of transistor T31 is completely (DC) isolated and the charge that flowed into that node is stored on the capacitor C31; as long as transistor T33 and transistor T34 remain off, there is no path for this charge to drain away, and the node will

retain the aforementioned voltage that has been “programmed” (hence the name of the period) there.

107. Note that the specific voltage induced on this node will be a specific function of the particular threshold voltage of the specific instance of transistor T31 in this particular case of the driving circuit that is driving the one particular pixel in question. For different driving circuits (for different pixels) with different instances of transistor T31 (wherein, as described in Section VII.A.4, the threshold voltage will vary), different values of this node voltage will be produced – for reasons that will be explained in more detail in the following section.

108. With the programming period ended, the emitting period can begin. The emitting period was detailed earlier (as a starting point), and the explanation will be briefly repeated here – again, using an annotated version of “Figure 7”:

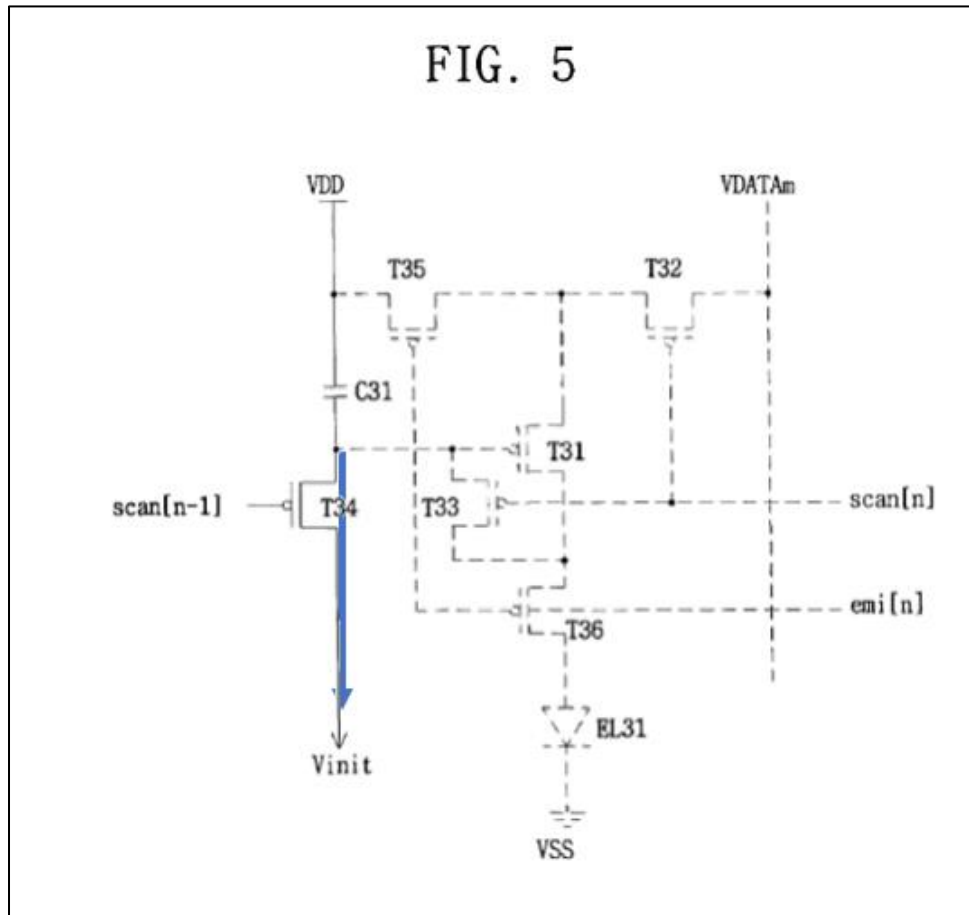


As was explained earlier, the emitting period involves pulling the `emi[n]` signal low – which turns on transistors T35 and T36; this creates a current flow path from VDD to VSS, with the current flowing through transistor T35, transistor T31, transistor T36, and the light-emitting element EL31 – causing that element to emit light.

109. This brings the discussion back to the initialization period – which, as noted earlier, can be more-readily explained now that the other details of the sequential operations (embodied in Figure 4) have been explained.

110. As described above, the emitting period is ended by pulling the emi[n] signal high – which turns off transistor T35 and transistor T36, which in turn cuts

off the aforementioned current-flow path that causes the light-emitting element EL31 to emit light. This ends the light emitting period. The initialization phase – explained briefly earlier, including via an annotated version of Figure 5 – begins again with the next pixel-refresh cycle:



As explained earlier, in this period the scan[n-1] line is pulled low – which turns on transistor T34, which causes the voltage on the node connected to the gate of transistor T31 (i.e., the charge stored on the capacitor C31) to be drained away until the voltage on this node decreases to Vinit. When this task is completed, the scan[n-

1] signal is pulled high – which turns off transistor T34, as the task has been completed. The next programming period can then begin.

111. The details of the initialization period and its immediate succession by the programming period can now be explained with more clarity than earlier. As the programming period serves to “program” the node connected to the gate of transistor T31, the initialization period serves to “de-program” (or “un-program”) that node – essentially, the programming applied to that node during the prior programming period is removed (i.e., erased), and the node has been set up to receive the next round of programming – as the next refresh cycle of the pixel of a particular driver circuit (and of the entire row of pixels in the display) is ready to begin.

112. The entire sequence of these three periods is repeated continually – each time that the refresh cycle reaches the particular row of pixels in question.

C. Threshold Voltage Compensation

113. As described in the prior section, the programming period described in the ‘599 patent serves largely to charge the node connected to the gate of transistor T31 to a voltage that is a function of the threshold voltage of transistor T31; in this way, for different instances of transistor T31 across different instances of the pixel-driver circuitry (of Figure 3), different values of the “programmed” voltage will be created for these different instances of transistor T31 – as the threshold voltage will

vary across these different instances of transistor T32 across those different pixel-driver circuits.

114. The programming period thus serves (among other things) to provide a way of compensating for these threshold voltage variations.

115. As was described in Section VII.B.1, the brightness (i.e., luminosity) of the light that is emitted by an LED is a strong function of the forward-bias current that is flowing through the LED; if this current varies across numerous instances of identical LEDs, the brightness will vary across these LED – and if these LEDs are used in the pixels of a display, this brightness-variability will noticeably-degrade the quality of the image that is presented on the display. Thus, some way of inducing the same current to flow through each instance of such multiple LEDs would be desirable.

116. As is relatively-easy to understand, a simple method of providing a current to an LED for light-emission (or for removing that current from the LED, causing it to turn off) is to provide that current via a transistor – which can be turned on or off, so as to turn the LED on or off. However, as discussed in Section VII.A.4, there will be some variability in the threshold voltage across many instances of the aforementioned transistor (due to statistical variations in a stable and well-controlled manufacturing process). As was explained in Section VII.A.1, a field-effect transistor does not provide an ideal switch – but rather, the current will vary to some

degree as the gate voltage (as imposed by a designer) and/or the threshold voltage (as caused by statistical variability) vary.

117. While to a coarse degree, a field-effect transistor can be regarded as a simple on/off switch (which is a digital interpretation), the finer details of the amount of current a field-effect transistor produces – and the fine-tuning of that current level – are actually analog functions.

118. Threshold voltage compensation is such an analog technique as applied to a field-effect transistor. Now, the threshold voltage compensation approach disclosed in the '599 patent can be explained in more detail.

119. As an initial item of critical importance to the task of threshold voltage compensation, a notable concern here involves what the designer can control and cannot control. The designer can set particular voltage levels on the transistor terminals to produce a corresponding output current; however, the designer cannot control the threshold voltage for a particular transistor – as the value of the threshold voltage is set during manufacturing-process development (in general) and in each particular transistor (in the specific); due to process variations during manufacturing, the threshold voltage will differ to some degree from transistor to transistor. In addition, the threshold voltage of a particular transistor may change with time as the transistor is used; this is a well-known phenomenon that also contributes to the threshold voltage differing to some degree from transistor to transistor.

120. Further, if particular details of the amount of current that is (or will be) flowing through a transistor are required, then more details must be considered in order to understand what is happening – since, as described earlier, the current being provided by a field-effect transistor is a function of both the gate voltage that is being applied and the inherent threshold voltage of a particular transistor.

121. In particular, a specific mathematical description of the amount of current flowing through a transistor – for a given set of applied terminal voltages – is required. The patentee was aware of this need – and invoked an approach that is well-known in the art, so as to provide a suitable mathematical description for the current that flows through a voltage-controlled current-source TFT.

122. The patentee used a well-known field-effect transistor current model – which appears in the specification at the top of column 3 and the top of column 8 (with the latter specific instance depicted here):

$$I_{EL31} = \frac{\beta}{2} (V_{GS} - V_{TH(M31)})^2$$

This is a very-well-known (and very old) generalized mathematical expression for the current in field-effect transistor. The term in parentheses ($V_{GS} - V_{TH}$) is known in the art as the “overdrive voltage” – as the current will effectively be zero when $V_{GS} = V_{TH}$, and will increase as V_{GS} is increased above V_{TH} ; notably, the term “overdrive voltage” appears twice in the specification of the ‘599 patent (at 1:59 and

1:66) – and that as the patentee provided no definition for this term, this serves to indicate that the patentee regarded this term as being well-known in the art at the time of the patent – and thus did not require the inclusion of a specific definition of this term in the patent.

123. Note in particular in the expression above that if the user holds the gate-source voltage (V_{GS}) constant across numerous transistors (which, in a normal circuit-design situation, is required) while the threshold voltage (V_{TH}) varies across those transistors, then the current produced will vary from transistor-to-transistor. The user can select a (fixed) value for the gate voltage, but just has to live with the inter-transistor variability of the threshold voltage – with the consequences just mentioned.

124. However, if some way could be found to adjust the actual applied gate voltage in each transistor, so that the overdrive voltage ($V_{GS} - V_{TH}$) could be made the same across all those transistors, then the current that is output would be the same across all of those transistors. This is the goal of threshold voltage compensation.

125. The '599 patent teaches an approach to providing such threshold compensation – as is described mathematically at the top of column 8:

$$\begin{aligned} I_{EL31} &= \frac{\beta}{2} (V_{GS} - V_{TH(M31)})^2 \\ &= \frac{\beta}{2} (V_{DD} - V_{DATA} + V_{TH(M31)} - V_{TH(M31)})^2 \end{aligned}$$

As is explained in the specification (at 8:1-21), the expression in parentheses in the second line above serves to provide the same overdrive voltage across a number of transistors – and to thus overcome the aforementioned problem of the threshold voltage varying from transistor to transistor.

126. As the specification explains,

As can be seen from the Expression 2, the driving current flows through EL element EL31, corresponding to the data signal voltage applied to the data line regardless of the threshold voltage of current driving transistor T31. That is, **because the present invention detects and self-compensates the threshold voltage deviation in current driving transistor T31 through transistor T33,** it is possible to finely control the current flowing into the organic EL element, thereby providing the high gradation of the organic EL element.

EX1001, 8:13-21 (emphasis added.). That is, the specification teaches that “the present invention” is to employ an approach that detects and self-compensates for threshold voltage deviations among different transistors. As a result, and as can be seen via examination of Expression 2, the overdrive voltage applied to every transistor is forced to be the same – and thus, the same driving current is applied to

all of the light-emitting elements, regardless of any inter-transistor variations in the threshold voltage across multiple instances of the transistor(s) providing current to the light-emitting element.

127. This is the “compensation” that is described in Claim 1, Claim 7, and Claim 14 of the ‘599 patent – in which the second transistor and the third transistor work together in combination to perform threshold voltage compensation. By implementing an approach that provides the same overdrive voltage to all transistors, the output current is the same across all transistors. In other words, any effects due to variations/deviations in the threshold voltage (from transistor to transistor) are eliminated.

IX. THE KIMURA PRIOR ART REFERENCE

128. U.S. Patent Publication 2003/0132931 (“Kimura,” EX1002), titled “Semiconductor Device and Driving Method Thereof,” published on July 17, 2003 from an application filed October 30, 2002. I have been instructed by counsel for Petitioner to assume that Kimura is prior art to the challenged patent.

129. That Kimura teaches in same area-of-interest as does the ‘599 patent is readily-apparent from the Abstract of this patent publication:

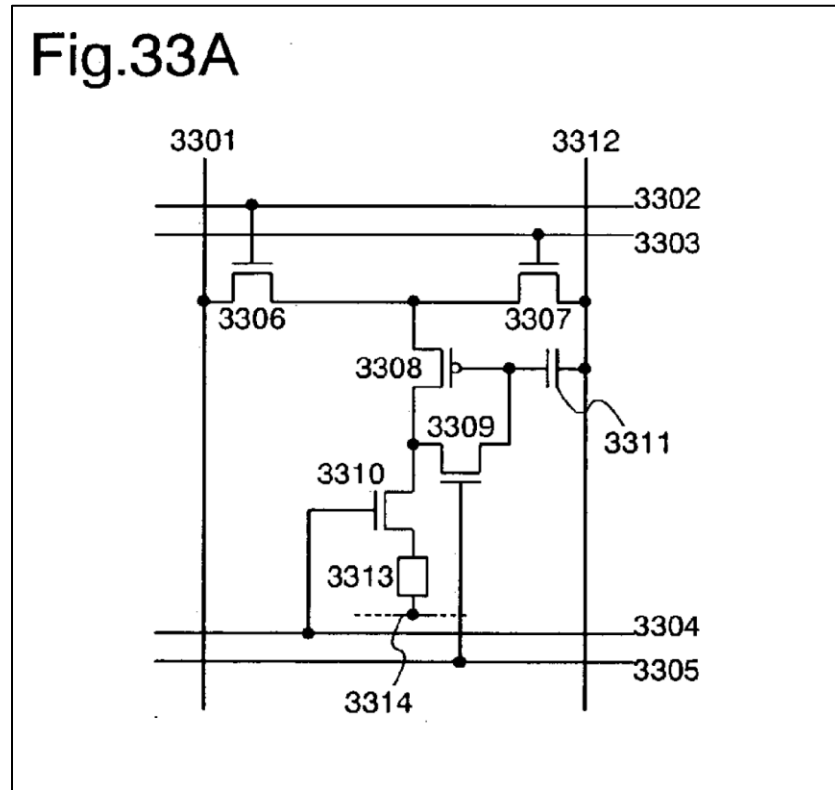
Brightness irregularities that develop in a light emitting device due to is persion [sic] among pixels in the threshold values of TFTs used for supplying electric current to light emitting devices become obstacles to improved image quality of the light emitting device. As an image signal input to a pixel from a source signal line, a desired electric

potential is applied to a gate electrode of a TFT for supplying electric current to an EL device, through a TFT having its gate and drain connected to each other. A voltage equal to the TFT threshold value is produced between the source and the drain of the TFT 105. An electric potential in which the image signal is offset by the amount of the threshold value is therefore applied to the gate electrode of the TFT. Further, TFTs are disposed in close proximity to each other within the pixel, so that dispersions in the TFT characteristics do not easily develop. A desired drain current can thus be supplied to the EL device even if there is dispersion in the threshold values of the TFTs among pixels, because this is offset by the threshold value of the TFT.

Kimura, Abstract. Kimura is a relatively long patent publication, containing dozens of figures and a robust specification that describes a number of embodiments – all of which is collectively-directed at addressing the challenges described in the Abstract of Kimura. Due to the size of Kimura, details of the numerous embodiments (and related teachings) will not be included here; rather, the embodiment of most interest here will be briefly reviewed.

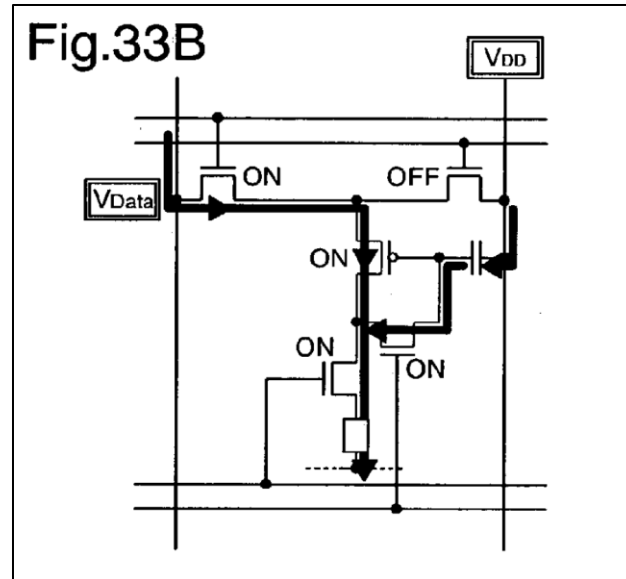
130. This particular embodiment in Kimura is contained in Figure 33 and described at [0654] – [0657]. It is important to note at the outset that Kimura Figure 36 is just an extension of Kimura Figure 33, and that (unless noted) the analysis and discussion of one figure applies equally to the other throughout this Declaration. Kimura explains the operation of the embodiment of Figure 33 by first providing a simple structural depiction of the circuitry in Figure 33A – providing the only

instance of the Figure 33 embodiment where the elements of the circuit are numbered so as to correspond to the discussion at [0654] – [0657].



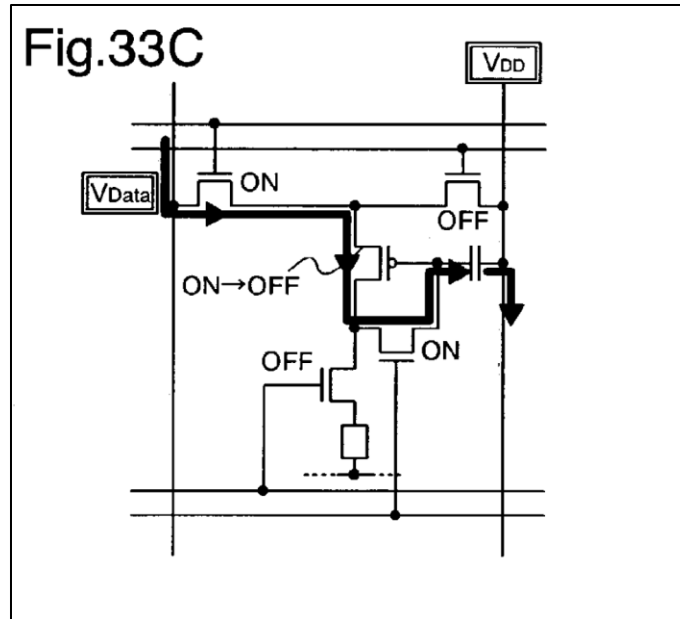
131. Further, it should be noted here at the outset that in the remaining images of Figure 33, Kimura has provided annotations to explain the operation of the disclosed circuitry; here, no annotations have been added to the figures from Kimura that will be presented below.

132. The first operational phase of the embodiment of Figure 33 is contained in Figure 33B.



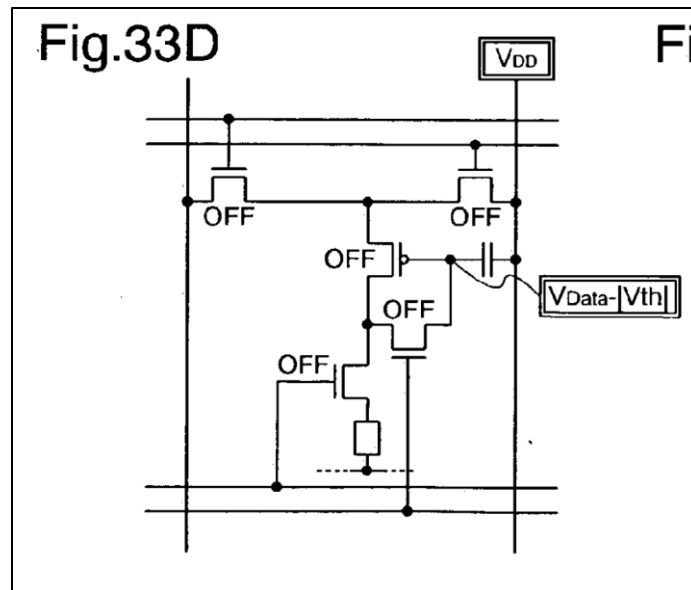
133. Here, transistor 3307 is turned off, while transistors 3306, 3309, and 3310 are turned on. As can be seen in the figure – and for reasons that will be explained below – with transistors 3309 and 3310 turned on, the voltage on the node that connects to the gate of transistor 3308 will be drained away, pulling the node low; this causes transistor 3308 to turn on.

134. The second operational phase of the embodiment of Figure 33 is contained in Figure 33C.



135. Once the node connected to the gate of transistor 3308 has been drained and that node pulled to a low voltage, transistor 3310 is turned off. Now, a current path has been created that essentially leads to a dead-end at the node that connects to the gate of transistor 3308. As shown, current flows through transistors 3306, 3308, and 3309 – “dead-ending” at the aforementioned node that is connected to the gate of transistor 3308, causing the node to charge up. This charging-up continues until the voltage on the aforementioned node reaches a value of $(V_{Data} - |V_{th(3308)}|)$ – at which point (as indicated in Figure 33C) transistor 3308 turns off and the voltage at this node has reached its final value for this phase of operation.

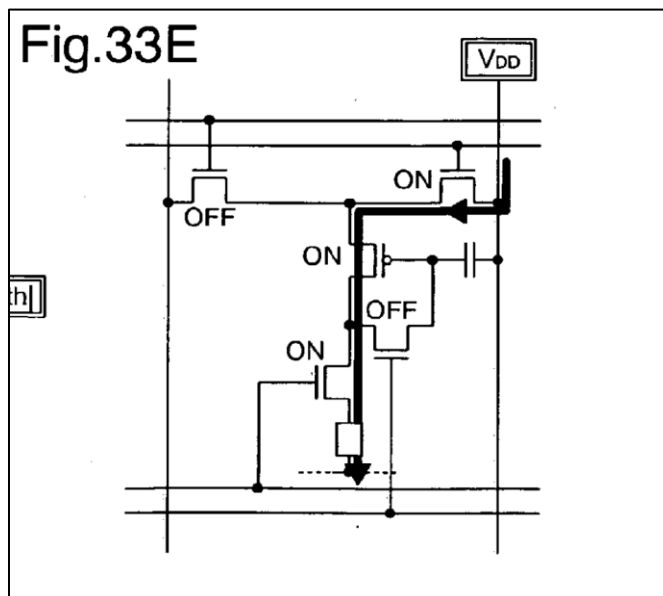
136. An intermediate step of the second operational phase is detailed in Figure 33D.



137. Here, transistors 3306 and 3309 have been turned off – and, as just mentioned, transistor 3308 essentially turned itself off during the second phase. As depicted in Figure 33D, with all of these transistors turned off, the node that is connected to transistor 3308 is electrically isolated – and thus it will retain the voltage that has just been created at that node. As noted in the figure, the specific voltage that is created at that node will be a function of the threshold voltage of the specific instance of transistor 3308 in the particular pixel-driver circuit in question – with that voltage varying across various instances of transistor 3308 across various multiple instances of the pixel-driver circuit. This is the method of threshold-voltage compensation that was already described above (in Section VIII.C) – and, notably, Kimura also uses the Shichman-Hodges model in describing the current that will be output by transistor 3308 when it has been programmed (whereby the overdrive voltage is induced to be the same across numerous instances of transistor 3308 (in

various pixel driver circuits) when there is variability in the threshold voltage value across those numerous transistors).

138. The third operational phase is depicted in Figure 33E.



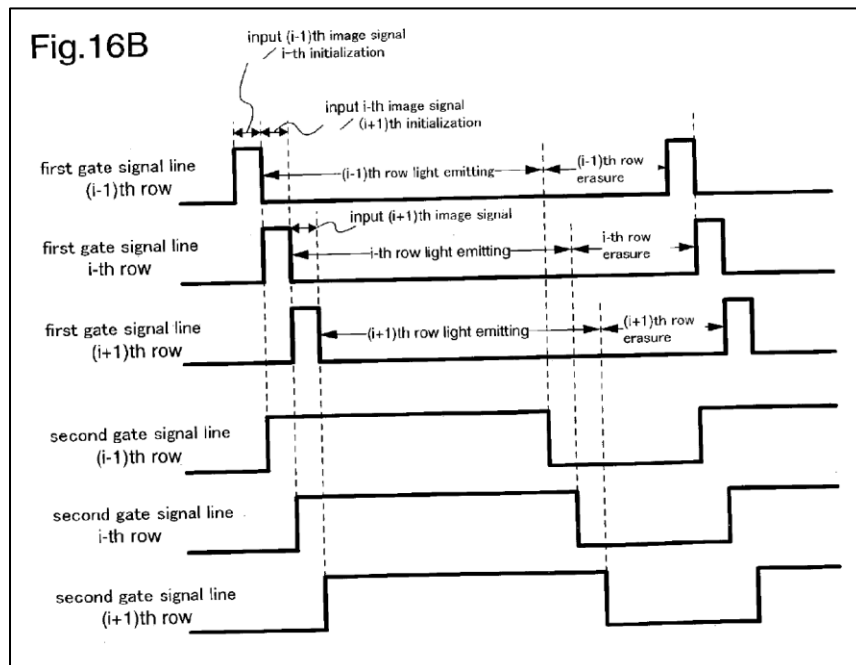
139. Here, transistors 3307 and 3310 are turned on, creating a current flow path from the supply voltage V_{DD} to the low rail on the lower side of the light-emitting element 3313 – which causes the light-emitting element to emit light. Because the voltage on the gate of transistor 3308 (which, as explained above, is $(V_{Data} - |V_{th(3308)}|)$) is lower than the supply voltage V_{DD} , transistors 3307 and 3310 will provide negligible resistance to the current flow path while the resistance in the current flow path will thus be provided by transistor 3308 – which thus determines the specific amount of current that will flow through the light-emitting element 3313. As explained in Section VIII.C, this threshold-voltage compensation technique serves to insure that the same overdrive voltage is applied to each instance of

transistor 3308 across the various pixel circuits – so that any variability of the threshold voltage across the various instances of transistor 3308 are essentially eliminated; in this way, the same current flows through the various instances of the light-emitter 3313 – causing all of them to emit the same brightness of light (as explained in Section VIII.C and in Section VII.B.1).

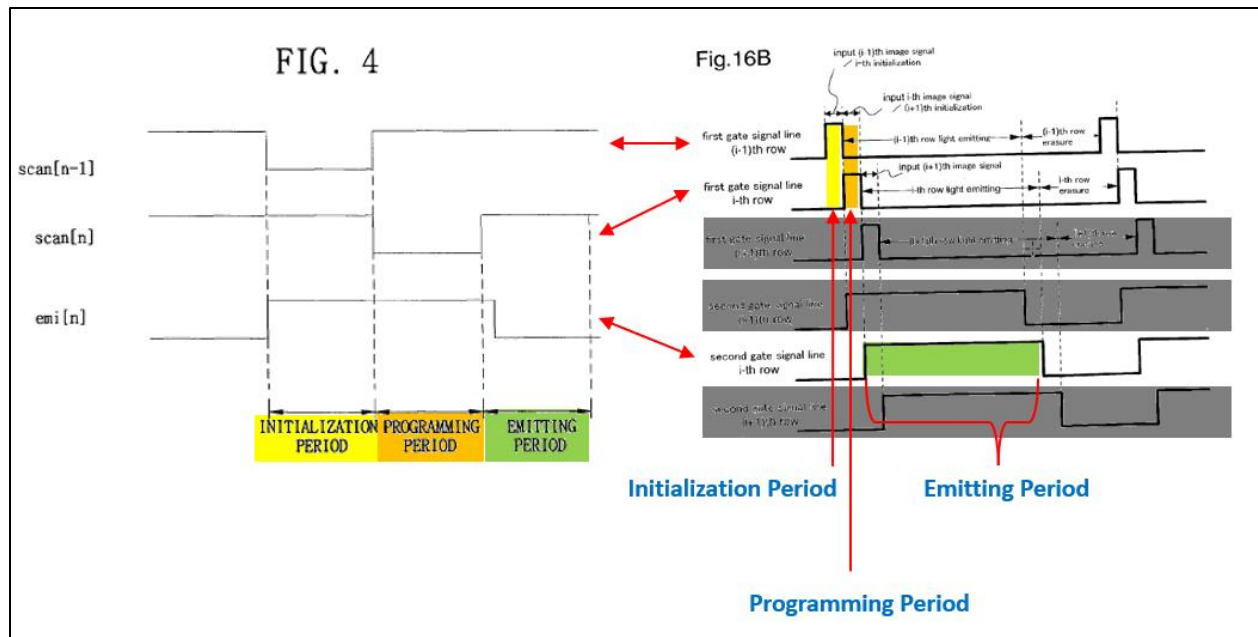
140. This (light-emitting) phase of operation is ended by turning off transistor 3307 and turning on transistors 3307 and 3309; this returns operation to the first phase, which is contained in Figure 33B and which was explained earlier. Here, the detail mentioned for later consideration in that earlier discussion of the first phase (the draining-away of the voltage on the node that is connected to the gate of transistor 3308) can now be explained. This node is drained so that the voltage imposed onto that node (during the second phase, described earlier) can be removed – in preparation for the next cycle of pixel-illumination. Kimura (at Figure 16B and [0658]-[0667]) refers to this operation as “erasure” – which is an apt description, as the second phase has programmed this node, and now that node must be de-programmed (i.e., erased) to make it ready for the next cycle of pixel illumination.

141. Although Kimura does not provide a dedicated input signal timing diagram of the signals that control the operation of Figure 33, there is no need to do so because Kimura previously provided input signal timing diagrams that are applicable to Figure 33, with little or no modification. As explained here and further

described at Kimura [0422]-[0429], one such timing diagram is contained in Figure 16B, which shows two signals (i.e., a “first gate signal line” and a “second gate signal line”). Each signal is shown for three adjacent rows (i.e., the (i-1)th row, the i-th row, and the (i+1)th row). *Id.*

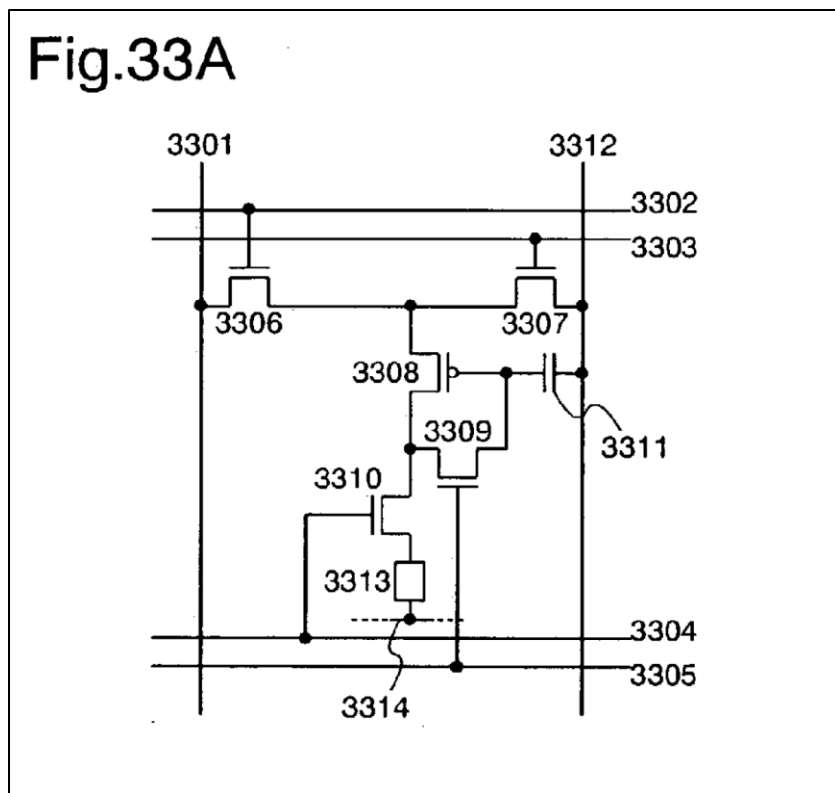


142. For subsequent reference, the mapping between the three operational phases in Kimura and the ‘599 patent are shown below, along with the control signal mappings. While Figure 16B uses an “active-high” signal scheme based on nMOS switching transistors, an active-low signal scheme for an all-PMOS implementation would look the same as Figure 4 of the ‘599 patent. See Section VII.A.2.



(Annotations added.) The yellow, orange, and green annotation boxes indicate the correspondence between the three periods identified in the '599 patent and the same periods as they appear in Kimura. The additional signals in Kimura Figure 16B that are not illustrated in Figure 4 of the '599 patent have been greyed out for simplicity, but a POSITA would understand that such signals would be present in the circuit associated with Figure 4. In Sections X.B and XII.B (claim 8), a modified version of Figure 33 is discussed that includes a dedicated reset transistor. Notably, the timing diagram of Figure 16B would directly apply to the modified embodiment discussed in Section XII.B.

143. Before concluding this section, it is worth revisiting the structural image of Figure 33 of Kimura.



144. Of the five transistors in the circuitry, four of them are nMOS transistors (3306, 3307, 3309, and 3310) while transistor 3308 is a pMOS transistor. As per the descriptions above, transistors 3306, 3307, 3309, and 3310 are used as simple on/off switches – while transistor 3308 is “programmed” via the charging-up method of the second phase of operation (explained above).

X. MOTIVATION TO MODIFY KIMURA

145. As will be explained below (in Section XII), all of the claims of the ‘599 patent may be found in Kimura – either explicitly, or in forms that require only modest (and obvious) modification. As all of the content required may be found in this single prior-art document, a POSITA would be motivated to modify Kimura to

the small degrees necessary – and would be able to do so without undue experimentation and a high expectation of success.

A. Modifying Kimura to an All-PMOS Implementation

146. As was explained in Section IX, in the Figure 33 embodiment of Kimura, the four transistors that are used as simple on/off switches are nMOS transistors, while the transistor that is “programmed” to provide threshold-voltage compensation is a pMOS transistor (for the reasons explained in the earlier discussion). As (as just mentioned) the nMOS transistors are used as simple switches, a POSITA would understand (for the reasons explained Section VII.A.2) that these nMOS transistors could readily be replaced with pMOS transistors; further, this would not require undue experimentation on the part of that POSITA – as the only operational change necessary would be to change the on/off polarity of the input signals – so that “on” would be low rather than high and “off” would be high rather than low.

147. Kimura itself teaches replacing nMOS transistors with pMOS transistors when they function as simple on/off switches. *See, e.g.*, EX1002, [0438] (“Note that a structure is used [in Figs. 3B-3D] in which the TFTs 304 and 306 are n-channel TFTs....**However, the TFTs 304 and 306 function as simple switching devices, and therefore any polarity may be used.**” (Emphasis added)); *id.*, [0396] (same for Figs. 1-2); *id.*, [0445] (same for Figs. 4B-4D); *id.*, [0649] (“All other TFTs

are only used as switching devices for performing only on and off control, and therefore may be of any polarity.”); *id.*, [0362] (showing an all-PMOS driver circuit in Fig. 22). Indeed, more than just generally teaching the interchangeability of nMOS and pMOS switching transistors, Kimura actually provides further details about using pMOS transistors – further details that apply to Figure 33.

148. For instance, Kimura discusses the replacement of the first or fourth transistor in Figure 33 with a pMOS device – and even provides an example circuit in Figure 34A, where the fourth transistor is a pMOS device. *See* EX1002, [0659] (“[T]he polarity of one of the TFTs [first or fourth transistors] may be made opposite to the polarity of the other TFT....”). It was well-known at the time to a POSITA that converting an nMOS transistor to the “opposite [] polarity” means using a pMOS transistor instead.

149. Kimura also discusses using a pMOS device for the fifth transistor (shown in Figure 37A) to enable “threshold voltage acquisition at higher speed.” EX1002, [0670]; *see also id.*, [0434] (“any polarity may be used” for series-connected switching transistor (labelled 1809 in Figure 18A and discussed in Figures 19A-C)); [0432] (using PMOS device in “close proximity” to the driving transistor “increase[s] the aperture ratio within a pixel, and [] reduce[s] the tendency for dispersion in TFT characteristics”).

150. In terms of the sixth transistor (i.e., the erasure/reset transistor discussed in the next section), Kimura teaches that “there are no particular limitations placed on the polarity of the [erasure/reset transistor].” EX1002, [0418]. The only switching transistor left unmentioned in the circuit of Kimura Figure 33 is the third transistor – and using a pMOS transistor would have been a simple design choice that would have been obvious to a POSITA.

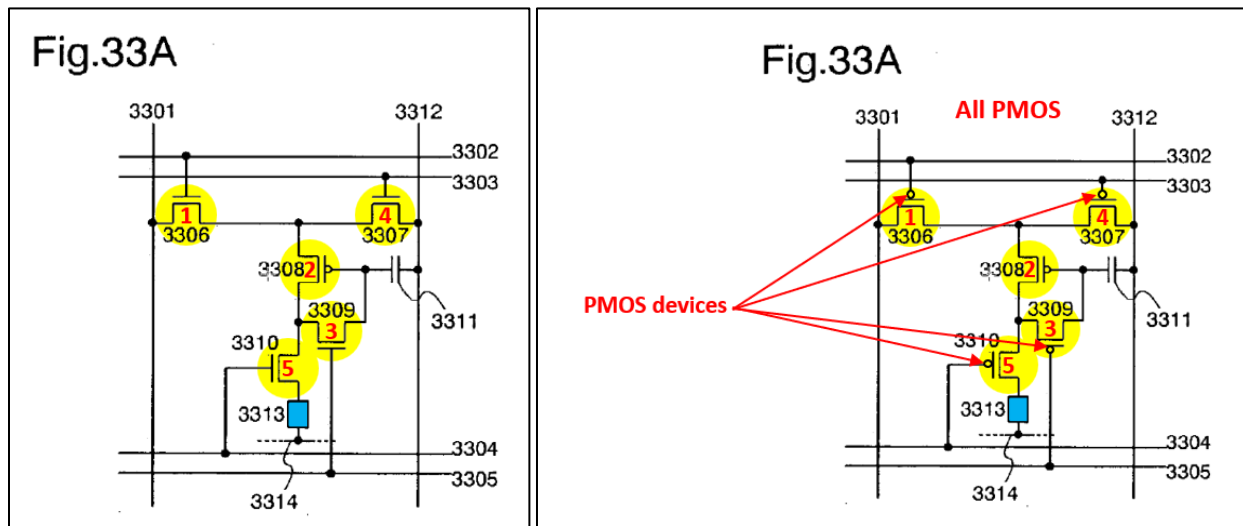
151. As also explained in Section VII.A.2, there is another reason a POSITA would actually be motivated to make such a change – since (as was explained in Section VII.A.2) this change would result in a single-transistor-species circuit – which would be simpler and less costly to manufacture. In fact, in another prior art patent explicitly acknowledges this issue:

Moreover, the example shown in FIG. 1 is constructed with the mixture of a P channel type TFT and an N channel type TFT, however, every TFT can be N channel type TFTs or all TFTs can be P channel type TFTs. However, in consideration that the voltage/current characteristics and threshold characteristics of the driving TFTs 110 are compensated by the compensating TFT 120, it is advantageous to construct these driving TFTs 110 and compensating TFTs 120 by the same process as the same type TFTs. Particularly, if both TFTs are formed in the same film forming process, the degree of characteristic similarities between both TFTs generally increases, so that it becomes possible to provide the transistor circuit 100 on the same Substrate with little or no variance in voltage/current characteristics and threshold characteristics. On the other hand, the resetting TFT 130 and the switching TFT 140 can be either a P channel type TFT or an N channel type TFT without being dependent on whether the driving TFT 110 is a P channel type TFT or N channel type TFT. However, it is often advantageous in manufacturing when all TFTs are of the same type.

EX1004 (U.S. Pat. 6,362,798 “Kimura ’798”) at 12:30-49.

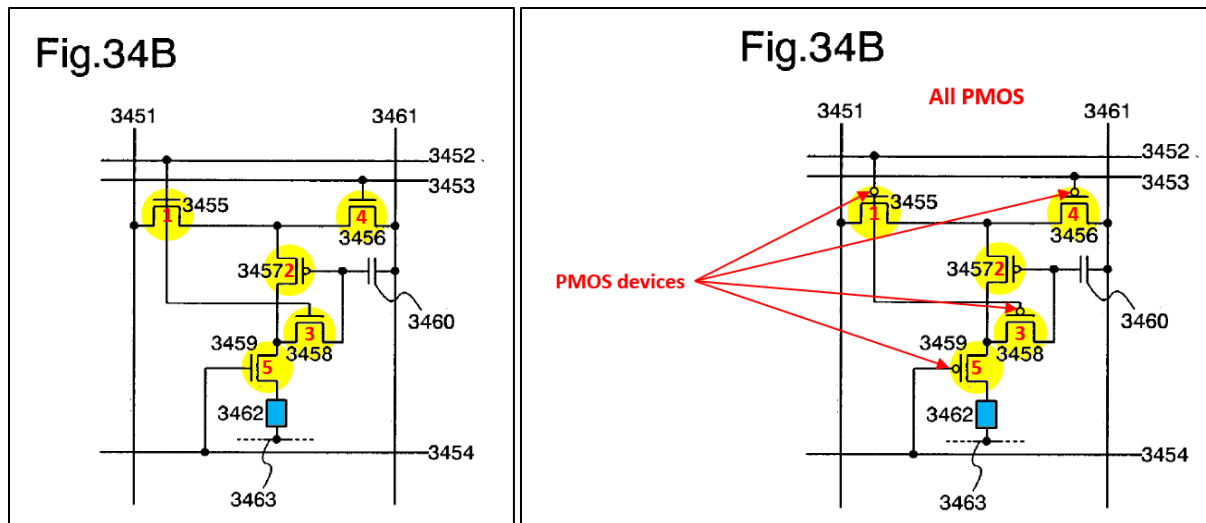
152. Thus, a POSITA would understand that such a modification would be straightforward – and that POSITA would even be clearly-motivated to do so.

The resulting all-PMOS version of Figure 33 is shown below with the original for reference.



Because the modifications are so minor, arrows have been added to the right-hand figure to show the addition of the small circles (indicating pMOS devices) that have been placed on transistors 1 and 3-5 to indicate that here these are pMOS transistors.

153. The “all-PMOS” version of Figure 33 is used for the patentability analysis of Section XII – and will include the label “All-PMOS” to avoid confusion. Reference will also be made to an “all-PMOS” version of Figure 34B as well – as is shown here.



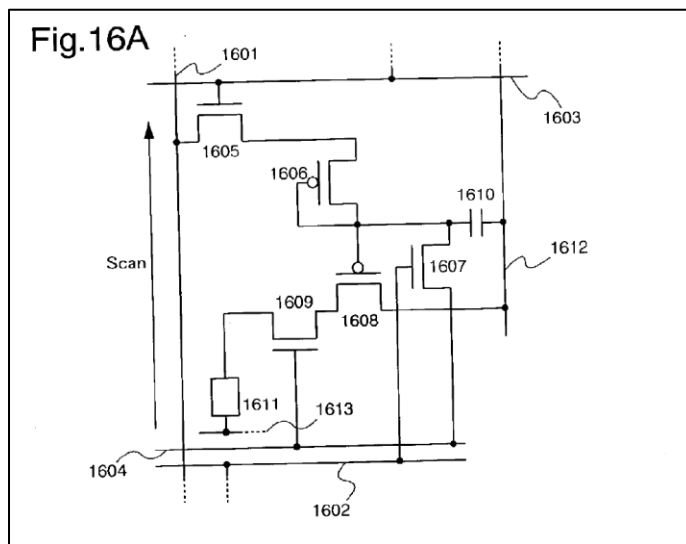
154. Given the express teachings of Kimura and the knowledge of a POSITA, there would have been far more than a reasonable likelihood of success in using an all-PMOS implementation. Indeed, such changes were both well-known in the art at the time, and well within the skill of a POSITA. While an all-PMOS version would require active-low signaling on the pMOS gates, this was also extremely well-known in the art – and would have been easy for a POSITA to implement.

B. Reset/Erase Transistor

155. As a general matter, various techniques for “resetting” a circuit have long been known in the field of electronics, and the concept is not limited to OLED driver circuits. Further, as explained in the discussion above with respect to Figure 33B, this particular embodiment in Kimura performs the reset/erase step – wherein the voltage on the node that connects to the gate of transistor 3308 is drained away – by draining this charge out of the circuit via the path that runs through the light-

emitting element 3313. However, as Kimura explicitly notes (at [0666]), this has the undesirable effect of causing a brief, spurious emission of light from the light-emitting element.

156. However (and as will be explained in further detail in Section XII), Kimura provides other embodiments in which a separate, dedicated transistor is included which serves solely to provide an independent drainage path (for the draining-away of the voltage that had been programmed onto the node that connects to the gate of transistor 3308). For example, in the embodiment depicted in Figure 16A, such a dedicated reset/eraser transistor (transistor 1607) is provided.



157. As can be seen, transistor 1607 serves one purpose – to drain the node that, in this depiction, is connected to that gate of transistor 1606.

158. Thus, a POSITA would have available, entirely from Kimura, the option of including a dedicated transistor for purpose of draining the voltage off of

a “programmed” node. Further, a POSITA would be motivated to add a transistor of the type shown in Figure 16 to the embodiment of Figure 33 – as a way of accomplishing the reset/erasure of the node connected to the gate of transistor 3308 without having the side-effect (explicitly acknowledged by Kimura) of a spurious, transient light emission from the light-emitting element 3313; in addition, a POSITA would understand (as per the discussion presented in Section X.A) that it would be a simple matter to use a pMOS transistor in the Figure 33 embodiment (rather than the nMOS transistor that is depicted in Figure 16A) – for the reason explained above in Section X.A. Finally, a POSITA would understand that (as also explained above) this inclusion would exact a price – in that by increasing the number of transistors in the circuitry of Figure 33, the complexity and size of this circuitry will be increased; however, the motivation provided by the ability to eliminate the aforementioned spurious light emission is sufficient for such a modification to be chosen.

XI. CLAIM TERMS

159. I have given the terms in the challenged claims their plain and ordinary meanings, as would have been understood by a person of ordinary skill in the art at the time of the alleged invention, taking into consideration the language of the claims, the specification, and the prosecution history of the '599 patent. I have

applied these understandings of the claim terms in my analysis and in forming my opinions where appropriate in this Declaration.

XII. UNPATENTABILITY ANALYSIS

160. For my analysis, I will begin with Claim 7 rather than Claim 1. Claim 1 uses a somewhat unusual (and confusing) scheme for numbering the transistors in the disclosed circuitry – wherein a “fifth transistor” and a “sixth transistor” are identified, but no “fourth transistor” is identified. In contrast, Claim 7 numbers the transistors in the normal order of “first transistor” to “fifth transistor” – making the analysis simpler to do and easier to explain; further, the remaining independent claims of the ‘599 patent (Claim 14, Claim 15, and Claim 17) use the same numbering scheme as does Claim 7. Thus, Claims 7 – 18 will be analyzed first – and then Claims 1 – 6 will be analyzed afterward.

A. Independent Claim 7

1. [Claim 7 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”

161. As an initial matter, I will be offering no opinion regarding whether or not the preamble of Claim 7 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting – and I have thus conducted my analysis using that assumption.

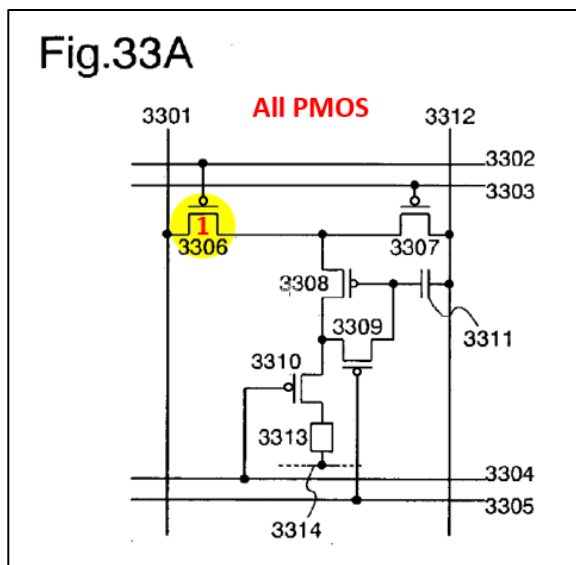
162. Kimura discloses the preamble of Claim 7. As is made clear by even a cursory examination of Kimura, Kimura involves circuitry for driving LED loads that are used in pixels; in fact, the word “pixel” appears 203 times in Kimura. The Abstract begins with the sentence: “Brightness irregularities that develop in a light emitting device due to isersion [sic] among pixels in the threshold values of TFTs used for supplying electric current to light emitting devices become obstacles to improved image quality of the light emitting device.” (Kimura at Abstract.) In addition, Kimura contains 44 figures – most of which (e.g., Figures 1 – 10, 16 – 23, and 32 – 40) depict transistor-level circuit diagrams of circuits that drive the light-emitting device of a pixel. This is further confirmed via examination of the textual parts of the specification of Kimura; e.g., at [0476] (where reference is made to “a plurality of pixels [] arranged in a matrix shape over a substrate.”); at [0035]; [0352], where the pixel circuits (including the electroluminescent element that emits light) form part of a “light emitting device,” such as a display; at [0001] (discussing “configuration of an active matrix **light emitting device**.”) (Emphasis added). In addition, Figure 31 depicts various displays/screens formed by the aforementioned pixels; Kimura also discloses that “[a]n **organic light emitting material**...can be used as the EL [electroluminescent] layer.” (Kimura at [0556] and [0557] (emphasis added)).

163. Thus, Kimura discloses the preamble of Claim 7 of the ‘599 patent.

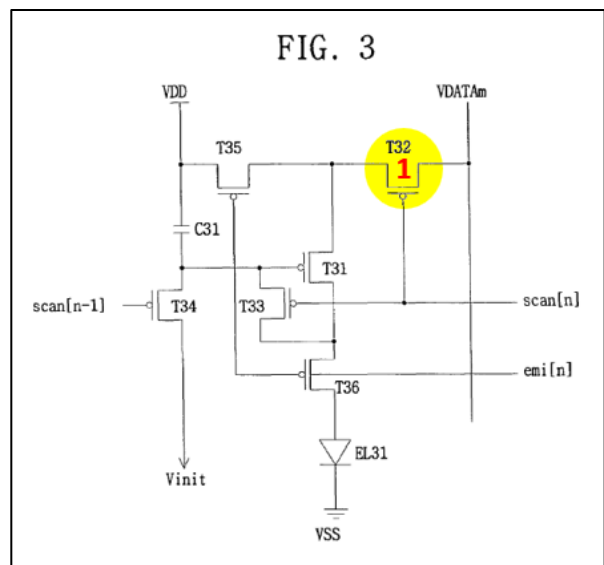
164. It should also be noted that while the circuitry disclosed in both the ‘599 patent and in Kimura is described as serving to drive a light-emitting device that is used in a pixel of, e.g., an LED display screen, there is nothing in particular about this transistor-based circuitry that restricts its use solely to this task. The problem identified by both the ‘599 patent and by Kimura (the difficulties caused by variations among the threshold voltages of different instances of the driver transistor among many such transistors across many identical circuits) is inherent in all transistor-based circuitry of this general type; the same circuitry (and the same approach to coping with the variability of the transistor threshold voltage across many instances of what would ideally be absolutely-identical transistors) could be used in any situation where the same problem occurs (and would be improved by the remedies described in the ‘599 patent and in Kimura).

2. [7a]: “a first transistor for delivering a data signal voltage in response to a current scan line signal;”

165. Kimura discloses this claim element of Claim 7 of the ‘599 patent; this is made readily-apparent by comparative examination of Figure 33 of Kimura and Figure 3 of the ‘599 patent.



Kimura

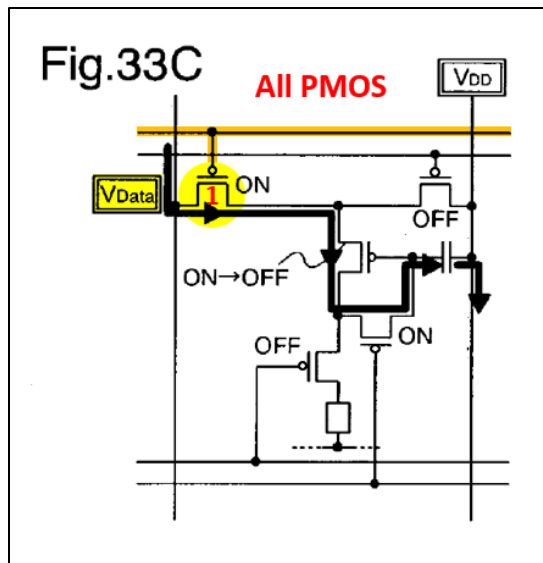


'599 Patent

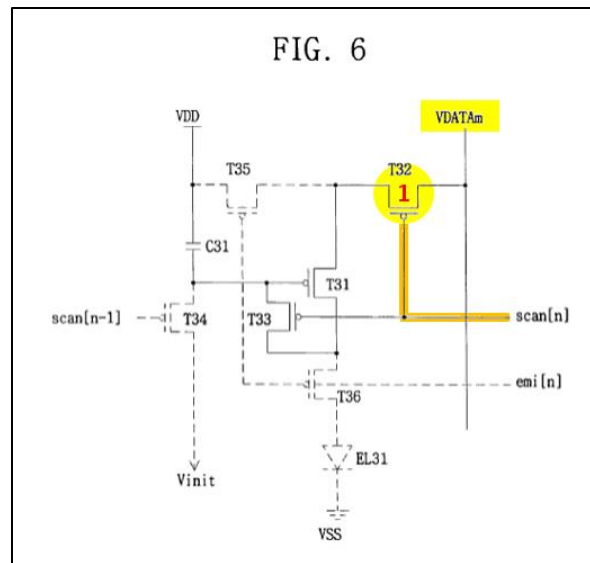
166. (Here, both figures have been annotated to ease the explanation below.)

Kimura identifies transistor 3306 as being a TFT; thus, this transistor (3306) in Kimura corresponds to transistor T32 of Claim 7 of the '599 patent – and therefore, transistor 3306 in Kimura provides the “first transistor” (identified as such in the '599 patent) of Claim 7 of the '599 patent.

167. Kimura explicitly describes the “data signal voltage” via labeling in Figure 33B and Figure 33C (the latter of which is depicted below); this corresponds to what is depicted in Figure 6 of the '599 patent.



Kimura



'599 Patent

168. (Annotations have been added to both figures, in yellow and orange; however, note that the black pathway-arrows depicted in Kimura's Figure 33C are in the original.) The "data signal voltage" in Kimura is V_{Data} – which corresponds to the "data signal voltage" $VDATAm$ in the '599 patent. Further, in both Kimura and the '599 patent, this data signal causes a current to flow through the first transistor when that first transistor is turned on; this is indicated by the black-arrow annotation provided by Kimura, and by the annotations added here to Figure 6 of the '599 patent. Finally, it should be noted that the differing location of the "first transistor" in the circuit diagrams of Kimura and the '599 patent is immaterial – as the depiction is merely topological (showing which elements are present and which element terminals are connected to other element terminals) rather than indicating some sort of locational requirement.

169. Claim element [7a] further stipulates that the first transistor delivers the data signal voltage “in response to a current scan line signal.” In both the ‘599 patent (the annotated Figure 6 above) and in Kimura (the annotated Figure 33C above), this claim element is denoted by the orange annotations that have been added; the line highlighted in orange runs (in both the ‘599 patent and Kimura) to the gate of the first transistor – and thus serves to control the operation of that transistor. In the ‘599 patent (and as shown above in Figure 6), the current signal scan line is named as “scan[n]” – which clearly indicates that this line serves the function as defined in this claim element of the ‘599 patent. While Figure 33 in Kimura does not include a label for this line, it is clear (and would be clear to a POSITA) that as this line connects to the gate of the first transistor of Kimura, it provides the “current scan line signal” in Kimura – as it controls the operation of that transistor. Kimura calls this signal the “first gate signal” (see Kimura at Figure 16 and Figure 17, which accompany the discussion at [0421] – [0429] – and of particular note, Kimura states that the first transistor is controlled by the “first gate signal line 1603” – and see also the discussion in Section IX regarding the use of the input-signal-timing diagram of Figure 16B with the embodiment of Figure 33). Further, the term “first gate signal” is used more than 80 times in Kimura, and is explained in the timing diagrams (such as Figure 16B); it is also clear from Figure 16B that, in Kimura, “i” is used as an indexing variable – so that the “i-th” row is the “current” scan line signal, while the

(i-1)th signal is the previous scan line signal and the (i+1)th signal is the subsequent scan line signal. This indexing variable “i” is identical to the indexing variable “n” in the ‘599 patent – and is used in the same way.

170. Kimura further explains (with reference to Figure 16B) that when “the first gate signal line 1603 of the i-th row is selected, the TFT 1605 turns on, and the image signal is input to the i-th row.” (Kimura at [0427].) In Kimura, the term “image signal” refers to the scan signal(s) (i.e. Kimura’s first gate signal) sent to display a particular image. In addition, Kimura explains that “a gate electrode of the first transistor is electrically connected to the first gate signal line.” (Kimura at [0158], [0176], [0194], [0211], [0230], and [0248].) Note also that when pMOS transistors are used instead of the nMOS transistors specified in Kimura, the current scan line signal of Kimura would be activated by pulling it from high to low voltage (rather than from low to high voltage). As described earlier, this is known in the art as “active low” signaling; this well-known concept was explained in Section VII.A, and was well-known to a POSITA at the relevant time.

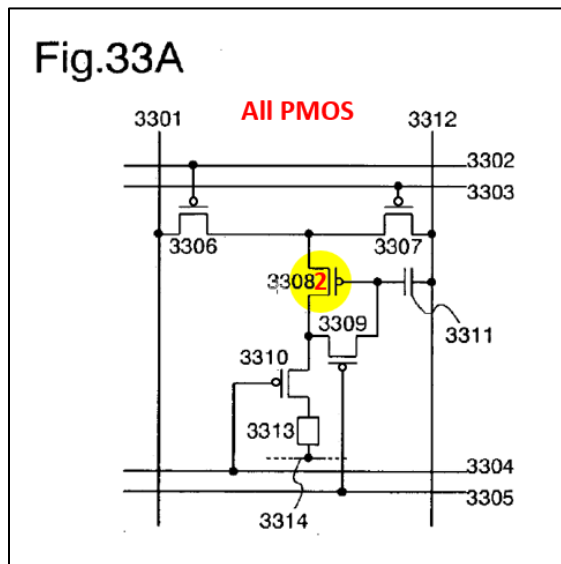
171. Thus, in total, Kimura discloses claim element [7a] of the ‘599 patent.

3. [7b]: “a second transistor for programming the data signal voltage and for generating a driving current in response to a programmed data signal when light is emitted;”

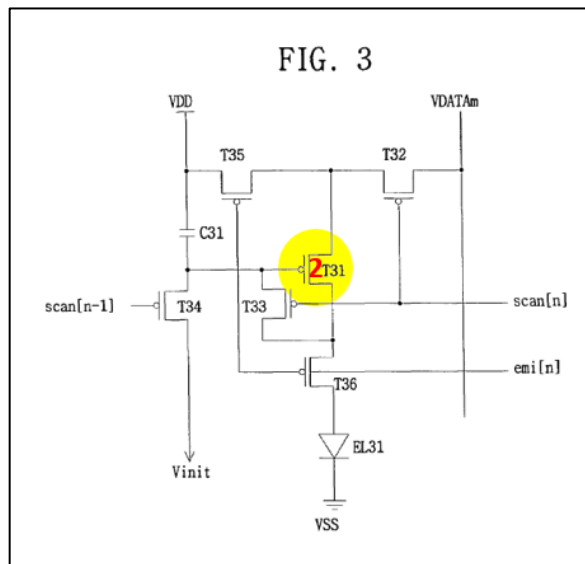
172. Kimura discloses this claim element of the ‘599 patent. This claim element describes the second transistor, and then two functionalities associated with

the operation of that second transistor; each of these three items will be considered in turn.

173. With regard to the second transistor, Kimura discloses this part of the claim element.



Kimura

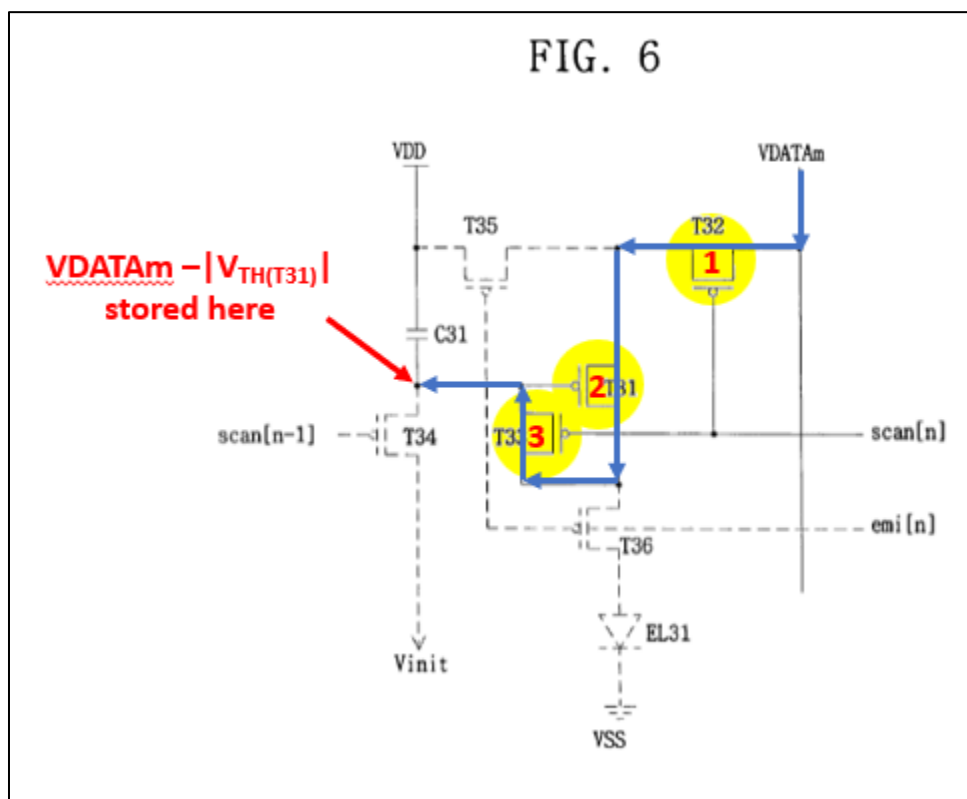


'599 Patent

174. As was detailed earlier, transistor T31 in the '599 patent is the “second transistor” in Claim 7. As shown in the annotated figure above, transistor 3308 in Kimura meets this description of a “second transistor” – since transistor 3308 is the same transistor at the same topological location in the same circuit; further, as will be shown below, this transistor serves the same functions that follow in this claim element – that is, “programming the data signal voltage”; and “generating a driving current in response to a programmed data signal when light is emitted.” In both the

claimed embodiment of the '599 patent and in Kimura Figure 33, the “second transistor” is the driving transistor for the circuit.

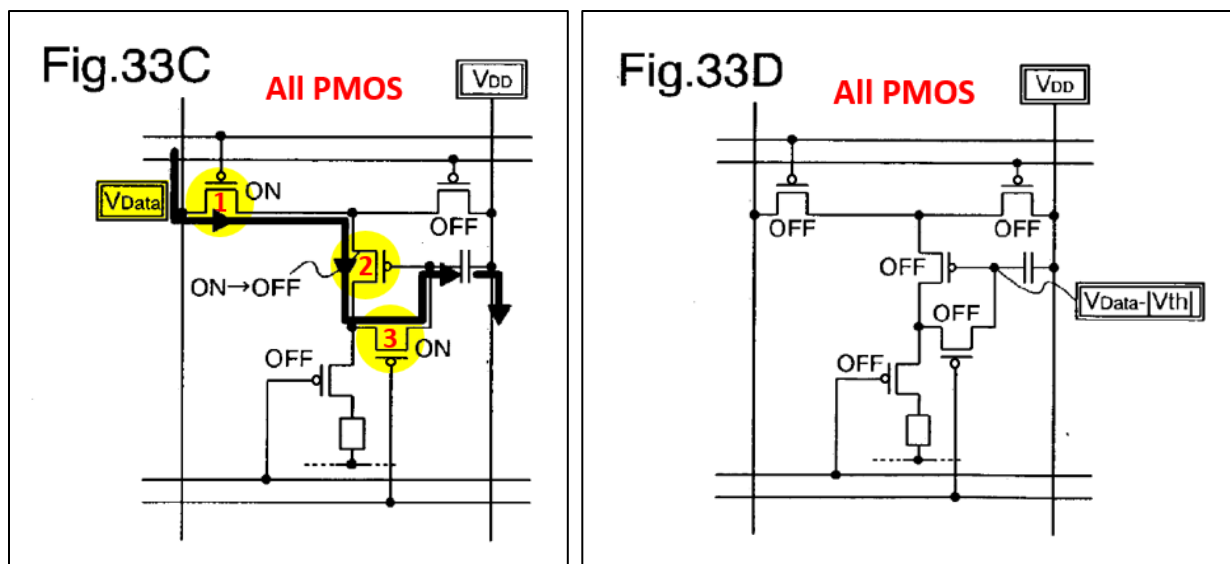
175. With regard to “programming the data signal voltage,” this functionality in the '599 patent was described earlier, in the detailed overview of the '599 patent – and can once again be demonstrated via an annotated version of Figure 6 from the '599 patent.



During the programming step, the scan[n] line is pulled low – which turns on transistors T32 and T33. Current flows through T32, T31, and T33, charging up the node that connects to the gate of transistor T31 – and this charging-up of this node (which is connected to capacitor C31) continues until the voltage on that node

reaches a value of $(V_{DATAm} - |V_{TH(T31)}|)$; at that point, transistor T31 turns off – and the voltage on that node has reached the endpoint of the programming step. When the programming step is ended by pulling the scan[n] line high, transistors T32 and T33 turn off – and the voltage on the node that connects to the gate of transistor T31 remains fixed at the aforementioned programmed level.

176. Kimura discloses the exact same operation using the same circuitry – which is readily-demonstrated via these annotated figures from Kimura.

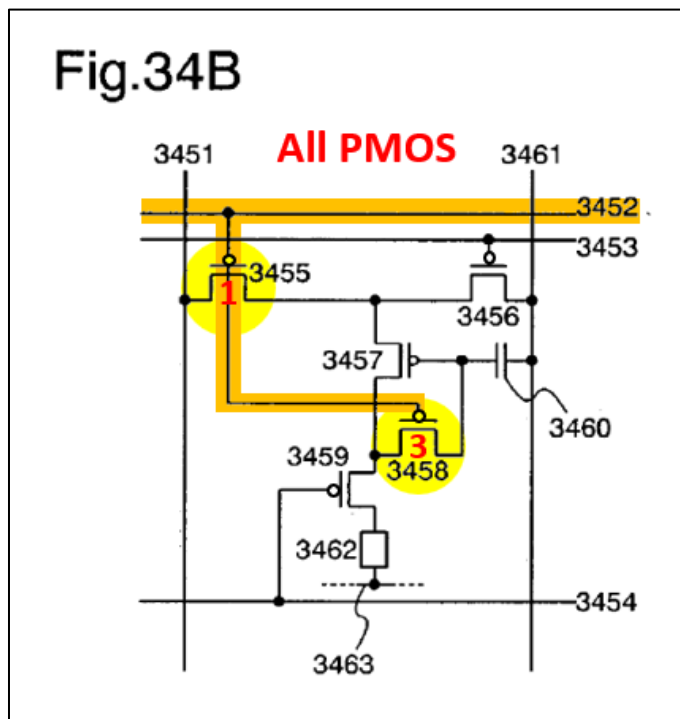


177. (Note again that the black arrows in Figure 33C, depicting a charge-flow path, is *not* an annotation that was added here – but appears in this figure in Kimura.) In Kimura, the gates of the “first transistor” (3306) and the “third transistor” (3309) are pulled low, turning those transistors on; this causes current to flow so as to charge up the node that connects to the gate of the “second transistor” (3308) – until the voltage on this node reaches a voltage of $(V_{Data} - |V_{TH(3308)}|)$; at

that point, the second transistor (3308) turns off, and the voltage on the node of the gate connected to this transistor remains at this level. The gates of the first transistor and the third transistor are then pulled back to high – turning those transistors off and ending the programming step, and leaving the aforementioned programmed voltage on the node connected to the gate of the second transistor at the programmed level. This operation, in both structure and functionality, is identical in the ‘599 patent and Kimura.

178. As can be seen in the figures presented above, in the ‘599 patent, a single line (the scan[n] line) is connected to the gate of the first transistor and the gate of the third transistor – so that these transistors will explicitly turn off-and-on together as the scan[n] line is pulled high or low. In contrast, in Figure 33 Kimura depicts separate lines (3302 and 3305) that connect to, respectively, the first transistor and the third transistor. However, it is readily-seen that the same circuit functionality as that of the ‘599 patent (using the scan[n] as just described) can be created in Kimura by simply controlling these two lines (3302 and 3305) in tandem; in fact, Kimura explicitly describes doing exactly that. Kimura explains that “the TFT 3306 [first transistor] and the TFT 3309 [third transistor] in FIG. 33A *are controlled to turn on and off at the same timing* [sic]. They can therefore be controlled by using the same gate signal line 3452, as shown in FIG. 34.B.” (Kimura at [0659] (emphasis added)). Further, as per the last sentence of this excerpt from

Kimura, Figure 34B of Kimura depicts an embodiment in which a single line is used to control the first transistor and the third transistor in tandem, by connecting to the gates of both of these transistors.

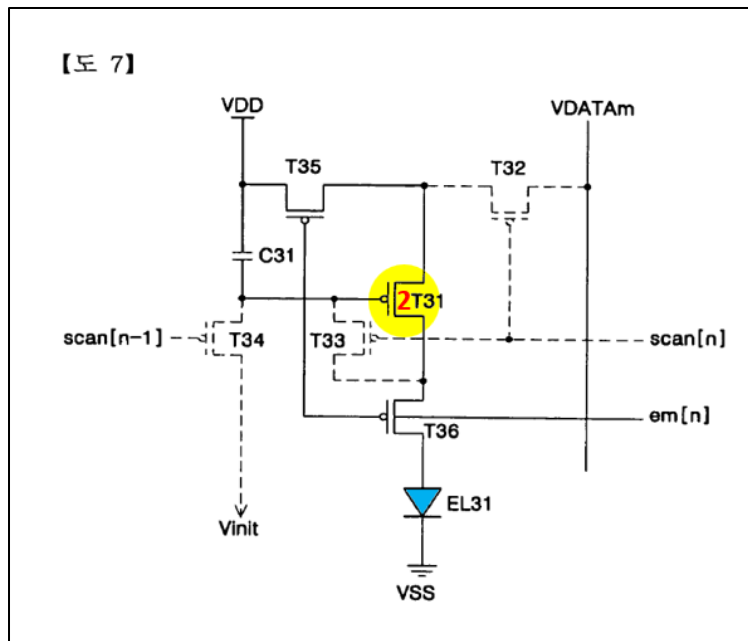


(This figure has been annotated to highlight the shared “current scan signal” line that connects to the gates of the first and third transistors.) In response to the signal on line 3452 (the “current scan line”), the first transistor (labeled 3455 in Figure 34B and 3306 in Figure 33) and the third transistor (labeled 3458 in Fig. 34 and 3309 in Figure 33) are turned on – and the programming of the data signal voltage onto the node which connects to the gate of the second transistor (labeled 3308 in Figure 33 and 3457 in Figure 34) is carried out as described above. Further, as Kimura explicitly discloses the use of a shared signal line (to the gates of the first transistor

and the third transistor,) it would have been obvious to a POSITA to use the shared signal of Figure 34 in the circuitry of Figure 33 – in particular, as a simple method of ensuring that what Kimura describes (as detailed above) as “the TFT 3306 [first transistor] and the TFT 3309 [third transistor] in FIG. 33A *are controlled to turn on and off at the same timing* [sic].” Kimura at [0659] (emphasis added). As also noted above, Kimura states: “They [the first transistor and the third transistor] can therefore be controlled by using the same gate signal line 3452, as shown in FIG. 34B.” Kimura at [0659] (emphasis added).

179. With regard to “generating a driving current in response to a programmed data signal when light is emitted,” this functionality in the ‘599 patent was also described earlier in the detailed overview of the ‘599 patent – and can once again be demonstrated via an annotated version of “Figure 7”¹⁴ from the ‘599 patent.

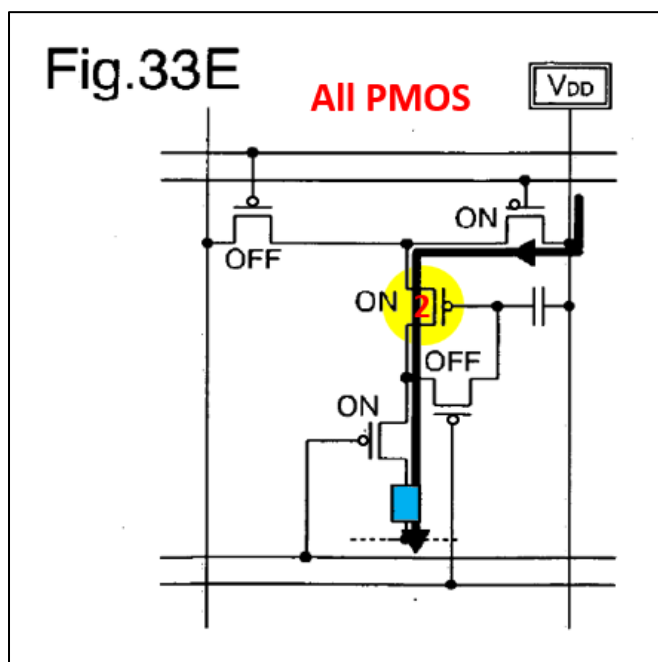
¹⁴ See the earlier discussion of the erroneous “Figure 7” in the ‘599 patent – and how the correct Figure 7 from the earlier Korean patent application is being used here to allow for a proper explanation of the teachings of the ‘599 patent.



The light-emission phase is initiated by pulling the emi[n] line low – which turns on the “fourth transistor” (T35) and the “fifth transistor” (T36). This creates a current path from the high voltage rail (VDD) to the low voltage rail (VSS), via the fourth transistor T35, the second transistor T31, the fifth transistor T36, and the light-emitting diode element EL31. As explained in Section VII.B, the light emitter is a light-emitting diode (i.e., an OLED or similar) – which emits light of a particular level of brightness that is a strong function of the forward-bias current flow that is being put through that light emitting element. The specific level of current is set by the voltages on the terminals of the second transistor T31 – which has been “programmed” (during the programming step) to output a current level that includes compensation for threshold voltage variations among the different T31 instances across numerous instantiations of the pixel circuit of Figure 3 – so that, despite these

threshold voltage variations, the same forward-bias current will flow through the emitter EL31, leading to the same pixel brightness across the various pixels of, e.g., a display.

180. Kimura discloses the same functionality using the same circuitry – as is readily-demonstrated via examination of an annotated version of Figure 33E from Kimura.



(Here, again, the black arrows depicting current flow are *not* an annotation – but appear in Figure 33E in Kimura.) During the light-emitting phase, the “fourth transistor” (3307) and the “fifth transistor” (3310) are turned on; as detailed above, the level of the current that flows down from VDD provides a forward-bias current that causes the light-emitting device 3313 to emit light, where the brightness of the emission is a direct function of the level of this forward-bias current. Here, once

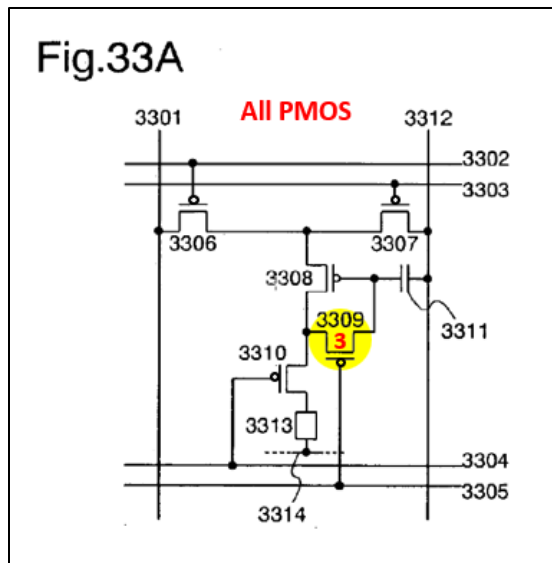
again, that current level is set by the voltages on the terminals of the second transistor 3308 – with the compensation approach that was described earlier serving to cause the same forward-bias current to be generated and provided to the light-emitting device, so that threshold voltage variations across many instances of the second transistor and the single-pixel circuitry are compensated-out; this results in the same forward-bias current being supplied to the different emitters, causing all such instances of light emission to have the same brightness.

181. In sum, Kimura discloses this claim element of Claim 7 of the ‘599 patent.

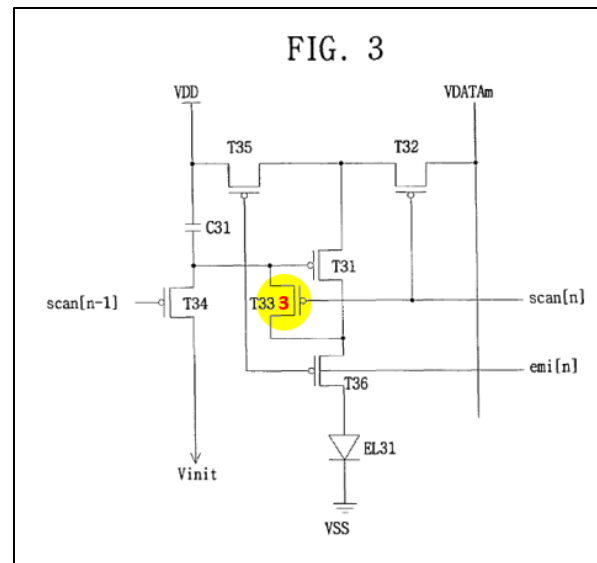
4. [7c]: “a third transistor for providing the data signal voltage for the second transistor in response to the current scan signal;”

182. Kimura discloses this claim element of the ‘599 patent. This claim element describes the third transistor, and then a functionality associated with the operation of that third transistor; each of these items will be considered in turn.

183. With regard to the third transistor, Kimura discloses this part of the claim element.



Kimura



'599 Patent

As was detailed earlier, the claimed “third transistor” is T33 in Fig. 3 from the ‘599 patent. As shown in the annotated figure above, transistor 3309 in Kimura meets this description of a “third transistor” – since transistor 3309 is the same transistor at the same location in the same circuit; further, as will be shown below, this transistor provides the same function that follows in this claim element – that is, “providing the data signal voltage for the second transistor in response to the current scan signal.”

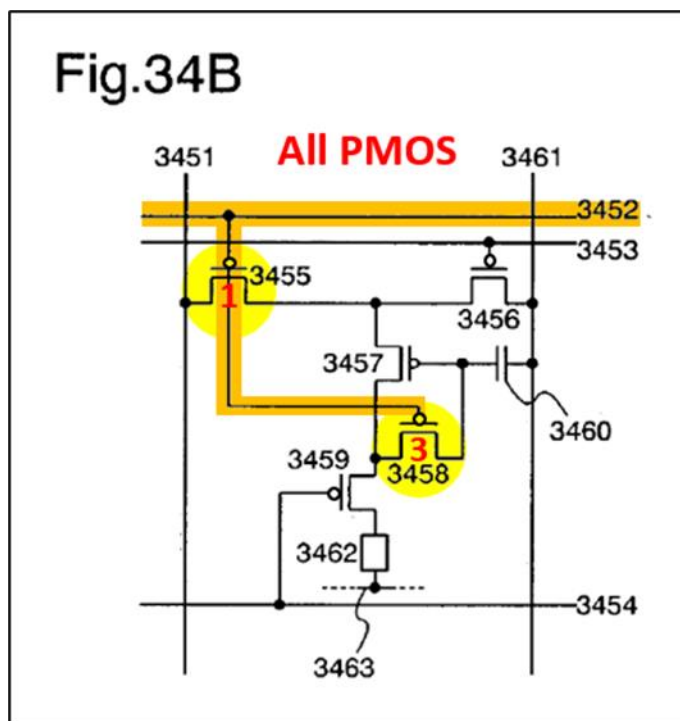
184. This functionality was already described in detail earlier – in both the detailed description of the ‘599 patent, and in the discussion of claim element 7[b] just above; further, this functionality refers specifically to the programming phase of the operation of the circuitry disclosed in both the ‘599 patent and in Kimura.

185. As was thusly detailed above, in both the ‘599 patent and Kimura, the “current scan signal”^{15,16} (the scan[n] line in the ‘599 patent and lines 3302 and 3305 in Figure 33 of Kimura) is turned on during the programming phase; this, among other things, turns on the third transistor – so that the “data signal voltage” (i.e., $V_{\text{Data}} - |V_{\text{TH}}|$) is created at the node that connects to the gate of the second transistor. Further, as was explained in the discussion above regarding claim element 7[b], as can be seen in the figures presented above, in the ‘599 patent, a single line (the scan[n] line) is connected to the gate of the first transistor and the gate of the third transistor – so that these transistors will explicitly turn off-and-on together as the scan[n] line is pulled high or low. In contrast, in Figure 33 Kimura depicts separate lines (3302 and 3305) that connect to, respectively, the first transistor and the third transistor. However, it is readily-seen that the same circuit functionality as that of the ‘599 patent (using the scan[n] as just described) can be created in Kimura by

¹⁵ Note again that, as discussed above with regard to claim element 7a, in Kimura, “i” is used as an indexing variable – so that the “i-th” row is the “current” scan line signal, while the (i-1)th signal is the previous scan line signal and the (i+1)th signal is the subsequent scan line signal. This indexing variable “i” is identical to the indexing variable “n” in the ‘599 patent – and is used in the same way.

¹⁶ Note that claim element 7c uses the term “current scan signal,” while claim element 7a uses the term “current scan line signal”; these two terms describe the same thing – and a POSITA would understand this.

simply controlling these two lines (3302 and 3305) in tandem; in fact, Kimura explicitly describes doing exactly that. Kimura explains that “the TFT 3306 [first transistor] and the TFT 3309 [third transistor] in FIG. 33A *are controlled to turn on and off at the same timing* [sic]. They can therefore be controlled by using the same gate signal line 3452, as shown in FIG. 34.B.” (Kimura at [0659] (emphasis added)). Further, as per the last sentence of this excerpt from Kimura, Figure 34B of Kimura depicts an embodiment in which a single line is used to control the first transistor and the third transistor in tandem, by connecting to the gates of both of these transistors.



(This figure has been annotated to highlight the shared “current scan signal” line that connects to the gates of the first and third transistors.) In response to the signal on

line 3452 (the “current scan line”), the first transistor (labeled 3455 in Figure 34B and 3306 in Figure 33) and the third transistor (labeled 3458 in Fig. 34 and 3309 in Figure 33) are turned on – and the programming of the data signal voltage onto the node which connects to the gate of the second transistor (labeled 3308 in Figure 33 and 3457 in Figure 34) is carried out as described above. Further, as Kimura explicitly discloses the use of a shared signal line (to the gates of the first transistor and the third transistor,) it would have been obvious to a POSITA to use the shared signal of Figure 34 the circuitry of Figure 33 – in particular, as a simple method of ensuring that what Kimura describes (as detailed above) as “the TFT 3306 [first transistor] and the TFT 3309 [third transistor] in FIG. 33A *are controlled to turn on and off at the same time.*” (Kimura at [0659]; emphasis added.) As also noted above, Kimura also states (as also noted above): “They [the first transistor and the third transistor] can therefore be controlled by using the same gate signal line 3452, as shown in FIG. 34.B.” Kimura at [0659] (emphasis added).

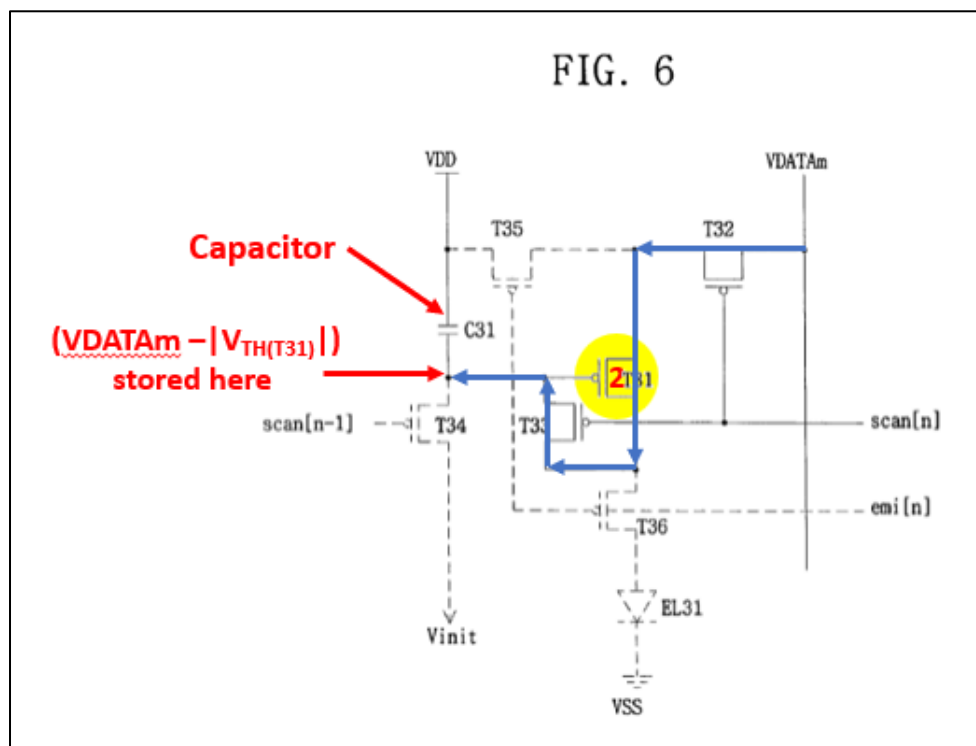
186. Thus, the recited “providing the data signal voltage for the second transistor” occurs in Kimura “in response to the current scan signal.” Further, as detailed earlier, this gate voltage on the gate of the second transistor is programmed by the circuitry – so that the same overdrive voltage will be applied to all instances of the second transistor across all instances of the pixel driver circuit, for the reason (equal brightness across all of the pixels) discussed earlier.

187. Thus, Kimura discloses this claim element of the '599 patent.

5. [7d]: “a capacitor for maintaining the data signal voltage programmed onto the second transistor;”

188. Kimura discloses this claim element of Claim 7 of the '599 patent.

189. This is best-explained by first examining an annotated version of Figure 6 which is the claimed embodiment of the '599 patent.



As has already been explained several times, during the programming step the first transistor (T32) and the third transistor (T33) are turned on, so that charge will flow through the first, second (T31), and third transistors, for the purpose of charging up the node connected to the gate of the second transistor – a process which continues until the voltage on this node reaches $(V_{DATAm} - |V_{TH(31)}|)$, at which point the second transistor T31 turns off, which fixed the voltage on this node at the

aforementioned voltage. The capacitor C31 provides DC isolation between this node and the supply voltage VDD – so that there can be no DC current between the VDD supply voltage and this node. Thus, as long as transistor T33 (and transistor T34) is off, there is no DC current path out of this node – and, by storing charge on the capacitor, the voltage on this node will self-maintain the programmed voltage (i.e., the “data signal voltage) for as long as this condition (T33 and T34 turned off) continues.¹⁷

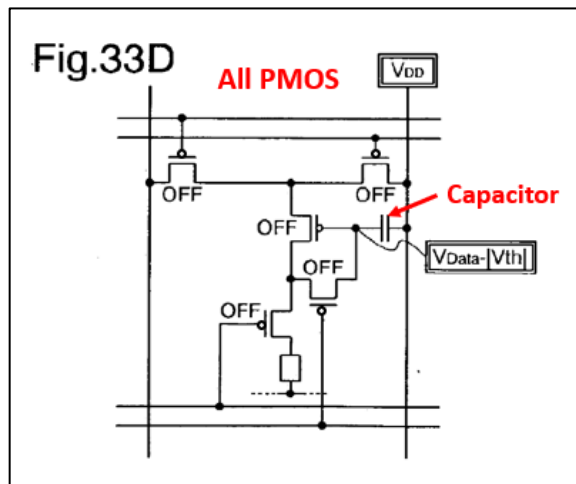
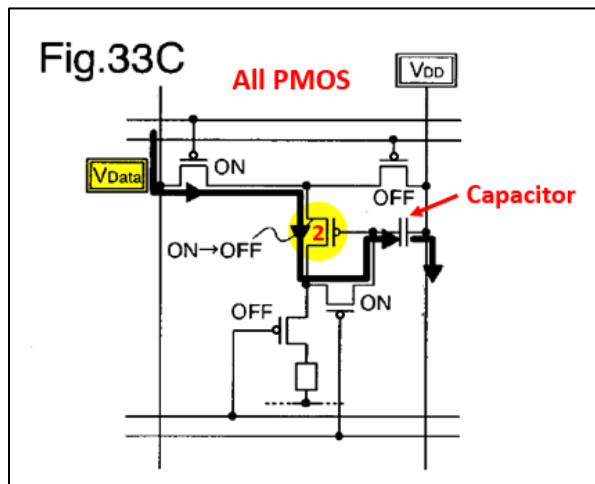
190. Kimura discloses a capacitor – which is in the circuit in the same place, and which serves the same function as that just described.

191. As an initial matter, it has already been explained above that the programming step in Kimura is identical to the one described in the ‘599 patent – in

¹⁷ In detail, all field-effect transistors (i.e., IGFETs) are subject to some leakage when in the off condition; however, one advantage of transistors of this type is that these leakage mechanisms are sufficiently slow, so that the time it will take for that leakage to matter is generally longer than the time required for the circuit functions to change the operating conditions of circuit operation. A contrast to this situation is provided by DRAM memory cells – which are designed to retain stored charge (and voltage) for extended periods of time; in that situation, a time period is set – after which the stored state (high or low) of each cell is read, and the stored state (high or low) is restored by re-injecting charge to each cell as necessary.

which a node (the gate node of the second transistor) is charged up, and then left isolated at a self-compensated voltage.

192. The capacitor in Kimura's circuitry is in the same place and serves the same function as does the capacitor C31 in the '599 patent.



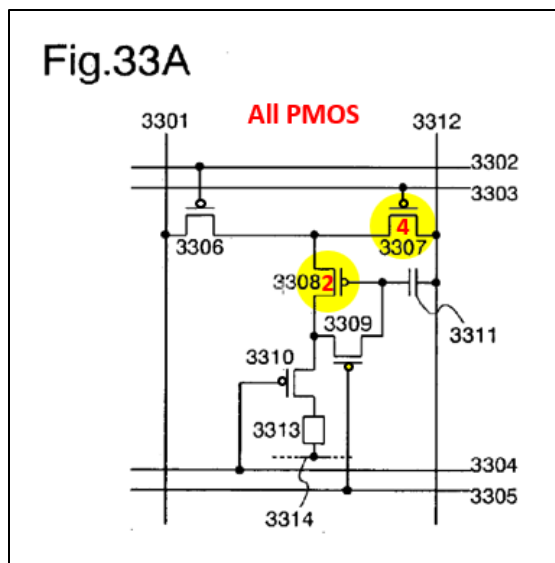
(Note again that the black arrows in Figure 33C are *not* annotations, but appears as-is in Kimura's figure.) The capacitor (labeled 3311 in Fig. 33A) isolates the node connected to the gate of the second transistor (3308) from the power supply line V_{DD} – just as is done in the '599 patent. Thus, as in the '599 patent, when the third transistor (3309) is turned off, the node connected to the gate of the second transistor (3308) is DC-isolated – and the voltage programmed there (the “data signal voltage”) will be maintained there.

193. Thus, Kimura discloses this claim element of Claim 7 of the '599 patent.

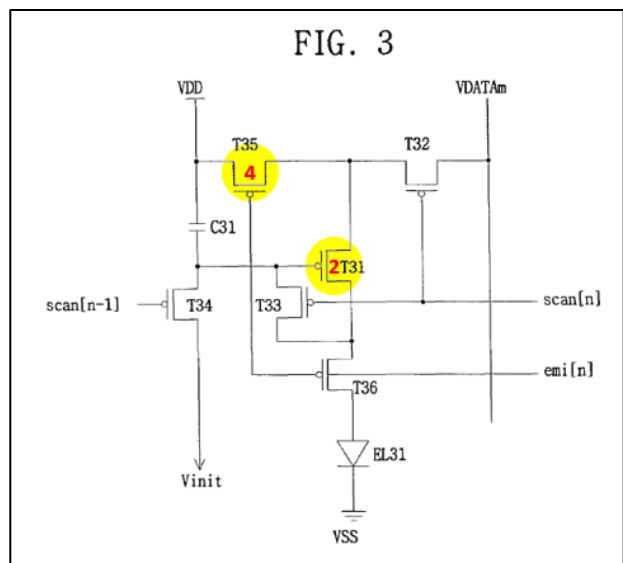
6. [7e]: “a fourth transistor for delivering a power supply voltage to the second transistor when the light is emitted;”

194. Kimura discloses this claim element of Claim 7 of the ‘599 patent.

195. As an initial matter, it has already been shown that the claimed “fourth transistor” maps to transistor T35 in the ‘599 patent. It has also been shown previously that in Kimura’s circuit, the “fourth transistor” is provided by transistor 3307 – as this is the same transistor in the same place in the same circuit as is described in the ‘599 patent.



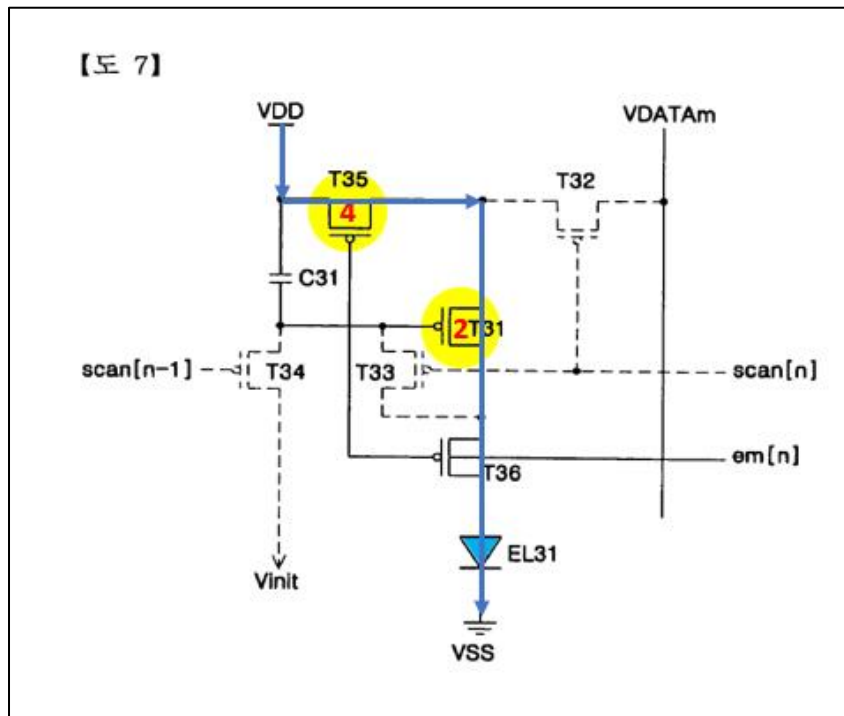
Kimura



‘599 Patent

196. The remainder of the claim element stipulates that the fourth transistor serves the function of “delivering a power supply voltage to the second transistor when the light is emitted.” This occurs during the emission step of circuit operation

– the details of which were already described earlier; this is readily-explained via an annotated version of Figure 7 of the ‘599 patent.¹⁸

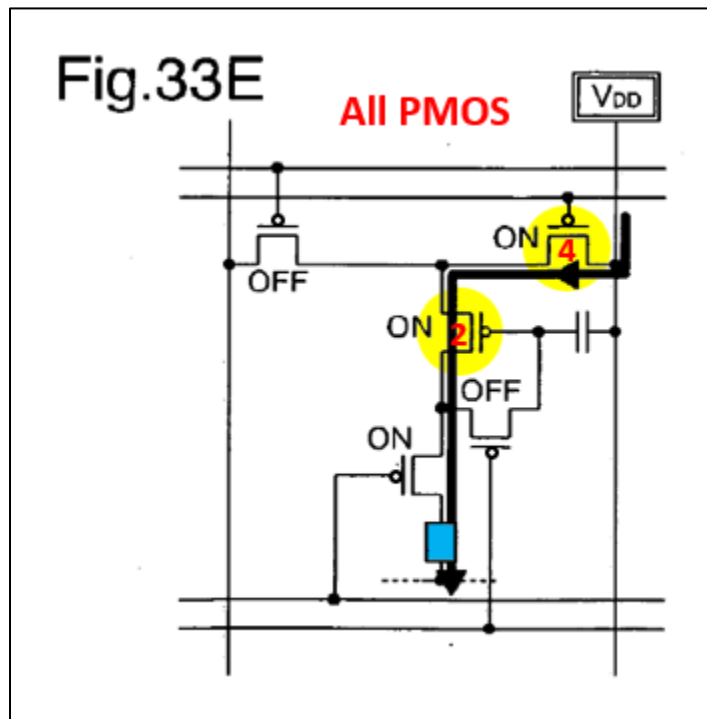


The emission step is induced by pulling the emi[n] line low – and turning on the fourth transistor (T35) and the fifth transistor (T36); in this way, a current path is provided from the high rail (VDD) to the low rail (VSS) – and a forward-bias current flows through the light-emitting element EL31, inducing it to emit light. In particular, the fourth transistor, when turned on, enters a state of negligible resistance – and thus, the VDD voltage appears on both sides (source and drain) of the fourth transistor, and thus this voltage appears on the node between the fourth transistor

¹⁸ See again the discussion of the problems with “Figure 7” as it exists in the ‘599 patent.

and the second transistor. Therefore, the fourth transistor delivers a power supply voltage to the second transistor when the entire current-flow path is activated during the emission step.

197. Kimura's circuitry operates in the same manner.



(Note once again that the black arrows in this figure are not annotations – but appears as-is in this figure in Kimura.) As Kimura explains, “[t]he TFTs 3307 [fourth transistor] and 3310 [fifth transistor] then turn on. The electric potential of a source region of the TFT 3308 [second transistor] increases from V_{Data} to VDD as the TFT 3307 [fourth transistor] turns on.” (Kimura at [0656].) Both the general operation during the emitting step *and* the specific detail of the high rail voltage VDD

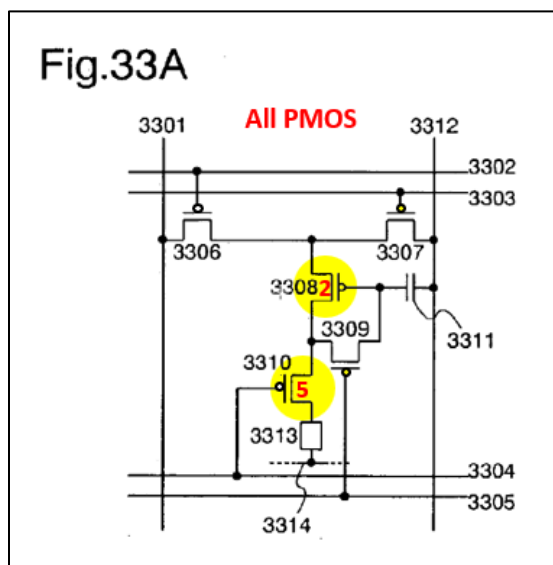
appearing at the node between the fourth transistor and the second transistor appear in Kimura exactly as they appear in the '599 patent.

198. Therefore, Kimura discloses this claim element of Claim 7 of the '599 patent.

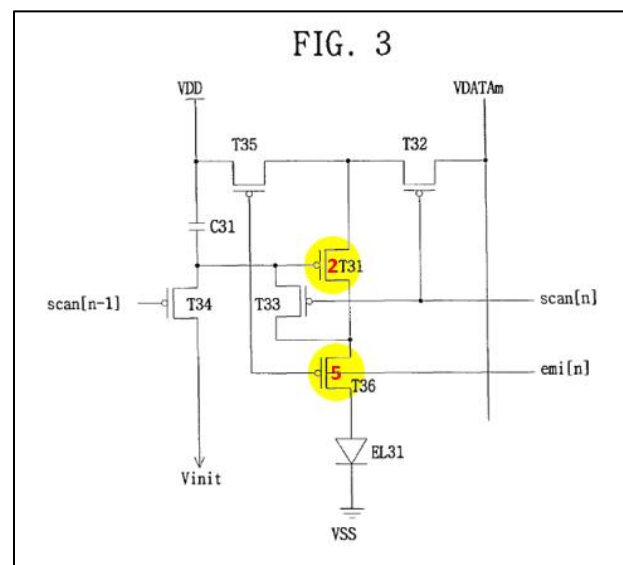
7. [7f]: “a fifth transistor for delivering the driving current, provided from the second transistor, in response to the data signal voltage when the light is emitted;”

199. Kimura discloses this claim element of Claim 7 of the '599 patent.

200. As an initial matter, as was explained earlier, the claimed “fifth transistor” maps to the transistor T36 in the claim embodiment of the '599 patent. As also shown earlier, transistor 3310 provides the fifth transistor in Kimura – as it is the same transistor, located in the same place in the circuit, serving the same function.

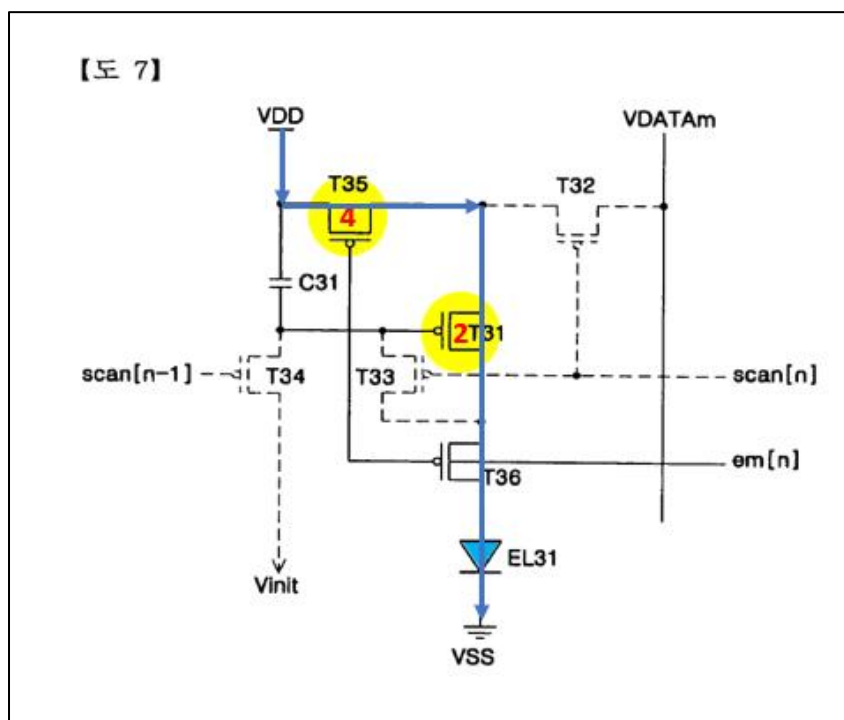


Kimura



'599 Patent

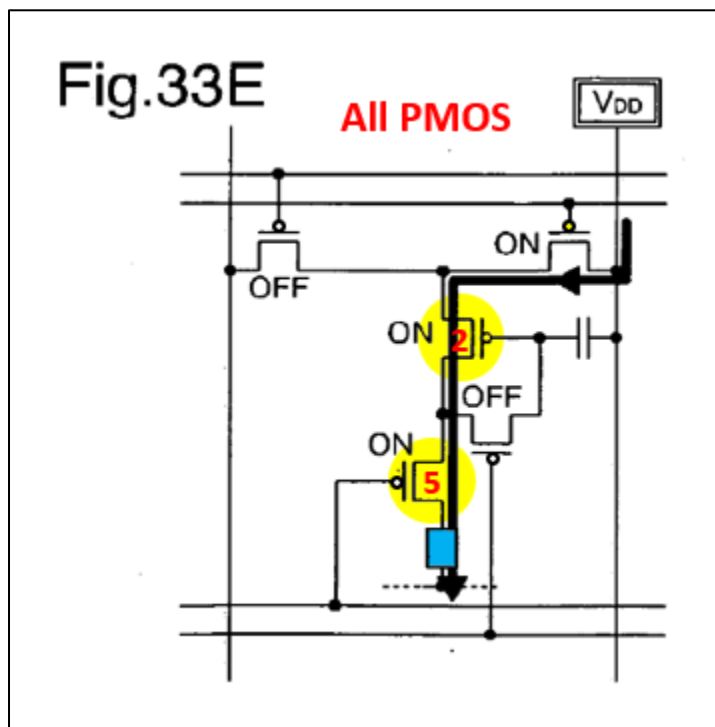
201. The claim element describes the functionality of that fifth transistor as: “delivering the driving current, provided from the second transistor, in response to the data signal voltage when the light is emitted.” As described in the detailed overview of the ‘599 patent, and as repeated more than once above, “when the light is emitted” refers to the emitting step of the operation of the circuitry described in the ‘599 patent – as detailed in an annotated Figure 7 from the ‘599 patent.



As detailed just above, by turning on the fourth transistor (T35), the voltage VDD is at the node between the fourth transistor and the second transistor (T31); the current that will be output (into the current flow path) by the second transistor (T31) will be set by the gate voltage that has been programmed onto the gate of transistor T31 – with that gate voltage being (as described earlier) the “data signal voltage.” With

the fifth transistor (T36) also turned on during the emitting step, that current will be passed transparently (i.e., unchanged) through the fifth transistor – and that current will pass through the light-emitter EL31 at that current level.

202. As detailed earlier, the Kimura's circuitry provides an emitting step that is identical (in both structure and function) to the emitting step of the '599 patent.



In the same way as was detailed just above for the emitting step of the '599 patent, in Kimura, by turning on the fourth transistor (3307), the voltage V_{DD} is provided at the node between the fourth transistor (3307) and the second transistor (3308); the current that will be output (into the current flow path) by the second transistor (3308) will be set by the gate voltage that has been programmed onto the gate of transistor 3308 – with that gate voltage being (as described earlier) the “data signal voltage.”

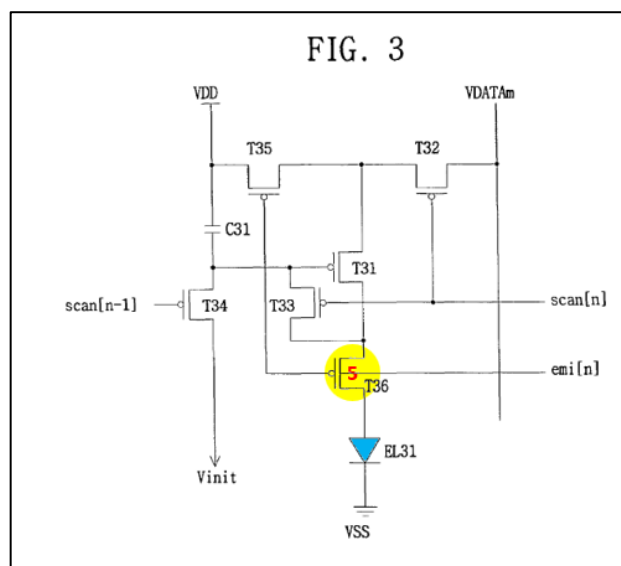
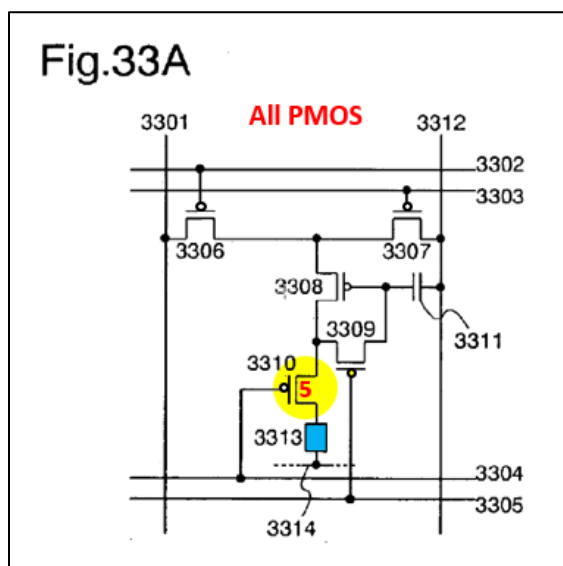
With the fifth transistor (3310) also turned on during the emitting step, that current will be passed transparently (i.e., with negligible change) through the fifth transistor (which is connected in series with the second transistor) – and that current will pass through the light-emitter 3313 at that current level. Thus, the driving current is “in response to the data signal voltage” because that voltage is stored on the node (using the capacitor) that controls the gate of the second transistor.

203. Thus, Kimura discloses this claim element of Claim 7 of the ‘599 patent.

8. [7g]: “an electroluminescent element for emitting light corresponding to the driving current delivered through the fifth transistor”

204. Kimura discloses this claim element of Claim 7 of the ‘599 patent.

205. As an initial matter, both the ‘599 patent and Kimura disclose “an electroluminescent element for emitting light.”



As mentioned several times above, this is specified in the ‘599 patent as element EL31, while in Kimura this is specified as element 3313. Kimura further states that “electric current flows in the EL device 3313 to cause it to emit light” (Kimura at [0656], and further explains that “EL” refers to “electroluminescent.” (Kimura at [0002].)

206. As was also explained above, the light-emitting element (EL31 in the ‘599 patent and 3313 in Kimura) emits light during what the ‘599 patent refers to as the light-emitting step of operation. As has been detailed more than once above, the light-emitting step in the ‘599 patent and the light-emitting step in Kimura are identical in both structure and function. As also explained earlier, the fifth transistor specified in the ‘599 patent (T36) is provided by transistor 3310 in Kimura – and both cases of the “fifth transistor” are annotated in the figures above. As was explained in the previous section, the fifth transistor (in both the ‘599 patent and Kimura) serves to transparently pass the driving current provided by the second transistor to the light-emitting element so that it can emit light. Thus, in Kimura, the light-emitting element receives the driving current that is delivered to it through the fifth transistor. Further, as was explained in Section VII.B, the amount of light that is emitted by an LED is a function of the amount of current that is flowing through it; therefore, the LED in Kimura emits an amount of light that “correspond[s] to the driving current delivered through the fifth transistor.”

207. Thus, Kimura discloses this claim element of Claim 7 of the ‘599 patent.

9. [7h]: “wherein the third transistor connects the second transistor in the form of a diode in response to the current scan signal so that the second transistor detects and compensates its threshold voltage deviation in itself.”

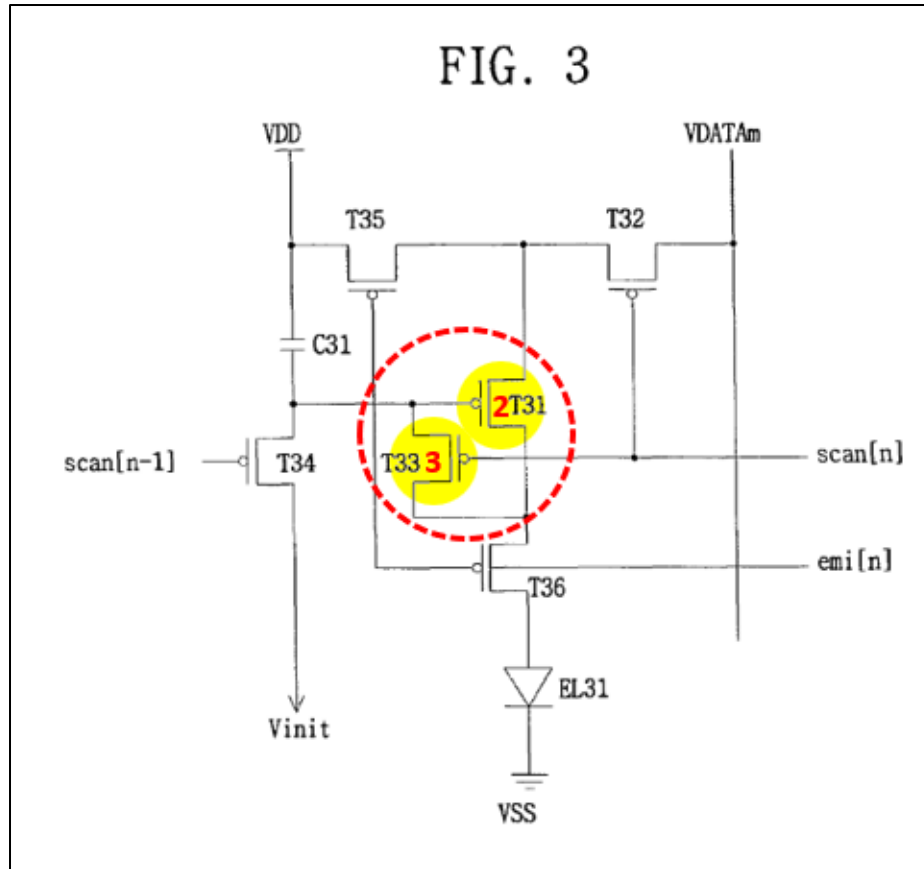
208. Kimura discloses this claim element of Claim 7 of the ‘599 patent.

209. As an initial matter, to connect a transistor “in the form of a diode” is something that is well-known in the art – and refers to a configuration of a field-effect transistor¹⁹ in which the gate of the transistor is directly connected to either the source or the drain of that same transistor; this was already explained earlier, in Section VII.A.6.

210. As a further initial matter, this claim element actually involves the details of the programming step described in the ‘599 patent – which was explained in the detailed overview of the ‘599 patent, as well as earlier in this evaluation of Claim 7.

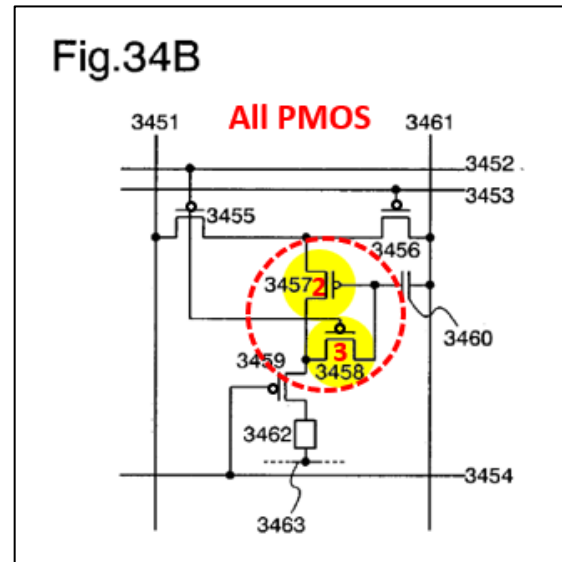
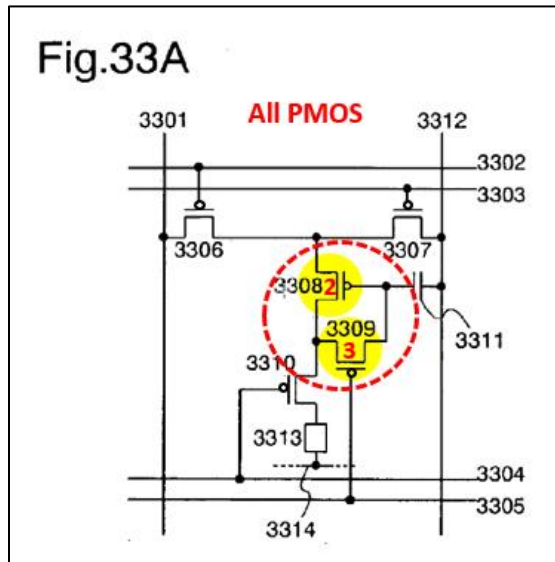
211. In terms of the first part of this claim element “wherein the third transistor connects the second transistor in the form of a diode,” this is a structure that is in the circuit depicted in Figure 3 of the ‘599 patent.

¹⁹ For completeness, it should be noted that other types of transistors (such as the bipolar transistor) can also be connected in the form of a diode.



As per the annotations added to Figure 3, the third transistor (T33) is connected to the second transistor (T31) in a configuration such that, when the third transistor T33 is turned on – and thus is in a state of negligible resistance – it acts as a connection that “connects the second transistor in the form of a diode.” This occurs when the third transistor is turned on; as the third transistor is turned on by pulling the scan[n] line to low, this diode-connected state for transistor T31 is created by turning on transistor T33 – and thus, this diode-connected state is created “in response to the current scan signal.”

212. Kimura also discloses this part of this claim element. As explained earlier, Kimura's circuitry has the same structure and functionality as does the circuitry of the '599 patent – and thus also discloses the transistor configuration that was just described in the '599 patent.



As can be readily seen in these annotated figures from Kimura, the third transistor (3309 in Figure 33A and 3458 in Figure 34B) is connected to the second transistor (3308 in Figure 33A and 3457 in Figure 34B) in the manner just described with respect to the '599 patent – that is, the third transistor is configured so that when it is turned on, it will provide a connection that will cause the second transistor to be connected in the form of a diode. As in the '599 patent, this is achieved by pulling the gate voltage on the third transistor to low – and as was explained earlier, this occurs when Kimura's equivalent of the current scan signal is pulled low. As Kimura explains, “(“the TFT 3309 [third transistor]...turn[s] on, and the TFT3308

thus behaves as a diode connected TFT.”) (Kimura at [0655].) The second transistor (3308 in Fig. 33 and 3457 in Fig. 34B) is in the form of a diode only when the third transistor (3309 in Fig. 33 and 3458 in Fig. 34) is activated by the control signal on its gate (the “current scan signal”). See Kimura, Figs. 33C, 33D, and 34B.

213. The final part of the claim element (“so that the second transistor detects and compensates its threshold voltage deviation in itself”) is a detail of the programming step – one that was explained in detail in the detailed overview of the ’599 patent presented earlier, and earlier in this analysis of Claim 7. There, it was shown that this part of the claim element is also present in Kimura.

214. Thus, Kimura discloses this claim element of Claim 7 of the ’599 patent.

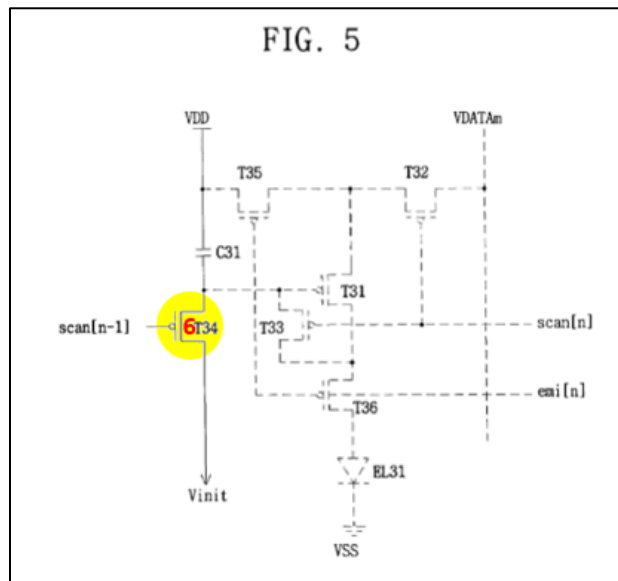
B. Claim 8

215. Claim 8 depends from Claim 7; as an initial matter, it was shown above that Kimura renders Claim 7 obvious.

216. With regard to Claim 8, this dependent claim requires “a sixth initialization transistor for discharging the data signal voltage stored in the capacitor in response to a scan signal just before the current scan signal upon initialization.” As will be shown below, Kimura renders this claim limitation obvious.

217. Before describing Kimura's circuitry and its operation, it is necessary to review the claimed embodiment of the '599 patent – and how Claim 8 appears there.

218. The “sixth transistor” in the claimed embodiment of the ’599 patent is transistor T34 as shown in Fig. 5 below.



The “sixth transistor” in the claimed embodiment of the ’599 patent is transistor T34, as shown in this annotated version of Figure 5 of the ’599 patent.

219. The '599 patent describes the purpose and operation of sixth transistor T34 at 7:15-27. The sixth transistor (T34) is used during what the '599 patent calls an "initialization operation" during which the control signals for the first, third, fourth, and fifth transistors are held high, so that these four transistors are off. ('599 patent at 7:15-17.) The purpose of the initialization step is to "clear" the programming voltage that had been created at the node connected to the gate of the

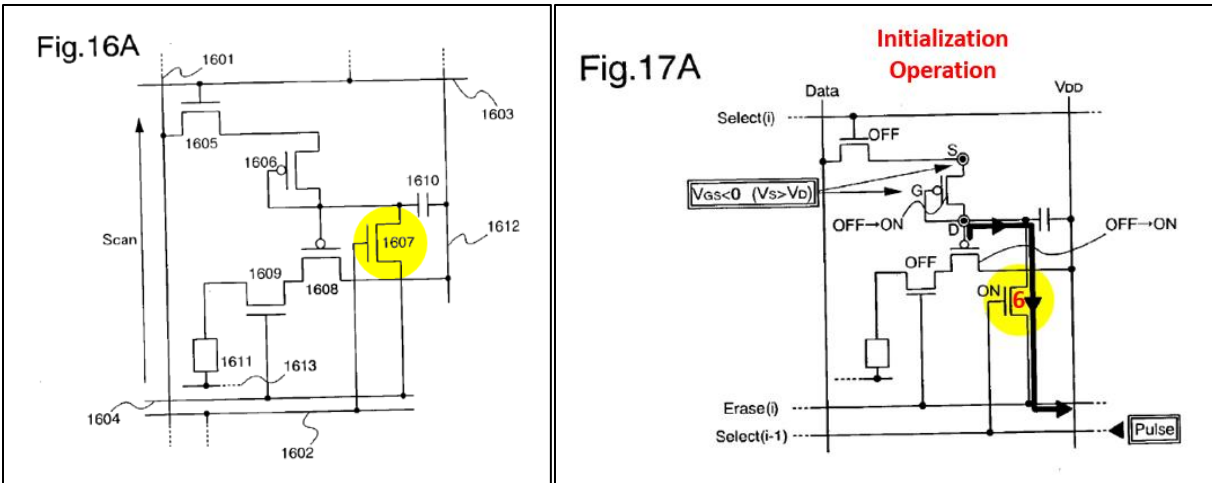
second transistor (T32) during the programming step of the just-executed sequence that leads to selected pixels being turned on (via light be induced to be produced by the light-emitting element EL31) during the emission step. As can be seen via examination of Figure 5 of the '599 patent, this is readily-accomplished by pulling the gate of the sixth transistor (T34) low – so that this transistor turns on, and allows the voltage on the aforementioned node (which had been created by storing charge on the capacitor C31) to drain away (i.e., discharge) through T34 to the low-voltage rail Vinit; in this way, the programming that was applied to this node (so as to program the gate voltage to be used by the second transistor (T31)) is removed – this node has now been pulled low (so that, at the end of the step, transistor T31 is turned on – but with transistors one, three, four, and five turned off, no current flows through it), and is thus ready for programming during the next round of pixel-illumination. Further, the scan signal from the prior (rather than the upcoming – now “current”) round of pixel illumination is still active and available at this point – and thus is used to choose whether or not to turn on T34 and perform this discharge operation; in this way, only instances where this node was charged up (in the prior round of pixel illumination) are discharged.

220. Thus, the sixth transistor performs the discharge function “in response to a scan signal just before the current scan signal upon initialization.” See '599, 7:6-8; 7:15-27.

221. With regard to Kimura, Kimura discloses that the fifth transistor in Figure 33 “can also be used as an erasure²⁰ [transistor]” -which, in the manner detailed above (with respect to the ‘599 patent), serves to discharge the node that connects to the gate of the second transistor (3308) by draining off the charge stored on the capacitor (3311) for this purpose. (Kimura at [0658].) While this approach has its benefits (i.e., by using the LED circuit path as the node-discharge path, via turning on the third transistor and fifth transistor to perform this function – and thus allowing the circuitry to have one less transistor), it also has its downsides – principally that during this initialization, the transient discharge current flows through the light emitting element – causing a transient-but-undesirable emission of light from the light-emitting device (3313). *See* Kimura, Fig. 33B; [0655]; [0658]; [0666].

222. However, Kimura discloses other embodiments where a separate-and-independent discharging (i.e., “erasure”) transistor is provided in the disclosed circuitry.

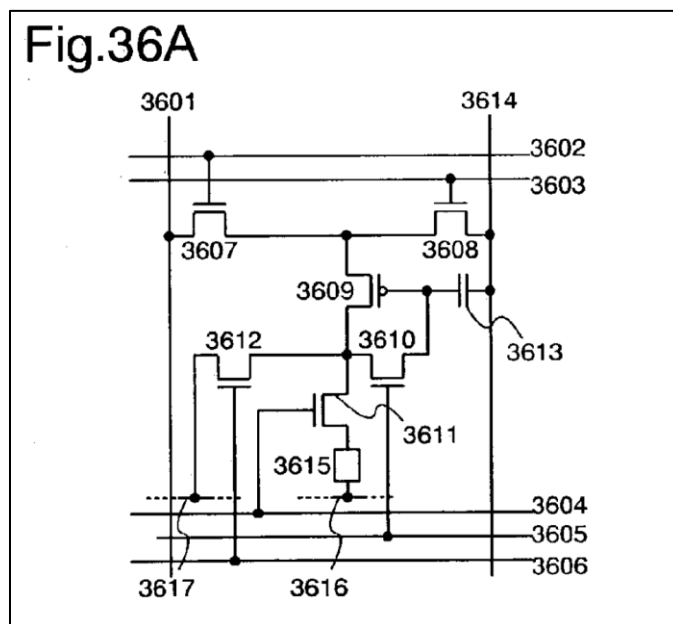
²⁰ As per the description above of the functionality of the circuitry during the initialization step of the ‘599 patent, the use by Kimura of the word “erasure” is descriptively appropriate.



(Annotations added.) Here, a “sixth transistor” (1607) is used to discharge the node connected to the gate of transistor 1608, by draining the charge from the capacitor 1610; in this way, the aforementioned node is discharged without having a transient current run through the light emitting element. Kimura, [0426].

223. Kimura provides a detailed discussion of the operation of the initialization transistor (1607) at [0422]-[0429]. The “gate electrode of the TFT 1607 is connected to the gate signal line 1602 of an (i-1)th row.” Kimura, [0423]. As was the case with the capacitor in the circuitry of Figure. 33, the capacitor in Figure 16 and Figure 17 “stores [a voltage] applied to the gate electrode of the TFT 1608 during the sustain (light emitting) period.” *Id.* As described above, the transistor 1607 serves the same function as does the “initialization transistor” of the circuitry of the ‘599 patent – and is used (as described above) to initialize the node connected to the gate of transistor 1605 – by discharging that node (by draining the charge off the capacitor 1610), as shown in Figure 17A of Kimura. Kimura, [0426].

Further, with transistor 1607 added to the embodiment of Figure 33, the input-signal-timing diagram of Figure 16B of Kimura can be applied to the modified circuitry without any timing modifications at all – as the first gate signal line of the i -th row can remain off during the initialization period (and then turned on at the outset of the programming period), as first gate signal line of the $(i-1)$ th row need only be applied to the reset transistor 1607 (and not at all to transistor 3310). Note also that at Figure 36, Kimura describes a similar modification – using an initialization transistor (3612) that is placed in a different location.



In this embodiment, the initialization/erase requires that the “third transistor” (3610) also be turned on (along with 3612) in order to perform the initialization/erase of the node that connects to the gate of the “second transistor” (3609); this is consistent with Kimura’s teaching that the initialization/erase

transistor (if chosen for explicit inclusion) could in fact be placed at many places in the circuitry.

224. In addition, as was explained above, Kimura uses “i” as an indexing variable – equivalent to the use of the indexing variable “n” in the ‘599 patent; thus, Kimura’s description of “an (i-1)th row” is equivalent to the ‘599 patent’s use of the scan[n-1] signal (described above) – as the prior scan line signal (in both the ‘599 patent and Kimura) is used so that only instances where the node that is connected to the gate of the second transistor was programmed are “initialized” or “erased”²¹, versus leaving the unprogrammed instances alone since those instances do not need to be initialized/erased. Further, Kimura includes detailed control signal/timing waveforms regarding this initialization/erasure operation of Figure 16 and Figure 17. See Kimura [0420]-[0430].

225. Kimura explains that “to perform initialization of a certain row, [the circuit] utilizes the selection pulse of the gate signal line of the previous row in controlling the TFT 1607.” Kimura, [0429]; *see also id.*, [0426] (“The TFT 1607 turns on when the first gate signal line 1602 of the (i-1)th row is selected.”). Again, Kimura is describing the use of a transistor which is activated to discharge the node connected to the gate of the second transistor, as a way of initializing/erasing the

²¹ The ‘599 patent refers to this process as “initialization” – while Kimura refers to this process as both “initialization” and “erasure.”

programming that had been applied to that node – and, by using the previous scan signal, only instances where this programming occurred (when the pixel of that instance was to be programmed to emit light) are activated for initialization/erasure – while the instances where programming did not occur (because the pixel was not going to be instructed to emit light) are left alone, as initialization/erasure is not required. As explained above with regard to the ‘599 patent, it is convenient to use the prior scan line signal (“i-1th” in Kimura), as it is available, and will initialize/erase only those instances where the gate of the second transistor had been programmed during the previous phase of pixel operation. See Kimura, [0422] (only two total control signals needed for pixel circuit; *id.*, [0429] (“[T]o perform initialization of a certain row, it utilizes the selection pulse of the gate signal line of the previous row in controlling the [sixth transistor]....The number of signal lines can be kept to a minimum.”)²² Kimura also provides a timing diagram (at Figure 16B) which shows exactly this – initializing a given row occurs when the “first gate signal” of the “(i-th) row” (i.e. the claimed current scan signal) is asserted. Kimura,

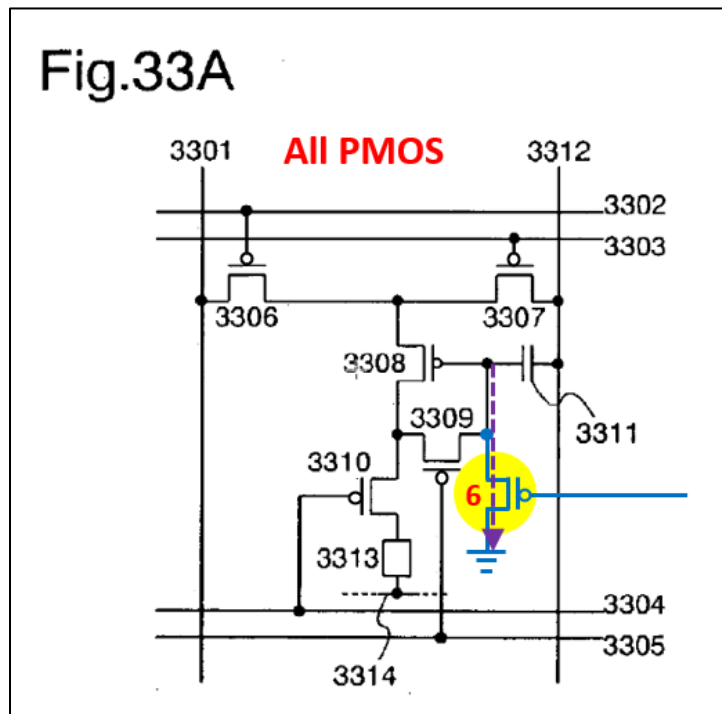
²² It should be noted that Kimura also describes a more-complex scheme which requires a “third gate signal line.” See Kimura, [0421]-[0422] (“In Embodiment Modes 2 and 3, erasure TFT control is performed using an additional third gate signal line” – which results in increased “surface area occupied by wirings.”). Kimura further observes that by reusing an existing signal “[t]he number of signal lines can be kept to a minimum and a high aperture ratio[] can be obtained.” Kimura, [0429].

[0423] (“A gate electrode of the TFT 1607 [sixth transistor] is connected to the gate signal line 1602 of an (i-1)th row.”). As Kimura explains for Figure 16 and Figure 17, “to perform initialization of a certain row, [the circuit] utilizes the selection pulse of the gate signal line of the previous row in controlling the TFT 1607 [sixth transistor].” Kimura, [0429]; *see also id.*, [0423] and [0426].

226. As further explained above, this initialization/erasure operation serves to erase the prior programming of pixels that had been programmed to emit light during that cycle – providing a clean slate for the programming of the pixels for the next cycle. *Id.*, [0427]. The operation that Kimura depicts in Figure 17B is similar to that which Kimura depicts in Figure 33C and Figure 33D.

227. Clearly, a POSITA reading Kimura would see the approach detailed in Figure 33 (and Figure 34) and explained in the specification of Kimura (including the reasons for that embodiment to discharge the relevant node through the light-emitting element), and would also see the approach described in Figure 16 and Figure 17 and explained in the specification of Kimura (including the reasons for putting up with the need for an extra transistor in the circuit as a way of avoiding light emission by the light-emitting element during the discharge step); further, a POSITA would readily understand the trade-offs inherent in using one approach or the other.

228. Thus, a POSITA would have been motivated to combine the initialization approach disclosed in Kimura at Figure 16 and Figure 17 with the approach disclosed by Kimura at Figure 33 – by adding a dedicated initialization transistor (i.e., the “sixth transistor” of the ‘599 patent).



(The figure has been annotated to depict this addition of the “sixth transistor,” in blue.) This is a simple insertion of an additional transistor into the circuitry of Figure 33 of Kimura, guided by Kimura’s disclosures as associated with Figure 16 and Figure 17; as noted earlier, when discussing Figure 33, Kimura expressly teaches that “the erasure [transistor] can be placed *in any location*, provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing.” Kimura, [0658] (emphasis added). Further, with regard to both

the embodiment of Figure 33 and the embodiment of Figure 16 and Figure 17, Kimura clearly describes the use of the existing prior scan signal (“i-1th”) to carry out the initialization/erasure operation – in a manner that is basically identical to that described in the ‘599 patent.

229. Thus, a POSITA would have been motivated to place the initialization transistor discussed in Figure 16 and Figure 17 in the same location (i.e., directly connected to the node that is connected to the gate of the second transistor and the capacitor) in Figure 33. Just as Kimura depicts in Figure 17B, during initialization/erasure in the modified Figure 33 shown above, the sixth transistor is turned on – thus a current path (shown by purple arrow in the annotated figure above) is created that discharges the node connected to the gate of the second transistor (by discharging the charge from the capacitor) to ground (or similar) with no current passing through the light emitting element. Kimura, [0666]. Finally, note that in Kimura this initialization/erasure operation occurs “just before the current scan signal upon initialization.” The ease of implementation (e.g. only adding one transistor) and the simple nature of this dedicated reset-transistor approach would provide a POSITA with a reasonable expectation of success.

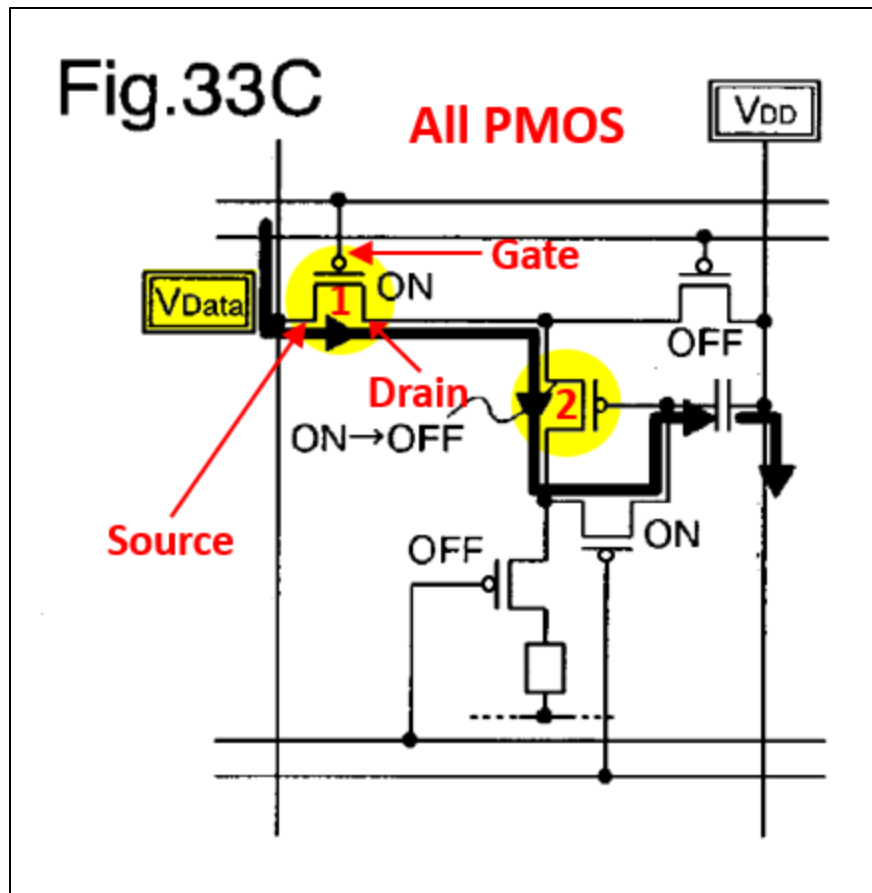
230. Thus, the combination of the initialization/erasure transistor (1607) from Figure 16 of Kimura with the circuitry of Figure 33 of Kimura renders Claim 8 of the ‘599 patent obvious.

C. Claim 9

231. Before beginning the analysis of Claims 9 – 13, it should be noted that these dependent claims recite the verbal description of the circuit topology of the circuitry disclosed in Figure 3 of the ‘599 patent.

232. Regarding Claim 9, Claim 9 depends from Claim 7; as an initial matter, it was shown above that Kimura renders Claim 7 obvious.

233. Claim 9 further requires that “the first transistor is composed of a PMOS transistor including a gate to which the current scan line signal is applied, a source to which the data signal voltage is applied, and a drain coupled to the second transistor.”



Earlier (in Section X.A), an all-PMOS version of Kimura was introduced – with the reasons-for and obviousness-of such a minor change noted both there and in Section VII.A.2. As depicted in the annotated figure above (which was also discussed earlier), the first transistor (3306) is pMOS, while the gate is connected to the current scan line signal (via the line 3302).

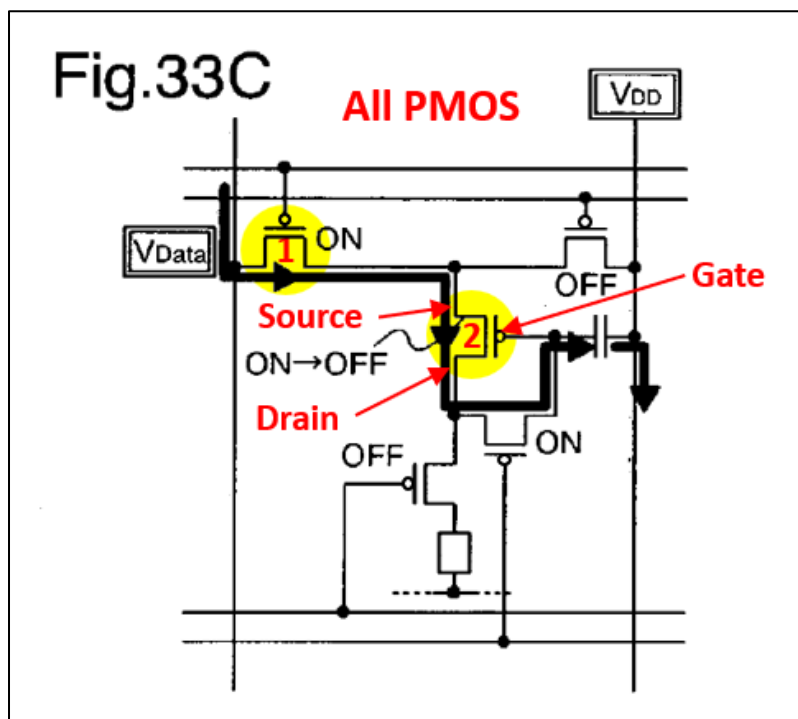
234. Further, as the annotated figure above shows, the “source” of the first transistor (as labeled) is connected to the “data signal voltage,” while the “drain” of the first transistor is coupled to (i.e., connected to the current flow path of) the second transistor.

235. Thus, Kimura renders Claim 9 of the '599 patent obvious.

D. Claim 10

236. Claim 10 depends from Claim 7; as an initial matter, it was shown above that Kimura renders Claim 7 obvious.

237. Claim 10 further requires that the “second transistor is composed of a PMOS transistor including a gate coupled to one terminal of the capacitor, a source coupled to the first transistor, and a drain coupled to the electroluminescent element.” Kimura discloses this limitation in Figure 33.



238. Earlier (in Section X.A), an all-PMOS version of Kimura was introduced – with the reasons-for and obviousness-of such a minor change noted both there and in Section VII.A.2. As depicted in the annotated figure above (which

was also discussed earlier), the second transistor (3308) is pMOS – and, as noted in those earlier discussions, Kimura specifically uses a pMOS transistor for the second transistor (3308), with the reason for this special usage (while all the other transistors are nMOS) also explained in those earlier discussions (see Section VII.A.2). Further, as the annotated figure above shows, the gate of the second transistor is connected to one terminal of the capacitor (3311), the “source” of the second transistor (as labeled) is coupled to (i.e., directly connected to the current flow path of) the first transistor, and the “drain” of the second transistor is coupled (i.e., directly connected to the current flow path of) the electroluminescent element (3313). Note that the “drain” of the second transistor is coupled to the electroluminescent element through the fifth transistor (3310).

239. Thus, Kimura renders Claim 10 of the ‘599 patent obvious.

E. Claim 11

240. Claim 11 depends from Claim 10, which depends from Claim 7; as an initial matter, it was shown above that Kimura renders Claim 7 obvious and Claim 10 obvious.

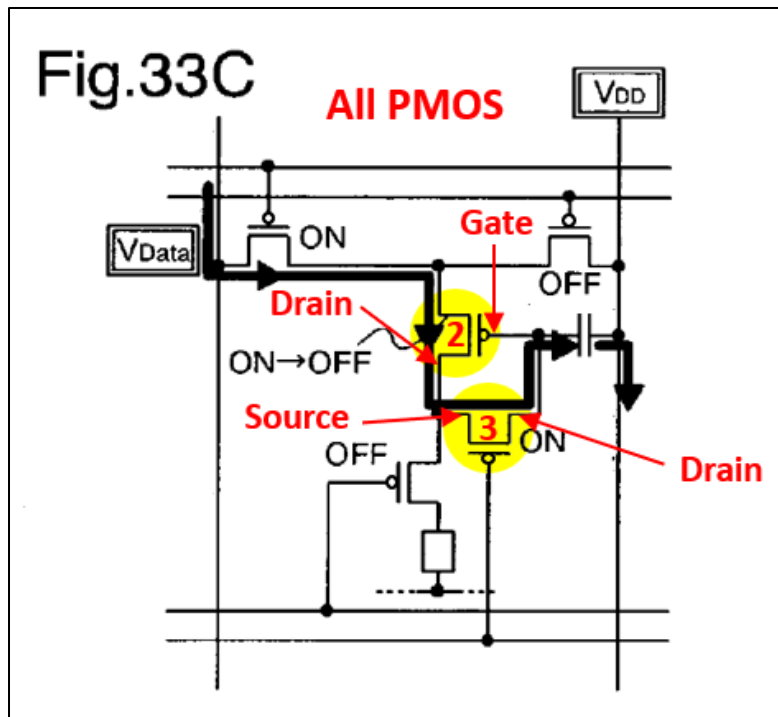
241. Claim 11 further requires that “the third transistor is composed of a PMOS transistor including a gate to which the current scan signal is applied, and a drain and a source which are coupled to the gate and the drain of the second transistor, respectively, so that the third transistor connects the second transistor in

the form of a diode in response to the current scan signal to self-compensate a threshold voltage of the second transistor.”

242. First, the earlier discussion of claim element [7b] has already explained how the current scan signal is used to “compensate a threshold voltage of the second transistor.” Second, the earlier discussion of claim element [7h] (and Section VII.A.6) has already explained the meaning of the phrase “in the form of a diode” with respect to the configuration of a transistor in that form – and it was also explained how the third transistor serves to connect the second transistor “in the form of a diode.”

243. Thus, Claim 11 adds only the requirement that third transistor be a pMOS transistor, and that the gate, source, and drain of that third transistor are connected so that “a gate to which the current scan signal is applied, and a drain and a source which are coupled to the gate and the drain of the second transistor.”

244. Kimura discloses this limitation in Figure 33C.



245. Earlier (in Section X.A), an all-PMOS version of Kimura was introduced – with the reasons-for and obviousness-of such a minor change noted both there and in Section VII.A.2. As depicted in the annotated figure above (which was also discussed earlier), the third transistor (3309) is pMOS. Further, the annotated figure above shows how the gate, source, and drain of the third transistor are connected in accordance with the operational definition of source and drain provided in Section VII.A.1; as explained in the discussion of claim element 7[c] above, “the current scan signal is applied” to the gate of the third transistor, while the source and drain of the third transistor “are coupled to the gate and the drain of the second transistor, respectively.” Thus, in Kimura, the source of the third transistor is coupled to the gate of the second transistor, and the drain of the third

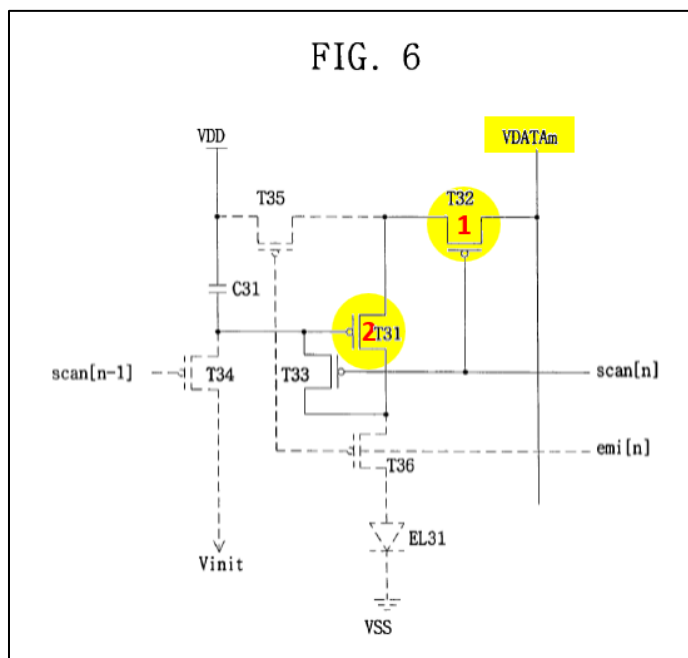
transistor is coupled to the drain of the second transistor; this is depicted in the annotated figure above, in accordance with the current flow direction.

246. Thus, Kimura renders Claim 11 of the '599 patent obvious.

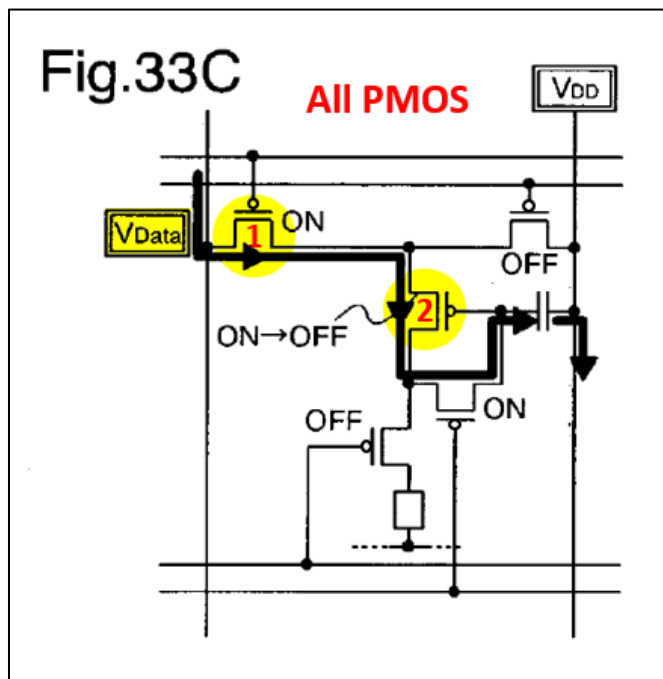
F. Claim 12

247. Claim 12 depends from Claim 7; as an initial matter, it was shown above that Kimura renders Claim 7 obvious.

248. Claim 12 further requires “a voltage source for providing the data signal voltage through the first transistor for the second transistor.” As was already described earlier in the discussion of claim element 7[a], in the '599 patent at Figure 6, the “voltage source for providing the data signal voltage” is VDATA_m – which is connected to the source of the first transistor (T32). *See also* Section VIII.B.



249. As was also described earlier in the discussion of claim element 7[a], Kimura discloses “a voltage source for providing the data signal voltage through the first transistor for the second transistor.”



(Note once again that the black arrows indicating current flow are *not* annotations added here – but appear as-is in Kimura; also, the label of “V_{data}” (as well as “V_{DD}”) are also in Kimura’s figure, as-is.) As shown in this annotated version of Figure 33C of Kimura, the “voltage source” (V_{Data}) passes through the first transistor to the second transistor – thus “providing the data signal voltage through the first transistor for the second transistor.” Based on the name V_{Data} and the overall operation of the circuit, a POSITA would understand that V_{Data} is a voltage source (and not, *e.g.*, a current source). Note also that Kimura states in the specification that “the TFT 3306 [the first transistor] turns on, and an image signal V_{Data} is input.”). Kimura at [0655].

250. Thus, Kimura renders Claim 12 of the ‘599 patent obvious.

G. Claim 13

251. Claim 13 depends from Claim 7; as an initial matter, it was shown above that Kimura renders Claim 7 obvious.

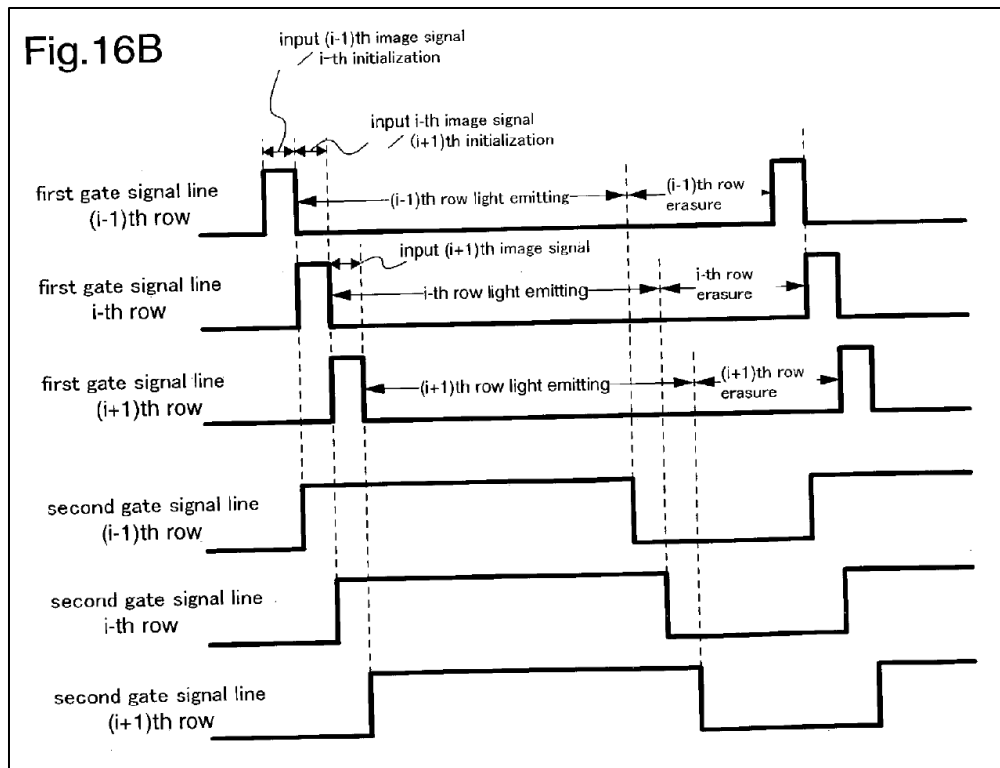
252. Claim 13 further requires that “the fourth transistor is composed of a PMOS transistor including a gate to which the current light-emitting signal is applied, a source to which a power supply voltage is applied, and a drain coupled to the second transistor; and the fifth transistor is composed of a PMOS transistor including gate to which the current light-emitting signal is applied, a source coupled to the second transistor, and a drain coupled to the electroluminescent element.” In order to simplify the analysis, the main part of this claim will be split into two elements (below). However, for further simplicity, two aspects common to both claim elements can be discussed beforehand.

253. First, earlier (in Section X.A), an all-PMOS version of Kimura was introduced – with the reasons-for and obviousness-of such a minor change noted both there and in Section VII.A.2. Thus, Kimura discloses this aspect of Claim 13 of the ‘599 – that it would be obvious to use pMOS transistors (rather than nMOS transistors) for the fourth transistor and the fifth transistor, as a simple choice of one (nMOS) or the other (pMOS).

254. Second, Claim 13 requires that “the current light emitting signal” be applied to the gate of both the fourth and fifth transistors. This is the first time that “the current light emitting signal” has appeared in this analysis – and thus, this term requires a discussion at this point.

255. As explained in the detailed overview of the ’599 patent (in Section VIII), the “light emitting signal” can be a shared control signal that simultaneously controls the gate of the fourth transistor and the gate of the fifth transistor; this simultaneous application to these two transistor gates serves two functional purposes: (1) to turn the fourth transistor and the fifth transistor on during light emission, so current flows through the light emitting element (causing it to emit light); and (2) to turn off the fourth transistor and the fifth transistor at all other times. *See, e.g.*, ’599 patent, Fig. 7 and 7:50-65.

256. In Kimura, the “second gate signal” (a term that appears dozens of times in Kimura to describe the various operations disclosed in numerous figures) is the claimed “light emitting signal.” (E.g., Kimura at Figs. 16-17, and in the accompanying discussion at [0422] – [0429].) As shown, for example, in the timing diagram of Fig. 16B, the “light emitting” period for each row is controlled by the corresponding “second gate signal” for that row.



In the same manner in which the '599 patent uses the index “n” to distinguish between adjacent lines of pixels, Kimura uses the index “i” for the same purpose.²³ For example, in Figure 16B, Kimura describes the “(i-1)th row” of pixels, the “i-th” row of pixels, and the “(i+1)th” row of pixels.

257. Although the embodiment described by Figure 33 shows the fourth and fifth transistors as having different signals applied to them (which is also indicated by depiction of Figure 33B, where the fourth transistor is “OFF” while the fifth transistor “ON”), the embodiment described in Figure 36 shows a different situation – one where, in all operation states depicted (which are Figure 36B (initialization),

²³ This was explained in more detail earlier – for example, in Section XII.A.2.

Figures 36C and 36D (programming), and Figure 36E (light emission)), the fourth and fifth transistors are always ON or OFF in tandem (that is, both are either OFF together at the same time, or ON together at the same time).

258. Thus, Kimura discloses an embodiment that, in practice, has the same current light-emitting signal applied to the gates of both the fourth transistor and the fifth transistor – and a POSITA would have been motivated to use a shared light-emitting signal to control them. Kimura itself provides one reason for doing so – that reducing the number of control lines improves the aperture ratio. (For example, Kimura at [0429], as well as at [0421] – [0422] (stating that a control scheme with fewer signals reduces “the surface area occupied by wirings in a pixel”).) Additionally, the fourth and fifth transistors must both be active during light emission – since light emission requires that both the fourth transistor and the fifth transistor be turned on (as detailed in Section IX), so that current is able to flow through those two transistors, the second transistor, and the electroluminescent element, so that the electroluminescent element will emit light. As it is obvious that the fourth transistor and the fifth transistor must both be turned on during light emission, this would have naturally led a POSITA to use a shared light-emitting signal in the various embodiments of Kimura.

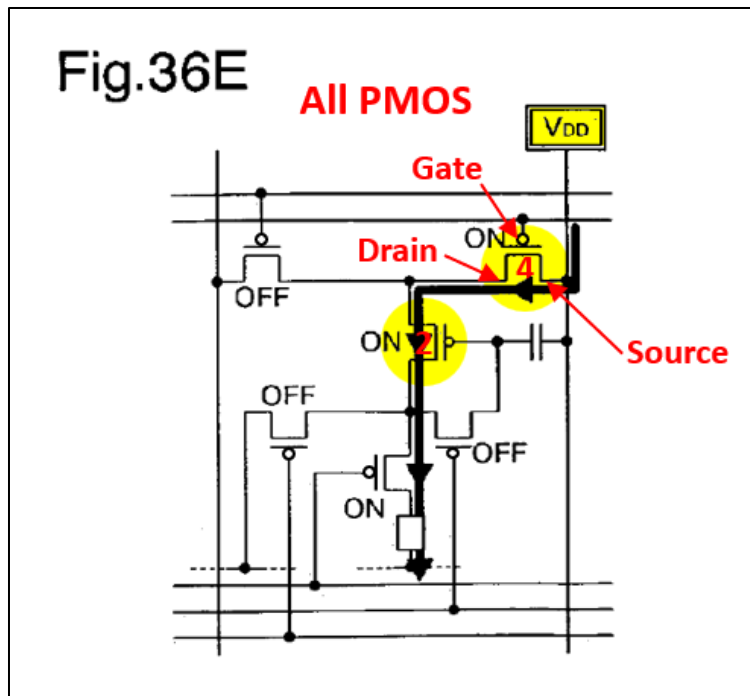
259. Finally, revisiting Figure 16B above, it should be noted that Kimura discloses a timing diagram and control scheme which utilizes only two signals – the

first gate signal (which has already been shown to be the “scan line signal” of the ‘599 patent), and the second gate signal (which has already been shown to be the “light emitting signal” of the ‘599 patent). In addition to Figure 16 and Figure 17, Kimura provides a detailed explanation in the specification at [0420] – [0429]. Thus, a POSITA would have been motivated to use a shared light emitting signal for application to the gates of the fourth and fifth transistors – and particularly given the various embodiments disclosed in Kimura, this would have a reasonable expectation of success.

260. As Kimura renders obvious those two aspects of Claim 13 with respect to the fourth transistor and the fifth transistor, the separate element analysis below need only consider the requirements provided for the connections of the terminals of each of these transistors.

1. **[13a] “wherein the fourth transistor is composed of a PMOS transistor including a gate to which the current light-emitting signal is applied, a source to which a power supply voltage is applied, and a drain coupled to the second transistor, and”**

261. Kimura discloses this claim element – as is made evident by examination of an all-PMOS version Figure 36E of Kimura.



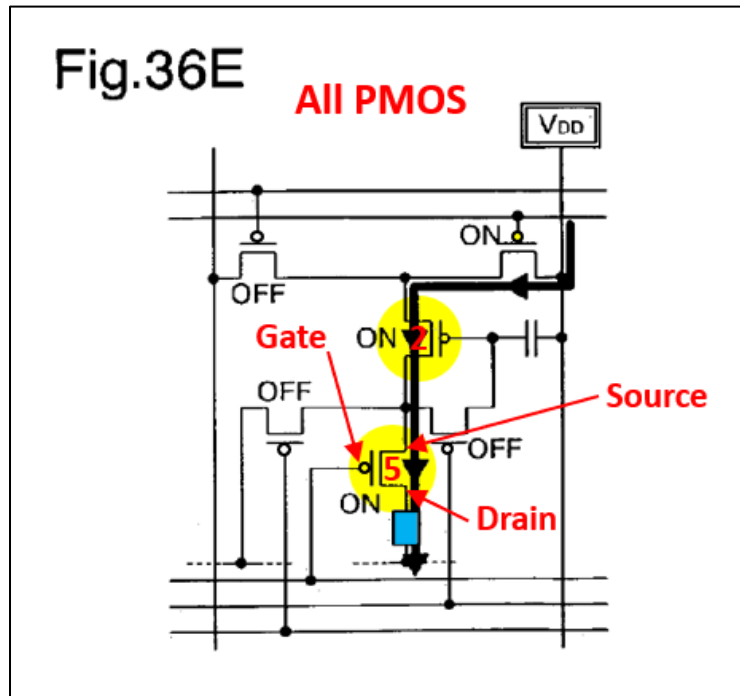
(Annotations added – though note again that the black arrows, depicting the flow of current, are *not* annotations, but are present as-is in Kimura’s figure.) This figure from Kimura depicts the light-emitting phase – in which a current-flow path is provided, so that a (compensated) current flows down and through the emitter (3615), so that the emitter emits light. As the annotations show regarding the fourth transistor (3608), the current light-emitting signal is applied to the gate, a power supply voltage (i.e., VDD) is applied to the source, and the drain is coupled to the second transistor (3609).

262. Thus, Kimura discloses this claim element of Claim 13 of the ‘599 patent.

2. [13b] “the fifth transistor is composed of a PMOS transistor including a gate to which the current light-emitting signal is

applied, a source coupled to the second transistor, and a drain coupled to the electroluminescent element.”

263. Kimura discloses this claim element – as is made evident by examination of Figure 36E of Kimura.



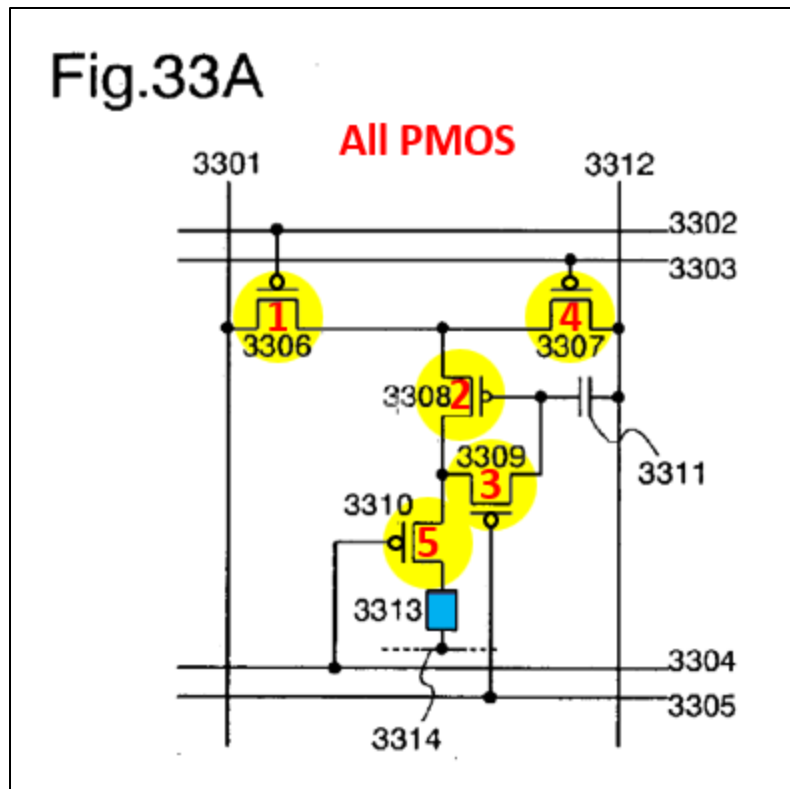
(Annotations added – though note again that black arrows, depicting the flow of current, are *not* annotations, but are present as-is in Kimura’s figure.) As detailed just above, this figure from Kimura depicts the light-emitting phase – in which a current-flow path is provided, so that a (compensated) current flows down and through the emitter (3615), so that the emitter emits light. As the annotations show regarding the fifth transistor (3611), the current light-emitting signal is applied to the gate, the source is coupled to the second transistor (3609), and the drain is coupled to the electroluminescent element (3615).

264. Thus, Kimura discloses this claim element of Claim 13 of the ‘599 patent.

265. Therefore, in complete summary, Kimura renders Claim 13 of the ‘599 patent obvious.

H. Independent Claim 14

266. Independent Claim 14 is substantially similar to independent Claim 7, which was analyzed above (in Section XII.A). Both claims use the same circuit elements, connected together in the same way, and operating in the same way; in fact, even the transistor numbering used in Claim 14 is the same as the numbering scheme used in Claim 7. As was explained in Section XII.A, the details of the circuitry are disclosed in Kimura – as a reprise of Figure 33A of Kimura makes clear.



267. As was also explained in Section XII.A, it would have been obvious to a POSITA to convert this circuitry of Kimura into the all-PMOS form that is recited in Claim 7 – using both the disclosure elsewhere in Kimura and the knowledge and experience of a POSITA (with the latter being explained via reference to other prior art references for confirmation). This is also the case with the recitations of Claim 14.

268. Thus, for substantially the same reasons as those disclosed with regard to Claim 7, Kimura discloses Claim 14 of the ‘599 patent.

269. To simplify the element-by-element of Claim 14 that follows, as much as possible reference will be made to details that were already explained in Section

XII.A (where the claim elements of Claim 7 were analyzed); the focus here will be on any lexicographical or material differences (with respect to Claim 7) that need to be addressed with respect to Claim 14.

1. [Claim 14 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”

270. As was the case with Claim 7, I will be offering no opinion regarding whether or not the preamble of Claim 14 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting.

271. The preamble of Claim 14 is identical to the preamble of Claim 7; thus, to the extent that the preamble of Claim 14 is limiting, Kimura discloses this claim element of Claim 14 of the ‘599 patent.

2. [14a]: “an electroluminescent element for emitting light in response to an applied driving current;”

272. This claim element is nearly identical in wording to claim element 7[g], which was analyzed in Section XII.A.8. Both recite “an electroluminescent element for emitting light” – and thus, this part of claim element 14[a] is disclosed in claim element 7[g], for the same reasons as those explained in Section XII.A.8.

273. The only difference between these two claim elements is a difference in wording – with the wording being “in response to an applied driving current” in this claim element, and “corresponding to the driving current” in claim element 7[g]. However, it is rather clear that these are the same thing – as it is (the magnitude of)

the driving current being forced through the electroluminescent element that will cause that element to emit light; both claim elements recite this limitation.

274. Therefore, Kimura discloses this claim element of Claim 14 of the ‘599 patent for the reasons explained for claim element 7[g].

3. [14b]: “a first transistor for delivering a data signal voltage in response to a current scan line signal;”

275. This claim element is identical to claim element 7[a], which was analyzed in Section XII.A.2. As it was shown there that Kimura discloses that claim element of Claim 7, Kimura thus also discloses this claim element of Claim 14 of the ‘599 patent.

4. [14c]: “a second transistor for generating a driving current to drive the electroluminescent element in response to the data signal voltage;”

276. This claim element is worded nearly identically to claim element 7[b] of the ‘599 patent – which was analyzed in Section XII.A.3. Both recite “a second transistor ... for generating a driving current ...” This claim element recites that this occurs “in response to the data signal voltage,” while claim element 7[c] recites that this occurs there “in response to a programmed data signal.” This is the same functionality stated in different words. The functionality in question was already described with regard to claim element 7[b] and claim element 7[c] – as involving the programming step, whereby a particular voltage is brought into being at the node that is connected to the gate of the second transistor. This claim element refers to

this programmed voltage as “the data signal voltage,” while claim element 7[b] refers to this programmed voltage as “a programmed data signal.” These are the same thing – and in both cases, as was explained in Section XII and in the technology background (in Section VIII and Section IX), it is this programmed voltage that is used to eliminate the effect of the variability of the threshold voltage across numerous instances of the second transistor across numerous instances of the pixel-driving circuitry – so each light emitter will receive the same current, and thus emit light at the same brightness.

277. Thus, for the reasons already discussed in Section XII.A.3 (and Section XII.A.4), Kimura discloses this claim element of Claim 14 of the ‘599 patent.

5. [14d]: “a third transistor for connecting the second transistor in the form of a diode in response to the current scan signal to self-compensate a threshold voltage of the second transistor;”

278. This claim element combines different elements from the claim elements of Claim 7. “A third transistor” is recited in claim element 7[c] (discussed in Section XII.A.4), while that the third transistor connects “the second transistor in the form of a diode in response to a current scan signal” is recited in claim element 7[h] (discussed in Section XII.A.9). For the reasons already discussed with regard to claim elements 7[c] and 7[h], Kimura discloses those parts of this claim element.

279. The only difference between the latter part of this claim element and the latter part of claim element 7[h] is that this claim element uses the language “to

self-compensate a threshold voltage of the second transistor,” while claim element 7[h] uses the language “so that the second transistor detects and compensates its threshold voltage in itself.” Once again, these are both differently-worded recitations of the programming step that is described in the ‘599 patent – as was explained in Section VIII and in Section XII.A; as was explained in Section IX and in Section XII.A, Kimura discloses this same programming step.

280. Thus, in sum, Kimura discloses this claim element of Claim 14 of the ‘599 patent.

6. [14e]: “a capacitor for storing the data signal voltage delivered to the second transistor;”

281. This claim element is nearly identical to claim element 7[d], which was analyzed in Section XII.A.5. Both disclose a capacitor which serves, as detailed in Section VIII and in Section XII.A.5, to cause the voltage that is programmed onto the node of the second transistor of the programming step (described repeatedly above) to remain static at the fixed, programmed value. This claim element refers to this functionality as “storing the data signal,” while claim element 7[d] refers to this functionality as “maintaining the data signal”; these are same functionality, and both are applied to the same place in the circuitry of the ‘599 patent (the node that connects to the gate of the second transistor). This claim element using the phrase “delivered to” in place of the use of “programmed onto” in claim element 7[d] – but again, these amount to the same thing.

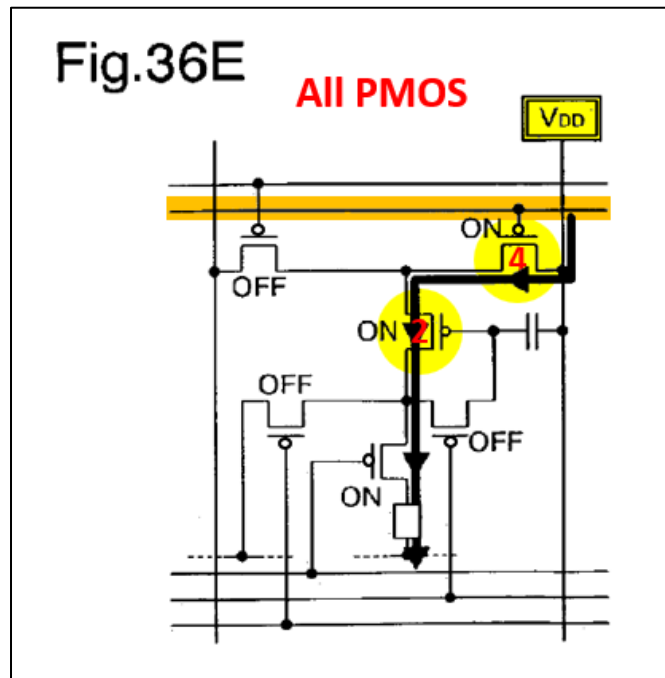
282. Thus, as Kimura discloses claim element 7[d], Kimura also discloses this claim element of Claim 14 of the ‘599 patent.

7. [14f]: “a fourth transistor for delivering a power supply voltage to the second transistor in response to a current light-emitting signal;”

283. This claim element of Claim 14 is nearly identical to claim element 7[e], which was analyzed in Section XII.A.6. Both recite “a fourth transistor for delivering a power supply voltage to the second transistor.” The only difference is one of wording – where here the concluding language is “in response to a current light-emitting signal,” while in claim element 7[e] the concluding language is “when the light is emitted.” Both of these involve the emitting period of the operation of the circuitry of the ‘599 patent – as was explained in Section VIII above. As was explained there, the light-emitting signal is identified as the “emi[n]” signal that is applied to the circuitry disclosed in Figure 3 of the ‘599 patent; this “current light-emitting signal” is applied to the fourth transistor (in the language of claim element 7[e] “when light is emitted.” Thus, these are the same things.

284. In Kimura Figure 36E, the signal line highlighted in orange controls the fourth transistor’s gate. When this signal activates the fourth transistor, the fourth transistor delivers V_{DD} (a power supply voltage) to the second transistor. For the reasons I discuss for Claim 13, it would have been obvious to a POSITA to use the

second gate signal for the row of pixels currently being activated (the “current light-emitting signal”) to control the fourth transistor.



285. Thus, for the same reasons as those already discussed in Section XII.A.6 and XII.G, Kimura discloses this claim element of Claim 14 of the ‘599 patent.

8. [14g]: “a fifth transistor for providing the driving current, provided from the second transistor, for the electroluminescent element in response to the current light-emitting signal.”

286. The first part of this claim element (“a fifth transistor for providing the driving current, provided from the second transistor”) is identical to wording already discussed with respect to claim element 7[f] – with the only difference being that this claim element uses the word “providing” while claim element 7[f] uses the word “delivering.” These are essentially synonyms for the exact same functionality.

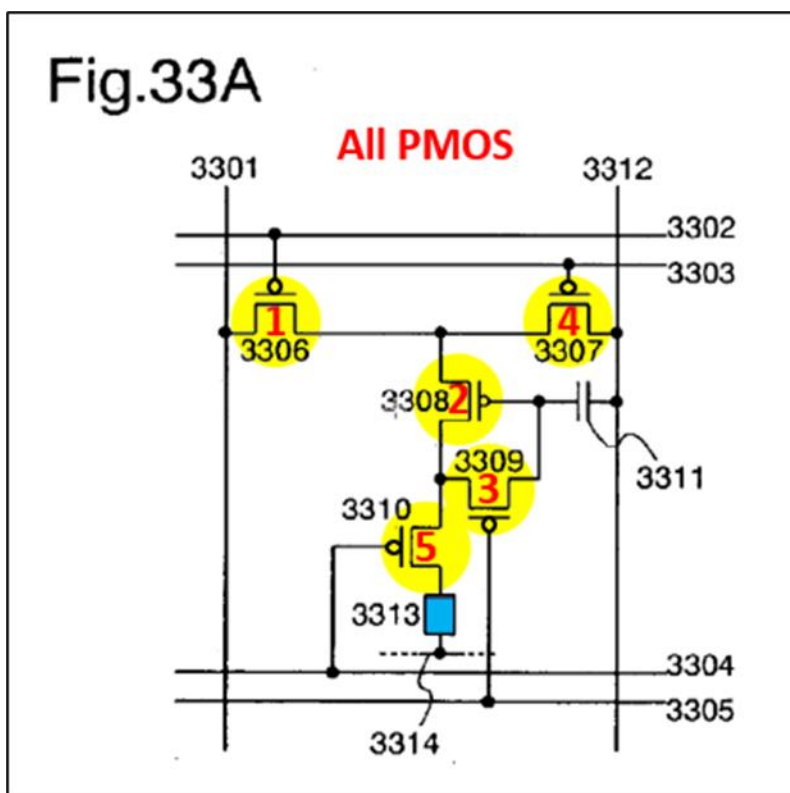
287. The latter part of this claim element uses the wording “for the electroluminescent element in response to the current light-emitting signal,” while claim element 7[f] uses the wording “in response to the data signal voltage when the light is emitted.” Once again, these are simply different ways of describing the emitting period in the operation of the circuitry of Figure 3 of the ‘599 patent – which was explained in detail in Section VIII, and also in Section XII.A.6 and Section XII.A.7. In both claim elements, these are simple statements that the fifth transistor is turned on during the emitting period, as part of the provision of a current-flow path from VDD to the low side of the light-emitting element – with the specific level of the current being determined by the programming that has been applied to the second transistor (as has been explained numerous times already). More particularly, the way in which Kimura meets that “current light-emitting signal” requirement is addressed in the discussion of Claim 13, which requires that “the current light-emitting signal is applied” to control the gate of the fifth transistor.

288. Thus, for the reasons discussed with respect to claim element 7[f] and claim 13, Kimura discloses this claim element of Claim 14 of the ‘599 patent.

I. Independent Claim 15

289. Independent Claim 15 is substantially similar to independent Claim 7 (which was analyzed above in Section XII.A). Both claims use five transistors, an electroluminescent element, and a capacitor for controlling the driving transistor,

and operate in the same way; in fact, even the transistor numbering used in Claim 15 is the same as the numbering scheme used in Claim 7. The main difference between Claim 7 and Claim 15 is that Claim 15 requires pMOS transistors due to the specified source and drain connections. As was explained in Section XII.A, the details of the circuitry are disclosed in Kimura – as a reprise of Figure 33A of Kimura makes clear.



290. As was also explained in Section XII.A, it would have been obvious to a POSITA to convert this circuitry of Kimura into the all-PMOS form – using both the disclosure elsewhere in Kimura and the knowledge and experience of a POSITA

(with the latter being explained via reference to other prior art references for confirmation). This is also the case with the recitations of Claim 15.

291. Thus, for substantially the same reasons as those disclosed with regard to Claim 7, Kimura discloses Claim 15 of the ‘599 patent.

292. To simplify the element-by-element of Claim 15 that follows, as much as possible reference will be made to details that were already explained in Section XII.A (where the claim elements of Claim 7 were analyzed) and Section XII.H (where the claim elements of Claim 14 were analyzed); the focus here will be on any lexicographical or material differences (with respect to Claim 7 and Claim 14) that need to be addressed with respect to Claim 15.

1. [Claim 15 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”

293. As was the case with Claim 7, I will be offering no opinion regarding whether or not the preamble of Claim 15 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting.

294. The preamble of Claim 15 is identical to the preamble of Claim 7; thus, to the extent that the preamble of Claim 15 is limiting, Kimura discloses this claim element of Claim 15 of the ‘599 patent.

2. [15a]: “a first transistor including a gate to which a current scan signal is applied, and a source to which a data signal voltage is applied;”

295. The identification of the “first transistor” in both the embodiment of Figure 3 of the ‘599 patent and in the embodiment of Figure 33 of Kimura was already explained earlier with regard to claim element 7[a] (Section XII.A.2).

296. The remainder of this claim element (“including a gate to which a current scan signal is applied, and a source to which a data signal voltage is applied”) appears nearly word-for-word the same in Claim 9 (Section XII.C) – with the only differences being the inconsequential instances of this claim element referring to “a current scan signal” (while Claim 9 refers to “the current scan line signal” and the inclusion of “and” in this part of the claim element (while Claim 9 is describing three things and thus does not include this particular instance of “and”).

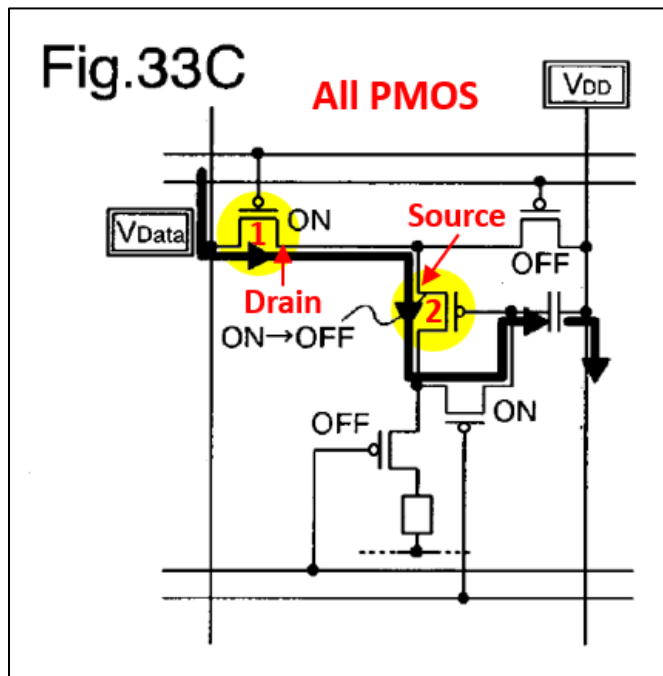
297. For the reasons explained in those earlier sections, Kimura discloses this claim element of Claim 15 of the ‘599 patent.

3. [15b]: “a second transistor whose source is coupled to a drain of the first transistor;”

298. The identification of the “second transistor” in both the embodiment of Figure 3 of the ‘599 patent and in the embodiment of Figure 33 of Kimura was already explained earlier with regard to claim element 7[b] (Section XII.A.3) .

299. That the second transistor in Kimura is coupled to the drain of the first transistor appears in Claim 9 (“wherein the first transistor... a drain coupled to the

second transistor”), as was shown in Section XII.C. The only additional requirement here is that, more specifically, the *source* of the second transistor must be coupled to the drain of the first transistor; this is readily-evident via examination of an annotated all-PMOS version of Figure 33C of Kimura.



As per the explanation of how the source and the drain of a transistor are operationally-defined (which appeared in Section VII.A.1), the source of the second transistor is coupled to the drain of the first transistor.

300. Thus, Kimura discloses this claim element of Claim 15 of the ‘599 patent.

4. [15c]: “a third transistor whose drain and source are connected between a gate and a drain of the second transistor;”

301. The identification of the “third transistor” in both the embodiment of Figure 3 of the ‘599 patent and in the embodiment of Figure 33 of Kimura was already explained earlier with regard to claim element 7[c] (Section XII.A.4).

302. The remainder of this claim element (regarding a third transistor “whose drain and source are connected between a gate and a drain of the second transistor”) appears in Claim 11 (“a drain and a source which are coupled to the gate and the drain of the second transistor, respectively”). As was explained in regard to Claim 11 (Section XII.E), Kimura discloses this part of this claim element.

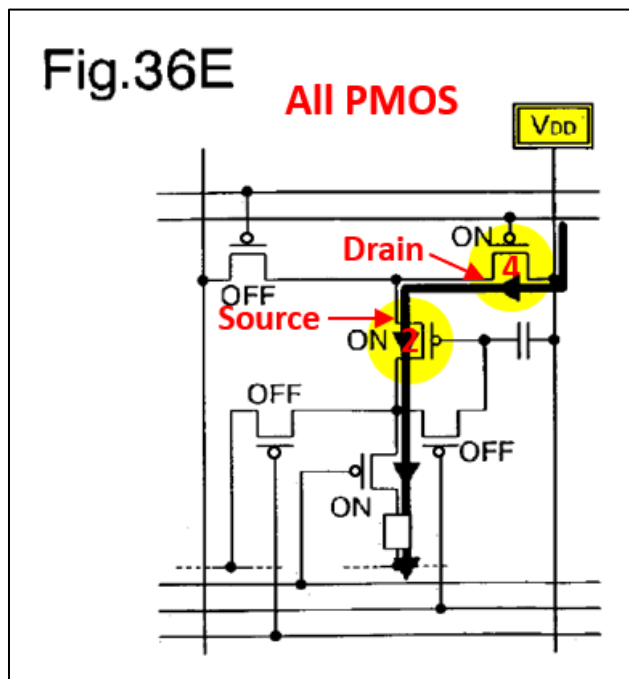
303. Thus, Kimura discloses this claim element of Claim 15 of the ‘599 patent.

5. [15d]: “a fourth transistor including a gate to which a current light-emitting signal is applied, a source to which a power supply voltage is applied, and a drain coupled to the source of the second transistor;”

304. Every aspect of this claim element is recited in Claim 13 (as was discussed earlier, in Section XII.G.1) – except for the additional detail that rather than “a drain coupled to the second transistor,” there is the additional detail here that the drain must be (more-specifically) couple to the *source* of the second transistor.

305. This additional detail is readily-evident via examination of an annotated all-PMOS version of Figure 36E of Kimura:

306. As the labeling shown here results from the operational method of defining a transistor source and a transistor drain (as explained in Section VII.A.1), this additional detail is disclosed in Kimura.



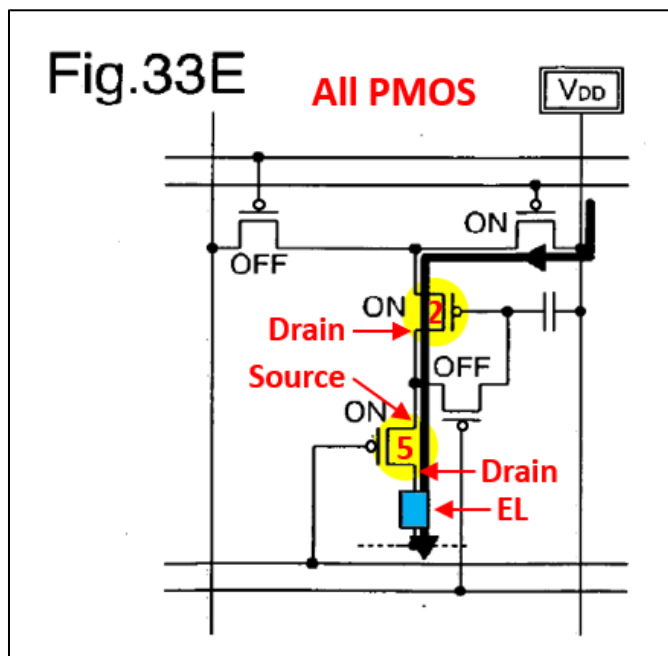
307. Thus, Kimura discloses this claim element of Claim 15 of the ‘599 patent.

6. [15e]: “a fifth transistor including a gate to which the current light-emitting signal is applied, a source coupled to the drain of the second transistor, and a drain coupled to one terminal of an electroluminescent element;”

308. Every aspect of this claim element is recited in claim element 14[g] (Section XII.H.8) and Claim 13 (Section XII.G.1) – except for the additional detail that rather than “a drain coupled to the second transistor,” there is the additional

details here that the fifth transistor's source is coupled to "the drain of" the second transistor, and that the fifth transistor's drain is coupled to "one terminal of" the electroluminescent element.

309. Kimura discloses these additional details – an examination of an annotated all-PMOS version of Figure 33E of Kimura makes clear.



Note that sources and drains have been labeled in this annotated figure using the operational definitions that were explained in Section VII.A.1. The electroluminescent element (labeled EL), as explained in Section VII.B, has two terminals – one of which is coupled to the drain of the fifth transistor. Meanwhile, the source of the fifth transistor is coupled to the drain of the second transistor.

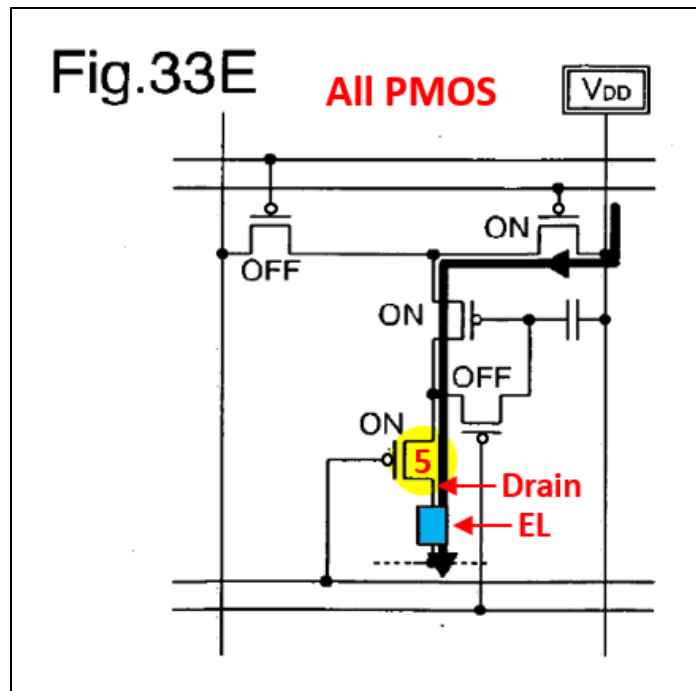
310. Thus, Kimura discloses this claim element of Claim 15 of the '599 patent.

7. [15f]: “the electroluminescent element having the one terminal coupled to the drain of the fifth transistor and the other terminal grounded;”

311. That one terminal of the electroluminescent element is coupled to the drain of the fifth transistor was already shown just above (in Section XII.I.6) to be disclosed in Kimura. The only addition here is the recitation that an electroluminescent element so-connected to the fifth transistor has its second terminal connected to ground.

312. As was explained in Section VII.B.1 (and at other points throughout this Declaration), it has long been well-known in the art that for a two-terminal electroluminescent element (such as an LED) to emit light, a forward-bias current must be applied to that element; here, a “forward bias” means that the voltage on the second terminal must be lower than the voltage on the aforementioned first terminal.

313. The explanation can be continued once an annotated all-PMOS version of Figure 33E of Kimura is presented.



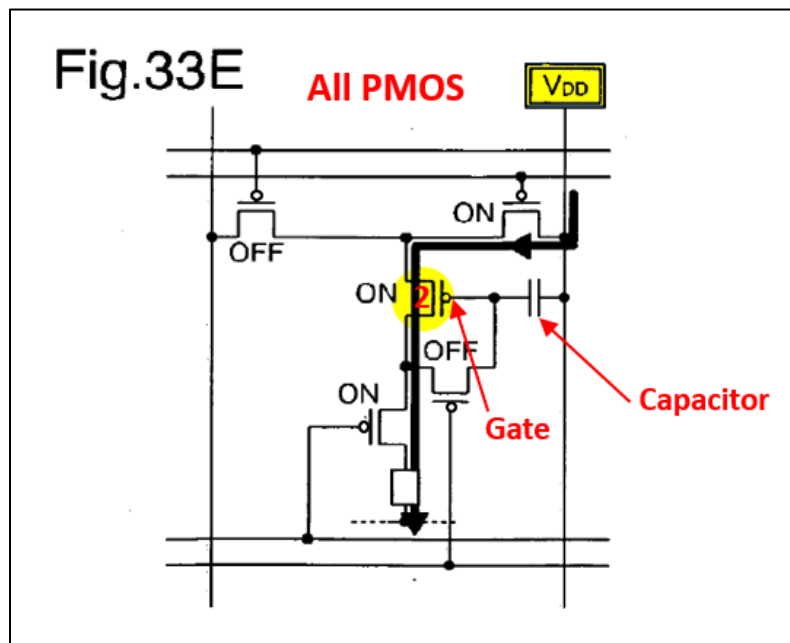
Because a positive voltage is created at the first terminal of the light-emitting element by the circuitry, the simplest and most-obvious selection for a POSITA to make for the second terminal would be, a voltage of 0V – that is, ground. Thus, this reasonable choice of ground would be obvious to a POSITA. That an LED can be connected, on its low side during light-emission, to ground is very well-known in the art as shown, for example, in U.S. Pat. Pub. 2001/0022565 (EX1006) at e.g., Figure 23A; U.S. Pat. Pub. 2003/0030603 (EX1007) at, e.g., Figures 1 and 2; and U.S. Pat. 6,229,506 (EX1012) at, e.g., Figure 2.

314. Thus Kimura renders obvious this claim element of Claim 15 of the ‘599 patent.

8. [15g]: “a capacitor in which one terminal of the capacitor is coupled to the gate of the second transistor and a power supply voltage is applied to the other terminal of the capacitor.”

315. The form and function of the capacitor (C31) in Figure 3 of the ‘599 patent was already partially explained in the analyses of claim element 7[d] (Section XII.A.5) – where, in both cases, the capacitor serves, once the programming period has been completed, to maintain the programmed voltage on the node that connects to the gate of the second transistor.

316. This claim element provides more structural details regarding the connections of the two terminals of that capacitor; that Kimura discloses both of these connections is made readily-evident by examining an annotated all-PMOS version of Figure 33E of Kimura.



As can be seen, “one terminal of the capacitor is coupled to the gate of the second transistor and a power supply voltage [i.e., V_{DD}] is applied to the other terminal of the capacitor.”

317. Thus, Kimura renders obvious this claim element of Claim 15 of the ‘599 patent.

J. Dependent Claim 16

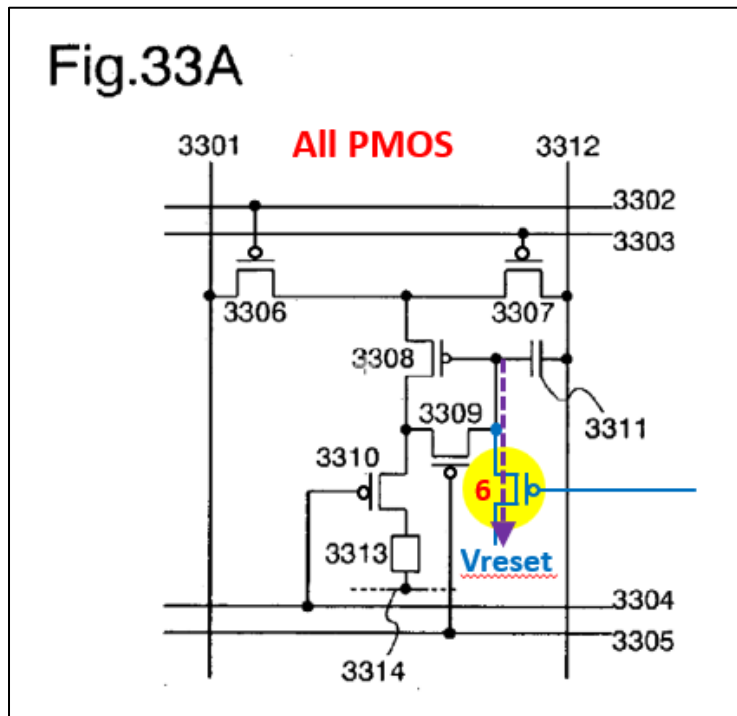
318. Claim 16 depends from Claim 15; as an initial matter, it was shown above that Kimura renders Claim 15 obvious.

319. Claim 16 further requires “a sixth transistor including a gate to which a scan signal just before the current scan signal is applied; a source coupled to the one terminal of the capacitor; and a drain to which an initialization voltage is applied.”

320. Most of the content of this dependent claim was already considered earlier, in the discussion of Claim 8 – where it was shown how other embodiments in Kimura, combined with the knowledge of a POSITA, would make it obvious (to a POSITA) to identify this sixth transistor from another embodiment in Kimura (the embodiment in Figure 16A) and combine it with the embodiment disclosed in Figure 33.

321. Claim 16 adds the further recitation (for the sixth transistor) of “a source coupled to the one terminal of the capacitor; and a drain to which an

initialization voltage is applied.” These are identified in an annotated, modified all-PMOS version of Figure 33A.



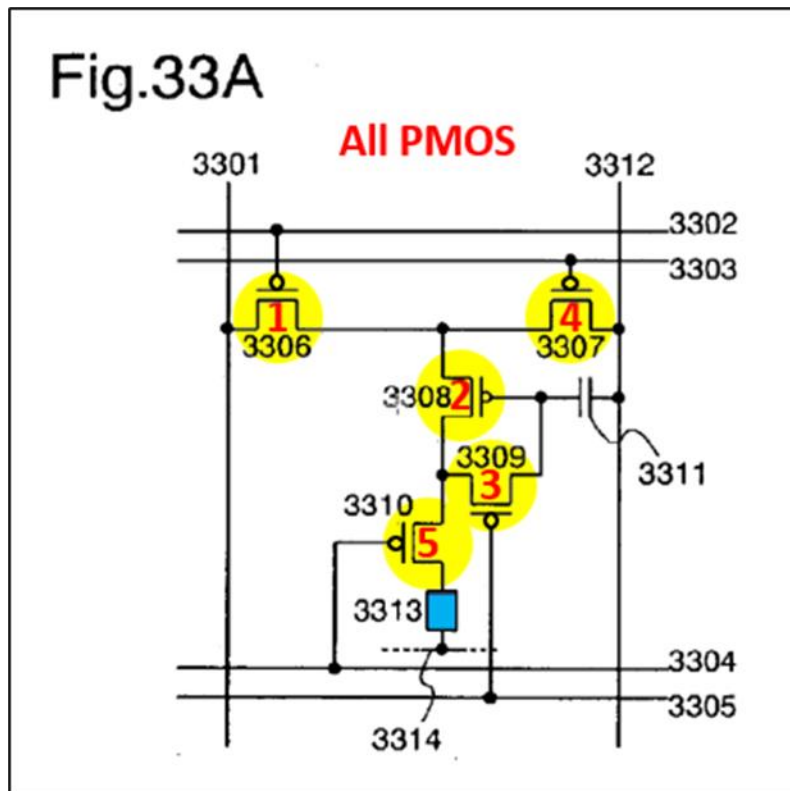
As was explained in the discussion of Claim 8 (Section XII.B), Kimura states that this transistor, when turned on, serves to “erase” or “reset” the voltage on the node that is connected to the gate of the second transistor (3308). In order for the charge to drain off of that node, current must flow in the direction shown in the figure above; as per the operational definition of “source” and “drain” explained in Section VII.A, the source of this sixth transistor is coupled to one terminal of the capacitor, while the drain has an initialization voltage applied to it. Further, what the ‘599 patent calls “the initialization voltage” is called the “reset voltage” in Kimura, while what the ‘599 patent calls “the initialization period” is called “the erasure period” in

Kimura; despite the different names, these are the same functional activities. In particular, Kimura refers to the “initialization voltage” as VReset (see Kimura [0425]) or an “erase” voltage in Figure 17A. These names (VReset and erase) are descriptive of the function being performed, which is to drain charge to a known default value when the sixth transistor is active. The actual voltage used for VReset is simply a design choice for the circuit designer (as long as VReset is low enough to drain the capacitor), but one obvious option is to use a fixed voltage such as a lower voltage rail. Another obvious option is disclosed in connection with Kimura Figures 16 and 17 where the drain of the reset transistor is connected to the light emitting signal (i.e., the second gate signal labeled 1604). See Kimura [0422]-[0427]. As shown in the timing diagram waveforms of Figure 16B, this signal is low (and thus serves as an initialization voltage) whenever the reset transistor is activated by the first gate signal 1604 (i.e., scan signal) for the “(i-1)th” row. *Id.* Either of these options, both of which would have been obvious to a POSITA, satisfy the “initialization voltage” limitation of Claim 16. By making this initialization voltage / reset voltage lower than the initial (i.e., programmed) voltage on the node that connects to gate of the second transistor, when the sixth transistor is turned on, charge will drain off of that node until its voltage is pulled down to the initialization voltage / reset voltage – at which point the initialization/erasure period will be completed.

322. Thus, Kimura renders obvious this claim of the ‘599 patent.

K. Independent Claim 17

323. Independent Claim 17 is substantially similar to independent Claim 7 (which was analyzed above in Section XII.A) and independent Claim 15 (which was analyzed above in Section XII.I). All three claims use the same circuit elements, connected together in the same way, and operating in the same way; in fact, even the transistor numbering used in Claim 17 is the same as the numbering scheme used in Claim 7 and Claim 15. Claim 17 most closely aligns with Claim 15 because, like Claim 15, the required gate/drain/source connections in Claim 17 mean that all five transistors in Claim 17 must be PMOS devices. As was explained in Section XII.A and Section XII.I, the details of the circuitry are disclosed in Kimura – as a reprise of Figure 33A of Kimura makes clear.



324. As was also explained in Section XII.A, it would have been obvious to a POSITA to convert this circuitry of Kimura into the all-PMOS form that is recited in Claim 7 and Claim 15 – using both the disclosure elsewhere in Kimura and the knowledge and experience of a POSITA (with the latter being explained via reference to other prior art references for confirmation). This is also the case with the recitations of Claim 17.

325. Thus, for substantially the same reasons as those disclosed with regard to Claim 7 and Claim 15, Kimura discloses Claim 17 of the ‘599 patent.

326. To simplify the element-by-element of Claim 17 that follows, as much as possible reference will be made to details that were already explained in Section

XII.A (where the claim elements of Claim 7 were analyzed) and Section XII.I (where the claim elements of Claim 15 were analyzed); the focus here will be on any lexicographical or material differences (with respect to Claim 7 and Claim 15) that need to be addressed with respect to Claim 17.

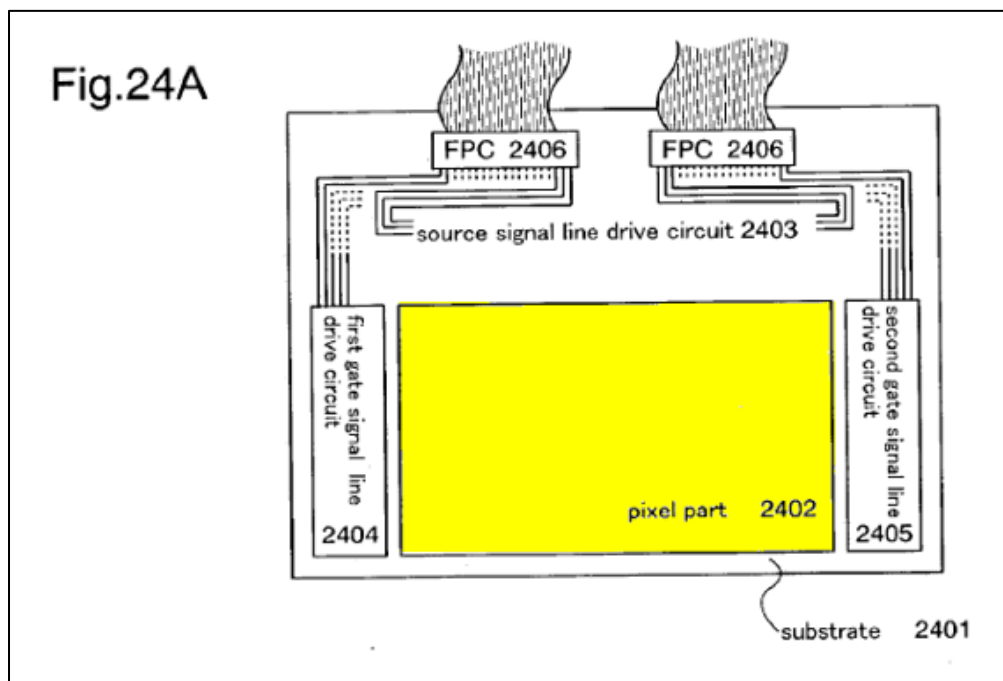
1. **[Claim 17 Preamble]: “A pixel circuit in an organic light emitting device having a plurality of data lines, a plurality of scan lines, a plurality of power lines, and a plurality of pixels each connected to one associated data line, scan line and power line of the plurality of data lines, scan lines and power lines, each pixel comprising:”**

327. As was the case with Claims 7, 14, and 15, I will be offering no opinion regarding whether or not the preamble of Claim 17 is limiting; I have been instructed by counsel for the Petitioner to assume that the preamble is limiting.

328. The first part of the preamble of Claim 17 (“A pixel circuit in an organic light emitting device”) is identical to the preamble of Claims 7, 14, and 15; thus, to the extent that the preamble of Claim 17 is limiting, Kimura discloses this part of this claim element of Claim 15 of the ‘599 patent.

329. The remainder of the preamble of Claim 17 adds in additional details involving structures by which a large number of pixels are used together in, e.g., a display. As (partially) explained in Section VII.B and VII.C, these are details that are generally known in the art; however, more specifically, these additional details are disclosed in Kimura.

330. In that vein, Kimura does not limit the disclosures to a single pixel; rather, Kimura discloses an “**active matrix**” forming a plurality of pixels. Kimura, [0001]; *see also id.*, [0476] (“The device [includes] **a plurality of pixels [] arranged in a matrix** shape over a substrate.”); [0487] (same); [0401] (discussing “pixels within a screen”), and [0708] (OLED screens used in “video cameras, digital cameras, ... notebook type personal computers, ... mobile telephones, ...”)). to provide one specific example, Kimura Figure 24A shows a pixel matrix (which is highlighted in yellow). Kimura [0476].



331. The circuit portions identified as 2403, 2404, and 2405 drive the “source signal line[s]” (which correspond to the “data lines” recited in the preamble of Claim 17), “first gate signal line[s]” (which correspond to the “scan lines” recited in the preamble of Claim 17), and “second gate signal line[s],” respectively, for the

pixel matrix. Kimura [0476]; *see also id.*, Figs. 24-27 (illustrating control circuitry that provides signals to the pixels). Even though Figure 24 does not expressly illustrate power supply lines, it is obvious (and would have been obvious) to a POSITA that the pixel matrix must be supplied with input power via power lines - since without input power, the circuit would simply not be able to function.

332. As was explained in Section VII.B.2, the array of pixels (in, e.g., a display) is organized into rows/lines for control purposes, and each row/line may be controlled by common signals. *See, e.g.*, Kimura, Figure 16 B and [0422]-[0430] (discussing the operation of rows of pixels). As one example, Kimura Figure 17A shows a “VDD” connection (i.e., a power supply), “data” signal input (i.e., a “data line”), and various control signals such as “Erase” and “Select” lines (i.e., scan lines) for each row. *See also* Kimura, [0655] (discussing the “V_{Data}” image signal on a data line); [0656] (discussing the V_{DD} power supply line); and [0659] (discussing “gate signal line[s]” (i.e., the claimed “scan lines”) for controlling rows of pixels).

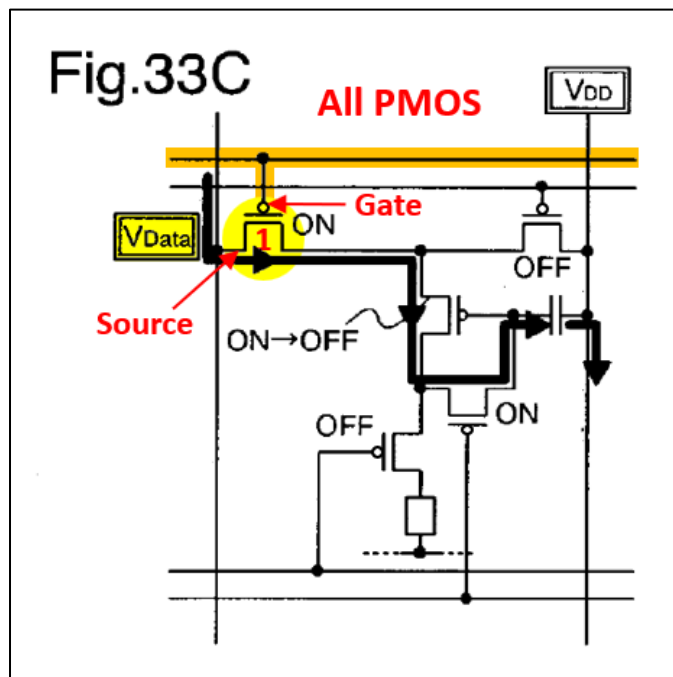
333. For these reasons, Kimura renders obvious the preamble of Claim 17 of the ‘599 patent.

2. [17a]: “a first transistor including a gate to which a current scan signal to be applied to the associated scan line is applied, and a source to which a data signal voltage from the data line is applied;”

334. Claim element 17[a] includes all of claim element 15[a] (discussed in Section XII.I.2), with the addition of the wording that is shown in bold italics here:

“a first transistor including a gate to which a current scan signal *to be applied to the associated scan line* is applied, and a source to which a data signal voltage *from the data line* is applied.” These additions provided further details regarding how these claimed operations are carried out – but do not change the details of the actual operations as described in claim element 15[a]; thus, the analysis presented with regard to claim element 15[a] applies completely and equally to this claim element.

335. First, it would be obvious (and would have been obvious) to a POSITA that the “data signal voltage” (V_{Data}) in Kimura Figure 33 is supplied from the data line – and, indeed, the name of the signal (V_{Data}) indicates that this signal is provided on a “data line.”



As can be seen in this annotated, all-PMOS version of Figure 33C, the first transistor is turned on as part of the programming period (which was explained in Section

VIII.B and Section VIII.C – as well as elsewhere in this Declaration), via a current flow used to charge up the node (and storing that charge on the capacitor) that is connected to the gate of the second transistor.

336. Further, as previously explained in Section XII.A.2, the “current scan [line] signal” of the ‘599 patent is the “first gate signal” in Kimura – and this signal is applied to the gate of the first transistor as highlighted in orange in the annotated figure above. As explained repeatedly above, the first transistor is turned on as part of the creation of a current flow path that leads to the node that is connected to the gate of the second transistor – so that the voltage at this node can be programmed (based on the Vdata input voltage and the threshold voltage compensation technique, as explained in Section VIII.C and in Section IX; see also the discussion in Section IX of the application of the input-signal-timing diagram of Figure 16B in the embodiment of Figure 33).

337. Thus, Kimura discloses this claim element of Claim 17 of the ‘599 patent.

3. [17b]: “a second transistor whose source is coupled to a drain of the first transistor;”

338. Claim element 17[b] is identical to claim element 15[b]; for the reasons explained in association with that claim element (in Section XII.I.3), Kimura discloses this claim element of Claim 17 of the ‘599 patent.

4. [17c]: “**a third transistor whose drain and source are connected between a gate and a drain of the second transistor, respectively;**”

339. Claim element 17[c] is identical to claim element 15[c] – with the exception of the addition of the word “respectively” to the end of this claim element. This addition is not material to the content of the claim element – but serves to further indicate that the drain of the third transistor is connected the gate of the second transistor, while the source of the third transistor is connected to the drain of the second transistor. The analysis presented earlier for claim element 15[c] (in Section XII.I.4) was carried out based on the arrangement detailed in that claim element being as detailed in the prior sentence.

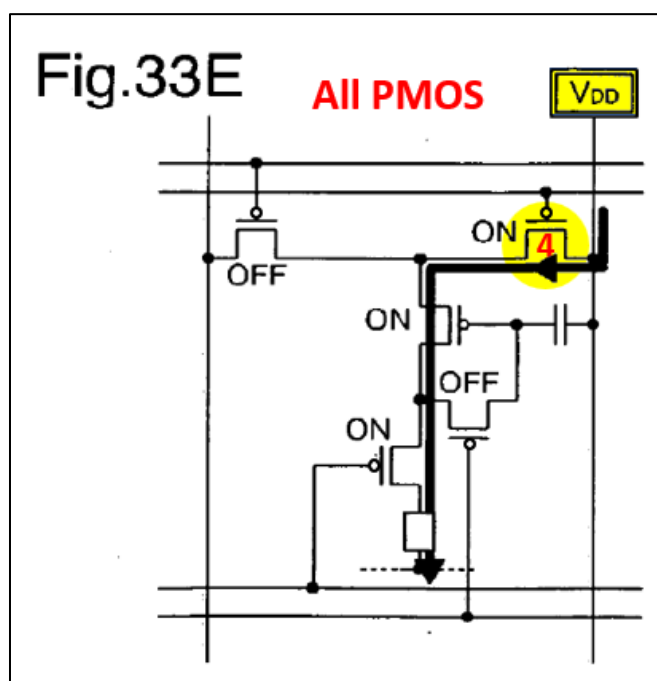
340. Thus, Kimura discloses this claim element of Claim 17 of the ‘599 patent.

5. [17d]: “**a fourth emitting transistor including a gate to which a current light-emitting signal is applied, a source to which a power supply voltage from the power line is applied, and a drain coupled to the source of the second transistor;**”

341. Claim element 17[d] is nearly identical to claim element 15[d] - with the only differences being some additional language that has been added to claim element 17[d] - as shown here in bold italics: “a fourth ***emitting*** transistor including a gate to which a current light-emitting signal is applied, a source to which a power supply voltage ***from the power line*** is applied, and a drain coupled to the source of the second transistor.”

342. That Kimura discloses claim element 15[d] was already explained in Section XII.I.5; thus, only these two instances of additional language need be addressed here.

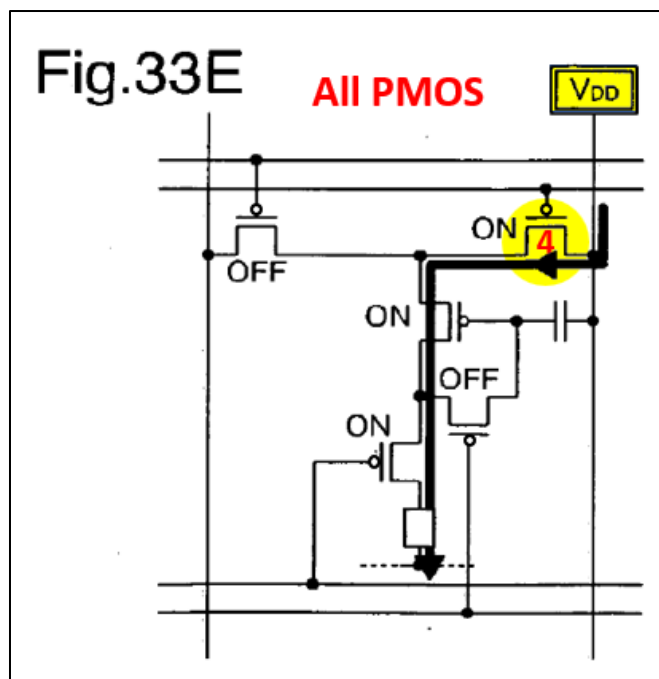
343. As per explanations provided earlier (in Section IX and elsewhere), the fourth transistor in Kimura can be identified in an annotated, all-PMOS version of Figure 33E.



344. In this claim element, the word “emitting” has been added to the description of the fourth transistor (i.e., “fourth *emitting* transistor”); the only other appearance of this phrase in the ‘599 patent is at 5:30-31. Further, no other “emitting transistors” are identified (e.g., there is no “first emitting transistor,” “second emitting transistor,” or “third emitting transistor”). Thus, it is obvious that the “fourth emitting transistor” is just another name for what is described elsewhere as

the “fourth transistor.” Further, as was explained in Section VIII.B, this transistor is turned on during the “emitting period” – and thus, this transistor can be characterized as being an “emitting transistor.”

345. Second, as noted above, this claim element also adds a phrase: “a source to which a power supply voltage *from the power line* is applied.” This is again readily explained by examining the annotated, all-PMOS version of Figure 33E of Kimura that was presented earlier.



The addition (vs. claim element 15[d]) is that the power supply voltage is applied “from the power line.” As this figure shows, a line runs from the power supply voltage (V_{DD}) to the source of the fourth (emitting) transistor. A POSITA would understand that a power supply voltage normally comes from a “power line” – and that is what a POSITA reading the disclosure of Kimura would understand. In

particular, the power supply voltage in Kimura Figs. 33B-33E is labelled “ V_{DD} ,” which is a common way of identifying a power supply. And a POSITA would understand the line to which the V_{DD} power supply is connected to be a “power line.” Thus, this additional detail appears in Kimura – as this addition (vs. claim element 15[d]) is just a further description here of what is the same structure.

346. Thus, Kimura renders obvious this claim element of Claim 17 of the ‘599 patent.

6. [17e]: “a fifth transistor including a gate to which the current light-emitting signal is applied, and a source coupled to the drain of the second transistor;”

347. This entirety of this claim element is contained in claim element 15[e] – with claim element 15[e] including (at the end) the further requirement of “and a drain coupled to one terminal of an electroluminescent element.” However, this additional requirement appended there has no effect on the other requirements of claim element 15[e]; thus, the analysis of claim element 15[e] (in Section XII.I.6) applies in the same way to this claim element.

348. Thus, Kimura renders obvious this claim element of Claim 17 of the ‘599 patent.

- 7. [17f]: “an electroluminescent element including one terminal coupled to the drain of the fifth transistor and the other terminal grounded;”**

349. Aside from a few minor-and-inconsequential changing of wording between them, this claim element is essentially identical to claim element 15[f] – which was already analyzed in Section XII.I.7.

350. Thus, Kimura renders obvious this claim element of Claim 17 of the ‘599 patent.

- 8. [17g]: “a capacitor including one terminal coupled to the gate of the second transistor, and the other terminal to which the power supply voltage from the power line is applied.”**

351. This claim element is nearly identical to claim element 15[g] – with the only difference being the addition of the phrase “from the power line”. This is an addition that also appears in claim element 17[d] with respect to claim element 15[d] – and was explained above with respect to claim element 17[d], this is an addition that provides an additional detail regarding the nature of the circuitry but is in fact describing the exact same (unchanged) circuitry.

352. As this addition is not material to the structure or operation of the circuitry, the analysis presented earlier for claim element 15[g] applies here in the same way.

353. Thus, Kimura discloses this claim element of Claim 17 of the ‘599 patent.

L. Dependent Claim 18

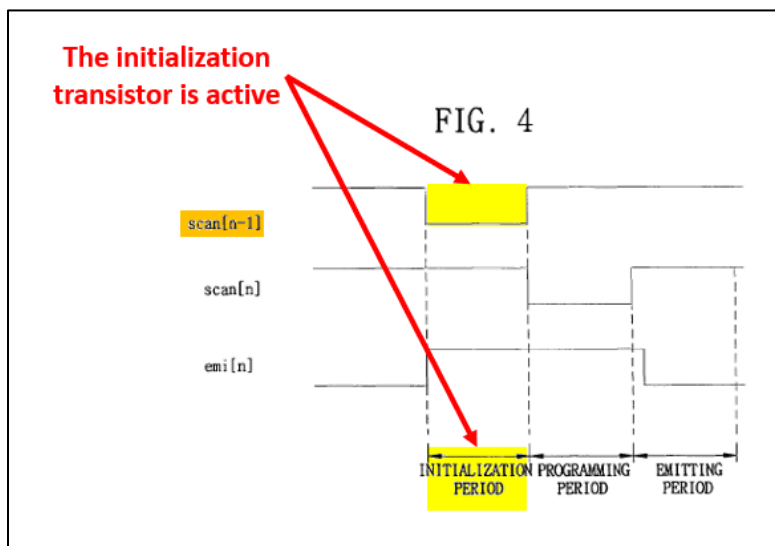
354. Claim 18 depends from Claim 18; as an initial matter, it was shown above that Kimura renders Claim 17 obvious.

355. Dependent Claim 18 further requires “a sixth transistor including a gate to which a scan signal to be applied to a scan line just before the associated scan line is applied, a source coupled to the one terminal of the capacitor, and a drain to which an initialization voltage is applied.” This claim is substantially identical to Claim 16 (which was analyzed in Section XII.J) – with the difference being that Claim 16 recites “a scan signal just before the current scan signal is applied” instead of “a scan signal to be applied to a scan line just before the associated scan line is applied.” However, it is obvious (and would be obvious to a POSITA) that these phrases are using slight-different language to describe the same thing; both of these phrases are describing the signal that is used to control the sixth transistor – which, as detailed in Section VIII.B and VIII.C, serves to initialize (i.e., erase) the voltage that was stored on the node that is connected to the gate of the second transistor during the prior programming period. Both Claim 16 and Claim 18 explain that the previous cycle of the scan signal (i.e., the scan signal applied to the immediately adjacent row/line of pixels) is used to turn on the sixth transistor – which serves to drain off the aforementioned charge that had be forced onto the node connected to the gate of

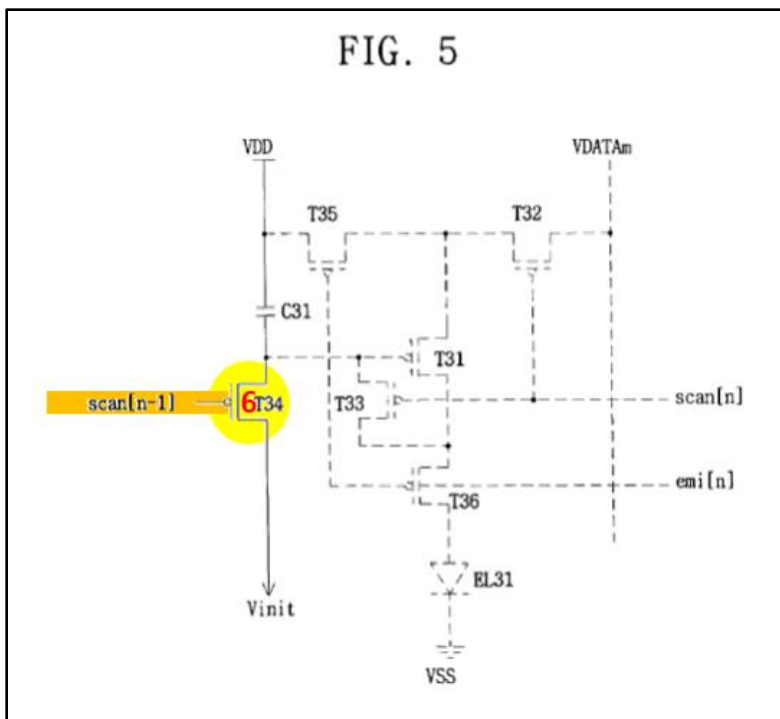
the second transistor (for programming that node) during the prior programming period).

356. As was explained in Section VIII.B, this signal is denoted as “scan[n-1]” in the claimed embodiment of the ’599 patent (Figure 3); further (as was also explained in Section VIII.B, in the signal waveforms that are used are presented in Figure 4, and the detailed operation of the initialization period (in the disclosed circuitry) is presented in Figure 5 (which shows the circuit-level functionalities of the initialization operation of the initialization period). *See also* the description provided in the ’599 patent at 7:15-27.)

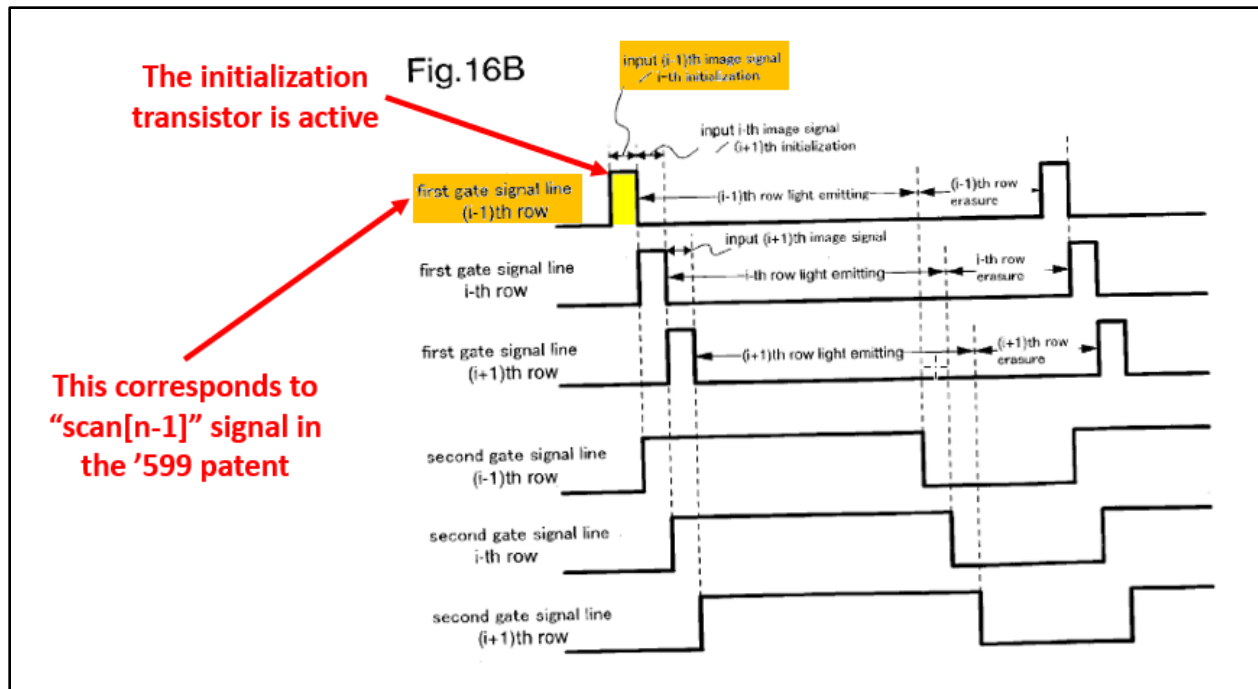
357. These operational details can be explained via annotated versions of Figure 4 and Figure 5 – where the relevant signal is highlighted in orange.²⁴



²⁴ Note that, as the initialization transistor is pMOS, it will be turned on when the “scan[n-1]” signal on the gate is pulled low.



358. In the same way, Kimura at Figure 16B shows that the “first gate signal line” (the scan signal) for the “(i-1)th row” (adjacent/previous row) controls and activates the initialization transistor (i.e., the “first gate signal line (i-1)th row” – and thus is the claimed “scan signal to be applied to a scan line just before the associated scan line is applied”). This is highlighted in an annotated version of Figure 16B of Kimura.



The black text in the original figure indicates that the “i-th initialization” (i.e., initialization of the i^{th} row) occurs according to the “input (i-1) image signal” (i.e., the scan signal for the previous/adjacent row).

359. The timing diagram in Figure 16B of Kimura uses high signal levels to turn transistors on – since the original embodiment in Kimura employs nMOS transistors. However, as was explained in Section IX and Section X, it would be an obvious modification to replace these nMOS switching transistors with pMOS switching transistors – and that Kimura actually states that this is a reasonable design choice that could be carried out (as a POSITA would understand) without undue experimentation and with a high probability of success. Further, both Kimura (Section X) and a representative textbook and contemporaneous patent (Sections VII.A.2 and X.A) provide a rather-obvious motivation to make such a change (i.e.,

the beneficial manufacturing process simplification that is inherent in using only one species of transistor (nMOS or pMOS) in the circuitry).

360. Therefore, the analysis presented earlier for Claim 16 applies in the same way here to Claim 18.

361. Thus, Kimura renders obvious Claim 18 of the '599 patent.

M. Independent Claim 1

362. Independent Claim 1 is quite similar to independent Claim 7; thus, for the reasons that are largely the same as those involving Claim 7 (and as will be explained in more detail below), Kimura renders Claim 1 unpatentable as obvious – for largely the same reasons as those already explained (in Section XII.A) for Claim 7. Both claims recite the same circuit elements (five transistors, a capacitor for controlling the driving transistor, and an electroluminescent element), connected together into the same circuit structure, and operated in the same way.

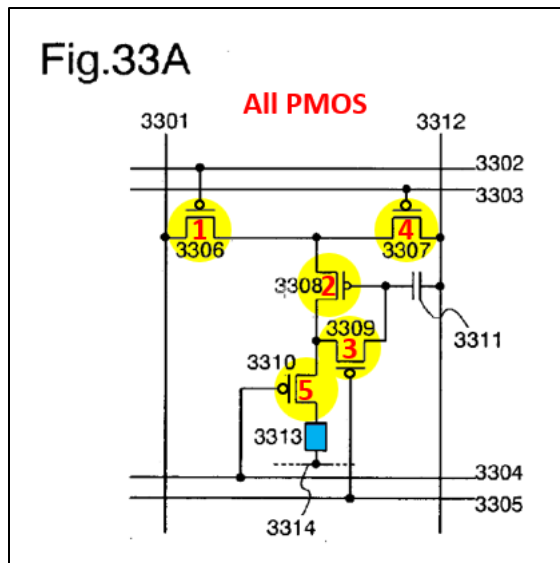
363. The main difference between Claim 1 and Claim 7 was mentioned in passing at the start of Section XII – where it was noted that Claim 1 cosmetically differs from Claim 7 (as well as from Claims 8 – 18) in that two of the transistors in Claim 1 are identified using different numbers than those used in Claim 7. The first, second, and third transistors of both claims use the same numbering scheme; however, Claim 1 does not have a “fourth transistor,” and thus has a “fifth transistor” and a “sixth transistor.” Because of this anomaly, the “fourth transistor in Claim 7”

is called the “fifth transistor” in Claim 1, and the “fifth transistor in Claim 7” is called the “sixth transistor” in Claim 1.

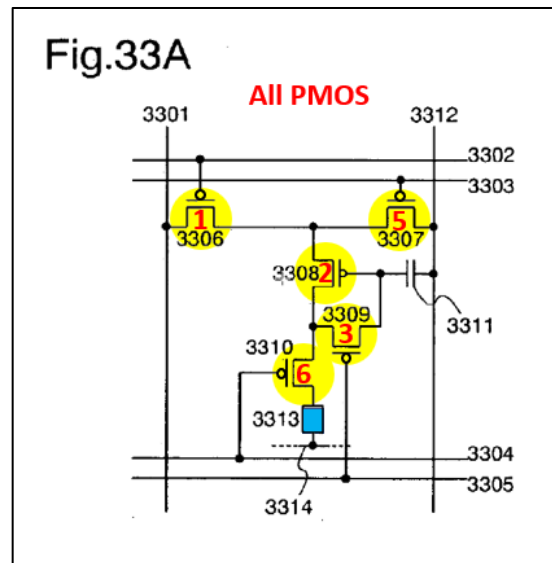
364. In order to provide a convenient tabulated reference, these differences in the transistor numbering between the two claims is provided this table.

Claim 7	Claim 1
First transistor	First transistor
Second transistor	Second transistor
Third transistor	Third transistor
Fourth transistor	Fifth transistor
Fifth transistor	Sixth transistor

365. Based on this mapping tabulation, a different figure for identifying the corresponding transistors in Kimura is required. The two images below show the Kimura Figure 33 (using the structural figure of the Figure 33 embodiment in Figure 33A (as explained in Section IX)), depicting the different transistor numberings (based on the table above) for comparison purposes (and for use in the discussion below).



CLAIM 7



CLAIM 1

Note again that the actual circuitry and components in Kimura Figure 33 are the same; the only difference here is the numbering assigned to the transistors, as per the table above. Thus, the “Claim 1” version of the transistor numbering will be used below, in the analysis of Claim 1 and its dependent claims.

366. As a final organizational note, in the analysis that follows, Claim 1 will only be compared (where necessary) to Claim 7. As has been noted earlier, most of the content of Claim 7 also appears in Claim 14, Claim 15 (and its dependent claim), and Claim 17 (and its dependent claim); thus, the correspondences between Claim 1 and Claim 7 will also appear in those other claims (and the related dependent claims).

1. [Claim 1 Preamble]: “A pixel circuit in an organic light emitting device, comprising:”

367. The preamble of Claim 1 is identical to the preamble of Claim 7.

368. Thus, for the reasons described for the preamble of Claim 7 (Section XII.A.1), Kimura renders obvious the preamble of Claim 1.

2. [1a]: “a first transistor for delivering a data signal voltage in response to a current scan line signal;”

369. Claim element 1[a] is identical to claim element 7[a].

370. Thus, for the reasons described for claim element 7[a] (Section XII.A.2), Kimura renders obvious this claim element of Claim 1 of the ‘599 patent.

3. [1b]: “a second transistor for generating a driving current depending on the data signal voltage delivered through the first transistor;”

371. Claim element 7[b] and claim element 1[b] use identical language to state that both claim elements require a “second transistor for [] generating a driving current.” Claim element 1[b] differs from claim element 7[b] in that claim element 1[b] also requires that the drive current “depend[s] on the data signal voltage delivered through the first transistor,” while claim element 7[b] states the requirement that the drive current is generated “in response to a programmed data signal when light is emitted.”

372. These, however, are different descriptions of the same thing, using different language – as they both are describing the (intentional) effect of the programming period on the emitting period; these details were explained in Section VIII.B and VIII.C. The language in claim element 7[b] explains that the voltage on the node that connects to the gate of the second transistor is programmed during the

programming period, and then the light emitted by the emitter during the emitting period is a direct function of this programmed voltage (i.e., “programmed data signal”) that was programmed to that node during the programming period. Claim element 1[b] describes the same structures and functionalities, but in a slightly different way – as the “the data signal voltage delivered through the first transistor” is delivered to the aforementioned node during the programming period, and once again it is this voltage that programs the drive current that will flow through the emitting current path (in the circuitry) during the emitting period.

373. Therefore, the analysis provided with respect to claim element 7[b] (Section XII.A.3) applies to this claim element as well.

374. Thus, Kimura renders obvious this claim element of Claim 1 of the ‘599 patent.

4. [1c]: “a third transistor for detecting and self-compensating threshold voltage deviation in the second transistor;”

375. This claim element describes the structure and functions of the “third transistor” when that transistor serves its function during the programming period (where the voltage on the node that connects to the gate of the second transistor is provided); the details of both the structure and function of the programming phase were explained in detail earlier (in Sections VIII.B and VIII.C).

376. For purposes here, it can be noted that this claim element combines portions of claim element 7[c] (“a third transistor for providing the data signal for

the second transistor” – which was analyzed in Section XII.A.4) and claim element 7[h] (“the third transistor connects the second transistor in the form of a diode...so that the second transistor detects and compensates its threshold voltage deviation in itself” – which was analyzed in Section XII.A.9). Taken together, this claim element is simply describing the same structures and functionalities of the programming period using different words – with, as mentioned, these structures and functionalities being identified in Kimura in the analysis of those two claim elements from Claim 7 (Section XII.A.4 and Section XII.A.9). In particular, although worded differently, claim elements 7[h] and 1[c] are both met by the same diode-connected configuration of second and third transistors that detect and self-compensate for threshold voltage deviation. The slightly different wording between the claims (i.e., claim element 7[h] says “the **second transistor** detects and compensates its threshold voltage deviation in itself” and claim element 1[c] says “a **third transistor** for detecting and self-compensating threshold voltage deviation in the second transistor”) is merely indicative of the fact that the **second and third transistors must work together** to detect and compensate for the threshold voltage deviation of the second transistor.

377. Therefore, Kimura renders obvious this claim element of Claim 1 of the ‘599 patent.

5. [1d]: “a fifth transistor for providing a power supply voltage for the second transistor in response to a current light-emitting signal;”

378. This claim element is nearly identical to claim element 7[e] – and the differences between this claim element and claim element 7[e] are in fact insubstantial.

379. First, as per the discussion earlier (at the outset of Section XII.M), the transistor-numbering scheme of Claim 1 differs from the transistor numbering scheme of Claim 7 – and, as per the helpful table provided along with that discussion, the “fifth transistor” in Claim 1 corresponds to the “fourth transistor” of Claim 7. Under that correspondence, the same circuit structure occurs in both this claim element and claim element 7[e] – and the related analysis of claim element 7[e] (Section XII.A.6) applies in the same way here.

380. Further, the language of this claim element differs from that of claim element 7[e] in two specific ways.

381. First, claim element 7[e] recites “**delivering** a power supply voltage,” but claim element 1[d] recites “**providing** a power supply voltage.” This difference in wording makes no practical difference – and the two highlighted words can be regarded as synonyms. Thus, the related analysis of claim element 7[e] (Section XII.A.6) applies in the same way here.

382. Second, this claim element states that power is supplied “in response to a current light-emitting signal,” while claim element 7[e] says that power is supplied “when the light is emitted.” Once again, this is not a substantive distinction when it comes to applying the Kimura reference. The reason is that “light is emitted” by Kimura’s circuit of Figure 33 “in response to a current light-emitting signal” (i.e. when the light-emitting signal is active). My analysis of Kimura’s “second gate signal” as the claimed “light-emitting signal” is set forth in connection with Claim 13. Accordingly, Kimura satisfies claim element 1[d] for the same reasons as claim element 7[e].

383. Thus, the related analysis of claim element 7[e] (Section XII.A.6) and claim 13 (Section XII.G) applies in the same way here.

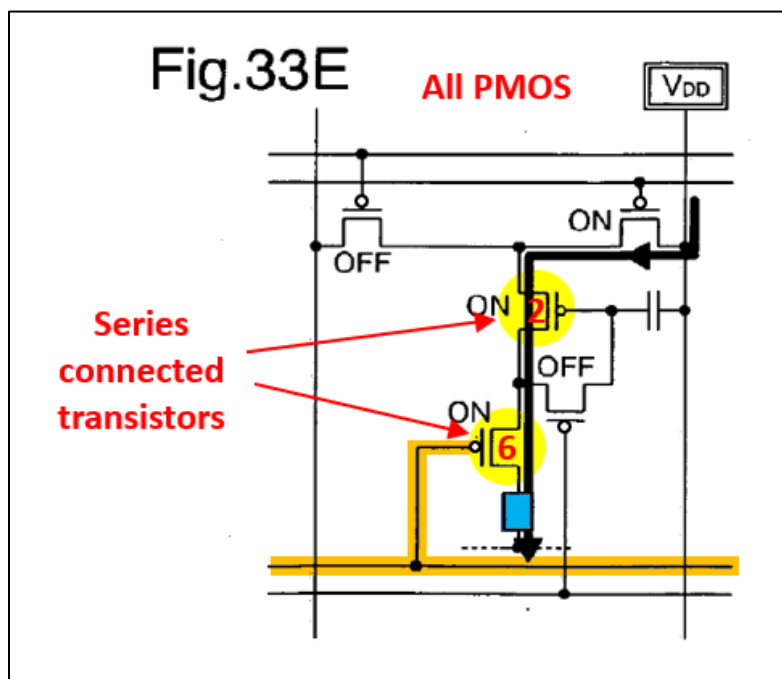
384. Thus, Kimura renders obvious this claim element of Claim 1 of the ‘599 patent.

6. **[1e]: “a sixth transistor which is coupled in series between the second transistor and an electroluminescent element and for providing the driving current for the electroluminescent element through the second transistor in response to the current light-emitting signal;”**

385. Claim elements 1[e] and 7[f] have many similarities, but are worded somewhat differently. However, the differences do not relate to either the recited structures or functionalities.

386. As an initial matter, as was explained at the outset of this section, the “sixth transistor” of Claim 1 corresponds to the “fifth transistor” of Claim 7. Thus, this particular transistor has already been analyzed in the discussion of claim element 7[f] (Section XII.A.7).

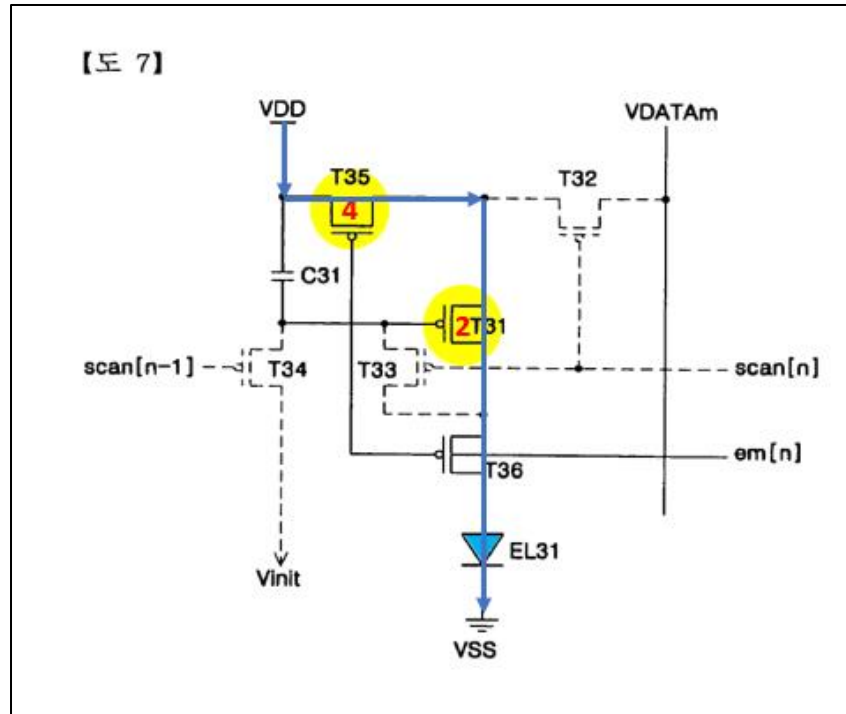
387. Further, the detail that “sixth transistor which is coupled in series between the second transistor and an electroluminescent element” was already explained in the background section regarding the ‘599 patent (Section VIII.B) and in the background section on Kimura (Section IX). The correspondence between Kimura and the ‘599 patent can be made readily-apparent by examining an annotated, all-PMOS version of Figure 33E of Kimura.



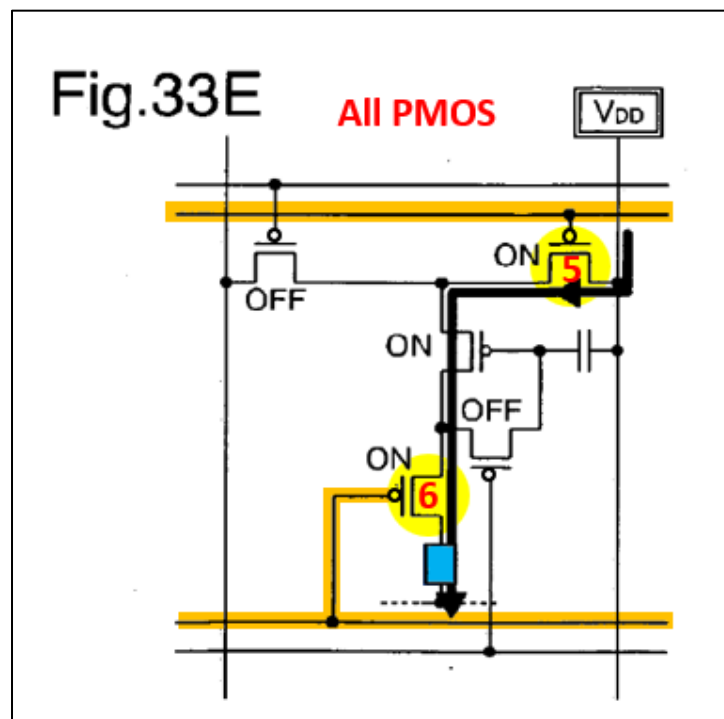
As can be seen, the “sixth transistor []” is coupled in series between the second transistor and an electroluminescent element.”

388. The remainder of this claim element discloses that the sixth transistor “provid[es] the driving current for the electroluminescent element through the second transistor in response to the current light-emitting signal.” The thick black arrow in Kimura Figure 33E (which is not an annotation, but is present in the figure in Kimura) shows current flow during the light emitting phase (the “emitting period” of the ‘599 patent). See Kimura, [0656]. As can be seen (and was explained in the background sections Section VIII.B and Section IX), the sixth transistor transparently provides the drive current (the level of which is set by the voltage that has been programmed onto the gate of the second transistor) to the electroluminescent element. As the sixth transistor is in the current-flow path of the emitting period, *and* is directly connected to the light-emitting element, the sixth transistor provides the driving current to the electroluminescent element.

389. A final aspect of this claim element is that these functions occur “in response to the current light-emitting signal.” As was explained in the background section regarding the ‘599 patent (Section VIII.B), in the circuitry of Figure 3 (and as further depicted in the functionality-figure Figure 7), the “current light-emitting signal” is the input signal *emi[n]*, which is provided in tandem to the gate of the fifth transistor and the gate of the sixth transistor.



In Figure 33 of Kimura, two separate lines are shown as providing the “current light-emitting signal” to the gates of the fifth transistor and the sixth transistor.



As was explained earlier (in Section XII.G), it would have been obvious (and would be obvious) to a POSITA that these two separate lines could be run in tandem (i.e., the same signal applied to both lines at the same times), or to simply use one line rather than two. See Kimura, Fig. 36 (showing common operational states for transistors 3608 and 3615). Thus, the orange signal line provides the current light-emitting signal (which is called “second gate signal” in Kimura). Thus, a POSITA would have found it obvious to use the “second gate signal” (current light-emitting signal) described in Kimura Figs. 16-17 (discussed at [0422]-[0429]) to activate the fifth and sixth transistors in Kimura Figure 33. See §VII.A.2 (discussing active-low signal scheme for pMOS devices).

390. Therefore, Kimura discloses all of the parts of this claim element – in the various locations in this Declaration, where the details are explained.

391. Thus, Kimura renders obvious this claim element of Claim 1 of the ‘599 patent.

7. [1f]: “a capacitor for storing the data signal voltage delivered to the second transistor”

392. This claim element is substantively the same as claim element 7[d] (which was analyzed in Section XII.A.5). There is a slight difference in language between Claim 1 (“**storing** the data signal voltage **delivered to** the second transistor”) and Claim 7 (“**maintaining** the data signal voltage **programmed onto** the second transistor”); however, as per the background discussion regarding the structure and

operation of the circuitry disclosed in the ‘599 patent (Section VIII.B and Section VIII.C), once again these minor difference in wording are immaterial – as the structures and functionalities described in this claim element and claim element 7[d] are identical.

393. In the first instance, “storing” and “maintaining” describe the same functionality – since, as this involves the charge that is programmed onto a node, that charge is stored there and maintained there by (as explained in Section VIII.B and Section VIII.C) isolating that node and storing the charge involved on a capacitor.

394. In the second instance, the terms “delivered to” and “programmed onto” also describe the same thing – since, as per the explanation of the programming period that was provided in Section VIII.B and Section VIII.C), the data signal voltage is delivered to the node connected to the gate of the second transistor, so that the appropriate (threshold-voltage-compensated) data signal voltage can be created (i.e., programmed) there.

395. Thus, the analysis of claim element 7[d] that was presented earlier (in Section XII.A.5) applies directly here as well.

396. Thus, Kimura renders obvious this claim element of Claim 1 of the ‘599 patent.

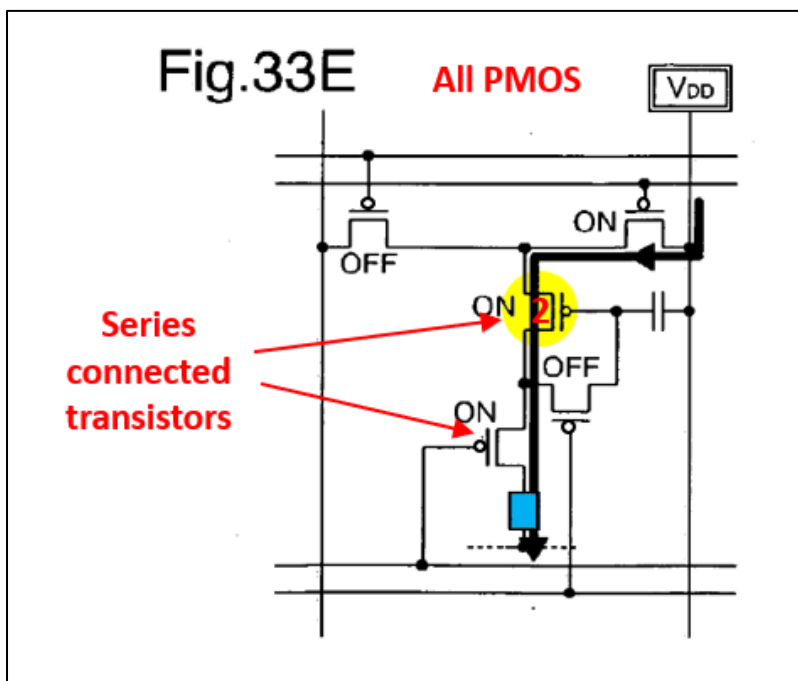
8. [1g]: “wherein the electroluminescent element emits²⁵ light corresponding to the driving current generated through the second transistor.”

397. This claim element is essentially identical to claim element 7[g] (which was discussed in Section XII.A.8) – with the exception that claim element 1[g] states that the driving current is “generated through the second transistor,” while claim element 7[g] states that the driving current is “delivered through the fifth transistor” (which is the “sixth transistor” in Claim 1).

398. As was explained in the background section regarding the ‘599 patent (Section VIII.B and Section VIII.C), these differences are merely excerpted descriptions of two different functionalities that are both active during the emitting period – that is, both are active, even if only one in particular is mentioned in a given piece of wording. As explained in Section VIII, the during the emitting period, the fourth transistor and fifth transistor (which is called the sixth transistor of Claim 1) are both turned on – so that a current flow path is created between the high (V_{DD}) rail and the low rail (on the low side of the light-emitting element) by the second transistor; thus, the driving current from the second transistor is “delivered through the fifth transistor,” as per claim element 7[g] and its analysis. *At the same time* (as is detailed in the complete description of the emitting phase as presented in Section

²⁵ This spelling error is present in the ‘599 patent.

VIII), the magnitude of that driving current is being determined by the voltage that has been programmed onto the gate of the second transistor; thus this driving current (by setting its magnitude) is “generated through the second transistor.” *See, e.g.*, Kimura, [0359] (discussing brightness levels that vary according to driving current). That this functionality is also present in the same way in Kimura (see Figure 33E below) as was explained in the background section on Kimura (Section IX), and in the specific analysis of this functionality of the second transistor that was provided with regard to claim element 7[b] (Section XII.A.3).



399. Thus, all of these parts of these claim elements have been previously analyzed with regard to claim element 7[g] and claim element 7[b].

400. Thus, Kimura renders obvious this claim element of Claim 1 of the ‘599 patent.

N. Dependent Claim 2

401. Claim 2 depends from Claim 1; as an initial matter, it was shown above that Kimura renders Claim 1 obvious.

402. Dependent Claim 2 further requires “a fourth initialization transistor for discharging the data signal voltage stored in the capacitor in response to a scan signal just before the current scan signal.” This claim element is substantially identical to Claim 8 - with two minor differences.

403. As per the discussion at the outset of this section, the “fourth transistor” in Claim 2 (as in Claim 1) is called the “sixth transistor” in Claim 8. Additionally, Claim 8 recites that the initialization transistor discharges the capacitor “in response to a scan signal just before the current scan signal ***upon initialization***” – where these last two words do not appear in Claim 2. Both Claim 2 and Claim 8 involve what the ‘599 patent describes (as explained in Section VIII.B) as the “initialization period.” Thus, these two added words add no content – as it is implicit that as the disclosures of Claim 8 involve the same structures, arranged in the same way, and performing the same functions, Claim 8 is also operational “upon initialization.”

404. Thus there is no material difference between Claim 8 and Claim 2 – and the discussion of Claim 8 (Section XII.B) applies equally to Claim 2.

405. Thus, Kimura renders obvious Claim 2 of the ‘599 patent.

O. Dependent Claim 3

406. Claim 3 depends from Claim 1; as an initial matter, it was shown above that Kimura renders Claim 1 obvious.

407. Dependent Claim 3 further requires that “the first transistor is composed of a PMOS transistor including a gate to which the current scan line signal is applied, a source to which the data signal voltage is applied, and a drain coupled to the second transistor.” Claim 3 is identical to Claim 9 – and therefore the analysis provided earlier for Claim 9 (Section XII.C) applies identically here.

408. Thus, Kimura renders obvious Claim 3 of the ‘599 patent.

P. Dependent Claim 4

409. Claim 4 depends from Claim 1; as an initial matter, it was shown above that Kimura renders Claim 1 obvious.

410. Dependent Claim 4 further requires that “the second transistor is composed of a PMOS transistor including a gate coupled to one terminal of the capacitor, a source coupled to the first transistor, and a drain coupled to the electroluminescent element.” Claim 4 is identical to Claim 10 – and therefore the analysis provided earlier for Claim 10 (Section XII.D) applies identically here.

411. Thus, Kimura renders obvious Claim 4 of the ‘599 patent.

Q. Dependent Claim 5

412. Claim 5 depends from Claim 4, which depends from Claim 1; as an initial matter, it was shown above that Kimura renders both Claim 1 and Claim 4 obvious.

413. Dependent Claim 5 further requires that “the third transistor is composed of a PMOS transistor including a gate to which the current scan signal is applied, and a drain and a source which are coupled to the gate and the drain of the second transistor, respectively, so that the third transistor connects the second transistor in the form of a diode in response to the current scan signal to self-compensate a threshold voltage of the second transistor.” Claim 5 is identical to Claim 11 – and therefore the analysis provided earlier for Claim 11 (Section XII.E) applies identically here.

414. Thus, Kimura renders obvious Claim 5 of the ‘599 patent.

R. Dependent Claim 6

415. Claim 6 depends from Claim 1; as an initial matter, it was shown above that Kimura renders Claim 1 obvious.

416. Dependent Claim 6 further requires “a voltage source for providing the data signal voltage through the first transistor for the second transistor.” Claim 6 is identical to Claim 12 – and therefore the analysis provided earlier for Claim 12 (Section XII.F) applies identically here.

417. Thus, Kimura renders obvious Claim 6 of the '599 patent.

XIII. SECONDARY CONSIDERATIONS

418. I am not aware of any secondary considerations of non-obviousness that are relevant to the challenged claims. If I later become aware of arguments of any secondary consideration, I may assess those arguments when they arise, in order to form opinions regarding their correctness; I reserve the right to file supplemental declarations should such circumstances occur.

XIV. CONCLUSION

419. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and thus such actions may compromise the validity of the IPR Petition. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

420. I declare under penalty of perjury that the foregoing is true and correct.

Executed this 9th day of June, 2023 in Fletcher, Vermont.



Daniel Foty, Ph.D.

APPENDIX A

SUMMARY

Dr. Foty has more than 30 years of engineering and management experience in the mainstream of the technology industry. During this time, he has worked in semiconductor physics, device design, process integration, modeling/simulation (process, device, and circuit), circuit design/analysis, and wireless communications. After seven years at the microelectronics unit of IBM, he founded his own consulting firm, Gilgamesh Associates, LLC, which works in very demanding areas of technology design and development such as analog, mixed-signal, RF, signal processing, wireless communications, and ultra-low-power design.

Dr. Foty is also an advisor to the Tallinn University of Technology (Estonia) and the University of Pretoria (South Africa). He is also the author of *MOSFET Modeling with SPICE: Principles and Practice*, the more-recent *Moore's Law: The Untold Story*, and several other books. He has also authored well over 100 journal articles and conference presentations, and is a frequent plenary (keynote) speaker at major international conferences throughout the world. He is also a licensed pilot and aircraft owner, possesses both an instrument rating and a seaplane rating, and is a registered "angel pilot" with Patient Airlift Services.

Expertise

- Analog/Mixed-Signal/RF CMOS
- CMOS Integrated Circuit Design
- IC Modeling/Simulation
- CMOS Technology and Process Integration
- Semiconductor Manufacturing/Fabrication
- Nanotechnology
- Design Automation (EDA) Software
- Semiconductor Memory (DRAM, SRAM, Flash)
- Semiconductor Physics
- RF/Radio Technology, Wireless Networks, and Wireless Communications
- Power Management
- Digital Communications, Signal Integrity, and Electromagnetic Interference
- Cryogenic Electronics

PROFESSIONAL EXPERIENCE

1994 to Present Gilgamesh Associates, LLC
President

- Analysis of analog/mixed-signal/RF CMOS circuits
- New technologies in high-speed wireless data communications
- Specialized process-design-kits (PDKs) for circuit design/simulation
- Foundry interfacing for fabless IC design companies
- Professional education via short courses and lectures
- Litigation support in various aspects of the integrated circuit industry

1988 to 1994 IBM Microelectronics Division
Scientist/Engineer

- Process integration, device design, semiconductor/IC physics
- Process and device simulation; circuit simulation
- Process and device integration for memory and logic technologies
- Process-design-kits (PDKs) for circuit simulation
- Spearheaded initial IBM foray into OEM foundry market; responsible for all "external customer" PDKs and support/interfacing; business grew from nothing to \$66M in revenue in first year.

EDUCATION

Ph.D., Materials Science, University of Vermont, 2001
MS, Electrical Engineering, University of Illinois, 1985
BS, Physics and Chemistry, Bates College, 1983

LITIGATION RELATED EXPERIENCE

Dr. Foty has served as a testifying expert, and provided declarations, expert reports, trial testimony, and arbitration-hearing testimony for cases that have touched on the complete spectrum of semiconductor/electronics engineering issues, electronic design automation software, wireless technology, contract interpretations and business processes, and prior art searches in both patents and the public-domain literature. He has also served as a consulting expert. Dr. Foty has been deposed some thirty times, and has testified at trial six times. Below are matters in which he has written expert reports and given testimony either at deposition, trial, or before an arbitration panel.

Type of Matter: *Inter Partes* review involving power conversion technology in solar power systems
Law Firm: Sheridan Ross LLP, Denver, Colorado
Case Name: SolarEdge Technologies, Ltd. v. Koolbridge Solar, Inc.
Represented: Patent holder
Case Number: IPR2022-00007, -00010, -00013
Filing Date: 10/11/2021, 10/11/2021, 10/8/2021
Court: Patent Trial and Appeal Board
Disposition: Prepared three declarations supporting the patent holder; deposed; ongoing.
Date: June 2022 – present.

Type of Matter: Patent infringement involving wireless communications technology
Law Firm: Folio Law Group, LLP, Seattle, Washington
Case Name: Dali Wireless v. Corning
Represented: Patent holder
Case Number: 6:20-cv-00827-ADA
Filing Date: 10/22/2020
Court: US District Court District of the Western District of Texas
Disposition: Prepared an expert report, deposed; ongoing.
Date: November 2021 – present.

Type of Matter: Patent infringement involving integrated circuit layout for lithographic control
Law Firm: Jones Day LLP, Chicago, Illinois
Case Name: NXP Semiconductors v. Impinj
Represented: Plaintiff
Case Number: 2:20-cv-01503-RSM-SKV337-TA-1272
Filing Date: 10/7/2020
Court: US District Court of the Western District of Washington,
Disposition: Ongoing.
Date: November 2021 – present.

Type of Matter: Patent infringement involving integrated circuit technology
Law Firm: Jones Day LLP, Washington DC (ITC matter)
Case Name: MediaTek v. NXP Semiconductors
Represented: Respondent
Case Number: 337-TA-1272
Filing Date: 6/21/2021
Court: International Trade Commission
Disposition: Ongoing.
Date: April 2021 – present.

Type of Matter: Patent infringement involving portable vehicle battery jump starters
Law Firm: Fox Rothschild LLP, Philadelphia, Pennsylvania (ITC matter)
Case Name: The Noco Company v. Deltran Global
Represented: Respondent
Case Number: 337-TA-1256
Filing Date: 1/19/2021
Court: International Trade Commission
Disposition: Prepared an expert report; deposed; plaintiff withdrew complaint against Deltran.
Date: June 2021 – November 2021.

Type of Matter: Patent infringement involving integrated circuit technology and signal integrity
Law Firm: Jones Day LLP, Chicago, Illinois
Case Name: WSOU v. Xilinx
Represented: Respondent
Case Number: 1:20-cv-01228-CFC; 1:20-cv-01229-CFC
Filing Date: 09/16/2020
Court: US District Court District of Delaware
Disposition: Ongoing.
Date: April 2021 – present.

Type of Matter: Patent infringement involving wireless communications technology
Law Firm: Folio Law Group, LLP, Seattle, Washington
Case Name: Dali Wireless v. JMA
Represented: Patent holder
Case Number: 1:19-cv-02367-RGA
Filing Date: 12/30/2019
Court: US District Court District of Delaware
Disposition: Settled.
Date: March 2021 – November 2021.

Type of Matter: Patent infringement involving wireless communications technology

Law Firm: Folio Law Group, LLP, Seattle, Washington

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Case Name: Dali Wireless v. Commscope
Represented: Patent holder
Case Number: 1:19-cv-00952
Filing Date: 5/22/2019
Court: US District Court District of Delaware
Disposition: Prepared an expert report; deposed; ongoing.
Date: March 2021 – present.

Type of Matter: Patent infringement involving integrated circuit technology (ITC matter)
Law Firm: Troutman Pepper LLP, Boston, Massachusetts
Case Name: Tela v. Intel
Represented: Patent holder
Case Number: 337-TA-1246
Filing Date: 12/18/2020
Court: International Trade Commission
Disposition: Settled; this includes all prior disputes between the parties
Date: March 2021 – April 2021.

Type of Matter: Patent infringement involving wireless battery charging and discharging
Law Firm: Feinberg Day Kramer Alberti Limtonkovich & Belloli LLP
Case Name: Garrity Power Services v. Samsung
Represented: Patent holder
Case Number: 2:20-cv-00269-JRG
Filing Date: 08/17/2020
Court: US District Court Eastern District of Texas
Disposition: Case dismissed by the Court
Date: October 2020 – March 2022.

Type of Matter: *Inter Partes* review involving wireless battery charging and discharging
Law Firm: Spencer Fane LLP, Plano, Texas
Case Name: Samsung v. Garrity Power Services
Represented: Patent holder
Case Number: IPR2021-00389
Filing Date: 12/31/2020
Court: Patent Trial and Appeal Board
Disposition: Prepared a declaration; PTAB denied institution.
Date: October 2020 – July 2021.

Type of Matter: Patent infringement involving MOS transistor design and MOS transistor manufacturing processes
Law Firm: Fish & Richardson LLP, Boston, Massachusetts
Case Name: Innovative Foundry Technologies v. SMIC, Broadcom, Cypress Semiconductor, and Dish Network
Represented: Respondents

Case Number: 6:19-cv-00719-ADA
Filing Date: 12/20/2019
Court: US District Court Western District of Texas
Disposition: Settled
Date: June 2020 – April 2021.

Type of Matter: Patent infringement involving digital communications integrated circuit technology
Law Firm: Morrison & Foerster LLP, Los Angeles, California
Case Name: Analog Devices v. Xilinx
Represented: Respondent
Case Number: 1:19-cv-02225-RGA
Filing Date: 12/05/2019
Court: US District Court District of Delaware
Disposition: Ongoing.
Date: April 2020 – present.

Type of Matter: Patent infringement involving integrated circuit technology
Law Firm: Pepper Hamilton LLP, Boston, Massachusetts
Case Name: Intel v. Tela
Represented: Respondent
Case Number: 3:18-cv-02848-WHO
Filing Date: 05/15/2018
Court: US District Court Northern District of California
Disposition: Prepared two expert reports; deposed; matter settled.
Date: March 2019 – April 2021.

Type of Matter: Patent infringement involving integrated circuit technology (ITC matter)
Law Firm: Mintz, Levin, Cohn, Ferris, Glovsky and Popeo, P.C., Boston, Massachusetts
Case Name: Globalfoundries v. TSMC
Represented: Patent holder
Case Number: 337-TA-1177
Filing Date: 08/26/2019
Court: International Trade Commission
Disposition: Settled.
Date: August 2019 – October 2019.

Type of Matter: *Inter Partes* review involving wireless/RF technology
Law Firm: Jones, Day LLP, Cleveland, Ohio
Case Name: Intel v. Qualcomm
Represented: Patent holder
Case Number: IPR2019-00128, IPR2019-00129, IPR2019-00047, IPR2019-00048, IPR2019-00049
Filing Date: 11/8/2018
Court: Patent Trial and Appeal Board

Disposition: Prepared five declarations supporting patent owner responses;
deposed; PTAB upheld all challenged claims of the patent as valid.
Date: June 2019 – July 2020.

Type of Matter: Patent infringement involving integrated circuit technology
Law Firm: Pepper Hamilton LLP, Boston, Massachusetts
Case Name: Tela v. Intel
Represented: Patent holder
Case Number: 337-TA-1148
Filing Date: 12/19/2018
Court: International Trade Commission
Disposition: Prepared two declarations supporting claim construction; prepared
an expert report; deposed; testified at the hearing/trial in December
2019.
Date: March 2019 – December 2019.

Type of Matter: Patent infringement involving RF/wireless technology
Law Firm: Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name: Qualcomm v. Apple
Represented: Patent holder
Case Number: 3:17-cv-02402-CAB-MDD
Filing Date: 12/29/2017
Court: US District Court Southern District of California
Disposition: Settled.
Date: January 2018 – December 2018.

Type of Matter: Patent infringement involving RF/wireless technology
Law Firm: Quinn Emanuel Urquhart & Sullivan LLP, New York, New York
Case Name: Qualcomm v. Apple
Represented: Patent holder
Case Number: 337-TA-1093
Filing Date: 7/7/2017
Court: International Trade Commission
Disposition: Prepared two expert reports regarding RF-IC/wireless technology;
deposed; testified at the hearing/trial in September 2018.
Date: January 2018 – September 2018.

Type of Matter: Patent infringement involving integrated circuit technology and
printed-circuit board technology
Law Firm: Dovel and Luner, LLP, Santa Monica, California
Case Name: X2Y v. Intel
Represented: Patent holder
Case Number: 3:18-cv-01394-HZ
Filing Date: 07/25/2018
Court: US District Court District of Oregon
Disposition: Prepared a declaration supporting claim construction; deposed;
case settled.

Date:	June 2017 – December 2019.
Type of Matter:	Patent infringement involving integrated circuit technology
Law Firm:	Jones, Day LLP, San Francisco, California, and Slater Matsil LLP, Dallas, Texas
Case Name:	IPBridge v. Xilinx
Represented:	Respondent
Case Number:	3:17-cv-06376-JD
Filing Date:	11/01/2017
Court:	US District Court Northern District of California
Disposition:	Settled.
Date:	February 2017 – February 2019.
Type of Matter:	Patent infringement involving analog circuits
Law Firm:	Covington & Burling LLP, San Diego, California
Case Name:	Tessera v. Broadcom
Represented:	Patent holder
Case Number:	1:16-cv-00380-LPS-CJB
Filing Date:	05/23/2016
Court:	US District Court District of Delaware
Disposition:	Settled.
Date:	December 2016 – December 2017.
Type of Matter:	Patent infringement involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	Synopsys v. ATopTech
Represented:	Patent holder
Disposition:	Prepared an expert report; deposed; matter was suspended when ATopTech filed for Chapter 11 bankruptcy.
Date:	June 2016 – March 2017.
Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology for wireless communications
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Ericsson v. TCL
Represented:	Plaintiff
Disposition:	Prepared an expert report regarding the costs and timelines associated with the development of integrated circuits for wireless communications, and the related difficulties encountered; trial was stayed when an IPR proceeding began, matter has since ended.
Date:	November 2015 – March 2016.
Type of Matter:	<i>Inter Partes</i> review involving integrated circuit design methods and integrated circuit design-automation software
Law Firm:	Jones, Day LLP, Cleveland, Ohio
Case Name:	ATopTech v. Synopsys

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Represented:	Patent holder
Disposition:	Prepared two declarations; deposited.
Date:	November 2014 – January 2016.
Type of Matter:	<i>Inter Partes</i> review involving a semiconductor flash memory technology patent
Law Firm:	Aka Chan LLP, Santa Clara, California
Case Name:	Silicon Motion Technology Corp. v. Phison Electronics Corp.
Represented:	Petitioner
Disposition:	Prepared a declaration; deposited; hearing before the PTAB in September 2014, PTAB ruled completely in Petitioners' favor
Date:	May 2014 – September 2014.
Type of Matter:	Patent infringement involving integrated circuit design
Law Firm:	Bragalone, Conroy, PC, Dallas, Texas
Case Name:	HSM v. Elpida Memory et al. (was HSM v. Fujitsu et al.)
Represented:	Plaintiff
Disposition:	Prepared numerous declarations and two expert reports; deposited; all respondents eventually settled.
Date:	February 2012 – February 2016.
Type of Matter:	Patent infringement involving integrated circuit process/manufacturing technology (ITC matter)
Law Firm:	McKool Smith, LLP, Dallas, Texas
Case Name:	Samsung v. Ericsson
Represented:	Defendant
Disposition:	Was assigned one patent in a larger matter, having done much original engineering work on the technology in question; produced extensive background prior art (having created much of it), demonstrated that the accused technology clearly did not practice the teachings of the patent, and clearly showed that the aforementioned prior art would call the patent's validity seriously into question; plaintiff dropped that patent from the action.
Date:	January 2013 – May 2013.
Type of Matter:	Patent infringement involving integrated circuit design, with a focus on RF-ICs for wireless communications
Law Firm:	Antonelli, Harrington, & Thompson, LLP, Houston, Texas
Case Name:	Semiconductor Ideas to the Market, BV v. Texas Instruments et al.
Represented:	Plaintiff
Disposition:	Prepared a declaration for pre-hearing; major defendant (Qualcomm) settled following this expert's examination of their Confidential Business Information (CBI) in June, 2012; other defendants settled shortly thereafter.
Date:	May 2012 – August 2012.
Type of Matter:	Bond forfeiture proceeding (ITC matter)

Law Firm: Adduci, Mastriani, & Schaumberg, LLP, Washington, D.C.
Case Name: Tessera v. Freescale
Represented: Plaintiff
Disposition: Following unfavorable ITC ruling, respondent argued that posted bond (pending final disposition) should be returned to them; prepared a declaration for hearing; ITC ruled against respondent, who then agreed to cease litigation and forfeit the bond.
Date: April 2012 – October 2012.

Type of Matter: Theft of trade secrets involving integrated circuit design, manufacturing, and characterization technology
Law Firm: Shore, Chan, Bragalone, and DePumpo, LLP, Dallas, Texas
Case Name: Xicor v. SST
Represented: Plaintiff
Disposition: Prepared a declaration for hearing regarding plaintiff's identification of its trade secrets; following favorable ruling on this, defendant agreed to settle on terms favorable to the plaintiff
Date: February 2012 – September 2012.

Type of Matter: Patent infringement in integrated circuit substrates (ITC matter)
Law Firm: Alston + Bird, LLP, Atlanta, Georgia
Case Name: X2Y v. Intel
Represented: Plaintiff
Disposition: Consulted on technology involved
Date: August 2011 – August 2012.

Type of Matter: Theft of trade secrets involving design of power management integrated circuits (ITC enforcement proceeding)
Law Firm: Alston + Bird, LLP, Menlo Park, California
Case Name: Richtek v. uPI, and Sapphire Technology
Represented: Plaintiff
Disposition: Prepared an expert report and a supplemental expert report; deposed; testified at hearing/trial; subsidiary respondent Sapphire settled and exited the case shortly before trial.
Date: June 2011 – March 2012; follow-on district/superior court cases temporarily stayed, but pending.

Type of Matter: Patent infringement in switching power supplies
Law Firm: McDermott, Will & Emery, LLP, Miami, Florida
Case Name: Power Integrations, Inc. v. Fairchild Semiconductor International, Inc.
Representing: Defendant
Disposition: Presented the tutorial at the Markman hearing in San Jose, California (Northern District of California) in March; matter ongoing, but no longer involved.
Date: December 2010 – March 2011.

Type of Matter: Patent infringement in the power management methodologies of portable/mobile device (ITC matter)
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington, D.C.
Case Name: HTC v. Apple
Represented: Plaintiff
Disposition: Deposed in March; testified at trial/hearing (ITC) in May; outcome pending.
Date: November 2010 – May 2011.

Type of Matter: Theft of trade secrets involving design of power management integrated circuits (ITC matter)
Law Firm: Alston + Bird, LLP, Menlo Park, California
Case Name: Richtek v. uPI, AMD, Sapphire Technology, Diamond Multimedia, and XFX Technology
Represented: Plaintiff
Disposition: Prepared an expert report and a supplemental expert report; deposed twice (three days total); subsidiary respondents settled and exited the case during May 2010 – July 2010; main respondent uPI agreed on 21 July 2010 to a Consent Order that included a ten-year ban on importation of the accused products to avoid an ITC hearing.
Date: January 2010 – July 2010; ITC enforcement proceeding opened against uPI and Sapphire, June 2011 – March 2012 (see above); follow-on district/superior court cases temporarily stayed, but pending.

Type of Matter: Patent infringement and theft of trade secrets involving integrated circuit manufacturing
Law Firm: Kecker and Van Nest, LLP, San Francisco, California
Case Name: TSMC v. SMIC
Represented: Plaintiff
Disposition: Deposed; testified at trial September 2009; jury returned guilty verdict on all 18 counts; parties settled during damages phase of trial.
Date: July 2007 – September 2009.

Type of Matter: Theft of Trade Secrets
Law Firm: Baker & McKenzie, LLP, San Diego, California
Case Name: Neology Inc. v. B. Roesner et al.
Represented: Plaintiff
Disposition: Reviewed materials produced during discovery and found considerable facially-labeled trade secret material in the possession of the defendant. Case Settled
Date: April 2007 – May 2007

Type of Matter: Theft of Trade Secrets
Law Firm: Weil, Gotshal, and Manges, LLP, New York, New York
Case Name: Synopsys v. Nassda
Represented: Defendant
Disposition: Wrote an expert report on behalf of defendant but was not
deposed. Case Settled
Date: September 2003 - August 2004

Type of Matter: Theft of Trade Secrets
Law Firm: Howrey, Simon, Arnold & White, LLP, Menlo Park, California
Case Name: Silvaco, Inc. v. Circuit Semantics, Inc.
Represented: Defendant
Disposition: Wrote an expert report on behalf of defendant and was deposed.
Case Settled
Date: February 2003 - September 2003

Type of Matter: Contract dispute, Copyright Infringement, and Theft of Trade
Secret matter involving integrated circuit design tools
Law Firm: Russo & Hale, LLP, Palo Alto, California
Case Name: Virtual Silicon Technology, Inc. v. Library Technologies, Inc.,
Represented: Plaintiff
Disposition: On behalf of plaintiff, wrote an expert report, was deposed and
testified at arbitration hearing. Decision of binding arbitration
released in November 2003; all findings-of-fact in favor of the
plaintiff.
Date: December 2002 - November 2003

PUBLICATIONS

Books

1. D. Foty, “Moore’s Law: The Untold Story,” August 2017.
2. D. Foty, “The Rise and Fall of Classical Athens: A Short History,” January 2018.
3. D. Foty, “Thomas Seebeck: His Life and Science,” September 2018.
4. D. Foty, “Essential Digital, Analog, and Semiconductor Electronics Technology,” Chapter 19 in *Concise Higher Electrical Engineering* (ed. by E. Chikuni, M. Khan, and O. Okoro), Juta Academic, 2008.
5. D. Foty, *MOSFET Modeling with SPICE: Principles and Practice*, Prentice-Hall (now Pearson Education), 1997 (now in its third printing; Vietnamese-language edition published in 2006).
6. Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider, C. Claeys, D. Foty, T. Kawai, and R. Kirschman) (published in October 1993).
7. Proceedings of the Symposium on Low Temperature Electronic Device Operation (ed. by D. Foty) (published in December 1991).

Guest Journal Editor

1. Guest editor, special issue on Low Voltage/Low Power Design, Analog Integrated Circuits and Signal Processing, December 1999.

Refereed Journal Publications

1. D. Foty, “Nanoscale Electron Devices: Difficulties, Granularities, and Applications” (Invited Paper), *Romanian Journal of Information Sciences and Technology*, (published by the Romanian Academy of Sciences), January 2009, vol. 12(3), pp. 317 – 338.
2. D. Foty, “An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K” (Invited Paper), *Analog Integrated Circuits and Signal Processing* vol. 49, pp. 97 – 105 (2006).
3. D. Foty and K. Runge, “What’s Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We’ve Been Expecting” (Invited Paper), *the African Journal of Information and Communications Technology* (online publication).

4. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5 μ m Process and Implications for Analog Circuit Design," IEEE Transactions on Nuclear Science vol. NS-50, pp. 915 - 920 (2003).
5. D. Binkley, C. Hopper, S. Tucker, B. Moss, J. Rochelle, and D. Foty, "A CAD Methodology for Optimizing Transistor Current and Sizing in Analog CMOS Design," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems vol. CAD-22, pp. 225 – 237 (2003).
6. D. Foty, "Perspectives on Analytical Modeling of Small Geometry MOSFETs in SPICE for Low Voltage/Low Power CMOS Circuit Design" (Invited Paper), Analog Integrated Circuits and Signal Processing vol. 21, pp. 229 – 252 (1999).
7. D. Foty, "Taking a Deep Look at Analog CMOS," IEEE Circuits and Devices, March 1999, pp. 23 – 28.
8. D. Foty, "MOSFET Modeling for Circuit Simulation: Where Do We Go From Here?," IEEE Circuits and Devices, July 1998, pp. 26 – 31.
9. G. Gildenblat and D. Foty, "Low Temperature Models of Metal-Oxide-Semiconductor Field-Effect Transistors" (Invited Paper), The International Journal of High Speed Electronics and Systems vol. 6, pp. 317 - 373 (1995).
10. D. Foty and E. Nowak, "MOSFET Technology for Low Voltage/Low Power Applications" (Invited Paper), IEEE Micro, June 1994, pp. 68 - 77.
11. D. Foty, P. Wyns, and K. Oughstun, "On the Propagation of Short Optical Pulses in a Linear Dispersive Medium," IEEE Journal of Quantum Electronics vol. 28, pp. 1619 - 1622 (1992).
12. E. Farrell, P. Appino, D. Foty, and T. Linton, "Visual Interpretation of Multi-Dimensional Computations and Transistor Design," IBM Journal of Research and Development vol. 35, pp. 26 - 44 (1991).
13. D. Foty, "Impurity Ionization in MOSFETs at Very Low Temperatures," Cryogenics vol. 30, pp. 1056 - 1063 (1990).
14. D. Cole, E. Buturla, S. Furkay, K. Varahramyan, J. Slinkman, J. Mandelman, D. Foty, O. Bula, A. Strong, J. Park, T. Linton, J. Johnson, M. Fischetti, S. Laux, P. Cottrell, H. Lustig, F. Pileggi, and D. Katcoff, "The Use of Simulation in Semiconductor Technology Development" (Invited Paper), Solid State Electronics vol. 33, pp. 591 - 623 (1990).

15. K. Oughstun, P. Wyns, and D. Foty, "Numerical Determination of the Signal Velocity in Linear Dispersive Pulse Propagation," *Journal of the Optical Society of America A* vol. 6, pp. 1430 - 1440 (1989).
16. P. Wyns, D. Foty, and K. Oughstun, "Numerical Analysis of the Precursor Fields in Dispersive Pulse Propagation," *Journal of the Optical Society of America A* vol. 6, pp. 1421 - 1429 (1989).
17. D. Foty, "Thermal Effects in p-Channel MOSFETs at Low Temperatures," *IEEE Transactions on Electron Devices* vol. 36, pp. 1542 - 1544 (1989).
18. D. Foty and S. Titcomb, "Thermal Effects in n-Channel Enhancement MOSFETs Operated at Cryogenic Temperatures," *IEEE Transactions on Electron Devices* vol. 34, pp. 107 - 114 (1987).

Refereed Conference Proceedings

1. D. Foty, "Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low-Power Digital CMOS Circuits," *Invited Conference Plenary Lecture*, Proceedings of the 13th International Symposium on Signals, Circuits, and Systems, pp. 123 - 128 (published July 2017).
2. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" *Invited Conference Plenary Lecture*, Proceedings of the 11th International Symposium on Signals, Circuits, and Systems, pp. 1 - 8 (published July 2013).
3. D. Foty, "The Future of 'Moore's Law' – Does It Have One?" *Invited Conference Plenary Lecture*, Proceedings of the 13th Baltic Electronics Conference, pp. 21 – 26 (published October 2012).
4. D. Foty, B. Smith, S. Sinha, and M. Schröter, "Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology," *Invited Conference Plenary Lecture*, Proceedings of the 10th IEEE East-West Design and Test Symposium, pp. 264 - 269 (published September 2012).
5. D. Foty, B. Smith, S. Sinha, and M. Schröter, "The Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth," (Invited Paper), Proceedings of the 10th International Symposium on Signals, Circuits, and Systems, pp. 275 - 279 (published July 2011).
6. D. Foty, "Breaking the Entropy Addiction: Understanding Power Consumption and Overcoming It," *Invited Conference Plenary Lecture*, Proceedings of Africon2009, Proceedings on DVD (published September 2009).

7. B.C. Mabuza, S. Sinha and D. Foty, "On-chip Impedance Tuning for mm-wave Applications,"• Proceedings of the South African Conference on Semiconductor and Superconductor Technology, pp. 49 – 53 (published April 2009).
8. D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A. Uys, and E. Sibanda, "mm-Wave Radio Communications Systems: The Quest Continues," *Invited Conference Plenary Lecture*, Proceedings of the International Radio Electronics Forum, pp. 14 – 17 (published October 2008).
9. D. Foty, "Prospects for Nanoscale Electron Devices: Some Little-Recognized Problems," *Invited Conference Plenary Lecture*, Proceedings of the 31st Conference on Semiconductor Physics, pp. 3 – 13 (published October 2008).
10. D. Foty, "Nanoscale Electron Devices: The Untold Technology Story," *Invited Conference Plenary Lecture*, Proceedings of the 11th Baltic Electronics Conference, pp. 59 - 69 (published October 2008).
11. D. Foty, "Next-Generation Wireless Networks: A New World, From Bottom to Top," *Invited Conference Keynote Lecture*, Proceedings of Africon2007, Proceedings on DVD (published September 2007).
12. D. Foty, "Next-Generation Wireless Networks: New Building Blocks and New Network Topologies," *Invited Conference Plenary Lecture*, Proceedings of the International Conference on Dependable Systems, Services, and Technologies, pp. 220 - 228 (published April 2007).
13. D. Foty, "Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective," *Invited Conference Plenary Lecture*, Proceedings of the East-West Design and Test Workshop, pp. 29 - 38 (published September 2006).
14. D. Foty, "New Directions in Technology for High-Speed Wireless Data Communications," *Invited Conference Plenary Lecture*, Proceedings of the 13th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 19 – 27 (published June 2006).
15. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future" (Invited Paper), Proceedings of the International Workshop on System-on-Chip pp. xxx - xxx (published July 2005). (Paper was submitted on time but was inadvertently not included in the Proceedings volume – available upon request.)
16. D. Foty and G. Gildenblat, "Scaling Theory and 'Punctuated Equilibrium' in CMOS Technology," *Invited Conference Plenary Lecture*, Proceedings of the 7th International Symposium on Signals, Circuits, and Systems, pp. 1 - 8 (published July 2005).

17. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), Proceedings of the 12th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 939 - 945 (published June 2005).
18. D. Foty, "An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K" (Special Session Paper), Proceedings of the International Symposium on Industrial Electronics, pp. 1139 - 1144 (published June 2005).
19. D. Foty and K. Runge, "“What’s Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We’ve Been Expecting,” Invited Conference Plenary Lecture, Proceedings of the 12th International Conference on Telecommunications, (conference proceedings pages not numbered), (published May 2005).
20. D. Foty and G. Gildenblat, "Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future," Invited Conference Plenary Lecture, Proceedings of the 8th International Conference CADSM, pp. 21 – 28 (published February 2005).
21. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Past, Present, and Future" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 631 – 637 (published December 2004).
22. G. Gildenblat, C. McAndrew, H. Wang, W. Wu, D. Foty, L. Lemaitre and P. Bendix, "Advanced Compact Models: Gateway to Modern CMOS Design" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 638 – 641 (published December 2004).
23. P. Bendix, D. Foty, and D. Pachura, "Practical Aspects of MOS Transistor Model ‘Accuracy’ in Modern CMOS Technology" (Invited Paper), Proceedings of the 11th International Conference on Electronics, Circuits, and Systems, pp. 642 - 645 (published December 2004).
24. D. Foty and G. Gildenblat, "CMOS Scaling Theory – Why Our ‘Theory of Everything’ Still Works, and What That Means For The Future" (Invited Paper), Proceedings of the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, pp. 27 – 38 (published November 2004).
25. D. Foty, "Perspectives on Scaling Theory and CMOS Technology – Punctuated Equilibrium and Evolutionary Biology," Invited Conference Plenary Lecture, Proceedings of the 9th Baltic Electronics Conference, pp. 17- 24 (published October 2004).
26. D. Foty, "Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology," Invited Conference Plenary

- Lecture, Nordic VLSI Design Conference (NorChip), pp. 8 - 15 (published November 2003).
27. D. Foty, "Re-Generalizing the MOS Transistor, for Improved Analog Design and Extension to Nanotechnology: New Rules for a New Century," Invited Conference Plenary Lecture, Proceedings of the 4th Electronic Circuits and Systems Conference, pp. 86 - 95 (published September 2003).
28. D. Foty, "Re-Thinking and Re-Generalizing the MOS Transistor: Understanding, CMOS Design, and Extension to Nanotechnology," Invited Conference Plenary Lecture, Proceedings of the 16th European Conference on Circuit Theory and Design, pp. I-16 – I-21 (published September 2003).
29. D. Foty, "Modernizing the Framework for Deep Submicron Design – For CMOS and Beyond," Invited Conference Plenary Lecture, Proceedings of the 10th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 19 - 24 (published June 2003).
30. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5 μ m Process and Implications for Analog Circuit Design," Proceedings of the IEEE Nuclear Science Symposium, (conference proceedings pages not numbered), (published November 2002).
31. D. Foty, M. Bucher, and D. Binkley, "Re-Interpreting the MOS Transistor Via the Inversion Coefficient and the Continuum of gms/Id," Proceedings of the 9th International Conference on Electronics, Circuits, and Systems, pp. 1179 - 1182 (published September 2002).
32. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS," Proceedings of the 9th International Conference on Electronics, Circuits, and Systems, pp. 1183 -1186 (published September 2002).
33. D. Foty, D. Binkley, and M. Bucher, "gm/Id-Based MOSFET Modeling and Modern Analog Design" (Invited Paper), Proceedings of the 9th International Conference on the Mixed Design of Integrated Circuits and Systems, pp. 55 - 58 (published June 2002).
34. D. Foty, D. Binkley, and M. Bucher, "Starting Over: gm/Id-Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies" (Invited Paper), Proceedings of the International Conference on the Modeling and Simulation of Microsystems, pp. 682 - 685 (published in April 2002).
35. D. Foty, D. Binkley, and M. Bucher, "Measurements and Modeling of MOSFET Inversion Level Over a Wide Range as a Basis for Analog Design," Proceedings of the 15th European Conference on Circuit Theory and Design, pp. I-85 – I-88 (published in August 2001).

36. D. Foty, "MOSFET Modeling for Circuit Simulation: Requiem or Recovery?," Proceedings of the 15th European Conference on Circuit Theory and Design, pp. I-81 – I-84 (published in August 2001).
37. D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS Over the Continuum of Inversion Level and Channel Length," Proceedings of the 7th International Conference on Electronics, Circuits, and Systems, pp. 161 – 164 (published in December 2000).
38. D. Foty and E. Nowak, "Performance, Reliability, and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable" (Invited Paper), Proceedings of the 1993 European Solid State Device Research Conference, pp. 943 - 948.
39. D. Foty and E. Nowak, "Performance/Reliability Trade-Off and Optimized nMOSFET Design for 77K CMOS Logic," Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 89 - 95 (published in October 1993).
40. D. Foty, "The Design of Deep Submicron FETs for Low Temperature Operation" (Invited Paper), Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 63 - 77 (published in October 1993).
41. D. Foty, H. Hanafi, P. Agnello, and H. Ho, "Mixed Schottky/p-n Junction Behavior in Diodes Produced by Outdiffusion from Polycrystalline Cobalt Disilicide," Technical Digest of the 1992 International Electron Devices Meeting, pp. 841 - 845.
42. D. Foty, "Low Temperature Electronics and Future Electron Devices" (Invited Paper), Proceedings of the Symposium on Low Temperature Electronic Device Operation (ed. by D. Foty), pp. 13 - 24 (published in December 1991).
43. D. Foty and S. Titcomb, "Freeze-Out and Field Dependent Ionization in MOSFETs at Very Low Temperatures," Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductors (ed. by S. Raider), pp. 151 - 160 (published in March 1988).

Articles in Industry Trade Publications

1. D. Foty, "It's Time to Write Off the Past – Vermont Needs an Economic Future," Ethan Allen Institute Newsletter, November 2002. (This article was also published in the Springfield (Vt.) Reporter, the Brandon (Vt.) Bugle, the Brattleboro (Vt.) Reformer, and The Vermont Times.)
2. D. Foty and P. Bendix, "An Executive Guide to MOS Transistor Modeling," Fabless Mianyang BOE Ex. 1003 Forum, March 2002.

3. D. Foty, “Radio-Frequency Technology: Easier Said Than Done?,” Fabless Forum, September 1999.
4. D. Foty, “A Traveler’s Tales – An Essay on Globalization and the Culture of the ‘New Economy’,” Vermont Business Magazine, September 1998.
5. D. Foty, “MOSFET Modeling for Circuit Simulation: Where Do We Go From Here?,” Fabless Forum, March 1998.

Conference Presentations

1. D. Foty, “Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low-Power Digital CMOS Circuits at Dimensions Below 100nm,” (Invited Conference Plenary Lecture), presented at the 16th Baltic Electronics Conference, Tallinn, Estonia, 8 October 2018.
2. D. Foty, “Developing Critical Infrastructure – Data-Centric, Next-Generation Communications Networks,” (Invited Conference Plenary Lecture), presented at the 2nd Regional African Conference of the International Telecommunications Society, Lusaka, Zambia, 16 March 2018.
3. D. Foty, “Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low Power Digital CMOS Circuits,” (Invited Conference Plenary Lecture), presented at the 13th International Symposium on Signals, Circuits, and Systems, Iași, Romania, 13 July 2017.
4. D. Foty, “Developing Data-Centric, Next-Generation Communications Networks That Actually Work – and Work Well,” (Invited Conference Plenary Lecture), presented at the EAI International Conference for Research, Innovation and Development for Africa, Victoria Falls, Zimbabwe, 21 June 2017.
5. D. Foty, “Amplification, Feedback, and Sub-Biasing: Applying Analog Techniques to High-Speed, Low Power Digital CMOS Circuits,” (Invited Conference Plenary Lecture), presented at the 15th Baltic Electronics Conference, Tallinn, Estonia, 3 October 2016.
6. D. Foty, “The Future of ‘Moore’s Law’ – Does It Have One?” (Invited Conference Plenary Lecture), presented at the 12th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design, Istanbul, Turkey, 7 September 2015.
7. D. Foty, “Patents, Trade Secrets, Intellectual Property, and Such: What Engineers Need to Know,” (Invited Conference Plenary Lecture), presented at the 12th International Symposium on Signals, Circuits, and Systems, Iași, Romania, 10 July 2015.

8. D. Foty, “Patents, Trade Secrets, Intellectual Property, and Such: What Engineers Need to Know,” (Invited Conference Plenary Lecture), presented at the 14th Baltic Electronics Conference, Laulasmaa, Estonia, 8 October 2014.
9. D. Foty, “The Future of ‘Moore’s Law’ – Does It Have One?” (Invited Conference Plenary Lecture), presented at the 11th International Symposium on Signals, Circuits, and Systems, Iași, Romania, 11 July 2013.
10. D. Foty, “The Future of ‘Moore’s Law’ – Does It Have One?” (Invited Conference Plenary Lecture), presented at the 13th Baltic Electronics Conference, Laulasmaa, Estonia, 5 October 2012.
11. D. Foty, B. Smith, S. Sinha, and M. Schröter, “Expanding Wireless Bandwidth in a Power-Efficient Way: Developing a Viable mm-Wave Radio Technology,” (Invited Conference Plenary Lecture), presented at the 10th IEEE East-West Design and Test Symposium, Kharkov, Ukraine, 15 September 2012.
12. D. Foty, B. Smith, S. Sinha, and M. Schröter, “Addressing the Problem of Wireless Bandwidth and Power-Efficiency: Prospects for mm-Wave Radio Technology,” presented at MASFOR2012, Istanbul, Turkey, 22 June 2012.
13. D. Foty, B. Smith, S. Sinha, and M. Schröter, “Addressing the Emerging Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth: Prospects for mm-Wave Radio Technology,” (Invited Conference Keynote Lecture), presented at Africon2011, Livingstone, Zambia, 13 September 2011.
14. D. Foty, B. Smith, S. Sinha, and M. Schröter, “The Wireless Bandwidth Crisis and the Need for Power-Efficient Bandwidth,” (Invited Paper), presented at the 10th International Symposium on Signals, Circuits, and Systems, Iași, Romania, 1 July 2011.
15. D. Foty, “Thomas Johann Seebeck – Two Centuries Later, An Appreciation,” (Invited Conference Plenary Lecture – the Thomas Johann Seebeck Memorial Lecture), presented at the 12th Baltic Electronics Conference, Tallinn, Estonia, 4 October 2010.
16. D. Foty, B. Smith, S. Sinha, and M. Schröter, “Next-Generation Wireless Communications Networks - From Chips to Architecture,” (Invited Conference Plenary Lecture), presented at the International Association of Science and Technology for Development (IASTED) International Conference on Modeling and Simulation, Gaborone, Botswana, 7 September 2010.
17. D. Foty, “Breaking the Entropy Addiction: Understanding Power Consumption and Overcoming It,” (Invited Conference Plenary Lecture), presented at Africon2009, Nairobi, Kenya, 25 September 2009.

18. D. Foty, S. Sinha, M. Weststrate, C. Coetzee, A. Uys, and E. Sibanda, “mm-Wave Radio Communications Systems: The Quest Continues” (Invited Conference Plenary Lecture), presented at the International Radio Electronics Forum, Kharkov, Ukraine, 23 October 2008.
19. D. Foty, “Prospects for Nanoscale Electron Devices: Some Little-Recognized Problems” (Invited Conference Plenary Lecture), presented at the 31st Conference on Semiconductor Physics, Sinaia, Romania, 13 October 2008.
20. D. Foty, “Nanoscale Electron Devices: The Untold Technology Story” (Invited Conference Plenary Lecture), presented at the 11th Baltic Electronics Conference, Laulasmaa, Estonia, 8 October 2008.
21. D. Foty, “Electron Devices in Nanoelectronic Circuits and Systems: Problems and Prospects,” *Invited Presentation*, presented at the IEEE Electron Devices Society / Solid State Circuits Society Mini-Colloquium “Nanoelectronic Devices: Present and Perspective,” Sinaia, Romania, 14 October 2007.
22. D. Foty, “Next-Generation Wireless Networks: A New World, From Bottom to Top,” Invited Conference Keynote Lecture, presented at Africon2007, Windhoek, Namibia, 26 September 2007.
23. D. Foty, “The ‘MOS Miracle’ – A Behind-the-Scenes Look,” Conference tutorial presented at the 8th International Symposium on Signals, Circuits, and Systems, Iași, Romania, 11 July 2007.
24. D. Foty, “Next-Generation Wireless Networks: New Building Blocks and New Network Topologies,” Invited Conference Keynote Lecture, presented at the International Conference on Dependable Systems, Services, and Technologies, Kirovohrad, Ukraine, 27 April 2007.
25. D. Foty, “Factors in High-Speed Wireless Data Networking – New Ideas and a New Perspective” (Invited Conference Plenary Lecture), presented at the East-West Design and Test Workshop, Sochi, Russia, 18 September 2006.
26. D. Foty, “New Directions in Technology for High-Speed Wireless Data Communications” (Invited Conference Plenary Lecture), presented at the 13th International Conference on the Mixed Design of Integrated Circuits and Systems, Gdynia, Poland, 24 June 2006.
27. D. Foty and G. Gildenblat, “Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future” (Invited Paper), presented at the International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.
28. D. Foty and G. Gildenblat, “Scaling Theory and ‘Punctuated Equilibrium’ in CMOS Technology” (Invited Conference Plenary Lecture), presented at the 7th International Symposium on Signals, Circuits, and Systems, Iași, Romania, 14 July 2005.

29. D. Foty, “An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K” (Special Session Paper), presented at the 12th International Conference on the Mixed Design of Integrated Circuits and Systems, Krakow, Poland, 23 June 2005.
30. D. Foty, “An Evaluation of Deep-Submicron CMOS Design Optimized for Operation at 77K” (Special Session Paper), presented at the International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20 June 2005.
31. D. Foty and K. Runge, “What’s Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We’ve Been Expecting” (Invited Conference Plenary Lecture), presented at the 12th International Conference on Telecommunications, Cape Town, South Africa, 4 May 2005.
32. D. Foty and G. Gildenblat, “Fundamental Aspects of CMOS Technology: Basics, Implications, and a Roadmap to the Future” (Invited Conference Plenary Lecture), presented at the 8th International Conference CADSM, Polyana, Ukraine, 23 February 2005.
33. D. Foty, “Perspectives on Scaling Theory and CMOS Technology – Past, Present, and Future” (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.
34. G. Gildenblat, C. McAndrew, H. Wang, W. Wu, D. Foty, L. Lemaitre and P. Bendix, “Advanced Compact Models: Gateway to Modern CMOS Design” (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.
35. P. Bendix, D. Foty, and D. Pachura, “Practical Aspects of MOS Transistor Model ‘Accuracy’ in Modern CMOS Technology” (Invited Paper), presented at the 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 15 December 2004.
36. D. Foty and G. Gildenblat, “CMOS Scaling Theory – Why Our ‘Theory of Everything’ Still Works, and What That Means For The Future” (Invited Paper), presented at the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, Berg-en-Dal, Kruger National Park, South Africa, 8 November 2004.
37. D. Foty, “Perspectives on Scaling Theory and CMOS Technology – Punctuated Equilibrium and Evolutionary Biology” (Invited Conference Plenary Lecture), presented at the 9th Baltic Electronics Conference, Tallinn, Estonia, 4 October 2004.
38. D. Foty, “Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology,” (Invited Conference Plenary Lecture), presented at the Nordic VLSI Design Conference (NorChip), Riga, Latvia, 10 November 2003.

39. D. Foty, “Pondering the MOS Transistor in the 21st Century” (Conference Tutorial), presented at the Nordic VLSI Design Conference (NorChip), Riga, Latvia, 9 November 2003.
40. D. Foty, “Re-Generalizing the MOS Transistor, for Improved Analog Design and Extension to Nanotechnology: New Rules for a New Century” (Invited Conference Plenary Lecture), presented at the 4th Electronic Circuits and Systems Conference, Bratislava, Slovakia, 12 September 2003.
41. D. Foty, “Re-Thinking and Re-Generalizing the MOS Transistor: Understanding, CMOS Design, and Extension to Nanotechnology” (Invited Conference Plenary Lecture), presented at the 16th European Conference on Circuit Theory and Design, Krakow, Poland, 2 September 2003.
42. D. Foty, “Modernizing the Framework for Deep Submicron Design – For CMOS and Beyond” (Invited Conference Plenary Lecture), presented at the 10th International Conference on the Mixed Design of Integrated Circuits and Systems, Lodz, Poland, 27 June 2003.
43. D. Foty, M. Bucher, and D. Binkley, “Re-Interpreting the MOS Transistor Via the Inversion Coefficient and the Continuum of g_m/I_d ,” presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 18 September 2002.
44. D. Foty, and M. Bucher, “New Techniques for Modern Analog Design: CMOS Design Methodologies and the EKV MOSFET Model” (Conference Tutorial), presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 15 September 2002.
45. D. Foty, D. Binkley, and M. Bucher, “ g_m/I_d -Based MOSFET Modeling and Modern Analog Design” (Invited Paper), presented at the 9th International Conference on the Mixed Design of Integrated Circuits and Systems, Wrocław, Poland, 20 June 2002.
46. D. Foty and D. Binkley, “MOS Modeling as a Basis for Design Methodologies: New Techniques for Modern Analog Design” (Conference Tutorial), presented at the International Symposium on Circuits and Systems, Scottsdale, Arizona, 26 May 2002.
47. D. Foty, “MOS Modeling, Design Quality, and Modern Analog Design” (Conference Tutorial), presented at the Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 25 April 2002.
48. D. Foty, D. Binkley, and M. Bucher, “Starting Over: g_m/I_d -Based MOSFET Modeling as a Basis for Modernized Analog Design Methodologies” (Invited Paper),

- presented at the Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 23 April 2002.
49. D. Foty, "MOS Modeling, Design Quality, and Modern Analog Design" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 18 March 2002.
 50. D. Foty, D. Binkley, and M. Bucher, "Measurements and Modeling of MOSFET Inversion Level Over a Wide Range as a Basis for Analog Design," presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 29 August 2001.
 51. D. Foty, "MOSFET Modeling for Circuit Simulation: Requiem or Recovery?," presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 29 August 2001.
 52. D. Foty and D. Binkley, "MOS Modeling as a Basis for Design Methodologies: New Techniques for Next-Generation Analog Circuit Design" (Conference Tutorial), presented at the 15th European Conference on Circuit Theory and Design, Espoo, Finland, 28 August 2001.
 53. D. Foty and D. Binkley, "Re-Connecting MOS Modeling and Circuit Design: New Methods for Design Quality" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 26 March 2001.
 54. D. Foty and D. Binkley, "MOS Modeling and Circuit Design: Re-Establishing a Lost Connection" (Conference Tutorial), presented at the Design Automation Conference, Los Angeles, California, 7 June 2000.
 55. D. Foty, "A Circuit Designer's Guide to MOS Modeling" (Conference Tutorial), presented at the International Symposium on Circuits and Systems, Geneva, Switzerland, 28 May 2000.
 56. D. Foty, "MOS Models as a Factor in the Quality of Electronic Design" (Conference Tutorial), presented at the International Symposium on Quality Electronic Design, San Jose, California, 20 March 2000.
 57. D. Foty, "MOS Modeling – A Crucial Circuit Design Activity," presented at Silicon RF-IC: Modeling and Design," Lausanne, Switzerland, 25 February 2000.
 58. D. Foty, "An Overview of AC Simulation Aspects of MOS Modeling," presented at the RF MOS Modeling Workshop, Munich, Germany, 16 February 1999.
 59. D. Foty, "AC Simulation Aspects of MOS Modeling," presented at Northcon, Seattle, Washington, 22 October 1998.

60. D. Foty, "Effective MOSFET Modeling for SPICE Circuit Simulation" (Conference Tutorial), presented at Northcon, Seattle, Washington, 22 October 1998.
61. D. Foty, "What Every Circuit Designer Needs to Know About MOS Modeling for SPICE Circuit Simulation" (One-Day Short Course), presented at the Electronic Design Automation and Test Conference, Asia, Hsinchu, Taiwan, 15 October 1998.
62. D. Foty, "MOS Modeling of Small Geometry Structures for Circuit Simulation" (Conference Tutorial), presented at the Custom Integrated Circuits Conference, Santa Clara, California, 11 May 1998.
63. D. Foty, "MOS Modeling for Deep Submicron CMOS Circuit Simulation" (Conference Tutorial), presented at the Southeastern Workshop on Mixed-Signal VLSI, Knoxville, Tennessee, 1 April 1998.
64. D. Foty, "MOS Modeling Issues in the Emerging Analog and Low Power Era" (Conference Tutorial), presented at the Electronic Design Automation and Test Conference, Asia, Hsinchu, Taiwan, 28 August 1997.
65. D. Foty, "MOS Modeling Issues in the Emerging Analog and Low Power Era" (Conference Tutorial), presented at the Electronic Design Automation and Test Conference, Asia, Shanghai, China, 22 August 1997.
66. D. Foty, "Aspects of MOS Modeling for Analog/Mixed-Signal Design," presented at the CMP Analog/Mixed-Signal Design Conference, San Jose, California, 22 July 1997.
67. D. Foty, "MOS Modeling and SPICE: Are You an Educated Model Consumer?" (Conference Tutorial), presented at the Custom Integrated Circuits Conference, Santa Clara, California, 5 May 1997.
68. D. Foty, "The SPICE FET Models: Pitfalls and Prospects" (Conference Tutorial), presented at the Design Automation Conference, Las Vegas, Nevada, 5 June 1996.
69. D. Foty and E. Nowak, "Performance, Reliability, and Supply Voltage Reduction, with the Addition of Temperature as a Design Variable" (Invited Paper), presented at the Symposium on Low Voltage-Low Power Integrated Circuits, 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.
70. D. Foty and E. Nowak, "Performance/Reliability Trade-Off and Optimized nMOSFET Design for 77K CMOS Logic," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.
71. D. Foty, "The Design of Deep Submicron FETs for Low Temperature Operation" (Invited Paper), presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

72. D. Foty, H. Hanafi, P. Agnello, and H. Ho, "Mixed Schottky/p-n Junction Behavior in Diodes Produced by Outdiffusion from Polycrystalline Cobalt Disilicide," presented at the 1992 International Electron Devices Meeting, San Francisco, California, 16 December 1992.
73. D. Foty, "Low Temperature Electronics and Future Electron Devices (Invited Paper), presented at the Symposium on Low Temperature Electronic Device Operation, Washington, DC, 7 May 1991.
74. D. Foty, "Impurity Ionization in MOSFETs at Very Low Temperatures," presented at the First International Conference on Low Temperature Electronics, Berkeley, California, 24 April 1990.
75. D. Foty and T. Furukawa, "Behavior of an NMOS Trench Isolated Corner Parasitic Device at Low Temperature," presented at the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.
76. D. Foty and S. Titcomb, "Freeze-Out and Field Dependent Ionization in MOSFETs at Very Low Temperatures," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 October 1987.

Co-Authored Conference Presentations

1. S. Sinha and D. Foty, "SiGe Technology for mm-Wave Applications," (Invited Conference Plenary Lecture), presented at the 13th Baltic Electronics Conference, Tallinn, Estonia, 3 October 2012.
2. B.C. Mabuza, S. Sinha and D. Foty, "On-chip Impedance Tuning for mm-Wave Applications," presented at the South African Conference on Semiconductor and Superconductor Technology, Stellenbosch, South Africa 8 April 2009.
3. S. Terry, J. Rochelle, D. Binkley, B. Blaylock, D. Foty, and M. Bucher, "Comparison of a BSIM3V3 and EKV MOST Model for a 0.5 μ m Process and Implications for Analog Circuit Design," presented at the IEEE Nuclear Science Symposium, Norfolk, Virginia, 15 November 2002.
4. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, "Analysis of Transconductances at All Levels of Inversion in Deep Submicron CMOS," presented at the 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 18 September 2002.
5. D. Binkley, M. Bucher, and D. Foty, "Design-Oriented Characterization of CMOS Over the Continuum of Inversion Level and Channel Length," presented at the 7th Mianyang BOE Ex-1093 Case No. IPR2023-00941

International Conference on Electronics, Circuits, and Systems, Kaslik, Lebanon, 18 December 2000.

6. G. Gildenblat, M. Bradford, and D. Foty, "A New MOS C-V Simulator for Low Temperature Applications," presented at the Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 20 May 1993.

Conference Panel Participation

1. Member of Panel Discussion, 2nd Regional African Conference of the International Telecommunications Society, Lusaka, Zambia, 15 March 2018.
2. Member of Panel Discussion, 12th International Conference on Synthesis, Modeling, Analysis, and Simulation Methods and Applications to Circuit Design, Istanbul, Turkey, 7 September 2015.
3. Member of Panel Discussion, Future Wireless Telecommunications, "Telecosm," Lake George, New York, 16 October 2007.
4. Moderator of Panel Discussion, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.
5. Member of Panel Discussion, Custom Integrated Circuits Conference, San Jose, California, 23 September 2003.
6. Co-moderator of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, Santa Clara, California, 9 September 2002.
7. Member of Panel Discussion, Workshop on Compact Modeling, International Conference on the Modeling and Simulation of Microsystems, San Juan, Puerto Rico, 23 April 2002.
8. Member of Panel Discussion, "Vermont's High-Tech Future – Does it Have One?," Room 11, the Statehouse, Montpelier, Vermont, 26 April 2001.
9. Member of Panel Discussion, Fabless Semiconductor Association Quarterly Meeting, San Jose, California, 5 September 1999.
10. Member of Panel Discussion, Fabless Semiconductor Association Modeling Workshop, San Jose California, 24 May 1999.
11. Member of Panel Discussion, Symposium on Low Voltage-Low Power Integrated Circuits at the 1993 European Solid State Device Research Conference, Grenoble, France, 16 September 1993.

12. Member of Panel Discussion, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 19 May 1993.

Invited Seminars/Lectures

1. "Digital Semiconductor Electronics: Why It Happened, And Where It's Going," short course hosted by the University of Pretoria, Pretoria, South Africa, 15 August 2011.
2. "The Untold Story of 'Moore's Law': *Why It Happened*," short course hosted at the summer school of the Universitatea Politehnica București, held in Iași, Romania, 4 – 5 July 2011.
3. "Some Background Thoughts On mm-Wave Radio Technology," seminar presented at the University of Pretoria, Pretoria, South Africa, 17 August 2010.
4. "Digital Semiconductor-Based Electronics: Why It Became A Juggernaut," short course hosted by the University of Pretoria, Pretoria, South Africa, 16 August 2010.
5. "Some Thoughts On mm-Wave Radio Technology," short course hosted at the summer school of the Universitatea Politehnica București, held in Oradea, Romania, 13 July 2010.
6. "Silicon-Based Semiconductor Electronics – How It Came To Dominate," short course hosted at the summer school of the Universitatea Politehnica București, held in Oradea, Romania, 12 July 2010.
7. "The Powerful Entropy Challenge: Dealing With Power Consumption," presented at the IEEE South Africa Section Meeting, Pretoria, South Africa, 18 August 2009.
8. "Digital CMOS Electronics: The Background Story," short course hosted by the University of Pretoria, Pretoria, South Africa, 17 August 2009.
9. "An Overview of mm-Wave Radio Technology," short course hosted at the summer school of the Universitatea Politehnica București, held in Iași, Romania, 13 July 2009.
10. "Modern Electronics: How We Got Here," short course hosted at the summer school of the Universitatea Politehnica București, held in Iași, Romania, 13 July 2009.
11. "Prospects for mm-Wave Radio Technology: An Overview," short course hosted at the summer school of the Universitatea Politehnica București, held in Oradea, Romania, 22 July 2008.
12. "Into the NanoSmall: The Unexpected Challenges," short course hosted at the summer school of the Universitatea Politehnica București, held in Oradea, Romania, 22 July 2008.

13. "A Concise History of Modern Electron Devices," short course hosted at the summer school of the Universitatea Politehnica București, held in Oradea, Romania, 22 July 2008.
14. "Issues In mm-Wave Radio Systems: Prospects and Challenges," short course hosted by the University of Pretoria, Pretoria, South Africa, 8 May 2008.
15. "Prospects for mm-Wave Radio Technology: An Executive Summary for Decision-Makers," presented at the IEEE Region 8 meeting, University of Pretoria, Pretoria, South Africa, 8 May 2008.
16. "The MOS Transistor, On a Tourist Visa," short course hosted at the summer school of the Universitatea Politehnica București, held in Iași, Romania, 16 July 2007.
17. "Semiconductor Electronics: Some Fundamental Background," short course hosted at the summer school of the Universitatea Politehnica București, held in Iași, Romania, 16 July 2007.
18. "The MOS Transistor and CMOS Technology: Past, Present, and Future," short course hosted by Tallinn University of Technology, Tallinn, Estonia, 13 – 14 November 2006.
19. "New Directions in Technology for High-Speed Wireless Data Communications," seminar presented at the Universitatea Politehnica București, Bucharest, Romania, 28 July 2006.
20. "The MOS Transistor and CMOS Technology: History as a Guide to the Future," short course hosted at the summer school of the Universitatea Politehnica București, held in Brașov, Romania, 25 July 2006.
21. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century - Scaling Theory and New Methods in Analog/RF Design," short course hosted by l'École Polytechnique de Montréal, Montréal, Québec, Canada; sponsored by ReSMiQ and the local IEEE Solid State Circuits Society chapter, 27 October 2005.
22. "The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design," short course hosted by the Department of Electrical, Electronic, and Computer Engineering, University of Pretoria, Pretoria, South Africa, and sponsored by the IEEE South Africa Section, 9 – 10 May 2005.
23. "What's Ahead in High-Speed Wireless Data Communications? The Future Will Be Better Tomorrow – And Different Than What We've Been Expecting," seminar presented at the Department of Electrical Engineering, University of Cape Town, Cape Town, South Africa, 7 May 2005.

24. “Low Temperature CMOS: A Bad Idea Whose Time Has (Finally) Come?”, seminar presented at the Department of Computer-Aided Design, L’viv Polytechnic National University, L’viv, Ukraine, 28 February 2005.
25. “The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design,” Full-day “Eurotraining” course, held at the Danish Technical University, Lyngby, Denmark, 27 October 2004.
26. “The Underpinnings of the MOS Transistor and CMOS Technology in the 21st Century – Scaling Theory and New Methods in Analog/RF Design,” Full-day “Eurotraining” course, held at the Politecnico di Torino, Turin, Italy, 25 October 2004.
27. “CMOS Scaling and Low Temperature CMOS: A Bad Idea Whose Time Has Come?”, seminar presented at the Department of Electrical and Computer Engineering, Oakland University, Auburn Hills, Michigan, 25 March 2004.
28. “Modernizing the Interpretation of the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology,” presented at the IEEE Southeast Michigan Spring Section Meeting, Auburn Hills, Michigan, 24 March 2004.
29. “Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology,” seminar presented at Tallinn Technical University, Tallinn, Estonia, 13 November 2003.
30. “Re-Interpreting the MOS Transistor for the 21st Century: Generalized Methods and Their Extension to Nanotechnology,” seminar presented at Helsinki University of Technology, Espoo, Finland, 7 November 2003.
31. “A Practical Examination of MOS Transistor Model ‘Accuracy’ in Modern CMOS Technology,” presented at the MOS Arbeitskreis Meeting, Crolles, France, 5 May 2003.
32. “Building a New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond,” invited seminar presented at the Department of Electrical Engineering, Columbia University, New York, New York, 25 April 2003.
33. “A New Framework for Deep Submicron Analog/RF CMOS Design – and Beyond,” seminar presented at the Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia, 20 March 2003.
34. “Starting Over: Modernizing the Framework for Deep Submicron Analog CMOS Design,” seminar presented at the Nokia Research Center, Helsinki, Finland, 29 November 2002.

35. “Modernizing the Framework for Deep Submicron Analog CMOS Design,” Distinguished Guest Lecturer, IEEE Baltic Region Meeting (sponsored by Tallinn Technical University), Sagadi, Estonia, 19 – 20 August 2002.
36. “Modernizing the Framework for Deep Submicron Analog CMOS Design,” seminar presented at Helsinki University of Technology, Espoo, Finland, 16 August 2002.
37. “gm/Id-Based MOSFET Modeling and Modern Analog Design,” presented at the MOS Arbeitskreis Meeting, Unterpemstatten, Austria, 19 November 2001.
38. “MOS Modeling and Analog Circuit Design,” lecture as part of “Practical Aspects of Analog Design,” professional short course sponsored by Mead Microelectronics, San Francisco, California, 13 November 2001.
39. “MOS Modeling and Analog Circuit Design,” lecture as part of “Transistor-Level Analog IC Design,” professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 10 October 2001.
40. “Please Stop Imitating Us!’ – An Engineer Looks at the (Unstable) State of the Humanities,” presented at a meeting of the National Association of Scholars, Burlington, Vermont, 14 July 2001.
41. “Introduction to the Fabless Semiconductor Association (FSA) and the Modeling Committee Activities,” presented at the MOS Arbeitskreis Meeting, Munich, Germany, 5 March 2001.
42. “The EKV MOSFET Model: A MOS Model of, by, and for Analog Designers,” presented at Broadcom Corp., Irvine, California, 30 November 2000.
43. “Modeling and Simulation for Mixed-Signal IC Design,” lecture as part of “Transistor-Level Analog IC Design,” professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 27 September 2000.
44. “MOS Models as a Factor in the Quality of Electronic Design,” presented at the Rockwell Scientific Center, Thousand Oaks, California, 17 March 2000.
45. “MOS Models as a Factor in the Quality of Electronic Design,” presented at Micron Technology, Inc., Boise Idaho, 4 March 2000.
46. “Modeling and Simulation for Mixed-Signal IC Design,” lecture as part of “Practical Aspects of Analog and Mixed-Signal ICs,” professional short course sponsored by Mead Microelectronics, Monterey, California, 3 February 2000.
47. “Modeling and Simulation for Mixed-Signal IC Design,” lecture as part of “Transistor-Level Analog IC Design,” professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 30 September 1999.

48. “AC Simulation Aspects of MOS Modeling,” presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.
49. D. Foty, M. Bucher, and C. Enz, “The EKV MOSFET Model – A MOS Model for the Analog Designer,” presented at the Fabless Semiconductor Association Modeling Workshop, San Jose, California, 25 May 1999.
50. Several lectures on MOS device physics, modeling, and analog design, presented at Mentor Graphics, Heliopolis, Cairo, Egypt, 5 – 8 May 1999.
51. “A Brief History of MOS Modeling (or, How We Got In This Mess In the First Place),” presented at Philips Research Laboratories, Eindhoven, The Netherlands, 24 March 1999.
52. “An Overview of MOS Modeling for SPICE Circuit Simulation,” presented at Mitel Corporation, Bromont, Québec, Canada, 2 February 1999.
53. “Modeling and Simulation for Mixed-Signal IC Design,” lecture as part of “Practical Aspects of Analog and Mixed-Signal ICs,” professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1998.
54. “MOS Modeling Challenges for Deep Submicron CMOS,” lecture presented as part of “Deep Submicron CMOS Design,” professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 12 October 1998.
55. “Modeling the Temperature-Dependent Characteristics of MOSFETs for Circuit Simulation,” presented at the Electronic Parts Selection and Management Workshop, Center for the Analysis of Life-Cycle Engineering, University of Maryland, College Park, Maryland, 17 June 1998.
56. “A Primer on Trench Isolation Technology (or, Why Do Process Engineers Hate Circuit Designers?),” presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Opti, Inc., Milpitas, California, 12 May 1998.
57. C. Enz, M. Bucher, and D. Foty, “The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design,” satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 30 April 1998.
58. “MOS Modeling Challenges for Deep Submicron CMOS Circuit Simulation,” presented at Digital Equipment Corporation, Hudson, Massachusetts, 13 April 1998.
59. “Challenges for 0.25 μ m CMOS Circuit Design: Scaling, MOS Modeling, and Complexity,” presented at CERN, Geneva, Switzerland, 6 February 1998.

60. "MOS Modeling Challenges for Deep Submicron CMOS," lecture presented as part of "Deep Submicron CMOS Design," professional short course sponsored by Mead Microelectronics, Monterey, California, 11 December 1997.
61. C. Enz, M. Bucher, and D. Foty, "The EKV MOSFET Model for Analog and Mixed-Mode Circuit Design," one-day short course sponsored by the Fabless Semiconductor Association, San Jose, California, 8 November 1997.
62. "MOS Modeling Issues in the Emerging Analog and Low Power Era," presented Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, 27 August 1997.
63. "Current Problems in MOSFET Modeling for Analog Circuit Simulation," presented at Level One Communications, Inc., Sacramento, California, 9 August 1997.
64. Guest lecturer, Centre National pour les Recherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 23 – 28 June 1997.
65. "MOSFET Modeling and Analog Circuit Design," presented at the Centre National pour les Recherches Scientifique (CNRS) Summer Lecture Series, La Londe des Maures, France, 27 June 1997.
66. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at the Fabless Semiconductor Association Modeling Subcommittee Meeting, Adaptec, Inc., Milpitas, California, 6 May 1997.
67. "Benchmarking and Pre-Screening SPICE FET Models for Circuit Simulation Usage," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.
68. "MOSFET Modeling and SPICE: Are You an Educated Model Consumer?," presented at Cirrus Logic, Inc., Fremont, California, 6 May 1997.
69. "MOS Modeling and SPICE: Are You an Educated Model Consumer?," satellite broadcast class, National Technological University (hosted by North Carolina State University, Raleigh, North Carolina), 21 April 1997.
70. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Lausanne, Switzerland, 18 February 1997.
71. "An Overview of the SPICE FET Modeling Infrastructure" lecture presented as part of "Modeling and Simulation of MOS Analog ICs," professional short course sponsored by Mead Microelectronics, Monterey, California, 12 December 1996.
72. "Analytical MOSFET Modeling and SPICE - Past, Present, and Future", seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 9 May 1995.

73. “Constraints on CMOS Technology for Low Voltage/Low Power Applications”, seminar presented at the Department of Electrical Engineering, Ohio State University, Columbus, Ohio, 8 May 1995.
74. “Submicron FET Design: Physical Considerations and Technological Choices”, seminar presented at the Electrical Engineering Department, University of Hawaii, Honolulu, Hawaii, 24 May 1993.
75. “Aspects of the Design of Deep Submicron FETs for CMOS Operation at 300K and 77K”, seminar presented at the Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania, 10 November 1992.

PROFESSIONAL AFFILIATIONS & AWARDS

Honorary Member of the Applied Radio Electronics Science Academy of Ukraine

Senior Member, The Institute of Electrical and Electronic Engineers (IEEE); and of the Electron Devices, Lasers and Electro-Optics, Circuits and Systems, and Communications Societies of the IEEE.

Reviewer/evaluator of funding proposals, Natural Science and Engineering Research Council of Canada, 1991 - present.

Reviewer/evaluator of funding proposals, California MICRO program, 2001 - present.

Reviewer/evaluator of funding proposals, National Research Foundation of South Africa, 2007- present.

Industrial and Academic Mentoring

Member of the Advisory Board, Department of Electrical, Electronic & Computer Engineering, University of Pretoria, South Africa, 2012 – present.

Advisor to the Tshwane University of Technology, Pretoria, South Africa, 2007 - present.

Advisor to the University of Pretoria, Pretoria, South Africa, 2005 – present.

Advisor to the Tallinn University of Technology, Tallinn, Estonia, 2004 – present.

Industrial Mentor for “Development and Applications of a New MOS C-V Simulator for the 2 - 300K Temperature Range” (Professor Gennady Gildenblat, Principal Investigator, Department of Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania), funded by the IBM Shared University Research Contract program, calendar year 1992.

Committees/Conferences

1. Member of the Organizing Committee, and Chair of the Track on Electromagnetics and Antennas, Africon 2011, Victoria Falls, Zambia, September 2011.
2. Member of the Organizing Committee, and Chair of the Track on Electron Devices and Circuits, Africon 2009, Nairobi, Kenya, September 2009.
3. Session Chair, 31st International Conference on Semiconductor Physics, Sinaia, Romania, 14 October 2008.
4. Session Chair, Africon 2007, Windhoek, Namibia, 27 September 2007.
5. Session Chair, 13th International Conference on the Mixed Design of Integrated Circuits and Systems, Gdynia, Poland, 24 June 2006.
6. Session Chair, International Workshop on System-on-Chip, Banff, Alberta, Canada, 22 July 2005.
7. Session Chair, 7th International Symposium on Signals, Circuits, and Systems, Iași, Romania, 15 July 2005.
8. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2005.
9. Special Session Organizer, 12th International Conference on the Mixed Design of Integrated Circuits and Systems, Krakow, Poland, 22 - 25 June 2005.
10. Special Session Organizer, International Symposium on Industrial Electronics, Dubrovnik, Croatia, 20 – 23 June 2005.
11. Session Chair, 12th International Conference on Telecommunications, Cape Town, South Africa, 4 – 6 May 2005.
12. Session Chair, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 - 15 December 2004.
13. Session Chair, the 12th International Symposium on Electron Devices for Microwave and Optoelectronic Applications, Berg-en-Dal, Kruger National Park, South Africa, 8 - 9 November 2004.
14. Member of the International Program Committee, International Conference on Mixed Design of Integrated Circuits and Systems, 2004 – present.
15. Member of the Technical Program Committee, International Symposium on Signals, Circuits, and Systems, 2004 – present.

16. Special Session Organizer, 11th International Conference on Electronics, Circuits, and Systems, Tel Aviv, Israel, 13 – 15 December 2004.
17. Session Chair, 4th Electronic Circuits and Systems Conference, Bratislava, Slovakia, 11 – 12 September 2003.
18. Member of the Scientific Committee, European Conference on Circuit Theory and Design (ECCTD), 2003.
19. Session Chair, 9th International Conference on Electronics, Circuits, and Systems, Dubrovnik, Croatia, 16 - 18 September 2002.
20. Member, Analog Signal Processing Technical Committee, IEEE Circuits and Systems Society, 2002 – present.
21. Member, Program Committee, Analog Circuits and Signal Processing, International Symposium on Circuits and Systems (ISCAS), 2002 – present.
22. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 18 – 20 March 2002.
23. Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 2001 – 2003.
24. Chairman, Fabless Semiconductor Association Modeling Workshop, 2001 – present.
25. Member of Technical Program Committee, European Conference on Circuit Theory and Design (ECCTD), 2001.
26. Member, IEEE Advisory Committee, 2001 – present.
27. Member of the Organizing Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.
28. Member of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2000 – 2002.
29. Chairman of the Modeling Committee, International Symposium on Quality Electronic Design (ISQED), 2001.
30. Session Chair, International Symposium on Quality Electronic Design, San Jose, California (ISQED), 26 – 28 March 2001.
31. Lead Organizer, Fabless Semiconductor Association Workshop, 2000 – present.
32. Member of the MOS Arbeitskreis, 2000 – present.

33. Co-Chairman, Modeling Subcommittee, Fabless Semiconductor Association, 1999 – 2000.
34. Member of the Executive Committee, Modeling Subcommittee, Fabless Semiconductor Association, 1998 – present.
35. Member, Modeling Subcommittee, Fabless Semiconductor Association, 1996 – present.
36. Organizer, Symposium on Low Temperature Electronics and High Temperature Superconductors, Honolulu, Hawaii, 16 - 21 May 1993.
37. Organizer, Symposium on the Physics and Fabrication of Semiconductor Nanostructures, Washington DC, 5 - 10 May 1991.
38. Lead Organizer, Symposium on Low Temperature Electronic Device Operation, Washington DC, 5 - 10 May 1991.
39. Co-Chaired the Symposium on Low Temperature Electronics, Materials, and Processing, Hollywood, Florida, 17 October 1989.