

PHYSICS AND TECHNOLOGY OF SEMICONDUCTOR DEVICES

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Preface

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The 1950's was the decade in which semiconductor technology attained great prominence and attained great industrial importance. Most of the research and engineering effort of the 1950's was devoted to the development of the technology. The 1960's can be considered as the decade of the development of devices and integrated circuits made of silicon and germanium devices.

The purpose of this book is to provide a comprehensive treatment of the technology and technology of *planar silicon devices*. To be sure, the physical principles and the operation of these devices do not differ from those of the technology of fabrication and the operation of devices made by other technologies. However, problems are to be very difficult to solve. To reduce the complexity of the problem, we concentrate on its most important features. For example, we concentrate on the alloy germanium diode, for instance, and the silicon diode. As a result, approximate characteristics of the former often give rise to observations on the latter. Most of the research is concentrated on those factors that are common to both alloy devices. In this one, the emphasis is on dealing with planar silicon devices.

After a brief description of the planar technology, the book is divided into three parts. The first one deals with the

for $V_D \leq V_{Dsat}$. Note that a high mobility is desirable for a large cut-off frequency as in the case of junction field-effect transistors.

c. Source-to-Drain Resistance in Saturation⁵

We have seen in the previous section that after saturation the potential at the end of the inversion layer—at the point X —will be fixed at the value V_{Dsat} . As the drain voltage is increased further, the reverse bias across the drain junction will increase. As a result, the depletion region separating point X from the drain will widen and the point X will move toward the source, as indicated in Figure 11.2c. Thus the effective channel length will become shorter and, as a result, the drain current will increase slightly with increasing drain voltage, resulting in an upward tilting of the current-voltage characteristics beyond saturation. This phenomenon is particularly prominent for devices with small channel length L .

d. Effect of Series Resistance

The same considerations that were applied in the case of junction field-effect transistors lead to the conclusion that the effect of unmodulated series resistances near the source and the drain will be to lower the observed channel conductance and transconductance as compared to their values without series resistances according to the formulas

$$g(\text{obs}) = \frac{g}{1 + (R_s + R_d)g} \quad [\text{Linear region}] \quad (11.23)$$

and

$$g_{msat}(\text{obs}) = \frac{g_{msat}}{1 + R_s g_{msat}}, \quad [\text{Saturation region}] \quad (11.24)$$

where g and g_{msat} denote the channel conductance and transconductance in the absence of series resistances.

Because in a surface field-effect transistor of the type illustrated in Figure 11.1 all of the channel region is under the influence of the gate, the series-resistance effect is considerably less important than in junction field-effect transistors.

11.4 OTHER TYPES OF SURFACE FIELD-EFFECT TRANSISTORS

The preceding discussion so far was for an n -channel device of the type where we have to apply a positive voltage to the gate in order to bring

about the onset of channel conduction. By complete analogy, the discussion could have been applied to a p -channel device where a negative gate voltage would have been required to bring about channel conduction. Because with zero gate voltage applied neither of these devices conducts, such devices are called *normally "off"* MOS transistors.

By contrast, a *normally "on"* device can be made by suitable control of the flat-band voltage. Thus, if V_{FB} is sufficiently negative in the case of an n -channel device or positive in the case of a p -channel device, a conducting channel exists even with zero gate voltage applied. In such a case, the channel conductance can be both increased and decreased with suitable variation of the gate voltage.

The normally "off" n - and p -channel devices as well as a normally "on" n -channel device are illustrated in Fig. 11.8. In all three devices the conducting channel is induced by surface fields, whether the surface fields are due to a gate voltage or to charges within the oxide. Thus we may call these devices *field-induced channel* devices. It is also possible to build-in a channel metallurgically. Two examples of such *metallurgical channel* devices are shown in Figure 11.9. The first of these, illustrated in Figure 11.9a, is made by epitaxially growing an n -type film on a p -type substrate.⁶ The conductivity between the source and drain regions is then modulated

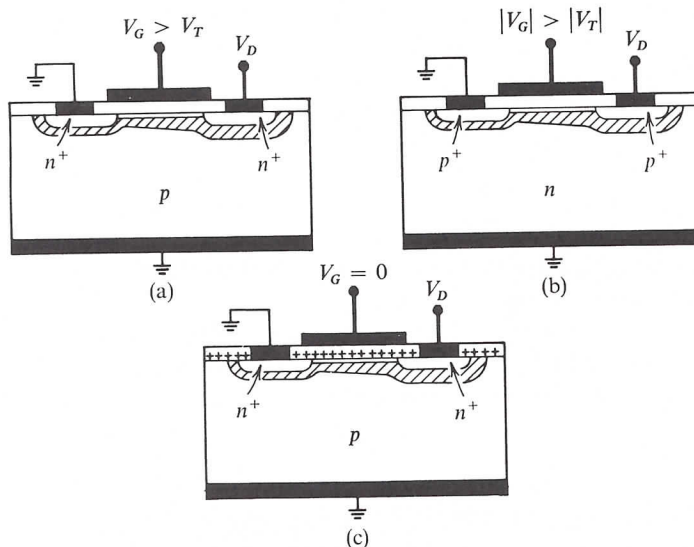


Fig. 11.8 Surface field-effect transistors with field-induced channels.
(a) Normally "off" n -channel device.
(b) Normally "off" p -channel device.
(c) Normally "on" n -channel device.

References Cited

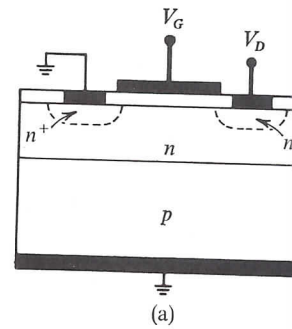


Fig. 11.9 Surface field-effect transistors with metallurgical channels.
(a) Epitaxially grown n -channel device.
(b) Silicon-on-sapphire n -channel device.

by the gate voltage. A positive gate voltage increases the cross-sectional area of the channel, while a negative gate voltage decreases it. In the normally "on" mode of operation, this surface field-effect transistor operates as a junction field effect transistor.

READING

MOS transistors are reviewed in *Microelectronic Applications*, J. T. Wallmark and H. J. Pao.

REFERENCES

1. J. E. Lilienfeld, U.S. Patent 1,745,199 (1929).
2. O. Heil, British Patent 439,457 (1935).
3. W. Shockley and G. L. Pearson, *Physics of Semiconductors by Surface Charge*, Wiley, New York, 1960.
4. D. Kahng and M. M. Atalla, "Silicon Surface Field-Effect Transistor," *IRE Solid-State Device Research Conference*, 1960.
5. This treatment follows that given by R. D. R. Fieser, "The Surface Field-Effect Transistor," *Stanford University Report*, 1661-1 (1961), and by H. K. J. Ilk, "The Surface Field-Effect Transistor," *Solid-State Electronics*, 10, 1 (1963). The characteristics of such devices are discussed by Heiman, "The Silicon Insulated-Gate Transistor," *IEEE Trans.*, 1963; and by C. T. Sah, "Characteristics of the Surface Field-Effect Transistor," *IEEE Trans.*, 1963.