

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.;
WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO., LTD.;
AND VISIONIX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case IPR2023-00941
U.S. Patent No. 7,414,599

PATENT OWNER'S PRELIMINARY RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit	Description
Ex. 2001	Certified File History for U.S. Patent No. 7,414,599
Ex. 2002	U.S. Patent Publication No. 2004/0041750 (“Abe”)
Ex. 2003	U.S. Patent Publication No. 2004/0145547 (“Oh”)
Ex. 2004	Digital Integrated Circuits, A Design Perspective 2 nd ed. (2003)
Ex. 2005	Claim Construction Order, Inv. No. 337-TA-1351

I. Introduction

Petitioner challenges all 18 claims of U.S. Patent No. 7,414,599 (Ex. 1001, the “’599 Patent”) based on only a single ground, which is based on only a single-reference, U.S. Patent Publication No. 2003/0132931 (Ex. 1002, “Kimura”). Out of Kimura’s 85-page disclosure with at least twenty-seven distinct embodiments and “embodiment modes,” Petitioner picks and chooses from unrelated embodiments and argues for combinations and modifications having no support in Kimura and that, on the contrary, contradict Kimura’s teachings. Not only do Petitioner’s arguments lack merit, but the circuits disclosed by Kimura were submitted to the Office during prosecution, and Petitioner fails to establish material error by the Office under *Advanced Bionics*. The Board should therefore exercise its discretion to deny the Petition under 35 U.S.C. § 325(d).

Moreover, as explained below, Petitioner’s arguments are flawed technically and legally. For example, Petitioner wrongly portrays “erasure” and “initialization” as referring to the same operation in Kimura’s pixel circuits, when Kimura teaches that they are separate and distinct operations; mischaracterizes Kimura’s disclosure about which transistors can share a signal line while maintaining the circuit’s operation; and disregards that CMOS technology (which uses both NMOS and PMOS transistors on the same semiconductor substrate) is a key feature of Kimura’s disclosed embodiments. Stripped of these errors, there is no rationale or

basis in Kimura for Petitioner’s obviousness arguments. Rather, Petition presents a flawed effort to reconstruct the inventions of the ’599 Patent through hindsight. For these reasons as well, the Board should deny institution.

II. The Board Should Exercise Its Discretion to Deny the Petition Under 35 U.S.C. § 325(d)

Discretionary denial under 35 U.S.C. § 325(d) is appropriate here, as the Petition’s sole ground is premised entirely on the prior art Kimura reference, whose Japanese counterpart (with the relevant figures and an English translation of the abstract) was repeatedly presented to the Office during prosecution. Under the precedential *Advanced Bionics* framework, “the same or substantially the same art” was before the Office during prosecution. *See Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020). And, as discussed further below, Petitioner’s conclusory assertions do not demonstrate that the Office erred in a manner material to patentability.

Indeed, the Petition devotes little space to addressing Section 325(d)—declaring that “[t]he ’599 patent prosecution history is short,” and then providing a cursory, one-page analysis (Pet. at 11–12). Yet Petitioner significantly mischaracterizes the prosecution history. During prosecution, while the claims were still pending, Kimura’s Japanese counterpart (Japanese Publication No. 2003-202833, hereinafter “JP Kimura”) was submitted to the Patent Office—identified by the Applicants in numerous submissions—and was explicitly signed off on by

the Examiner. Moreover, the sole basis on which Petitioner claims Kimura is not cumulative of the Dawson reference (relied upon by the Examiner for claim rejections) is that Kimura discloses “multiple circuits with five or more transistors.” Pet. at 12. Yet Petitioner disregards that the Examiner applied two other references disclosing circuits having five or more transistors. The Examiner correctly recognized that the claims of the ’599 Patent were allowable over the prior art, including the circuits on which Petitioner now relies. Petitioner has not shown, and could not show, material error.

A. The Same or Substantially the Same Art Was Previously Presented.

Pursuant to *Advanced Bionics* step 1, and as relevant to *Becton, Dickinson* factors (a), (b), and (d), the Kimura reference is at least substantially the same as art that was presented to the Office during prosecution—namely, JP Kimura. That reference—equipped with all of the specific circuit configurations now relied upon by Petitioner for its invalidity challenge—is included in its entirety in the ’599 Patent file history. *See* Ex. 1005 at 154–216.

Under *Advanced Bionics*, “[p]reviously presented art includes . . . art provided to the Office by an applicant, such as on an Information Disclosure Statement (IDS), in the prosecution history of the challenged patent.” *Advanced Bionics*, IPR2019-01469, Paper 6, at 7–8. Petitioner does not, and could not,

dispute that JP Kimura was provided to the Office by the applicant during prosecution.

Petitioner instead seeks to sidestep step 1 of *Advanced Bionics* by inaccurately arguing that JP Kimura “was identified in an IDS *after* the examiner indicated the claims were allowable.” Pet. at 12 (emphasis in original). In actuality, JP Kimura was submitted while a number of claims stood rejected, and nearly a year before the Examiner issued a Notice of Allowability. Nor does *Advanced Bionics* even acknowledge such a distinction as Petitioner would attempt to draw.

In fact, JP Kimura was identified to the Examiner on four separate occasions:

- On July 20, 2007, JP Kimura was first submitted, along with an English abstract of the reference as part of an Information Disclosure Statement (IDS). *See* Ex. 1005 at 81–84, 154–216. Subsequently, the Applicants filed an Amendment on October 12, 2007, *see id.* at 62–79, and the Examiner issued a second office action on January 17, 2008, *see id.* at 54–60.
- On March 20, 2008, the Applicants again brought JP Kimura to the Examiner’s attention, as part of their remarks accompanying a subsequent amendment. Ex. 1005 at 41 (directing the Examiner’s attention to the July 20, 2007 IDS).
- On April 19, 2008, two weeks after the Examiner issued a Notice of Allowability, *see* Ex. 1005 at 20–25, the Applicants flagged the IDS yet

again, asking the Office to “[p]lease acknowledge receipt and consideration of the July 20, 2007 IDS.” *Id.* at 13 (Amendment Under 37 CFR § 1.312). The Office also sent an internal memo requesting the Examiner to “[p]lease initial/line through citations.” *Id.* at 12.

- On May 12, 2008, an Office communication was issued, in which the Supervisory Examiner confirmed that the “IDS . . . has been considered.” Ex. 1005 at 9. The Supervisory Examiner also provided a signed version of the IDS listing JP Kimura, and confirmed “all references considered except where lined through,” as highlighted below. *Id.* at 10–11.

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
		EP 1 220 191	07-03-2002	Kwon	
		JP 2000-347621	12-15-2000	Kondo et al.	Patent Abstracts of Japan
		JP 2002-215096	07-31-2002	Kwon	Patent Abstracts of Japan
		JP 2002-244617	08-30-2002	Furumiya	Patent Abstracts of Japan
		JP 2003-173165	06-20-2003	Aoki	Patent Abstracts of Japan
		JP 2003-202833	07-18-2003	Kimura et al.	Patent Abstracts of Japan
		JP 2003-223138	08-08-2003	Kimura	Patent Abstracts of Japan
		JP 2004-133240	04-30-2004	Asano et al.	Patent Abstracts of Japan

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		European Search Report dated April 23, 2007, for EP 04090270.2, in the name of Samsung SDI Co., Ltd.
		Patent Abstracts of Japan, Publication No. 2000-347621, dated December 15, 2000, in the name of Yuji Kondo, et al.

EXAMINER SIGNATURE	/Alexander Eisen/	DATE CONSIDERED	05/08/2008
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English Language Translation is attached.

Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DBP/dg ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AE/

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As noted above, previously presented art includes “art provided to the Office . . . on an Information Disclosure Statement.” *Advanced Bionics* IPR2019-

01469, Paper 6, at 7–8. Here, the prior art disclosing the same circuitry now relied upon by Petitioner was included in an IDS submitted three times to the Examiner, and the Examiner explicitly confirmed that this art was among the “references considered.” Ex. 1005 at 10.

JP Kimura includes all of the same figures that are cited in the Petition—which clearly depict the five- and six-transistor circuit configurations on which Petitioner seeks to ground its obviousness arguments as well as the phases of operation of those circuits. *See* Ex. 1005 at 191–215, Figs. 16A–B, 17A–C, 33A–E, 34A–B, 36A–E. Additionally, the applicants submitted an English abstract of JP Kimura reference. Although the abstract is not included in the version of the file history submitted with the Petition (Ex. 1005), it appears in the certified copy of file history that was produced to Petitioner in parallel litigation, and is identified on the IDS. Ex. 2001 at 279–280.¹

Thus, the same or substantially the same art was previously presented to the Office. *See, e.g., Biocon Pharma Ltd. v. Novartis Pharmaceuticals Corp.*, IPR2020-01263, Paper 12 at 9 (PTAB Feb. 16, 2021) (“[W]e accept that the

¹ To the extent that the Petition makes arguments based on the text of the U.S.

Kimura publication (Ex. 1002), it fundamentally misinterprets the reference, as discussed below in Sections III and VI.

Examiner considered [the prior art at issue] because it is listed on the IDS and the Examiner signed the IDS with the statement ‘all references considered except where lined through.’” (citation omitted)).

B. Petitioner Does Not Demonstrate Office Material Error.

Under step 2 of *Advanced Bionics*, and pursuant to *Becton, Dickson* factors (c), (e), and (f), a petitioner who seeks to rely on previously presented art must “demonstrat[e] that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics*, IPR2019-01469, Paper 6, at 8. Petitioner makes no such showing.

Here, Petitioner argues only that Kimura is not cumulative of the Dawson reference (on which the Examiner relied to reject certain pending claims) on account of “Dawson ha[ving] only four transistors” whereas Kimura discloses “multiple circuits with five or more transistors.” Pet. at 12. From this, Petitioner summarily asserts that “the Patent Office erred in not applying Kimura (or any other reference) that even had the minimum number of transistors recited in the claims.” *Id.* at 13.

Petitioner’s implication—that the Examiner failed to consider the prior art of record disclosing circuits having at least five transistors—is incorrect. In fact, in the initial office action, the Examiner affirmatively identified not only Dawson, but two additional references that Petitioner ignores—U.S. Patent Publication No.

2004/0041750 (Ex. 2002, hereinafter “Abe”) and U.S. Patent Publication No. 2004/0145547 (Ex. 2003, hereinafter “Oh”). *See* Ex. 1005 at 300 (Examiner’s Notice of References Cited); *see also id.* at 288–89 (July 12, 2007 Office Action, attaching same). Importantly, both Abe and Oh include five-transistor pixel circuits. *See* Ex. 2002 at Fig. 19, ¶¶ 121–122; Fig. 26, ¶ 136; Fig. 32, ¶ 147; and Figs. 35–36, ¶ 155; *see also* Ex. 2003 at Fig. 6, ¶¶ 60–62; Fig. 9A, ¶¶ 71–72; and Fig. 10A, ¶¶ 76–79. The Examiner recognized that the specific claimed inventions of the ’599 Patent are allowable over such structures. For example, the Examiner concluded in this action that “***none of*** the prior art” disclosed the fourth and fifth transistors recited in prosecution claims 8–19, which issued as claims 7–18. Ex. 1005 at 294 (July 12, 2007 Office Action at 5) (emphasis added).² While the Examiner rejected other pending claims over the Dawson reference specifically, *id.* at 291, the Examiner’s broader statement about “none of the prior art” and attachment of the “Notice of References Cited” to the action, underscores that the five-transistor references of Abe and Oh were considered and evaluated with respect to all of the issued claims. Thus, contrary to Petitioner’s argument, the

² The Examiner likewise found that “[n]one of the prior art” disclosed the “fifth” and “sixth” transistors in prosecution claim 3, which ultimately were included in issued claim 1. Ex. 1005 at 294 (July 12, 2007 Office Action at 5).

Examiner explicitly considered prior art disclosing circuits having at least five transistors.

Accordingly, under Petitioner’s “transistor-count” criterion for assessing cumulativeness, Kimura is cumulative of at least three references that were previously presented to the Office and that disclose five-transistor circuits, two of which were affirmatively identified by the Examiner, and all of which were specifically signed off upon. *See* Ex. 1005 at 300 (listing Abe and Oh), 8–11 (listing JP Kimura).

In sum, the file history of the ’599 Patent demonstrates that the Examiner considered and evaluated multiple references disclosing five-transistor circuits while the claims were pending—namely, Abe and Oh, in addition to JP Kimura, yet did not consider any of them to raise a patentability issue as to the claims that the Examiner allowed. As to those claims, the logical inference from this record is *not* that the Examiner erred (let alone materially), but that the Examiner considered the information and—in light of the particular requirements of the claims including the specific “fourth” transistor and “fifth transistor,” which were not found in any of the prior art—determined that those claims are not obvious. Petitioner, with its bare-bones step 2 analysis based on a simplistic transistor-count criterion (Pet. at 13), fails to “point[] out sufficiently how the examiner erred in its evaluation of the asserted prior art” pursuant to *Becton, Dickinson* factor (d). *Cf. Nespresso USA,*

Inc. v. K-fee System GmbH, IPR2021-01223, Paper No. 9 at 31 (PTAB Jan. 18, 2022) (explaining that “[i]f reasonable minds can disagree regarding the purported treatment of the art or arguments” by the Examiner, then “it cannot be said that the Office erred in a manner material to patentability”; and concluding that “the paucity of analysis provided by Petitioner in the Petition tips the scales in favor of a discretionary denial.”).

Accordingly, the Board should exercise its discretion to deny the Petition Under 35 U.S.C. § 325(d).

III. Petitioner’s Understanding of Kimura Is Flawed

The obviousness theories set forth in the Petition are based on fundamental misunderstandings of Kimura’s disclosure. For clarity, before discussing the Petition’s obviousness theories in detail, Patent Owner provides the following corrective background on the reference.

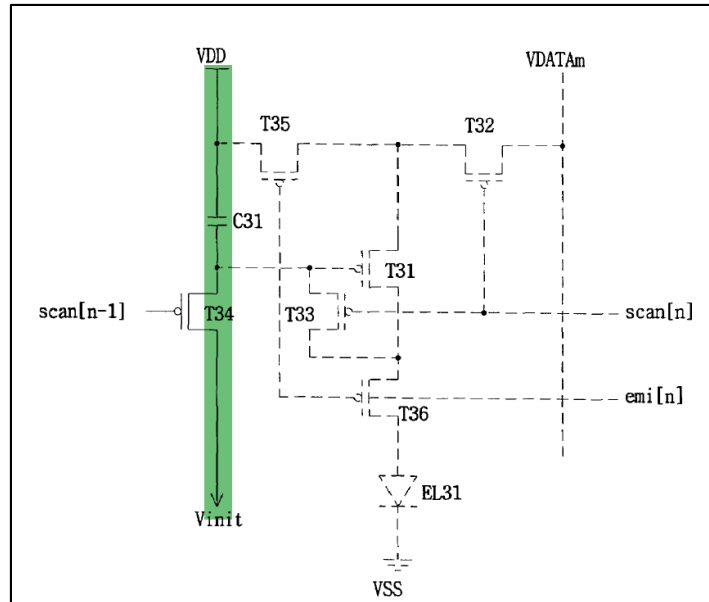
A. Petitioner Incorrectly Describes Figures 33 and 36 of Kimura as Involving “Initialization.”

Kimura is an 85-page reference that is directed to active matrix LED devices using CMOS semiconductor technology, and the manufacture, design and operation of pixel circuits for use in this context. *See e.g.*, Kimura at ¶¶ 1, 502. It includes twenty-seven embodiments and “embodiment modes,” as well as forty-four numbered figures (many containing upwards of five separate diagrams each). As the “baseline circuit for Petitioner’s patentability analysis” (Pet. at 15),

Petitioner relies on Figure 33 of Kimura—although Petitioner provides no reason why a person of ordinary skill in the art would choose to start with this design, which is not identified by Kimura as holding any particular promise. In fact, as discussed further below, Kimura itself notes a critical flaw in the circuit design of Figure 33 (which it attempts to correct in later embodiments), that would lead to light output at undesired times and thus undermine the goal of the pixel circuit. Not only that, but Petitioner mischaracterizes Kimura’s disclosure with respect to the operation of this circuit.

The circuit’s operation is illustrated in Figures 33B through 33E. Petitioner, determined to try to relate Figure 33 of Kimura to the materially different pixel circuit of Figure 3 of the challenged ’599 Patent, characterizes Kimura’s Figure 33 as having the same three operational phases as are taught in the ’599 Patent: “programming” (Figs. 33C and 33D), “light emitting” (Fig. 33E) and “initialization” (Fig. 33B). But this is inaccurate. In actuality, the Kimura circuit operates quite differently from the driving circuit of the ’599 Patent, particularly with respect to the ’599 Patent’s “initialization” phase.

In the ’599 Patent, “initialization” refers to the process of resetting the data signal stored on capacitor C31 by setting it to a known initialization voltage—i.e., Vinit. This is illustrated in Figure 5 below.

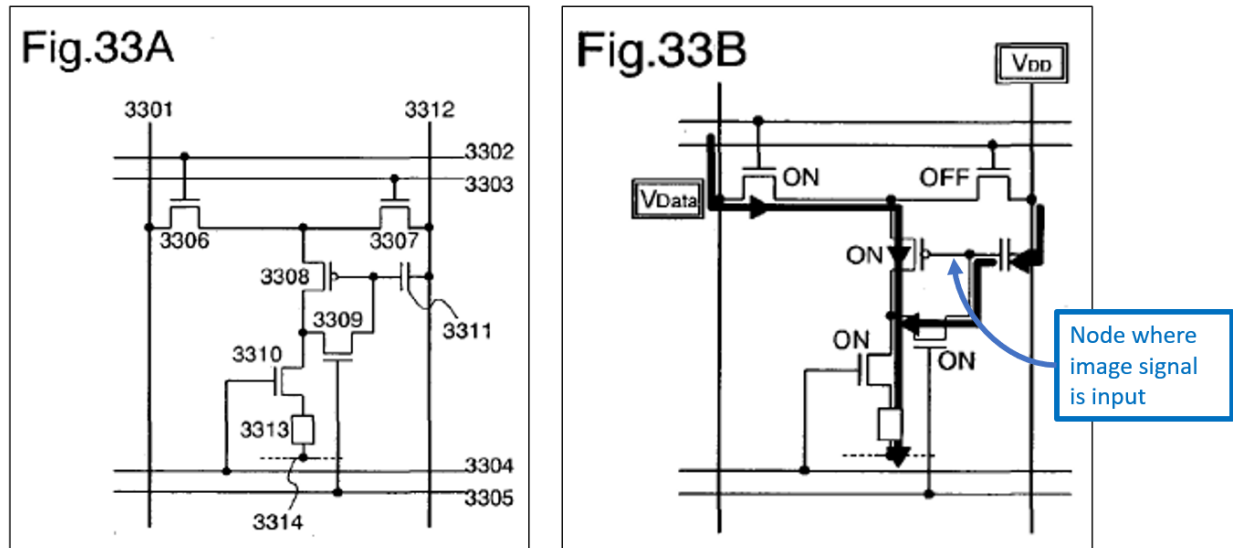


'599 Patent Fig. 5
(highlighted to indicate the initialization path)

The '599 Patent explains that, “in an initialization operation, . . . an initialization path (as indicated by a solid line shown in FIG. 5) is formed. Accordingly, the data signal that has been stored in capacitor C31, namely, a gate voltage of driving transistor T31, is initialized.” '599 Patent at 7:15–26; *see also id.* at 7:3–6 (“initialization transistor T34 [is] for initializing the data signal stored in capacitor C31”); *id.* at 2:41–49 (explaining, with respect to prior art Fig. 1, that “the data stored in capacitor C11 is initialized through transistor T12 to initialization voltage Vin[it].”).

The circuit of Kimura Figure 33 does not have such an initialization phase. Petitioner asserts that “initialization” is shown in Figure 33B, but nothing in

Kimura teaches or suggests that Figure 33B (shown below alongside Figure 33A) involves initialization or storing a default voltage on a capacitor.



Rather, Kimura explains the operation of Figure 33B as follows:

First, the TFT [transistor³] 3306 turns on and an *image signal VData is input as shown in FIG. 33B*. In addition, the TFT 3309 and a TFT 3310 turn on, and the TFT 3308 thus behaves as a diode connected TFT.

Kimura at ¶ 655 (emphasis added). That is, Figure 33B is described as being part of a *programming* phase, in which Kimura seeks to store its *image signal* (“Vdata”) on the capacitor.

³ Kimura refers to its transistors as “TFTs,” using an abbreviation for thin film transistor. *See* Kimura at ¶ 1.

As mentioned, Kimura discusses many different pixel circuits, and for certain other embodiments, which are unrelated to the embodiment of Figure 33, Kimura *does* discuss a process of “initialization” in which a reset voltage (“VReset”) is applied to a capacitor or gate of a driving transistor. *See, e.g.*, Kimura at ¶¶ 425–426 (discussing Figure 17). But it never describes the embodiment of Figure 33 as including such an initialization step (or resetting a capacitor with VReset or any other default voltage).

Accordingly, Petitioner mischaracterizes the reference in arguing that in the circuit of Figure 33 “Kimura discloses . . . reset[ting] the capacitor voltage to a default initialization value.” Pet. at 18, 51. Petitioner cites to Paragraph 658 of Kimura as its only basis for this assertion, but this paragraph makes no mention of the capacitor or of initialization.

Petitioner’s error appears to stem from misunderstanding Kimura’s statement in Paragraph 658 that “TFT 3310 can also be used as an erasure TFT.” Importantly, Kimura discusses “erasure” and “initialization” as separate operations and concepts. Whereas “initialization” in Kimura entails applying a reset voltage (“VReset”) to a capacitor or gate electrode (*see, e.g.*, Kimura at ¶¶ 425–426), Kimura describes “erasure” as “forcibly plac[ing] [the EL device] in a non-light-emitting state.” Kimura at ¶ 410. Indeed, as shown below, Kimura depicts “erasure” and “initialization” as distinct operations in its Figure 16B. Despite this

distinction, Petitioner wrongly treats Kimura’s discussion of “erasure” as being synonymous with “initialization,” as discussed further below.

Petitioner makes the same errors in discussing Figure 36—alleging that this embodiment includes a “dedicated initialization transistor” (TFT 3612) and that Fig. 36B shows that “during initialization, the capacitor discharges through [that] transistor instead of the light emitting element.” Pet. at 19. While Petitioner cites to Paragraphs 666–667 of Kimura for this allegation, those paragraphs make no mention of the capacitor, let alone state that its voltage is initialized to a fixed value. On the contrary, Paragraph 666 states that the additional TFT 3612 helps prevent unintended light emission “*during the input of the image signal*” (emphasis added)—i.e., as part of the programming operation. Paragraph 667 notes that “[i]t is also possible to use the TFT 3611 as an erasure TFT.” As discussed above, erasure is distinct from initialization, and Petitioner’s conflating of these two distinct operations misreads Kimura.

Petitioner’s misreading of Kimura is foundational to its obviousness arguments. It supplies the basis for Petitioner’s only proposed motivation to incorporate features of the embodiment of Figures 16–17 with the circuit of Figure 33. In fact, contrary to Petitioner’s assertions, Figure 33 does *not* include an initialization operation, and Figures 16–17 reflect a different type of circuit design which *does* include an initialization operation. When Kimura is read according to

its actual disclosures, Petitioner has identified no reason to combine these entirely different and disconnected designs, let alone in a way that would have resulted in the claimed inventions of the '599 Patent. Simply put, a person of ordinary skill in the art would not have had any reason to do so, let alone a reasonable expectation of success.

B. Petitioner Conflates “Initialization” with “Erasure.”

In seeking to portray the embodiment of Figure 33 as including an “initialization” phase, Petitioner asserts that Kimura uses the terms “erasure” and “initialization” interchangeably to refer to a process of “reset[ting] the capacitor voltage to a default initialization value.” Pet. at 18; *see also id.* at 18 n.4 (“Kimura also calls this [initialization] ‘reset’ (*see* Fig. 1B) and ‘erasure’ (*see* ¶ 658.”)). This is incorrect. Kimura deliberately uses these different terms, “initialization” and “erasure,” to refer to different operations.

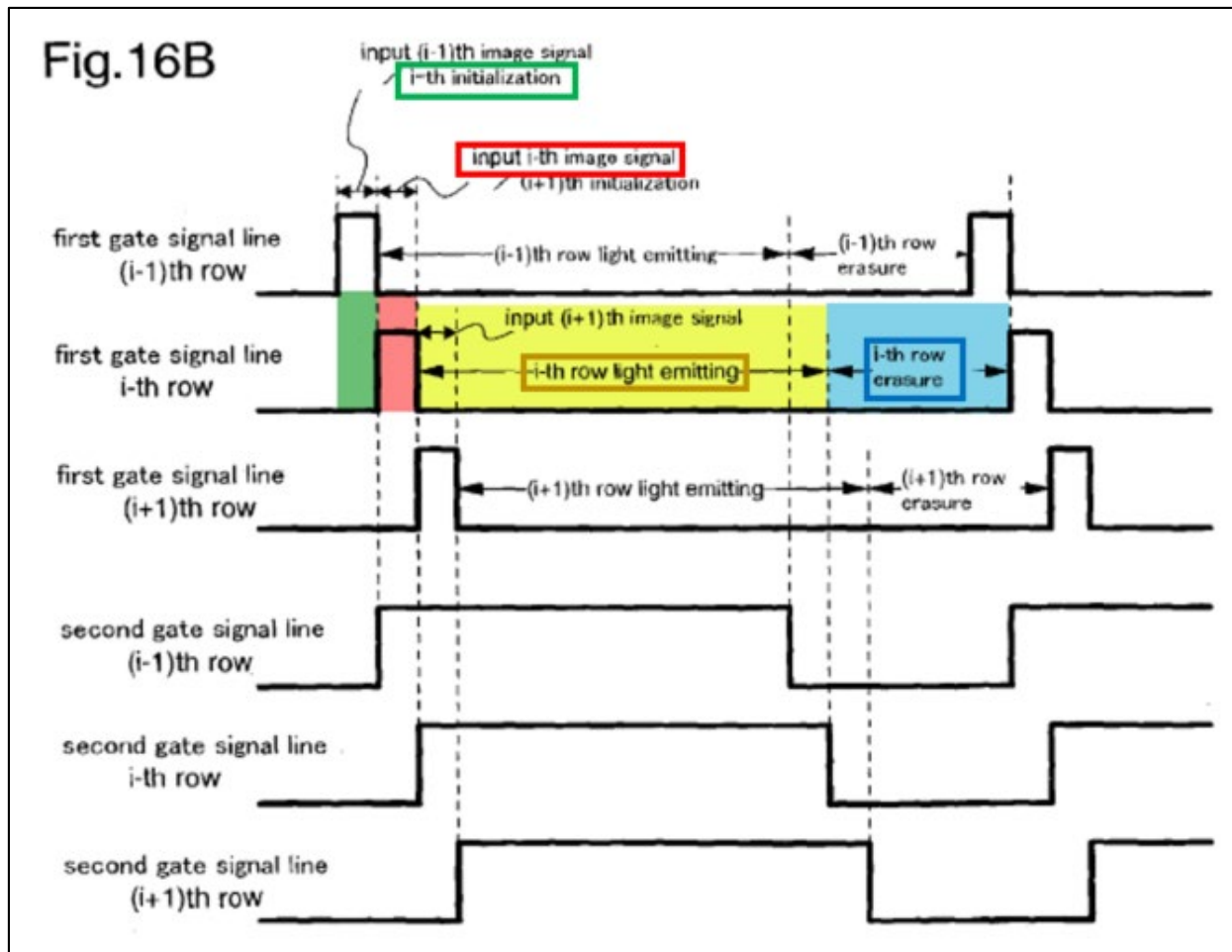
Kimura uses “erasure” to mean “forcibly plac[ing] [the EL device] in a non-light-emitting state. Kimura at ¶ 410. In certain embodiments, Kimura discloses use of an “erasure period” in which “electric current to the EL device [is] cutoff.” Kimura at ¶ 415. This period is used to resolve timing issues that can arise in certain embodiments. *See generally* Kimura at ¶ 406 (explaining that “normal display becomes impossible” in instances “when the address (write in) periods of different subframe periods overlap”; and that “[t]he erasure period is formed in

order to resolve these kinds of problems, and is formed so that two different address (write in) periods do not overlap after sustain (light emitting) periods”).

Kimura identifies an “erasure TFT,” in turn, as a transistor that permits “electric current supplied to the EL device [to] be cut off at an arbitrary timing.” Kimura at ¶ 658; *see also id.* at ¶ 415 (“The erasure TFT 914 is off during . . . the erasure period, and electric current to the EL device 909 is thus cutoff.”), ¶ 688 (“It is also possible to use a TFT 3912 . . . as an erasure TFT here. An electric current path to the EL device 3916 can be cut off by turning the TFT 3912 off.”).

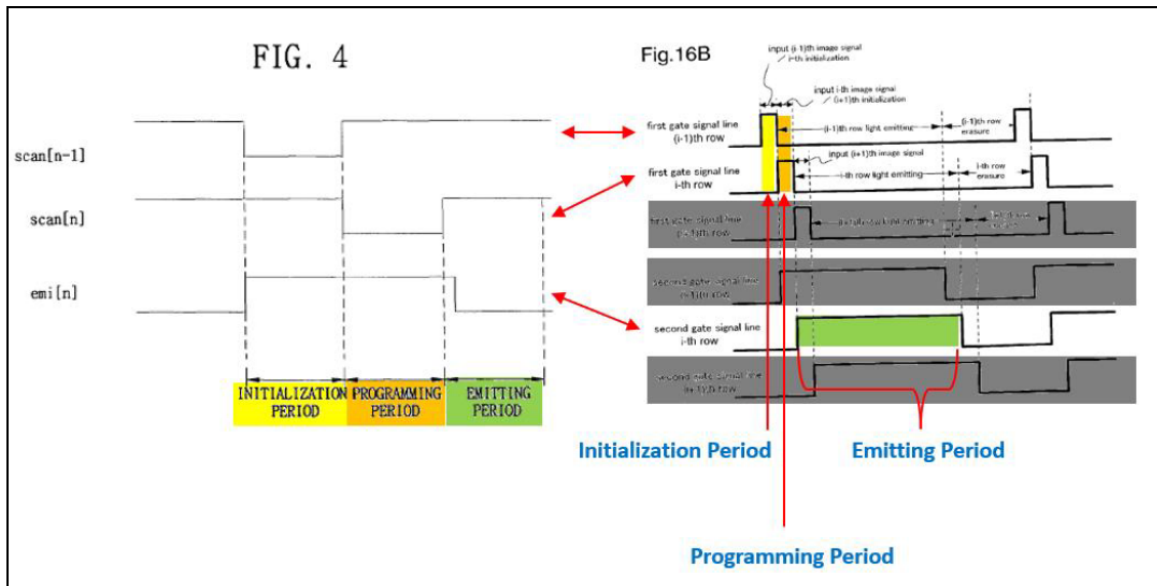
Thus, Petitioner makes a critical error in claiming that Kimura uses “erasure” as a synonym for initialization, and that Kimura’s “erasure TFT” is used to “reset[] the capacitor voltage to a default initialization value.” Pet. at 18.

Kimura discusses a different operation, and concept, of “initialization” with respect to certain embodiments, such as the embodiment of Figures 16–17. It does *not* use this term interchangeably with erasure. In fact, the dissimilarity between “erasure” and “initialization” is starkly illustrated in Figure 16B, on which Petitioner seeks to rely. *See* Pet. at 55–56, 64, 82, 91. As shown below (with annotations highlighting the initialization in green and the erasure in blue), this figure separately identifies “erasure” and “initialization” as distinct operational phases.



Kimura Fig. 16B (with periods for the i -th row highlighted to show the distinction between “initialization” and “erasure”)

In fact, Petitioner’s expert seeks to analogize Figure 4 of the ’599 Patent (showing designated periods of “initialization,” “programming,” and “emitting” periods), with Figure 16B of Kimura, using the following side-by-side comparison. *See* Ex. 1003 at ¶ 142. However, Dr. Foty’s analysis of Figure 16B neglects the “erasure period,” which is tellingly left un-highlighted and not otherwise discussed:



'599 Patent Fig. 4 and Kimura Fig. 16B
as annotated by Dr. Foty (Ex. 1003 at ¶ 142)

Turning back to Figure 33, Petitioner is therefore wrong to assert that:

Kimura discloses that the fifth transistor “can also be used as an erasure [transistor]” that resets the capacitor voltage to a default initialization value. EX1002, [0658].

Pet. at 18. Nothing in Kimura teaches or suggests that the transistor “resets the capacitor voltage to a default initialization value.” Rather, Kimura’s statement that this transistor “can also be used as an erasure TFT” means that it can be used to “forcibly place[] [the EL device] in a non-light-emitting state.” Kimura at ¶ 410. Indeed, this is evident from the very paragraph cited by Petitioner in the block quote above, which states that the “erasure TFT can be placed in any location, provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing.” Kimura at ¶ 658 (emphasis added).

Thus, in Kimura, “erasure” means forcibly placing the EL device in a non-light-emitting state (rather than initialization); and an “erasure TFT” is a transistor that permits cutting off current supplied to the EL device at an arbitrary timing. This is different from an “initialization transistor,” or a transistor “that resets the capacitor voltage to a default initialization value,” as Petitioner mistakenly asserts. Pet. at 18.

IV. Claim Construction

Patent Owner notes that on September 11, 2023, the Administrative Law Judge in the related ITC Investigation No. 337-TA-1351 issued a claim construction order construing certain claim terms of the ’599 Patent. *See* Ex. 2005 at 15-16, 39–45.

For purposes of this Preliminary Response, however, Patent Owner does not believe that any specialized constructions are necessary. Petitioner fails to establish a reasonable likelihood of prevailing under any claim interpretation.

V. Level of Ordinary Skill in the Art

Patent Owner notes that, in its September 11, 2023 claim construction order in the related ITC Investigation No. 337-TA-1351, the Administrative Law Judge agreed with Patent Owner’s proposal that, as to the ’599 Patent, a person of ordinary skill in the art (“POSITA”) would have had a relevant degree in Electrical Engineering, Computer Engineering, Materials Science, Physics, or the like, and

experience in active matrix display design and electroluminescence. *See* Ex. 2005 at 12–13.

For purposes of this Preliminary Response, however, Patent Owner does not believe it necessary to dispute the level of ordinary skill in the art.

VI. Petitioner Has Not Established a Reasonable Likelihood of Prevailing as to Any Challenged Claim

Petitioner presents only a single ground of unpatentability—obviousness over Kimura. But as it walks through the challenged claims, Petitioner advances a number of disparate and conflicting theories, purporting to draw from various unrelated embodiments appearing in this 85-page reference. As explained below, these theories all suffer from fundamental flaws. Accordingly, Petitioner does not establish a reasonable likelihood of prevailing as to any challenged claim.

The Petition addresses the claims in an unconventional order. In an effort to avoid confusion, this Preliminary Response seeks to adhere to that order.

First, the Petition begins with the circuit of Kimura’s Figure 33, which is a CMOS circuit consisting of one PMOS transistor and four NMOS transistors, and proposes to replace each of its four NMOS transistors with PMOS transistors. Pet. at 21. Petitioner argues that changing Kimura’s CMOS circuit to a so-called “all-PMOS implementation of Fig. 33” would “have been a simple and obvious design choice.” This “all-PMOS” redesign of what Kimura designed as a CMOS circuit in Figure 33 serves as the “baseline circuit for Petitioner’s patentability analysis.” Pet.

at 15. That is, Petitioner relies on the all-PMOS modification for every challenged claim, beginning on page 23 (for claim 7).

As explained in Subsection A below, not only is such an all-PMOS redesign not taught or suggested anywhere in Kimura, it is in fact contrary to Kimura's teachings. Petitioner disregards, among other things, Kimura's extensive disclosures of CMOS circuitry and manufacturing processes and the advantages associated with them. An assertion of "design choice," moreover, cannot make up for the shortcomings in the prior art. Because Petitioner relies on this unsupported modification for every challenged claim, it fails to establish a likelihood of prevailing on any of them for this reason alone.

Second, for the claims requiring an "initialization transistor" (claims 2, 8, 16, and 18), and beginning on page 49 of the Petition (for claim 8), Petitioner relies on still further alterations inconsistent with the disclosures of Kimura. Petitioner asserts that its "all-PMOS" modification of Figure 33 could be further modified to incorporate features from an unrelated embodiment of a different CMOS circuit shown in Figures 16–17. As a basis for this change, Petitioner cites a shortcoming of Figure 33 that Kimura identifies (unwanted light emission during programming). *See* Pet. at 51. Notably, however, Kimura not only identified the problem, it explicitly provided the solution, explaining that this problem is solved

by using the circuit of Figure 36. And yet, Petitioner disregards Kimura's express solution.

Petitioner argues that "[a]nother solution" appears in the unrelated embodiment of Figures 16–17, Pet at. 19, and seeks to incorporate features of this embodiment into the "all-PMOS" Figure 33, *id.* at 51–56. But as explained in Subsection B below, there are numerous flaws in Petitioner's reasoning. Petitioner fails to explain why a POSITA would eschew the solution that Kimura explicitly provides to this very problem with Figure 36 and seek a different solution to the problem Kimura already solved. And, even if a POSITA looked for a different solution, Petitioner fails to demonstrate a reason to take particular features (but not others) from the CMOS circuit of Figures 16–17, when Kimura in no way singles out this embodiment as having a particular feature that may be used elsewhere. Moreover, the proposed motivation to combine Figure 33 with the unrelated embodiment of Figures 16–17 is based solely on Petitioner's mistaken premise that "erasure" in Kimura (as referenced in Figure 33) is equivalent to "initialization" (as discussed for Figures 16–17), when as shown above "erasure" and "initialization" are different operations in Kimura. A POSITA would not make the mistake that Petitioner does. When Kimura is read correctly, it becomes clear that no such motivation exists.

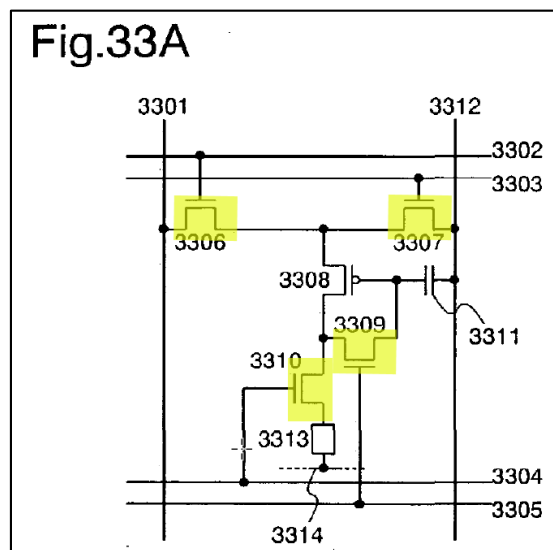
Third, for the claims requiring that the “current light-emitting signal” control the fourth and fifth transistors (claims 13–18) or fifth and sixth transistors (claims 1–6), and beginning on page 62 (for claim 13), Petitioner seeks to turn back to the CMOS circuit of Kimura’s Figure 36—the very embodiment that it disregards for the “initialization transistor” claims. Petitioner argues that that an “all-PMOS version of Kimura Fig. 36 . . . renders claim 13 obvious,” Pet. at 62–63, based on a theory that would further require modifying the signal lines of this circuit.

As explained in Subsection C below, Petitioner’s modifications of Kimura’s Figure 36 are inconsistent with Kimura, and a POSITA would have had no reason to make them. Moreover, Petitioner’s patched-together argument illustrates its failure to consider claims of the ’599 Patent as a whole, as it leads to inconsistent theories for meeting different claim limitations recited in a given claim. That is, Petitioner attempts to rely on Figure 36 for the “current light-emitting signal” limitation; even while it disregards that figure and proposes “another solution” based on Figures 16–17 for the “initialization transistor” limitation. But Petitioner never tries to reconcile its different theories for the two limitations, based on two competing embodiments, even though both limitations appear together in claims 2, 16, and 18. The result is an internal inconsistency and unresolved conflict for those claims, as to what embodiments and modifications are even being applied.

A. Converting Kimura Figure 33 to an “All-PMOS” Circuit (All Challenged Claims)

The Petitioner’s arguments all begin with Kimura’s Figure 33, but Petitioner provides no reason why a POSITA would choose to start with this design. In fact, as discussed further below, Kimura itself notes a critical flaw in the circuit design of Figure 33 that would lead to light output at undesired times, and proposes the circuit of Figure 36 as a solution to this problem. Nevertheless, Petitioner uses Figure 33 as the “baseline circuit for Petitioner’s patentability analysis.” Pet. at 15.

As shown below, Kimura’s Figure 33 is a CMOS circuit that uses NMOS transistors for each of TFTs (transistors) 3306, 3307, 3309, and 3310.⁴



Kimura Fig. 33 (with NMOS TFTs highlighted)

⁴ TFT 3308 includes a circle at its gate electrode to indicate that it is a PMOS transistor, whereas TFTs 3306, 3307, 3309, and 3310 (NMOS transistors) do not.

Petitioner seeks to replace all four NMOS transistors of the Figure 33 circuit with PMOS transistors. Pet. at 19–22. As to a subset of claims requiring a sixth “initialization transistor,” Petitioner proposes a further modification of Figure 33 that requires replacing a total of *five* NMOS transistors with PMOS transistors. *See, e.g., id.* at 53. Petitioner relies on these “all-PMOS” redesigns for all challenged claims. Yet nothing in Kimura teaches or suggests such circuits, and the assortment of theories alleged by Petitioner would not give a POSITA reason to make the required modifications.

1. Kimura’s “opposite polarity” disclosure for the “first” and “fourth” transistors teaches away from an “all-PMOS” design.

In seeking to justify its “all-PMOS” redesign of Figure 33, Petitioner largely cites to “broad teachings” in Kimura about the supposed interchangeability of NMOS and PMOS transistors (Pet. at 20), and statements in the reference about certain transistors appearing in embodiments *other* than Figure 33. *See* Pet. at 19–21.

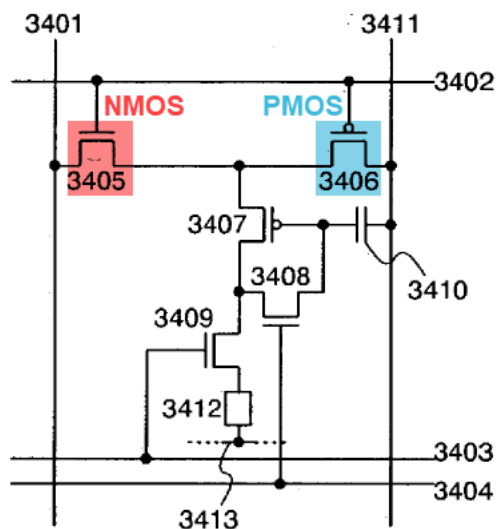
In fact, Petitioner only cites one PMOS teaching in Kimura that relates to Figure 33, arguing that “Kimura expressly discloses replacing the **first or fourth transistor** in Fig. 33 with PMOS.” Pet. at 20–21 (citing Kimura at ¶ 659 and Fig. 34A) (emphasis in original). But this disclosure does not support replacing *both* of the corresponding NMOS transistors in Figure 33 with PMOS transistors, as would

be needed for an all-PMOS redesign. Rather, it teaches that using PMOS for one of these transistors *but not the other* enables for a reduction in gate signal lines:

Furthermore, a gate signal line for controlling a TFT can be shared among a plurality of TFTs, as shown in FIGS. 34A and 34B. For example, the TFT 3306 and the TFT 3307 are controlled so as to turn on and off at mutually opposite timings, and therefore ***the polarity of one of the TFTs may be made opposite to the polarity of the other TFT***, and both of the TFTs can thus be controlled by the same gate signal line 3402, as shown in FIG. 34A.

Kimura at ¶ 659. That is, by using a *combination* of NMOS *and* PMOS for TFTs 3306 and 3307 in Figure 33 (the alleged “first” and “fourth” transistors), a single gate signal line can be used to control them. This is illustrated in Figure 34A, where NMOS TFT 3405 and PMOS TFT 3406 are controlled by a single gate line, 3402:

Fig.34A



Kimura Fig. 34A
(with NMOS TFT 3405 and PMOS TFT 3406 highlighted)

Indeed, it is this *difference in polarity*—i.e., one transistor being PMOS *while the other is NMOS*—that leads to the beneficial signal-line sharing capability that Kimura discusses. And, as Petitioner stresses, “Kimura itself [teaches] that reducing the number of control lines improves aperture ratio.” Pet. at 65 (citing Kimura at ¶¶ 429, 421–422). Yet this beneficial signal-line sharing capability would be lost if Petitioner’s all-PMOS configuration were pursued, as different signal lines would be necessary to ensure that the two transistors continue to have inverted timing. Accordingly, Kimura’s disclosure would not motivate a POSITA to replace both the first and fourth transistors with PMOS transistors. If anything, it teaches away from such a modification. *See In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994) (A reference teaches away “when a person of ordinary skill, upon

reading the reference . . . would be led in a direction divergent from the path that was taken by the applicant.”).

2. Design choice considerations cannot support replacing four of the five transistors in Figure 33.

Apart from Kimura’s disclosure of using “opposite polarity” transistors for TFTs 3306 and 3307 (the alleged “first” and “fourth” transistors)—which, as discussed above, counsels against Petitioner’s proposed modifications since it requires the pixel circuit to use both NMOS and PMOS transistors—there is nothing in Kimura that would give a POSITA reason to replace any of the TFTs in Figure 33 with PMOS transistors. Instead, Petitioner’s obviousness theory is grounded on alleged “interchangeability” of NMOS and PMOS transistors. Petitioner argues that “Kimura repeatedly and expressly teaches the interchangeability of NMOS and PMOS transistors used as switches,” Pet. at 19–20, and points to instances in which Kimura discusses the use of PMOS for certain switching transistors in embodiments *other* than Figure 33, *id.* at 20–21.

This amounts to a design choice argument—that because switching transistors are “interchangeable,” it would have been obvious to modify Figure 33 by using PMOS transistors in place of NMOS transistors 3306, 3307, 3309, and 3310 (and, for certain dependent claims, the PMOS “initialization transistor” that Petitioner seeks to add based on an NMOS transistor appearing in Figures 16–17). Indeed, Petitioner repeatedly invokes the design choice rationale, concluding that

“[a]pplying Kimura’s express teachings (and/or POSITA knowledge) to create an all-PMOS implementation of Figure 33 would have been a *simple and obvious design choice*.” Pet. at 21 (emphasis added).

But Petitioner’s all-PMOS version of Figure 33 is not a “simple design choice.” As an initial matter, Petitioner’s proposal does not involve a choice between two alleged alternatives (NMOS versus PMOS) for one switching transistor of a pixel circuit.⁵ Instead, the proposal requires that PMOS transistors be chosen not once, but four (or five) times, and is thus one of sixteen (or thirty-two) distinct permutations of NMOS and PMOS transistors for the five-transistor circuit of Figure 33.

And because NMOS and PMOS transistors are, in fact, structurally and operationally different, “design choice” considerations cannot substitute for teachings or suggestions in the prior art. *See, e.g., In re Gal*, 980 F.2d 717, 719–20

⁵ *Cf. Uber Technologies Inc. v. XOne, Inc.*, 957 F.3d 1334, 1340 (Fed. Cir. 2020) (finding that proposed combination implementing one of *only two* available, predictable solutions, provided the POSITA with a “simple design choice”) (citation omitted); *ACCO Brands Corp. v. Fellowes, Inc.*, 813 F.3d 1361, 1367 (Fed. Cir. 2016) (finding that each of “*two* design choices [wa]s an obviousness combination of prior-art elements” (emphasis added)).

(Fed. Cir. 1992) (reversing Board finding of “obvious design choice” where the claimed structure and the function it performs are different from the prior art). Indeed, PTAB panels have denied institution based on this principle, explaining that “a finding of obviousness based on design choice is precluded where the difference between the claimed feature and prior art results in a functional difference.” *Lumenis Be Ltd. v. BTL Healthcare Technologies A.S.*, IPR2021-01275, Paper No. 8 at 30 (PTAB Feb. 8, 2022); *Unified Patents Inc. v. Velos Media, LLC*, IPR2019-00749, Paper No. 7, at 11–12 (PTAB Oct. 15, 2019).

As Petitioner acknowledges, NMOS transistors turn on by an “active high” gate signal whereas PMOS transistors turn on by an “active low” signal. Pet. at 4. This is a significant functional difference. For example, an “all PMOS” circuit would preclude the reduction in gate lines discussed in the prior subsection (for the alleged “first” and “fourth” transistors made possible by having them have opposite polarities) and may thus require additional gate lines. *See generally* Section VI.A.1, above. As Petitioner also acknowledges, “Kimura itself [teaches that] reducing the number of control lines improves aperture ratio.” Pet. at 65 (discussing claim 13, citing Kimura at ¶¶ 429, 421–422).

Additionally, an “active low” signaling scheme would require corresponding changes to the driver circuit that sends the selection gate signals to the pixel circuits. The timing of these signals is critical to the overall operation of the

display. For example, it was known at the relevant time that PMOS transistors are slower in operation as compared to NMOS transistors. *See, e.g.*, Ex. 2004 at 17 (“NMOS-only logic[] has the advantage of higher speed over the PMOS logic”).

Yet Petitioner all but ignores these considerations. It merely asserts in a footnote, without explanation, that “[o]f course, an all-PMOS implementation requires active-low signaling, but that was well-known to a POSITA and would have been trivial to implement.” Pet. at 21, n.5. Although Petitioner cites paragraphs 154 and 57 of its expert declaration for this statement, the assertions in those paragraphs are similarly conclusory, and therefore are “entitled to little to no weight” under 37 C.F.R. § 42.65(a); *see also Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9, at 15 (PTAB Aug. 24, 2022) (precedential) (denying institution, rejecting expert testimony that “adds little to the conclusory assertion for which it is offered to support”).

In light of these design considerations posed by Petitioner’s proposed all-PMOS conversion—number of gate lines, aperture ratio, drive circuitry, signaling and timing scheme, operating speed for PMOS versus NMOS devices—a finding of obviousness based on “design choice” considerations here would be inappropriate. *See, e.g., Philip Morris Products S.A. v. International Trade Commission*, 63 F.4th 1328, 1346-48 (Fed. Cir. 2023) (upholding Commission’s nonobviousness ruling, where Commission found that “the heater design in an

electronic cigarette” entailed a “multitude of design considerations” and “was anything but a ‘simple design choice,’” noting that Appellant failed to demonstrate that the claimed invention was one of only three design choices).

In relying on this design choice theory, Petitioner provides no “articulated reasoning with []rational underpinning” (*TQ Delta, LLC v. CISCO Systems, Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019)) as to why a POSITA would have been motivated to replace *all* of TFTs 3306, 3307, 3309, and 3310 to arrive at its all-PMOS redesign. Instead, Petitioner’s “interchangeability” arguments amount to a suggestion that a POSITA *could* have modified the various transistors.⁶ But that is inadequate. Indeed, the Federal Circuit has specifically rejected obviousness arguments where, as here, the expert’s “testimony primarily consisted of

⁶ This standard is invoked repeatedly by Petitioner’s expert. *See, e.g.*, Ex. 1003

¶ 16 (“That is, if the POSITA *could* have adapted the reference to meet the claims of the patent by applying known concepts to achieve expected results, then the patent claims are rendered obvious by that reference.”), ¶ 146 (“[A] POSITA would understand . . . that these nMOS transistors *could* readily be replaced with pMOS transistors.”), ¶ 359 (“replac[ing] these nMOS switching transistors with pMOS switching transistors . . . *could* be carried out (as a POSITA would understand).”) (all emphasis added).

conclusory references to her belief that one of ordinary skill *could* combine the references, not that they *would* have been motivated to do so.” *InTouch Technologies, Inc. v. VGO Communications, Inc.*, 751 F.3d 1327, 1352 (Fed. Cir. 2014) (emphasis in original); *see also Polaris Industries, Inc. v. Arctic Cat, Inc.*, 822 F.3d 1056, 1068–69 (Fed. Cir. 2018) (overturning PTAB’s obviousness determination, where “the Board focused on what a skilled artisan would have been *able* to do, rather than what a skilled artisan would have been *motivated* to do at the time of the invention” (emphasis in original)).

3. The unrelated “Kimura ’798” reference does not support a PMOS modification for the “third” or “sixth” transistors.

As to the “third” and “sixth” transistors, Petitioner advances a different theory. In addition to asserting that “changing the third transistor to PMOS in Kimura Fig. 33, was a simple design choice,” Pet at 21, Petitioner argues that “it would have been ‘advantageous’ to ‘manufactur[e] all TFTs [] of the same type,’” citing a passing statement in an unrelated reference. Pet. at 21 (quoting Ex. 1004 at 12:30–49); *see also id.* at 53 (advancing similar argument for the “sixth” initialization transistor appearing in certain claims). This argument fails for a number of reasons.

As an initial matter, Petitioner’s logic on this point is circular. For the sixth transistor, e.g., it argues: “*Given that all other transistors in the All-PMOS*

implementation are PMOS devices, a POSITA would have been motivated to implement the initialization transistor as a PMOS device.” Pet. at 53 (emphasis added). This assumes a contrived scenario in which a POSITA is only permitted to consider the alleged “manufacturing advantage” of an all-PMOS design *after* having already changed all of the other NMOS transistors in Figure 33 to PMOS transistors (for no reason). If anything, Petitioner’s logic would suggest converting Figure 33 into an “all-NMOS” circuit, as Figure 33 has four-NMOS transistors versus just one PMOS transistor.

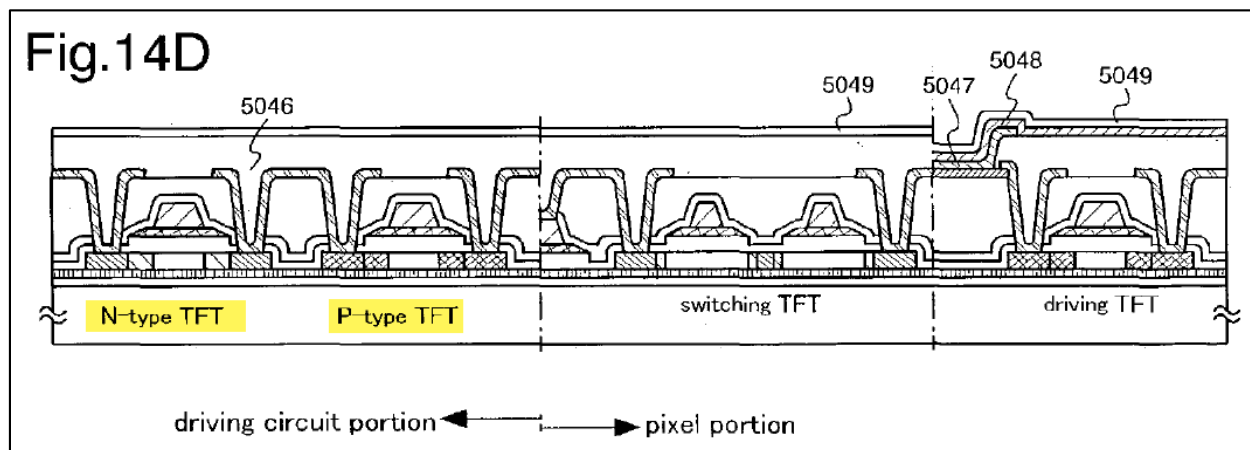
Additionally, the alleged manufacturing benefit of an all-PMOS circuit has no support in Kimura and, to the contrary, is inconsistent with Kimura’s disclosures. Petitioner’s theory of a purported manufacturing benefit is based wholly on citation to a passing statement in an unrelated reference (Exhibit 1004), and Petitioner fails to explain how it would be applicable to Kimura. Petitioner calls this unrelated reference “Kimura ’798,” but it does not mention that this “Kimura” of Exhibit 1004 is a different inventor (Matsumi Kimura) than the “Kimura” of Exhibit 1002 (Hajime Kimura). Nothing in the Kimura reference that underlies the Petition’s obviousness ground (Exhibit 1002) teaches or suggests that there would be benefits in modifying its circuits to use “all TFTs [] of the same type.” In fact, none of the pixel circuits in Kimura use an all-PMOS configuration (setting aside Figures 22–23, which depict the prior art).

Exhibit 1004 briefly mentions “advantageousness in manufacturing” for the circuits discussed in that reference—which is unrelated to Kimura. Petitioner fails to explain how any such advantages would allegedly apply to the different circuits of Kimura. On the contrary, Kimura includes extensive disclosures, including manufacturing instructions, that underscore that it is directed to active matrix devices formed using CMOS (“complementary metal oxide semiconductor”) technology—i.e., circuitry that by its definition requires *both* PMOS and NMOS transistors. *See, e.g.*, Ex. 1011 at 5 (observing that the CMOS process entails fabricating NMOS and PMOS transistors on the same semiconductor chip); Kimura at ¶¶ 547, 582 (referencing the “CMOS circuit composed of the N-channel TFT and the P-channel TFT.”). And Kimura expressly teaches that its process, which forms a CMOS driver together with a CMOS pixel circuit, confers manufacturing advantages—“the process is shortened and it can contribute to the reduction in manufacturing cost and the improvement of a yield.” *Id.* at ¶ 571.

Kimura’s opening paragraph states that it is directed to “*active matrix* light emitting device[s],” Kimura at ¶ 1 (emphasis added), and Kimura later explains that its “active matrix” devices necessarily include CMOS circuitry:

In this specification, a substrate in which [i] a driver circuit ***including a CMOS circuit*** and [ii] a pixel part having a switching TFT and a drive TFT are formed on the same substrate ***is called an active matrix*** substrate as a matter of convenience.

Kimura at ¶ 502 (emphasis added).⁷ Accordingly, Kimura teaches that its disclosed pixel circuits (the “pixel part”)—including the specific embodiments relied upon by Petitioner—are used alongside CMOS driver circuits (e.g., for driving the signal line voltages), as part of the same substrate. This can be seen in Figure 14D:



Kimura Fig. 14D (highlighting the inclusion of NMOS (“N-type”) and PMOS (“P-type”) TFTs in the driver circuit portion of the active matrix substrate)

Because the CMOS driver circuit and pixel circuits are formed together on the same active matrix substrate, the pixel circuits are (like the driver circuit) formed in a process that involves making both NMOS and PMOS transistors. Indeed, Kimura includes detailed process steps for manufacturing the active matrix

⁷ Petitioner itself emphasizes Kimura’s teaching that the baseline pixel circuit of Figure 33 is part of “an ‘*active matrix*’” substrate, and relies upon that context for its obviousness challenge. Pet. at 81 (emphasis in original) (citing Kimura at ¶¶ 1, 476, for challenged claim 17).

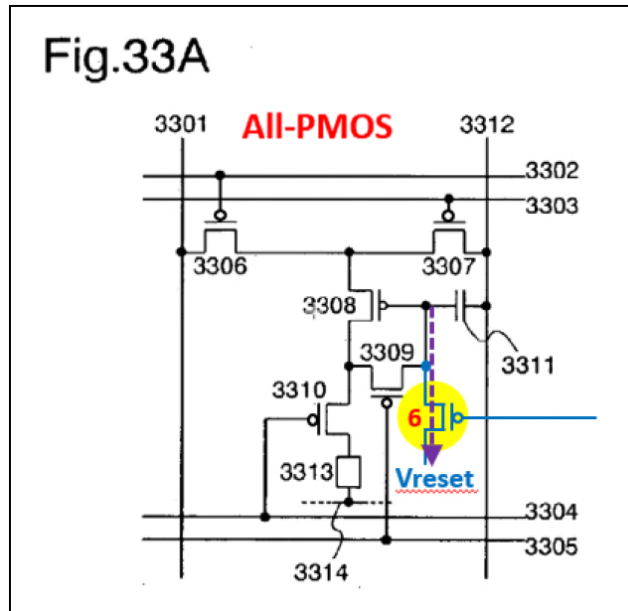
substrate, which results in the creation of both NMOS and PMOS TFTs. *See* Kimura at ¶¶ 502–571, Figs 13A–13D & 14A–14D. Kimura explains that, by following its disclosed processing steps, “as shown in Fig. 14D, the driver circuit portion including the *CMOS circuit composed of the N-channel TFT and the P-channel TFT* and the pixel part including the switching TFT and the drive TFT can be formed on the same substrate.” *Id.* at ¶ 547; *see also id.* at ¶ 582. Even more, Kimura teaches that following its disclosed CMOS processing steps entails a manufacturing advantage—“the process is shortened and it can contribute to the reduction in manufacturing cost and the improvement of a yield.” Kimura. at ¶ 571.

Thus, even assuming there is any “advantage[] in manufacturing when all TFTs are of the same type” in designs like those of the unrelated reference of Exhibit 1004 (Ex. 1004 at 12:30–49), Petitioner (by ignoring that Kimura’s embodiments are tethered to CMOS circuitry) fails to explain how such an advantage could even apply in Kimura’s Figure 33. Kimura’s active matrix substrates, by definition, include both NMOS and PMOS transistors in the driver portion, and thus even an all-PMOS redesign of Figure 33 (which is solely the pixel portion of the substrate) would not result in a substrate containing “all TFTs . . . of the same type” (Ex. 1004 at 12:30–49).

**B. Claims Requiring a Sixth “Initialization Transistor”
(Claims 2, 8, 16, 18)**

Claims 2, 8, 16, and 18 of the ’599 Patent require, as part of the pixel circuit, a specific initialization transistor, which discharges the data signal voltage stored in the capacitor in response to a scan signal ($\text{scan}[n-1]$) just before the current scan signal ($\text{scan}[n]$).⁸ Petitioner recognizes that the five-transistor circuit of Kimura in Figure 33 (and even any all-PMOS modification posited by Petitioner) does not disclose or suggest such a design. In an effort to cobble together an argument as to these claims, Petitioner advances a different type of proposed modification of Figure 33, which entails taking an NMOS “initialization transistor” that Petitioner purports to find in the unrelated embodiment of Figures 16–17 (and taking nothing else from that embodiment, which has a significantly different structure than Figure 33), replacing that NMOS transistor with a PMOS transistor, and then adding it to the all-PMOS version of Figure 33, which Petitioner illustrates as follows:

⁸ This is the “sixth” transistor recited in claims 8, 16 and 18, and the “fourth” transistor in claim 2.



Petitioner's all-PMOS Figure 33A, further modified to add a sixth "initialization transistor" (Pet. at 54)

Petitioner's arguments are fundamentally flawed, including in that (1) Petitioner relies on Kimura's identification of a problem in the Figure 33 circuit but ignores Kimura's explicit solution to that problem provided in the embodiment of Figure 36, and (2) Petitioner's arguments rest on the erroneous premise that Kimura's "erasure" means the same thing as "initialization" when Kimura discloses those as separate and distinct operations.

1. Petitioner fails to explain why a POSITA would seek an alternative solution to a problem that Kimura already solves.

Petitioner's theory for adding an "initialization transistor" to Kimura Figure 33 begins by noting that the approach of Figure 33 "is less desirable" because of

“undesired light emission.” Pet. at 51. Kimura acknowledges this shortcoming in Paragraph 665:

In the structures shown FIGS. 33 to 35, there are cases in which *electric current flows in the EL device to cause light emission*, before or after threshold voltage acquisition, that is *during a period that is not the normal light emitting period*.... [T]his therefore causes errors to develop between the actual brightness and the target brightness.

Kimura at ¶ 665. However, Kimura provides its solution to this problem in the very next paragraph—namely, the circuit of Figure 36:

A TFT 3612 is therefore added as shown in FIG. 36A. Electric current flowing in the TFT 3609 during input of the image signal flows through the TFT 3612 and to an electric power source line 3617. An electric current path to the EL device 3615 is cut off by a TFT 3611, and therefore the EL device 3615 does not emit light. *Light emission by the EL device during unnecessary periods can thus be prevented by using this type of structure.*

Kimura at ¶ 666 (emphasis added). Indeed, Petitioner acknowledges that “Kimura solves this problem . . . as shown in with Figure 36B.” Pet. at 19.

But Figure 36 is a different circuit than is described in claims 2, 8, 16, and 18 of the '599 Patent and does not satisfy the claim requirements. As an initial matter, Kimura does not even state or suggest that Figure 36 involves initialization, let alone that its TFT 3612 serves as a “dedicated initialization transistor,” as

discussed above in Section III.A. Moreover, the '599 Patent's claims at issue require that the initialization transistor be controlled by “a scan signal just before the current [or associated] scan signal”⁹—in other words, controlled by the previous scan line.¹⁰ TFT 3612 is not controlled by the previous scan line, as required by the '599 patent claims (and Petitioner does not contend otherwise). As shown above, TFT 3612 is controlled by line 3606, which Kimura does not teach or suggest as being the previous scan signal line for the circuit. Thus, even if TFT 3612 *could* be viewed as a “dedicated initialization transistor,” Figure 36 would not meet the claims.

Rather than accept the nonobviousness of the '599 Patent, Petitioner proposes that a POSITA seeking to overcome the “undesired light emission” of Figure 33 could (1) reject the solution actually taught by Kimura in Figure 36, yet then (2) scour all of the many varied embodiments within Kimura's 85-page disclosure looking for ideas for an alternative solution, (3) land upon the configuration of Figures 16–17 that Kimura does not connect in any way to the circuits of Figures 33 and 36, (4) observe TFT 1607, (5) take only that TFT from

⁹ '599 Patent at claims 2, 8, 16, 18.

¹⁰ *See, e.g.*, '599 Patent at Fig. 3 (including a “scan[n-1]” line that controls the initialization transistor T34).

the circuit of Figures 16–17 and not the other features, and (6) seek to use a PMOS version of this transistor.

This is dubious. Why would an artisan turn to Figures 16–17 to try find “[a]nother solution” to Figure 33, when Kimura already provides its solution in Figure 36? Petitioner does not say. It does not even attempt to argue that its alternative solution provides any benefit over Figure 36.

Petitioner is also wrong in asserting that Figures 16–17 represent “[a]nother solution taught by Kimura.” Pet. at 19, 51. Kimura never portrays Figures 16–17 as a solution to the light-emission problem of Figure 33. Kimura does not even discuss unwanted light emission in connection with Figures 16–17. And nowhere does Kimura teach or suggest that the embodiment of Figures 16–17 should be combined with Figure 33, or vice-versa. They are portrayed as entirely separate embodiments. Thus, Petitioner offers no reason why a POSITA would look to the circuit of Figures 16–17. *See In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000) (obviousness “cannot be predicated on the mere identification in [a prior art reference] of individual components of claimed limitations. Rather, particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed”).

2. Petitioner’s rationale for adding an “initialization transistor” to Kimura Figure 33 hinges on its misunderstanding of “erasure.”

The Petition’s theory for the “initialization transistor” claims also suffers from a fundamental technical flaw, stemming from its error in portraying “erasure” in Kimura as being synonymous with “initialization.” As explained in Section III.B, “erasure” and “initialization” in Kimura are separate operations. In Kimura, “erasure” means “forcibly plac[ing] [the EL device] in a non-light-emitting state.” Kimura at ¶ 410. And an “erasure TFT” is a transistor that permits “electric current supplied to the EL device [to] be cut off at an arbitrary timing.” Kimura at ¶ 658. Kimura does not use “erasure” to refer to “reset[ting] the capacitor voltage to a default initialization value” (i.e., initialization) as Petitioner mistakenly asserts. Pet. at 18.

Petitioner’s flawed reading of “erasure” in Kimura is the basis for its proposal to combine Figures 16–17 with Figure 33. First, it leads Petitioner to inaccurately assert that Figure 36 (for which Kimura discusses “erasure” but does not discuss any “initialization”) reflects the addition of an “initialization transistor” to Figure 33. Pet. at 19. This, in turn, is the rationale for Petitioner’s assertion that a POSITA might seek to use the “initialization transistor” of Figures 16–17 as an alternative. *See id.* at 19, 51. Finally, Petitioner’s flawed reading of “erasure” is also the sole premise for Petitioner’s faulty reasoning that Kimura’s discussion of

an *erasure transistor* in connection with Figure 33 would make the *initialization* approach of Figures 16–17 “readily applicable to the baseline circuit of Fig. 33.” *Id.* at 52–53.

Beginning with Figure 36, Petitioner asserts that this embodiment includes “a dedicated initialization transistor (labelled sixth transistor) . . . where, during initialization, the capacitor discharges through the sixth transistor instead of the light emitting element.” Pet. at 19 (emphasis added). Contrary to Petitioner’s assertion, Kimura does not identify any “initialization transistor” (or otherwise discuss initialization) with respect to the Figure 36 embodiment.

Petitioner points to TFT 3612 as the purported “initialization transistor” of Figure 36. *See* Pet. at 19.¹¹ Nothing in Kimura teaches or suggests that this transistor is used for initialization. On the contrary, Kimura describes TFT 3612 as preventing light emission, consistent with the purpose of this embodiment:

A TFT 3612 is therefore added as shown in FIG. 36A. ***Electric current*** flowing in the TFT 3609 during input of the image signal ***flows through the TFT 3612 and to an electric power source line***

¹¹ On page 19, the Petition includes an annotated version of Figure 36B in which the transistor on the lower left of the circuit is identified as the “dedicated initialization transistor (labelled sixth transistor).” This transistor is TFT 3612 as shown in Figure 36A.

3617. An electric current path to the EL device 3615 is cut off by a TFT 3611, and therefore the EL device 3615 does not emit light. ***Light emission*** by the EL device during unnecessary periods ***can thus be prevented by using this type of structure.***

Kimura at ¶ 666 (emphasis added).

Kimura thus describes TFT 3612 as preventing unwanted light emission “during input of the image signal” (i.e., the programming phase). Kimura does not characterize this transistor as relating to an “initialization” phase or operation.

Kimura also states that “[i]t is also possible to use the TFT 3611 [a different transistor in Figure 36] as an erasure TFT.” Kimura at ¶ 667 (cited in Pet. at 19). Thus, Kimura refers to the possibility of using TFT 3611 for its erasure operation. As discussed above in Section III.B, an “erasure TFT” in Kimura is a transistor that permits “electric current supplied to the EL device [to] be cut off at an arbitrary timing.” Kimura at ¶ 658. Kimura does not ever disclose or suggest using this TFT for initialization. Kimura’s reference to an “erasure TFT” is for a different operation than initialization.

Next, on the mistaken premise that Figure 36 involves adding an “initialization transistor” to Figure 33 (when there is actually no initialization transistor in the circuit of Figure 36), Petitioner proposes combining Figure 33 with a different “initialization transistor”—that of Figures 16–17. *See* Pet. at 51. But

when Kimura is read correctly, it becomes clear that the circuit of Figures 16–17 is not directed to the same problem as Figure 36.

As discussed in the preceding paragraphs, Kimura presents Figure 36 as a pixel configuration capable of preventing unwanted light emission during programming, but it does not discuss or suggest having a transistor for initialization in this circuit. For the embodiment of Figures 16–17, the converse is true. In describing the operation of Figures 16–17, Kimura *does* discuss initialization (see Kimura at ¶ 426), but it *does not* discuss preventing unwanted light emission during programming (see Kimura at ¶¶ 420–430).

Finally, Petitioner fails to show that the initialization approach of Figures 16–17 is “readily applicable” to the circuit of Figure 33 (or an all-PMOS modification thereof). Pet. at 52. Once again, the argument is premised on the erroneous assumption that “erasure TFT” means the same thing “initialization TFT,” as is illustrated in the following passage from the Petition:

Such an approach is readily applicable to the baseline circuit of Fig. 33. [EX1003, ¶¶221-230 and ¶¶155-158]; *see also id.*, ¶¶141-143. Indeed, when discussing Fig. 33, ***Kimura expressly teaches that “the erasure [transistor] can be placed in any location***, provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing.” EX1002, [0658]. ***Thus, a POSITA would have been motivated to place the initialization transistor***

discussed in Figs. 16-17 in the same location (i.e., directly connected to the capacitor) in Fig. 33.

Pet. at 52–53 (emphasis added). That is, Petitioner assumes that an “initialization transistor” (as in Figures 16–17) can be placed in any location suitable for an “erasure transistor” (as in Figure 33), when in fact they perform different functions.

Accordingly, all of Petitioner’s motivations for adding an “initialization transistor” to Figure 33 are based on its misunderstanding of “erasure” in Kimura. When the reference is properly interpreted, none of these motivations apply.¹²

C. Claims Requiring that the “Current Light-Emitting Signal” Control the Fourth and Fifth Transistors (Claims 13–18) or Fifth and Sixth Transistors (Claims 1–6)

Finally, Petitioner fails in its attempt create a circuit from Kimura that would satisfy the claims requiring that the “current light-emitting signal” be used to

¹² Petitioner also contends that a POSITA “would have been motivated to implement the initialization transistor as a PMOS device,” “[g]iven that all other transistors in the All-PMOS implementation are PMOS devices.” Pet. at 53. This is wrong for the reasons discussed in Sections VI.A.2 and VI.A.3 above.

control the gates of both the “fourth” and “fifth” transistors for claims 13–18, and the “fifth” and “sixth” transistors for claims 1–6.¹³ *See, e.g.*, Pet. at 63.

Although this key element is relegated to near the end of the Petition, it is central to the line-sharing benefits of the ’599 Patent’s innovative design. In fact, the requirement appears in four out of the five independent claims of the ’599 Patent (claims 1, 14, 15, and 17), as well as one additional dependent claim (claim 13), as shown in the following table:

Claims	“Current Light-Emitting Signal” Limitations
Claims 1 and 14	a fourth [fifth] transistor for delivering [providing] a power supply voltage ... in response to a current light-emitting signal; a fifth [sixth] transistor [...] for providing the driving current ... in response to the current light-emitting signal
Claims 13, 15, and 17	a [the] fourth transistor [...] including a gate to which a [the] current light-emitting signal is applied ...; a [the] fifth transistor [...] including a gate to which the current light-emitting signal is applied ¹⁴

¹³ For simplicity, this remainder of this section refers to these as the “fourth” and “fifth” transistors. But the discussion is equally applicable to the “fifth” and “sixth” transistors (respectively) of claim 1 and its dependent claims.

As Petitioner acknowledges, the above elements all require “that ‘the current light-emitting signal’ control the gates of both the fourth and fifth transistors.” Pet. at 63 (addressing claim 13); *see also id.* at 69–70 (addressing elements 14[f] and [g]).

Petitioner’s obviousness arguments for this requirement begin at page 63. Petitioner concedes that even were Kimura’s Figure 33 modified to replace all four of its NMOS transistors with PMOS transistors while keeping its PMOS transistor unchanged (which as discussed above, a POSITA would have had no reason to do), Petitioner’s modified circuit still would not meet this requirement, because it “shows the [alleged] fourth and fifth transistors controlled by *different* signals.” Pet. at 64 (emphasis added). Instead, Petitioner attempts to cobble together a different modified circuit. To do this, Petitioner proposes to turn back to Kimura’s Figure 36—the same embodiment it disregarded for the “initialization transistor” claims. And although Figure 36 *also* shows these transistors controlled by different gate signal lines, Petitioner seeks to take an “all-PMOS” version of Figure 36 (which already would require changing its five NMOS transistors to PMOS

¹⁴ In this context, a transistor “including a gate to which [this] signal is applied” means that the signal is used to control the transistor, since the gate voltage controls the transistor’s operation.

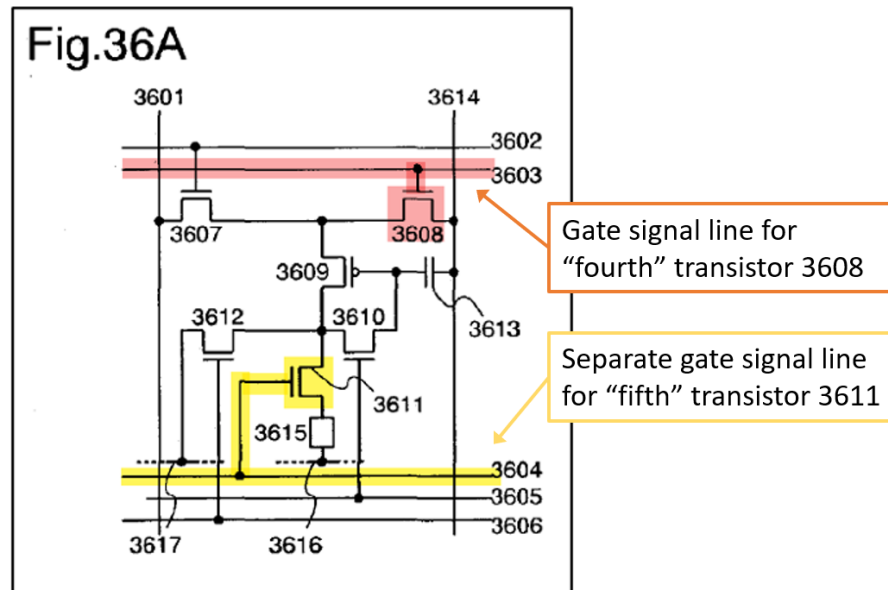
transistors while leaving the PMOS transistor unchanged) and modify it even further to come up with a new circuit in which the “fourth” and “fifth” transistors somehow share the same gate signal line.

This argument should be rejected for numerous reasons. First, the modification is inconsistent with Kimura’s teachings. Second, Petitioner’s attempt to apply Figure 36 for the “current light-emitting signal” requirement is flatly inconsistent with its arguments for the “initialization transistor” requirement, where it turns to Figures 16–17. Petitioner never attempts to square its two inconsistent theories for these requirements—based on two alternative embodiments—despite the fact that both of these requirements appear together in many of the same claims of the ’599 Patent (e.g., claims 2, 16, and 18 each require both that the “current light-emitting signal” be used to control the gates of the two specified transistors and that a different initialization transistor discharges the data signal voltage stored in the capacitor in response to a scan signal (scan[n-1]) just before the current scan signal (scan[n])).

1. Kimura does not teach or suggest using a shared gate signal for the “fourth” and “fifth” transistors.

As shown below, Kimura’s Figure 36 depicts two separate gate signal lines for the alleged “fourth” and “fifth” transistors of that circuit. Nonetheless, Petitioner asserts that, because these transistors “are always ON/OFF together,” a

POSITA “would have understood (or at least found it obvious) that Kimura uses a shared light-emitting signal to control them.” Pet. at 65. This does not follow.



Kimura Fig. 36A
(highlighted to show pertinent gate signal lines)

Petitioner overlooks that (i) Kimura specifically addresses which lines can be combined in its pixel circuits, (ii) Kimura identifies two sets of lines that can be combined in Figure 36, and (iii) Kimura does not teach or suggest combining the gate signal lines for the “fourth” and “fifth” transistors in this circuit.

Specifically, Kimura states the following about line sharing in the embodiment of Figure 36:

Further, *the electric power source line 3617 may also be shared with a gate signal line of another row*, similar to other embodiments. In addition, it is possible for a *gate signal line 3604 and a gate signal line 3606* to be shared with each other.

Kimura at ¶ 668 (emphasis added).

Thus, for the circuit of Figure 36, Kimura teaches that it is possible to share lines 3604 and 3606, as well as line 3617 with a signal line of a different row. Kimura does not teach or suggest combining gate signal lines 3603 and 3604 (i.e., the signal lines for the alleged fourth and fifth transistors), as required by the challenged claims—indicating that this pair of lines cannot be combined.

Kimura also discusses line sharing in the circuit of Figure 33, for which it likewise identifies two sets of lines that can be combined. *See* Kimura at ¶ 659; Figs. 34A and 34B. For example, as discussed above in Section VI.A.1, Kimura teaches that it is possible to share a line for TFTs 3306 and 3307 in that figure, and explains how this requires that a combination of NMOS and PMOS transistors be used for these transistors. This reinforces that Kimura considered where lines could be shared in its embodiments, and provided instructions for how to do so. The simple fact is that sharing gate signal lines in accordance with Kimura’s teachings leads to a different kind of circuit than is claimed in the ’599 Patent, one that would not satisfy the requirements of the challenged claims. If anything, this reinforces the nonobviousness of the claimed circuits of the ’599 Patent.

2. Petitioner’s attempt to apply Figure 36 for the “current light-emitting signal” requirement conflicts with its reliance on Figures 16–17 for the “initialization transistor” requirement.

Petitioner’s theory of obviousness for the “current light-emitting signal” requirement also conflicts with its theory of obviousness for the “initialization transistor” requirement, even though these requirements appear together in many of the same claims.

Petitioner presents the circuits of Figure 36 and Figures 16–17, as two alternative approaches for allegedly solving the undesired light emission of Figure 33. *See* Pet. at 19. For the “initialization transistor” requirement of claims 2, 8, 16, and 18, Petitioner proposes that a POSITA disregard Figure 36 (Kimura’s express solution for this problem), and instead attempt “another solution” based on Figures 16–17, as discussed in Subsection B above. Yet, when Petitioner gets to the “current light-emitting signal” requirement of claims 1–6 and 13–18, Petitioner inexplicably returns to Figure 36.

These claim requirements are not abstract elements to be addressed in isolation, as Petitioner seeks to do. Rather, they are part of an integrated whole circuit as described in the claims of the ’599 Patent. For example, the elements of

independent claim 15 (for which Petitioner relies on Figure 36)¹⁵ are part of dependent claim 16 (for which Petitioner relies on Figures 16–17).¹⁶ The same is true for independent claim 17 (relying on Figure 36)¹⁷ and dependent claim 18 (relying on Figures 16–17).¹⁸ And for independent claim 1 (relying on Figure 36 as well as Figure 16)¹⁹ and dependent claim 2 (relying on Figures 16–17).²⁰ Thus, when these claims are considered as a whole, it becomes clear that Petitioner is

¹⁵ See Pet. at 74–75 (analysis for element [15d], citing *id.* at 65–67 (analysis for claim 13, relying on Kimura’s Figure 36 embodiment)).

¹⁶ See Pet. at 78–80 (analysis for claim 16, relying on Kimura’s Figures 16–17).

¹⁷ See Pet. at 84–85 (analysis for element [17d], cross-referencing analysis for element [15d]), 74–75 (analysis for element [15d], citing *id.* at 65–67 (analysis for claim 13, relying on Kimura’s Figure 36 embodiment)).

¹⁸ See Pet. at 86 (analysis for claim 18, cross-referencing analysis for claim 16), 78–80 (analysis for claim 16, relying on Kimura’s Figures 16–17).

¹⁹ See Pet. at 90–92 (analysis for element 1[e], relying on Kimura’s Figure 36 embodiment).

²⁰ See Pet. at 93 (analysis for claim 2, cross-referencing analysis for claim 8), 49–56 (analysis for claim 8, relying on Kimura’s Figures 16–17).

relying on inconsistent theories to purportedly satisfy different elements of some of the same claims of the '599 Patent.

Moreover, these two approaches are notably different, based on Petitioner's own drawings of Figure 33 as modified based on Figures 16–17 (as used for the “initialization transistor” requirement, and shown below left) and Figure 36 (as used for the “current light-emitting signal” requirement, and shown below right):

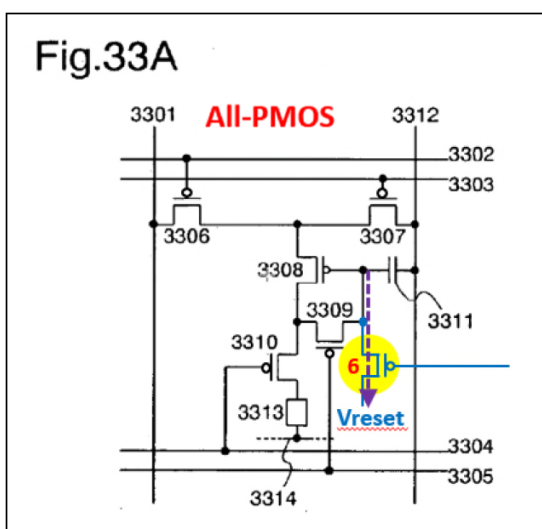
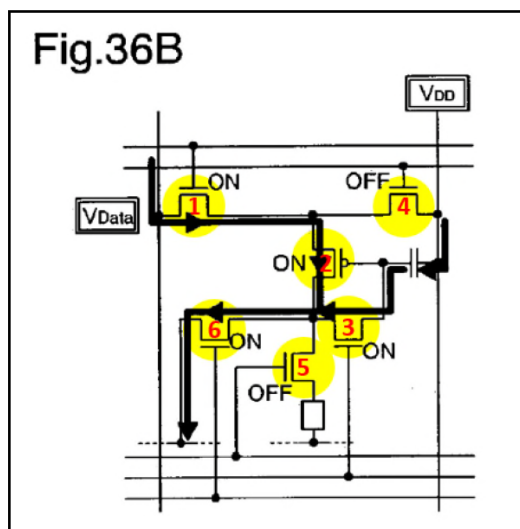


Figure 33 as modified based on
Figures 16–17 (Pet. at 54)



Petitioner's annotation of Fig. 36B
(Pet. at 19)

For example, the “sixth” transistors that Petitioner identifies in these respective circuits are configured at different places. The circuits also differ with respect to their gate and power lines. Yet Petitioner fails to articulate any approach for somehow combining the two circuits, let alone any reason for a POSITA to do so, and certainly not with any reasonable expectation of success.

Thus, Petitioner does not present a coherent theory of obviousness for these two overlapping claim sets (claims 2, 8, 16, and 18, for the “initialization transistor” requirement, and claims 1–6 and 13–18, for the “current light-emitting signal” requirement)—leading to an unresolved conflict when the claims are considered as a whole.

This is emblematic of Petitioner’s overall approach of picking and choosing from disparate embodiments of Kimura—splicing them together and making other unwarranted modifications along the way—to try to meet the various claim requirements of the ’599 Patent. The Federal Circuit has rejected such an approach, and the Board should reject it here. *See, e.g., In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988) (“One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.”).

VII. Conclusion

For all of the foregoing reasons, Patent Owner respectfully submits that institution should be denied.

Date: September 20, 2023

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that the present paper contains 11,828 words based on the word count indicated by the word-processing program used to generate the paper and excluding those portions exempted by 37 C.F.R. §§ 42.24(a) and (b).

Date: September 20, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6, I hereby certify that the foregoing Patent Owner's Preliminary Response and accompanying exhibits were served by electronic mail on the following counsel of record for petitioner:

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