

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO. LTD.,
WUHAN CHINA STAR OPTOELECTRONICS SEMICONDUCTOR
DISPLAY TECHNOLOGY CO., LTD., TIANMA MICROELECTRONICS
CO. LTD, and VISIONOX TECHNOLOGY, INC.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.,
Patent Owner.

IPR2023-00941
Patent 7,414,599 B2

Before JAMESON LEE, TERRENCE W. McMILLIN, and
JOHN A. HUDALLA, *Administrative Patent Judges*.

LEE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Mianyang Boe Optoelectronics Technology Co., Ltd., Wuhan China Star Optoelectronics Semiconductor Display Technology Co., Ltd., Tianma Microelectronics Co. Ltd., and Visionnox Technology, Inc. (collectively “Petitioner”) filed a Petition requesting an *inter partes* review of claims 1–18 (“challenged claims”) of U.S. Patent No. 7,414,599 B2 (Ex. 1001, “the ’599 patent”). Paper 1. Samsung Display Co., Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 9 (“Prelim. Resp.”). With our authorization, Petitioner filed a Preliminary Reply (Paper 10 (“Prelim. Reply”)) and Patent Owner filed a Preliminary Sur-reply (Paper 11 (“Prelim. Sur-reply”)) addressing Patent Owner’s arguments in the Preliminary Response regarding discretionary denial under 35 U.S.C. § 325(d).

We have authority to determine whether to institute review under 35 U.S.C. § 314 and 37 C.F.R. § 42.4. Upon consideration of the contentions and the evidence of record before us, we conclude Petitioner has shown a reasonable likelihood that it would prevail in establishing unpatentability of at least one challenged claim of the ’599 patent. Accordingly, we institute an *inter partes* review of all challenged claims of the ’599 patent on all grounds set forth in the Petition.

II. BACKGROUND

A. *Real Parties in Interest*

Petitioner identifies itself and its subsidiaries as real party in interest. Pet. 95. Patent Owner identifies only itself as the real party in interest. Paper 7, 2.

B. Related Matters

Patent Owner identifies the following litigations involving the '599 patent as related matters:

1. *Certain Active Matrix Organic Light-Emitting Diode Display Panels And Modules For Mobile Devices, and Components Thereof*, Inv. No. 337-TA-1351 (U.S.I.T.C.);
2. *Samsung Display Co., Ltd. v. BOE Technology Co., Ltd.*, Case No. 2-23-cv-00309 (E.D. Texas).

Paper 7, 2. Petitioner identifies the same matter before the International Trade Commission, Inv. No. 337-TA-1351, as a related matter. Pet. 95.

C. The '599 Patent

The '599 patent is directed to a pixel circuit in an organic light emitting device, which self-compensates the threshold voltage of a driving transistor. Ex. 1001, code (57). The '599 patent describes a problem with preexisting organic light emitting devices, i.e., nonuniformity from pixel to pixel caused by a variation of the threshold voltage of the driving transistor in each pixel circuit leading to a difference in the current flowing through the electroluminescent element in each pixel circuit. *Id.* at 1:38–50.

The pixel circuit of the '599 patent includes an electroluminescent element for emitting light in response to an applied driving current, and first, second, third, fourth, and fifth transistors, and a capacitor. *Id.* at code (57). The first transistor delivers data signal voltage in response to a current scan line signal. *Id.* The second transistor generates a driving current to drive the electroluminescent element in response to the data signal voltage. *Id.* The third transistor connects the second transistor in the form of a diode in response to a current scan signal to self-compensate the threshold voltage of

the second transistor. *Id.* The fourth transistor delivers a power supply voltage to the second transistor in response to a current light-emitting signal. *Id.* The fifth transistor provides the driving current, provided from the second transistor, for the electroluminescent element in response to the current light-emitting signal. *Id.* The capacitor stores the data signal voltage delivered to the second transistor. *Id.*

Figure 3 of the '599 patent, annotated by Petitioner (Pet. 7) to highlight the transistors and the light-emitting element, as well as to number the transistors as 1 through 5, is reproduced below:

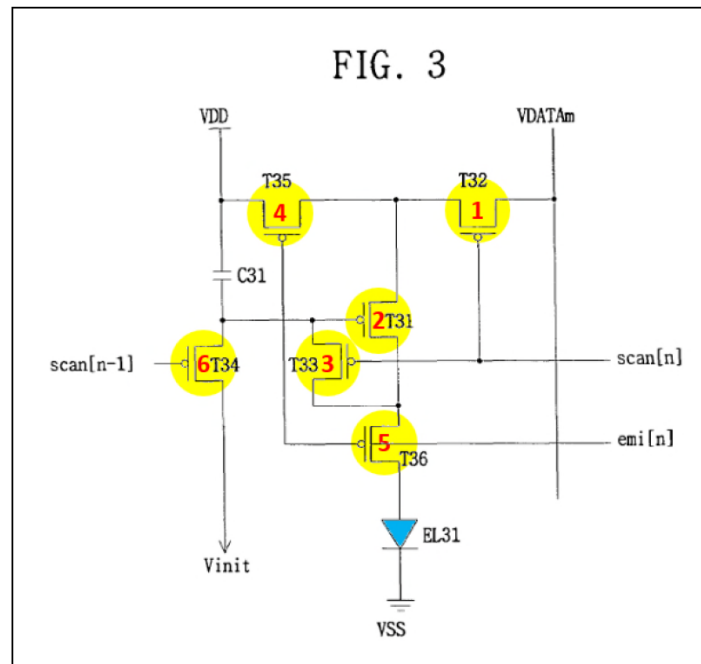


Figure 3 illustrates a pixel circuit according to one embodiment of the '599 patent. Ex. 1001, 5:65–67. Petitioner highlights the transistors in yellow and the light-emitting element in blue, and numbers the transistors as 1 through 5 in red. Pet. 7.

The '599 patent describes three different operations for the pixel circuit of Figure 3: an initialization operation, a data program operation, and

a light-emitting operation. Ex. 1001, 7:15–64. The initialization operation initializes the data signal stored in capacitor C31 which provides the gate voltage of driving transistor 31. *Id.* at 7:24–26. The '599 patent explains:

First, in an initialization operation, during an initialization period in which previous scan signal SCAN[n-1] is of a low level, and current scan signal SCAN[n] and light-emitting signal EMI[n] are of high level as shown in FIG. 4, since transistor T34 is turned on by the low level of previous scan signal SCAN[n-1], and transistors T31-T33 and T35-T36 are turned off by the high level of current scan signal SCAN[n] and current light-emitting signal EMI[n], an initialization path (as indicated by a solid line shown in FIG. 5) is formed. Accordingly, the data signal that has been stored in capacitor C31, namely, a gate voltage of driving transistor T31, is initialized.

Id. at 7:15–26 (bracketed material in original). Figure 5 of the '599 patent is reproduced below:

FIG. 5

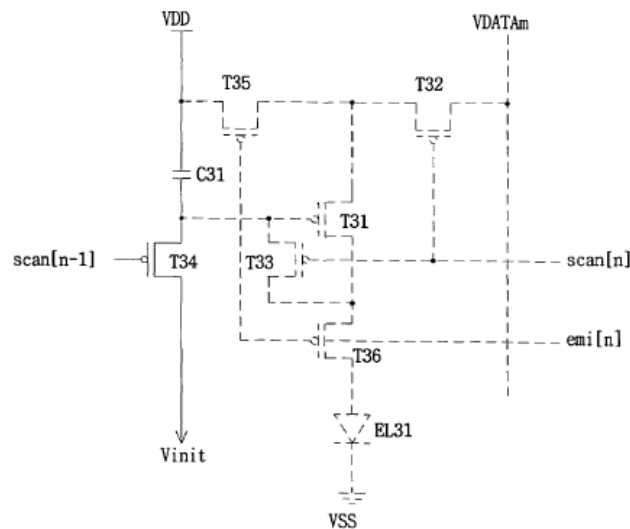


Figure 5 is a diagram for explaining the initialization operation of an embodiment of the pixel circuit of the '599 patent. *Id.* at 6:4–7.

The data programming operation applies a data voltage VDATAm to the gate of driving transistor T31 through threshold voltage compensation transistor T33. *Id.* at 6:41–44. The '599 patent explains:

Next, in a data program operation, during a programming period in which previous scan signal scan [n-1] is at a high level, current scan signal SCAN[n] is at a low level and current light-emitting signal EMI[n] is at a high level as shown in FIG. 4, transistor T34 is turned off, and transistor T33 is turned on by the low level of current scan signal SCAN[n], such that driving transistor T31 is connected in the form of a diode.

Since switching transistor T32 is also turned on by current scan signal SCAN[n], and switching transistors T35 and T36 are turned off by current light-emitting signal EMI[n], such that a data program path (as indicated by a solid line shown in FIG. 6) is formed. Accordingly, data voltage VDATAm applied to the associated data line is provided for the gate of driving transistor T31 through threshold voltage compensation transistor T33.

Since driving transistor T31 is in the diode connection, $\text{VDATAm} - V_{\text{TH}(\text{T31})}$ is applied to the gate of transistor T31 and the gate voltage is stored in capacitor C31, such that the program operation is completed.

Id. at 7:28–48 (bracketed material in original). Figure 6 of the '599 patent is reproduced below:

FIG. 6

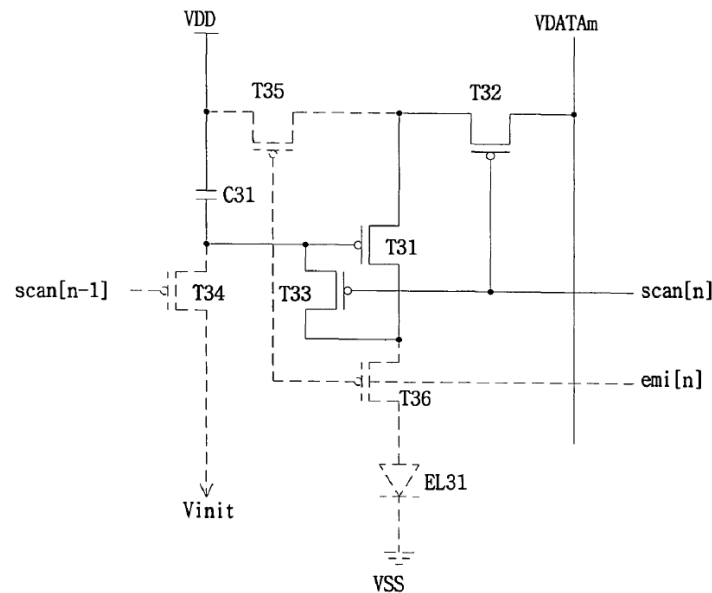


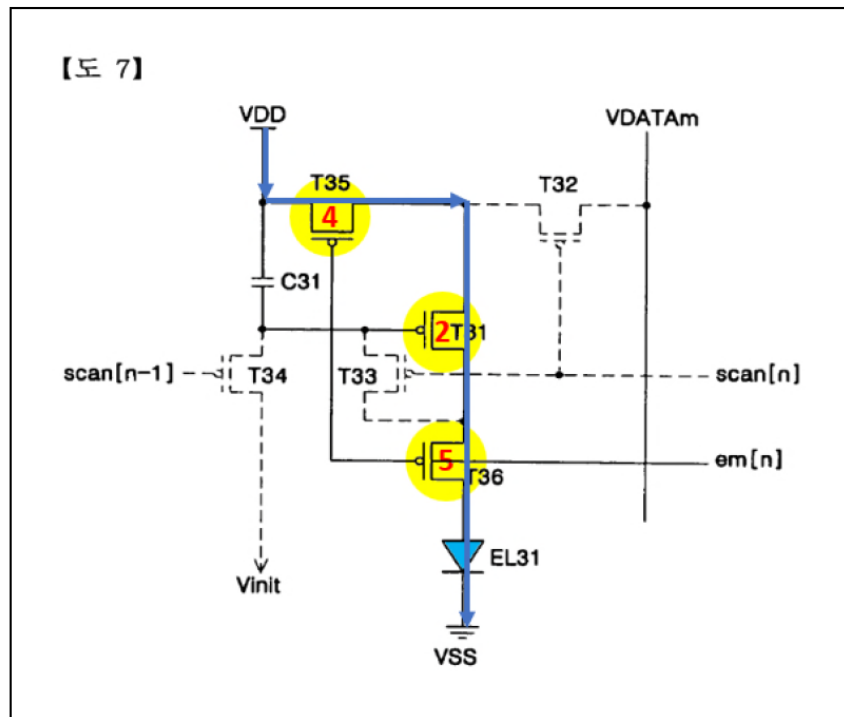
Figure 6 is a diagram for explaining the data program operation of an embodiment of the pixel circuit of the '599 patent. *Id.* at 6:4–7.

The light-emitting operation causes emission of light from light-emitting element EL31 by a driving current generated through transistor T31 in response to the data signal voltage applied to the gate of driving transistor T31. *Id.* at 7:60–64. The '599 patent explains:

Finally, in a light-emitting operation, during an light-emitting period in which previous scan signal SCAN[n-1] is of high level, current signal SCAN[n] becomes a high level, and then current light-emitting signal EMI[n] becomes a low level as shown in FIG. 4, an light-emitting path (as indicated by the solid line as shown in FIG. 7) is formed. That is, switching transistors T35 and T36 are turned on by the low level of current light-emitting signal EMI[n], initialization transistor T34 is turned off by the high level of previous scan signal SCAN[n-1], and threshold voltage compensation transistor T33 and switching transistor T32 are turned off by the high level of current scan signal SCAN[n]. Accordingly, a driving current generated in response to the data signal voltage applied to the gate of driving transistor T31 is provided through transistor T31 for organic EL

element EL31, such that the light-emitting of organic EL element EL31 occurs.

Id. at 7:49–65 (bracketed material in original). Although this description references a solid line indicating a light-emitting path in Figure 7, the drawing figure labeled “Figure 7” in the ’599 patent does not have such a solid line. In fact, Figure 7 appears to mistakenly duplicate Figure 6 of the ’599 patent. In the Petition, Petitioner refers instead to Figure 7 of the Korean patent application to which the ’599 patent claims priority in order to illustrate the textual description in the ’599 patent for Figure 7. Pet. 6 n.1; *see also* Ex. 1001, code (30) (foreign priority data); Ex. 1003 ¶ 101 (Dr. Foty reproducing the Korean application version of Figure 7). Patent Owner does not dispute that there is inaccuracy in that regard. We accept Figure 7 of the Korean priority application of the ’599 patent as Petitioner’s illustration of the textual description in the ’599 patent for Figure 7. We find that it is consistent with and also a reasonable depiction of the textual description in the ’599 patent for Figure 7. Figure 7 of the Korean priority application (as annotated by Petitioner) of the ’599 patent is reproduced below:



This figure is used by Petitioner to illustrate the textual description in the '599 patent for the light-emitting operation of the pixel circuit. Pet. 10–11.

Claims 1, 7, 14, 15, and 17 are independent. Claim 7 and 14 are representative and reproduced below:¹

[Claim 7 Preamble] A pixel circuit in an organic light emitting device, comprising:

- [7a] a first transistor for delivering a data signal voltage in response to a current scan line signal;
- [7b] a second transistor for programming the data signal voltage and for generating a driving current in response to a programmed data signal when light is emitted;

¹ The bracketed labels correspond to those used by Petitioner to reference the claim elements. See Pet. 23–49, 67–70. We use the same labels here for ease of reference, understanding, and consistency.

- [7c] a third transistor for providing the data signal voltage for the second transistor in response to the current scan signal;
- [7d] a capacitor for maintaining the data signal voltage programmed onto the second transistor;
- [7e] a fourth transistor for delivering a power supply voltage to the second transistor when the light is emitted;
- [7f] a fifth transistor for delivering the driving current, provided from the second transistor, in response to the data signal voltage when the light is emitted; and
- [7g] an electroluminescent element for emitting light corresponding to the driving current delivered through the fifth transistor,
- [7h] wherein the third transistor connects the second transistor in the form of a diode in response to the current scan signal so that the second transistor detects and compensates its threshold voltage deviation in itself.

Ex. 1001, 9:35–58.

[Claim 14 Preamble] A pixel circuit in an organic light emitting device, comprising:

- [14a] an electroluminescent element for emitting light in response to an applied driving current;
- [14b] a first transistor for delivering a data signal voltage in response to a current scan line signal;
- [14c] a second transistor for generating a driving current to drive the electroluminescent element in response to the data signal voltage;
- [14d] a third transistor for connecting the second transistor in the form of a diode in response to the current scan signal to self-compensate a threshold voltage of the second transistor;
- [14e] a capacitor for storing the data signal voltage delivered to the second transistor;

[14f] a fourth transistor for delivering a power supply voltage to the second transistor in response to a current light-emitting signal; and

[14g] a fifth transistor for providing the driving current, provided from the second transistor, for the electroluminescent element in response to the current light-emitting signal.

Id. at 10:29–49.

D. Evidence relied on by Petitioner

Petitioner relies on the following reference:²

Name	Patent Document	Exhibit
Kimura ³	US 2003/0132931 A1	1002

Petitioner also relies on the Declaration of Daniel Foty, Ph.D.

Ex. 1002. Patent Owner’s Preliminary Response and Preliminary Sur-Reply do not rely on the testimony of any expert witness.

E. Asserted Ground of Unpatentability

Petitioner asserts that the challenged claims of the ’599 patent are unpatentable based on the following ground (Pet. 15, 50):

Claims Challenged	35 U.S.C. § ⁴	Reference(s)/Basis
1–18	103	Kimura

² The ’599 patent issued from Application No. 10/886,014, filed July 6, 2004, and claims priority to KR 10-2003-0045610, filed July 7, 2003. Ex. 1001, codes (21), (22), (30).

³ Published July 17, 2003, based on Application No. 10/283,330, filed Oct. 30, 2002. Ex. 1002, codes (21), (22), (43). Kimura claims priority to JP 2002-298062, filed Oct. 10, 2002, and JP 2001-333575, filed Oct. 30, 2001. *Id.* at code (30).

⁴ The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Based on the record before us, we preliminarily determine that the ’599 patent has an effective

III. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner asserts the following with respect to the level of ordinary skill in the art:

A person of ordinary skill in the art (“POSITA”) in the technology field of the ‘599 patent would have had a Bachelor’s degree in electrical engineering or similar discipline, along with 2-3 years of circuit design/analysis experience. *See* EX1003, ¶31. Lack of work experience can be remedied by additional education, and vice versa. *Id.*

Pet. 13.

Patent Owner proposed a different statement of the level of ordinary skill in the art in related litigation involving the ‘599 patent before the U.S. International Trade Commission (“ITC”), which was agreed to by the Administrative Law Judge at the ITC. Prelim. Resp. 20. Patent Owner, however, also states: “For purposes of this Preliminary Response . . . Patent Owner does not believe” it necessary to dispute the level of ordinary skill in the art. *Id.* Thus, Patent Owner at this stage does not dispute Petitioner’s articulation of the level of ordinary skill in the art.

At this preliminary stage and on this record, we adopt Petitioner’s statement of the level of ordinary skill in the art. It is supported by the testimony of Dr. Foty and not disputed by Patent Owner. Further, it appears consistent with what is reflected by the content of the applied prior art references. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

filing date prior to the effective date of the applicable AIA amendments (March 16, 2013). We, therefore, refer to the pre-AIA version of 35 U.S.C. § 103.

B. Claim Construction

We use the same claim construction standard that would be used to construe a claim in a civil action under 35 U.S.C. § 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.100(b) (2022). The claim construction standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc) is applicable.

Claim terms are generally given their ordinary and customary meaning as would be understood by one with ordinary skill in the art in the context of the specification, the prosecution history, other claims, and extrinsic evidence including expert and inventor testimony, dictionaries, and learned treatises, although extrinsic evidence is less significant than the intrinsic record. *Phillips*, 415 F.3d at 1312–17. Usually, the specification is dispositive, and it is the single best guide to the meaning of a disputed term. *Id.* at 1315.

The specification may reveal a special definition given to a claim term by the patentee, or the specification or prosecution history may reveal an intentional disclaimer or disavowal of claim scope by the inventor. *Id.* at 1316. If an inventor acts as his or her own lexicographer, the definition must be set forth in the specification with reasonable clarity, deliberateness, and precision. *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1249 (Fed. Cir. 1998). The disavowal, if any, can be effectuated by language in the specification or the prosecution history. *Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016).

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

Petitioner asserts that “no term requires construction for this proceeding.” Pet. 14. Patent Owner asserts that it “does not believe that any specialized constructions are necessary.” Prelim. Resp. 20. We agree that on the current record it is not necessary to conduct express claim construction for any term.

C. Alleged Obviousness of Claims 1–18 over Kimura

1. Overview of Kimura

Kimura relates to an active matrix light emitting device including a semiconductor device having a thin film transistor (“TFT”). Ex. 1002 ¶ 1. Kimura describes numerous embodiments of a pixel including a light-emitting device, some with the pixel including “first to third transistors” (*id.* ¶¶ 123, 139), some with the pixel including “first to fourth transistors” (*id.* ¶¶ 40, 54, 68, 82, 95, 110), and some with the pixel including “first to fifth transistors” (*id.* ¶¶ 156, 174, 192, 209, 228, 246).

The Abstract of Kimura describes as follows:

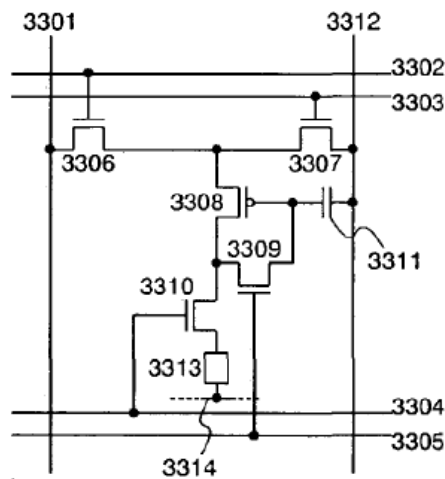
Brightness irregularities that develop in a light emitting device due to [dispersion] among pixels in the threshold values of TFTs used for supplying electric current to light emitting devices become obstacles to improved image quality of the light emitting device. As an image signal input to a pixel from a source signal line, a desired electric potential is applied to a gate electrode of a TFT for supplying electric current to an EL device, through a

TFT having its gate and drain connected to each other. A voltage equal to the TFT threshold values is produced between the source and the drain of the TFT 105. An electric potential in which the image signal is offset by the amount of the threshold value is therefore applied to the gate electrode of the TFT. Further, TFTs are disposed in close proximity to each other within the pixel, so that dispersions in the TFT characteristics do not easily develop. A desired drain current can thus be supplied to the EL device even if there is dispersion in the threshold values of the TFTs among pixels, because this is offset by the threshold value of the TFT.

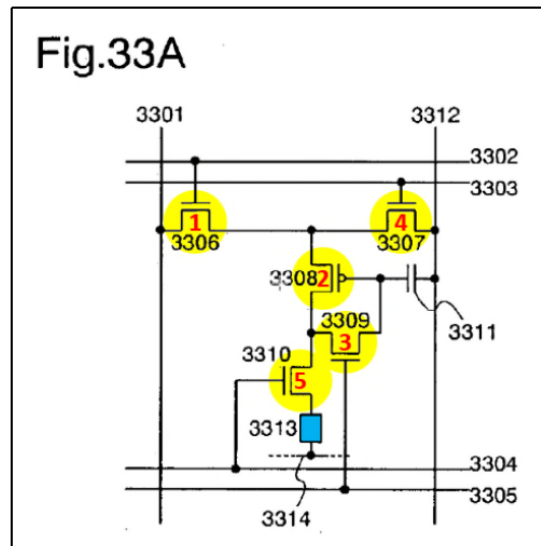
Ex. 1002, code (57).

We focus on the embodiment described in Kimura's Figures 33A through 33E, referred to as Embodiment 9 in Kimura (Ex. 1002 ¶ 652), because Petitioner primarily relies on this embodiment. Figure 33A of Kimura is reproduced below:

Fig.33A



Figures 33A is one of several figures, 33A–33E, used to illustrate one embodiment of Kimura's device. Ex. 1002 ¶ 339. Petitioner has annotated Figure 33A as shown below (Pet. 22):



In this version of Kimura's Figure 33A, Petitioner has highlighted in yellow and numbered Transistors 1–5 and has highlighted in blue EL device 3313. Hereinafter, we use the same numbering when referring to transistors in Figures 33B, 33C, 33D, and 33E.

Figures 33B–33E of Kimura are reproduced below:

Fig.33B

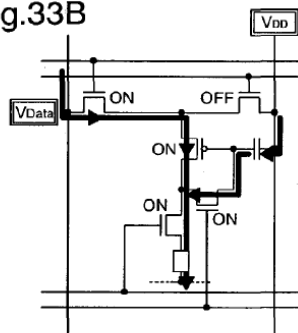


Fig.33C

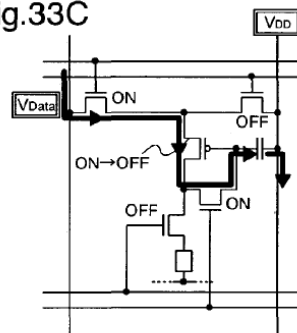


Fig.33D

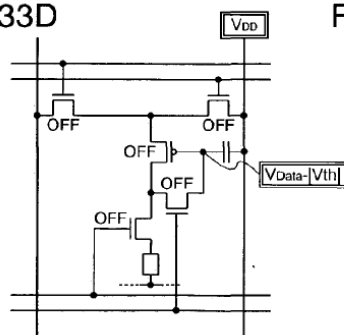
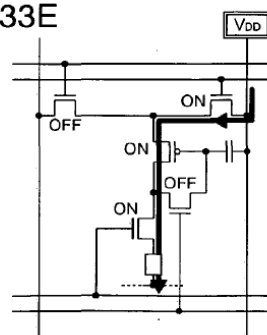


Fig.33E



Figures 33B–33E are the remainder of the figures used to illustrate the same embodiment of Kimura’s device. Ex. 1002 ¶ 339.

As shown above in Figure 33A, TFT 3309 (Transistor 3) is connected between the gate electrode and the drain electrode of TFT 3308 (Transistor 2), and Transistor 2 exhibits the behavior of a diode connected TFT when Transistor 3 is on. *Id.* ¶ 654. Kimura explains:

Operation is explained. First, the TFT **3306** turns on, and an image signal VData is input as shown in **FIG. 33B**. In addition, The TFT **3309** and a TFT **3310** turn on, and the *TFT 3308 thus behaves as a diode connected TFT*. When the TFT **3310** then turns off electric charge moves as shown in **FIG. 33C**. The voltage between the source and the drain of the TFT **3308**, in other words the voltage between the gate and the source of the TFT **3308**, eventually becomes equal to the threshold voltage, at which point the TFT **3308** turns off as shown in **FIG. 33D**.

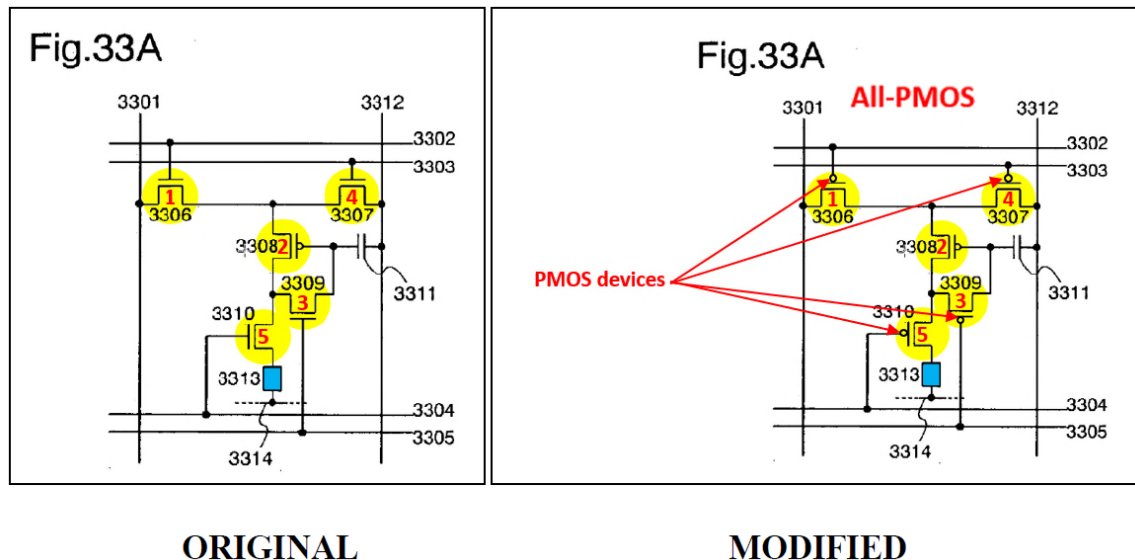
The TFTs **3307** and **3310** then turn on. The electric potential of a source region of the TFT **3308** increase from VData to VDD as the TFT **3307** turns on. The voltage between the gate and the source of the TFT **3308** therefore exceeds the threshold voltage to cause it to turn on, so that electric current flows in the EL device **3313** to cause it to emit light, as shown in **FIG. 33E**.

Thus, an electric potential difference equal to the threshold value can be produced between the gate and the source of the driver TFT **3308** in advance in accordance with the above processes, so that even if there is dispersion in the threshold voltages of the TFTs **3308** between adjacent pixels, there is no dispersion in the voltages between the gate and the source of the driver TFTs **3308** of adjacent pixels. In addition, *correction of dispersions in the threshold values is performed in the foregoing embodiments by a method in which the threshold voltage of a diode connected TFT is added to the image signal*, and then input to the gate electrode of another driver TFT.

Id. ¶ 655–657 (emphasis added).

2. *Petitioner's "All-PMOS" Modification of Kimura*

Petitioner states: "Before the element-by-element patentability analysis, it is helpful to discuss a modification to Kimura Fig. 33 [Figs. 33A–33E]." Pet. 19. That is a modification which replaces all nMOS transistors with pMOS transistors such that the only transistors used in the embodiment shown Figures 33A–33E are pMOS transistors. Pet. 19–23. The modification is shown on page 22 of the Petition via a side-by-side illustration of the before and after views of the modification to Figure 33A, with colored annotations added by Petitioner, as reproduced below:



In the version of Figure 33A on the left, labeled "ORIGINAL," Petitioner numbered Transistors 1–5 and colored them yellow as well as colored the EL element blue. In the modified version of Figure 33A on the right, labeled "MODIFIED," Petitioner changed the symbols for Transistors 1, 3, 4, and 5 from nMOS to pMOS, and pointed to them as "PMOS devices" with red arrows.

Petitioner uses the modified Figures 33A–33E (nMOS transistors 1, 3, 4, and 5 all changed to pMOS transistors so that all transistors are pMOS) as

illustration in support of its assertions of unpatentability for all claims including each independent claim. *See, e.g.*, Pet. 24–49, 72–73, 76–78, 81, 86–93. Patent Owner asserts that “Petitioner uses Figure 33 as the ‘baseline circuit for Petitioner’s patentability analysis,” and that “Petitioner relies on these ‘all-PMOS’ redesigns for all challenged claims.” Prelim. Resp. 25–26. To the extent Patent Owner is arguing that, according to Petitioner’s presentation, the all-pMOS modification is required in all of Petitioner’s theories of obviousness for all challenged claims, we disagree.

None of the independent claims includes any limitation with regard to whether one or more recited transistors must be nMOS or pMOS. Some dependent claims have limitations specifying the type of transistor for one or more of the recited transistors, such as claims 3–5, 9–11, and 13. When presenting its explanation of unpatentability of independent claim 7, Petitioner refers to the all-pMOS version of Figures 33A–33E for illustration purposes only, and never represented that the all-pMOS modification is necessary to meet the requirements of claim 7. Pet. 23–49.

For instance, limitation [7a] recites “a first transistor for delivering a data signal voltage in response to a current scan line signal.” The Petition states: “Kimura discloses claim element 7[a].” *Id.* at 24. In that context, the subsequent assertion that “[t]he ‘**first transistor**’ in Kimura is labelled 3306 in Fig. 33 (below left)” simply uses the all-pMOS version of Figure 33A for illustration purposes only and does not convey the all-pMOS modification is necessary to meet limitation [7a]. *Id.* Thus, it is Petitioner’s contention that transistor 3306 in unmodified Figure 33A meets limitation [7a].

Similarly, when discussing limitation [7b] which recites a second transistor, limitation [7c] which recites a third transistor, limitation [7e]

which recites a fourth transistor, and limitation [7f] which recites a fifth transistor, the Petition states that Kimura discloses each of limitations [7b], [7c], [7e] and [7f], even though it makes reference to the modified all-pMOS version of Figure 33A.

Likewise, when presenting its explanation of unpatentability of independent claims 1, 14, 15, and 17, Petitioner refers to the all-pMOS version of Figures 33A–33E for illustration purposes only, and never represented that the all-pMOS modification is necessary or required to meet the requirements of those other independent claims.

In essence, the all-pMOS modification of Kimura’s embodiment shown in Figures 33A–33E is inconsequential for independent claims 1, 7, 14, 15, and 17. For these claims, it makes no difference whether any nMOS transistor in Kimura’s Figure 33A is changed to a pMOS transistor.

Nevertheless, the proposed modification is important for dependent claims 3–5, 9–11, and 13, which do require certain transistors to be of the pMOS type. Patent Owner asserts that Petitioner has not provided sufficient motivation for one of ordinary skill in the art to make the modification to having all pMOS transistors for Kimura’s embodiment shown in Figures 33A–33E. Prelim. Resp. 26–38. We address this question here.

Petitioner acknowledges that all transistors in Kimura’s “Figure 33” are nMOS transistors except for the driving transistor, i.e., transistor 3308 identified as Transistor 2, which is pMOS.⁵ Pet. 39. Petitioner notes:

Kimura repeatedly and expressly teaches the interchangeability of NMOS and PMOS transistors used as switches, which is the

⁵ We understand that when Petitioner refers to Figure 33 of Kimura, Petitioner is referring to Kimura’s Figures 33A–33E, because there is no “Figure 33” in Kimura. We adopt the same usage to maintain consistency.

case for all but the second transistor. *See, e.g.*, EX1002, [0438] (“Note that a structure is used [in Figs. 3B-3D] in which the TFTs 304 and 306 are n-channel TFTs. . . . **However, the TFTs 304 and 306 function as simple switching devices, and therefore any polarity may be used.**”); *id.*, [0396] (same for Figs. 1-2); *id.*, [0445] (same for Figs. 4B-4D); *id.*, [0649] (“All other TFTs are only used as switching devices for performing only on and off control, and therefore may be of any polarity.”); *id.*, [0362] (showing an all-PMOS driver circuit in Fig. 22); EX1003, ¶¶146-154.

Id. at 19–20 (alteration in original). Petitioner also asserts that the “interchangeability of NMOS and PMOS *switching transistors* was well-known by 2003.” *Id.* at 4 (citing Ex. 1004, 12:30–49) (emphasis added). Petitioner’s expert, Dr. Foty, explains:

If the design need is for a transistor to be used as a simple on/off switch, then either an nMOS transistor or a pMOS transistor can be chosen – since, as shown in the figure from Kang and Leblebici 2003 above, each can function as a simple on-off switch. As the primary operational difference between nMOS and pMOS (when a simple switch is desired) is that the on/off characteristics are the opposite of each other – and the on-off signals to be applied must be altered (i.e., reversed as it were) to account for this. In particular, as described in Section VII.A.1, nMOS devices turn on in response to a “high” voltage on the gate terminal and turn off when a “low” voltage is applied. This is known in the art as “active-high” signaling. pMOS transistors are just the opposite – they turn on when a “low” voltage is applied to the gate terminal and turn off in response to a “high” voltage on the gate. This is known in the art as “active-low” signaling. Changing the polarity of a switching transistor (from nMOS to pMOS or vice versa) would require changing the polarity of the gate signal to achieve the same functionality, but doing so was easy and well-known to a POSITA. In contrast, swapping an nMOS transistor that performs an analog-like function for a pMOS transistor (or vice versa) may be more difficult, no such change is proposed in this IPR.

Id. ¶ 57 (emphasis added) (cited at Pet. 4). Dr. Foty further explains that “if only one [transistor] species (nMOS or pMOS) is used exclusively in a circuit, then the [manufacturing] process complexity and the cost [of manufacturing] will be lower.” *Id.* ¶ 58 (cited at Pet. 4). Dr. Foty testifies that if the change is made in Kimura to use only pMOS transistors, that “would result in a single-transistor-species circuit which would be simpler and less costly to manufacture.” *Id.* ¶ 151 (cited at Pet. 20).

Petitioner additionally cites US Patent No. 6,362,798 (Ex. 1004, “Kimura ’798”) as supporting Petitioner’s assertion that “interchangeability of NMOS and PMOS switching transistors was well-known by 2003.”

Pet. 4 (citing Ex. 1004, 12:30–49). The cited portion of Kimura ’798 states:

Moreover, the example shown in FIG. 1 is constructed with the mixture of a P channel type TFT and an N channel type TFT, however, every TFT can be N channel type TFTs or all TFTs can be P channel type TFTs. However, in consideration that the voltage/current characteristics and threshold characteristics of the driving TFTs 110 are compensated by the compensating TFT 120, it is advantageous to construct these driving TFTs 110 and compensating TFTs 120 by the same process as the same type TFTs. Particularly, if both TFTs are formed in the same film forming process, the degree of characteristics similarities between both TFTs generally increases, so that it becomes possible to provide the transistor circuit 100 on the same substrate with little or no variance in voltage/current characteristics and threshold characteristics. On the other hand, the resetting TFT 130 and *the switching TFT 140 can be either a P channel type TFT or an N channel type TFT without being dependent on whether the driving TFT 110 is a P channel type TFT or N channel type TFT.* However, it is often advantageous in manufacturing when all TFTs are of the same type.

Ex. 1004, 12:30–49 (emphasis added).

Petitioner asserts that one of ordinary skill in the art “would have had far more than a reasonable likelihood of success as making such changes [to use all pMOS transistors] was common place and well within a POSITA’s skill.” Pet. 21–22 (citing Ex. 1003 ¶ 154).

We have considered Petitioner’s rationale for modifying the embodiment in Kimura’s Figures 33A–33E. It is based on two theories: (1) a first theory based on general interchangeability of nMOS and pMOS transistors which are used as *switching transistors*, and (2) a second theory that single-transistor-species circuit is simpler and less costly to manufacture. We discuss them in sequence.

a) First Theory

For reasons discussed below, the first theory is sufficiently persuasive. In particular, we are persuaded preliminarily that an ordinarily skilled artisan would have known to implement a version of the pixel circuit shown in Figures 33A–33E of Kimura with all pMOS transistors. Notwithstanding Patent Owner’s arguments to the contrary, discussed below, we are sufficiently persuaded that there is general interchangeability of nMOS and pMOS transistors used as switching transistors. Thus, we are sufficiently persuaded, for institution purposes, that it would have been obvious to one of ordinary skill in the art to make a modification of Kimura’s embodiment shown in Figures 33A–33E to use pMOS type transistors for all switching transistors in the pixel circuit, which leads to an all pMOS version of Kimura’s Figure 33 embodiment.⁶

⁶ Petitioner points to other disclosures in Kimura allegedly teaching the use of a pMOS transistor for various ones, not all, of the nMOS transistors in Kimura’s Figures 33A–33E. Pet. 20–21. We do not find that such teachings add anything of significance to Petitioner’s general interchangeability theory

(1) *Patent Owner's Assertion of Misapplied Teachings*

First, Patent Owner argues that the various teachings Petitioner relies on from Kimura about nMOS and pMOS transistors being interchangeable are gleaned from Kimura's discussion of embodiments other than that disclosed in Figures 33A–33E. Prelim Resp. 26. This argument is unavailing, because the interchangeability teaching is described generically for all “switching transistors” and transcends any particular embodiment of the pixel circuit. Patent Owner gives no reason why this teaching has to be reiterated each and every time a new embodiment of the pixel circuit is introduced, and we can see none. Nothing indicates this disclosure of interchangeability is specifically tied to any particular embodiment other than the embodiment shown in Figures 33A–33E, and Patent Owner has provided no reason why it would be. We find this teaching has general applicability across all disclosed embodiments.

Second, Patent Owner argues that Kimura's teaching of replacing the “first or fourth” transistor in the embodiment of Figures 33A–33E, disclosed as nMOS type transistor, does not support replacing both the first and fourth transistor with pMOS type transistor. Prelim. Resp. 26–28. We agree, and we already determined above that we do not rely on that aspect of Petitioner's assertions. *See supra* n.6.

and do not rely on them in making our decision. Further, we find Kimura's teaching to use a pMOS transistor for the first or fourth transistor hinges on using nMOS transistor for the other transistor in the pair, and thus does not support the all-PMOS design proposed by Petitioner. Also, replacing just the third transistor with a pMOS transistor does not result in Petitioner's proposed all-pMOS design.

Patent Owner further asserts that Kimura’s disclosure of changing just one of the first or fourth transistor to pMOS type transistor is, if anything, a teaching away from using only pMOS transistors in the embodiment shown in Kimura’s Figures 33A–33E. Prelim. Resp. 28–29. We disagree. That Kimura describes a benefit for making the first and fourth transistor of different polarity types does not constitute a teaching away from having them both being of the same polarity type.

A reference teaches away from a claimed invention if it criticizes, discredits, or otherwise discourages modifying the reference to arrive at the claimed invention. *See In re Fulton*, 391 F.3d 1195, 1201 (Fed. Cir. 2004). The Court of Appeals for the Federal Circuit has stated: “[T]he prior art’s mere disclosure of more than one alternative does not constitute a teaching away . . . because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed.” *Fulton*, 391 F.3d at 1201. Accordingly, in order for there to be teaching away, the statement in Kimura must rise above merely assessing the advantages and disadvantages among viable alternatives. It does not. The Federal Circuit explained that “[c]hoosing one alternative necessarily means rejecting the other,” and that “[t]his interpretation of our case law [treating the choosing of one alternative as a teaching away from the other alternative] fails.” *Fulton*, 391 F.3d at 1201. Thus, we do not find that Kimura teaches away from making the first and the fourth transistor of the same polarity type.

(2) *Patent Owner’s Assertion of Complexity*

Patent Owner asserts that Petitioner’s “all-PMOS version of Figure 33 is not a ‘simple design choice.’” Prelim. Resp. 30. Patent Owner explains:

Petitioner’s proposal does not involve a choice between two alleged alternatives (NMOS versus PMOS) for one switching

transistor of a pixel circuit. Instead, the proposal requires that the PMOS transistors be chosen not once, but four (or five) times, and is thus one of sixteen (or thirty-two) distinct permutations of NMOS and PMOS transistors for the five-transistor circuit of Figure 33.

Id. The argument is unavailing. Patent Owner has made the issue more complicated than it is or needs to be. Kimura already discloses that either p-type or n-type transistors can be used for switching transistors. We do not agree at this stage that the merits of Petitioner’s obviousness case are impacted meaningfully merely by the number of switching transistors Petitioner proposes to change. Given the teaching that either p-type or n-type transistors can be used for switching transistors in the pixel circuit, Ex. 1002 ¶¶ 438, 649, we are persuaded preliminarily, based on the present record, that choosing nMOS, pMOS, or transistors of mixed types would be a simple design choice for a person of ordinary skill in the art.

Patent Owner further asserts:

As Petitioner acknowledges, NMOS transistors turn on by an “active high” gate signal whereas PMOS transistors turn on by an “active low” signal. Pet. at 4. This is a significant functional difference. For example, an “all PMOS” circuit would preclude the reduction in gate lines discussed in the prior subsection (for the alleged “first” and “fourth” transistors made possible by having them have opposite polarities) and may thus require additional gate lines. *See generally* Section VI.A.1, above. As Petitioner also acknowledges, “Kimura itself [teaches that] reducing the number of control lines improves aperture ratio.” Pet. at 65 (discussing claim, 13, citing Kimura at ¶¶ 429, 421–422).

Additionally, an “active low” signaling scheme would require corresponding changes to the driver circuit that sends the selection gate signals to the pixel circuits. The timing of these signals is critical to the overall operation of the display. For example, it was known at the relevant time that PMOS transistors

are slower in operation as compared to NMOS transistors. See, e.g., Ex. 2004 at 17 (“NMOS-only logic[] has the advantage of higher speed over the PMOS logic”).

Prelim. Resp. 31–32 (alterations in original). The arguments are misplaced and unavailing.

Although nMOS and pMOS type transistors operate differently, e.g., one is turned on by a positive voltage at the gate electrode and the other is turned on by a negative voltage at the gate electrode, that does not preclude them from both being usable to provide a switching function, as Petitioner demonstrates, which we discussed above. And, even though the number of gate lines can sometimes be reduced by having both nMOS and pMOS type switching transistors in a pixel circuit, it does not follow that the use of only pMOS type switching transistors in a pixel circuit is beyond the level of ordinary skill in the art.

Patent Owner does not contend that one of ordinary skill in the art would have any trouble determining how many gate lines would be needed if there were only pMOS type switching transistors in the pixel circuit. It is not necessary to show that a modification is “the *best* option, only that it be a *suitable* option.” See *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); *Par Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197–98 (Fed. Cir. 2014). Even if pMOS transistors are slower in operation than nMOS transistors, that is inconsequential given the teaching that for switching transistors in the pixel circuit, either p-type or n-type transistors can be used, as discussed above. And, again, only a suitable option need to be shown by Petitioner, not a choice that is necessarily better in each and every respect. See *id.*

Patent Owner asserts that Dr. Foty's testimony in paragraphs 57 and 154 of his Declaration should be entitled to little or no weight because it is conclusory. Prelim. Resp. 32. Based on the preliminary record, we disagree. Dr. Foty testifies:

Given the express teachings of Kimura and the knowledge of a POSITA, there would have been far more than a reasonable likelihood of success in using an all-PMOS implementation. Indeed, such changes were both well-known in the art at the time, and well within the skill of a POSITA. While an all-PMOS version would require active-low signaling on the pMOS gates, this was also extremely well-known in the art – and would have been easy for a POSITA to implement.

Ex. 1003 ¶ 154. Dr. Foty also testifies:

If the design need is for a transistor to be used as a simple on/off switch, then either an nMOS transistor or a pMOS transistor can be chosen – since, as shown in the figure from Kang and Leblebici 2003 [Ex. 1011] above [in ¶ 56 of the same Declaration], each can function as a simple on-off switch. As the primary operational difference between nMOS and pMOS (when a simple switch is desired) is that the on/off characteristics are the opposite of each other – and the on-off signals to be applied must be altered (i.e., reversed as it were) to account for this. In particular, as described in Section VII.A.1, nMOS devices turn on in response to a “high” voltage on the gate terminal and turn off when a “low” voltage is applied. This is known in the art as “active-high” signaling. pMOS transistors are just the opposite – they turn on when a “low” voltage is applied to the gate terminal and turn off in response to a “high” voltage on the gate. This is known in the art as “active-low” signaling. Changing the polarity of a switching transistor (from nMOS to pMOS or vice versa) would require changing the polarity of the gate signal to achieve the same functionality, but doing so was easy and well-known to a POSITA.

Id. ¶ 57 (the reference to Kang and Leblebici 2003 identifies a figure which illustrates a CMOS inverter having an nMOS switch and a pMOS switch).

The above-quoted testimony of Dr. Foty is not merely conclusory. Rather, it relies on the disclosures of Kang, Leblevici 2003, and Kimura. It also relies on the level of ordinary skill in the art and explains specifically how the change from nMOS to pMOS switching transistor, and vice versa, would be done. Also, notably, Patent Owner does not assert that implementing a switching transistor by a pMOS transistor exceeds the level of ordinary skill in the art. We also preliminarily credit the testimony of Dr. Foty because it currently stands unrebutted.

(3) *Patent Owner's Assertion of Lack of Motivation, "could have" versus "would have"*

Patent Owner further argues that Petitioner's "interchangeability" arguments amount to a suggestion that one of ordinary skill in the art "could" have modified the various transistors, rather than "would have" modified the transistors to just a single type, pMOS. Prelim. Resp. 33–34. The argument is unavailing.

Where the rationale for modification is interchangeability of parts, if Petitioner sufficiently establishes interchangeability, Petitioner need not separately assert that one of ordinary skill would have made the change, because interchangeability itself provides the motivation to change. Interchangeability implies that, to one of ordinary skill in the art, either choice is a suitable option. Recognition of a suitable option provides sufficient motivation to make a change. *See Intel Corp.*, 61 F.4th at 1380; *Par Pharm, Inc.*, 773 F.3d at 1197–98.

(4) *Patent Owner's Assertion that Kimura '798 does Not Support Changing Kimura's Third Transistor to a pMOS Transistor*

Patent Owner asserts “the alleged manufacturing benefit of an all-PMOS circuit has no support in Kimura and, to the contrary, is inconsistent with Kimura’s disclosures.” Prelim. Resp. 35. We address below Petitioner’s theory that it would have been obvious to modify Kimura based on a manufacturing benefit for a circuit having all-pMOS type transistors. Here, we address Patent Owner’s argument regarding potential inconsistencies between Petitioner’s theory and Kimura’s disclosures.

Patent Owner asserts that Kimura includes extensive disclosures directed to active matrix devices using CMOS (having complementary nMOS and pMOS components), and “that its process, which forms a CMOS driver together with a CMOS pixel circuit, confers manufacturing advantages—‘the process is shortened and it can contribute to the reduction in manufacturing cost and improvement of a yield.’ [Ex. 1002] at ¶ 571.” Prelim. Resp. 36. The alleged benefit for the process of making a CMOS circuit appears to be relative to other methods of manufacturing a CMOS circuit, not with respect to a process of manufacturing a circuit having only pMOS components. Nonetheless, even assuming that Kimura discloses a manufacturing method for a CMOS circuit including both nMOS and pMOS transistors, which has certain advantages over a method of manufacturing a circuit having only pMOS elements, that still does not undermine Petitioner’s theory based on general interchangeability of nMOS and pMOS transistors used only as switching transistors. The law on obviousness does not require Petitioner’s proposed modifications to be superior to the prior art in every way. It is not necessary for a showing of obviousness that a

modification be the best option, as it need only be a “suitable option.”

Intel Corp., 61 F.4th at 1380.

(5) *Conclusion*

For the foregoing reasons, we are sufficiently persuaded, for institution purposes, that it would have been obvious to one of ordinary skill in the art to make a modification of Kimura’s embodiment shown in Figures 33A–33E to use pMOS type transistors for all switching transistors in the pixel circuit, which leads to an all pMOS version of Kimura’s Figure 33 embodiment.

b) *Second Theory*

We question the completeness of the second theory. The second theory appears incomplete because what is shown in Figures 33A–33E is merely a pixel circuit and does not include other components which are fabricated on the same substrate. Patent Owner notes that in addition to the pixel circuit, Kimura discloses a CMOS driver circuit, separate from the pixel circuit, on the same semiconductor substrate, which includes complementary nMOS and pMOS transistors. PO Resp. 36. Petitioner has not asserted, much less explained, the interchangeability of a CMOS pair of nMOS and pMOS transistors with either two nMOS transistors or two pMOS transistors.

At this stage, the record does not show sufficiently how a circuit would stay operative if a CMOS pair of nMOS and pMOS transistors were replaced with two nMOS transistors or two pMOS transistors. Petitioner does not explain how two nMOS transistors or two pMOS transistors would provide the same outputs, as seen from the other connected elements in the circuit, as a CMOS pair of complementary nMOS and pMOS transistors.

The parties may further develop this issue subsequent to institution of trial. On the current record, we are not persuaded by Petitioner's second theory in support of an all p-MOS version of Kimura's Figure 33 embodiment.

3. *Independent Claim 7*

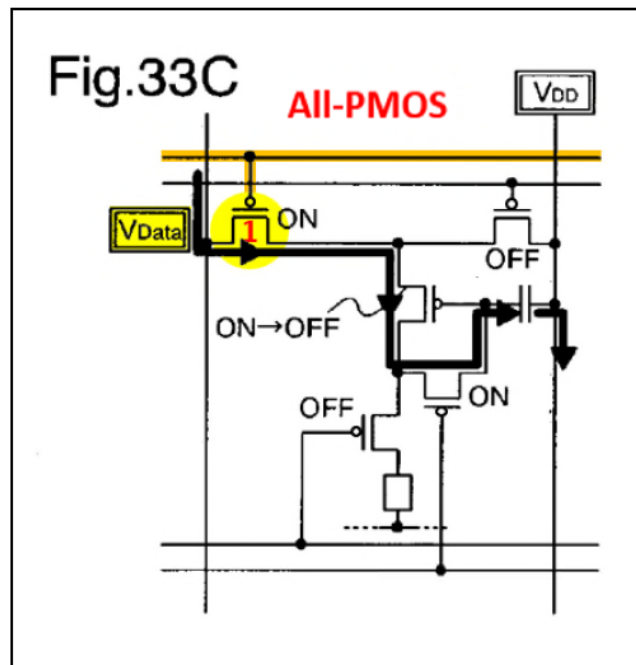
a) *[Claim 7 Preamble]*

In its preamble, claim 7 recites: "A pixel circuit in an organic light emitting device." Ex. 1001, 9:35. Petitioner explains that Kimura relates to the configuration of an active matrix light emitting device and discloses that an organic light emitting material can be used as the electroluminescent layer. Pet. 23 (citing Ex. 1002 ¶¶ 0001, 0556–0557). Petitioner further explains that Kimura's semiconductor device has a plurality of pixels arranged in a matrix shape over a substrate, and that each pixel includes the electroluminescent element that emits light, and driving circuitry such as a driver TFT (thin film transistor) for performing control of electric current supplied to the electroluminescent element. *Id.* at 24.

On the basis of the foregoing, and assuming the preamble is limiting, Petitioner asserts that Kimura discloses a pixel circuit in an organic light emitting device. *Id.* at 23. The assertions are supported by the cited disclosures and not disputed by Patent Owner. We are sufficiently persuaded that Kimura discloses the preamble recitation of claim 7. We need not determine whether the preamble is limiting.

b) *Limitation [7a]*

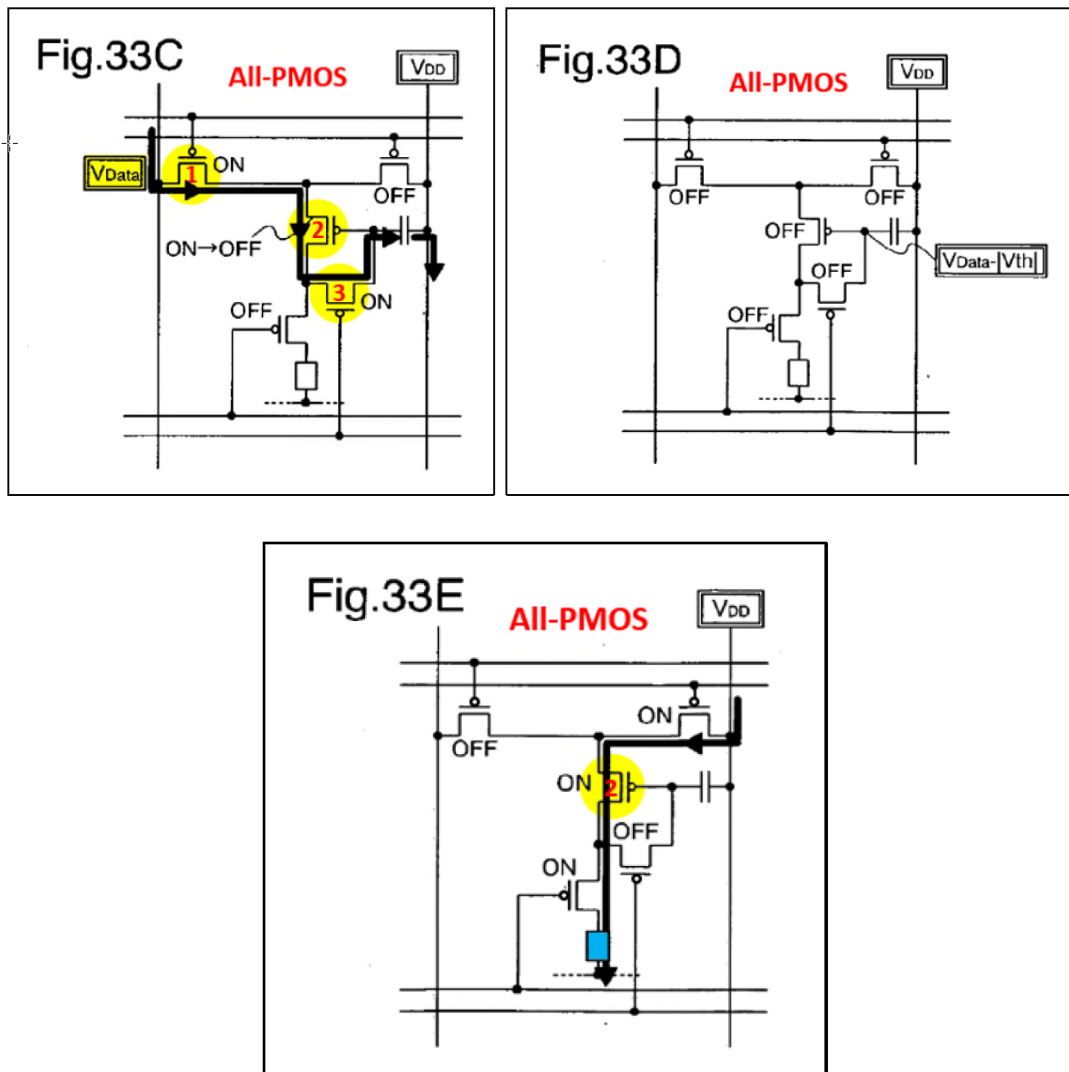
Claim 7 in limitation [7a] recites: "a first transistor for delivering data signal voltage in response to a current scan line signal." Ex. 1001, 9:37–38. Petitioner relies on an all-PMOS version of Kimura's Figure 33C, color annotated by Petitioner and reproduced below (Pet. 25):



In this version of Kimura's Figure 33C, Petitioner identifies and numbers Transistor 1 as the claimed first transistor, and explains how Transistor 1 delivers data signal voltage (shown as V_{Data}) in response to a current scan line signal (colored orange). Pet. 24–27 (both V_{Data} and Transistor 1 are highlighted yellow). Patent Owner does not dispute these assertions. Petitioner's assertions are supported by the cited evidence, and Petitioner has sufficiently shown that limitation [7a] is met by Kimura.

c) Limitation [7b]

Claim 7 in limitation [7b] recites: "a second transistor for programming the data signal voltage and for generating a driving current in response to a programmed data signal when light is emitted." Ex. 1001, 9:39–41. Petitioner uses an all-pMOS version of Kimura's Figures 33C, 33D, and 33E, color annotated by Petitioner and reproduced below, to illustrate its contentions for this limitation (Pet. 30, 32):



In this version of Figure 33A, Petitioner shows the current flow in black arrows when Transistors 1, 2, and 3 are turned on. Ex. 1002 ¶ 0655.

Transistors 1, 2, and 3 are numbered in red and highlighted in yellow. In this version of Figure 33D, the capacitor is shown being charged to a self-compensating voltage $V_{\text{Data}} - |V_{\text{th}}|$. In this version of Figure 33E, Petitioner shows the current flow in black arrows during the light-emitting mode. Ex. 1002 ¶ 0656. Transistor 2 is numbered in red and highlighted in yellow. EL element is highlighted in blue.

Petitioner identifies Transistor 2 as the claimed second transistor, and asserts Transistor 2 performs the claimed functions of (1) “programming the data signal voltage,” and (2) “generating a driving current in response to a programmed data signal when light is emitted.” Pet. 28. Regarding the programming functionality, Petitioner explains as follows:

Kimura explains that, when the first, second, and third transistors are on (and all others off), current flows as shown in Fig. 33C. EX1002, [0655]. As a result, “the voltage between the gate and the source of the TFT 3308 [the second transistor] eventually becomes equal to the threshold voltage.” *Id.* The operation and role of the capacitor is discussed in more detail *infra* in connection with claim element 7[d] (“a capacitor for maintaining the data signal voltage programmed onto the second transistor”). Relevant here, just like the capacitor in ’99 patent Fig. 3, the capacitor in Kimura Fig. 33 charges to a self-compensating voltage (*viz.*, $V_{\text{Data}} - |V_{\text{th}}|$). See EX1002, Fig. 33D; EX1003, ¶¶135–137 and ¶ 180.

Pet. 29 (alteration in original). Regarding the functionality of generating a driving current in response to a programmed data signal when light is emitted, Petitioner explains as follows:

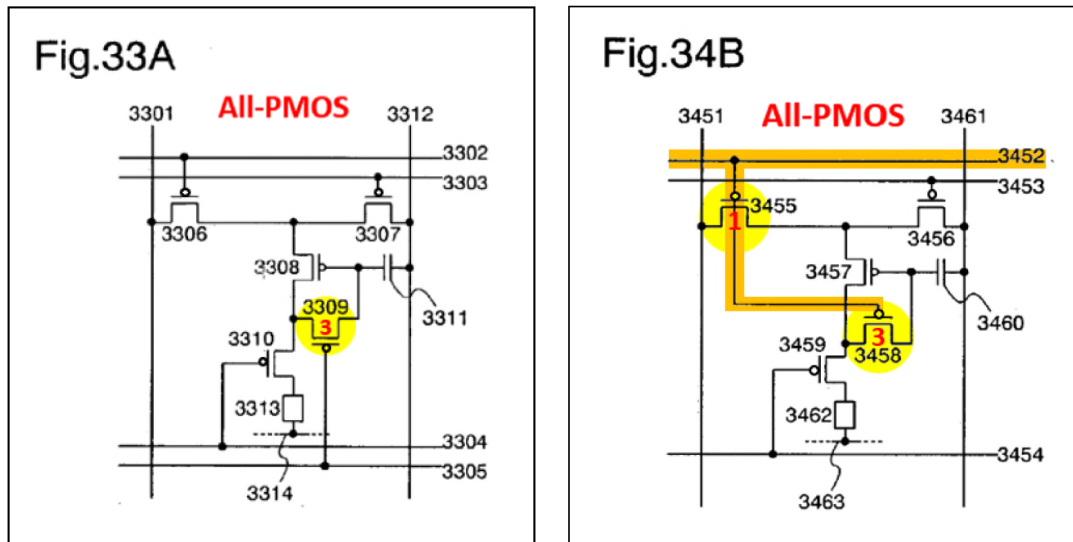
The solid black arrows in Fig. 33E illustrate current flowing through the “ON” transistors when in light emitting mode. See EX1002, [0656] (“The voltage between the gate and the source of the TFT3308 [shown in yellow] therefore exceeds the threshold voltage to cause it to turn on, so that electric current flows in the EL device 3313 to cause it to emit light.”). The “programmed data signal voltage” stored on the capacitor (*i.e.*, $V_{\text{Data}} - |V_{\text{th}}|$) activates the second transistor to push current through the light emitting diode to emit light.

Id. at 31 (alteration in original).

Petitioner’s assertions are supported by the cited evidence. Patent Owner does not dispute these assertions about limitation [7b]. Petitioner has sufficiently shown that limitation [7b] is met by Kimura.

d) *Limitation [7c]*

Claim 7 in limitation [7c] recites: “a third transistor for providing the data signal voltage for the second transistor in response to the current scan signal.” Ex. 1001, 9:42–44. Petitioner relies on an all-pMOS version of Kimura’s Figures 33A and 34B, color annotated by Petitioner and reproduced below (Pet. 32, 36):



In this version of Figure 33A, Petitioner has numbered in red and highlighted in yellow the third transistor. In this version of Figure 34B, Petitioner has numbered in red and highlighted in yellow the first transistor and the third transistor, and highlighted in orange current scan signal line 3452 which is shared by the gate of Transistor 1 and Transistor 3.

Petitioner identifies Transistor 3 in this all-pMOS version of Figure 33A as the claimed “third resistor.” Pet. 32. Petitioner asserts that this Transistor 3 performs the recited function of “providing the data signal voltage for the second transistor in response to the current scan signal.” *Id.* at 33. Petitioner explains that this function programs the charge on the capacitor and requires a shared control signal, i.e., the current scan signal,

that simultaneously activate the first and the third transistor to charge the capacitor and that otherwise turn them off. *Id.* at 34. Petitioner further explains:

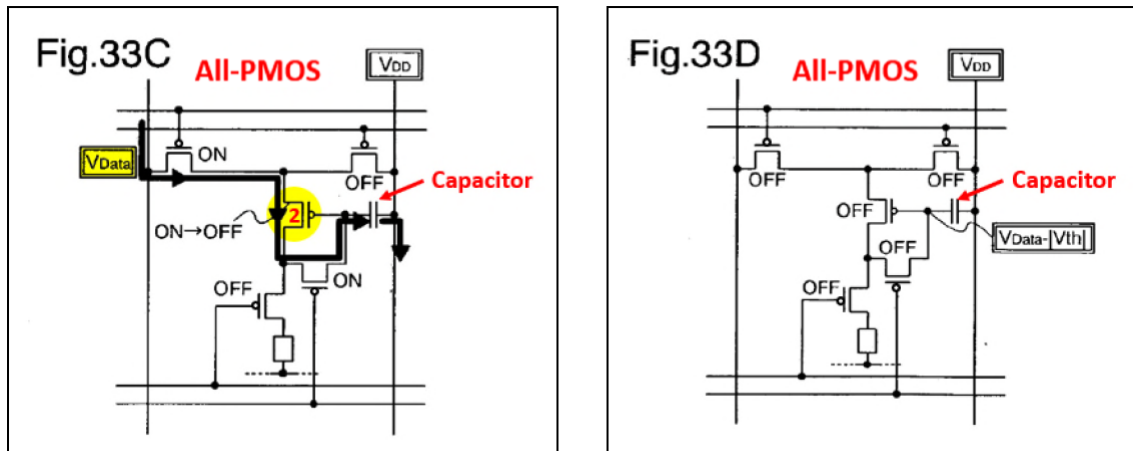
Although Kimura Fig. 33 does not expressly show a shared signal that controls both the first and third transistors, Kimura explains that “the TFT 3306 [first transistor] and the TFT 3309 [third transistor] in FIG. 33A are controlled to turn on and off at the same time. They can therefore be controlled by using the same gate signal line 3452, as shown in FIG. 34B.” *Id.*, [0659]. A version of Fig. 34B highlighting the shared “current scan signal” line for the first and third transistors is shown below. In response to the signal on line 3452 (the “current scan line”), the third transistor (labelled 3458 in Fig. 34B and 3309 in Fig. 33A) charges the capacitor and provides the gate of the second transistor (labelled 3457 in Fig. 34B and 3308 in Fig. 33A) with the data signal voltage. It would have been obvious to a POSITA to use the shared signal of Fig. 34B in Fig. 33. EX1003, ¶185.

Id. at 35 (alterations in original).

Petitioner’s assertions are supported by the cited evidence. Patent Owner does not dispute these assertions about limitation [7c]. Petitioner has sufficiently shown that Kimura reasonably would have suggested limitation [7c] to one of ordinary skill in the art.

e) Limitation [7d]

Claim 7 in limitation [7d] recites: “a capacitor for maintaining the data signal voltage programmed onto the second transistor.” Ex. 1001, 9:45–46. Petitioner uses an all-PMOS version of Kimura’s Figures 33C and 33D, color annotated by Petitioner and reproduced below, to illustrate its contentions for this limitation (Pet. 37):



In this version of Figure 33C, Petitioner identifies a current path, in black arrowed line, that charges the capacitor that is labeled in red. Pet. 37. Transistor 2 is numbered in red and highlighted in yellow. *Id.* In this version of Figure 33D, Petitioner has labeled the capacitor in red and indicated the voltage across the electrodes of the capacitor as $V_{Data} - |V_{th}|$. *Id.*

Petitioner explains:

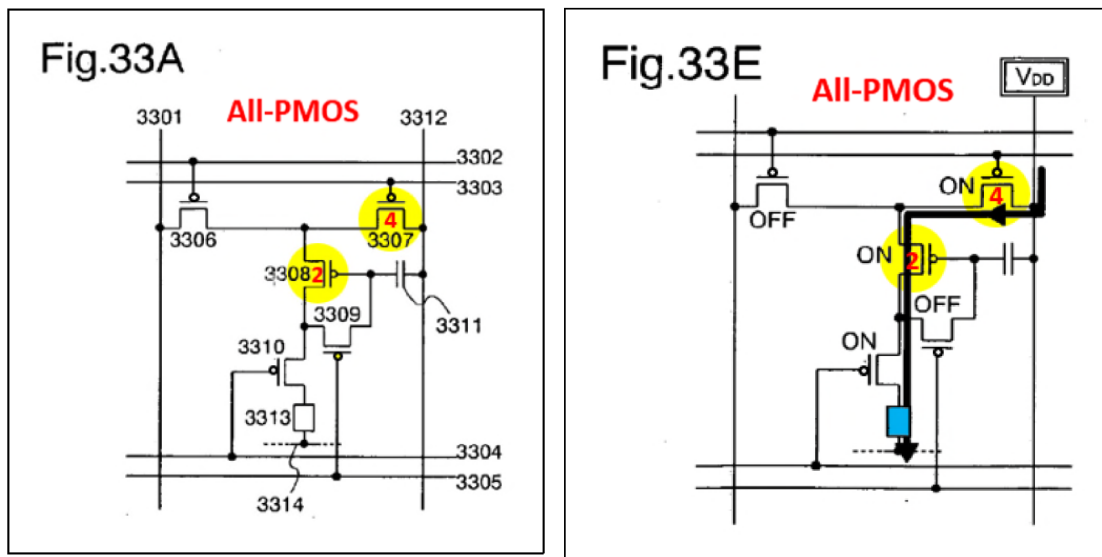
The black arrows in Fig 33C show current flow onto the capacitor which charges the capacitor (*i.e.* “program[s]” it) with the “data signal voltage.” EX1002, [0655] (“[E]lectric charge moves as shown in FIG. 33C. The voltage between the source and the drain of the TFT 3308 [second transistor]...eventually becomes equal to the threshold voltage, at which point the TFT 3308 [second transistor] turns off as shown in FIG. 33D.”). As was well-known in the art at the relevant time, capacitors store charge and maintain a voltage until discharged. EX1003, ¶37. Kimura’s capacitor—connected to the gate of second transistor 3308—maintains the “data signal voltage” on that node. As shown in Fig. 33D, the capacitor’s voltage across its electrodes equals $V_{Data} - |V_{th}|$. EX1003, ¶¶190-192 and ¶¶134-137.

Id. (alterations in original).

Petitioner’s assertions are supported by the cited evidence. Patent Owner does not dispute these assertions about limitation [7d]. Petitioner has sufficiently shown that Kimura discloses limitation [7d].

f) Limitation [7e]

Claim in limitation [7e] recites: “a fourth transistor for delivering a power supply voltage to the second transistor when the light is emitted.” Ex. 1001, 9:47–48. Petitioner uses an all-PMOS version of Kimura’s Figures 33A and 33E, color annotated by Petitioner and reproduced below, to illustrate its contentions for this limitation (Pet. 39, 41):



In this version of Figure 33A, Petitioner has numbered in red Transistors 2 and 4, and also highlighted Transistors 2 and 4 in yellow. In this version of Figure 33E, Petitioner has labeled a current path in black arrows through Transistors 2 and 4 and the EL element, and highlighted the EL element in blue. Petitioner identifies Transistor 4 (3307) in these figures as the claimed fourth transistor. Pet. 40. Petitioner explains:

Kimura explains that “[t]he TFTs 3307 [fourth transistor] and 3310 [fifth transistor] then turn on. The electric potential of a source region of the TFT 3308 [second transistor] increases from V_{Data} to VDD as the TFT 3307 [fourth transistor] turns on.” *Id.* This results in “electric current flows in the EL device 3313 to cause it to emit light, as shown in FIG. 33E.” *Id.*; see also EX1003, ¶¶194–198. Thus, Kimura discloses “a fourth transistor

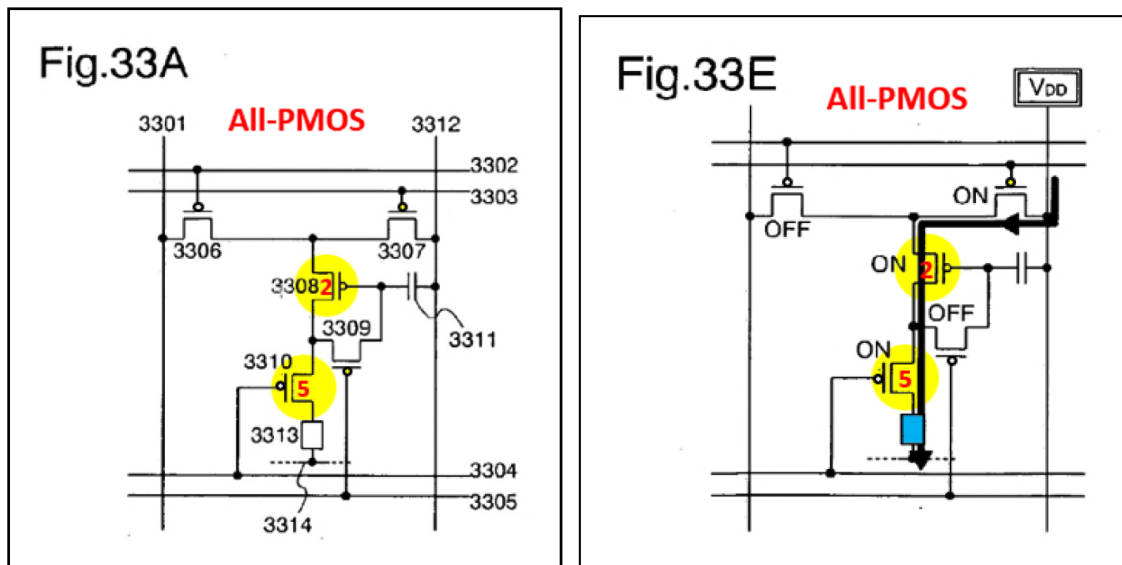
for delivering a power supply voltage to the second transistor when the light is emitted.”

Id. (alteration in original).

Petitioner’s assertions are supported by the cited evidence. Patent Owner does not dispute these assertions about limitation [7e]. Petitioner has sufficiently shown that Kimura discloses limitation [7e].

g) Limitation [7f]

Claim 7 in limitation [7f] recites: “a fifth transistor for delivering the driving current, provided from the second transistor, in response to the data signal voltage when the light is emitted.” Ex. 1001, 9:49–51. Petitioner relies on an all-PMOS version of Kimura’s Figures 33A and 33E, color annotated by Petitioner and reproduced below (Pet. 42, 44):



In this version of Figure 33A, Petitioner identifies Transistor 5 (3310) as the fifth transistor and numbers Transistors 2 and 5 in red as well as highlights them in yellow. Pet. 41–42. In this version of Figure 33E, Petitioner illustrates the current flow through Transistors 2 and 5 with black arrowed

lines. *Id.* at 43–44. Transistors 2 and 5 are numbered in red and highlighted yellow, and the EL element is highlighted blue. *Id.* at 44.

Petitioner explains:

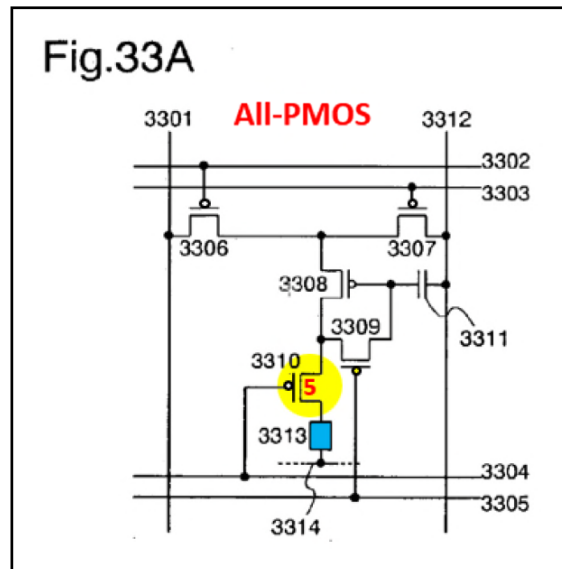
After the fourth and fifth transistors turn on, “[t]he voltage between the gate and the source of the TFT 3308 [second transistor] exceeds the threshold voltage to cause it to turn on, so that electric current flows in the EL device 3313 to cause it to emit light.” *Id.* The fifth transistor is connected in series with the second transistor such that the fifth transistor delivers the drive current provided by the second transistor. EX1003, ¶202. The driving current is “in response to the data signal voltage” because that voltage is stored on the capacitor and controls the second transistor. *Id.*, [0655] (explaining that electric charge flows onto the capacitor in Fig. 33C); *see also* EX1003, ¶202 and ¶¶136–140. Thus, Kimura satisfies claim element 7[f].

Id. at 43 (alterations in original).

Petitioner’s assertions are supported by the cited evidence. Patent Owner does not dispute these assertions about limitation [7f]. Petitioner has sufficiently shown that Kimura discloses limitation [7f].

h) Limitation [7g]

Claim 7 in limitation [7g] recites: “an electroluminescent element for emitting light corresponding to the driving current delivered through the fifth transistor.” Ex. 1001, 9:52–54. Petitioner uses an all-PMOS version of Kimura’s Figures 33A, color annotated by Petitioner and reproduced below, to illustrate its contentions for this limitation (Pet. 45):



In this version of Figure 33A, Petitioner numbers in red and highlights in yellow Transistor 5, and highlights in blue electroluminescent element 3313 for emitting light. Petitioner asserts: “Kimura explains that ‘electric current flows in EL device 3313 to cause it to emit light.’ EX1002, [0656].

Elsewhere, Kimura explains the ‘EL’ refers to ‘electroluminescent.’ *See, e.g., id.*, [0002].” Pet. 44. Petitioner further explains that because the second transistor (3308) which regulates the drive current is in series with the fifth transistor which merely acts as an on/off switch, “the current driven by the second transistor is delivered through the fifth transistor to the electroluminescent element.” *Id.* at 45 (citing Ex. 1003 ¶¶ 204–207).

Petitioner further explains why the amount of light emitted by the electroluminescent element corresponds to the drive current delivered through the fifth transistor:

The amount of light emitted from an OLED electroluminescent element varied based on the current driven through it. *See, e.g.*, EX1002, [0359] (discussing problems with the “dispersion in the brightness of the EL devices” due to differences in current flow), [0390]; EX1001, 4:22–24 (“An electroluminescent element emits light corresponding to the

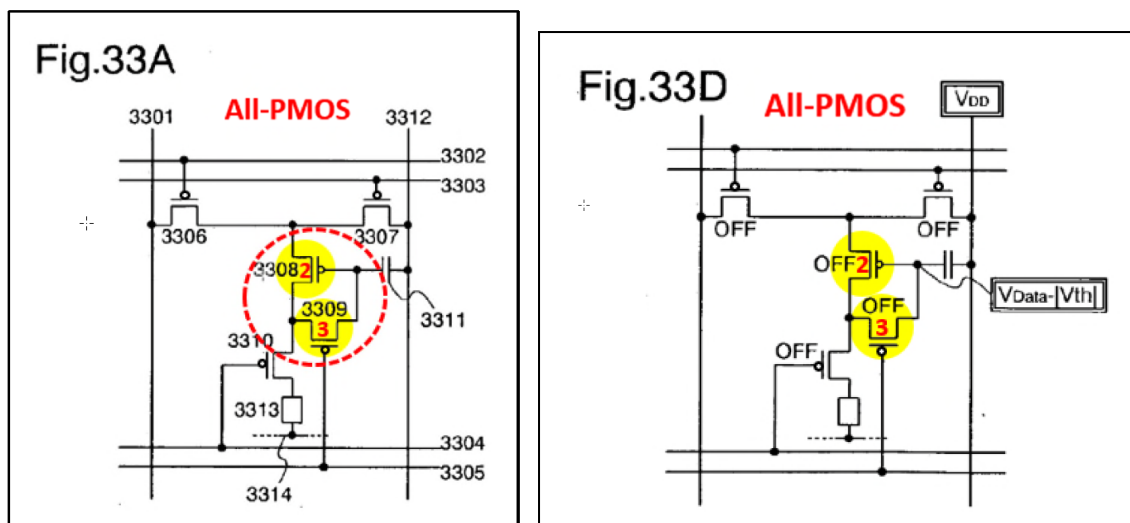
driving current”); *see also* EX1003, ¶85. And the amount of current driven was determined, in part, by the gate voltage applied to the driving transistor. EX1002, [0359], [0654] (second transistor “behaves as a driver TFT for performing control of electric current supplied to an EL device 3313.”); EX 1003, ¶¶205–206. Indeed, fixing problems caused by this characteristic was a motivation to Kimura.

Id. at 45–46.

Petitioner’s assertions are supported by the cited evidence. Patent Owner does not dispute these assertions about limitation [7g]. Petitioner has sufficiently shown that Kimura discloses limitation [7g].

i) *Limitation [7h]*

Claim 7 in limitation [7h] recites: “wherein the third transistor connects the second transistor in the form of a diode in response to the current scan signal so that the second transistor detects and compensates its threshold voltage deviation in itself.” Ex. 1001, 9:55–58. Petitioner uses an all-PMOS version of Kimura’s Figures 33A and 33D, color annotated by Petitioner and reproduced below, to illustrate its contentions for this limitation (Pet. 47–48):



In this version of Figure 33A, Petitioner has circled in red the connection between Transistors 2 and 3, which makes Transistor 2 behave as a diode when Transistor 3 is turned on. Ex. 1002, ¶¶ 379, 654. Transistors 2 and 3 are numbered in red and highlighted in yellow. In this version of Figure 33D, Petitioner shows storing of self-compensated voltage, i.e., $V_{\text{Data}} - |V_{\text{th}}|$, on the capacitor. Transistors 2 and 3 are numbered in red and highlighted in yellow.

Petitioner asserts that the circuit configuration highlighted in the Figure 33A illustration above is referred to as a “diode connection” configuration, and that as Kimura explains, “the TFT 3308 [second transistor] exhibits the behavior as a diode connected TFT when the TFT 3309 [third transistor] is on.” Pet 46 (alterations in original) (citing Ex. 1002 ¶¶ 379, 654). Petitioner explains that the third transistor connects the second transistor in the form of a diode “in response to the current scan signal,” because that connection occurs “only when the signal controlling the gate of the third transistor is asserted.” *Id.* at 47. Petitioner notes that the Figure 33D illustration above shows the result in which a self-compensated voltage, i.e., $V_{\text{Data}} - |V_{\text{th}}|$, is stored on the capacitor. *Id.* (citing Ex. 1002 ¶ 655; Ex. 1003 ¶¶ 135–137, 213). Petitioner further explains that providing self-compensation for threshold voltage variation of the second transistor is precisely why the third transistor is included in Kimura’s embodiment shown in Figures 33A–33E. *Id.* at 48 (citing Ex. 1002 ¶¶ 652–657).

Petitioner’s assertions are supported by the cited evidence. Patent Owner does not dispute these assertions about limitation [7h]. Petitioner has sufficiently shown that Kimura discloses limitation [7h].

j) *Conclusion*

For reasons discussed above, Petitioner has shown a reasonable likelihood that it would prevail in establishing obviousness of claim 7 over Kimura.

4. *Dependent Claims 9–12*

Claims 9–12 each depend, directly or indirectly, from claim 7. Ex. 1001, 9:59–10:19. Petitioner specifically addresses all of them in detail. Pet. 56–62. Petitioner’s assertions are supported by the cited evidence, and Patent Owner does not present any argument additional to those it presents for claim 7. Petitioner has shown a reasonable likelihood that it would prevail in establishing obviousness of each of claims 9–12 over Kimura.

5. *Dependent Claim 8*

Claim 8 depends from claim 7 and further recites: “a sixth initialization transistor for discharging the data signal voltage stored in the capacitor in response to a scan signal just before the current scan signal upon initialization.” Ex. 1001, 9:59–64.

Petitioner begins its analysis of claim 8 with the following description of the initialization operation, making reference to the Specification of the ’599 patent including Figure 5:

The purpose and operation of sixth transistor T34 [as an initialization transistor] is described at col. 7:15–27. In summary, the sixth transistor (T34) is active during an “initialization operation” when the control signals for other transistors are unasserted. EX1001, 7:15–17. As shown in Fig. 5, the sixth transistor (T34) is connected to the capacitor and, during initialization, *discharges the capacitor from residual voltage to “ V_{init} ” voltage*. *Id.*; EX1003, ¶¶218–220. Because the sixth transistor’s gate is controlled by the scan[n-1] signal (*i.e.*, the previous scan signal), the sixth transistor performs the discharge function “in response to a scan signal just before the

current scan signal upon initialization.” See EX1001, 7:6–8, 7:15–27.

Pet. 50 (emphasis added) (second alteration in original). Petitioner’s color-annotated version of Figure 5 of the ’599 patent is reproduced below:

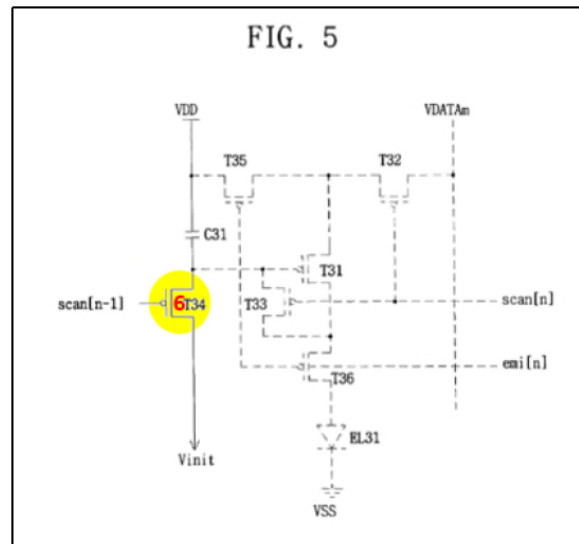
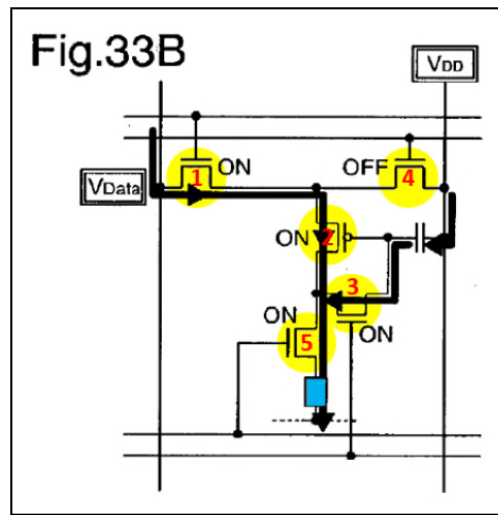


Figure 5 is one of several circuit diagrams for explaining the initialization operation, the programming operation, and the light-emitting operation. Ex. 1001, 6:4–7. The sixth transistor is numbered in red and highlighted in yellow. Patent Owner does not dispute the above-quoted assertions of Petitioner regarding the description in the ’599 patent about the initialization operation and initialization transistor.

Next, Petitioner continues with this assertion: “Kimura discloses that the fifth transistor in Fig. 33 ‘can also be used as an erasure [transistor]’ that resets the capacitor voltage to a default initialization value. EX1002, [0658].” Pet. 51. According to Petitioner, such use of Kimura’s fifth transistor as an erasure transistor resets the capacitor voltage to a default initialization value, is shown in Kimura’s Figure 33B. *Id.* at 18. Petitioner’s color-annotated version of Kimura’s 33B is reproduced below:



This version of Figure 33B shows current paths, in black arrows, passing through the EL element. The transistors are numbered and highlighted in yellow, and the EL element is highlighted in blue.

Petitioner explains: “[T]he black arrow coming from the right shows the current path which discharges the capacitor. This initialization approach, however, is less desirable because current discharges through the light emitting element causing undesired light emission.” Pet. 18. Based on its identification of an undesirable consequence of using the fifth transistor as an erasure transistor to reset the capacitor voltage, Petitioner proposes a modification to incorporate an additional transistor from Kimura’s embodiment of Figure 16 and 17, into Kimura’s Figure 33 embodiment to reset the capacitor voltage. Pet. 51–56.

Patent Owner asserts that Petitioner “Conflates ‘Initialization’ with ‘Erasure.’” Prelim. Resp. 16. On this record, that appears to be true. The record evidence does not support Petitioner’s assertion that the fifth transistor, when used as an erasure transistor, resets the capacitor voltage to a default initialization value. In particular, Kimura’s paragraph 658, cited by Petitioner, does not support this assertion. It reads as follows:

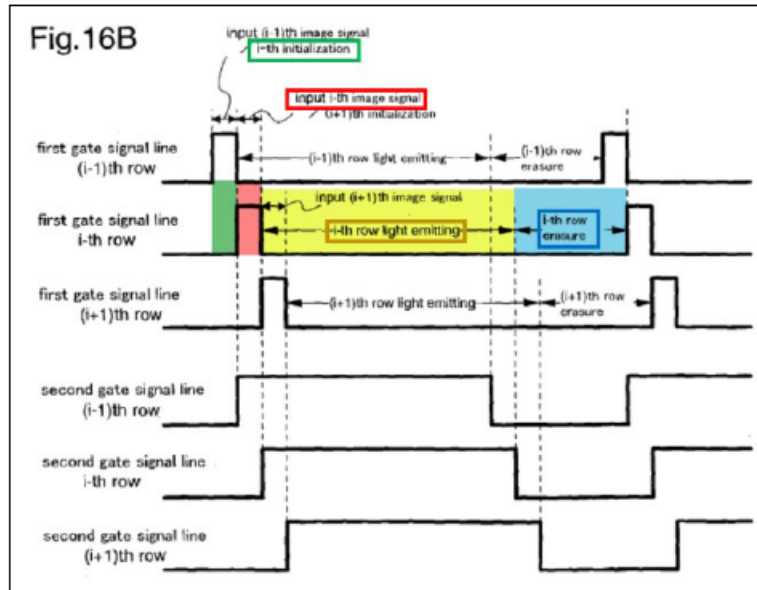
Further, the TFT 3310 [fifth transistor] can also be used as an erasure TFT when applying a driving method that uses a digital time gray scale method. In addition, the erasure TFT can be placed in any location, provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing.

Ex. 1002 ¶ 658. Based on the preliminary record, we agree with Patent Owner that “Kimura uses ‘erasure’ to mean ‘forcibly plac[ing] [the EL device] in a non-light-emitting state.” Prelim. Resp. 16 (alterations in original). In that regard, Kimura describes the following:

Electric current corresponding to the voltage between the gate and the source of the TFT 907 flows in an EL device 909 after image signal input is complete, as shown in Fig. 9B, and the EL device 909 emits light. A pulse is then input to the third gate signal line 913 when the timing for completion of the sustain (light emitting) period is reached, *the erasure TFT 914 turns on*, and the voltage between the gate and the source of the TFT 907 is set to zero, as shown in Fig. 9C. The TFT 907 therefore turns off, electric current flow to the EL device is cutoff, *and the EL device 909 is forcibly placed in a non-light emitting state*.

Ex. 1002 ¶ 410 (emphasis added). This description does not indicate the turning on of an erasure transistor discharges the capacitor to initialize the capacitor, much less discharges the capacitor through the EL device, as Petitioner contends. Instead, the EL device is forcibly placed into a non-light emitting state in an erasure operation. *Id.* Further supporting that understanding is Kimura’s paragraph 415, which states in part: “The erasure TFT 914 is on only during the sustain (light emitting) period. *The erasure TFT 914 is off during initialization*, image signal input, and the erasure period, and the current to the EL device 909 is thus cutoff.” *Id.* ¶ 415 (emphasis added). Kimura’s paragraph 415 indicates that erasure is an operation different from initialization. *Id.*

Additionally, Kimura's Figure 16B, which is a timing diagram for Kimura's embodiment of Figures 16–17 on which Petitioner relies to add a sixth initialization transistor, shows separate periods of initialization and erasure. Patent Owner's color-annotated version of Kimura's Figure 16B is reproduced below:



In this version of Figure 16B, Patent Owner has highlighted the initialization period in green and the erasure period in blue, and the two do not overlap. Prelim. Resp. 18. Further, the input image signal period is highlighted in red and a portion of the light emitting period is highlighted in yellow.

For the foregoing reasons, Petitioner has not shown sufficiently based on the present record that initialization and erasure are the same. Given that Petitioner grounds its reasoning for claim 8 on that theory, we question Petitioner's accounting for the alleged obviousness of claim 8 over Kimura.

6. *Dependent Claim 13*

Claim 13 depends from claim 7 and further recites:

wherein the *fourth transistor* composed of a PMOS transistor including a gate to which the current light-emitting signal is

applied, a source to which a power supply voltage is applied, and a drain coupled to the second transistor; and

the *fifth transistor* is composed of a PMOS transistor including a *gate to which the current light-emitting signal is applied*, a source coupled to the second transistor, and a drain coupled to the electroluminescent element.

Ex. 1001, 10:20–28 (emphasis added). Petitioner acknowledges that claim 13 requires the gates of both the fourth and fifth transistors to be controlled by “the current light emitting signal.” Pet. 63. Petitioner relies on an “all-PMOS version of Kimura Fig. 36.” *Id.* at 62–63. Petitioner explains:

Although Fig. 33B shows the fourth and fifth transistors controlled by different signals (viz., fourth transistor OFF while fifth transistor ON), that is not the case for Fig. 36. EX1003, ¶257. In all operation states of Fig. 36 (viz., Fig. 36B (initialization), Figs. 36C-D (programming), and Fig. 36E (light emission)), the fourth and fifth transistors are always ON/OFF together. EX1003, ¶257. Thus a POSITA would have understood (or at least found it obvious) that Kimura uses a shared light-emitting signal to control them. EX1003, ¶256-259. Kimura itself provides one reason for doing so—reducing the number of control lines improves aperture ratio. See, e.g., EX1002, [0429]; see also id., [0421]-[0422] (control scheme with fewer signals reduces “surface area occupied by wirings in a pixel”). Additionally, the fourth and fifth transistors must both be active during light emission, otherwise the electroluminescent element will not emit light. EX1003, ¶¶138-140; see also EX1002, [0659] (signals “turn[ing] on and off at the same timing . . . can therefore be controlled by using the same gate signal line”). This, too, would have naturally led a POSITA to use a shared light-emitting signal. EX1003, ¶¶ 258-259.

Moreover, Kimura discloses a timing diagram and control scheme utilizing only two signals (*i.e.*, first and second gate signals which map to the claimed “scan line signal” and “light

emitting signal” respectively). *See* EX1002, Figs. 16-17 and explanation at [0420]-[0429]; EX1003, ¶259. This disclosure would have motivated a POSITA to use a shared light emitting signal for the fourth and fifth transistors and provided a reasonable expectation of success. EX1003, ¶259.

Pet. 64–65 (emphasis added).

We agree that if the fourth and fifth transistors are always turned on and off together, as Petitioner asserts is the case for the embodiment of Figures 36A–36E, there is reason for one of ordinary skill in the art to drive the fourth and fifth transistors by the same control signal, i.e., reducing the number of control lines and improving aperture ratio.

However, Petitioner’s argument is questionable, because Petitioner’s reasoning only has application to the embodiment of Figures 36A–36E, where the fourth and fifth transistors are always on and off together, and does not apply to the embodiment of Figures 33A–33E in which the fourth and fifth transistors do not always turn on and off together. If the fourth and fifth transistors in the Figure 33 embodiment were to be controlled by the same shared signal, such that they have to be turned on and off together, they would produce outputs and make current connections and disconnections inconsistent with what the other components in the pixel circuit of the Figure 33 embodiment expect from them. Petitioner does not explain the effect this inconsistency has on the operation of the Figure 33 embodiment, e.g., whether anything useful results from the change.

The Figure 36 embodiment is also different structurally from the Figure 33 embodiment in that it makes use of six transistors, not five as in the case of the Figure 33 embodiment. In accounting for claim 7, Petitioner relied on the Figure 33 embodiment to meet each of the limitations regarding the first, second, third, fourth, and fifth transistors. It is questionable

whether the Figure 33 embodiment, after being modified to make the fourth and fifth transistor always turn on and off together, as Petitioner proposes based on the Figure 36 embodiment, would still meet all the requirements of the first, second, third, fourth, and fifth transistor, as recited in claim 7. Based on the present record, we find that Petitioner has not provided an adequate explanation as to this potential discrepancy.

Notably, we find the circumstance here to be different from Petitioner's proposal to modify all transistors of the nMOS type in Kimura's Figure 33 embodiment to pMOS type. In that proposal, the output of the switching transistor remains the same after the modification, and the other components in the pixel circuit, connected to the switching transistors, are unaffected by the modification. Here, the architecture differences between the embodiments in Kimura's Figures 33 and 36 result in different connections made and output signals provided to the other components in the pixel circuit. At this stage, Petitioner has not shown sufficiently that operations that used to be governed by a particular output from the fourth or fifth transistor in Figure 33 would continue to operate the same as they used to operate, when the output provided from the fourth or fifth transistor is different.

For the foregoing reasons, we question Petitioner's reasoning presented to account for claim 13. The parties may further develop the issue subsequent to institution of trial.⁷

⁷ Patent Owner argues that Petitioner's reliance on the Figure 36 embodiment is inconsistent with Petitioner's reasoning submitted to account for claim 8, which characterizes certain aspects of the Figure 36 embodiment as undesirable and then not adopt a certain feature from Kimura's embodiment of Figure 36. Prelim. Resp. 54–57. That argument appears

7. *Independent Claims 14, 15, and 17*

Claim 14 is substantially the same as claim 7, except for limitations [14f] and [14g]. Claim 14 via limitation [14f] additionally requires the fourth transistor to deliver a power supply voltage to the second transistor “in response to a current light-emitting signal.” Ex. 1001, 10:44–46. Claim 14 via limitation [14g] additionally requires the fifth transistor to provide drive current “in response to the current light-emitting signal.” *Id.* at 10:47–49. These additional features of claim 14 are essentially the same as those required by claim 13, which recites that the fourth transistor includes “a gate to which the current light-emitting signal is applied,” and that the fifth transistor includes “a gate to which the current light-emitting signal is applied.” *Id.* at 10:20–28. Petitioner relies on its reasoning for claim 13, discussed above, to account for limitations [14f] and [14g]. Pet. 69–71.

Given Petitioner’s reliance on the same analysis from claim 13, we find that the potential deficiencies discussed above for claim 13 apply equally to Petitioner’s analysis for claim 14.

Claim 15 is similar to claim 7, but differs in several respects. First, claim 15 requires each of first to fifth transistors be of the pMOS type. As discussed above in the context of claim 7, Petitioner has adequately accounted for the all p-MOS transistor requirement. Second, claim 15 requires the source of the second transistor be coupled to the drain of the first transistor. Petitioner adequately shows that in Kimura’s Figure 33

misplaced. The Figure 36 embodiment may have aspects which are desirable as well as aspects which are undesirable. In addition, Petitioner cites different aspects of Figure 36 for its analysis of claims 8 and 13. As such, we see no conflict between Petitioner’s positions for claims 8 and 13.

embodiment, the source of Transistor 2 is coupled to the drain of Transistor 1. Pet. 73. Third, claim 15 requires the drain and source of the third transistor be connected between a gate and drain of the second transistor. Petitioner asserts that its accounting for limitation [7c] and limitation [7h], together with an all p-MOS implementation of all switching transistors in Kimura's Figure 33 embodiment, accounts for the requirement that the drain and source of the third transistor be connected between a gate and drain of the second transistor. *Id.* at 59–60, 73–74. The assertion is supported by the cited evidence. Patent Owner argues only that it would not have been obvious for one of ordinary skill in the art to adopt an all p-MOS version of Kimura's Figure 33 embodiment, an argument we already determined above to be unavailing.

In addition, claim 15 recites: “the electroluminescent element having the one terminal coupled to the drain of the fifth transistor and the other terminal grounded.” Petitioner adequately accounts for this limitation, asserting:

Although the electroluminescent element's other terminal is not expressly identified as connected to ground in Fig. 33, a POSITA would have found it obvious to do so. EX1003, ¶¶311–314. It was well-known to POSITAs in 2003 that a forward-bias current must be applied to an LED to emit light. Because of Kimura's circuit configuration (with positive voltage at the light-emitting terminal connected to the fifth transistor), the simplest and most obvious choice for a POSITA would be to connect the other terminal to ground (*i.e.*, 0V). EX1003, ¶¶311–314.

Pet. 77. Patent Owner does not present a contrary argument. Further, claim 15 recites: “a capacitor in which one terminal of the capacitor is coupled to the gate of the second transistor and a power supply voltage is applied to the other terminal of the capacitor.” Petitioner identifies a

capacitor in Kimura's Figure 33E, one terminal of which is connected to the gate of the second transistor, and the other terminal of which is connected to the V_{DD} power supply. *Id.* at 78. Patent Owner does not dispute this assertion.

Claim 15 differs from claim 7 in its recitation of the fourth and fifth transistors. According to claim 15, the fourth transistor includes "a gate to which a current light-emitting signal is applied," and the fifth transistor also includes "a gate to which the current light-emitting signal is applied." Ex. 1001, 10:60–67. These additional features of claim 15 are the same as those required by claim 13, which recites that the fourth transistor includes "a gate to which the current light-emitting signal is applied," and that the fifth transistor includes "a gate to which the current light-emitting signal is applied." *Id.* at 10:20–28. Petitioner relies on its reasoning for claim 13, discussed above, to account for these limitations of claim 15. Pet. 74–75.

Given Petitioner's reliance on the same analysis from claim 13, we find that the potential deficiencies discussed above for claim 13 apply equally to Petitioner's analysis for claim 15.

Claim 17 is substantially the same as claim 15, but recites in its preamble a plurality of data lines, a plurality of scan lines, and a plurality of power lines. Ex. 1001, 11:14–19. The body of claim 17 refers to power supply voltage from a data signal voltage from a data line and power supply voltage from a power line. *Id.* at 11:20–23, 12:6–7, 12:15–17.

Claim 17, like claim 15, recites that the fourth transistor includes "a gate to which a current light-emitting signal is applied," and that the fifth transistor includes "a gate to which the current light-emitting signal is applied." Ex. 1001, 12:4–11. These additional features of claim 17 are the

same as those required by claim 13, which recites that the fourth transistor includes “a gate to which the current light-emitting signal is applied,” and that the fifth transistor includes “a gate to which the current light-emitting signal is applied.” *Id.* at 10:20–28. Petitioner relies on its reasoning for claim 13, discussed above, to account for these limitations of claim 17. Pet. 74–75.

Given Petitioner’s reliance on the same analysis from claim 13, we find that the potential deficiencies discussed above for claim 13 apply equally to Petitioner’s analysis for claim 17.

8. *Dependent Claims 16 and 18*

Claim 16 depends from claim 15 and thus includes all limitations of claim 15. Ex. 1001, 11:8–13. Claim 18 depends from claim 17 and thus includes all limitations of claim 17. *Id.* at 12:18–24. Thus, the potential deficiencies discussed above for claims 15 and 17 apply equally to Petitioner’s analysis for claims 16 and 18, respectively.

Claim 16 also adds a transistor the source of which is coupled to one terminal of the capacitor and the drain of which receives an initialization voltage, with a gate to which a scan signal just before the current scan signal is applied. *Id.* at 11:8–13. Claim 18 adds the same. Petitioner accounts for the additional transistor of claims 16 and 18 by relying on the reasoning it provides for the sixth transistor added by claim 8 relative to claim 7. Pet. 78–79, 86. Thus, the potential deficiencies discussed above for claim 8 apply equally to Petitioner’s analysis for claims 16 and 18.

9. *Independent Claim 1*

Claim 1 is similar to claim 7, but differs in several respects. Although, like claim 7, claim 1 recites five different transistors, claim 1

refers to them as first, second, third, *fifth*, and *sixth* transistors, rather than first, second, third, *fourth*, and *fifth* transistors as in claim 7. Petitioner refers to the skipping of the designator “fourth” as an “unusual numbering scheme,” and as “an artifact from prosecution” where dependent claim 3 was rewritten into independent form. Pet. 11–12, 23. Specifically, application claim 1 had recited first, second, and third transistors, and application claim 3 depended from application claim 1 and further recited fifth and sixth transistors without reciting a fourth transistor. Ex. 1005, 415–416.

Because Petitioner regards the “fifth” and “sixth” identification of transistors simply as a numbering scheme without other significance, Petitioner performs its analysis as though “fifth” and “sixth” read the same as “fourth” and “fifth” in independent claim 7, and relies on the same reasoning as it presents for independent claim 7 to account for these differently named transistors of claim 1. Pet. 86–93. Patent Owner has not expressed disagreement with Petitioner’s approach, and does not present arguments additional to those it presents for claim 7.

On this record, we accept that the designators “first,” “second,” “third,” “fourth,” “fifth,” and “sixth” for the recited transistors in the claims merely identify particular transistors and do not, by themselves, set forth other requirements that need to be accounted for by Petitioner. *See 3M Innovative Properties Co. v. Avery Dennison Corporation*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (noting that the use of ordinals in a claim “is a common patent-law convention to distinguish between repeated instances of an element or limitation”).

Claim 1 requires both the “fifth transistor” and “sixth transistor” to activate “in response to” the “current light-emitting signal.” To account for

this requirement, Petitioner relies on the same reasoning it presents for essentially the same limitation in claim 13, that the fourth and fifth transistors each include “a gate to which the current light-emitting signal is applied.” Pet. 91. Thus, we find that the potential deficiencies discussed above for claim 13 apply equally to Petitioner’s analysis for claim 1.

10. Dependent Claims 2–6

Claims 2–6 each depend, directly or indirectly, from claim 1, and thus each include all of the limitations of claim 1. Ex. 1001, 9:8–34. The potential deficiencies discussed above for claim 1 apply equally to Petitioner’s analysis for claims 2–6. Claim 2 adds another transistor, “[an] initialization transistor for discharging the data signal voltage stored in the capacitor in response to a scan signal just before the current scan signal.” Ex. 1001, 9:8–12. It is the same limitation added by claim 8 relative to claim 7. *Id.* at 9:59–64. For claim 2, Petitioner relies on the same reasoning it provides to account for claim 8. Pet. 93. Thus, the potential deficiencies discussed above for claim 8 also apply equally to Petitioner’s analysis for claim 2.

D. Discretionary Denial Under 35 U.S.C. § 325(d)

Patent Owner contends that we should exercise discretion to deny institution under 35 U.S.C. § 325(d) based on the framework set forth in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential). Prelim. Resp. 2. In *Advanced Bionics*, the Board applied a two-part framework in considering whether to exercise discretion to deny institution under 35 U.S.C. § 325(d):

(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.

Advanced Bionics at 8 (footnote omitted).

Within this two-part framework, the Board considers a number of non-exclusive factors in evaluating whether to exercise its discretion under § 325(d). *See Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, first para.); *see also Advanced Bionics* at 9–11. The factors set forth in *Becton, Dickinson* are as follows:

(a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson at 17–18 (footnote omitted).

Becton, Dickinson factors (a), (b), and (d) relate to whether the art or arguments presented in the Petition are the same or substantially the same as those previously presented to the Office. *Advanced Bionics* at 10. Factors (c), (e), and (f) “relate to whether the petitioner has demonstrated a material error by the Office” in its prior consideration of that art or arguments. *Id.*

Only if the same or substantially the same art or arguments were previously presented to the Office do we then consider whether petitioner has demonstrated a material error by the Office. *Id.* “At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown.” *Id.* at 9.

Patent Owner asserts that “During prosecution, while the claims were still pending, Kimura’s Japanese counterpart (Japanese Publication No. 2003-202833, hereinafter “JP Kimura”) was submitted to the Patent Office—identified by the Applicants in numerous submissions—and was explicitly signed off on by the Examiner.” Prelim. Resp. 2–3.⁸

Petitioner clarifies, however, that “[w]hen the first Office Action issued allowing the claims, no version of Kimura (Japanese or English) was before the Office (and no English version was ever submitted). Prelim. Reply 1. Petitioner explains that despite previously submitting several information disclosure statements (hereinafter “IDS”), “the Applicant waited until eight days *after* the first Office Action allowing the claims to submit an IDS containing the *Japanese* language version of Kimura [JP Kimura] (which was among six other Japanese language references totaling almost 200 pages).” *Id.*

Petitioner notes that JP Kimura was identified to the Examiner four times only because “the Examiner repeatedly failed to consider the IDS, and had not done so when the Notice of Allowance issued.” *Id.* at 2. Petitioner further explains “it was not until the allowed application was sent for

⁸ The meaning of “Kimura’s Japanese counterpart” is unclear. We note that it is not either one of the two Japanese priority applications identified on the cover of Kimura.

printing that the IDS [citing JP Kimura] was acknowledged,” and that “[e]ven then, it was the Supervisory Patent Examiner (SPE)—not the original examiner H-Q. Ho)—that initialed the IDS.” *Id.*

In our view, the fact that the IDS citing JP Kimura was acknowledged by an examiner after issuance of the Office Action allowing the claims is inconsequential, so long as the acknowledgement still was prior to issuance of the '599 patent, which is the case here. Also, the fact that a Supervisory Patent Examiner signed the IDS is also inconsequential, particularly when the same Supervisory Patent Examiner earlier signed an Office Action rejecting a claim in the application, which is the case here. *See* Ex. 2001, 443–447 (Action dated 1/17/2008).

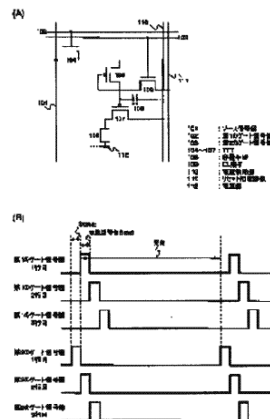
The real issue here concerns the fact that JP Kimura is in Japanese language and it appears that no English translation of the full document was ever provided to the Examiner. Patent Owner notes that “the applicants submitted an English abstract of JP Kimura reference.” Prelim. Resp. 6. The referenced abstract is a publication titled “PATENT ABSTRACTS OF JAPAN.” Ex. 2001, 279–280. An image of its entire substantive disclosure is reproduced below:

(54) SEMICONDUCTOR DEVICE AND DRIVING METHOD THEREFOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a light emitting device using a semiconductor device as a pixel capable of correcting dispersion of threshold voltages of TFTs by a configuration not influenced by dispersion of capacitance values.

SOLUTION: As for a video signal inputted to a pixel from a source signal line, a desired potential is applied to the gate electrode of a TFT 107 for supplying a current to an EL element 109 via a TFT 105 connected across the gate and drain. Across the source and drain of the TFT 105, a voltage equal to the threshold value of the TFT is generated. Therefore, a potential offsetting the video signal by the threshold value of the TFT 105 is applied to the gate electrode of TFT 107. Moreover, the TFTs in the pixel are arranged close to each other, so that dispersion in the characteristic is hardly caused. Thus, even if the threshold value of TFT 107 is dispersed pixel by pixel, the dispersion is offset by the threshold value of TFT 105 and a desired drain current can be fed to the EL element 109.



Id. at 279. The image includes one paragraph on the problem to be solved and one paragraph on the solution, and two figures, all appearing on a single page with the caption “SEMICONDUCTOR DEVICE AND DRIVING METHOD THEREFOR.”

In contrast, Kimura is a forty-page published U.S. Patent Application with seven hundred and twenty-two numbered paragraphs and forty-four figures many of which include multiple sub-figures. Ex. 1002. Despite the fact that the figures of JP Kimura appear to be the same as the figures in Kimura, we find that the quality of the substantive disclosures to the Office of JP Kimura in Japanese, together with the English abstract noted above, are not the same as the version of Kimura asserted in this case.⁹ We are not persuaded that the two would convey a substantially equal understanding of the disclosures.

For the foregoing reasons, we find that Kimura was not previously considered by the Office, as Patent Owner contends.

Patent Owner further argues that Kimura is cumulative to two prior art references other than JP Kimura that were cited by the Examiner in an Office Action dated July 12, 2007, i.e., U.S. Patent App. Pub. No. 2004/0041750 (Ex. 2002, “Abe”), and U.S. patent App. Pub. No. 2004/0145547 (Ex. 2003, “Oh”). Prelim. Resp. 7–8 (citing Ex. 1005, 288–289, 300). According to Patent Owner, each of Abe and Oh discloses a pixel circuit including at least five transistors. *Id.* at 8.

⁹ As one example, the Petition cites to portions of Kimura which explains that for transistors used as switching transistors, either polarity type, nMOS or pMOS, are suitable. Pet. 20 (citing Ex. 1002 ¶¶ 362, 396). That is not conveyed by either JP Kimura or the English abstract noted above.

We agree with Petitioner, however, that Abe's and Oh's disclosure of a pixel circuit including use of five transistors does not make Kimura cumulative with respect to either Abe or Oh. Prelim Reply 3. There are numerous other claim limitations beyond merely a pixel circuit including five or at least five transistors. Patent Owner does not persuade us that with respect to those limitations Kimura is cumulative to either Abe and Oh. For example, as Petitioner further explains:

The Examiner expressly stated why original claim 3 (issued claim 1) was allowable: the prior art (including Abe and Oh) lacked “a fifth transistor for providing a power supply voltage for the second transistor **in response to a current light-emitting signal**; and a sixth transistor for providing a driving current for the electroluminescent element through the second transistor in response to **the current light-emitting signal**.” Ex2001, 185 (emphasis added); *see also id.* (similar for original claim 8 (issued claim 7)). In other words, Abe and Oh lack a **shared light-emitting signal** that controlled the claimed transistors. Indeed, Patent Owner does not even try to identify the transistors in Abe or Oh that would need to share a light-emitting signal. By contrast, *Kimura* teaches the ***shared light-emitting signal*** that the prior art of record lacked. *See, e.g.,* Petition at 64–65.

Prelim. Reply 3–4.

Patent Owner argues that, in the Preliminary Reply, Petitioner presents new theories as to why Kimura is not cumulative to prior art which had been considered, i.e., the shared light-emitting signal that controls two transistors such as the fifth and sixth transistor in claim 1. Prelim. Sur-Reply 1. Patent Owner notes that in the Petition, when discussing 35 U.S.C. § 325(d), Petitioner only stated that the prior art of record had not taught a “five transistor” pixel circuit, which is incorrect. *Id.*; *see also id.* at 3.

Patent Owner asserts that the Board is within its discretion to disregard these new arguments in the Preliminary Reply. *Id.* at 1.

We do not find that Petitioner is precluded from adding reasoning in its Preliminary Reply as to why Kimura is not cumulative with respect to the prior art references already of record. It is Patent Owner who is requesting that we exercise our discretion under 35 U.S.C. § 325(d) to deny the Petition. As such, we decline to disregard the reasoning presented in the Preliminary Reply. We further note that Patent Owner has suffered no prejudice, as Patent Owner has, in the Preliminary Sur-Reply, substantively responded to the reasoning raised in Petitioner's Preliminary Reply.

For the foregoing reasons, we find that the same or substantially the same prior art was not presented previously to the Office. Accordingly, we need not proceed past the first stage of the *Advanced Bionics* framework with respect to Kimura. Thus, we decline to exercise our discretion under 35 U.S.C. § 325(d) to deny the Petition.

IV. CONCLUSION

For the foregoing reasons, we conclude that the information presented in the Petition and Preliminary Response establishes a reasonable likelihood that Petitioner would prevail in showing that at least one of claims 1–18 of the '599 patent is unpatentable.

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that *inter partes* review of all challenged claims, i.e., claims 1–18 of the '599 patent, is hereby instituted on all grounds stated in the Petition; and

IPR2023-00941
Patent 7,414,599 B2

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

IPR2023-00941
Patent 7,414,599 B2

For Petitioner:

Travis Jensen
David Daybell
Xiang Wang
ORRICK, HERRINGTON & SUTCLIFFE, LLP
T61PTABDocket@orrick.com
D2DPTABDocket@orrick.com
XW0PTABDocket@orrick.com

For Patent Owner:

David A. Garr
Scott C. Weidenfeller
Covington & Burling LLP
dgarr@cov.com
sweidenfeller@cov.com