

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; WUHAN
CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO. LTD.; AND
VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case No. IPR2023-00941
U.S. Patent No. 7,414,599

**PETITIONER’S MOTION TO SUBMIT SUPPLEMENTAL
INFORMATION PURSUANT TO 37 C.F.R. § 42.123(a)**

UPDATED LISTING OF EXHIBITS

Exhibit	Description
EX1001	U.S. Pat. 7,414,599 (Chung)
EX1002	U.S. Pat. Pub. 2003/0132931 (Kimura)
EX1003	Expert Declaration of Dr. Daniel Foty
EX1004	U.S. Pat. 6,362,798 (Kimura '798)
EX1005	File History for U.S. Pat. 7,414,599
EX1006	U.S. Pat. Pub. 2001/0022565
EX1007	U.S. Pat. Pub. 2003/0030603
EX1008	Excerpts from <i>Analog Integrated Circuit Design</i> , David A. Johns et al., John Wiley & Sons, Inc., 1997.
EX1009	<i>Modeling and Simulation of Insulated-Gate Field-Effect Transistor Switching Circuits</i> , Harold Shichman et al., IEEE Journal of Solid-State Circuits, Vol. SC-3, No. 3, September 1968.
EX1010	Excerpts from <i>Physics and Technology of Semiconductor Devices</i> , A. Grove, John Wiley & Sons, 1967.
EX1011	Excerpts from <i>CMOS Digital Integrated Circuits: Analysis and Design</i> , (third edition), S. Kang et al., McGraw-Hill, 2003.
EX1012	U.S. Pat. 6,229,506 ("Dawson")
EX1013	U.S. Pat. 5,666,046
EX1014	<i>TFT AMOLED Pixel Circuits and Driving Methods</i> , J. Stanford, SID 03 Digest, pp. 10-13 (2003))
EX1015	<i>A New Pixel Circuit for Active Matrix Organic Light Emitting Diodes</i> , J. Goh, IEEE Electron Device Letters vol. 23, pp. 544-546 (2002)

Exhibit	Description
EX1016	<i>A Novel Pixel Circuit for Active-Matrix Organic Light-Emitting Diodes</i> , J. Goh et al., SID 03 Digest, pp. 494-497 (2003)
EX1017	<i>Current-Writing Active-Matrix Circuit for Organic Light-Emitting Diode Display Using a-Si:H Thin-Film-Transistors</i> , R. Hattori et al., IEICE Transactions on Electronics vol. E83-C, pp. 779 – 782 (2000).
EX1018	Declaration of T. Credelle
EX1019	Supplemental Expert Declaration of Dr. Daniel Foty
EX1020	U.S. Pat. Pub. 2004/0056257 (Sakamoto)
EX1021	U.S. Pat. Pub. 2003/0067424 (Akimoto)

Pursuant to 37 C.F.R §42.123(a), and as authorized by the Board (via email on January 18, 2024), Petitioner moves to submit three items of supplemental information: (1) EX1019 (supplemental declaration of Dr. Foty); (2) EX1020 (U.S. Pub. 2004/0056257, “Sakamoto”); and (3) EX1021 (U.S. Pub. 2003/0067424, “Akimoto”). Collectively, these items address three topics raised in the Institution Decision (Paper 12, “ID”), including two where the Board invited “further develop[ment]”: (1) obviousness of a shared light-emitting signal in Kimura Fig. 36 (ID, 51-52); (2) operation of Kimura’s “initialization transistor” (*id.*, 47-49); and (3) Petitioner’s “second theory” re using all PMOS transistors (*id.*, 31-32).

Petitioner’s motion should be granted because it meets both requirements of §42.123(a). First, Petitioner timely requested authorization to file this motion within one month of the ID. Second, as explained further below, Dr. Foty’s supplemental declaration (and the Akimoto and Sakamoto references discussed therein) are relevant to a claim for which trial has been instituted.

While the Board suggested during the parties’ conference call that supplemental information was “atypical,” Petitioner submits that the Board often allows supplemental information under similar circumstances. *See, e.g., MED-EL Elektromedizinische Geraete GmbH v. Advanced Bionics AG*, IPR2020-00190, Paper 24 (PTAB Aug. 10, 2022); *Apple Inc. v. Telefonaktiebolaget LM Ericsson*, IPR2022-00343, Paper 14 (PTAB Nov. 10, 2022); *Frameless Hardware Company*,

LLC v. CR Laurence Co., Inc., IPR2022- 00356, Paper 29 (PTAB Oct. 25, 2022).

As the Federal Circuit has stated, “[t]he introduction of new evidence in the course of the PTAB trial is to be expected in [IPR] proceedings and, as long as the opposing party is given notice of the evidence and an opportunity to respond to it, the introduction of such evidence is perfectly permissible under the APA.”

Telefonaktiebolaget LM Ericsson v. TCL Corp., 941 F.3d 1341, 1345-46 (Fed. Cir. 2019) (internal citation omitted); *see also id.* (allowing supplemental declaration).

I. APPLICABLE STANDARD

A motion to submit supplemental information under Rule 42.123(a) requires (1) requesting authorization to file the motion within one month of institution, and (2) that the information is relevant to an instituted claim. Both requirements are easily met as discussed below. Unlike Rule 123(b), Rule 123(a) does not require “show[ing] why the supplemental information reasonably could not have been obtained earlier.” Rule 42.123(b); *see also, e.g., MED-EL*, Paper 24 at 4-5; *Apple, Inc. v. Uniloc 2017 LLC*, IPR2019-00251, Paper 23 at 6 (PTAB July 20, 2020).

II. DISCUSSION

The ID issued December 15, 2023 (*see* Paper 12) and Petitioner requested authorization for this motion on January 11, 2024, within one month of institution. PO has yet to notice Dr. Foty’s deposition and can examine him on his original and supplemental declarations in a single deposition. PO’s Response is due March 8,

2024 (Paper 13 at 12)—more than six weeks away—which is ample time for PO to respond. No deadlines are affected and the supplemental information will not adversely affect the Board’s ability to timely and efficiently complete the IPR.

On the call with the Board, PO expressed concern Petitioner might introduce new grounds. That is not the case. As can be seen from Dr. Foty’s supplemental declaration (*see* ¶¶23-24, 57-59), Sakamoto and Akimoto are used for limited purposes and do not introduce new combinations. Indeed, Petitioner provides no motivation to combine for either reference. The issues on which Dr. Foty now opines address positions taken in the Petition and his original declaration. *See, e.g.*, EX1003, ¶¶141-142 (applicability of Kimura Fig. 16B timing diagram), 155-158 and 215-230 (applying Kimura Figs. 16/17 reset transistor to Figs. 33/36), 251-260 (obviousness of shared “light emitting signal”), 58 (discussing all-PMOS pixel circuit); Petition, 4 and 18-23 (all-PMOS pixel), 49-56 (initialization transistor), 62-67 (shared light-emitting signal). Thus, the grounds remain the same. This motion satisfies the timing, notice, and efficiency requirements, and Petitioner turns to the relevance requirement, which is also readily satisfied.

A. Shared Light Emitting Signal

Dependent claim 13 (and independent claims 14, 15, and 17) all include a requirement that the gate terminals of the claimed “fourth” and “fifth” transistors are controlled by the same “light emitting signal” (*i.e.*, a “shared” light emitting

signal). *See, e.g.*, Petition, 63-67. Petitioner argued that Kimura Fig. 36 rendered this limitation obvious because in Fig. 36 “the fourth and fifth transistors are always ON/OFF together,” and thus a POSITA would be motivated to use a shared signal to, *e.g.*, “reduc[e] the number of control lines.” *Id.* The Board agreed (*Id.*, 51), but was concerned about a “potential discrepancy” (*id.*, 52) that such an approach would have on the operation of Kimura Fig. 33. In particular, the Board stated that “[a]t this stage, Petitioner has not shown sufficiently that operations that used to be governed by a particular output from the fourth or fifth transistor in Figure 33 would continue to operate the same as they used to operate, when the output provided from the fourth or fifth transistor is different [in Fig. 36].” *Id.*, 52. The Board suggested “further develop[ing] the issue subsequent to institution.” *Id.*

Petitioner seeks to submit Dr. Foty’s supplemental declaration (EX1019) to address the Board’s concern and elaborate how and why the operation of Fig. 36 is congruent in all material respects with Fig. 33, including vis-à-vis the claimed shared light-emitting signal requirement. *See* EX1019, ¶¶7-24. Dr. Foty’s supplemental declaration provides a comparison of each operational phase (*viz.*, initialization/reset, programming, and light emission) of Kimura Figs. 33 and 36 to show compatibility. *See id.*, ¶¶19-22. In particular, Dr. Foty demonstrates that the arrangement and connections of all transistors in Fig. 33 remain unchanged in Fig. 36, and that Fig. 36 expressly teaches the precise changes necessary to utilize a

shared emitting signal. *Id.*, ¶¶9-22.

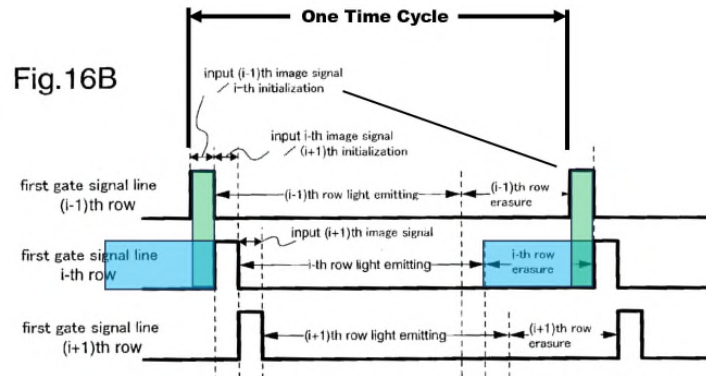
To the extent Fig. 36 has “architecture differences” (ID, 52) of significance, Petitioner submits Sakamoto to show suitability and use of a shared light emitting signal in a variety of pixel configurations, demonstrating a high likelihood of success and POSITA knowledge. *See, e.g.*, EX1020, Fig. 5B (shared light emitting signal controls transistors Tr2 and Tr4 in pixel circuit), [0169] (“transistors Tr2 and Tr4 are connected to the second scanline”); EX1019, ¶¶23-24. The relevance requirement of §42.123(a)(2) is thus met.

B. Initialization/Reset Transistor

Claims 2, 8, 16, and 18 require an “initialization transistor” for “discharging” (*i.e.*, resetting) the voltage stored on the capacitor prior to programming. Petitioner applies Kimura’s transistor 1607 (in Figs. 16/17) to the pixel circuit of Kimura Figs. 33/36 as the claimed “initialization transistor.” *See* Petition, 51-56. Petitioner explained how the timing diagram of Kimura Fig. 16B for the initialization/reset operation “would directly apply to the modified embodiment” of Kimura Figs. 33/36. EX1003, ¶142 (figure correlating “initialization period” in ’599 patent timing diagram to “initialization” period in Kimura Fig. 16B); *see also* Petition, 16, 55-56.

Patent Owner asserted that “Petitioner Conflates ‘Initialization’ with ‘Erasure’” (ID at 47 (citing POPR at 16)), which led to some confusion (ID at 47-

49). The Board observed that “Patent Owner highlighted the initialization period [of Kimura Fig. 16B] in green and the erasure period in blue, and the two do not overlap.” *Id.*, 49. PO’s assertion (embraced by the Board) is based on incomplete labelling of Fig. 16B and is plainly incorrect when Kimura Fig. 16B is properly understood, as it would be by a POSITA. EX1019, ¶¶25-45. Indeed, there is a simple explanation that readily resolves the apparent confusion—the initialization phase repeats itself every time the first gate line signal pulses. EX1019, ¶¶27-36. Dr. Foty explains annotated Fig. 16B below, which plainly shows that the initialization period (green) overlaps (and is contained within) with the erasure period (blue), which explains operation of the initialization transistor. *Id.*



The relevance requirement of §42.123(a)(2) is thus met.

C. All-PMOS Implementation

Numerous claims require PMOS transistors. *See, e.g.*, claims 3-5, 9-11, and 13. The Petition relies on modified “all-PMOS” implementations of Kimura Figs. 33/36 to meet the “PMOS transistor” requirements. *See, e.g.*, Petition, 19-23.

Petitioner presented multiple rationales for using all-PMOS implementations. *Id.* Although the Board found Petitioner’s “general interchangeability” rationale “sufficiently persuasive” for institution (ID, 23), the Board “question[ed] the completeness” of Petitioner’s second rationale dealing with manufacturing aspects of an all-PMOS pixel (*id.*, 31-32). The Board was “not persuaded by Petitioner’s second theory” and suggested the parties “further develop this issue.” *Id.*, 32.

Petitioner seeks to submit Dr. Foty’s Supplemental Declaration (EX1019) to address the Board’s concern about how and why manufacturing an all-PMOS pixel would be not only feasible, but also desirable, even when controlled by peripheral CMOS circuitry. *See* EX1019, ¶¶46-59 (Kimura’s disclosure not limited to CMOS process; and explaining the benefits/desirability of PMOS-only *pixel circuit* made with CMOS process). Petitioner submits Akimoto to demonstrate a POSITA’s knowledge in this regard. For example, Akimoto explains that “since the pixel 40 is composed of only [PMOS] transistors, the layout of the pixel unit is simplified so as to achieve a high definition and high yield.” EX1021, [0062]. Akimoto identifies *additional* manufacturing advantages (*e.g.*, reduced “production cost”) where “peripheral circuits [*viz.*, external drivers] are made up with [only PMOS transistors.” *Id.* The relevance requirement of §42.123(a)(2) is thus met.

III. CONCLUSION

The Board should allow Petitioner’s supplemental information into evidence.

Dated: January 23, 2024

Respectfully submitted,

/Travis Jensen/

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CERTIFICATE OF SERVICE

The undersigned certifies that on January 23, 2024, a copy of the following was served in its entirety via electronic mail, upon the following attorneys of record for the Patent Owner:

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