

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; TCL
CHINA STAR OPTOELECTRONICS TECHNOLOGY CO., LTD.; TIANMA
MICROELECTRONICS CO. LTD.; AND VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

U.S. Patent No. 7,414,599

Inter Partes Review No. IPR2023-00941

SUPPLEMENTAL DECLARATION OF DR. DANIEL FOTY

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I. INTRODUCTION

1. I have been retained by counsel for Mianyang BOE Optoelectronics Technology Group Co., Ltd. (“BOE” or “Petitioner”) in the above-captioned matter as an independent consultant to offer opinions regarding the patentability of the claims in U.S. Patent No. 7,414,599 (“the ‘599 patent” or “the challenged patent”).

2. In my Original Declaration (EX1003), I analyzed and provided examples of how Kimura, combined with the knowledge of a POSITA, rendered obvious the Challenged Claims (*i.e.*, claims 1-18) of the ‘599 patent.

3. In view of the Institution Decision (Paper 12) rendered by the Board in this IPR proceeding, I have since been asked to provide a supplemental analysis to further explain certain aspects of Kimura and the knowledge of a POSITA as it relates to three specific issues. In particular, I was asked to address the following three items: (1) how the use of a shared light-emitting signal to control the fourth and fifth transistors would affect the configuration and operation of Kimura Figs. 33/36; (2) the relationship between “erasure” and “initialization” in the timing diagram of Kimura Fig. 16B as it relates to the reset/initialization transistor added to Figs. 33/36; and (3) the manufacturing and design benefits of using an all-pMOS implementation for Kimura’s pixel circuit in Figs. 33/36.

4. My supplemental analysis here is based on my years of education, research, and experience, as well as my investigation and study of relevant materials,

including those cited herein. I may rely upon these materials, my knowledge and experience, and/or additional materials (including materials cited and relied upon in my original declaration) to address any statements or issues subsequently raised in this proceeding. Further, I may also consider additional documents and information in forming any necessary opinions - including documents that may not yet have been provided to me.

5. The combination of my Original Declaration and this Supplemental Declaration represents only those opinions that I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein – based on any new information and on my continuing analysis of the materials provided.

6. For information regarding my background and qualifications, compensation, and the legal standards at issue, please refer to §§II, III, and V of my Original Declaration (EX1003), which is incorporated by reference herein. For a summary of the '599 patent, please refer to §VIII of my Original Declaration, (again, incorporated by reference herein). Note that as this analysis is supplemental, I have hereby incorporated the analysis of my Original Declaration in full.

II. THE SHARED LIGHT-EMITTING SIGNAL IN KIMURA FIGS. 33/36

7. Dependent claim 13 requires that the gate terminals of the “fourth” and “fifth” transistors are controlled by a shared “light-emitting signal.” Independent claims 1, 14, 15, and 17 include the same requirement (except that claim 1 uses

different transistor numbering). I analyzed this limitation for claim 13 in my Original Declaration at ¶¶255-259. *See also id.*, ¶¶283-288 (for claim 14), 304-310 (for claim 15), 341-348 (for claim 17), and 378-391 (for claim 1). In summary, as I stated in my Original Declaration, Kimura Fig. 33 does **not** show the fourth and fifth transistors being controlled by a shared light-emitting signal. EX1003, ¶257 (discussing that in Fig. 33B, “the fourth transistor is ‘OFF’ while the fifth transistor ‘ON’.”). However, Kimura Fig. 36 renders obvious a shared light-emitting signal because the fourth and fifth transistors are **always** “ON”/“OFF” together in every operational phase (*i.e.*, “Figure 36B (initialization), Figures 36C and 36D (programming), and Figure 36E (light emission)”). *Id.* Thus, “a POSITA would have been motivated to use a shared light-emitting signal to control them” because, *e.g.*, Kimura itself teaches doing so to “reduc[e] the number of control lines.” *Id.*, ¶258 (citing Kimura, [0429], [0421]-[0422]).

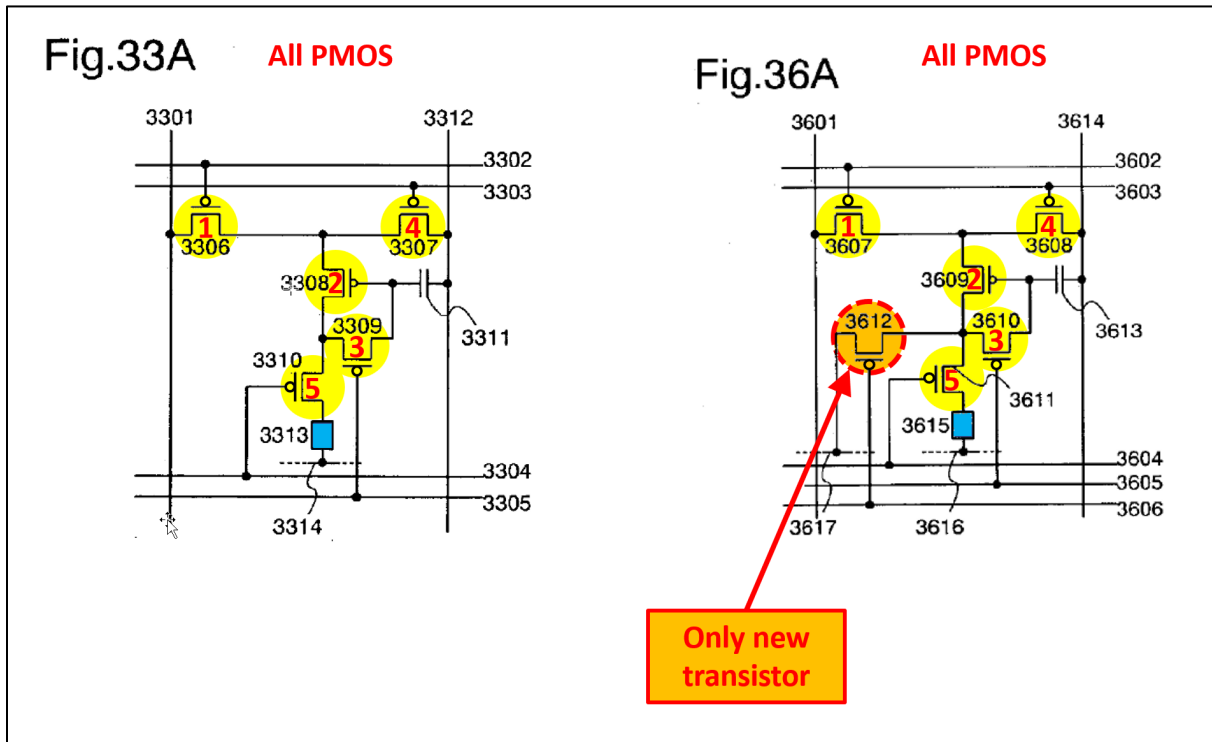
8. The Board agreed that “if the fourth and fifth transistors are always turned on and off together, as Petitioner asserts is the case for the embodiment of Figures 36A–36E, there is reason for one of ordinary skill in the art to drive the fourth and fifth transistors by the same control signal, *i.e.*, reducing the number of control lines and improving aperture ratio.” *See* Institution Decision at 51. However, the Board was concerned about a “potential discrepancy” as to how the addition/presence of a sixth transistor in the pixel circuit of Fig. 36 (and use of a

shared light emitting signal) would affect the operation of Fig. 33. *Id.*, 52. In this Supplemental Declaration I was asked to explain the similarities and differences in the structure and operation of Kimura's pixel circuits in Figs. 33 and 36 vis-à-vis their mapping to the first, second, third, fourth, and fifth transistors recited in claim 7 of the '599 patent.

9. The most important thing to note is that Kimura teaches that Fig. 36 is merely an extension of Fig. 33, and almost everything is the same in both embodiments. The reason my Original Declaration did not repeat all of my Fig. 33 analysis for Fig. 36 is because (as just mentioned) these two embodiments (as depicted in these two figures) are identical in most respects. Rather, I "note[d] at the outset that Kimura Figure 36 is just an extension of Kimura Figure 33, and that (unless noted) the analysis and discussion of one figure applies equally to the other throughout this Declaration." Original Declaration, ¶ 130; see also Petition, fn. 3. Kimura itself similarly adopts the disclosure of Fig. 33 as applying to Fig. 36 and merely describes the differences in Fig. 36.

10. The only difference between the embodiment of Figure 33 and the embodiment of Figure 36 is the addition of transistor 3612 to the Figure 33 embodiment (thus creating the embodiment of Figure 36) – which allows transistor 3611 (in Fig. 36) to always share a common operation state with transistor 3608, which in turn allows transistors 3611 and 3608 (which are the fourth and fifth

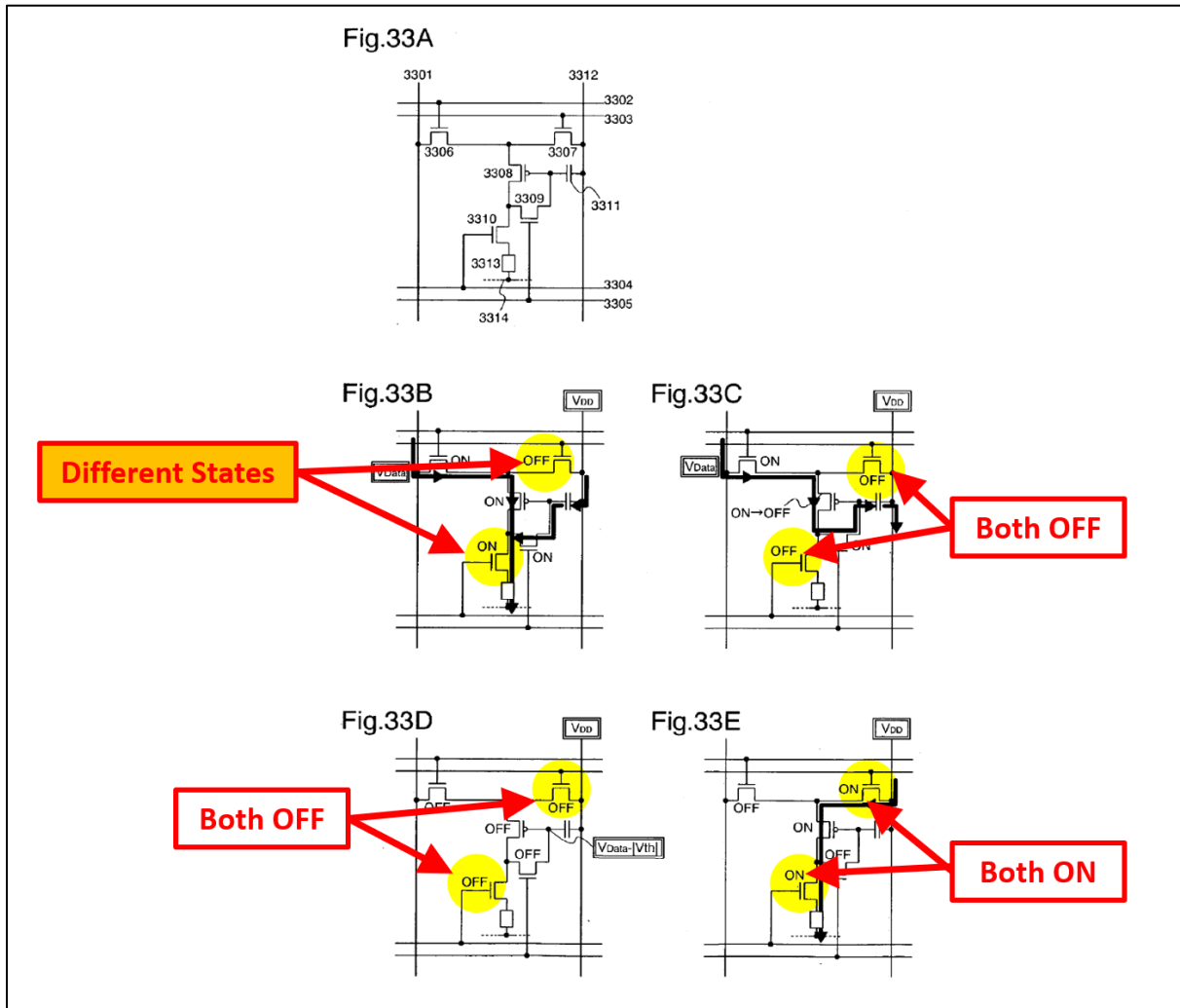
transistors in claim 7) to use a shared light emitting signal. In fact, it is precisely this slight change in Fig. 36 that enables use of a shared light emitting signal. Moreover, all of the '599 claims are “comprising” claims – and thus do not preclude the use/presence of an additional transistor in the pixel circuit.



11. To provide a more-detailed explanation here, I map and compare each operational phase in Figs. 33B, 33C, 33D, and 33E to its respective counterpart in Figs. 36B, 36C, 36D, and 36E to explain the role of transistor 3612 and how/why it allows the transistor 3611 to be “OFF” in Fig. 36B instead of “ON” (as is the case for transistor 3310) in Fig. 33B.

12. Examination of Figure 33 of Kimura shows that there is only one operational phase (Fig. 33B) where the fourth transistor (3608) and the fifth

transistor (3611) are *not* operated with the same gate signal (OFF or ON) on the gate electrode of both transistors at the same time.

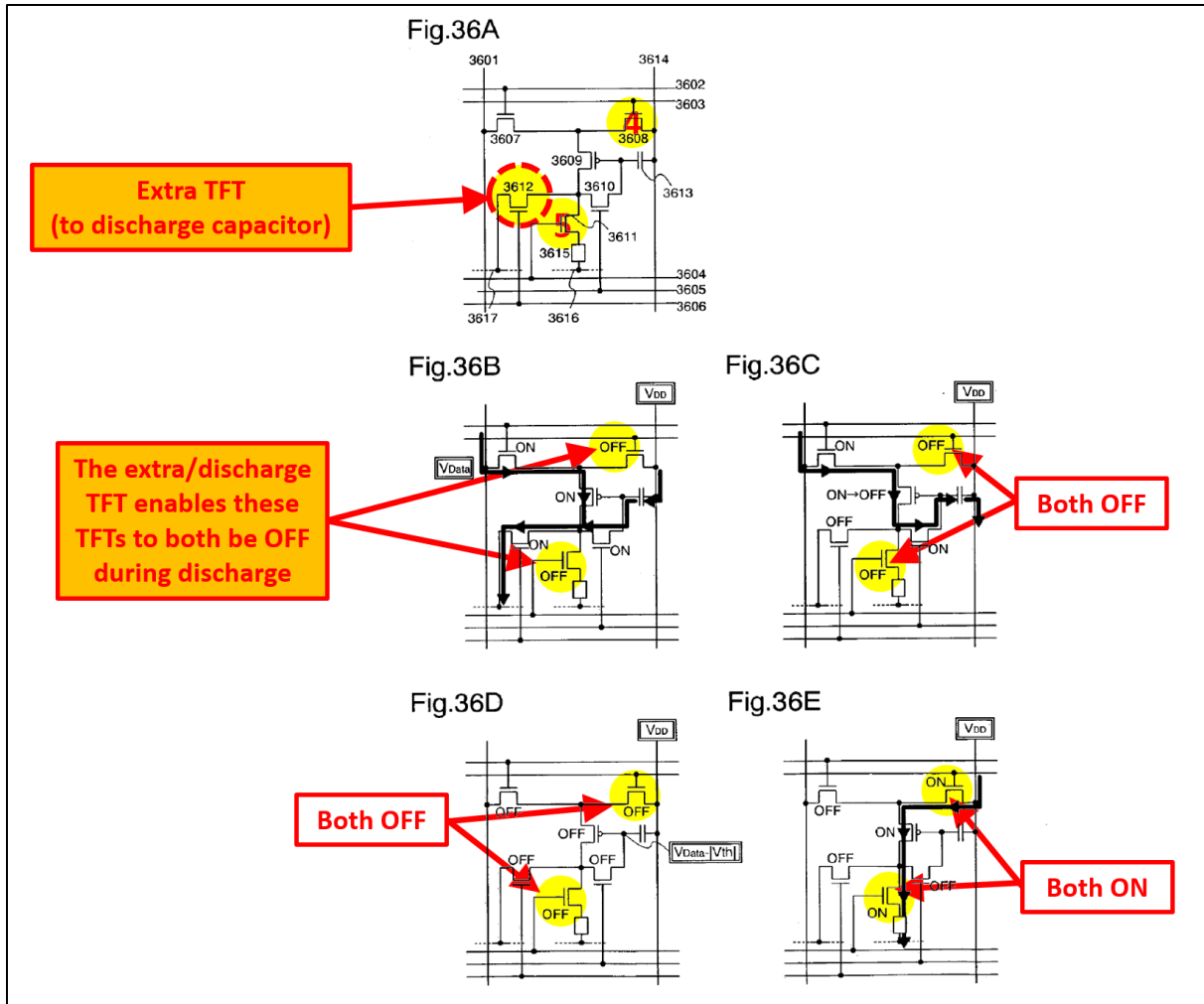


13. As can be seen, the only such instance occurs in the operational phase depicted in Figure 33B. Regardless of what one calls this phase (e.g., “initialization,” “erasure,” or “reset”), this is where the charge (voltage) on the programming capacitor is being drained off, in preparation for the next programming phase. As Kimura explains (and as was also explained in my Original Declaration), this occurs because the fifth transistor (3310) in Figure 33 is tasked with doing two

separate jobs – it is turned on during the light emitting phase (Figure 33E) as part of the current path which directs the appropriate current through the emitting device (3313) (in which case it is on together with the fourth transistor), but is *also turned on separately* (Figure 33B) to provide a path for the charge flowing off the programming capacitor in preparation for programming.

14. As I explained in my earlier declaration, Kimura discusses this situation – noting that passing the capacitor-discharge current through the light emitter will cause a small-and-brief but potentially disruptive (to image quality) emission of light from the light emitter; in this embodiment, this is the price that is paid for having circuitry with one less transistor (which saves space and simplifies the wiring).

15. As I also explained in my earlier declaration, Kimura's Figure 36 embodiment is based upon the embodiment of Figure 33 – but provides the alternative version of the circuitry, in which another transistor is included for the purpose of providing a discharge path for the charge being drained off the programming capacitor (*i.e.*, to initialize/reset it).



16. At the “cost” of one additional transistor in the circuitry, this discharge path does *not* go through the light emitter – and the undesirable “extra” light emission that occurs during this phase in the Figure 33 embodiment is eliminated in Figure 36 (as per Kimura’s explanation as cited in my original declaration).

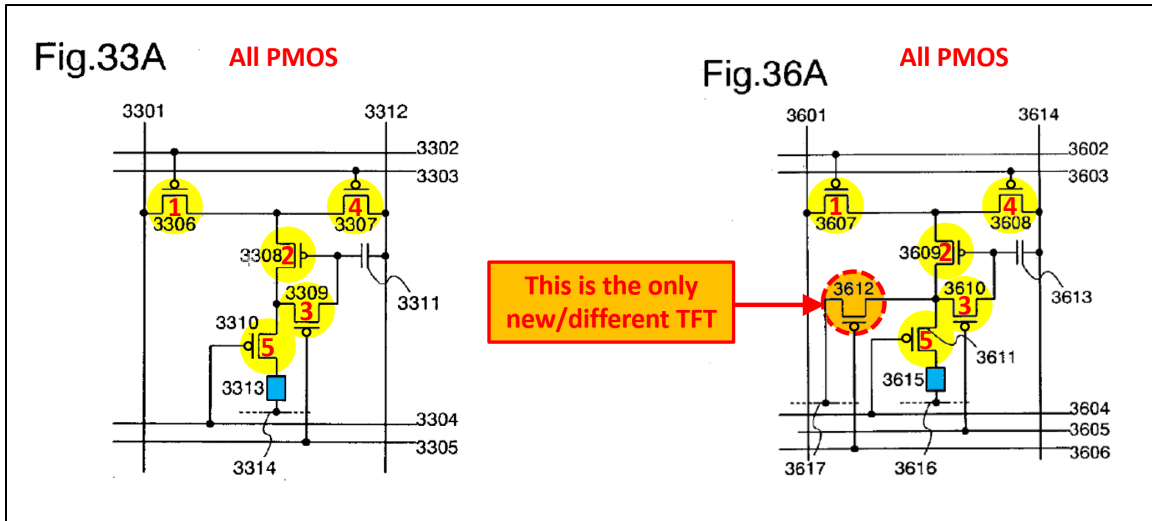
17. In Figure 36, the fifth transistor (3611) is not tasked with performing two jobs (as was the situation for the fifth transistor of the Figure 33 embodiment). With only one job to do, the ON/OFF state of the fifth transistor will always match that of the fourth transistor (3608). As a result of this synchronized operation of the

fourth transistor and the fifth transistor, a POSITA would be motivated to use one control line for the gates of these two transistors – rather than two lines, with one each going to the gate electrode of each transistor; as I noted in my earlier declaration, using shared signal lines is taught in Kimura (at 421-422 and particularly at 429 – “The number of signal lines can be kept to a minimum and a high aperture ration [sic] can be obtained by using this type of structure...”).

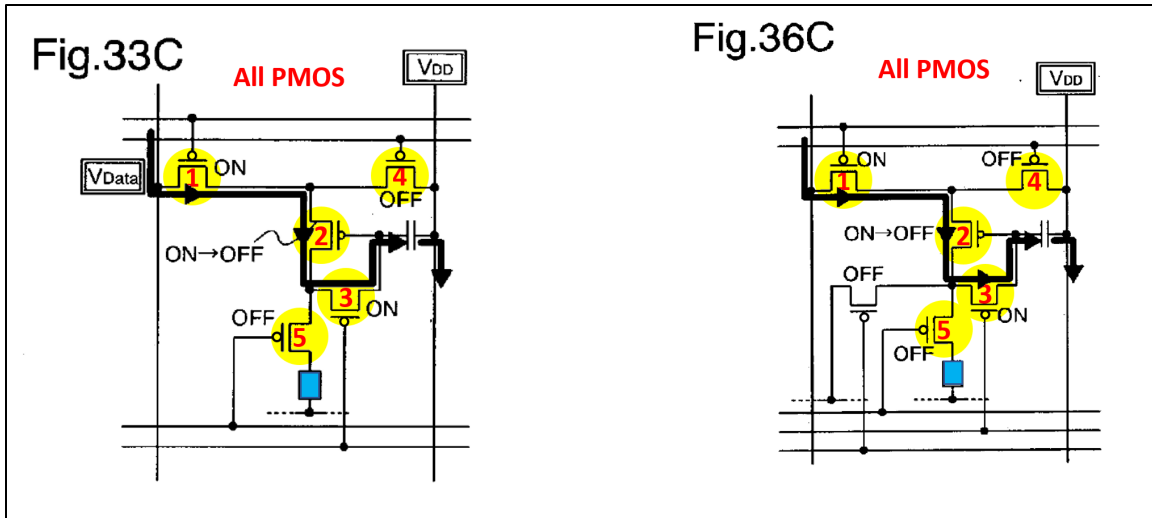
18. In my earlier declaration, I did not rely on the embodiment of Figure 33 to demonstrate the teaching of a shared light emitting signal in Kimura – but rather was relying on the embodiment of Figure 36 for this purpose. As just explained, these two embodiments are nearly identical – with one modification made to the Figure 33 embodiment to create the embodiment of Figure 36, and with that modification being done for a particular and well-explained (by Kimura) reason. As just explained, the shared light emitting signal is found using the Figure 36 embodiment and other teachings of Kimura.

19. The Board questioned “whether the Figure 33 embodiment, after being modified to make the fourth and fifth transistor always turn on and off together, as Petitioner proposes based on the Figure 36 embodiment, would still meet all the requirements of the first, second, third, fourth, and fifth transistor, as recited in claim 7.” Institution Decision at 51-52. The answer to that question is “yes” - the first through fifth transistors still meet all the requirements of claim 7. As shown below,

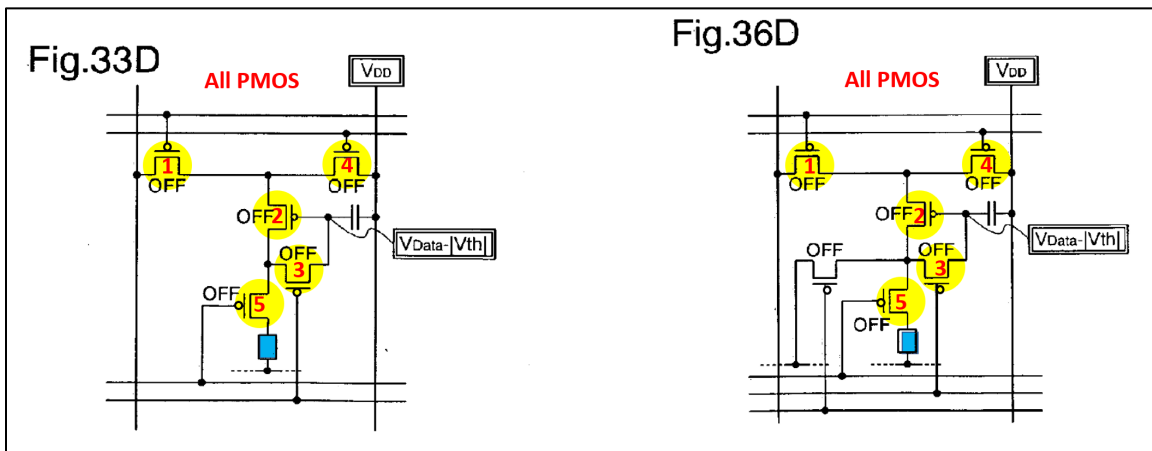
everything in Figure 36 continues to operate in the same manner as is the case in Figure 33 - except as explained above with respect to the extra transistor 3612 (which discharges the capacitor) and transistor 3611 (which is present in the same location and operates in the same way during the light-emitting phase, but no longer carries the added task of discharging the capacitor). Modifying Figures 33 and 36 to both use all-pMOS TFTs does not change the fact that they continue to operate identically (except for the differences already noted).



20. I have already explained the structural and operational differences between Figures 33B and 36B. As can be seen in the side-by-side comparison below (for the programming operation in Figures 33C and 36C), transistors one, two, three, four, and five operate identically.

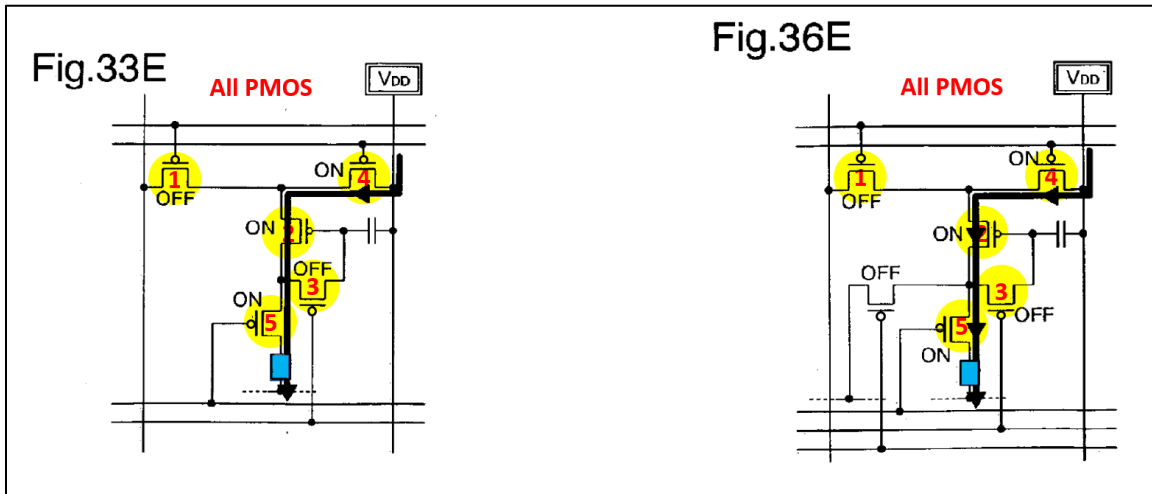


21. As illustrated below, the same is true for Figures 33D and 36D (*i.e.*, identical operation of transistors one through five); these (annotated) figures show that the results of the programming operation in each figure are the same (*i.e.*, the same voltage $V_{\text{Data}} - |V_{\text{th}}|$ has been stored on the capacitor in each case).

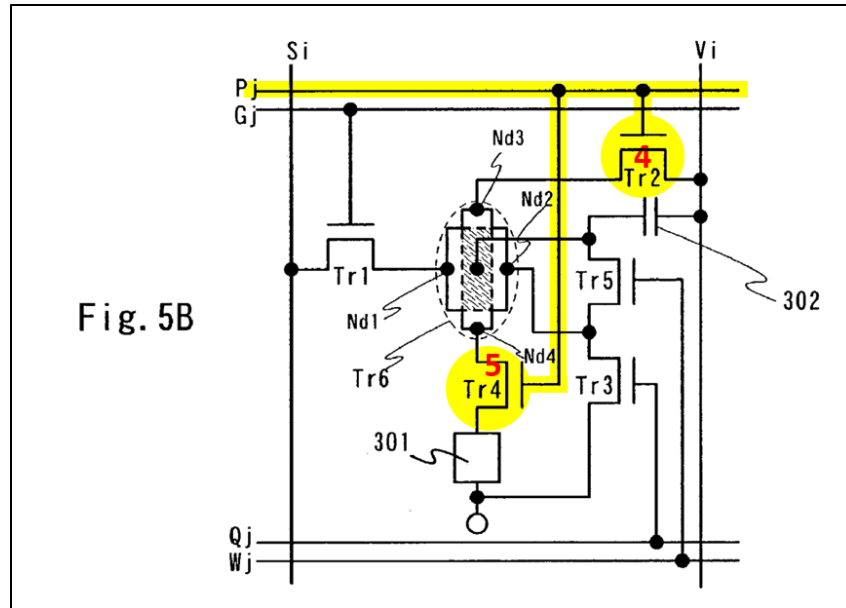


22. Likewise, the side-by-side comparison below shows that transistors one, two, three, four, and five behave identically (*i.e.*, if a given transistor is ON in Figure 33E, it is ON in Figure 36E – and vice versa) during the light emitting phase in Figures 33E and 36E. Again, the only difference is the presence of the additional

discharge transistor in Fig. 36E; however, this addition does not alter the operational behavior of any of the other transistors.



23. Subsequent to the filing of my original declaration, another germane prior art reference came to my attention – Sakamoto (EX1020, U.S. Pat. Pub. 2004/0056257). Sakamoto was published on March 25, 2004 from an application filed May 29, 2003. Sakamoto demonstrates the knowledge of a POSITA vis-à-vis use of a shared light emitting signal – and confirms the likelihood of success of using such a signal in Kimura Figure 36, because Sakamoto expressly discloses a pixel circuit with a shared light-emitting signal in Figure 5B:



24. Sakamoto's multi-terminal transistor Tr6 provides the second (programming) transistor for the pixel, while Tr2 and Tr4 provide, respectively, the fourth transistor and the fifth transistor that are turned on to activate light emission. Note that the gate electrodes of Tr2 and Tr4 are both directly connected to the signal line Pj – and thus, Sakamoto explicitly discloses the shared light emitting signal for the fourth transistor and the fifth transistor. EX1020, [0169] ("FIG. 5B shows a circuit diagram of a pixel where both of the gates of the transistors Tr2 and Tr4 are connected to the second scanline Pj. ... The pixel in FIG. 5B may have a lower number of scanlines than that of the pixel shown in FIG. 5A."). Given that other contemporaneous references (such as, as just shown, Sakamoto) expressly disclose the use of a shared light emitting signal, including in multiple pixel circuit configurations, a POSITA would have a high expectation of success using a shared

light-emitting signal in the pixel circuit of Kimura Figure 36. This is especially true given Kimura's teaching of the use of shared signals when possible – so as to reduce the number of wires (and thus, among other things, to save space). *See* Kimura, [0429] (“The number of signal lines can be kept to a minimum” by re-using existing signals).

III. INITIALIZATION/RESET TRANSISTOR

25. Claims 2, 8, 16, and 18 require an “initialization transistor” for “discharging” (*i.e.*, resetting) the voltage stored on the capacitor before the capacitor is programmed. In my Original Declaration, I applied Kimura's transistor 1607 (in Figs. 16/17) to the pixel circuit of Kimura Figs. 33/36 as the claimed “initialization transistor.” EX1003, ¶¶155-158, 215-230; *see also* Petition, 51-56. I further explained how the timing diagram of Kimura Fig. 16B “would directly apply to the modified embodiment” of Kimura Figs. 33/36. EX1003, ¶142 (highlighted figure correlating “initialization period” in '599 patent timing diagram to “initialization” period in Kimura Fig. 16B); *see also* Petition, 16, 55-56.

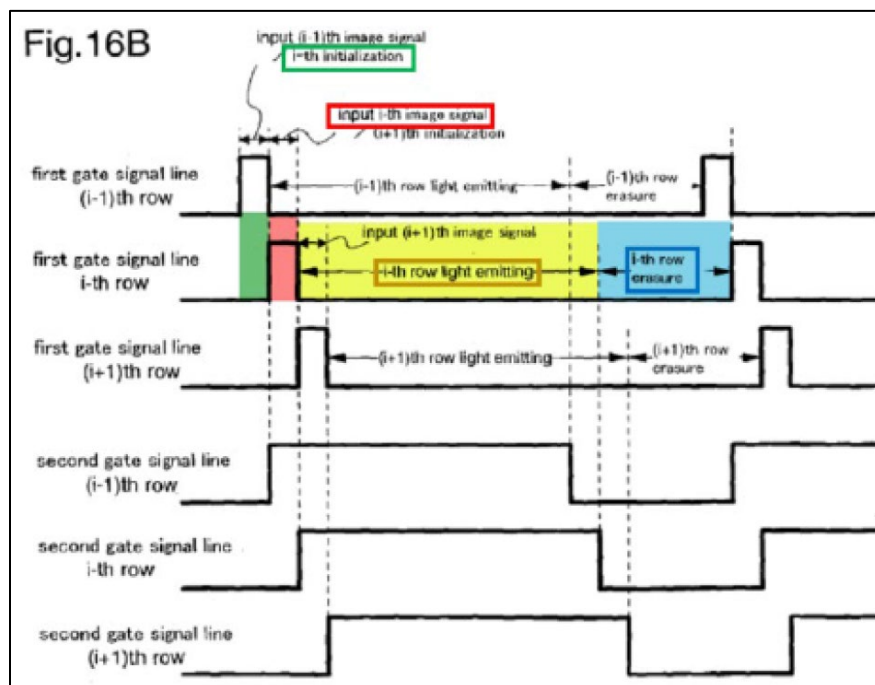
26. However, some further clarifications are helpful.

A. Patent Owner Confuses “Initialization” and “Erasure” in Kimura

27. In its POPR, Patent Owner asserted that “Petitioner Conflates ‘Initialization’ with ‘Erasure’” (Institution Decision at 47 (citing POPR at 16)), which caused some confusion (Institution Decision at 47-49). The Board observed

that “Patent Owner highlighted the initialization period [of Kimura Fig. 16B] in green and the erasure period in blue, and the two do not overlap.” *Id.*, 49. This conclusion is actually (and, in fact, plainly) incorrect when Kimura Fig. 16B is properly understood, as it would be by a POSITA – as I will now further explain.

28. To begin, consider the timing diagram of Figure 16B of Kimura – which I used in my original declaration, and which the Patent Owner used in its POPR; here, for clarity, I will use the color-annotated rendition of Figure 16B that the Patent Owner provided in its POPR (and which the Board used in its Institution Decision).



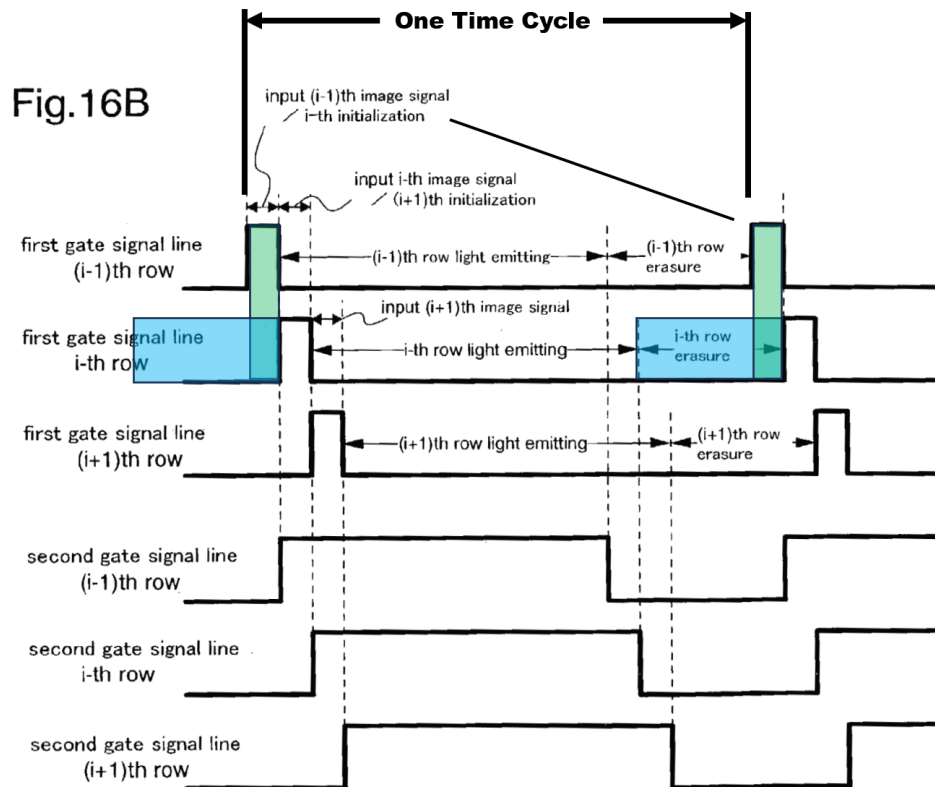
29. As will be discussed in some additional detail below, this timing diagram is intended to be repetitive (*i.e.*, repeat itself over and over). As is often the case with such diagrams, only the details necessary to allow the reader to understand the entirety of one complete time cycle (and the operations conducted therein) are

provided. Of particular note, as time flows from left to right in such a diagram, the details of one cycle can be said to begin¹ with the “i-th initialization” in the upper left, and end with the “(i-1)th row erasure” that appears further along in the top waveform in the figure; as just described, at that point the next time cycle begins anew, and the waveforms (and the activities they induce) repeat themselves.

30. Thus, even though a POSITA reading a timing diagram such as this one (which are common in the art) would understand all of this, further clarity can be provided by examining a fuller set of details regarding the timing diagram and its repetitions. Of particular note, the “i-th initialization” period (highlighted in green) and the “i-th row erasure” (period) highlighted in blue are *not* actually separate from each other (as the figure above, as annotated by Patent Owner, attempts to imply). Rather, there should be another blue “i-th row erasure” period on the left side of the waveform, and there should be another green “i-th initialization” period on the right side of the diagram – with the green-highlighted region being contained entirely within the blue-highlighted region.

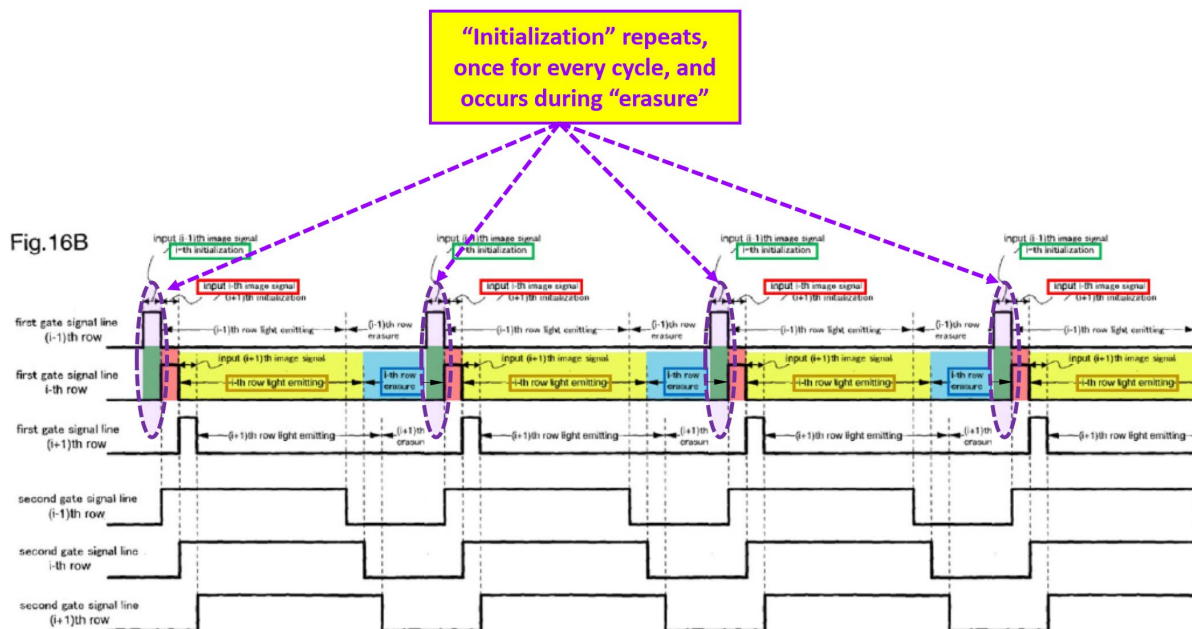
¹ Of course, as this process is repetitive, one time-cycle could be chosen to begin pretty much anywhere – as long as the time cycle is deemed as ending at the point where the activities will begin to repeat themselves in the next cycle; the particular choice used here is the simplest way to allow the activities of one cycle to be explained in detail.

31. This is best-explained by providing proper annotations to Figure 16B of Kimura – in which the just-described additional details (for the repetitive blue erasure periods and the repetitive green initialization periods) can be annotated onto the figure from Kimura.



32. As can be seen from this annotated diagram, the waveforms repeat themselves (as just described) for each time cycle – with the blue erasure period and the green initialization period repeating for successive time cycles (as shown by the annotations above). As can also be seen via this annotated diagram, when the timing diagram is properly understood, the erasure (blue) period and the initialization

33. Thus, what the Patent Owner has asserted is incorrect – the initialization period and the erasure period in fact *do* overlap (in time); as just described, the initialization period is shorter (in time) than is the erasure period, but the initialization period occurs entirely within the erasure period. Perhaps more importantly, neither the erasure nor initialization periods overlap or conflict with light emission or programming (labelled “input [] image signal” in Fig. 16B).



initialization event of the initialization period) being repeated continually during circuit operation.

35. It should also be noted that even if other things besides initialization occur during the “erasure” period, the claims are comprising claims – and it is my understanding from counsel for Petitioner that this allows for other such things to be present (including things which are simply irrelevant to the ’599 claims). This includes Samsung’s example (cited by the Board) that erasure “forcibly plac[es] [the EL device] in a non-light-emitting state”). *See* Institution Decision at 47-49.² Rather, I rely on Kimura’s disclosure that the initialization/reset transistor 1607 discharges the voltage on the capacitor – and resets it to a known/pre-determined voltage (which prepares the programming circuitry for the next programming cycle). This is also why Kimura sometimes refers to what the ’599 patent calls the “initialization” process as being (in Kimura) both “initialization” and “erasure.” EX1003, ¶224, fn. 21; *see also* Petition, fn. 4 (Kimura also refers to “initialization” as “reset” (*see* Fig. 1B) and “erasure” (*see* [0658])).

36. The fact that the erasure period in Figure 16B includes more (in time) than just the initialization operation does not affect my analysis. Indeed, Kimura

² In any event, forcing the LED into a non-light emitting state is entirely consistent with an “initialization” operation designed to occur when no light is being emitted from the LED.

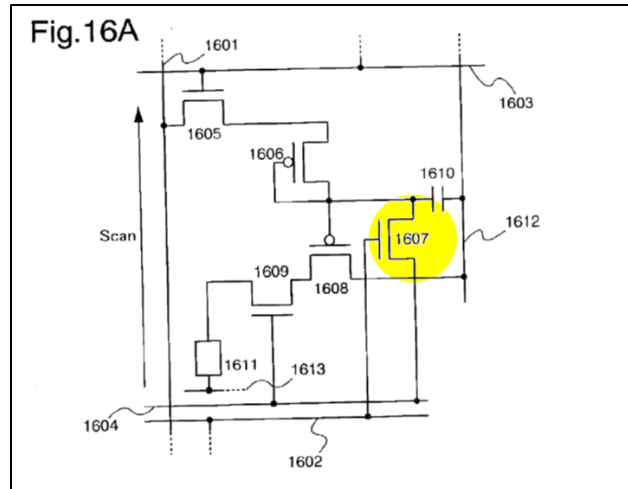
expressly recognizes a flexible approach, stating that “*other steps may be taken if an erasure period is provided*”) (emphasis added). Kimura, [0651]. As annotated Figure 16B above indicates, my opinion is based on the initialization period (highlighted in green) rather than the optional additional erasure period in blue.

B. The “Resetting” of a Circuit is Well-Known in the Art, and is Explicitly Disclosed by Kimura

37. As a general matter, various techniques for “resetting” a circuit have long been known in the field of electronics, and the concept is not limited to OLED driver circuits. Further, as explained in the discussion above with respect to Figure 33B, this particular embodiment in Kimura “resets” the capacitor – wherein the voltage on the capacitor node that connects to the gate of transistor 3308 is drained away – by draining this charge out of the circuit via the path that runs through the light-emitting element 3313. While Kimura provides the Fig. 33 embodiment as an alternative, it explicitly notes (at [0666]), that this choice for the capacitor-discharge path has the undesirable effect of causing a brief, spurious emission of light from the light-emitting element. This teaching fully informs the reader of the pros and cons of this embodiment (e.g., fewer transistors are used at the expense of spurious light emission).

38. Kimura then further educates the reader by providing other embodiments in which a separate, dedicated transistor is included which serves solely to provide an independent drainage path (for the draining-away of the voltage

that had been programmed onto the node that connects to the gate of transistor 3308). For example, as discussed above, in the embodiment depicted in Figure 36, such a dedicated initialization/reset/erasure transistor is included (as a modification to the embodiment depicted in Figure 33); in addition, in the embodiment depicted in Figure 16A, such a dedicated initialization/reset/erasure transistor (transistor 1607) is also provided. Transistor 1607 (regardless of what it is called) serves one purpose – to drain the node that, in this depiction, is connected to the capacitor 1610.



39. Kimura explains that “to perform initialization of a certain row, [the circuit] utilizes the selection pulse of the gate signal line of the previous row in controlling the TFT 1607.” Kimura, [0429]; *see also id.*, [0426] (“The TFT 1607 turns on when the first gate signal line 1602 of the (i-1)th row is selected.”). Again, Kimura is describing the use of a transistor which is activated to discharge the node connected to the capacitor, as a way of initializing/erasing/resetting the programming (if any) that had been applied to that node.

40. Kimura, like the ‘599 patent, further expressly teaches the benefits of using the prior scan line signal (“i-1th” in Kimura), as it is already available. *See* Kimura, [0422] (only two total control signals needed for pixel circuit; *id.*, [0429] (“[T]o perform initialization of a certain row, it utilizes the selection pulse of the gate signal line of the previous row in controlling the [sixth transistor].... The number of signal lines can be kept to a minimum.”). Kimura also provides an accompanying timing diagram (at Figure 16B, which was discussed above) which shows exactly this – initializing a given row occurs when the “first gate signal” of the “(i-th) row” (i.e. the claimed current scan signal) is asserted. Kimura, [0423] (“A gate electrode of the TFT 1607 [sixth transistor] is connected to the gate signal line 1602 of an (i-1)th row.”). As Kimura explains for Figure 16 and Figure 17, “to perform initialization of a certain row, [the circuit] utilizes the selection pulse of the gate signal line of the previous row in controlling the TFT 1607 [sixth transistor].” Kimura, [0429]; *see also id.*, [0423] and [0426].

41. Thus, a POSITA would have available, entirely from Kimura, the option of including a dedicated transistor for the purpose of draining the voltage off of a “programmed” node (*i.e.*, discharging the capacitor). Further, a POSITA would be motivated by the express teachings of Kimura to add a transistor of the type shown in Figure 16 to the embodiment of Figure 33/36 – as a way of accomplishing the initialization/reset/erasure of the node connected to the gate of transistor 3308, but

without having the side-effect (explicitly acknowledged by Kimura) of a spurious, transient light emission from the light-emitting element 3313; in addition, a POSITA would understand (as per the discussion below, in Section IV) that it would be a simple matter to use a pMOS transistor in the Figure 33/36 embodiments (rather than the nMOS transistor that is depicted in Figure 16A) – for the reasons to be explained below in Section IV.

42. Finally, a POSITA would understand that (as also explained above) this inclusion (of a dedicated initialization/reset/erase transistor) would exact a price – in that by increasing the number of transistors in the circuitry of Figure 33,³ the complexity and size of this circuitry will be increased; however, the motivation provided by the ability to eliminate the aforementioned spurious light emission is sufficient for such a modification to be chosen.

³ I note here that in Figure 36, locating the initialization/reset transistor in the same place as Fig. 16A would not even increase the number of transistors in Figure 36, and would have the benefit of draining the capacitor through a single transistor rather than through two transistors.

C. Patent Owner Confuses the Issues by Citing Extraneous Circuit Embodiments

43. Finally, it should be noted that Patent Owner confuses these issues by citing circuit embodiments in its POPR that were not used in either the Petition or my original declaration.⁴

44. For example, at pages 14, 16, and 19 of the POPR, the Patent Owner cites paragraph 410 of Kimura. However, simple examination of this paragraph of Kimura shows that here, Kimura is discussing the Figure 9 embodiment – more specifically in this paragraph, Figure 9B and Figure 9C. This is not the embodiment from which the initialization/reset transistor was drawn in either my original declaration or in the Petition; it is thus irrelevant to the unpatentability analysis presented in both my original declaration and the Petition.

45. In addition, on page 16 of the POPR, the Patent Owner cites paragraph 415 of Kimura. However, simple examination of this paragraph of Kimura shows that here, Kimura is discussing the Figure 10 embodiment – more specifically in this paragraph, Figure 10A. This is also an embodiment that was never referenced or relied on in either my original declaration or in the Petition; it is thus also irrelevant

⁴ It should also be noted that in the pages in the POPR that are discussed in the following two paragraphs, the Patent Owner continues to confuse “initialization” and “erasure” – in the same ways that were already explained above in Section III.A.

to the unpatentability analysis and opinions presented in both my original declaration and the Petition. At a minimum, the operations occurring during the “erasure” period (which includes “initialization”) in Figure 16B must be evaluated on their own merits and in the context of the actual circuits they describe in Kimura (Figures 16/17) and as applied by Petitioner (viz., Figures 33/36).

IV. MANUFACTURING AND DESIGN BENEFITS OF AN ALL-PMOS PIXEL CIRCUIT IMPLEMENTATION

46. Certain claims in the ’599 patent specifically require the exclusive use of pMOS transistors. *See, e.g.*, claims 3-5, 9-11, and 13. In my Original Declaration, I discussed various reasons for modifying the pixel circuit in Kimura Figs. 33/36 to replace the nMOS switching transistors with pMOS switching transistors. EX1003, ¶¶56-58, 146-154. My Original Declaration then analyzed how the “all-pMOS” implementation satisfied the pMOS claim limitations.

47. With respect to using an all-pMOS switching transistor configuration in Kimura’s pixel circuit, in my Original Declaration I pointed to various express teachings in Kimura (*id.*, ¶¶146-150), as well as other references (*id.*, ¶¶56-58, 151), which demonstrate the knowledge of a POSITA regarding the interchangeability of pMOS and nMOS switching transistors. In two places (*id.*, ¶58, 151), I touched on manufacturing benefits of using only pMOS transistors; I have been asked to further explain this aspect of my Original Declaration.

48. To begin, it is important to distinguish between: (1) making an all-pMOS *pixel circuit* (which can be done even if a CMOS process is used – as both nMOS transistors and pMOS transistors will be available for fabrication); and (2) using a pMOS-only *manufacturing process* (*i.e.*, a manufacturing process that is limited to only making pMOS transistors). Both scenarios present manufacturing benefits, as I discuss below.

49. In the former scenario, (*i.e.*, where a CMOS manufacturing process is used, and thus both nMOS transistors and pMOS transistors are available – but the pixel circuit is all-pMOS), the overall complexity of the manufacturing process itself (*e.g.*, the number of process steps required) is not changed.⁵ One benefit of this approach is that the same manufacturing process can be used to make both the pixel array (*i.e.*, the OLED pixel circuits) and the circuitry for generating the control

⁵ If the pixel circuit is all-pMOS but the peripheral circuits are CMOS, and the pixel circuit is manufactured on the same substrate as are the peripheral circuits, then the number of processing steps is not reduced by having an all-pMOS pixel circuit. However, if exclusively-pMOS circuitry (for either the pixel circuit alone or a combination of the pixel circuitry and the peripheral circuitry) were to be manufactured on the same substrate but using a CMOS process, many of the nMOS processing steps could be dropped from the manufacturing sequence – so the process flow would have fewer process steps than the fully-used CMOS process, but more process steps than would be the case with a true pMOS-only manufacturing process.

signals (typically located on the periphery of the pixel array) on the same substrate – wherein the latter circuitry can consist of well-known “true CMOS” logic circuits.⁶ Such an approach is described (by Kimura) for certain embodiments in Kimura. *See, e.g.,* EX1002, ¶¶501-502 (“Embodiment 4. In this specification, a substrate in which a driver circuit including a CMOS circuit and a pixel part having a switching TFT and a drive TFT are formed on the same substrate is called an active matrix substrate as a matter of convenience.”).

50. I note, however, that Kimura’s disclosure would *not* be understood by a POSITA to be limiting – as in being limited to the use of a CMOS manufacturing process; rather, a POSITA would understand the teachings of Kimura as having application where the pixel array and the peripheral control circuitry are made separately from each other (using two different manufacturing processes and on two separate substrates) - then electrically-connecting those substrates together.

51. This has, for example, long been common practice in the mainstream silicon integrated circuit industry – where well-known trade-offs exist between (at one end of the spectrum) having all circuits in a single silicon IC and (at the other

⁶ For clarity, it should be noted that a “CMOS manufacturing process” means that both nMOS transistors and pMOS transistors can be fabricated together in that process - while a “CMOS circuit” refers to the use of both nMOS and pMOS transistors in a circuit configured in a particular (“CMOS”) architectural form.

end of the spectrum) having functionality distributed across two-or-more silicon ICs (with those separate ICs being connected together, e.g., by mounting them on a printed circuit board, which has wiring traces to implement the interconnectivity). As an example, one key factor in such a trade-off might be speed – which, if it is the dominating factor, would be enhanced by having all of the functionalities in very close proximity to each other in a single silicon IC; as a countervailing example, yield might be the dominant consideration – as it would be if a large, digital, high-yield IC were to be combined with a small, analog, low-yield IC (which would result in a large IC with a low yield – which is not a good plan).⁷

52. As a further example, consider a POSITA with an existing pMOS-only pixel circuit (fabricated with a pMOS-only process or a CMOS process) who encounters the teachings of Kimura. The POSITA could be constrained to using only pMOS transistors in the pixel circuitry – due to the sole availability of pMOS transistors (i.e., only a pMOS-only manufacturing process is available), or a mandate to use only pMOS transistors in the pixel circuitry (for the reasons described earlier).

⁷ In the silicon IC space, a foundry sells processed wafers to designers at a particular price per wafer – which amounts to selling silicon with a per-unit-area price. Converting a large, high-yielding IC into a slightly-larger but low-yielding IC is an expensive (and unnecessarily-expensive) thing to do. The same basic ideas apply to TFTs used in the pixel circuits and peripheral circuits of OLED displays.

Such a POSITA, reviewing the Figure 33/36 embodiments of Kimura and understanding the benefits of that circuitry would certainly be motivated to find some way to convert that embodiment into an all-pMOS form and thus make use of that embodiment (as opposed to seeing the nMOS transistors in the Kimura Figure 33/36 embodiment and just giving up on those embodiments). As I explained in my Original Declaration (e.g. at paragraphs 56-58) a POSITA would understand that it would not be a complex task to do this – as the nMOS switching transistors could be replaced with pMOS switching transistors, and some relatively-simple changes (such as changing the waveforms from active-high to active-low) would be required of the operating conditions; these structural and operational changes are not difficult to do – and there would be a reasonable expectation of success in doing so.

53. Thus, the benefits of lower cost and simpler manufacturing processes that stem from using a pMOS-only manufacturing process for an OLED pixel array are still applicable to Kimura Figs. 33/36 – which depict only a pixel circuit, and are not focused on peripheral control circuitry.

54. In this regard, I note that Kimura focuses far more on the pixel circuit architecture and operation than it does on details of manufacturing processes or peripheral circuits. Accordingly, a POSITA would understand that manufacturing Kimura's pixel circuits (separate and apart from any peripheral control circuitry) using a pMOS-only process is within the disclosure of Kimura (as Kimura himself

states, as noted above).

55. In any event, even were a CMOS process used to make both the pixel array *and* the surrounding control circuitry on the same substrate,⁸ there are manufacturing benefits to be gained by using an all-pMOS pixel circuit. For example, I discussed Kimura '798 (EX1004) in my Original Declaration (*see* EX1003, ¶151). Kimura '798 discloses that “a transistor circuit 100 [in Fig. 1] may consist of a driving TFT 110 (P channel type), a compensating TFT 120 (P channel type), a resetting TFT 130 (N channel type) and a switching TFT 140 (N channel type).” EX1004, 8:3-6. Kimura '798 further teaches that “the example shown in FIG. 1 is constructed with the mixture of a P channel type TFT and an N channel type TFT,” which indicates to a POSITA that a CMOS manufacturing process is being considered. *Id.*, 12:30-49. Kimura '798 goes on to explain that “all TFTs can be P channel type TFTs” and “it is often advantageous in manufacturing when all TFTs are of the same type.”

56. In fact, one reason that Kimura '798 provides as to why it is “advantageous” to employ only pMOS transistors for both the compensating transistor and the driving transistors is because doing so increases the “degree of

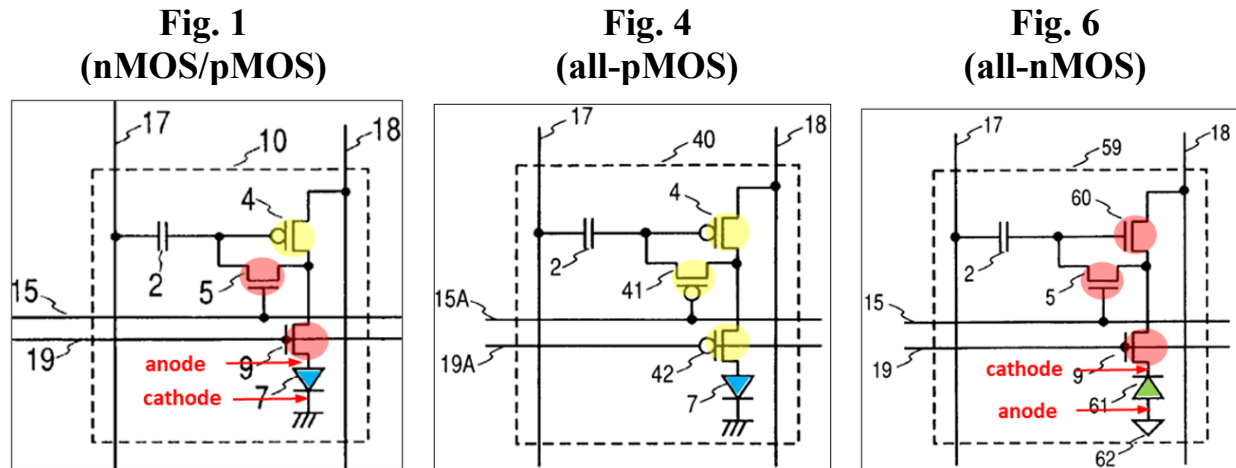
⁸ I note that the limited examples Samsung cites in its POPR – of a combined nMOS/pMOS pixel array and CMOS control circuitry – generally relate to different embodiments than those which I relied on in my Original Declaration.

characteristic similarities” among transistors and results in “little or no variance in voltage/current characteristics and threshold characteristics.” *Id.* This is well-known in the art, as nMOS transistors and pMOS transistors are manufactured using many process steps that are exclusive to either nMOS transistors or pMOS transistors – so that manufacturing variations between the two species, to a large degree, do not correlate (or, at best, only partially correlate). Therefore, using only pMOS transistors leads to greater uniformity of light output among pixels in an array – and, as just discussed, is an expected result. Indeed, this general principle (*viz.*, maximizing the uniformity among the components in a circuit) is well-known across various types of circuit designs⁹ to achieve better uniformity and better performance.

57. Other references also describe the knowledge of a POSITA as it relates to the manufacturing benefits that result from the use of only pMOS transistors in pixel circuits. One such example is U.S. Pub. Pub. 2003/0067424 (EX1021, “Akimoto”). Akimoto is in the same field as is the ’599 patent, and is titled “Image Display Device.” Akimoto was published on April 10, 2003 from an application filed August 6, 2002. Akimoto discloses multiple embodiments of functionally-identical TFT pixel circuits, including mixed nMOS/pMOS implementations, *all-pMOS implementations*, and all-nMOS implementations; for example, this triad is

⁹ The well-known “common centroid” methods in analog circuit design are good examples of using a design technique to improve both uniformity and performance.

shown below (pMOS transistors are annotated yellow and nMOS transistors red):



58. Against this backdrop, Akimoto explains that “since the pixel 40 [of Fig. 4] is composed of only the p-channel MOS transistors, *the layout of the pixel unit is simplified so as to achieve a high definition and high yield.*” EX1021, [0062] (emphasis added). In other words, the “simplified” design of an all-pMOS pixel circuit provides two manufacturing benefits: (1) it allows for a denser pixel array (*i.e.*, more pixels in the same amount of surface area) to achieve higher definition displays; and (2) the uniformity of using a single “flavor” (nMOS or pMOS) of TFT for the pixel results in “high yield” (*i.e.*, a greater percentage of functional units, which translates (among other things) to higher return-on-investment – and thus (hopefully) to profitability (or better profitability). I note here that Akimoto acknowledges that similar results can be achieved with an all-nMOS pixel circuit (EX1021, [0069]), but states no such benefit for a combined nMOS/pMOS pixel circuit (likely for the known reasons that were discussed above).

59. That Akimoto is talking about the benefits of an all-pMOS *pixel circuit* as opposed to an all-pMOS *manufacturing process* is made clear in paragraph [0062] – where Akimoto goes on to further explain that *additional* manufacturing advantages (beyond those already mentioned) such as further “production cost [reductions]” may be achieved if the “peripheral circuits [*viz.*, external drivers] are made up with [only] p-channel MOS transistors.” EX1021, [0062]. Accordingly, a POSITA would understand that choosing to design and use an all-pMOS pixel circuit provides advantages – such as higher manufacturing yield and better display definition; further, these advantages can be obtained regardless of whether the underlying manufacturing process is a CMOS process or a pMOS-only process.

V. CONCLUSION

60. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and thus such actions may compromise the validity of the IPR proceeding. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

61. I declare under penalty of perjury that the foregoing is true and correct.
Executed this 23rd day of January, 2024 in Fletcher, Vermont.



Daniel Foty, Ph.D.