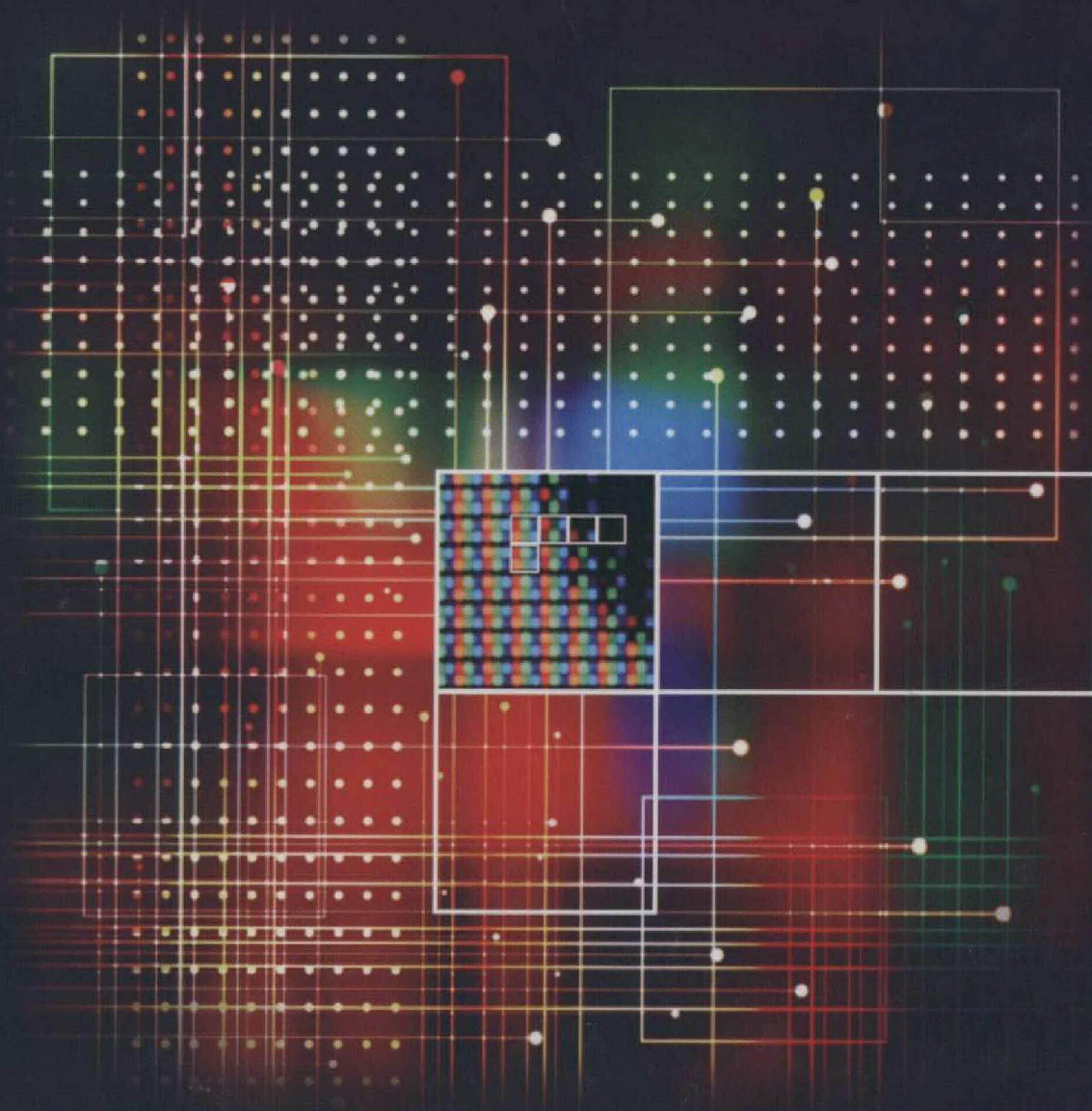


Mobile Displays

Technology and Applications

Edited by

Achintya K. Bhowmik | Zili Li | Philip J. Bos



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Advances in AMOLED Technologies

**Y.-M. Alan Tsai, James Chang, D.Z. Peng, Vincent Tseng,
Alex Lin, L.J. Chen, and Poyen Lu**

TPO Displays Corp., Chunan, Taiwan

14.1 Introduction

In all electronic displays, the front of screen (FOS) performance and physical dimensions (e.g. thickness and weight) are the most straightforward features that users can feel and appreciate. Flat-panel displays such as liquid crystal display (LCD) and plasma display have progressed well technically, and made the move in many applications to replace bulky and energy-consuming cathode ray tubes (CRTs). Nowadays, flat-panel displays have become the dominant display choices for large-size PC monitors and TVs. In recent years the multimedia and digital era has emerged, with more and more functions built on mobile devices, such as camera and TV viewing on mobile/cell phones. As a result, FOS performance, such as brightness, contrast ratio, viewing angle, and response time, all need to be substantially enhanced. Emissive display is the natural display to choose to provide superior FOS performance. One emissive technology that shows promise involves organic electroluminescence devices (or organic light-emitting diodes – OLEDs), has been studied extensively, and its commercial products have gradually started to come on the market. Usually, they have appeared at just the right time to fulfill the massive need.

In this chapter, we will give an overview of OLED technology, including the OLED electroluminescence mechanism, materials, and device structure, as well as the backplane that is needed to drive the OLED – thin-film transistor (TFT). Advances in active-matrix organic electroluminescence display (AMOLED) will be reviewed and discussed.

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14.2 OLED Technology

14.2.1 Introduction

OLED displays have attracted a lot of attention due to their many advantages, such as fast response time, wide viewing angle, higher contrast ratio, and very thin structure. In 1987, Tang and Van Slyke of Kodak described an efficient green OLED from thin-film evaporation of the vapor organic compounds, triphenylamine and aluminum tris-8-hydroxyquinoline (Alq) [1, 2]. This important discovery enhanced the prospects for producing larger and inexpensive displays that could replace CRT and LCD. In 1990, another new electroluminescence device based on conjugated polymer (para-phenylenevinylene, PPV) that emitted yellow-green light was produced by Burroughes's group at Cambridge University [3]. Since then, OLED has become a popular topic in academia and industry, and has the potential to be the great display of the future.

In addition to the features that OLED can offer in FOS and physical dimensions, active-matrix OLED (AMOLED) has generated much attention due to its capability to deliver higher resolution, larger panel, and better display quality. Many OLED development activities have been based on AMOLED to further strengthen OLED's advantages. Significant progress has been made in AMOLED materials, device, and production technologies in recent years. In this section, we will give an overview of OLED technology, including its electronic mechanism, materials, device structure, advanced processes, and application in AMOLED.

14.2.2 Electroluminescence Mechanism

(1) Physics for OLED Operation

The simple structure of OLED is illustrated in Figure 14.1. The simplest OLED structure consists of an anode (ITO), a hole transporting layer (triphenylamine), an electron transporting layer with emitting function (Alq), and a cathode [1]. In order to reduce the driving voltage and improve efficiency of the OLED, the hole injection layer and electron injection layer have been introduced.

When a voltage is applied across the OLED, the charged carriers (holes and electrons) are injected from the anode and cathode into the adjacent organic layers, respectively. Traveling through the

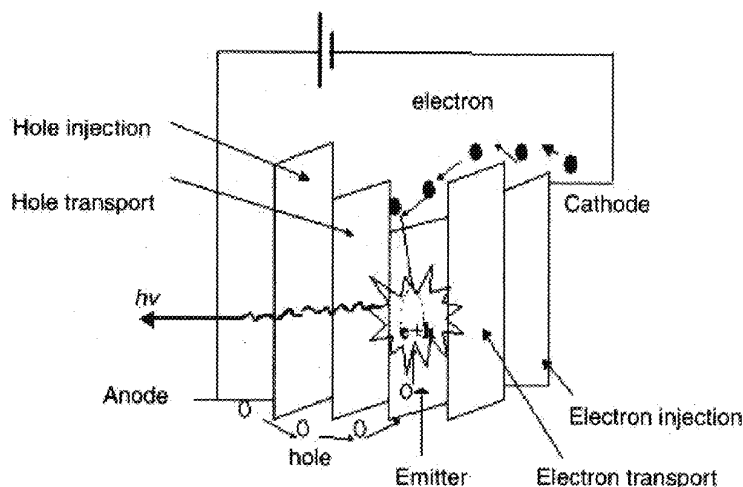


Figure 14.1 OLED structure.

injection materials and transporting materials, the carriers with opposite polarity recombine in the emitting layer and generate the 'exciton'. Relaxation of the exciton leads to photon emission.

(2) Relaxation and Luminescence

When carriers with opposite polarity recombine they produce excitons. An exciton is essentially a molecule in the excited state. By means of the electroluminescent mechanism, there are four excited microstates of the exciton. One is the anti-symmetry spin hybrid ($s = 0$, singlet), and the other three are symmetry spin hybrids ($s = 1$, triplet). According to the selection rule, only relaxation from the singlet excited state to the ground state is in general allowed. The allowed relaxation that produces a photon is called fluorescence (see Figure 14.2).

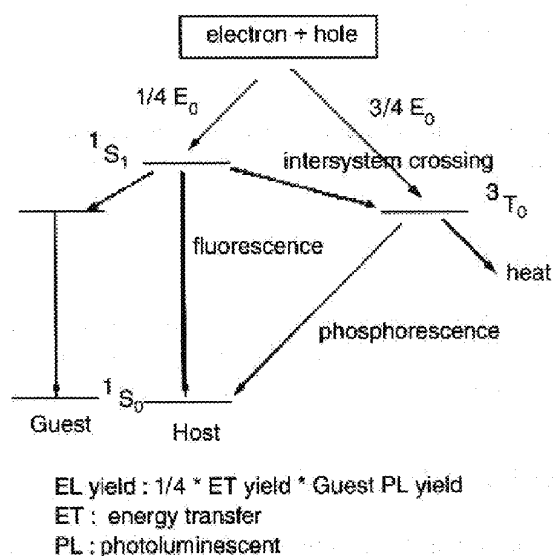


Figure 14.2 Hole-electron recombination and energy distribution.

Relaxation from triplet excited states to the ground state is forbidden in the selection rule. However, when spin orbital coupling occurs, this kind of relaxation can still take place, and is called phosphorescence [4].

(3) Efficiency

Since the mechanisms of OLED are related to carrier injection, carrier recombination, and relaxation of the excited state, the internal quantum efficiency (η_{int}) is defined as

$$\eta_{\text{int}} = \gamma \eta_{\text{ex}} \phi_p \quad (1)$$

γ : the ratio of electrons and holes injected from opposite contacts (the electron-hole charge balance factor).

η_{ex} : the fraction of total excitons formed which result in radiative transition.

ϕ_p : the intrinsic quantum efficiency for radiative decay.

The γ factor is the ratio of recombination. The effective collision of electrons and holes takes place on the same emitting molecule, and then the molecule is excited and forms the exciton. The injection ratio of the carriers and the recombination zone should be well controlled to improve the efficiency.

The η_{ex} factor is the energy transfer ratio during relaxation of the exciton. It refers to the photoluminescent efficiency of the emitting material. Introducing high photoluminescent efficiency emitting material will give rise to high quantum efficiency. The ϕ_p factor is the intrinsic quantum efficiency based on the selection rule of the relaxation. For fluorescent emitting material, the maximum value for the ϕ_p factor is 1/4.

The internal quantum efficiency is the energy transfer ratio between the electric energy and photo energy. It only occurs inside the emitting layer and is not easy to measure. We usually detect the photons through the organic layers, electrode, and substrate. The detected efficiency is the external quantum efficiency (η_{ext}) defined by

$$\eta_{ext} = \eta_{int} \chi = \gamma \eta_{ex} \phi_p \chi \quad (2)$$

η_{int} : internal quantum efficiency.

χ : light out-coupling efficiency.

γ , η_{ex} , and ϕ_p : as defined above.

There is optical interference between the organic layers, organic-electrode interface, electrode-substrate interfaces, and substrate-air interface. The χ factor is the total effect of the interference. A good optical design should reduce the interferences, and improve the external quantum efficiency.

14.2.3 OLED Materials

Organic materials can be classified, according to their function, as hole injection materials (HIM), hole transport materials (HTM), emitters (guest and dopant), electron transport materials (ETM) and electron injection materials (EIM).

14.2.3.1 Hole Injection Material

The function of the hole injection material is to help hole injection into the organic layer from the anode (ITO). Thus, there are some requirements for these materials, such as:

- (a) the work function needs to be as close to the ITO work function (4.8 eV) as possible;
- (b) good adhesion to ITO.

Popular materials for hole injection include: CuPc, CFX, mTDTA, and TNATA (see Figure 14.3).

14.2.3.2 Hole Transport Material

The function of hole transport material is to transport holes to the emitting layer. Required properties for these materials are:

- (a) high hole mobility;
- (b) high T_g (glass transition temperature) material;
- (c) good electrochemical stability;
- (d) good thin-film quality from vapor deposition.

Popular materials include: NPB, TPD, and Spiro-NPB (see Figure 14.3).

14.2.3.3 Emitter

The function of the emitter is to control light output and color. Two types of material can be used for an emitter: one is the host, and the other is the dopant. Required properties for an emitter include:

- (a) high quantum yield;
- (b) good electrochemical stability;
- (c) good thin-film quality from vapor deposition.

Popular materials include: DPVBi, C-545T, DCJTb, Rubrene, AND, Ir(ppy)₃, UGH1, UGH2, UGH3, UGH4, FIr₆, Ir(pmb)₃, and Ir(btp)₂(acac) [5–11] (see Figure 14.3).

14.2.3.4 Electron Transport Material

The function of electron transport material is to transport electrons to the emitting layer. Hence, there are some requirements for these materials, such as:

- (a) high electron mobility;
- (b) good electrochemical stability;
- (c) good thin-film quality from vapor deposition.

Popular materials include: Alq, BeBq, TPBI, and TAZ (see Figure 14.3).

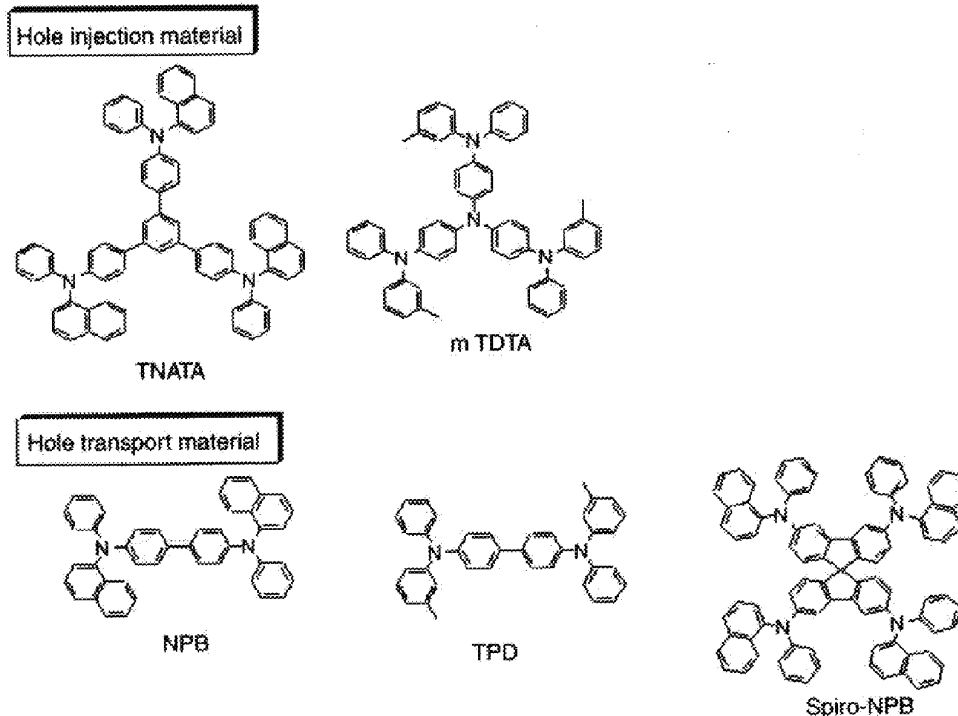


Figure 14.3 Popular OLED materials.

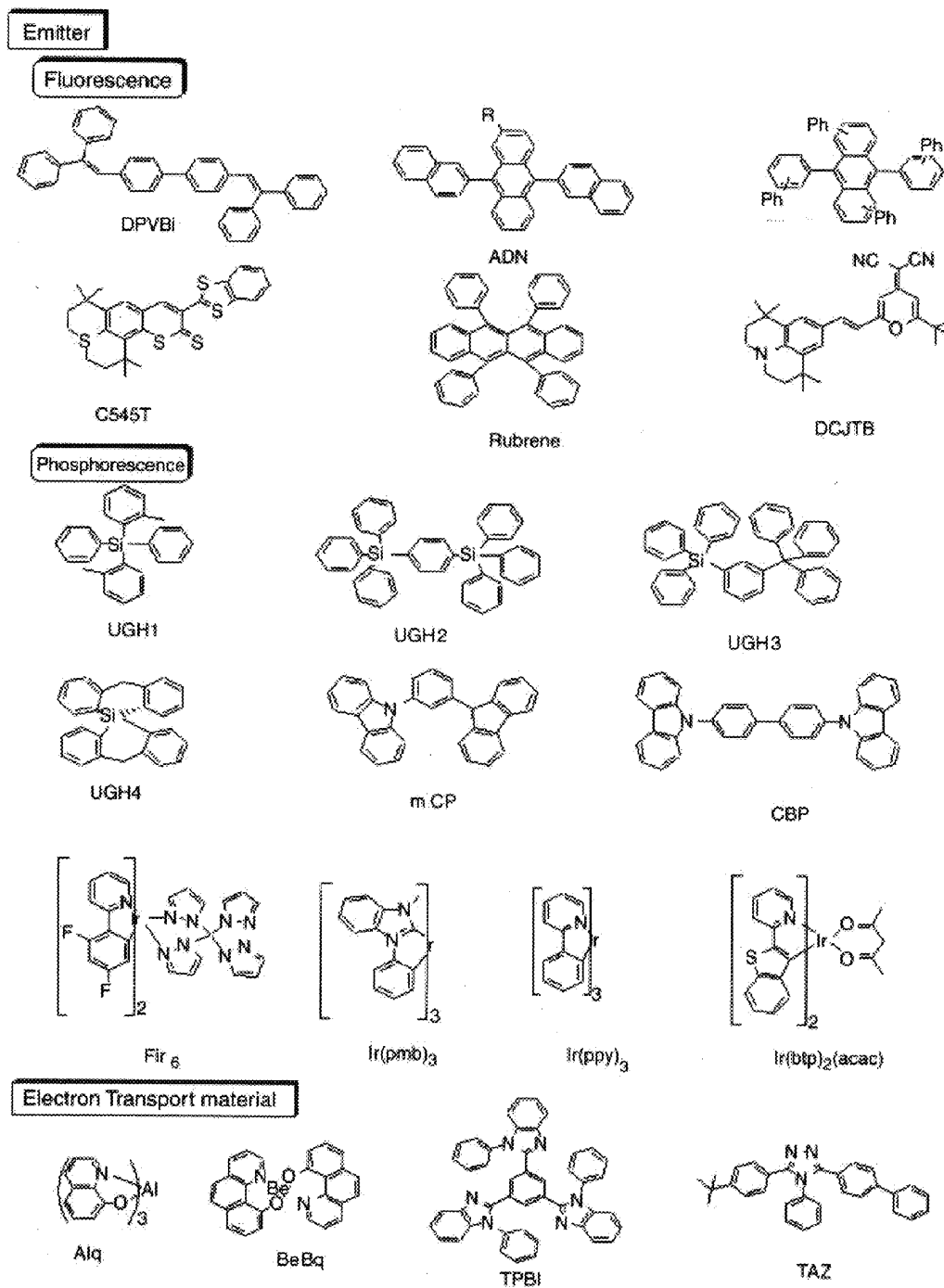


Figure 14.3 (Continued)

14.2.4 Advanced OLED Devices

Compared to advanced TFT-LCD devices, low power consumption is one of the key properties that AMOLED need in order to be competitive, especially in mobile devices. High-efficiency inorganic LED is used in current TFT-LCD products as a backlight, thus efficiency improvement is a crucial topic in OLED technology development.

Recently, some new designs in OLED device structure have been published that give rise to better performance. One is the p-i-n structure; the other is the tandem OLED structure.

14.2.4.1 The p-i-n Structure

To obtain high power efficiency and low driving voltage for OLEDs, efficient charge injection at the interface and low ohmic transport layer are two key factors. A commonly used method is to insert a buffer layer between the anode and HTL, and to insert a thin layer between ETL and EIL, to improve hole and electron injection respectively. A method that increases the conductivity of the organic semiconductor layer by doping with p-type acceptors into HTL or n-type acceptors into ETL can theoretically reduce the driving voltage of OLEDs, as reported by Leo's group in 1998 [12, 13]. For instance, one OLED structure reported is ITO/mTDATA: F4-FCNQ/TPD/Alq/Bphen/BPhen:Li/LiF/Al (Figure 14.4) which resulted in a good OLED device with a performance of 5.4 cd/A and 1000 cd/m² at 2.65 V.

Moreover, Forrest's group [14–16] used the p-i-n structure in a phosphorescence OLED. The structure is ITO/mTDATA: F4-FCNQ/Irppy:CBP/Bphen/BPhen:Li/Al, which produced a highly efficient OLED with a performance of 29 lm/W and 200 cd/m² at 1 mA/cm².

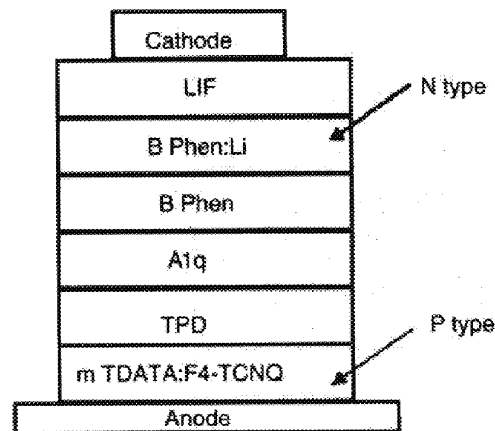


Figure 14.4 Pin structure of OLED.

14.2.4.2 Tandem Structure of the OLED

An OLED device having multiple emitting units stacked vertically in series, i.e. tandem OLED, can provide high luminance, enhancement of current efficiency, and convenient tuning of the emission spectra. The spectral tuning of devices, through stacking units emitting different colors, is particularly useful. The major challenge in tandem OLED is to prepare an effective connecting structure between emitting units so that the current can flow smoothly without encountering substantial barriers. This has already been stated in 1st line of section. Therefore, some researchers

have proposed using the tandem structure to provide high luminance from OLED. They used connecting electrodes such as:

Mg:Ag/IZO [17], ITO [18], BPhen:Cs/V₂O₅(or ITO) [19], Alq₃:Li/NPB:FeCl₃

or

TPBI:Li/NPB:FeCl₃ [20], Alq₃:Mg/V₂O₅ [21], Alq₃:Mg/WO₃ [22], and LiF/Ca/Ag

or

LiF/Al/Au [23].

In our study, the connecting structure consists of a thin metal layer (Al) as the common-electrode, a hole injection layer (MoO₃) providing hole injection into the upper unit, and an electron injection layer (Alq₃:Cs₂CO₃) providing electron injection into the lower unit. The white-emitting two-unit tandem devices were fabricated with a structure of ITO/HT-01 (60 nm)/HT-01 (20 nm)/BH-01:BD-04 (10 nm)/BH-01:RD-01 (25 nm)/Alq₃ (10 nm)/Alq₃:Cs₂CO₃ (20 nm)/Al (1 nm)/MoO₃ (5 nm)/HI-01 (device A: 50 nm, device B: 55 nm, device C: 60 nm)/HT-01 (20 nm)/BH-01:BD-04 (10 nm)/BH-01:RD-01 (25 nm)/Alq₃ (25 nm)/Cs₂CO₃ (1 nm)/Al (Figure 14.5).

The I-V-L characteristics and efficiency of tandem devices are shown in Figure 14.6, below. The device A-C exhibits a driving voltage roughly double the single-unit device voltage, and the current efficiency of tandem devices (A: 16.9 cd/A; B: 16.6 cd/A; C: 17.5 cd/A at 20 mA/cm²) is more than double that of a device with a single unit (8.3 cd/A at 20 mA/cm²) [24].

14.2.5 Advanced OLED Process

OLED technology for full color display can be achieved with various approaches. The most conventional OLED process is the RGB side-by-side approach. A fine metal mask (FMM) is applied during RGB deposition for the color patterning.

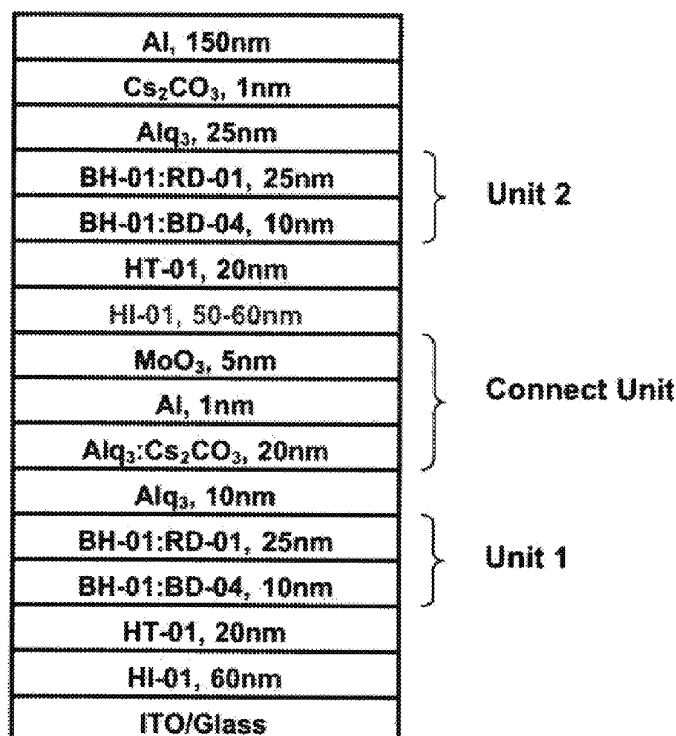


Figure 14.5 The structure of tandem white OLED.

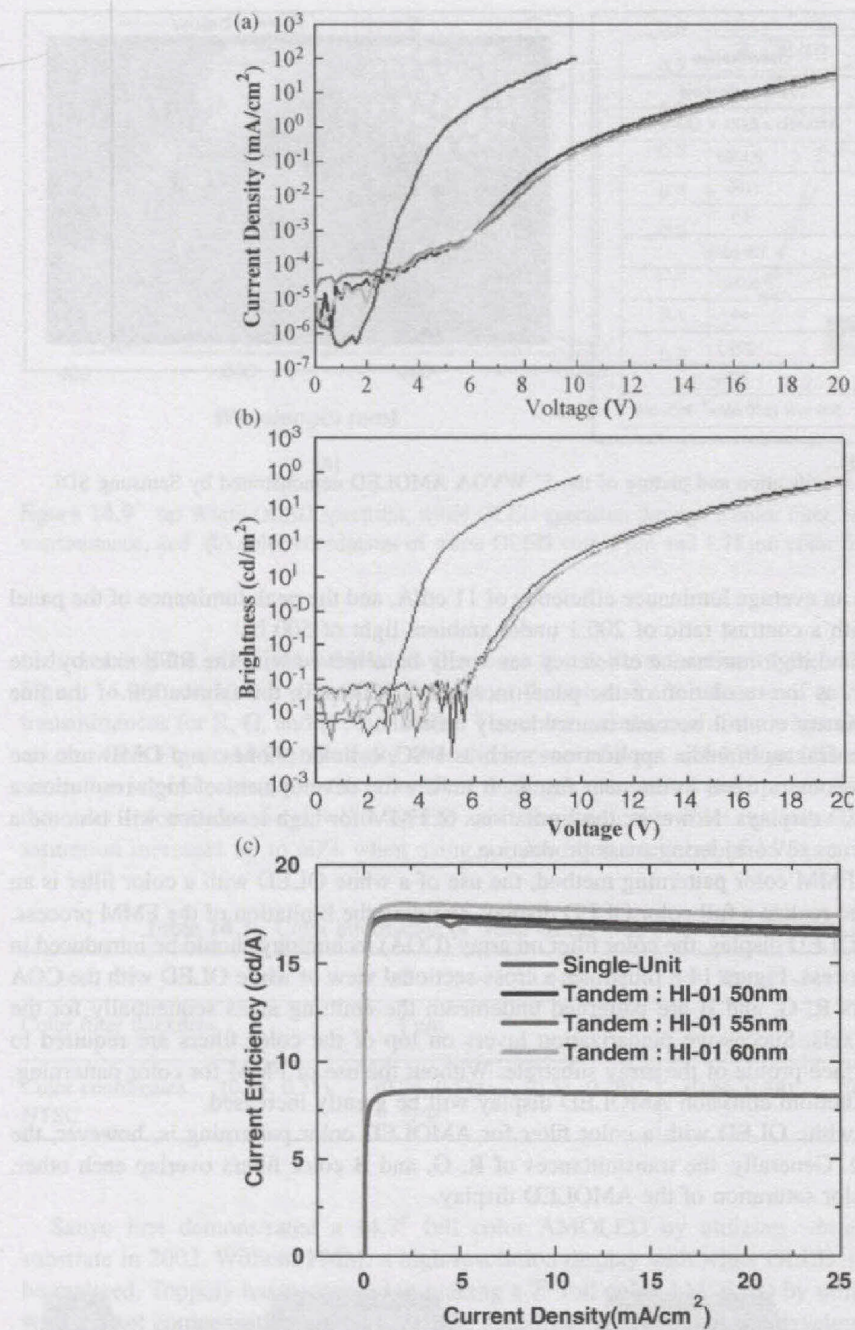


Figure 14.6 (a) The I-V curve of single unit, A, B, and C devices. (b) The L-V curve of single unit, A, B, and C devices. (c) The efficiency-current curve of single unit, A, B, and C devices.

In 2003, Samsung SDI developed a high-resolution AMOLED full color display by utilizing a fine metal mask [25]. The prototype display is 5" diagonal size with WVGA (800×480) resolution and with a pixel pitch equal to 0.1365 mm (186 ppi), as shown in Figure 14.7, below. The specification of the prototype is also listed in Figure 14.7. The white CIE coordinates are $x = 0.31$ and $y = 0.32$. The

Parameter	Specification
Display size	5.0 inch diagonal
Resolution	800(H) x RGB x 480(V)
Pixel pitch (mm)	0.1365
Pixel per inch (ppi)	186
Aspect ratio	5:3
Peak luminance	> 300 cd/m ²
Driving frequency	50 Hz
Gray level	64
Contrast ratio	>200:1
Aperture ratio	33%
Power consumption	500 mW (250 cd/m ² , 30% on)



Figure 14.7 The specification and picture of the 5" WVGA AMOLED demonstrated by Samsung SDI.

performance exhibits an average luminance efficiency of 11 cd/A, and the peak luminance of the panel is over 300 cd/m² with a contrast ratio of 200:1 under ambient light of 500 lx.

High NTSC ratio and high luminance efficiency can easily be achieved with the RGB side-by-side technology. However, as the resolution of the panel increases (>200 ppi), the fabrication of the fine metal mask and alignment control become tremendously difficult.

The merging of several multimedia applications such as DSC, cellular phones, and DMB into one mobile device will become a trend in the near future. It makes the development of high-resolution a critical factor in OLED displays. However, the limitations of FMM for high resolution will become a key issue when it comes to considering mass production.

In addition to the FMM color patterning method, the use of a white OLED with a color filter is an alternative approach to realize a full color OLED display, avoiding the limitation of the FMM process. For an active-matrix OLED display, the color filter on array (COA) technology should be introduced in the array substrate process. Figure 14.8 illustrates a cross-sectional view of white OLED with the COA structure. Color filters R, G, and B are patterned underneath the emitting areas sequentially for the primary color sub-pixels. Successive planarization layers on top of the color filters are required to flatten the ragged surface profile of the array substrate. Without the use of FMM for color patterning, the resolution of the bottom emission AMOLED display will be greatly increased.

One drawback of white OLED with a color filter for AMOLED color patterning is, however, the color saturation issue. Generally, the transmittances of R, G, and B color filters overlap each other, which reduces the color saturation of the AMOLED display.

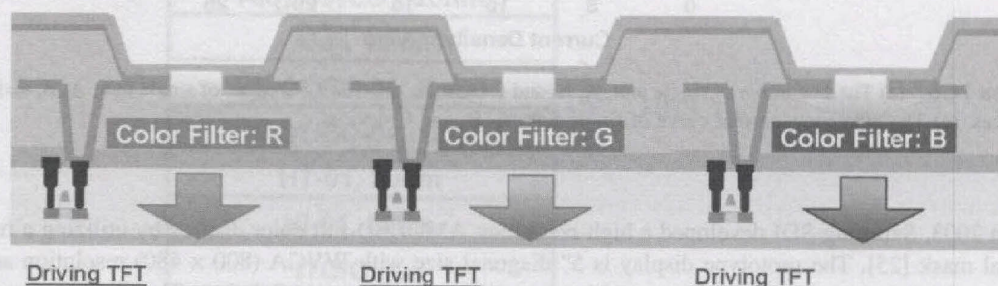


Figure 14.8 Cross-section of white OLED with COA structure.

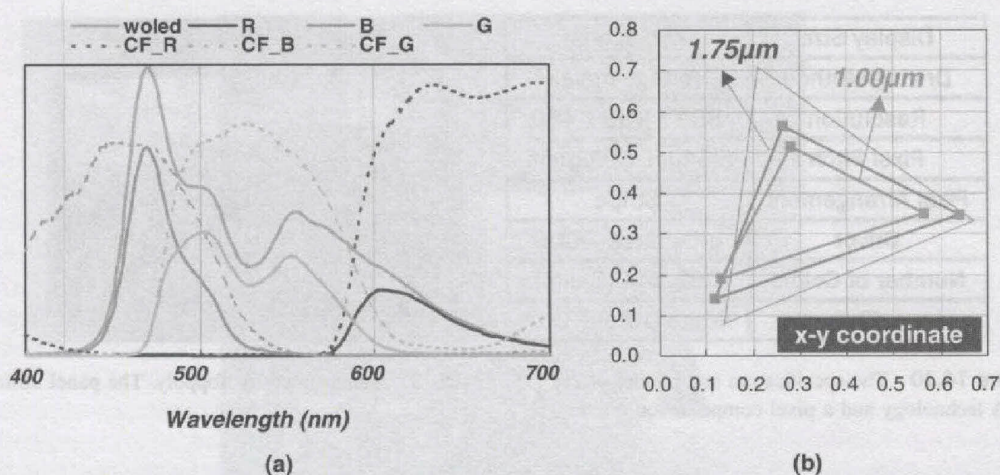


Figure 14.9 (a) White OLED spectrum, white OLED spectrum through a color filter, and the R/G/B color filter transmittance, and (b) color coordinates of white OLED with 1 μm and 1.75 μm color filter thickness.

Increasing the color filter thickness improves the color saturation of the AMOLED display [26]. Figure 14.9(a) shows the white OLED spectrum before and after the use of color filters as well as the transmittances for R, G, and B color filters. The color coordinates of the white OLED after color filters are shown in Figure 14.9(b) for color filter thicknesses of 1 μm and 1.75 μm. The improvement in color saturation is noticeable when the color filter thickness increases from 1 μm to 1.75 μm. Table 14.1 lists the color information for a white OLED with the two color filter thicknesses in each color. Color saturation increases up to 60% when using a color filter thickness of 1.75 μm.

Table 14.1 Color information of white OLED with color filter thickness of 1.75 μm.

	R	G	B	R	G	B
Color filter thickness	1 μm			1.75 μm		
Color coordinates	(0.56, 0.35)	(0.28, 0.51)	(0.31, 0.19)	(0.66, 0.34)	(0.25, 0.59)	(0.12, 0.12)
NTSC	37%			60%		

Sanyo first demonstrated a 14.7" full color AMOLED by utilizing white OLED with a COA substrate in 2002. Without FMM, a high-resolution display with white OLED + COA technology can be realized. Toppoly has succeeded in making a 7" full color AMOLED by utilizing COA technology with a pixel compensation circuit [27]. The specification, as well as the developed AMOLED display, is shown in Figure 14.10, below.

One drawback of the white OLED + COA technology may be the higher power consumption for display applications. Much of the white light is absorbed by color filters, which gives a low luminance efficiency. Van Slyke *et al.*, from Eastman Kodak Company, introduced a white emitter-based AMOLED with an RGBW pixel format in 2005 [28]. It was shown that a simple approach for the RGBW format to achieve low power consumption is to select white OLED material for which the CIE is equivalent or close to the required white point in the specification. The power consumptions of white OLED with the RGB and RGBW formats and various white materials are compared in Table 14.2 for 2.2" AMOLED displays.

Display Size	7" diagonal
Driving Method	Voltage-driven
Resolution	800 x RGB x 480
Pixel Pitch	64 μ m x 192 μ m
Pixel Arrangement	Stripe
Driver	Integrated / COG
Number of Colors	262,144 (6-bits)
EL	White OLED + COA



Figure 14.10 The specification and picture of the 7.0" AMOLED demonstrated by Toppoly. The panel utilized COA technology and a pixel compensation circuit.

According to Table 14.2, the smallest power consumption for the RGBW panel is only 42% of that for the RGB display. Moreover, this table also indicates that the power consumption of the RGBW display is determined by the color and efficiency of the white emitter.

Recently, laser-induced thermal imaging technology (LITI) was introduced to realize high-resolution OLED displays [29, 30]. The LITI process utilizes a donor film, a highly accurate laser-exposure system, and a substrate. The LITI process can be described as follows (as shown in Figure 14.11, below):

- (1) The thermal transfer donor is first laminated to a substrate. The donor and receptor surfaces must be in intimate contact.
- (2) The donor is then exposed in a pattern with the laser beam. The result is a release of the transfer layer (light-emitting materials) from the donor interface and adhesion of the transfer layer to the receptor interface.
- (3) The used donor is peeled away and discarded. The film in exposed regions is transferred to high-resolution stripes and the performance of the device is as good as an evaporated small-molecule device. Three donor films (red, green, and blue) are used sequentially to create a full color display. LITI transfer is a laser-addressed imaging process and has unique advantages such as high-resolution patterning, excellent film thickness uniformity, multi-layer stack ability, and scalability to large-size mother glass.

Samsung SDI introduced a high-resolution AMOLED panel by utilizing LITI technology. The specification as well as the image sample of the panel are indicated in Figure 14.12, below [31]. The

Table 14.2 Power consumption comparison between RGB and RGBW formats. In all cases, the target color temperature is 6500 K, the luminance is 100 cd/m², and the calculations include a circular polarizer with 44% transmittance.

WOLED structure	Emitter combination	Efficiency (cd/A)	CIE	RGBW avg. power (mW)	RGB avg. power (mW)
White 1	BlueX + RedX	11.3	(0.319, 0.326)	137	280
White 2	BlueX + YD3	15	(0.318, 0.434)	318	387
White 3	BD2 + YD3	11.2	(0.314, 0.327)	137	328
White 4	BD3 + RedX	6.2	(0.329, 0.217)	466	566
White 5	BD3 + YD3	10.4	(0.313, 0.281)	191	305

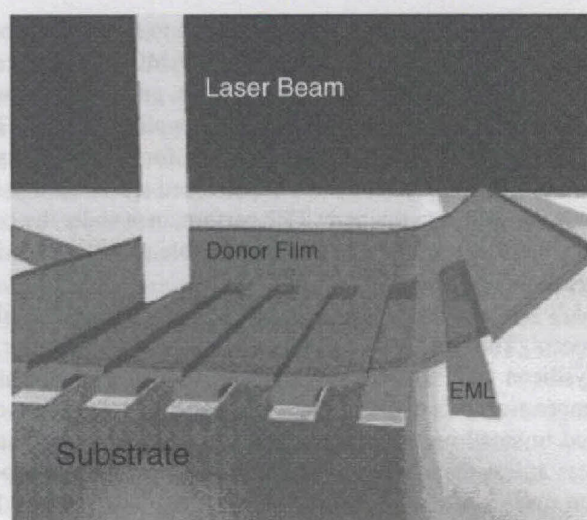


Figure 14.11 Illustration of LITI process.

developed display features a 2.6" diagonal size and $28\mu\text{m}$ (302 ppi) sub-pixel pitch with 40% emission aperture, which make it the highest resolution AMOLED display to date. The white CIE coordinates of the panel are $x=0.31$, $y=0.31$, and the peak luminance is 200 cd/m^2 with 74.1% NTSC color saturation.

14.3 Backplane for AMOLED Display

An OLED, like a liquid crystal display (LCD), is driven by a thin-film transistor (TFT) to achieve high resolution and high display quality. However, the basic theory driving OLEDs and LCDs is quite different: the latter is driven by a voltage while the former is operated by a current supply.

	Specification
Display size	2.6-inch diagonal
Number of pixels	480 x RGB x 640
Pixel pitch	$28\mu\text{m} \times 84\mu\text{m}$
Pixels per inch	302 ppi
Aperture ratio	40%
Pixel circuit	Voltage programming type
Pixel structure	6TFT + 1Capacitor
Emission type	Top emission
Brightness	200 cd/m^2
Color Coordinates	White (0.31, 0.31)
	Red (0.67, 0.32)
	Green (0.30, 0.65)
	Blue (0.15, 0.15)



Figure 14.12 Specification of, and picture on, an AMOLED display using LITI technology.

a-Si TFT has been used extensively in LCD applications due to its simple process and scalability. It is therefore a natural consideration to evaluate a-Si TFT for AMOLED applications. In the voltage-driven LCD applications, the TFT is only used as a switch and a-Si performance is capable of delivering this function. However, for current-driven OLED applications, the TFT needs to act as a current source, to deliver the required current level accurately for different gray levels or luminance. Many technical difficulties and challenges have been experienced and studied using a-Si TFT [32–34]; the most challenging course for a-Si is to maintain TFT performance under the continuous current flow conditions. Until now, a-Si has not seemed to offer any reliable answer. We will review and discuss TFT performance in the following sections.

As its name suggests, low-temperature polysilicon (LTPS) is polycrystalline silicon that is fabricated by a low-temperature process. The so-called ‘low temperature’ is only a relative term when compared to high-temperature polysilicon (HTPS) which is typically formed at temperatures of 800–1000°C. Because of the high-temperature process, HTPS needs to utilize expensive quartz as a substrate, therefore HTPS is limited to small panel applications (<1’). On the other hand, LTPS is generally manufactured by a process at less than 600°C, which is well below the strain point of glass, thus the glass used for polysilicon manufacturing is compatible with the inexpensive glasses that are widely used by the a-Si TFT-LCD industry. Moreover, peripheral circuit integration and a compensation circuit can be fabricated in LTPS due to its high mobility and better performance characteristics. System-on-glass is therefore becoming feasible, and has been realized utilizing LTPS technology [35].

LTPS has proved to be the only technology able to drive OLED and give rise to good reliability; however, LTPS does have issues of its own, luminance ‘non-uniformity’ being a general concern that needs a better solution. Various approaches from industry to tackle non-uniformity issues will be described in the following sections.

14.3.1 Comparison of a-Si TFT and LTPS TFT for AMOLED

LTPS TFT and a-Si TFT have been studied widely as suitable choices for an AMOLED backplane. Table 14.3 shows a comparison of LTPS and a-Si TFT technologies for AMOLED backplane applications.

Table 14.3 Comparison of LTPS TFT and a-Si TFT in AMOLED backplane technology.

	LTPS TFT	a-Si TFT
Device performance	Excellent	Poor
Process complexity	High	Low
Large-size capability	Medium	High
Device reliability	Good	Bad
High-resolution capability	Good	Bad

The process steps in a-Si TFT fabrication are around six photolithography steps for AMOLED applications, and the process temperature is under 400°C. Because of the low temperature and simple process, a-Si TFTs are easy to scale up in manufacturing. Today, Gen 7 glass size equipment is in production, and Gen 8 is in planning. On the other hand, LTPS TFT manufacturing needs a higher process temperature, more complicated process steps, and it is therefore difficult to use glass larger than Gen 5 due to the unavailability of certain equipment, such as laser annealing and ion doping machines. Nevertheless, the device performance of poly-Si TFTs is very much better than that of a-Si TFTs. LTPS is fabricated from the crystallization of an a-Si film by excimer laser annealing or by furnace annealing. This crystallization process changes the disordered, defect-abundant a-Si film to a

more organized polycrystalline silicon film. As a result, device performance is greatly improved, making it suitable for realizing AMOLED displays.

Figure 14.13 shows the transfer curves of a poly-Si TFT and an a-Si TFT. The Poly-Si TFT exhibits a steep increased performance in the sub-threshold region and a higher driving current in the turn-on (or saturation) region. The device characteristics of LTPS TFTs and a-Si TFTs are illustrated in Table 14.4. It is apparent that the electron mobility of LTPS TFTs is $300 \times$ that of a-Si TFTs. The high driving current capability of poly-Si TFTs implies that there is potential for a smaller device in the pixel circuit. Using a small-size device can increase the aperture ratio of the sub-pixels, thus AMOLED lifetime and/or luminance can be significantly improved. High driving capability also makes peripheral circuit integration on glass feasible. We can also see from Table 14.4 that there is a large difference in threshold voltage (V_{th}); the low threshold voltage characteristics of LTPS mean AMOLED displays can offer lower power consumption.

For the reliability study, a-Si TFT and LTPS TFT devices were investigated under DC bias stress conditions. Figure 14.14(a) shows the a-Si TFT transfer characteristics under DC bias stress with $V_{ds}=15$ V, and $V_{gs}=9$ V for 40,000 seconds. The variations of threshold voltage and on-current (I_{on}) are shown in Figure 14.14(b). The threshold voltage shift is as large as 0.95 V during the stress period; it resulted in more than 30% variation in the driving current. In other words, the luminance change will be up to 30% during a-Si device operation without even considering the decay occurring in the OLED

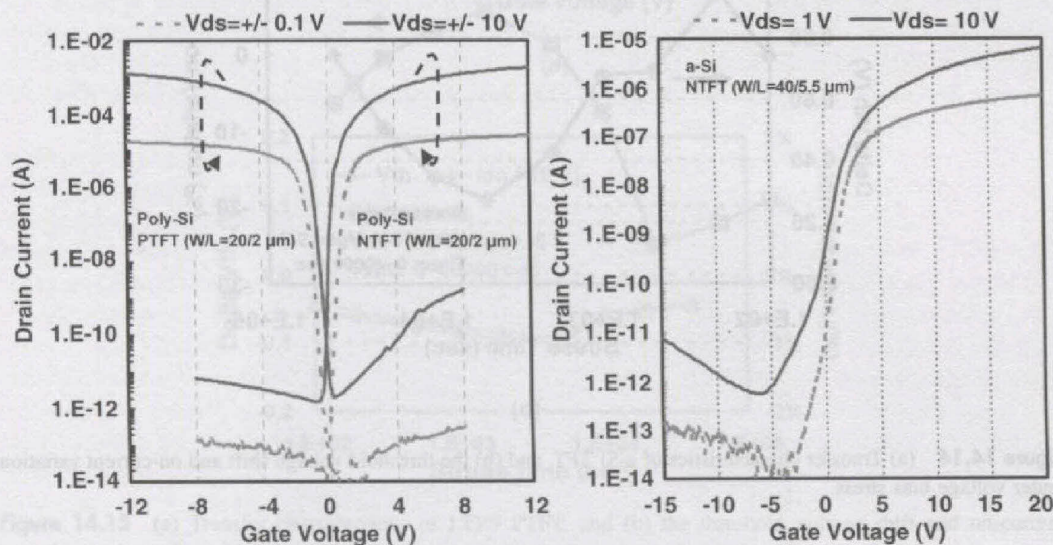
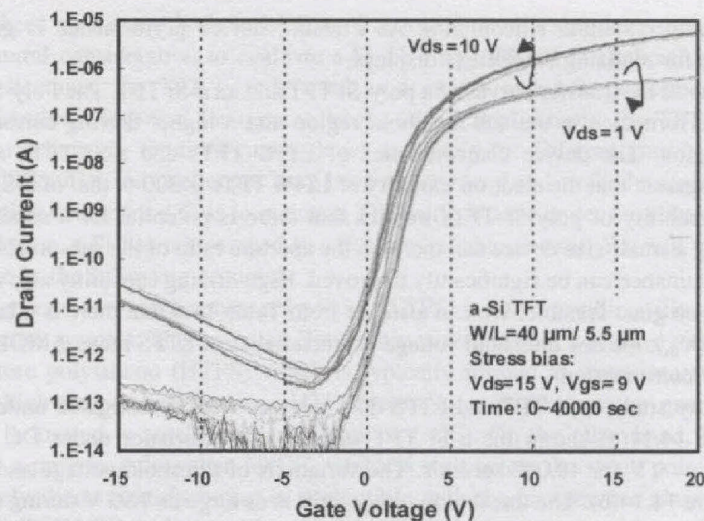


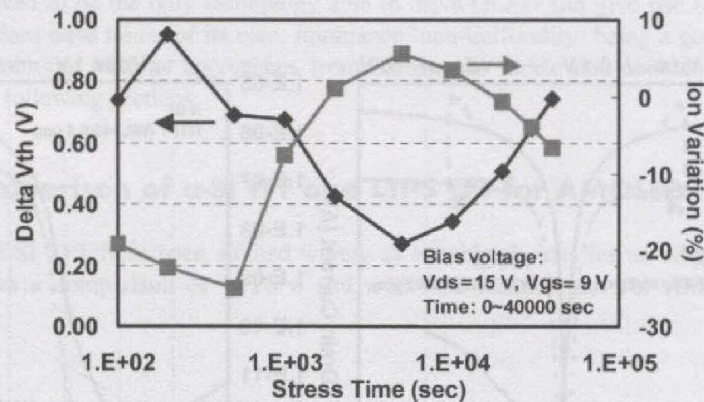
Figure 14.13 Transfer characteristics of LTPS TFT and a-Si TFT.

Table 14.4 Device characteristics of LTPS and a-Si TFTs.

	LTPS NTFT	LTPS PTFT	a-Si TFT
	W/L = 20 μ m/2 μ m		W/L = 40 μ m/5.5 μ m
V_{th} (V)	0.56	-1	1.85
SS (V/dec)	0.15	0.15	0.76
Mobility ($\text{cm}^2/\text{V}\cdot\text{s}$)	107.5	84.8	0.3



(a)



(b)

Figure 14.14 (a) Transfer characteristics of a-Si TFT, and (b) the threshold voltage shift and on-current variation under voltage bias stress.

device. Therefore an a-Si driven AMOLED panel will suffer serious reliability issues: the luminance or even the white point of the display changes with the time of device operation, and this decay occurs quickly from the initial stage of display utilization.

In contrast to an a-Si TFT, there is no noticeable reliability issue for the LTPS p-type TFT. Figure 4.15(a) shows the LTPS PTFT transfer characteristics under DC voltage bias stress with $V_{ds} = -10$ V, and $V_{gs} = -5$ V for 40,000 seconds. In contrast to the split curves in the a-Si case, the I-V curves for LTPS TFT during the stress period are almost all overlapped. Only small threshold voltage (V_{th}) shift and I_{on} variation are observed in Figure 14.15(b). It is obvious that I_{on} varied by less than 1% during the entire stress period, while V_{th} shifts by less than 0.1 V. The degradation of the LTPS device is almost negligible and thus it is reliable for the AMOLED applications.

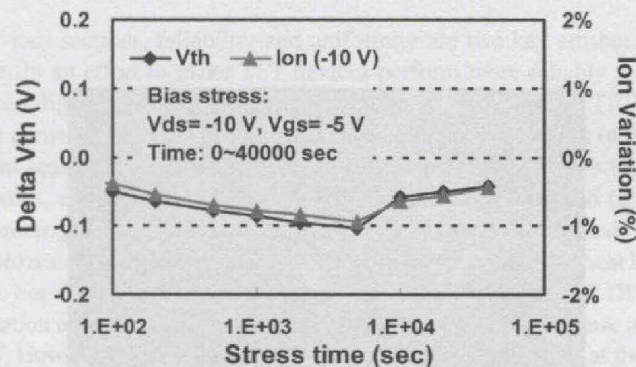
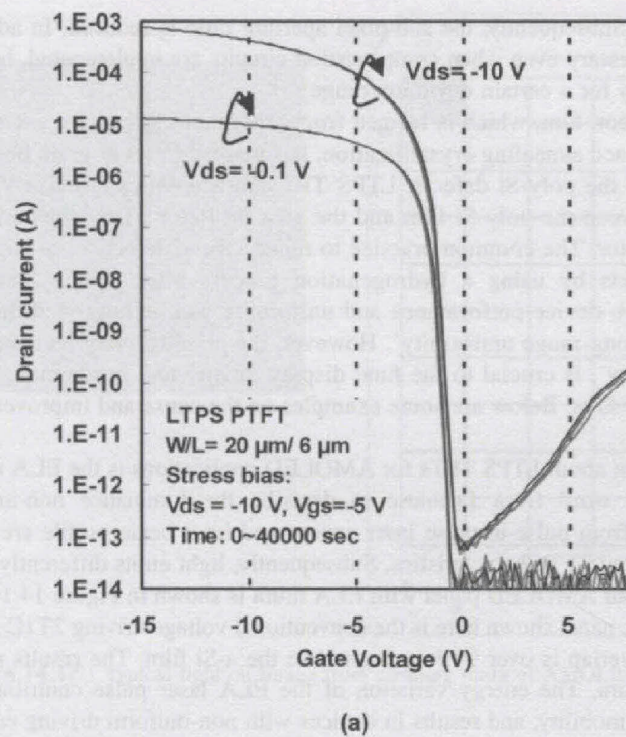


Figure 14.15 (a) Transfer characteristics of LTPS PTFT, and (b) the threshold voltage shift and on-current variation under voltage bias stress.

14.3.2 TFT Uniformity Issues in AMOLED Applications

It is well known that the display luminance non-uniformity on AMOLED panels generally results from variation of the backplane. Although the LTPS TFT device is capable of driving an OLED device, the pixel-to-pixel level device variation is the key issue that makes the AMOLED panel a concern for certain applications. In order to solve this issue, several pixel compensation circuits for AMOLED applications have been proposed, which include the threshold voltage compensation circuit, current copy, current mirror, and pulse width modulation [36–39]. Most of the compensation circuits can greatly improve the luminance uniformity, but, nevertheless, complicated pixel circuits require more

TFTs and capacitors. Subsequently, the sub-pixel aperture ratio is reduced. In addition, good device uniformity is still necessary even when compensation circuits are implemented, because the compensation is effective only for a certain deviation range.

Polycrystalline silicon film, which is formed from amorphous silicon by excimer laser annealing crystallization or furnace annealing crystallization, has many defects at grain boundaries and within grains. In addition to the poly-Si defects, LTPS TFT characteristics are also very sensitive to the interface defects between the poly-Si film and the gate insulator where the carriers transfer in the channel of the transistor. The common practice to reduce these defects is to passivate the dangling bonds of these defects by using a hydrogenation process after device fabrication. After this hydrogenation process, device performance and uniformity can be improved throughout the whole glass, the so-called 'long-range uniformity'. However, the pixel-to-pixel level uniformity, so-called 'short-range uniformity', is crucial to the final display quality and needs more technical tuning to achieve satisfactory results. Below are some examples on the cause and improvement of short-range uniformity.

The greatest concern about LTPS TFTs for AMOLED applications is the ELA mura (a well-known and extensively used word from Japanese to describe the luminance non-uniformity, so-called 'MURA'). Variations from pulse-to-pulse laser energy and laser beam profile are the main causes of variation in the localized TFT characteristics. Subsequently, light emits differently in these areas. One typical example from an AMOLED panel with ELA mura is shown in Figure 14.16. The pixel driving scheme for the specific panel shown here is the conventional voltage driving 2T1C PMOS design. ELA laser pulse-to-pulse overlap is over 90% to crystallize the a-Si film. The results show apparent ELA pulse-to-pulse line mura. The energy variation of the ELA laser pulse contributes to the different threshold voltage and mobility, and results in devices with non-uniform driving capability. Therefore, knowing how to stabilize the output energy of each laser pulse is key to reducing this kind of mura on AMOLED panels.

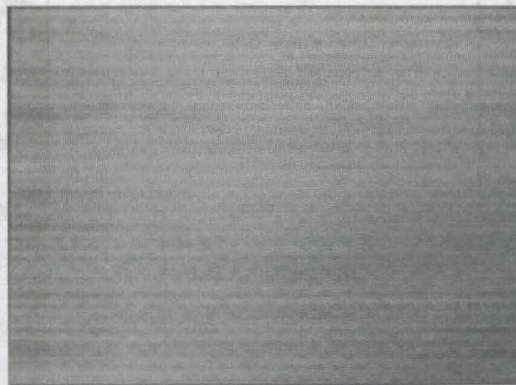


Figure 14.16 A typical light-on image from ELA mura of AMOLED panel.

Besides the crystallization process of a-Si film, the cleaning process is also critical to the luminance uniformity of an AMOLED display. Figure 14.17 below shows the typical cleaning mura on AMOLED panels. The distribution of this type of cleaning mura is also shown in Figure 14.16. Although the luminance non-uniformity is severe, there is no significant difference in device characteristics between regions that displayed normally and abnormally (mura area). This type of cleaning mura comes from contamination in the drying step of the specific cleaning process; better control of the drying recipe can eliminate this mura.

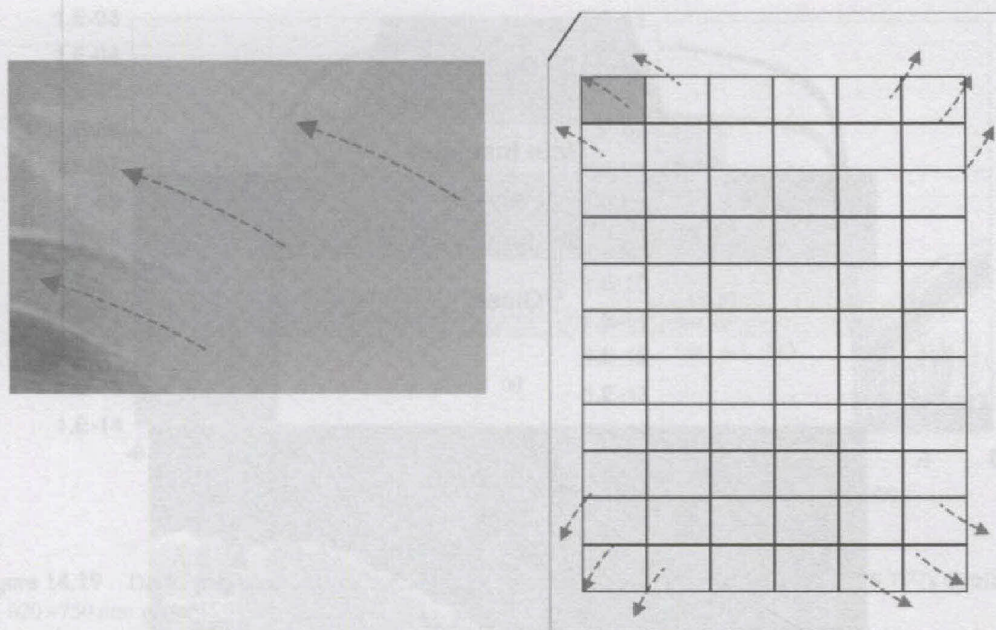


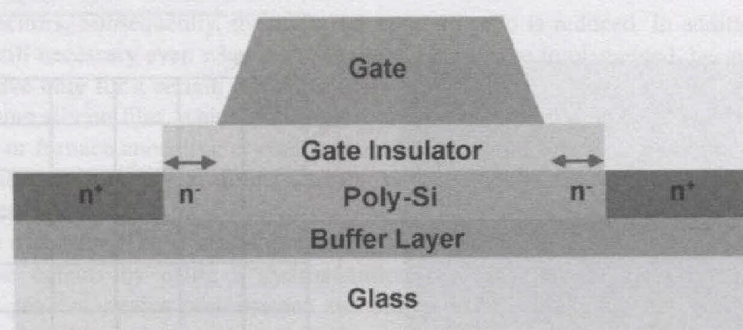
Figure 14.17 Typical light-on image from cleaning mura of AMOLED panel.

14.3.3 Advanced Device for AMOLED Applications

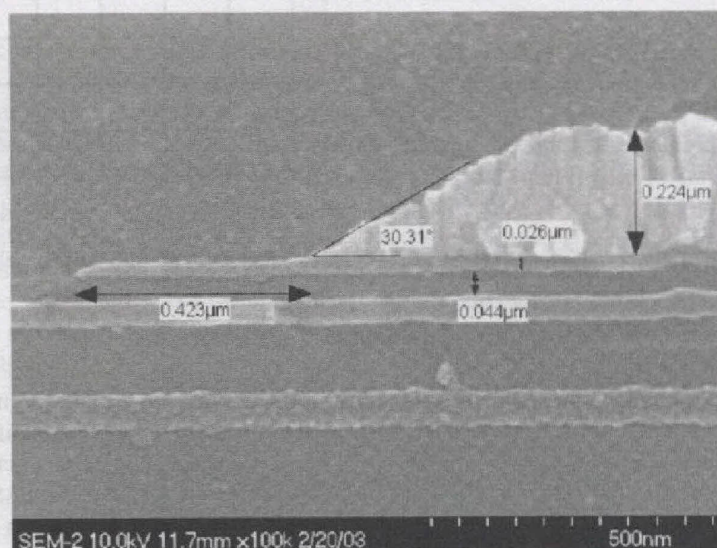
As discussed in previous sections, reliability and uniformity are two key attributes to make AMOLED displays competitive. In an effort to make TFT devices perform more reliably and uniformly, we have developed a fully self-aligned symmetric (FASt) lightly doped drain (LDD) TFT structure [40, 41]. In comparison with the conventional semi self-aligned LDD structure, the length of the FASt LDD is much easier to control, and scale down in LTPS production, which results in more uniform and stable TFT electrical characteristics, especially for small-size TFTs. Figures 14.18(a) and (b) below show the TFT structure and SEM micrograph of the FASt LDD. The LDD length is controlled by the gate metal side-etching time and photo resist profile, so that it is not constrained by photo-alignment limitations and is much easier to scale down. For a conventional LDD process approach, the length of LDD is usually larger than $1\text{ }\mu\text{m}$ due to the limitation of photo alignment for large-size glass, which will cause a large series resistance for a small-size TFT. However, the length of the FASt LDD is easy to control at the sub-micron level.

In order to enhance the TFT performance, the device's physical size, such as gate insulator thickness and channel length, is shrunk along with the FASt LDD structure. Figure 14.19 below shows the transfer characteristics of 24 n-channel and p-channel FASt LDD LTPS TFTs distributed on $620\times 750\text{ mm}$ glass. Table 14.5 shows the statistical electrical characteristics of FASt LDD LTPS TFTs. These TFTs show good and uniform electrical characteristics, such as low threshold voltage and small sub-threshold swing, and are suitable for high-speed and low-power circuitry. They also show promise in pixel circuits for AMOLED displays.

Figure 14.20 below shows the transfer curve transformation of a $2\text{ }\mu\text{m}$ conventional TFT with $1.5\text{ }\mu\text{m}$ LDD length and a $2\text{ }\mu\text{m}$ FASt TFT with $0.5\text{ }\mu\text{m}$ LDD length under hot carrier stress (HCS). The drain avalanche hot carrier (DAHC) stress – which has been reported as the severest condition in the LTPS TFT reliability test [42, 43] – is used to evaluate the reliability of the LTPS TFT. To accelerate the degradation rate, the stress drain voltage is 4 V higher than the operating voltage $2V_{DD}$, and the stress gate voltage is $V_{th}+1\text{ V}$. It is obvious that conventional LDD TFTs suffer severe hot carrier stress degradation. State creation is generated at the high field drain junction region because of the short channel effect. Therefore, mobility and on-current ($V_{ds}=0.1\text{ V}$) degrade seriously in conventional LDD



(a)



(b)

Figure 14.18 (a) TFT structure and (b) SEM micrograph of FAST LDD.

TFTs due to these created defects in the upper half of the band gap. Compared to the conventional LDD TFTs, FAST TFTs show better HCS endurance in the mobility and on-current parameters.

Table 14.6 shows the degradation of electrical characteristics of LTPS TFTs under 100 second DAHC stress. The results show good stress endurance of FAST LDD LTPS TFTs in comparison with general LDD LTPS TFTs, even with a smaller physical size. The high reliability of FAST LDD LTPS TFTs is attributed to the elaborate engineering of the doping process for LDD and the source/drain.

14.4 AMOLED Pixel Circuit Design

14.4.1 Pixel Circuit

LTPS was considered mandatory for AMOLEDs because it has the advantages of higher driving capability, superior reliability, and higher thermal endurance compared to a-Si [44]. However, the non-uniformity caused by LTPS process variations [45] as well as its high-cost technology impede large-panel

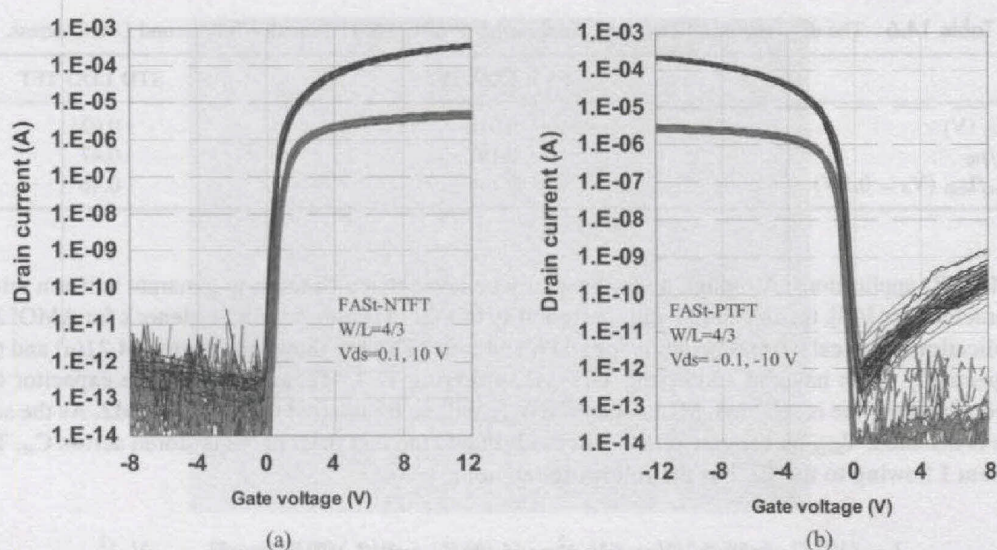


Figure 14.19 The transfer characteristics of 24 (a) n-channel and (b) p-channel FASt LDD LTPS TFTs distributed on 620×750 mm glass.

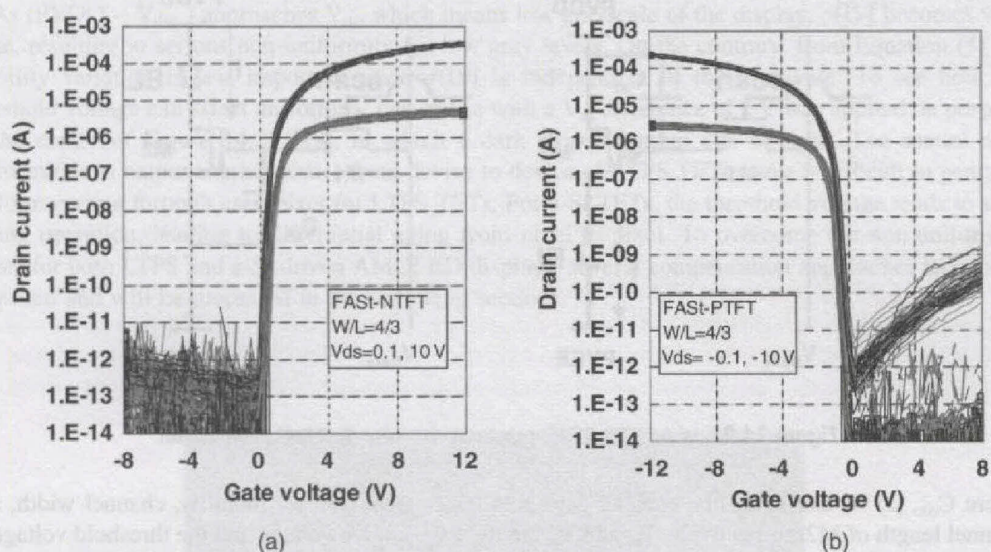


Figure 14.20 The transfer curve of the (a) conventional and (b) FASt TFT with channel length = 2 μm before and after hot carrier stress. The stress conditions are $V_{gs} = V_{th} + 1$ V and $V_{ds} = 10$ V for $t = 0 - 100$ s.

Table 14.5 The statistical electrical characteristics of FASt LDD LTPS TFTs.

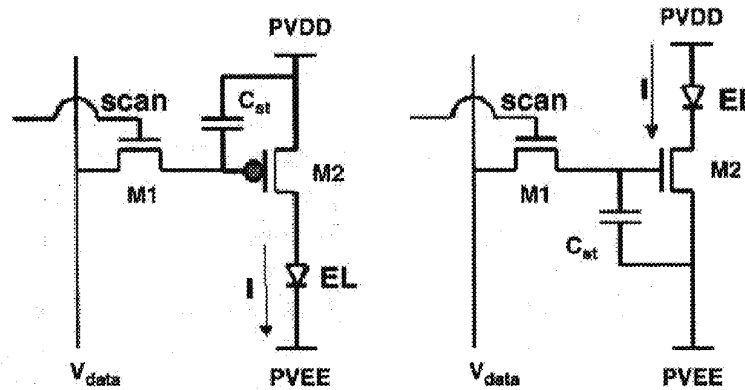
	N-channel TFTs		P-channel TFTs	
	AVG	STDEV	AVG	STDEV
V_{th} (V)	0.71	0.09	-0.96	0.07
SS (V/dec)	0.16	0.02	0.15	0.03

Table 14.6 The degradation of electrical characteristics of LTPS TFTs under 100 second DAHC stress.

	FASi LDD TFT	STD LDD TFT
ΔV_{th} (V)	0.018	0.025
$\Delta \mu/\mu_0$	0.19	0.47
$\Delta I_{on}/I_{on0}$ ($V_d = 0.1$ V)	0.14	0.48

AMOLED applications. Although it was generally believed that a-Si tends to generate uniform initial characteristics [46], the instability and low mobility of a-Si [47] have been a bottleneck for AMOLED applications. Typical 2T pixel circuits for LTPS and a-Si TFTs are shown in Figures 14.21(a) and (b), respectively. Both have an addressing TFT M1, a driving TFT M2, and one storage capacitor C_{st} . When the scan line is selected, M1 is open and V_{data} will be transferred to the gate of M2. As the scan line is disabled, V_{data} on the gate of M2 still holds due to the fact that charge is stored across C_{st} . The current I flowing to the EL has the following relation:

$$I = (1/2) C_{ox} (\mu W/L) (V_{gs} - V_{th})^2 = (1/2) C_{ox} (\mu W/L) (PVDD - V_{data} - V_{th})^2 \quad (3)$$

**Figure 14.21** (a) LTPS 2T1C pixel circuit; (b) a-Si 2T1C pixel circuit.

where C_{ox} , μ , W , and L are the channel capacitance per area, channel mobility, channel width, and channel length of M2, respectively. V_{gs} and V_{th} are the gate-source voltage and the threshold voltage of M2, respectively. PVDD is changed to PVEE in Equation (3) if the a-Si pixel circuit is referred to.

Since the OLED is a current-driven device, the brightness uniformity over the panel is susceptible to variations in device characteristics of TFTs and EL itself. However, the EL process can be well controlled and uniformity of EL is not a big issue. Figure 14.22 below gives one example showing the front-of-screen non-uniformity of the brightness for the LTPS-driven AMOLED display [48]. The non-uniformity is attributed mainly to the ELA, cleaning, and CVD process of LTPS. Equation (3) indicates two factors of TFTs that influence the uniformity: the mobility and threshold voltage. By simple calculation, it can be shown that the percentage current variation $\sigma(I)/I$ with respect to the threshold voltage variation $\sigma(V_{th})$ and mobility $\sigma(\mu)$ are given by

$$\sigma(I)/I = -2\sigma(V_{th})/(PVDD - V_{data} - V_{th}) \quad (4)$$

$$\sigma(I)/I = \sigma(\mu)/\mu \quad (5)$$

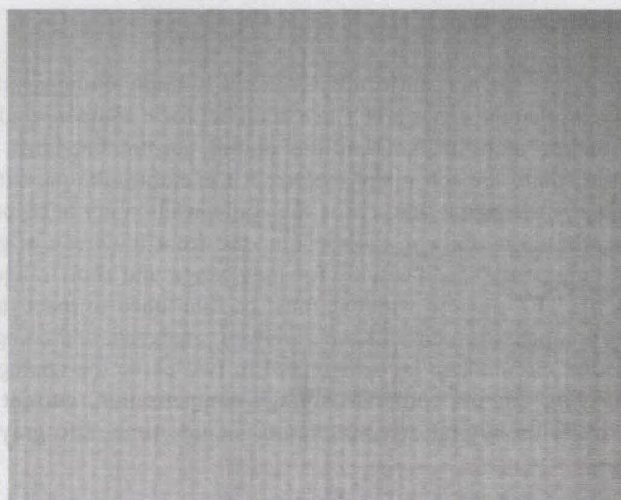


Figure 14.22 Image showing the non-uniformity brightness.

As $(V_{DD} - V_{data})$ approaches V_{th} , which means low grayscale of the display, $\sigma(I)/I$ becomes very large, resulting in serious non-uniformity for low gray levels. On the contrary, from Equation (5) the mobility variation is less important since $\sigma(I)/I$ is independent of the grayscale. To see how the threshold voltage can affect uniformity, one image with a V_{th} difference of 1 V was applied on purpose in the center of Figure 14.23 [49], in which a dark striped pattern can be seen. The spatial non-uniformities in output characteristics from device to device of LTPS TFTs make it difficult to generate uniform current through each pixel for LTPS TFTs. For a-Si TFTs, the threshold voltage tends to shift during operation, leading to differential aging from pixel to pixel. To overcome the non-uniformity issues for both LTPS and a-Si driven AMOLED displays, several compensation approaches have been proposed and will be discussed in the following sections.

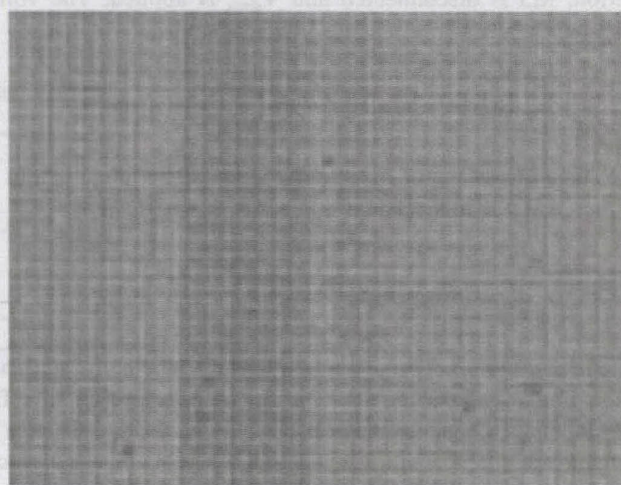


Figure 14.23 A dark striped pattern can be seen in accordance with the 1 V difference of V_{th} .

14.4.1.1 Pixel Compensation

One of the solutions to tackle the non-uniformity issues is to apply compensation circuits in every pixel. Compensation means that the driving TFT in a pixel has to be compensated for parameters such as threshold voltage and/or mobility, so that the output current becomes independent of the parameters. In real cases, there are too many factors; for example, the parasitic effects and load-dependent RC time delay of the signal lines cause the compensation not to be perfect. The more the circuit can compensate, the more uniform will become the front-of-screen brightness of the panel. Since every panel has uniformity specifications for long range and short range, the compensation circuits, together with the TFT process window, must be fine-tuned to meet them. In this section, several published pixel compensation circuits are reviewed, analyzed, and compared.

The pixel compensation circuits can be categorized in two parts: the analog and digital driving circuits. The analog driving circuits comprise voltage compensation, current compensation, and hybrid compensation, while the digital driving circuits include time-ratio grayscale and area-ratio grayscale.

14.4.1.2 Analog Driving Circuits

By analog driving circuits we mean that the grayscale is defined by the data signal, either voltage or current. Figures 14.24(a) and (b) show typical data signals versus grayscale in the 2T pixel (Figure 14.21) for data voltage and data current, respectively. Note that a gamma factor equal to 2.2 is applied in Figure 14.24. Suppose there are 256 grayscales for each color; there should be 256 corresponding V_{data} or I_{data} .

14.4.1.3 Voltage Compensation

Dawson *et al.* [50] from the Sarnoff Corporation proposed a voltage-driven pixel compensation circuit which contains four transistors and two capacitors. The circuit and its corresponding timing are shown in Figure 14.25 below. The additional transistors, M3 and M4, automatically zero the threshold voltage of the driving transistor, M2. During this period, M4 turns off and M3 turns on. M2 and M3 form a diode-connected structure and the disconnection of M4 forces the voltage at the gate of M2 to be $V_g = V_{DD} - V_{th}$. V_{th} is the threshold voltage of M2. Now the voltage across the capacitor C1 is V_{th} . In the second period, M3 is disconnected and V_{data} is applied. The voltage across C1 now becomes

$$(V_{DD} - V_{data}) \times C2 / (C1 + C2) + V_{th} \quad (6)$$

Equation (6) is the voltage across V_{gs} of M2. From (3), it can be found that in the emission period, the current flowing to the OLED is independent of V_{th} of M2 and is given by

$$I = (1/2)C_{ox}(\mu W/L)\{(V_{DD} - V_{data}) \times C2 / (C1 + C2)\}^2 \quad (7)$$

The improvement in the pixel-to-pixel brightness uniformity is demonstrated in Figure 14.26 below. After compensation, the image becomes more uniform, and according to ref. [50], the standard deviation of the pixel luminance changes from 16.1% (2T) to 4.7% (4T) at a panel luminance of 15 cd/m². This is a simple example of a voltage-controlled pixel compensation circuit, and the basic principle is the diode-connected structure to sense and store the threshold voltage of the driving TFT. Although there are many voltage-driven compensation circuits with 4–6 transistors and 1–2 capacitors,

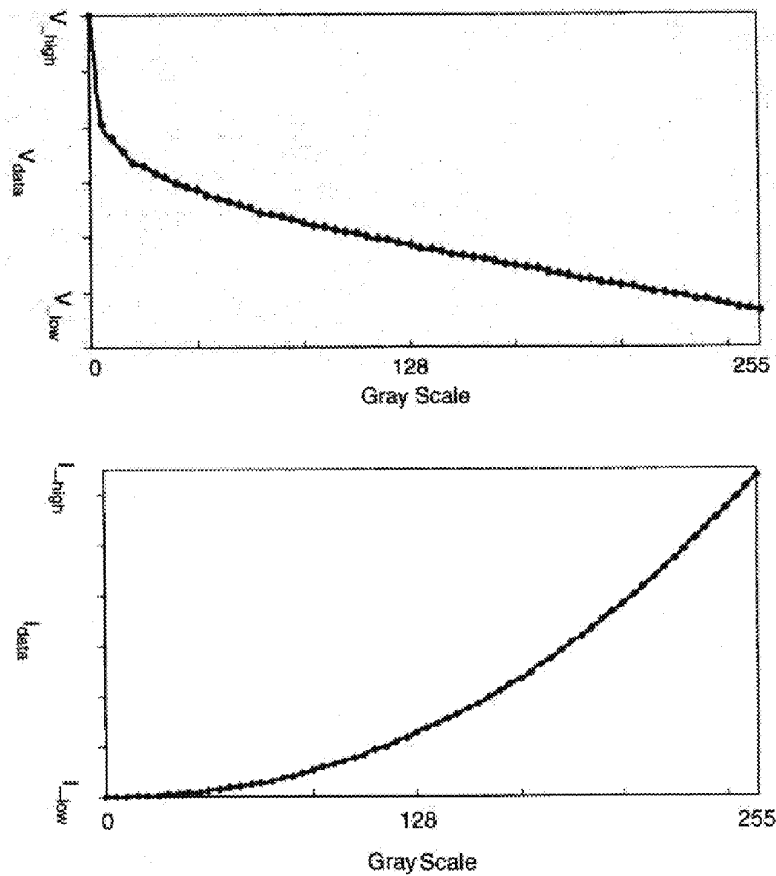


Figure 14.24 (a) V_{data} with respect to the grayscale for a voltage-driven pixel; gamma has been considered. (b) I_{data} with respect to the grayscale for a current-driven pixel; gamma has been considered.

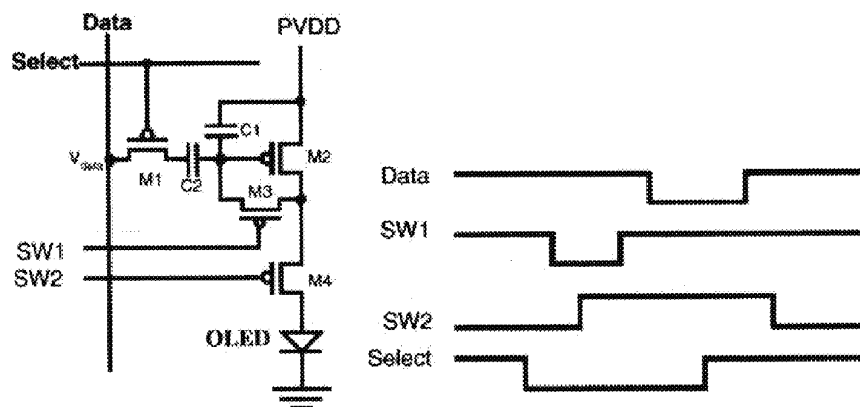


Figure 14.25 The 4T2C voltage-driven pixel compensation circuit and its timing.

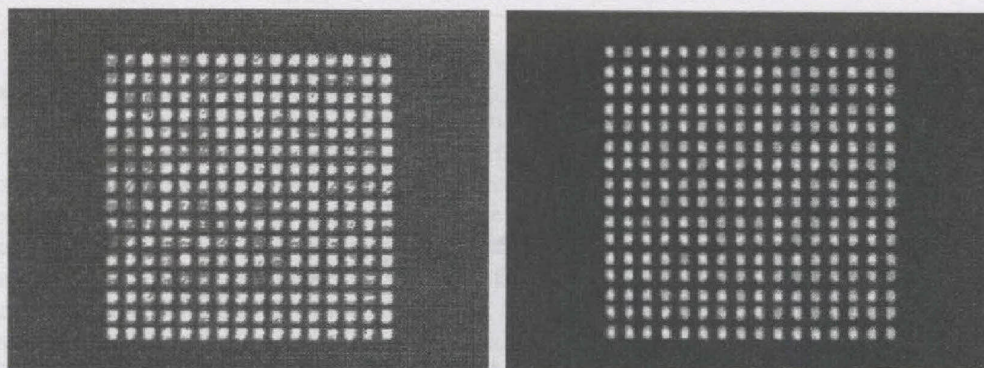


Figure 14.26 Comparison of the light-on results before and after correction.

they follow the same basic principle. From a design point of view, fewer control lines and power lines are preferred for a compensation circuit in one limited pixel size and, moreover, easier operation of the pixel is also desired.

Ono *et al.* [51], from IDT, proposed a voltage-controlled 4T1C pixel circuit for an a-Si AMOLED. Figure 14.27 shows the proposed pixel circuit and its corresponding timing. There are four control lines: MRG, RST, SCT, and COM. These control lines can be generated externally in the driver IC or power IC. During the compensation cycle, the OLED device serves as a capacitor, C_{OLED} . The pixel operation can be divided into four periods, as indicated in the timing in Figure 14.27. The operation of each period will be analyzed as follows:

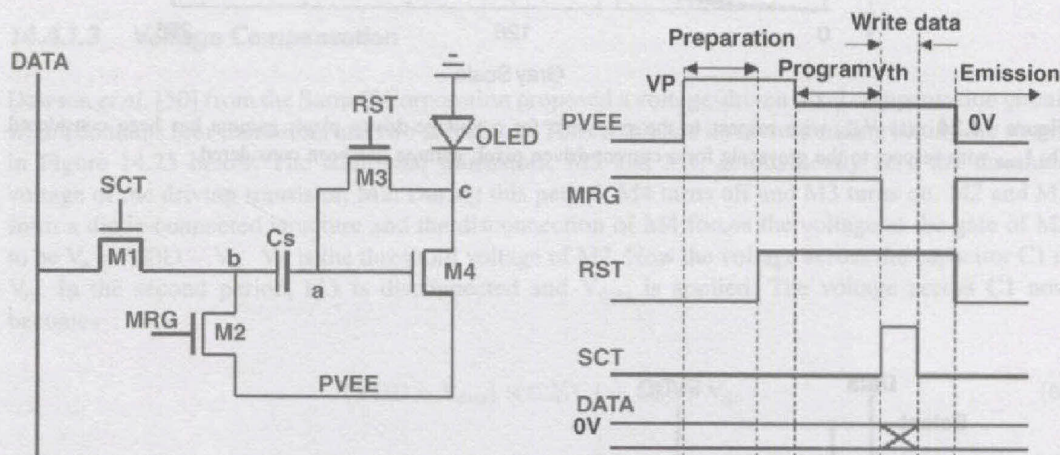


Figure 14.27 The 4T1C voltage-driven pixel compensation circuit for a-Si TFT and its corresponding timing.

- (1) *Preparation*: The purpose of this period is to prepare the voltage at some nodes for programming V_{th} . The voltage of the COM line rises to some voltage level, e.g. V_p , and the voltage at node B (V_b) will become V_p as well. The voltage at node A (V_a) becomes higher than V_p due to the fact that in the emission period from the last frame, V_a was higher than that at V_b . If V_p is higher than V_{th} of T4, T4 would conduct reversely, i.e. current would flow from the COM line to ground. At the end of the preparation period, the voltage at node C (V_c) approaches V_p since very low current is flowing. The turn-on of T3 turns off T4 and V_a equals V_c .

(2) *Program V_{th}* : The voltage at the COM line changes from V_p to ground, 0 V. T4 turns on and serves as a diode-connected structure, and C_s is charged to V_{th} of T4. V_a and V_c now become V_{th} at the end of the V_{th} programming period.

(3) *Write data*: $-V_{data}$ is written from the DAT line and V_b equals $-V_{data}$. Now $V_a = V_c$ becomes

$$-V_{data} \times C_s / (C_s + C_{oled}) + V_{th} \quad (8)$$

The V_{gs} of T4 is the voltage $V_a - V_b$ and is expressed as follows:

$$V_{data} \times C_{oled} / (C_s + C_{oled}) + V_{th} \quad (9)$$

In the last period,

(4) *Emission*: The current flowing to the OLED from Equation (3) is

$$I = (1/2)C_{ox}(\mu W/L)(V_{data} \times C_{oled} / (C_s + C_{oled}))^2 \quad (10)$$

Equation (10) is independent of V_{th} of the driving TFT. Figure 14.28 depicts the simulation results and Figure 14.29 compares the deviation of the drain current for 4T and conventional 2T, with respect to the variation of V_{th} of the driving TFT. The proposed 4T ensures that deviation of the drain current is less than 15% for $dV_{th} = 5$ V. One drawback that has to be mentioned is that a longer time is required in the V_{th} programming period due to the fact that the low driving capability of a-Si TFT has to charge the large OLED capacitance. The longer programming time (~ 3 ms) limits panel operation during one frame. Row by row programming of V_{th} is not possible. The panel frame sequence starts with V_{th} programming for all pixels simultaneously, followed by data writing row by row and then emission. The control lines of MRG, RST, and SCT are easily generated from the external IC; however, the COM power line has three levels of voltage changing alternately, which limits the accuracy of programmed V_{th} resulting from the parasitic capacitor across the gate-source of T4.

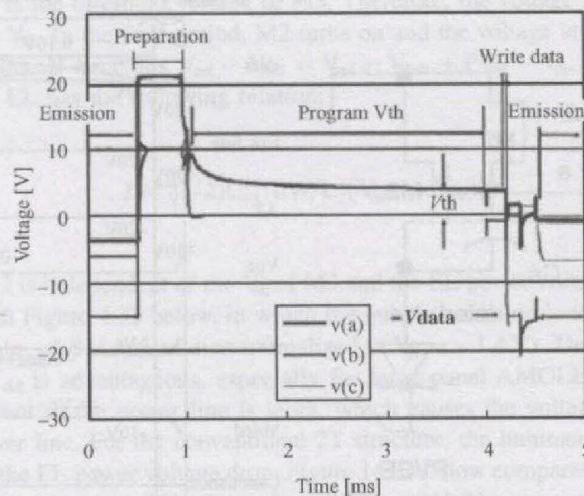


Figure 14.28 Simulation result to show pixel operation.

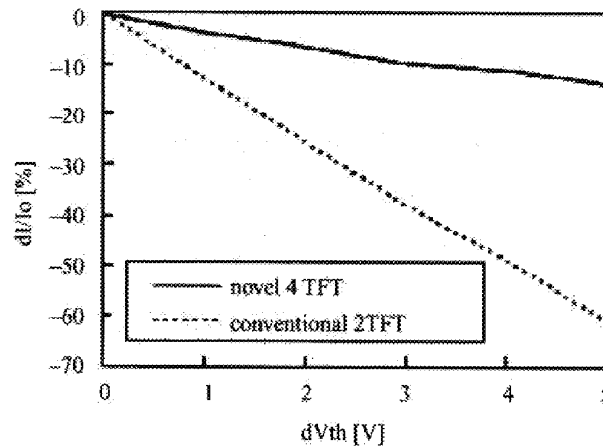


Figure 14.29 Comparison of the deviation of the drain current for 4T and conventional 2T with respect to the variation of V_{th} of the driving TFT.

Sanford and Libsch [52], from IBM T. J. Watson Research Center, proposed a simple V_{th} correcting circuit. Figure 14.30 shows the proposed pixel circuit and its corresponding timing. The circuit is simple with three TFTs, one capacitor, and two control lines. The operating principle is similar to the previous one. One frame is divided into three sections. The first section sets and stores the threshold voltage across the storage capacitor through the diode connection of T3, and therefore V_c equals V_{th} of T3. In the second section, the data is written into the pixel row by row. The voltage across the storage capacitor now becomes $V_{data} \times \{C_{oled}/(C + C_{oled})\} + V_{th}$. In the final emission section, the cathode voltage (V_{ca}) becomes more negative and the current flow into the OLED will be independent of V_{th} of T3. At the beginning of one frame, V_{ca} is high (10 V) for a while, which acts as a preparation period in Figure 14.27. The transistor T2 is only open during the V_{th} programming period to make $V_a = 0$ V, which can also be realized as the row line is selected and make $V_{data} = 0$ V. If such timing is given, T2 can be neglected, leading to a more simplified pixel compensation circuit with only 2T1C.

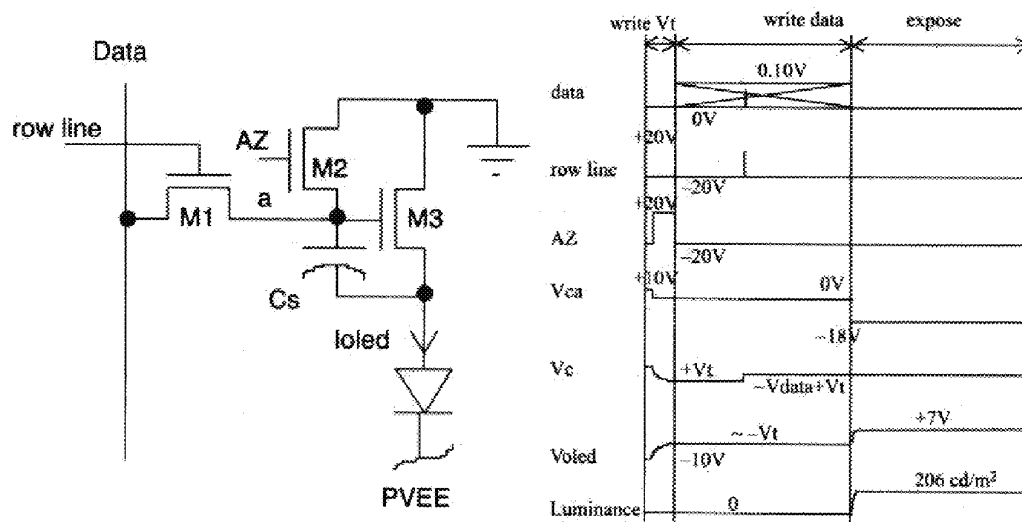


Figure 14.30 The 3T1C voltage-driven pixel compensation circuit and its timing.

The accuracy of the compensation circuit is limited by two factors: the first one results from the parasitic effect when V_{ca} changes from 0 V to -18 V. The voltage across the storage capacitor will be changed. The second factor occurs during the period for data writing. At the end of the V_{th} programming period, the voltage across the OLED is $-V_{th}$. After the V_{data} programming, the voltage across the OLED becomes $V_{data} \times \{C/(C + C_{oled})\} - V_{th}$, which is smaller than 0V for a typical case. Therefore, T3 will conduct to charge up the OLED, and the voltage across the storage capacitor will change. The V_{th} compensation error can be observed in Figure 14.31, in which the luminance difference is 20% for V_{data} higher than 2 V. For V_{data} smaller than 2 V, the pixel circuit may fail to sense the accurate V_{th} . To lower the compensation error, another transistor in series with T3 to block the current during the data writing period is suggested.

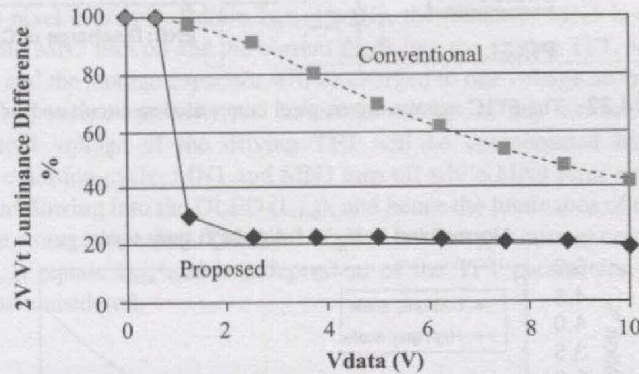


Figure 14.31 Compensation error occurs when V_{data} is smaller than 2 V.

Du-Zen Peng *et al.* [53, 54] from Toppoly Optoelectronics Corp. proposed another pixel compensation circuit, which compensates not only the threshold voltage of the driving TFT, but also the EL power voltage drop on the power lines. The pixel circuit contains five transistors and one capacitor and is shown in Figure 14.32 below together with its corresponding timing. The operation of the pixel is divided into three periods. The first period is to discharge C_{st} in preparation for data loading and programming. The second period loads V_{data} into node A, and meanwhile the driving TFT M3 and M4 form a diode-connected structure and the voltage at node B will be charged to approximately $PV_{dd} - V_{th}$, where V_{th} is the threshold voltage of M3. Therefore, the voltage across C_{st} now becomes $V_{AB} = V_{data} - PV_{dd} + V_{th}$. In the final period, M2 turns on and the voltage at node A equals V_{ref} , and now the voltage at node B becomes $V_{ref} - V_{AB} = V_{ref} - V_{data} + PV_{dd} - V_{th}$. From Equation (3), the current I flowing into EL has the following relation:

$$I = (1/2)C_{ox}(\mu W/L)(V_{data} - V_{ref})^2 \quad (11)$$

Notice that current I is independent of the V_{th} of M3 and the EL power voltage PV_{dd} . The simulation results can be found in Figure 4.33 below, in which the current variation is very small ($< 5\%$) for V_{th} changes from -1.1 V to -1.8 V (calculation normalized to $V_{th} = -1.4$ V). The fact that the EL current is independent of PV_{dd} is advantageous, especially for large-panel AMOLED applications, since in large panels, the current in the power line is large, which causes the voltage drop due to the finite resistance on the power line. For the conventional 2T structure, the luminance and hence uniformity will be influenced by the EL power voltage drop. Figure 14.34 below compares the current variation for 2T and 5T pixel circuits assuming PV_{dd} drops from 10 V to 9 V. The current variation is within 10% even for a 1 V drop of PV_{dd} for the proposed 5T structure.

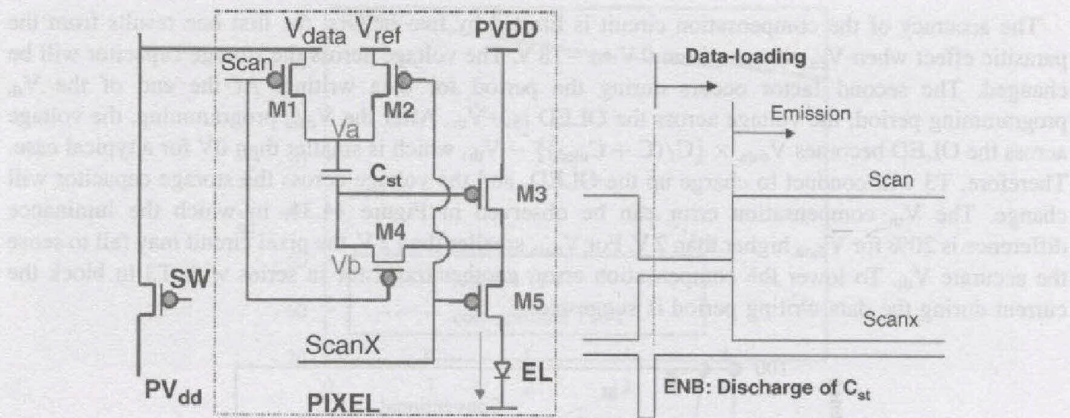


Figure 14.32 The 5T1C voltage-driven pixel compensation circuit and its timing.

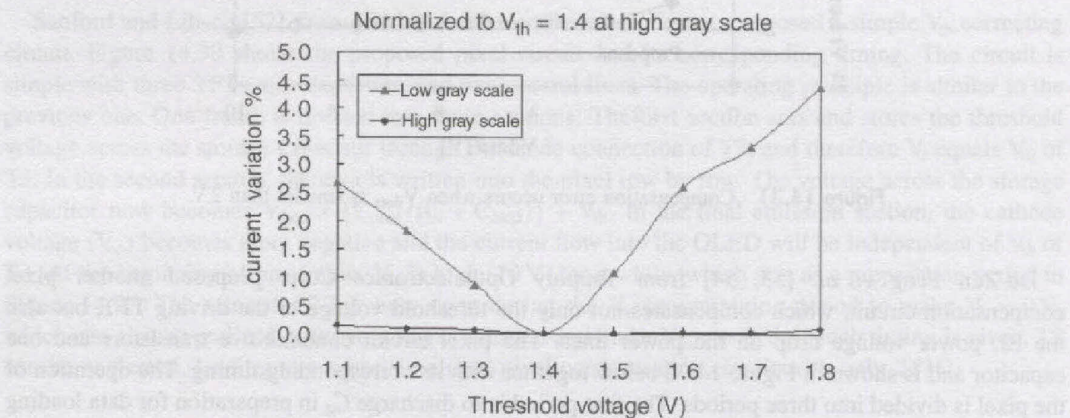


Figure 14.33 Comparison of the current variation for threshold voltage changing from -1.1 V to -1.8 V.

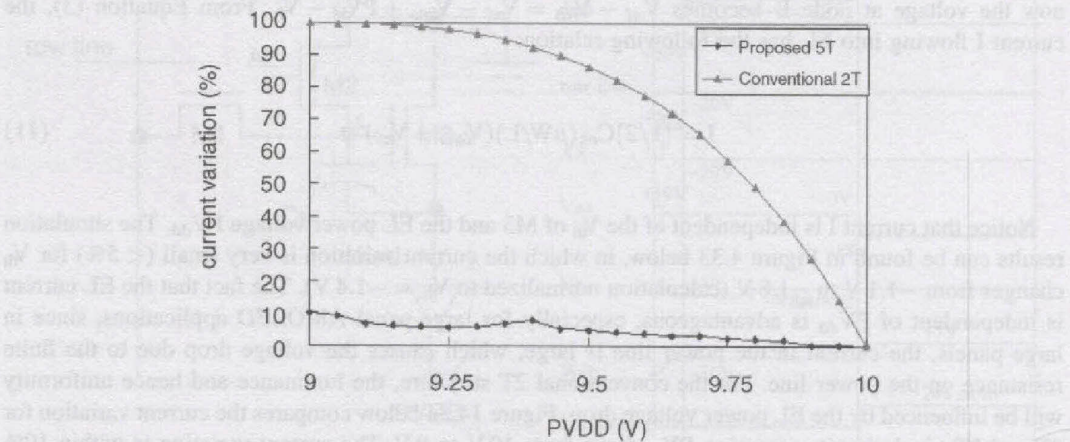


Figure 14.34 Comparison of the current variation for EL power voltage PV_{dd} changing from 10 V to 9 V.

The drawback of the pixel circuit is that only one capacitor is used, and is subject to a feed-through effect easily on node V_b during operation, which may cause voltage deviation on node V_b . This, however, can be recovered if V_{data} is higher than expected, and then the programming of V_{th} will not be influenced by the feed-through effect.

14.4.1.4 Current Compensation

Since the OLED is driven by a current and its luminance is proportional to that current, it is logical to apply current data to the pixel. Dawson *et al.* [55] from the Sarnoff Corporation proposed a current-driving pixel compensation circuit. Figure 14.35 depicts the pixel circuit and its corresponding timing. The operation of the pixel is simple. Before I_{data} is ready, the transistor MN4 is turned off, and when I_{data} is ready, MN1 and MN3 turn on and the current flows into the driving TFT, MN2. MN2 is a diode connection structure and the storage capacitor will be charged to one voltage according to I_{data} , and the characteristics of MN2, such as mobility and threshold voltage. In this manner, the deviation of the mobility and threshold voltage of the driving TFT will be compensated by the voltage across the capacitor. In the emission cycle, MN1 and MN3 turn off while MN4 turns on and emission starts. The amount of current flowing into the OLED (I_{oled}), and hence the luminance of the panel, depends on the voltage across the storage capacitor. This kind of pixel is known as current copy due to its operating principle. Ideally, I_{oled} equals I_{data} and is independent of the TFT parameters. There are, however, issues that have to be considered.

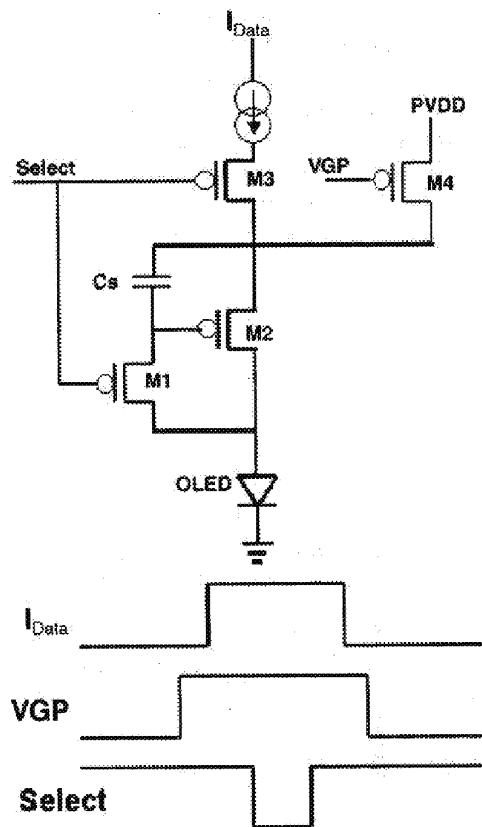


Figure 14.35 The 4T1C current-driven pixel compensation circuit and its timing.

The first issue is that the driver IC is not common and does not exist commercially. One difficulty for the driver IC is that it has to provide channel-to-channel accuracy of I_{data} , especially at low grayscales. At a low grayscale, the required I_{data} is as low as several nA, and driver IC output uniformity within the nA range is not guaranteed. An other issue is also encountered at low grayscales. During the programming period, the very low current from the IC has to charge not only the storage capacitor in the pixel, but also the whole data line it is connected to. Therefore, very long programming time is expected, which limits either the image quality or the panel resolution. Yet another issue arises for the quick-test procedure of the panel. This procedure means that before IC bonding, every panel is examined with a simple plain or monochrome image to check the panel uniformity and functionality. This normal procedure, however, is not suitable for current-driven AMOLEDs, since too many pads are required for driving the panel, which is not practical for mass production and inspection. The issues described above can be tackled by applying the current-mirror type of pixel compensation circuit, and will be described as follows.

Sasaoka *et al.* [56], from Sony Corporation, developed a current-driven pixel compensation circuit. The pixel contains four transistors and one capacitor, and is illustrated in Figure 14.36. The pixel structure is known as the current-mirror type, and the operating principle is simple and similar to the current-copy type. When 'write scan' and 'erase scan' are selected, I_{data} on the data line is ready and flows from V_{dd} to the external driver IC through the diode connection transistor T1. The flowing of I_{data} will charge the capacitor and finally, a voltage, V_{data} , will be stored across the capacitor. The deviation of the characteristics of T1, such as mobility and threshold voltage, will be self-compensated and V_{data} corresponds to the deviation. The current-mirror pixel has some advantages over the current-copy pixel in that I_{data} for the current-mirror pixel can be made larger during the programming period simply by adjusting the W/L ratio of T1 and T2. By programming larger I_{data} , the previously described issues for the current-copy pixel can be tackled. To keep the same amount of current flowing into the OLED, the dimensions of T1 and T2 must be tuned to $(W/L)_{T1} = k(W/L)_{T2}$, where k is a factor larger than 1, depending on how much I_{data} is shrunk under the assumption that the threshold voltages of the two transistors T1 and T2 are identical. In actual practice, although T1 and T2 are different transistors, and hence have different threshold voltages, T1 and T2 are placed close to each other in the layout and are well designed to minimize the V_{th} difference. More examples of current-driven pixel compensation circuits can be found in Figures 14.37–14.39 below.

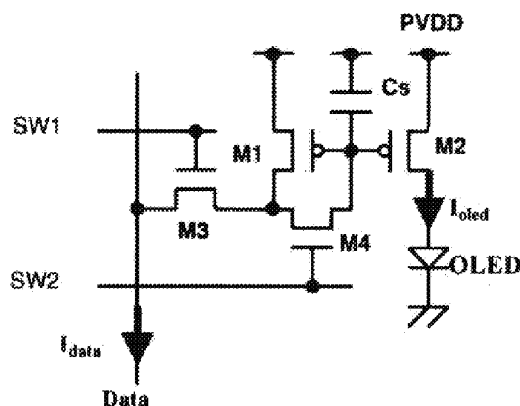


Figure 14.36 The 4T1C 'current-mirror' pixel compensation circuit.

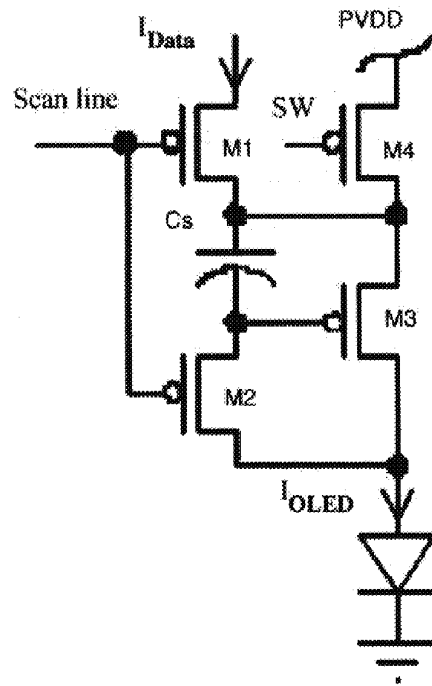


Figure 14.37 A 4T1C current-driven pixel compensation circuit, which can be applied in LTPS TFTs.

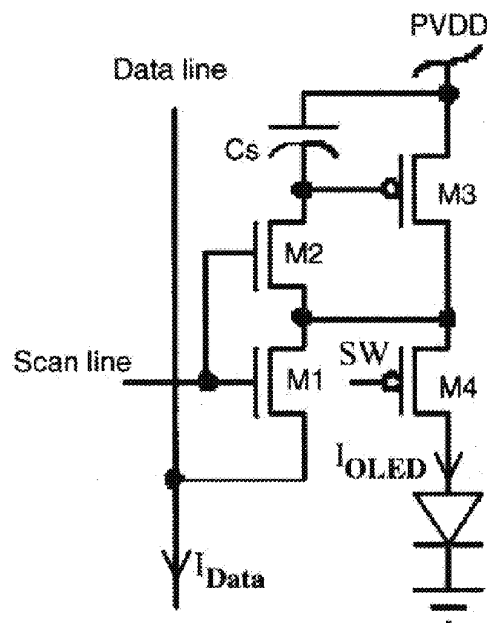


Figure 14.38 Another example of a 4T1C current-driven pixel compensation circuit, which can be applied in LTPS TFTs.

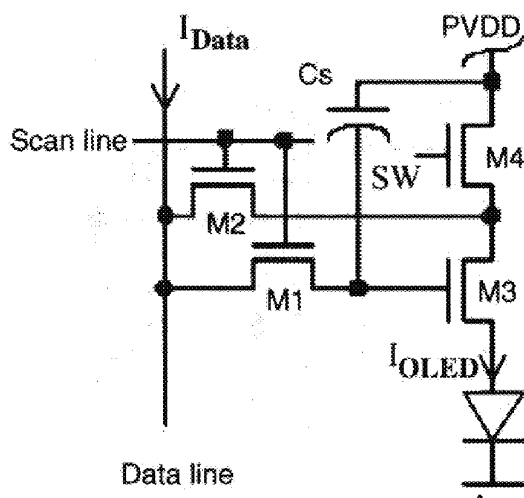


Figure 14.39 A 4T1C current-driven pixel compensation circuit, which can be applied in both LTPS and a-Si TFTs.

14.4.1.5 Digital Driving Circuits

In contrast to the conventional types of AMOLED displays, digital driving communicates data information by way of digital signals. The digitally driven pixel has only two states: on and off. The grayscale of each pixel is determined by either the emission time within one frame or the area it emits; the former is called time-ratio grayscale and the latter area-ratio grayscale. Hitachi proposed a particular pixel circuit [57, 58] named 'clamped inverter driving' in 2002, which is a hybrid of voltage digital driving. The pixel is turned on and off according to the analog V_{data} input from the driver IC and the other sweep signal. The details of this clamped inverter driving are described as follows.

Figure 14.40 depicts the clamped inverter pixel proposed by Hitachi. The V_{data} and sweeping signal within one frame are also indicated in Figure 14.41 below. The panel operation is divided into two periods per frame: the first period is for data writing (for all pixels in one panel), and the other period is for panel emission. In the first period, analog V_{data} is written into its corresponding pixel through T1; in the meantime, T2 is turned on and the voltage at node A (V_A) will be clamped at one voltage V_c as shown in Figure 14.42 below. The voltage across the capacitor will be $V_{data} - V_c$. In the second period, the

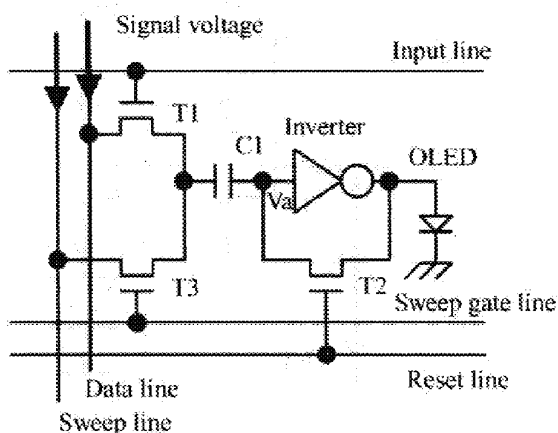


Figure 14.40 Clamped inverter pixel circuit.

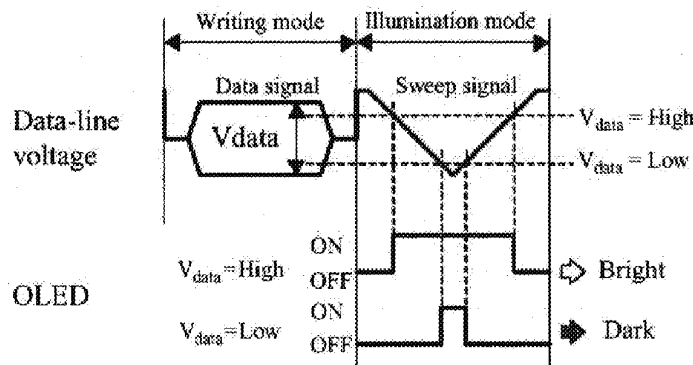


Figure 14.41 Operating principle of the clamped inverter pixel.

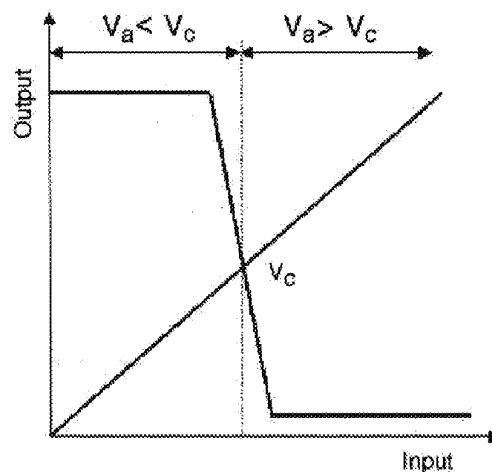


Figure 14.42 The inverter characteristic showing that it will be biased at V_c if input equals output.

sweeping signal starts. T3 is turned on and T2 is turned off. V_a now becomes variable and is controlled by the sweeping signal minus the voltage $V_{data} - V_c$, i.e. $V_a = V_{sweep} - V_{data} + V_c$. Since the amplitude of the sweeping signal changes with time, V_a will also change with time at the same rate. If $V_{sweep} - V_{data} < 0$, then $V_a < V_c$ and the OLED will be driven by a constant current (Bright). If $V_{sweep} - V_{data} > 0$, then $V_a > V_c$ and no voltage will appear across the OLED (Dark). For one pixel, V_{data} determines the emission time and hence the grayscale. Information on the threshold voltage and mobility is determined in V_c , and the emission time does not depend on V_c .

Although the pixel circuit can achieve AMOLED displays with better uniformity, another issue is raised during operation. The power consumption may be higher than expected. During the data-writing period each pixel is biased at V_c , and both PTFTs and NTFTs will turn on, which consumes extra power. In the emission period, the sweeping signal changes alternately and when V_a approaches V_c , extra power is consumed.

14.4.1.6 Time-Ratio Grayscale

Time-ratio grayscale has been conventionally used for plasma display panels (PDPs), and any time-ratio driving method for PDPs may also be applicable to AMOLEDs. Mizukami *et al.* [59], from Semiconductor Energy Laboratory (SEL), applied the digital driving approach to a VGA AMOLED

display. The pixel circuit can be as simple as the 2T1C structure and is redrawn in Figure 14.43. Figure 14.44 depicts the OLED current versus the input data voltage for different characteristics of the driving TFT. It can be seen that for any fixed V_{data} between V_{sl} and V_{sh} , I_{OLED} will vary due to different TFT characteristics. However, for $V_{data} = V_{sl}$, which drives the TFT into the linear operating region, excellent image uniformity can be obtained since the current of the driving TFT in this region is expected to be similar all over the panel. It is therefore better to have the driving TFT operate in the two states (V_{sl} and V_{sh}) only. The grayscale of each pixel is determined in Figure 14.45 below, in which 6 bits are used. For 6 bit operation, one frame is divided into six sub-frames (SF1–SF6). The initial time T_A for each sub-frame is reserved for data writing over the whole panel, and during each T_A period, the cathode voltage is pulled high (V_{ch}) to make sure there is no emission during data writing. The rest of the time for each sub-frame is for the emission period (TL1–TL6). The emission periods for TL1–TL6 are ratioed according to the time weight of the 1st, 2nd, 3rd, 4th, 5th, and 6th bits. For example, the data of 101100 should store V_{sl} , V_{sh} , V_{sl} , V_{sl} , V_{sh} , V_{sh} at the gate of the driving TFT for TL1 to TL6, respectively.

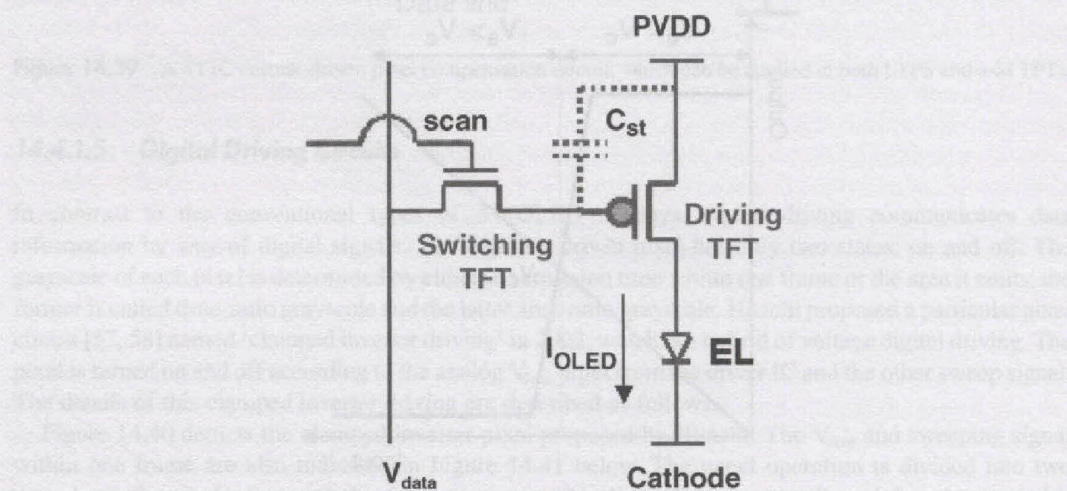


Figure 14.43 Simple 2T1C circuit for digital-driven pixel.

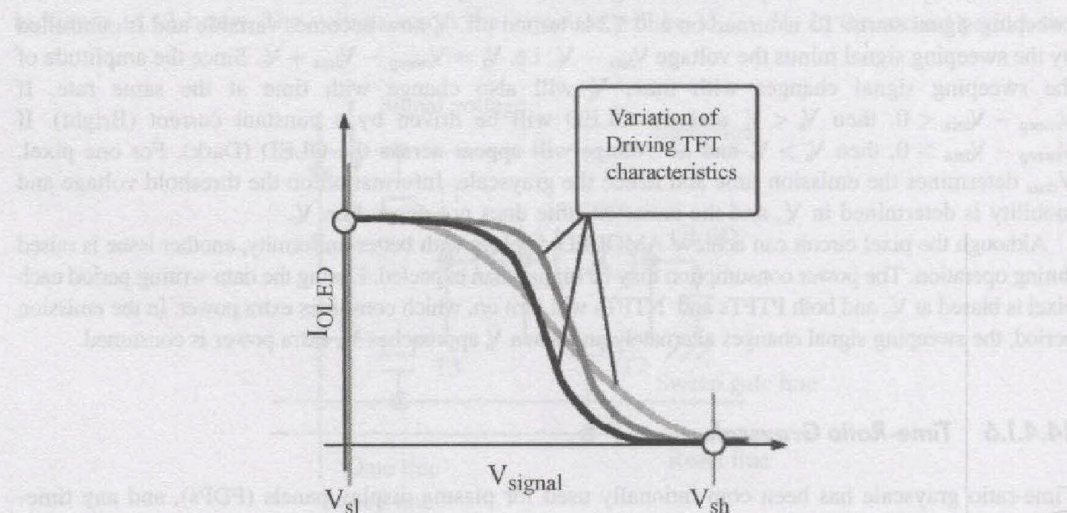


Figure 14.44 The output I_{oled} versus the input data V_{signal} for different devices.

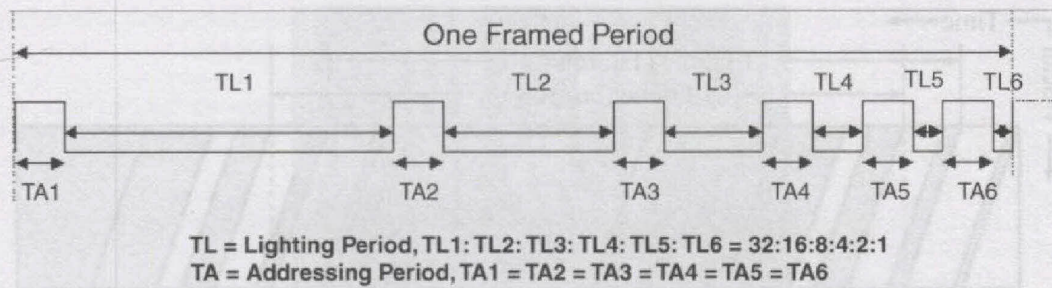


Figure 14.45 Conceptual drawing of the operation of digital driving method within one frame.

Although this approach gives excellent luminance uniformity, one drawback is that the pixel requires very rapid data addressing for each sub-frame or the emission time will be shortened, which influences the EL life time if total front-of-screen luminance is kept constant. Eight bit operation will become even more difficult from the design point of view. Another drawback is that the luminance is linearly proportional to grayscale, which means that this method can only be applied for a linear gamma panel. In this circuit, the cathode has to be turned on and off six times within one frame, and this may lead to spike noise on the panel and extra power consumption. To avoid this, the same group (SEL) proposed a modified approach [60], and the pixel circuit is drawn in Figure 14.46. The driving approach within one frame is also illustrated in Figure 14.47 below. In Figure 14.46, the pixel contains one extra transistor (SW2) and one extra signal line (ES line). When the ES line turns on the transistor SW2, the charge on the storage capacitor will vanish and no current flows into the OLED. The pixel operation is different from the previous one in that the pixel emits at the time when the data is written into the pixel. When one sub-frame starts, the data is written row by row into the pixel and hence the emission starts row by row. After a time, which depends on the corresponding emission time for the sub-frame, the OLED is turned off by turning on switch SW2 row by row. One sub-frame is then finished and is followed by the data writing and emission for the next sub-frame. Notice that in this modified approach, the total emission time in one frame is longer than that in the previous approach and the cathode voltage is always kept constant. To further increase the total emission time and decrease the data addressing frequency, a continuous sub-field with a multiplex scanning system and a multiple addressing method were proposed by Ouchi *et al.* from Hitachi Research Laboratory [61] and Tagawa *et al.* from Sharp Corporation [62], respectively. These approaches, however, required more complicated peripheral driving schemes.

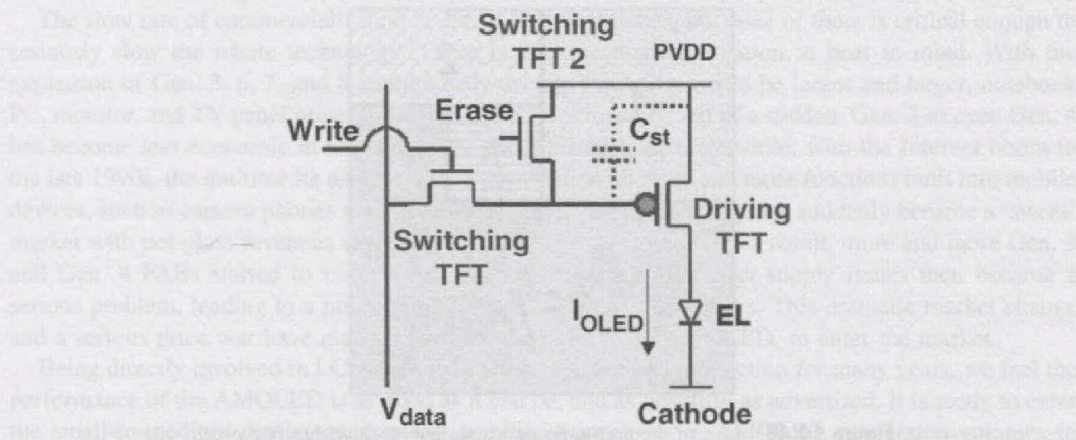


Figure 14.46 Another digital-driven pixel circuit with one extra transistor and one signal line.

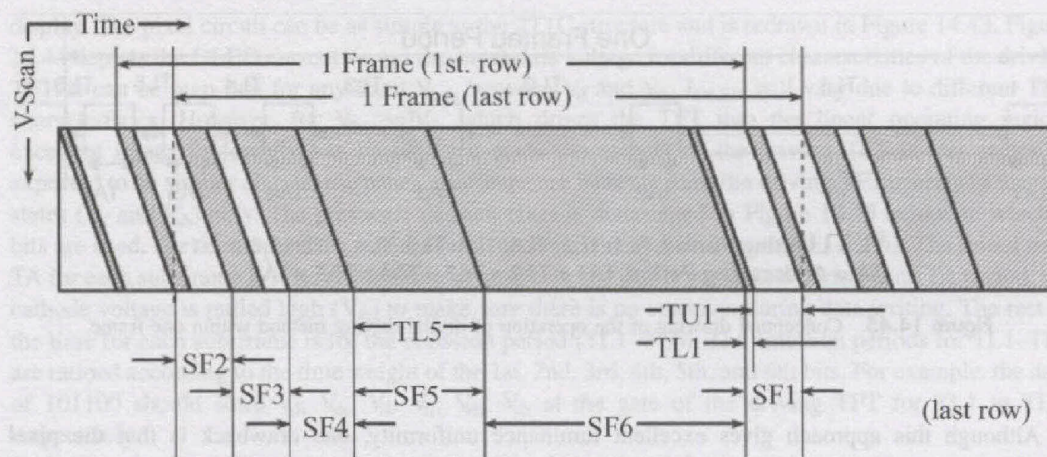


Figure 14.47 Improved operation of digital driving method to increase the emitting time in one frame.

14.4.1.7 Area-Ratio Grayscale

In the area-ratio grayscale method, the emitting area is modulated and divided into several sub-areas, depending on the grayscale. The concept of this approach can be seen in Figure 14.48, in which one pixel is shown for 3 bit grayscale. The ratio of the emitting area is 4:2:1, while the other area is left for addressing and driving TFTs and storage capacitors. One advantage of this approach is that if the driving TFT is biased at V_{sl} or V_{sh} (see Figure 14.44) during emission, uniformity can be obtained since the grayscale is determined by the ratio of the emitting areas. The disadvantage is, however, the limited grayscale due to the limited area for subdivision within one pixel. Kimura *et al.* [63], from Ryukoku University, applied this approach to a TFT-driven polymer display, and a picture of the emitting area as well as the driving TFT in the pixel can be found in Figure 14.49 below. The details can be found in ref. [63].

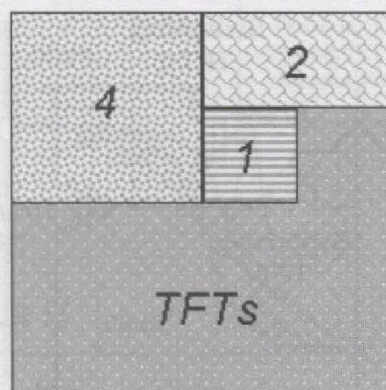


Figure 14.48 Idea of the area-ratio grayscale approach within one pixel.

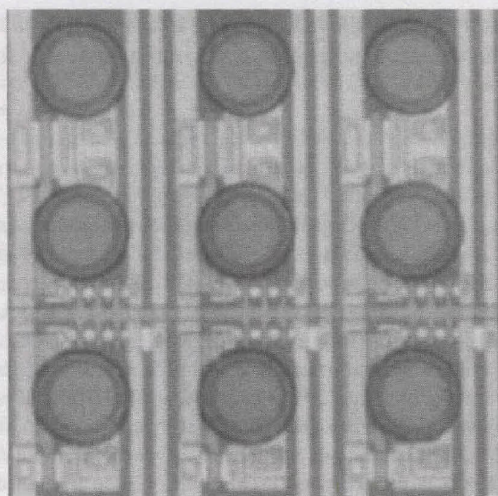


Figure 14.49 A picture shows the emitting area as well as the driving TFT for the area-ratio grayscale approach.

14.5 Summary and Outlook

The invention of the OLED has produced an exciting emissive display that can naturally deliver vivid front-of-screen visual experiences. It shows great potential to become a disruptive technology to the existing dominant display technology, TFT-LCD. The OLED offers potentially a lower bill of materials (BOM) cost, simpler structure and process, and far better performance in contrast ratio, response time, viewing angle, and color saturation. Looking back at its history, the first LCD panel was produced in 1960, but a-Si TFT-LCD mass production started in the late 1980s and early 1990s, almost 30 years from invention to commercialization. The first efficient OLED device was described in 1987, and the first AMOLED product appeared on the market in 2003. The AMOLED has shown a much faster pace to commercialization. The maturity of TFTs in the LCD industry played an important role in accelerating AMOLED commercialization.

However, the commercialization activities slowed down considerably after 2003. The production yield did not improve quickly, with issues relating to fine shadow mask and TFT non-uniformity being two major bottlenecks. These have been discussed extensively in this chapter. Alternative device architectures and compensation schemes have been widely studied and implemented.

The slow rate of commercialization is due to technical issues, but none of them is critical enough to seriously slow the whole technology. There is also the market situation to bear in mind. With the expansion of Gen. 5, 6, 7, and 8 continuously driving the LCD size to be larger and larger, notebook PC, monitor, and TV panel prices have all dropped significantly. All of a sudden, Gen. 3 or even Gen. 4 has become less economic in terms of large panel production. Meanwhile, with the Internet boom in the late 1990s, the multimedia and digital era emerged. With more and more functions built into mobile devices, such as camera phones and mobile TVs, small-to-medium displays suddenly became a 'sweet' market with per-glass revenues several times those of large panels. As a result, more and more Gen. 3 and Gen. 4 FABs started to make small-to-medium panels, and over-supply issues then became a serious problem, leading to a price drop of 40–50% in just a few years. This dramatic market change and a serious price war have made it hard for the newcomer, AMOLED, to enter the market.

Being directly involved in LCD and OLED development and production for many years, we feel the performance of the AMOLED is as good as it can be, and as beautiful as advertised. It is ready to enter the small-to-medium display market and significant increases in AMOLED production volumes in

2007 seem to indicate a new dawn. We believe that in just a few years from now, we will see AMOLED panels in many of our mobile devices, and people will continuously ask for OLEDs.

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