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Study of leakage current in *n*-channel and *p*-channel polycrystalline silicon thin-film transistors by conduction and low frequency noise measurements

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The off-state current in *n*- and *p*-channel polycrystalline silicon thin-film transistors (polysilicon TFTs) is investigated systematically by conduction measurements at various temperatures and low-frequency noise measurements at room temperature. It is demonstrated that the leakage current is controlled by the reverse biased drain junction. The main conduction mechanisms are due to thermal generation at low electric fields and Poole–Frenkel accompanied by thermionic filed emission at high electric fields. The leakage current is correlated with the traps present in the polysilicon bulk and at the gate oxide/polysilicon interface which are estimated from the on-state current activation energy data. Analysis of the leakage current noise spectral density confirms that deep levels with uniform energy distribution in the silicon band gap are the main factors in determining the leakage current. The density of deep levels determined from noise analysis is in agreement with the value obtained from conductance activation energy analysis. The substantially lower leakage current observed in the *n*-channel polysilicon TFT is explained by the development of positive fixed charges at the interface near the drain junction which suppress the electric field.
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I. INTRODUCTION

Polycrystalline silicon thin-film transistors (polysilicon TFTs) present increasing interest due to their use as switching devices in active matrix liquid crystal displays. For such applications, the leakage current I_L has to be as low as 1 pA/μm to hold the signal levels for acceptable image quality.[1] However, polysilicon TFTs suffer from relatively high leakage currents, especially under high applied gate and drain voltages, generated by trap states present at the grain boundaries in the drain and channel regions. In view of this, considerable effort has been devoted to identifying the conduction mechanisms of the leakage current in polysilicon TFTs.[2–6] It has been shown that the conduction mechanism of I_L is not determined by a unique mechanism but it depends on the gate bias V_G, drain bias V_D, device structure, and the polysilicon layer structure. All the investigations were based on the analysis of the TFT transfer characteristics at various temperatures. Recently, low-frequency noise measurements were employed to identify the origin of the leakage current in undoped low pressure chemical vapor deposited (LPCVD) polysilicon TFTs.[7]

In this article, the leakage current in *n*-channel and *p*-channel undoped hydrogenated polysilicon TFTs is systematically investigated by combined measurements of their transfer characteristics at various temperatures and low-frequency noise measurements at room temperature. The measured off-state current characteristics are investigated to identify the leakage current conduction mechanisms. The leakage current enhancement in the *p*-channel TFT and the correlation of the leakage current with the trap states density of the polysilicon TFTs are discussed. The trap states within the polysilicon bulk and at the polysilicon/gate oxide interface are determined by a method based on the field-effect conductance activation energy measurements.[8]

The origin of the leakage current is further investigated by low-frequency noise measurements at room temperature. In *n*-channel TFTs, the leakage current noise is due to carrier fluctuation within the space charge region of the drain junction. In *p*-channel TFTs, in addition to carrier fluctuation, the contribution of the diffusion noise is significant due to the presence of higher electric fields at the drain junction. The noise data indicate that deep levels with uniform energy distribution within the silicon band gap contribute mainly to the leakage current. From analysis of the leakage current noise data, the density of the deep levels is determined which is in agreement with the value obtained from the conductance activation energy data. It has also been proven that the noise analysis not only confirms the activation conductance results,

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but goes further giving a possible distribution of their kinetic parameters.

II. EXPERIMENT

The TFT devices studied in this work were made on undoped polysilicon layers (220 nm thick) first deposited on thermally oxidized silicon wafers by LPCVD using SiH_4 source gas at 620 °C and pressure about 0.4 mTorr. Then, the polysilicon layers were annealed at 1000 °C for 3 h in dry N_2 ambient for grain enlargement. Transmission electron microscopy analysis showed that the polysilicon layers have columnar structure with an average grain size close to the surface of about 100 nm. The gate dielectric was SiO_2 (45 nm thick) grown at 1000 °C in dry oxygen atmosphere. After depositing and patterning the LPCVD polysilicon gates, phosphorus ions were implanted at a dose $>10^{15}$ cm^{-2} with an energy 85 keV to form the source, drain, and gate n^+ regions for n-channel devices. For p-channel devices, boron implantation at a dose $>10^{15}$ cm^{-2} with an energy 35 keV was employed. The polysilicon layers were then hydrogenated by implanting hydrogen ions at a dose 1×10^{16} cm^{-2} and an energy 130 keV through the top passivating thick oxide, the polysilicon gate, and the gate oxide. Dopant activation was carried out at 450 °C for 30 min in H_2 ambient. The channel width was $W=50$ μm and the length $L=10$ μm was long enough to avoid short-channel effects.

Drain current-gate voltage (I_D-V_G) measurements were obtained from -12 to $+10$ V in the temperature range from room temperature to about 120 °C. Low frequency noise measurements (0.5–200 Hz) were performed at room temperature with a dynamic signal analyzer (HP 35665). A low-noise current-voltage converter (EG&G model 181) and a low-noise voltage amplifier (NF 5305) were used for direct measurement of the leakage current noise spectral density S_L. Gate and drain biases were supplied by Cd/Ni batteries to reduce any external low-frequency noise.

III. RESULTS AND DISCUSSION

A. Conduction measurements

Figure 1 shows typical transfer characteristics of n-channel and p-channel polysilicon TFTs, measured at room temperature and drain voltages $V_D=5$ V and -5 V, respectively. In the off-state current region, the leakage current I_L increases considerably when the applied gate bias V_G increases. We have found that I_L is independent of L. The dependence of I_L on $1/L$ as shown in Fig. 2 for a typical TFT, indeed indicates that the leakage current is caused by the reverse biased drain junction.

The junction leakage current can arise by electron-hole pairs generated via grain boundary traps in the depletion region. The main mechanisms through which a trapped carrier at an energy level E_t can be generated to the conduction or valence band are:

(a) thermal generation due to thermal excitation of trapped carriers;

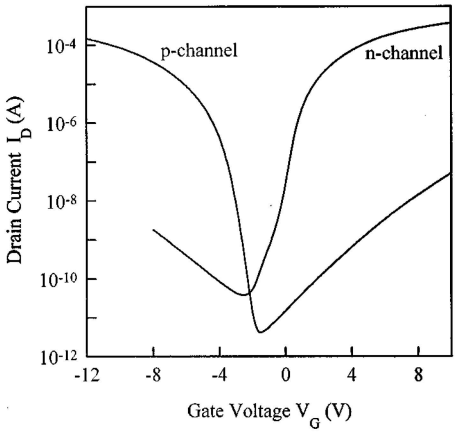

FIG. 1. Typical transfer characteristics of n-channel and p-channel polysilicon TFTs at drain voltages 5 V and -5 V, respectively. The gate ratio is $W/L=50/10$.

(b) pure field emission due to field ionization of trapped carrier tunneling through the potential barrier into the conduction or valence band;

(c) thermionic field emission or Poole–Frenkel emission due to field-enhanced thermal excitation of trapped carriers in the conduction or valence band.

The applied field causes the barrier to become thin enough that thermal excitation to virtual states prior to tunneling can easily occur.

In order to clarify the leakage current mechanism, the temperature dependence of the drain current was also measured at various drain voltages. The temperature dependence of the leakage current for a typical n-channel TFT at $V_d=5$ V is shown in Fig. 3. The activation energies E_a of the drain current are derived from Arrhenius plots and plotted in Figs. 4(a) and 4(b) for the n-channel and p-channel TFTs, respectively. In the on-state current regime, the value of the

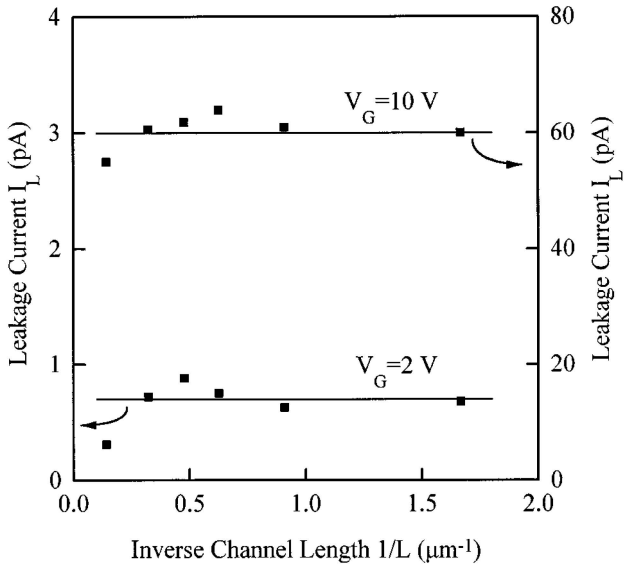

FIG. 2. Dependence of the leakage current I_L on the inverse channel length $1/L$ at drain voltage $V_D=-0.1$ V for typical p-channel polysilicon TFTs with channel width $W=50$ μm.

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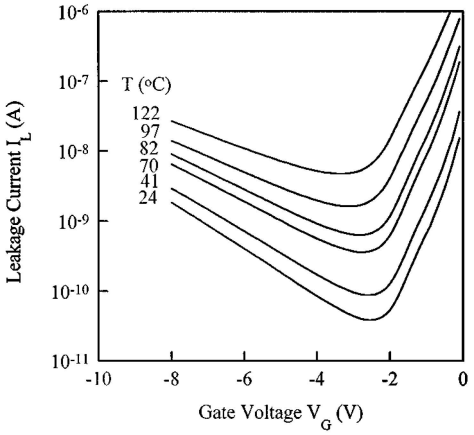

FIG. 3. Leakage current I_L vs gate voltage V_G of a typical n-channel polysilicon TFT measured at drain voltage $V_D=5$ V and various temperatures.

activation energy reflects the potential barrier height at the grain boundaries present within the TFT channel. In the off-state current regime, the activation energy of the minimum leakage current becomes about half the silicon band-gap energy at low drain biases (Fig. 4). This implies that the minimum leakage current is caused mainly by thermal excitation, since the thermal excitation current is proportional to the intrinsic carrier concentration (n_i) and n_i is proportional to $\exp(-E_g/2kT)$, where E_g is the energy gap of silicon.

With increasing $|V_G|$ in the off-state regime, E_a decreases indicating that the carrier generation rate is field-enhanced. The temperature dependence of the leakage current (Fig. 3) rules out the mechanism of pure field emission. The observed field-enhanced generation implies that the Poole–Frenkel effect is the most likely generation mechanism. According to this mechanism, the reversed-biased drain junction current is modeled as generation current which is field enhanced and of the form

$$I_L=I_{LO}e^{\beta\sqrt{E_m}}, \tag{1}$$

where $I_{LO}=qA_jw_DU$, A_j is the junction area, w_D is the reverse-biased drain junction depletion width, and U is the zero field carrier generation rate per unit volume. The expression for the generation rate U due to grain boundary defects is[9]

$$U=\frac{\sigma_n\sigma_p v_{\rm th}N_{\rm gb}n_i}{\sigma_n\exp\left(\dfrac{E_t-E_i}{kT}\right)+\sigma_p\exp\left(\dfrac{E_i-E_t}{kT}\right)}, \tag{2}$$

where σ_n and σ_p are the electron and hole capture cross-sections, respectively, $v_{\rm th}$ is the carrier thermal velocity, $N_{\rm gb}$ is the grain boundary trap density per unit area distributed throughout the grain, E_t is the trap level, E_i is the intrinsic Fermi level, and n_i is the intrinsic carrier density. For simplicity assuming $\sigma_n=\sigma_p=\sigma$ and the carriers are mainly generated from midgap defect states ($E_t=E_i$), the expression for the leakage current becomes[10]

$$I_L=qA_jw_D\sigma v_{\rm th}N_{\rm gb}n_ie^{\beta_{\rm PF}\sqrt{E_m}}e^{\beta_{\rm TFE}\sqrt{E_m}}. \tag{3}$$

In the above equation, $\beta_{\rm PF}$ and $\beta_{\rm TFE}$ are the field-enhancement factors arising from the Poole–Frenkel effect and the thermal field emission with expected values about 0.009 and 0.0011 $\rm cm^{1/2}\,V^{-1/2}$, respectively, at room temperature.[10] Considering that the peak electric field E_m at the drain junction is dominated by the vertical electric field at the interface,[11] then

$$E_m=\frac{|V_G-V_D-V_{\rm fb}|}{t_{\rm ox}(\epsilon_{\rm Si}/\epsilon_{\rm SiO_2})}, \tag{4}$$

where $\epsilon_{\rm Si}$ and $\epsilon_{\rm SiO_2}$ are the permittivities of Si and SiO_2, respectively, $V_{\rm fb}$ is the flatband voltage, and $t_{\rm ox}$ is the thickness of the gate oxide.

Figure 5 shows plots of $\log I_L$ vs $(E_m)^{1/2}$ obtained from the data of the n-channel and p-channel polysilicon TFTs at various drain voltages. In all cases, straight lines fit the data in the high electric field regions. This proves that I_L is dominated by Poole–Frenkel emission. By increasing the drain voltage, the slope β of the straight lines increases. For a typical p-channel polysilicon TFT, β increases from about 0.01 $\rm cm^{1/2}\,V^{-1/2}$ at $V_D=-0.1$ V to 0.02 $\rm cm^{1/2}\,V^{-1/2}$ at high drain voltages (Fig. 6). These results indicate that at the low value of $V_D=-0.1$ V the pure Poole–Frenkel emission is present ($\beta=\beta_{\rm PF}\cong 0.009\ \rm cm^{1/2}\,V^{-1/2}$) and at higher drain

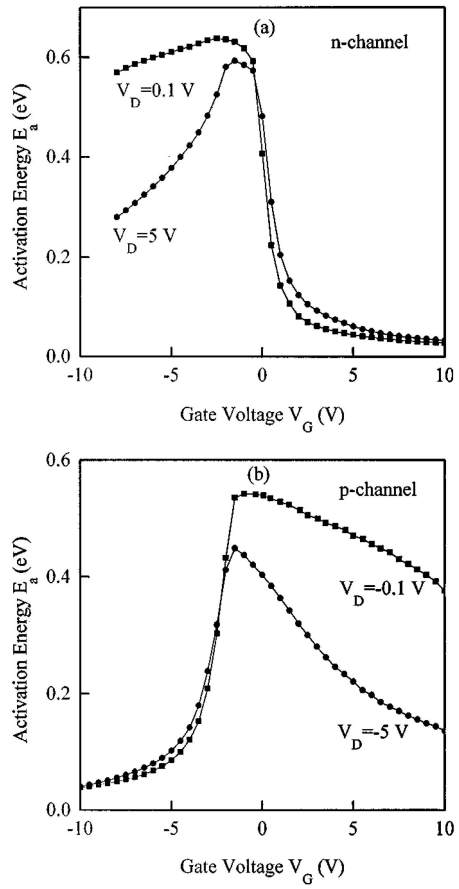

FIG. 4. Dependence of the drain current activation energy E_a on gate voltage V_G for: (a) n-channel polysilicon TFT at drain bias 0.1 V and 5 V and (b) p-channel polysilicon TFT at drain bias -0.1 V and -5 V. The gate ratio is $W/L=50/10$.

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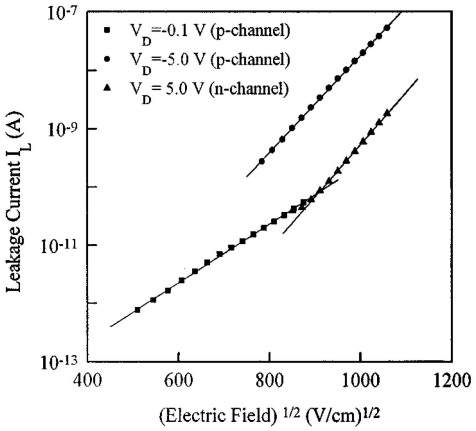

FIG. 5. Measured $\log I_L$ vs $(E_m)^{1/2}$ on a semilog scale of the junction at the drain end for n-channel and p-channel polysilicon TFTs at various drain voltages.

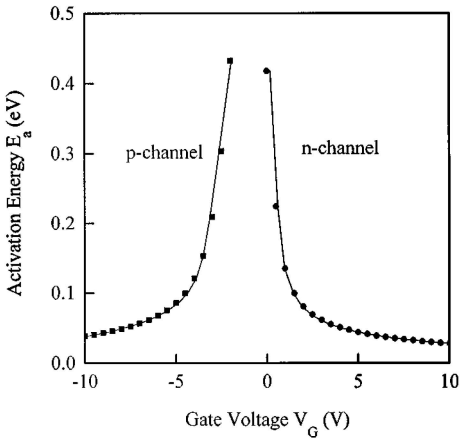

FIG. 7. On-state current activation energy E_a as a function of the gate voltage V_G of typical n-channel and p-channel polysilicon TFTs at drain voltages 0.1 V and -0.1 V, respectively. The solid lines are the calculated curves using the method described in Ref. 8 for the trap distribution parameters: (a) $N_d=2\times10^{11}$ cm^{-2}, $N_s=1.4\times10^{15}$ cm^{-2}, and $kT_s=0.014$ eV for the n-channel TFT and (b) $N_d=3\times10^{12}$ cm^{-2}, $N_s=2.8\times10^{14}$ cm^{-2}, and $kT_s=0.028$ eV for the p-channel TFT.

voltages the Poole–Frenkel effect is accompanied by thermal field emission ($\beta=\beta_{\rm PF}+\beta_{\rm TFE}\cong0.02$ cm$^{1/2}$ V$^{-1/2}$) due to the increased electric field at the drain junction.

In the thermionic field emission mechanism, the presence of trap states in the band gap assists the process by shortening the effective tunneling length of the carrier. In fact, polysilicon TFTs have many traps present in the band gap and, hence, this situation occurs easily. The density of trap states in the silicon band gap consists of the grain boundary traps and the SiO_2/polysilicon interface traps. Following the results of a recent work,[8] the energy distribution of the grain boundary traps can be modeled by

$$N_{\rm gb}(E)=N_d+N_t\ \exp\left(-\frac{E_c-E}{kT_t}\right), \tag{5}$$

where N_d is the density per unit area of deep levels with uniform energy distribution and N_t, and T_t are the characteristic parameters of the band tails with exponential energy distribution increasing towards the conduction band edge E_c. The deep levels are expected to give larger capture emission cross-section for carriers to tunnel through the band gap. The interface states distribution is considered to have the exponential distribution[8]

$$N_{\rm is}(E)=N_s\ \exp\left(-\frac{E_c-E}{kT_s}\right), \tag{6}$$

where N_s and T_s are parameters characterizing the exponential distribution. The grain boundary and the interface states were determined with a method based on the variation of E_a with V_G in the on-state regime at low drain voltage (Fig. 7). The extracted values of the trap parameters are presented in Fig. 7. It is found that, in both n-channel and p-channel TFTs, the total trap density consists of the exponential interface states $N_{\rm is}$ and the grain boundary deep states N_d with uniform energy distribution. Since the leakage current is proportional to the midgap trap density [Eq. (3)], the smaller leakage current of the n-channel TFT (Fig. 5) can be explained by the measured lower trap concentration N_d (Fig. 7).

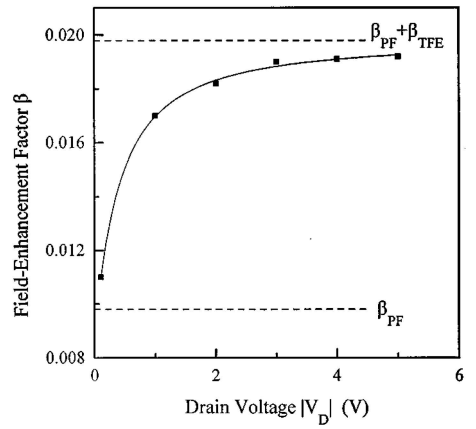

FIG. 6. Variation of the field-enhancement coefficient β as a function of the drain bias V_D of a typical p-channel polysilicon TFT. The dashed lines show the values of the field-enhancement coefficients $\beta=\beta_{\rm PF}\cong0.009$ cm$^{1/2}$ V$^{-1/2}$ and $\beta=\beta_{\rm PF}+\beta_{\rm TFE}\cong0.02$ cm$^{1/2}$ V$^{-1/2}$.

From the activation energy data in the off-state regime (Fig. 4), the following conclusions are obtained:

(a) The activation energy decreases with increasing the applied drain voltage. The decrease in the electric field at the drain junction causes the decrease of the leakage current activation energy. This feature corresponds to the leakage current of the TFTs shown in Fig. 1. That is, the increase of the leakage current in Fig. 1 corresponds to the decrease in the activation energy shown in Fig. 4.

(b) In the n-channel TFT, the decrease of the activation energy with increasing $|V_G|$ is less pronounced compared to the p-channel TFT. This result implies that the field-induced process in the n-channel TFT is suppressed.

One possible explanation for suppression of the electric field is the development of localized fixed charges at the

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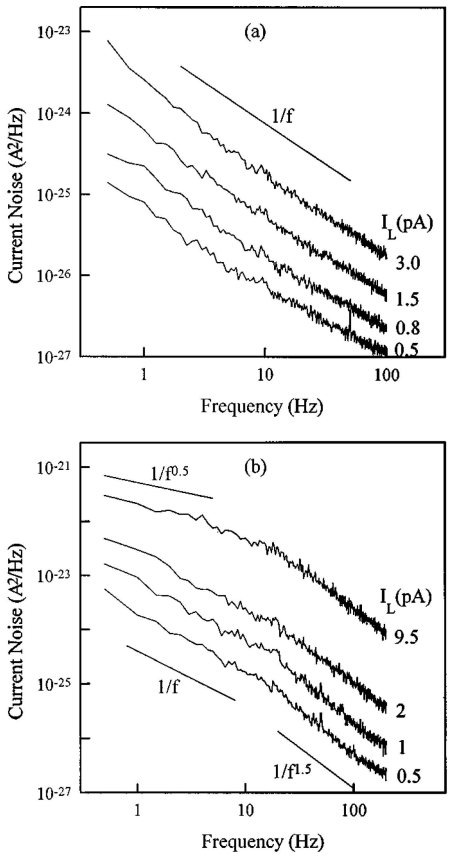

FIG. 8. Typical noise spectra obtained at various leakage currents from n-channel (a) and p-channel (b) polysilicon TFTs at drain voltages 4 V and -5 V, respectively.

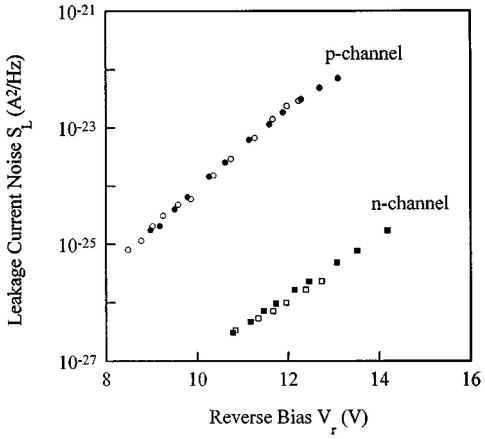

FIG. 9. Noise power spectral density of the leakage current S_L at the frequency of 10 Hz vs the reverse bias V_r of the drain junction at various drain voltages V_D of typical n-channel (□ $V_D=3$ V, ■ $V_D=4$ V) and p-channel (○ $V_D=-3$ V, ● $V_D=-5$ V) polysilicon TFTs.

interface near the drain junction. If the existing interface states are assumed to be donor states, these are positively charged during the p-channel TFT's operation since they are located above the Fermi level and neutral during the n-channel TFT's operation since they are occupied by electrons. However, in the n-channel and p-channel polysilicon TFTs, positive phosphorus ions and negative boron ions, respectively, may diffuse fast through the grain boundaries from the drain contact towards the interface. In the case of p-channel TFT, the negative charge of the boron ions at the interface near the drain junction is neutralized by the positive charge of the interface states. On the contrary, in the n-channel TFT the positive phosphorus ions lead to the development of positive fixed charges near the drain junction. Based on the above, we infer that the positive fixed charges suppress the electric field from the gate in the drain junction and finally reduce the leakage current in the n-channel polysilicon TFT. In order to clarify strictly the reasons for superiority of the n-channel TFT, more systematic investigations are required.

B. Noise measurements

The origin of the leakage current is further investigated by low-frequency noise measurements. Figures 8(a) and 8(b) show typical measurements of noise spectra of n-channel and p-channel polysilicon TFTs, respectively, for different leakage currents. For the n-channel TFT, the leakage current noise S_L exhibits an almost pure $1/f$ behavior. For the p-channel TFT, at low leakage currents, one can notice that the $1/f$ dependence is turned into a $1/f^{1.5}$ dependence for frequencies above 10 Hz. However, at high leakage currents ($I_L>2$ nA), the $1/f$ branch disappears in the low-frequency range; the spectra show a $1/f^{1.5}$ dependence at frequencies above 10 Hz with a changeover to a $1/f^{0.5}$ dependence. It is plausible, in our opinion, to suppose that in the p-channel polysilicon TFT the noise source is diffusion noise.[12,13] Such a noise source for the p-channel TFT reveals the presence of stronger electric field at the drain junction. Nevertheless, we cannot exclude another possible explanation based on the influence of a limited number of Lorentzian spectra which correspond to the presence of a different kinds of traps characterized by a limited number of relaxation times; in such a case, more adjustable parameters are needed and, therefore, this hypothesis can be considered as more speculative.

In order to clarify the origin of the leakage current in the n-channel and p-channel polysilicon TFTs, the leakage current noise spectral density S_L measured at the frequency of $f=10$ Hz is plotted versus the reverse bias of the drain junction $V_r=|V_G-V_D|$ (V_G and V_D are of opposite polarity) as shown in Fig. 9. Clearly, in both cases, different combinations of the drain and gate biases produce nearly the same off-state current noise for the same reverse bias. These results show that the leakage current is limited by the reverse biased drain junction, in agreement with results obtained from conduction measurements.

The $1/f$ frequency dependence of the leakage current noise S_L can be explained by carrier fluctuation between the conduction or valence band and gap states occurring within the space charge region of the drain junction. Such a model was also used in a previous work to explain the $1/f$ behavior in LPCVD polysilicon TFTs.[14] Since the leakage current is due to Poole–Frenkel emission, according to Eq. (1), the current fluctuation is considered to arise from fluctuations of the electric field E_m. Thus, the fluctuation in I_L can be written as

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$$\delta I_L = \frac{\partial I_L}{\partial E_m}\,\delta E_m . \tag{7}$$

Considering the voltage drop in the gate oxide and using Gauss' law at the polysilicon/oxide interface, an equation of the surface electrostatic potential (ψ_s) is

$$V_G = V_{\rm fb} + \psi_s + \frac{\epsilon_{\rm Si} E(\psi_s)}{C_{\rm ox}}, \tag{8}$$

where $C_{\rm ox}$ is the oxide capacitance per unit area. Considering that the flatband voltage fluctuation arises from the electrostatic potential fluctuation, then from Eq. (8) the field fluctuation is

$$\delta E_m = -\frac{2C_{\rm ox}}{\epsilon_{\rm Si}}\,\delta V_{\rm fb} . \tag{9}$$

From Eqs. (7) and (9), the current fluctuation δI_L is

$$\delta I_L = -\frac{2C_{\rm ox}}{\epsilon_{\rm Si}}\frac{\partial I_L}{\partial E_m}\,\delta V_{\rm fb} . \tag{10}$$

Therefore, the leakage current spectral density is

$$S_L = 4\left(\frac{C_{\rm ox}}{\epsilon_{\rm Si}}\right)^2\left(\frac{\partial I_L}{\partial E_m}\right)^2 S_{V_{\rm fb}} . \tag{11}$$

Since the flatband voltage spectral density is $S_{V_{\rm fb}} = S_{Q_{ss}}/(WLC_{\rm ox}^2)$, where $S_{Q_{ss}}$ is the interface charge spectral density,[15] Eq. (11) becomes

$$S_L = \frac{4}{\epsilon_{\rm Si}^2}\left(\frac{\partial I_L}{\partial E_m}\right)^2 \frac{S_{Q_{ss}}}{WL} . \tag{12}$$

For a single trap with a time constant τ and concentration N_t, $S_{Q_{ss}}$ is given by the relationship[16]

$$S_{Q_{ss}} = \frac{q^2 kT 4\tau N_t}{1+(2\pi\tau f)^2} . \tag{13}$$

For a continuous energy distribution of the trapping states with a distribution of time constants $g(\tau)$, the leakage current noise spectral density is given by

$$S_{Q_{ss}} = q^2 kTN_t \int_{\tau_1}^{\tau_2} \frac{4\tau g(\tau)\,d\tau}{1+(2\pi\tau f)^2} . \tag{14}$$

For uniform trap distribution of constant density N_d, the distribution of time constants is $g(\tau) = A/\tau$, where $A = \log(\tau_1/\tau_2)$, which in practical cases has the value of 0.1.[17] After analytical solution of the integral in Eq. (13),[14] using Eqs. (1) and (12), we obtain the following expression for the leakage current noise spectral density:

$$S_L = \frac{\beta^2 N_d}{\epsilon_{\rm Si}^2 E_m WL}\frac{q^2 A}{f} I_L^2 . \tag{15}$$

Since the leakage current increases with increasing the electric field E_m [Eq. (1)], from the above equation follows that the power spectral density S_L is proportional to I_L^γ with the exponent $\gamma < 2$, i.e., $S_L \times E_m$ should be proportional to I_L^2. Plots of $S_L \times E_m$ versus I_L for the n-channel and p-channel polysilicon TFTs are shown in Fig. 10. The experimental data lie on straight lines proportional to I_L^2 showing the validity of Eq. (15). From these straight lines and Eq. (15), we determine the trap densities $N_d = 3\times10^{12}$ cm^{-2} for the p-channel and $N_d = 2\times10^{11}$ cm^{-2} for the n-channel polysilicon TFTs which are in excellent agreement with the values extracted from the on-state current activation energy data (Fig. 7).

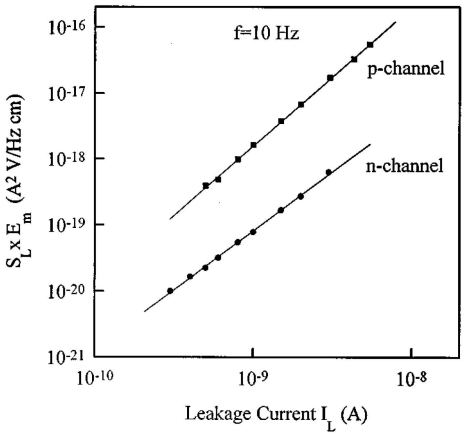

FIG. 10. Plots of $S_L \times E_m$ vs the leakage current I_L of typical n-channel and p-channel polysilicon TFTs. The noise power spectral density S_L was measured at the frequency of 10 Hz.

IV. CONCLUSIONS

In this article we have clarified the conduction mechanisms of the off-state current in n-channel and p-channel undoped hydrogenated polysilicon TFTs. The presented results indicate that the leakage current is caused by the drain junction. The junction leakage current is due to two basic mechanisms, pure thermal generation at low electric fields and field-assisted Poole–Frenkel emission accompanied by thermal field emission at high electric fields. The leakage current is correlated with the grain boundary and the gate oxide/polysilicon interface traps determined from the on-state current activation energy data. In addition to the electric field strength in the drain junction, it is confirmed that the main factor determining the leakage current is the deep levels with uniform energy distribution within the silicon band gap known by a previous analysis. The origin of the leakage current was also identified by low-frequency noise measurements. The article shows clearly that the analytical model developed for the leakage current noise spectral density provides a prediction for the grain boundary trap density. The substantially lower leakage current observed in the n-channel polysilicon TFT has been attributed to positive fixed charges at the interface near the drain junction which suppress the electric field.

ACKNOWLEDGMENTS

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