

CMOS Circuits for Peripheral Circuit Integrated Poly-Si TFT LCD Fabricated at Low Temperature Below 600°C

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Abstract—CMOS shift registers, buffers, and gray-scale representation circuits for integrated peripheral drive circuits of poly-Si TFT LCD's were fabricated at low temperature below 600°C on a glass substrate. The maximum operation frequency of the CMOS shift register was 1.25 MHz. The total power consumption of the 10-stage CMOS shift registers at a clock frequency of 46.8 kHz and a power supply voltage of 20 V was 10 μ W, which is three orders of magnitudes smaller than that of the 10-stage nMOS shift registers. The rise and fall times of the CMOS buffers were proportional to the inverse of the channel width, and the write time t_w of the gray-scale representation circuits was proportional to the line memory capacitance.

I. INTRODUCTION

INTEREST in polycrystalline-silicon (poly-Si) thin-film transistor (TFT) addressed liquid-crystal displays (LCD's) is increasing, especially in low-temperature processed poly-Si TFT's deposited on a glass substrate [1]–[6]. These poly-Si TFT's have a high-field effect mobility of the order of 30 $\text{cm}^2/\text{V} \cdot \text{s}$, making the realization of large-area and high-resolution displays possible [7]. Furthermore, peripheral drive circuits can be integrated through the use of these poly-Si TFT's [2], [4], [5], [8]–[12], reducing the number of external driver LSI's and external connections. These reductions would lead to a large improvement in reliability and potential cost reduction for the display. Therefore, high-resolution, low-cost, and compact TFT LCD's should be possible in the near future.

We previously reported that it is possible to integrate peripheral circuits by using only n-channel TFT's fabricated at low temperature below 600°C on a glass substrate [2], [11]. These peripheral circuits with only n-channel TFT's, however, have the following shortcomings: 1) large power consumption and 2) low maximum-operation frequency.

To overcome these shortcomings, CMOS circuits are suitable [12], [13] and a few reports are available [4], [7], [14], [15]. However, detailed characteristics of low-tem-

perature-processed poly-Si CMOS circuits have not yet been reported [4].

In the present paper, we describe electrical characteristics of the CMOS circuit fabricated at low temperature (below 600°C) on a glass substrate. In particular, electrical characteristics of CMOS inverters, CMOS shift registers, CMOS buffers, and gray-scale representation circuits are discussed.

II. CHARACTERISTICS OF n- AND p-CHANNEL POLY-Si TFT's

Fig. 1 shows a cross-sectional view of an n-channel poly-Si TFT fabricated by the low-temperature process technology (below 600°C) on a glass substrate [1], [5]. For a p-channel poly-Si TFT, the n^+ regions should be replaced by the p^+ regions. These TFT's have a conventional self-aligned gate MOSFET structure. A poly-Si active layer 150 nm thick and a poly-Si gate 100 nm thick were fabricated through the following procedure: 1) Low-pressure chemical vapor deposition (LPCVD) at 550°C was employed to obtain amorphous Si layer, and subsequent thermal annealing for 20–24 h in N_2 atmosphere at 600°C transformed these layers into the polycrystalline phase. The TEM observations of annealed poly-Si surfaces and cross sections showed that the maximum grain size was about 500 nm and that the grains were columnar [5]. 2) A SiO_2 gate insulator 100 nm thick was deposited by atmospheric-pressure chemical vapor deposition (APCVD) at 500°C. The breakdown electric field strength of the SiO_2 was $5\text{--}7 \times 10^6 \text{ V/cm}$, so that the quality of APCVD SiO_2 was apparently inferior to that of thermally grown SiO_2 . 3) The drain and source regions were formed by phosphorus-ion implantation for n-channel TFT's and by boron-ion implantation for p-channel TFT's. Phosphorus ions were implanted at a dose of $5 \times 10^{15} \text{ cm}^{-2}$ with energy of 30 keV. On the other hand, boron ions were implanted at a dose of $5 \times 10^{15} \text{ cm}^{-2}$ with energy of 20 keV. 4) After the deposition of phospho-silicate glass ($\text{PSG: SiO}_2 + \text{PH}_3$, 600 nm) for passivation, thermal annealing was carried out at 600°C for 20 h in N_2 atmosphere to activate implanted ions. 5) In order to improve the electrical characteristics of these poly-Si TFT's, i.e., to increase the field effect mobility μ_{FE} , and to reduce the

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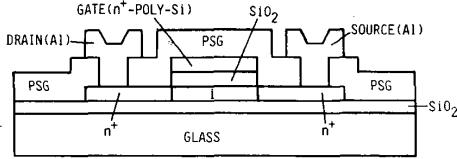


Fig. 1. Cross-sectional view of an n-channel poly-Si TFT (for a p-type poly-Si TFT, n^+ regions should be replaced by p^+ regions).

threshold voltage V_T and the leakage current (the off current) I_{off} , the poly-Si TFT's were passivated in a hydrogen plasma. This passivation process was carried out in a capacity-coupled-type plasma CVD (13.56 MHz and 300 W) at 300°C for 60 min under pressure of 0.75 torr in pure H_2 atmosphere. In the experiments, it was found that hydrogen penetrated through the PSG (600 nm) and the gate oxide (100 nm) easily, and that a thick poly-Si gate of more than 200 nm prevented hydrogenation of the poly-Si active layer. Therefore, thinning the poly-Si gate below 100 nm was necessary to realize effective hydrogenation of the channel region under the poly-Si gate.

Figs. 2 and 3 show the drain current versus gate voltage (I_D - V_G) characteristics of n- and p-channel TFT's, respectively. Here, the channel width W was 10 μm and the channel length L was 10 μm , and the drain voltage V_D was varied as 10, 5, and 0.1 V for n-channel TFT's and as -10, -5, and -0.1 V for p-channel TFT's. In the figures, V_G is defined by the voltage between the gate and source terminals, and I_D is the current flowing from the drain terminal to the source terminal. Field-effect mobility was calculated from the conductance in the linear region ($V_D = 0.1$ V). Threshold voltage was determined from the interpolated curve of the $\sqrt{I_D}$ - V_G characteristics in the saturated region ($V_D = 10$ V). The maximum field effect mobilities μ_{FE} of n- and p-channel TFT's were 35 and 30 $cm^2/V \cdot s$, respectively, and the threshold voltages V_T of n- and p-channel TFT's were 8.5 and -16 V, respectively. After the hydrogenation process, μ_{FE} was increased by 24% and V_T was decreased by 5 V in the n-channel TFT's. On the other hand, in the p-channel TFT's, μ_{FE} was increased by 11% and V_T was decreased by -4 V. When the channel length L of poly-Si is smaller than 10 μm , μ_{FE} tends to increase and V_T tends to decrease due to the short-channel effect. Therefore, short-channel devices with $L < 10 \mu m$ seem promising candidates for the integrated peripheral circuits. However, in the fabricated TFT's with the channel length of 10 μm , a probability of thermal breakdowns was increased due to drain breakdowns in the drain voltage region 20-30 V. From these characteristics, the TFT's with channel length of 10 μm was adopted. Moreover, in large-area displays, the devices with channel length of 10 μm are advantageous, because limitation due to photolithography is less severe.

The stability of the fabricated TFT's was tested at 50°C in air using the two mode biases, i.e., continuous on-state ($V_G = 20$ V, $V_D = 10$ V) bias and continuous off-state ($V_G = 0$ V, $V_D = 10$ V) bias. The results showed that

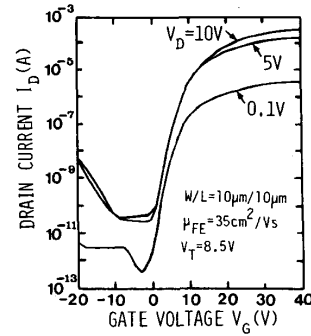


Fig. 2. I_D - V_G characteristics of n-channel TFT with V_D as a parameter.

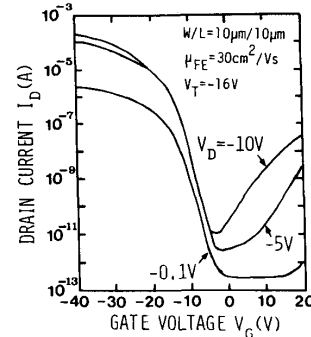


Fig. 3. I_D - V_G characteristics of p-channel TFT with V_D as a parameter.

TFT's were stable for more than 300 h, and maximum changes of I_{on} , I_{off} , V_T , and μ_{FE} were -4, ± 30 , ± 0.03 , and $\pm 2\%$, respectively.

III. TARGET DISPLAY CONFIGURATION

Fig. 4 shows a schematic diagram of the integrated peripheral circuit configuration of a target TFT LCD display. The TFT's for integrated peripheral circuits as well as the pixel TFT's are fabricated on glass at a low temperature below 600°C. The number of pixels is 1120 $\times$ 780, where one pixel is composed of three dots corresponding to red, green, and blue primary colors. The scan drive circuits consist of shift registers and buffers. The data drive circuits consist of shift registers, divided matrix switches, and gray-scale representation circuits. The scan drive circuits are connected to the gate bus, and the data drive circuits are connected to the drain bus.

The necessary clock frequency f_{CP} for the integrated scan drive circuits of a 780 scan-line display driven at 60 Hz is 46.8 Hz. On the other hand, the necessary clock frequency f_{CP} for integrated data drive circuits of (1120 $\times$ 3) $\times$ 780 dot display driven at 60 Hz is 157 Hz, which is too high to be realized even with the crystalline-silicon circuits. In order to decrease the necessary clock frequency, divided matrix switches should be employed [2], [10], [11]. Here, we discuss the case that the data drive

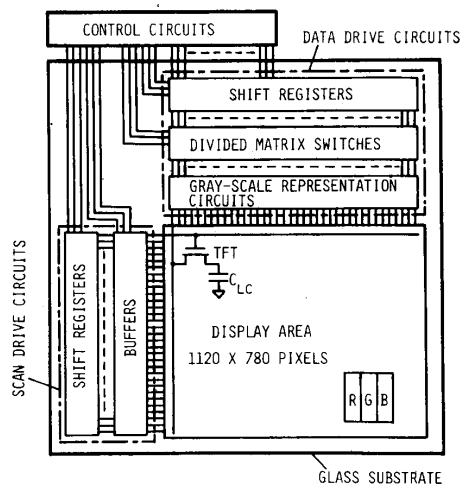


Fig. 4. Schematic diagram of integrated peripheral drive circuit configuration.

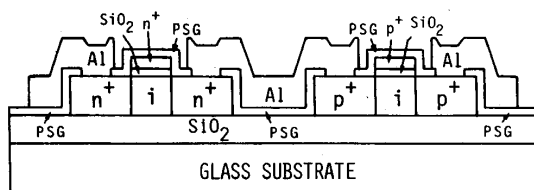


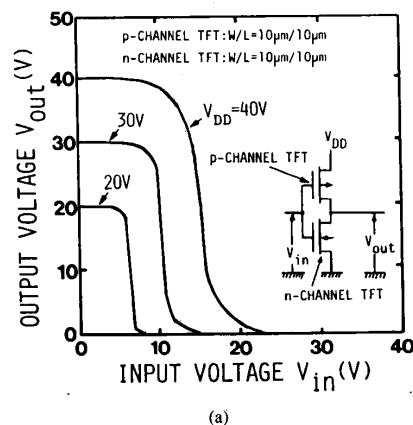
Fig. 5. Cross-sectional view of CMOS inverter.

circuits are divided into 20 blocks with 168 data circuits in each block. Then, the necessary clock frequency becomes 0.94 MHz, which is attainable by using low-temperature-processed poly-Si TFT's.

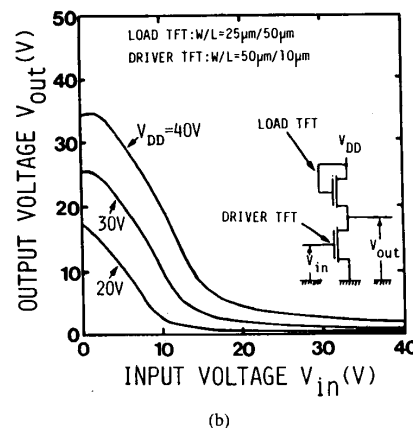
IV. CMOS INVERTER CHARACTERISTICS

In this section we discuss CMOS inverter characteristics in comparison with nMOS inverter characteristics, since inverters constitute the main parts of the peripheral circuits. Fig. 5 shows a cross-sectional view of the CMOS inverter. Fig. 6(a) and (b) shows transfer characteristics of the CMOS and nMOS inverters, respectively, with the power supply voltage V_{DD} as a parameter. Here, the x-axis indicates the input voltage V_{in} , varied from 0 to 40 V, and the y-axis indicates the output voltage V_{out} . The circuit configuration and definitions of V_{in} , V_{out} , and V_{DD} are shown in the figure. In the CMOS inverter, W/L of the p-channel TFT is $10\ \mu\text{m}/10\ \mu\text{m}$ and W/L of the n-channel TFT is $10\ \mu\text{m}/10\ \mu\text{m}$. On the other hand, in the nMOS inverter, W/L of the load TFT is $25\ \mu\text{m}/50\ \mu\text{m}$ and W/L of the driver TFT is $50\ \mu\text{m}/10\ \mu\text{m}$.

We discuss the $V_{DD} = 30\ \text{V}$ case. In the CMOS inverter, V_{out} is 30 V when V_{in} is 0 V, and V_{out} is 0 V when V_{in} is 20 V. In the nMOS case, V_{out} is 25 V when V_{in} is 0 V, and V_{out} is still 2.5 V when V_{in} is 20 V. From these data, we find that the amplitude of V_{out} in the CMOS in-



(a)



(b)

Fig. 6. Transfer characteristics of CMOS and nMOS inverters. (a) CMOS inverter. (b) nMOS inverter.

verter is larger than that in the nMOS inverter. Furthermore, a small-signal gain within the transition region in the CMOS inverter is higher than that in the nMOS inverter. Therefore, characteristics of the CMOS inverter are superior to those of the nMOS inverter.

V. CMOS SHIFT REGISTER CHARACTERISTICS

In the following discussion, we concentrate on shift registers and buffers, because characteristics of peripheral circuits are mainly governed by those of shift registers and buffers [2]. Fig. 7(a) and (b) shows circuit configuration and timing sequence of the CMOS and nMOS shift registers, respectively. In the CMOS shift registers, the two-phase dynamic-ratioless type was employed, where only two transfer-gate transistors and two inverters were used to make a single shift register. On the other hand, in the nMOS shift registers, the two-phase dynamic-ratio type was used.

Fig. 8 shows the output voltage versus the clock frequency ($V_{out}-f_{CP}$) characteristics of the CMOS and nMOS shift registers. In the CMOS shift registers, W/L of the

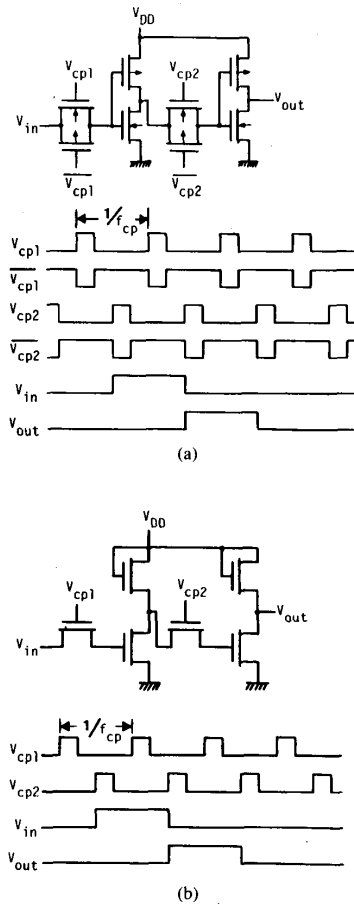


Fig. 7. Circuit configuration and timing sequence of CMOS and nMOS shift registers. (a) CMOS shift register. (b) nMOS shift register.

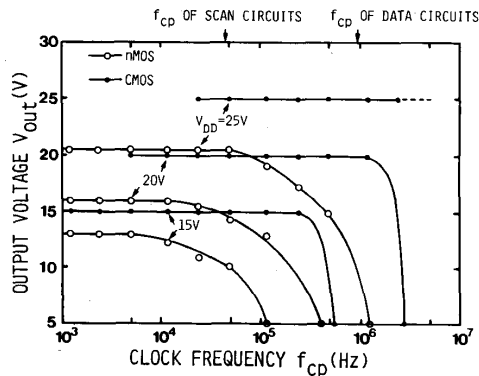


Fig. 8. Output voltage versus clock frequency (V_{out} - f_{CP}) characteristics of CMOS and nMOS shift registers.

n-channel TFT is $10\ \mu\text{m}/10\ \mu\text{m}$ and W/L of the p-channel TFT is $10\ \mu\text{m}/10\ \mu\text{m}$. On the other hand, in the nMOS shift registers, W/L of the load TFT is $25\ \mu\text{m}/$

$50\ \mu\text{m}$, W/L of the driver TFT is $50\ \mu\text{m}/10\ \mu\text{m}$, and W/L of the transfer gate TFT is $50\ \mu\text{m}/10\ \mu\text{m}$. The load capacitance C_L was set at $0.02\ \text{pF}$, which corresponds to the input capacitance of the picoprobe.

In the CMOS shift registers, the power supply voltage V_{DD} corresponds to the voltage heights of the clock pulses V_{CP1} , V_{CP1} , V_{CP2} , and V_{CP2} . On the other hand, in the nMOS shift registers, the voltage heights of V_{CP1} and V_{CP2} are always set at $20\ \text{V}$ for any V_{DD} . As an example, we discuss the $V_{DD} = 20\ \text{V}$ case, because $20\ \text{V}$ is an allowable maximum voltage in typical driver LSI's.

In the CMOS shift registers, indicated by closed circles, the output voltage V_{out} is $20\ \text{V}$ over a wide frequency range and the maximum operation frequency is $1.25\ \text{MHz}$. This value is larger than $0.94\ \text{MHz}$, necessary to drive data drive circuits of the display with $(1120 \times 3) \times 780$ dots at the frame frequency of $60\ \text{Hz}$. On the other hand, in the nMOS shift registers, indicated by open circles, the output voltage V_{out} is reduced down to $16\ \text{V}$ and the maximum operation frequency is only $25\ \text{kHz}$, too small for the present purpose. The maximum operation frequency was mainly restricted by the input gate capacitance of the TFT's, C_G , not by the load capacitance C_L , because the value for C_L was smaller than that for C_G : The C_G is $0.07\ \text{pF}/\text{stage}$ in CMOS shift registers and $0.17\ \text{pF}/\text{stage}$ in nMOS shift registers. On the other hand, C_L is $0.02\ \text{pF}$ in the experiment.

Fig. 9 shows the total power consumption versus clock frequency (P_s - f_{CP}) characteristics of the CMOS and nMOS 10-stage shift registers with the power supply voltage V_{DD} as a parameter. The clock frequency was varied from $12.5\ \text{kHz}$ to $2.5\ \text{MHz}$. Open circles indicate the results of the nMOS shift registers and closed circles indicate the results of the CMOS shift registers.

The total power consumption P_s of the CMOS shift registers was linearly proportional to f_{CP} . On the other hand, the P_s of the nMOS shift registers did not depend on the frequency. The reason for this behavior is as follows: As shown in Fig. 7(b), there exist two nMOS inverters per stage in the nMOS shift registers. At any operation mode, one of the two inverters is kept in the on-state, where a current from V_{DD} to the ground flows through. The power consumption due to this current, which is frequency-independent, is found to be much larger than the frequency-dependent power consumption within the nMOS shift registers.

Power consumptions at the two cases of clock frequency are discussed in the following: 1) $f_{CP} = 46.8\ \text{kHz}$ and 2) $f_{CP} = 0.94\ \text{MHz}$. As discussed in Section III, case 1) corresponds to the operation frequency of the integrated scan drive circuits and case 2) corresponds to the operation frequency of the integrated data drive circuits. First, we discuss the $f_{CP} = 46.8\ \text{kHz}$ case. The total power consumption of the CMOS shift registers is approximately three order of magnitudes smaller than that of the nMOS shift registers. In particularly, when V_{DD} is $20\ \text{V}$, the power consumption is $10\ \mu\text{W}$ in the CMOS shift registers and $8\ \text{mW}$ in the nMOS shift registers. In the nMOS

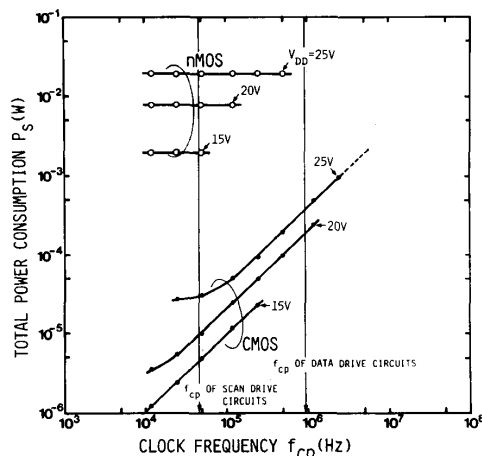


Fig. 9. Power consumption versus clock frequency (P_S - f_{CP}) characteristics of CMOS and nMOS shift registers.

shift registers, the total power consumption can be reduced by decreasing the W/L ratio of the load TFT. However, the W/L ratio must be larger than or equal to $25\ \mu\text{m}/50\ \mu\text{m}$, i.e., 0.5 in order to smoothly transfer signals to the level shifters in the integrated scan drive circuits [11]. Therefore, other means must be introduced. One such candidate is a ratioless-type shift register where no dc currents flow.

Next, we discuss the $f_{CP} = 0.9\ \text{MHz}$ case. At this clock frequency, the nMOS shift registers did not operate. On the other hand, in the CMOS shift registers, the total power consumption was $160\ \mu\text{W}$ when $V_{DD} = 20\ \text{V}$.

VI. CMOS BUFFER CHARACTERISTICS

Fig. 10 shows the channel width dependence of the rise time t_r and fall time t_f of the output signal in the CMOS buffer, which is made of a CMOS inverter as shown in the inset. The rise time t_r is defined by the 10 to 90% rise time and fall time t_f is defined by the 90 to 10% fall time. The channel width W was varied from 10 to $50\ \mu\text{m}$. The experimental conditions were as follows: The load capacitance C_L was set at $110\ \text{pF}$, which corresponds to the capacitance per one gate line of the display with (1120×3) data lines. The power-supply voltage V_{DD} is taken to be $20\ \text{V}$, which is an allowable maximum value in typical driver LSI's.

From the figure, we find that both t_r and t_f are inversely proportional to W , and at $W = 50\ \mu\text{m}$, t_r and t_f are 18 and $5\ \mu\text{s}$, respectively. The main reason why t_r is larger than t_f is that the threshold voltage of the p-channel TFT is larger than that of the n-channel TFT. Based on these results, we estimated the values for channel widths of the p- and n-channel TFT's in the CMOS buffer for integrated scan drive circuits of a $(1120 \times 3) \times 780$ dot display. In the 780-scan-line display driven at the frame frequency of $60\ \text{Hz}$, the select time of one scan line becomes $21.4\ \mu\text{s}$. Since the rise time t_r and fall time t_f must be smaller than

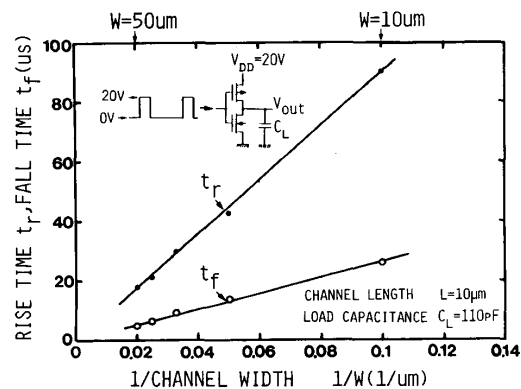


Fig. 10. Channel width dependence of rise time t_r and fall time t_f of output signal in CMOS buffer.

5% of the scan select time in the present design, t_r and t_f must be smaller than $1\ \mu\text{s}$. Therefore, the channel widths of p- and n-channel TFT's must be larger than 900 and $250\ \mu\text{m}$, respectively. However, the channel width W of $900\ \mu\text{m}$ in the p-channel TFT is too large for the CMOS buffer. The reason is as follows: When the value for the load capacitance is larger than $1\ \text{pF}$, which corresponds to the value for the input gate capacitance of TFT's with $W = 300\ \mu\text{m}$ and $L = 10\ \mu\text{m}$, the drivability of the fabricated CMOS shift registers is not good enough for the scan drive circuits. When the channel width W of the p-channel TFT in CMOS buffer is taken to be $900\ \mu\text{m}$, the input gate capacitance becomes nearly equal to $3\ \text{pF}$, which is too large to obtain a reasonable drivability. Therefore, W must be reduced. To realize this, it is necessary to reduce the threshold voltage of the p-channel TFT down to the value of that of the n-channel TFT. This should be realized by optimizing the deposition conditions.

VII. GRAY-SCALE REPRESENTATION CIRCUIT CHARACTERISTICS

In this section, we discuss the characteristics of gray-scale representation circuits. It is not easy to fabricate integrated data drive circuits with gray-scale representation, because analog voltages for analog data must be treated in order to obtain more than eight gray scales. We fabricated the integrated peripheral drive circuits with four gray-scale (64 colors) representation by using the multi-level selectors [11]. This method is not suitable for the integrated peripheral circuits with more than eight gray scales, i.e., 512 colors, because of the available space limitation. In addition, the integration of operational amplifiers in data drive circuits with gray-scale representation is not desirable, because the fabrication of operational amplifiers by using poly-Si TFT's is much more difficult than that by using crystalline Si TFT's and the power dissipation of operational amplifiers is large. To overcome these difficulties, we propose the following cir-

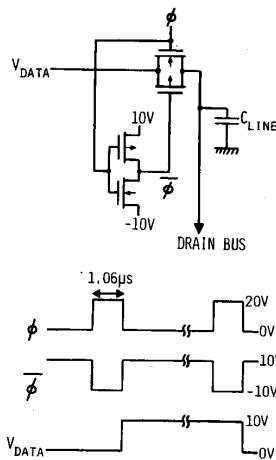


Fig. 11. Circuit configuration and timing sequence of gray-scale representation circuit.

cuits for the integrated data drive circuits with more than eight gray-scale representation.

Fig. 11 shows a circuit configuration and timing sequence of the gray-scale representation circuit, which consists of one CMOS transfer gate TFT, one CMOS inverter, and one line memory capacitance C_{LINE} . In this circuit, the CMOS transfer gate TFT's correspond to the divided matrix switches. In the figure, ϕ is the output signal voltage of the shift registers, varied from 0 to 20 V, $\bar{\phi}$ is the inverse signal voltage of ϕ , varied from -10 to 10 V, and V_{DATA} is the data signal voltage, varied from 0 to 10 V. In ϕ and $\bar{\phi}$, the pulsewidths of the on-state is taken to be 1.06 μ s, which corresponds to the value of the inverse of the operation frequency of the integrated data drive circuits, i.e., $1/0.94$ MHz.

Fig. 12 shows the line memory capacitance dependence of the write time t_w in the gray-scale representation circuits. The write time t_w is defined by the 10–95% rise time, i.e., the time duration for 1–9.5 V change, because brightness versus voltage ($B-V$) curves saturate above 9.5 V in the present display which uses the twisted-nematic liquid crystals. In the experiment, ϕ was applied to the gate of p-channel TFT in the CMOS transfer gate TFT. The W/L ratios of the n- and p-channel TFT's were 100 μ m/10 μ m. From the figure we find that t_w is proportional to the line memory capacitance C_{LINE} . We discuss the $C_{LINE} = 100$ pF case. With this value for C_{LINE} , the voltage drop of analog data on drain bus can be prevented even when the leak resistance between one drain bus and 780 gate buses is of the order of megaohms. When C_{LINE} is 100 pF, the write time t_w is 9.0 μ s. However, the write time t_w must be smaller than the gate pulsewidth in the transfer gate TFT, 1.06 μ s. In order to realize this, the threshold voltage of p-channel TFT must be reduced down to the level of n-channel TFT. Then the on-current of the p-channel TFT would be increased by one order of magnitude and t_w would become smaller than 1.06 μ s.

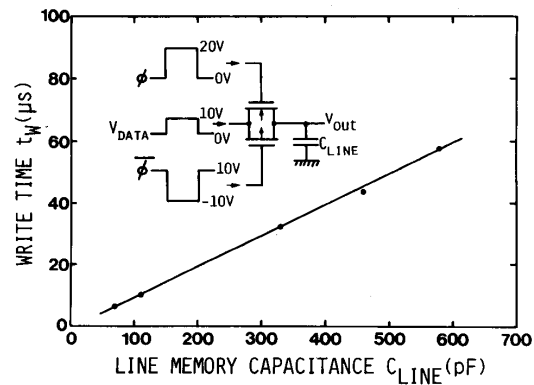


Fig. 12. Line memory capacitance dependence of write time t_w in gray-scale representation circuit.

VIII. CONCLUSION

CMOS shift registers, buffers, and gray-scale representation circuits for integrated peripheral drive circuits of poly-Si TFT LCD's were fabricated at low temperature below 600°C on a glass substrate. The electrical characteristics of the CMOS shift registers were as follows: 1) The maximum operation frequency was 1.25 MHz when the power supply voltage was 20 V with the load capacitance of 0.02 pF. 2) The total power consumption was 10 μ W when clock frequency is 46.8 kHz and the power supply voltage is 20 V. From these results, the fabricated CMOS shift registers are considered to be promising candidates for integrated peripheral circuits of poly-Si TFT LCD's with $(1120 \times 3) \times 780$ dots.

In the CMOS buffers, made of CMOS inverters, the following electrical characteristics were obtained: 1) Both the rise time t_r and fall time t_f were proportional to the inverse of the channel width W . 2) In the case of $(1120 \times 3) \times 780$ dot display driven at 60 Hz, the necessary channel widths of the p- and n-channel TFT's must be larger than 900 and 250 μ m, respectively. However, the channel width of 900 μ m is too large for the integrated peripheral circuits and must be reduced. To realize this, the threshold voltage of the p-channel TFT's must be reduced to the values of the threshold voltage of the n-channel TFT's.

In the gray-scale representation circuits with more than eight gray scales (≥ 512 colors), the following electrical characteristics were obtained: 1) The write time t_w was proportional to the line memory capacitance C_{LINE} . 2) When C_{LINE} was 100 pF, the write time t_w took 9.0 μ s, which is larger than the gate pulsewidth in transfer gate TFT, i.e., 1.06 μ s. Therefore, similarly to the CMOS buffer case, the threshold voltage of the p-channel TFT must be lowered to that of the n-channel TFT.

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