

Polysilicon TFT Circuit Design and Performance

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Abstract—Polysilicon thin-film technology is becoming increasingly attractive for active-matrix liquid-crystal displays (AMLCD's) and other large-area electronic devices, primarily because polysilicon thin-film transistors (TFT's) can be used to build integrated drive and interface circuitry on large-area substrates. Both n- and p-channel polysilicon TFT's can be fabricated, allowing CMOS circuit techniques to be used. However, TFT characteristics are poor in comparison to conventional single-crystal MOSFET's, and relatively coarse design rules must be used to be compatible with processing on large-area glass plates (more than 30 cm × 30 cm), and these limitations present a number of challenges for circuit design. This paper examines these issues and describes the performance of a range of digital and analog circuit elements built using polysilicon TFT's. Digital circuit speeds in excess of 20 MHz are reported, along with operational amplifiers with over 80 dB of gain and more than 1-MHz unity-gain frequency. Several polysilicon TFT switched-capacitor circuits are also reported and shown to have adequate linearity, output swing, and settling time to form integrated data line drivers on an AMLCD.

I. INTRODUCTION

INTEREST in circuits built using polysilicon thin-film transistors (TFT's) has recently increased for several reasons. Although the inferior performance of these devices in comparison to conventional single-crystal MOSFET's is well documented [1]–[4], they have the important advantage of being compatible with fabrication on large-area glass or quartz substrates (more than 30 cm × 30 cm). This makes TFT's usable in applications where the physical size of the circuit must be large, for example if the circuit is an active-matrix liquid-crystal display (AMLCD) [4]–[6], a page-width optical scanner [7], [8] or a page-width print head [9]. Although there have been many reports of particular devices incorporating polysilicon TFT's and TFT circuits [4]–[8], there has been little work published so far concentrating specifically on the underlying design issues and performance capabilities of polysilicon TFT circuits. This paper, like the ISSCC presentations on which it expands [2], [10], is intended to focus on these subjects. The work described here does not deal with a complete large-area polysilicon TFT electronic device, but rather examines the performance of a range of basic circuit elements, some of which are already used in applications, and some of which show promise for increased functionality on large-area substrates in the future.

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The most common, and the most important, application of polysilicon TFT's remains AMLCD's. As the various circuit elements are discussed in this paper, therefore, their performance will be compared with AMLCD driving requirements. In order to do this, typical drive circuits for AMLCD's are briefly reviewed in Section IV. It should be noted, however, that there are other applications for these devices, and more are likely to present themselves as the technology matures and TFT circuit performance improves.

II. POLYSILICON THIN-FILM TECHNOLOGY

In this section, the main features of polysilicon thin-film technologies are reviewed. Fig. 1 shows cross sections of n- and p-channel polysilicon TFT's along with an integrated capacitor. The TFT's themselves are very similar to single-crystal silicon-on-insulator (SOI) MOSFET's, except that the active silicon layer is polycrystalline instead of monocrystalline. Polysilicon technology also has several of the advantages of SOI, including excellent interdevice isolation and negligible parasitic capacitance. The capacitor is formed between the gate and active polysilicon layers by the addition of a single implant to dope the active polysilicon layer under the gate. The structure is similar in layout to a polysilicon-to-diffusion capacitor in a conventional single-crystal MOS technology, but in this case there is negligible parasitic capacitance associated with either electrode. Both plates of the capacitor can be sufficiently heavily doped that the series resistance remains low, and the capacitance does not vary significantly over the bias ranges typically found in large-area devices.

There are several broad types of polysilicon TFT technology, differentiated by the annealing process used to crystallize the active polysilicon layer and the maximum processing temperature used [3], [11]. High-temperature technologies typically use furnace annealing, and at least one high-temperature process step (often during the gate dielectric formation), and this restricts the choice of substrate material to quartz. Furnace annealed low-temperature technologies use a similar process to the high-temperature technologies, but keep the maximum processing temperature less than about 600°C in order to allow the use of lower cost glass substrates. A third technology variant uses laser annealing to achieve recrystallization and is also compatible with low-cost glass substrates. The laser annealed polysilicon TFT's have been shown to offer the best performance, although the technology is not

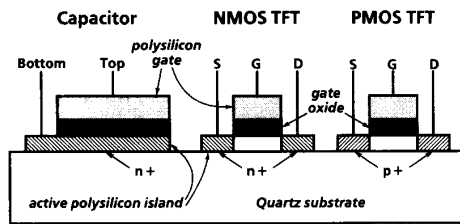


Fig. 1. Polysilicon TFT's with integrated capacitor.

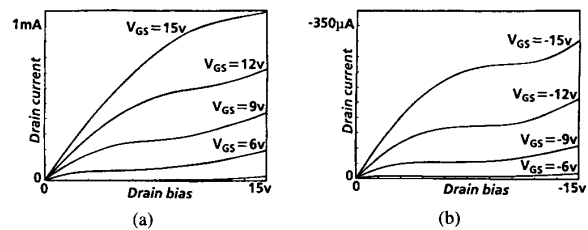
yet mature and poor consistency and uniformity remain significant problems. High-temperature quartz-based technologies are relatively mature, offer good TFT performance, and are used for small viewfinder or projection displays. Low-temperature glass-based technologies offer low cost, although the TFT performance is not usually as good as can be achieved with high-temperature technologies [12].

The results reported in this paper were obtained using relatively conventional high- and low-temperature furnace recrystallized polysilicon thin-film devices fabricated at Xerox PARC. The experimental circuits were fabricated on quartz wafers, although the process conditions and design rules are the same as those used with large-area substrates. The device performance achieved is comparable with the best reported for similar technologies by other authors [1], [4]–[8], [11]. Although, as discussed below, the TFT characteristics are inferior to conventional single-crystal MOSFET's, useful circuit performance can still be achieved. As laser annealed technologies mature, even greater circuit functionality is likely to become possible.

The circuits reported below were all designed using layout rules that are relatively coarse in comparison with those used in single-crystal technologies. There are several reasons for this. First, of course, are the photolithographic and processing restrictions imposed by the need to fabricate the TFT's on very large-area substrates. Second, short-channel effects are relatively severe in polysilicon TFT's, particularly at high drain voltages [13]. Third, most large-area devices are constrained to operate at supply voltages of at least 15 V; an AMLCD pixel, for example, typically requires a total voltage swing of about 10 V to encompass both drive polarities [14], and with sufficient headroom to achieve this using polysilicon TFT drivers means a supply voltage of about 15 V.

III. POLYSILICON TFT CHARACTERISTICS

Fig. 2 shows simple I - V characteristics for n- and p-channel TFT's fabricated using the high-temperature process; devices fabricated with the low-temperature technology are qualitatively similar although the drive currents are lower. The poor saturation arises through a similar mechanism to that responsible for the kink effect in SOI MOSFET's [15], that is, channel avalanche multiplication occurring in the high-field region near the drain combined with the floating body of the device. However,

Fig. 2. High-temperature polysilicon TFT characteristics ($W = 50 \mu\text{m}$, $L = 10 \mu\text{m}$). (a) NMOS. (b) PMOS.

in polysilicon TFT's there is an additional mechanism related to the high trap state density that exaggerates the effect of avalanche multiplication still further [16]. Since the poor saturation characteristics are not related to punchthrough or other breakdown effects, the off-state current is not affected. The impact on digital circuits is only minor, and the extra drain current even increases switching speeds slightly. However, the low output impedance presents a greater problem for analog circuit design where high impedances are needed to achieve good voltage gain.

The main weakness of polysilicon TFT's in comparison with single-crystal devices is their relatively low drive current, particularly in low-temperature devices. This can be seen from Fig. 2, and is further illustrated in Fig. 3 where the effective channel mobility is plotted as a function of normalized gate bias for both an n-channel polysilicon TFT and a conventional $2\text{-}\mu\text{m}$ gate length MOSFET. In each case the gate bias is normalized by the typical operating voltage for circuits built using the devices, 5 V for the MOSFET and 15 V for the polysilicon TFT. The peak MOSFET mobility is observed at a gate bias a little above threshold, and the degradation at higher gate bias is caused by increased surface scattering as the channel inversion layer is compressed by the increasing gate field. The TFT mobility is about an order of magnitude lower, and increases steadily as the gate drive rises until it saturates at a gate voltage of about 10 V; both the lower effective channel mobility and the gate bias dependence are due to the high trap state density in the device channel. The low drive current of the polysilicon TFT's has a significant effect on digital circuit speed, but in the analog case the effect is even more severe since transistors in amplifiers are typically biased with a low V_{GS} to keep V_{DSAT} low, and as Fig. 3 shows, under such conditions the effective TFT mobility is well below its peak value.

Another important device characteristic, particularly for analog circuit applications, is the noise performance, and in this respect polysilicon TFT's are again markedly inferior to single-crystal devices. Typical noise figures for polysilicon TFT's are about an order of magnitude higher than for conventional MOSFET's; at low frequencies (less than about 100 kHz) flicker noise dominates and shows roughly the same channel size dependence seen with MOSFET's. At higher frequencies, thermal noise dominates. The noise performance of polysilicon TFT's has

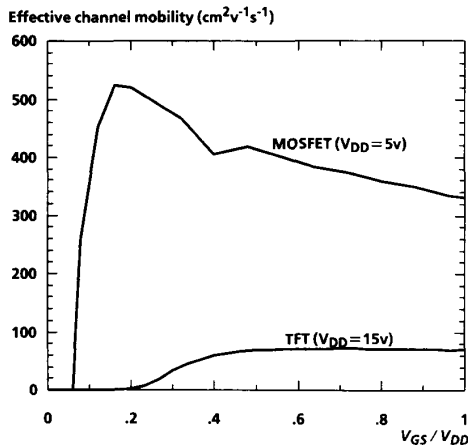


Fig. 3. Polysilicon TFT and single crystal MOSFET channel mobility. $V_{DS} = 0.1$ V, n-channel.

TABLE I
TECHNOLOGY COMPARISON

	Low-temperature poly-Si TFT	High-temperature poly-Si TFT	Conventional MOSFET
NMOS: V_T (V)	2	2	0.7
μ ($\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$)	40	100	500
PMOS: V_T (V)	-8	-3	-0.7
μ ($\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$)	20	50	200
Operating voltage (V)	18	15	5
Feature size (μm)	5	5	1
Substrate	LA glass	LA quartz	Si wafer

been discussed elsewhere [10], [17], and is not considered further here, except to note that since the frequency dependence is qualitatively similar to that obtained with conventional MOSFET's, the same switched-capacitor techniques used to suppress low-frequency noise in these devices are expected to be equally effective with TFT's.

Table I summarizes some of the main characteristics of polysilicon TFT's and compares them with typical values for conventional single-crystal MOSFET's. Data are shown for both low- and high-temperature processed TFT's. The low-temperature NMOS TFT's have lower channel mobility, and hence lower drive current, than their high-temperature counterparts, but otherwise are similar. However, the difference between low- and high-temperature p-channel TFT's is more marked. Not only is the channel mobility lower in the low-temperature device, but the threshold voltage is also much more negative, so that the drive current available from a low-temperature p-channel TFT is more than an order of magnitude lower than that available from a high-temperature device [12]. Despite the weak p-channel TFT's in the low-temperature technology, CMOS circuits are still often used for several reasons, including design simplicity, low power dissipa-

tion, good noise immunity, and the difficulty in fabricating depletion-mode NMOS devices to act as loads.

IV. DRIVE REQUIREMENTS FOR AMLCD's

This section reviews the main driving requirements for AMLCD's. These displays represent the major application area for polysilicon TFT's, and their drive requirements will be used to add perspective to the measured performance described below. Fig. 4 shows the main circuit elements of an AMLCD along with typical drive waveforms. The active matrix is composed of orthogonal scan and data lines, and a single pixel is formed at each intersection. Each pixel contains a TFT and a capacitor. The capacitor is formed by a pair of transparent electrodes sandwiching the liquid-crystal material. Plane polarizers are placed on each side of the cell so that incoming light is first polarized, then passes through the liquid crystal, and finally leaves via the second polarizer. The voltage applied to the capacitor controls the orientation of the liquid-crystal molecules, and this in turn controls the twist in the plane of polarization of the light traveling through the cell. In this way, the transmission of light through the entire module (liquid-crystal cell and polarizers) can be controlled [14]. When a scan line goes high, each TFT along that line is turned on and the voltages present on the data lines are transferred in parallel into all the pixels along that line, setting the required transmission pattern. When the scan line goes low again, the TFT is turned off, the charge remains on the pixel capacitance, and the pixel voltage remains fixed until it is rewritten during the next frame. The liquid-crystal capacitance is strongly voltage dependent and may not be large enough to store the pixel voltage until the next frame (charge can leak off both through the TFT and the liquid-crystal material), and in practice an additional storage capacitor is often added to the pixel to improve the storage time and linearity.

Conventional amorphous-silicon TFT AMLCD's use single-crystal integrated circuits to generate the drive waveforms illustrated in Fig. 4. A full-color 640×480 -pixel display requires about a dozen chips, and several thousand individual connections must be made between the active matrix substrate and the driver IC's. The driver IC's and the very large number of connections contribute significantly to the cost of the display, and also play an important role in determining long-term reliability. The use of polysilicon TFT's allows the driver circuits to be fabricated simultaneously with the active matrix on the same glass substrate, eliminating the need for external driver chips and greatly reducing the number of external connections needed to operate the display. In addition, integrated drivers allow much denser displays to be built, offering the possibility of physically small but high-pixel-count light valves for projection applications [18].

The function of the scan drivers is to generate the scan pattern, turning each scan line on in turn. This is usually accomplished by a simple shift register and buffers to drive the capacitive load presented by the scan lines. As Fig. 4

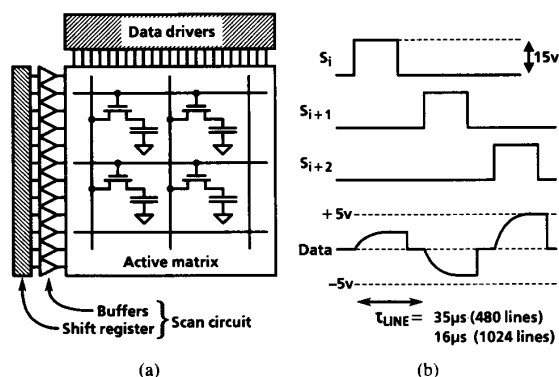


Fig. 4. AMLCD driving. (a) Main circuit elements of AMLCD. (b) Typical drive waveforms.

indicates, the total voltage swing needed on the gate lines is around 15 V; the scan frequency depends on the display size and video format, and is about 30 kHz for a progressive scan 480-line display and about 60 kHz with 1024 lines. The scan line buffer rise and fall times usually need to be around 1 μ s, although this depends somewhat on the display design and resolution. The capacitive load presented by a scan line can be very large, ranging from about 50 pF for a small projection display to as much as 500 pF for a large direct-view high-resolution display, and achieving fast enough transition times when driving such loads often requires very large buffers.

The data driver circuits are often even more challenging. They must perform serial-to-parallel conversion and drive the appropriate analog voltages onto the data lines. The voltage applied to the liquid-crystal cells must have a time-average value close to zero to prevent deterioration of the display, and to achieve this the voltage applied to each pixel is reversed every frame. The data driver voltage swing must be large enough to accommodate both drive polarities, normally requiring a total swing of about 10 V. The output settling time for the data drivers must be fast enough that once the data lines have reached their final values there is still time to transfer the signals into the pixels. In the case of polysilicon pixel TFT's, this transfer takes only a few microseconds [12], giving target settling times of about 30 μ s for a 480-line display and about 12 μ s with 1024 lines. The data-line capacitance is usually smaller than the scan-line capacitance, usually between about 20 pF for a small projection display and about 100 pF for a high-resolution direct-view display.

Fig. 5 illustrates two common data driver architectures. In the second [4], [6] (Fig. 5 (b)), analog video data are distributed along a common input line, which is linked via pass gates to the matrix data lines. The shift register turns each pass gate on in turn, and the analog input voltage present at that moment is transferred to the data line, where it remains stored on the data-line capacitance once the pass gate turns off. The rate at which data can be sampled from the analog input depends on the speed of the shift register generating the sample signals, and the speed

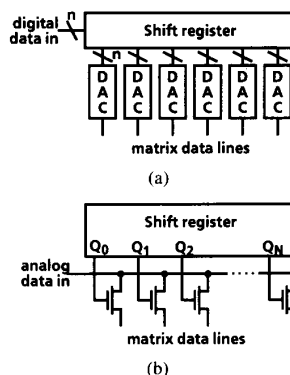


Fig. 5. AMLCD data driver architectures.

with which the data line can be charged via the pass gate; usually the latter limitation is the most severe. Normally, a separate analog input line is used for each color (red, green, blue), and on a large display several sets of input lines may be employed, each serving only a fraction of the data lines, in order to achieve the necessary data bandwidth. In the first architecture [5] (Fig. 5(a)), serial digital data are fed into the shift register. Once the register is fully loaded, the data are transferred in parallel to digital-to-analog converters (DAC's), which generate the appropriate analog signals to drive the data lines. The digital interface possible with such an architecture is very attractive, but the circuitry is far more complex than with the sampled analog architecture of Fig. 5(b).

V. DIGITAL CIRCUITS

This section describes the performance of some simple digital circuit elements built using both low- and high-temperature processed polysilicon TFT's. The circuits might be used, for example, as integrated addressing logic on large-area devices or for serial-to-parallel conversion of digital data.

A. Shift Registers

Fig. 6 illustrates the performance of simple polysilicon TFT CMOS dynamic shift registers built using devices with 5- and 10- μ m gate lengths; other features such as the TFT widths and interconnect line widths are scaled in line with the gate lengths. The inset to the figure shows one stage of the shift register; the two clock phases are generated by integrated polysilicon TFT buffers. The maximum clock frequency for error-free data transfer is determined by operating the shift register as a Johnson counter [19] and monitoring the ratio of clock and output frequencies; this provides a sensitive means of detecting the onset of misclocking as the frequency is increased. The maximum frequency achieved with the low-temperature devices is about 9 MHz with $L = 10 \mu$ m and about 15 MHz with $L = 5 \mu$ m; the high-temperature devices operate at higher clock rates due to their higher drive currents, with the circuits based on 5- μ m gate length TFT's

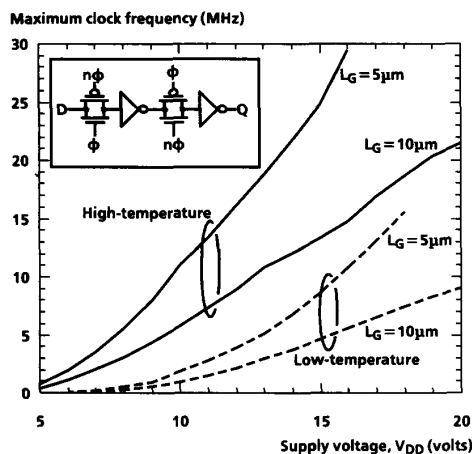


Fig. 6. Polysilicon TFT shift register maximum clock frequency for error-free data transfer.

reaching almost 30 MHz, and the $L = 10\text{-}\mu\text{m}$ circuits operating at up to 20 MHz.

Shift registers are used for both scan pattern generation and serial-to-parallel conversion of the input data stream in AMLCD's. The former application typically requires clock rates of less than 100 kHz (see Section IV), and static circuits are normally used. Static shift registers have been shown to be about 20% slower than dynamic circuits using the same TFT dimensions [2], and achieving the required scan rate is not normally an issue. Serial-to-parallel conversion of the input data is more challenging, and dynamic shift registers are more often used in order to achieve the highest possible speed. In both the architectures illustrated in Fig. 5, the shift register operates at the input data sampling rate. If this is less than the overall input data rate determined by the display pixel count and the frame rate, which is usually the case, then an input bus several pixels wide must be used. For example, a 480×640 -pixel display with a 60-Hz frame rate requires an input data rate of about 18 M pixels/s. Assuming the architecture of Fig. 5(a), two interleaved shift registers operating 180° out of phase clocked at 9 MHz would allow a single pixel wide bus. Such a clock frequency can be achieved in both technologies, although in practice a part of the line time must be used for data transfer to the DAC's and a reasonable safety margin must be allowed, and a two-pixel-wide bus would probably be used with the low-temperature technology.

B. Buffers

Integrated scan circuits for AMLCD's require not only a shift register to generate the scan pattern, but also digital buffers to drive the scan lines. Typical output rise and fall times for these buffers are around $1\text{ }\mu\text{s}$, and the load they must drive can be several hundred picofarads as discussed in Section IV. Fig. 7 shows rise and fall times for a simple three-stage CMOS buffer as a function of capacitive load; data are shown for the same circuit fabricated

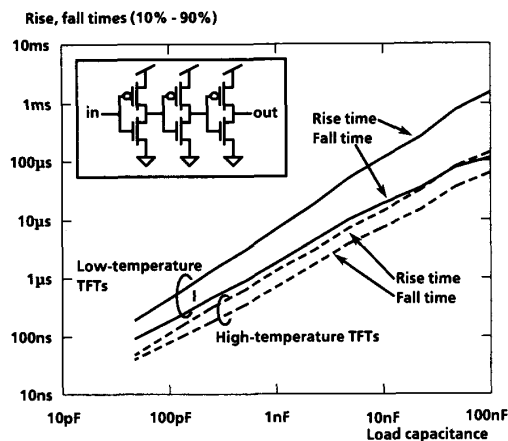


Fig. 7. Polysilicon TFT CMOS buffer rise and fall times. Final stage $W_N = W_P = 1000\text{ }\mu\text{m}$, $L = 5\text{ }\mu\text{m}$.

using both low- and high-temperature technologies. The n- and p-channel output TFT's are the same size, so the fall time is always less than the rise time due to the greater n-channel drive current. This is particularly true in the low-temperature case where the mismatch between n- and p-channel TFT's is greater. As expected, the high-temperature circuits give the fastest switching times, achieving transitions of less than $1\text{ }\mu\text{s}$ even with a load of 1 nF . However, the low-temperature TFT's can achieve the same $1\text{-}\mu\text{s}$ target for loads of several hundred picofarads, easily meeting display requirements.

C. High-Voltage Buffer

In some cases, it may be desirable to have a total gate voltage swing that is greater than either the maximum safe drain voltage for a TFT or the maximum gate-to-channel voltage. This might be the case, for example, if the polysilicon drivers were formed in laser recrystallized material on the periphery of an a-Si TFT active matrix. Fig. 8 shows a circuit that can be used to achieve a 40-V output swing from a 20-V input signal while limiting the voltage experienced by any individual TFT to about 20 V.

When the output is high, $MP1$ and $MP2$ are fully on and the full 40 V is dropped across $MN1$ and $MN2$. The voltage at point A will settle at a value such that the channel currents of both these devices will be equal; there is no possibility of leakage to the substrate via the source or drain junctions as there would be in a single-crystal MOS technology since the TFT's are formed on an insulating substrate. The two TFT's $MN1$ and $MN2$ are identical, and so will satisfy the equal channel current condition if their drain-source and gate-source biases are the same. This condition is satisfied when point A is at $V_{HH}/2$, equally dividing the supply voltage between the two TFT's. A similar argument applies to the p-channel TFT's when the output is low. Fig. 9 shows measured rise and fall times for this circuit fabricated in the high-temperature technology, including a level shifter and driven by a

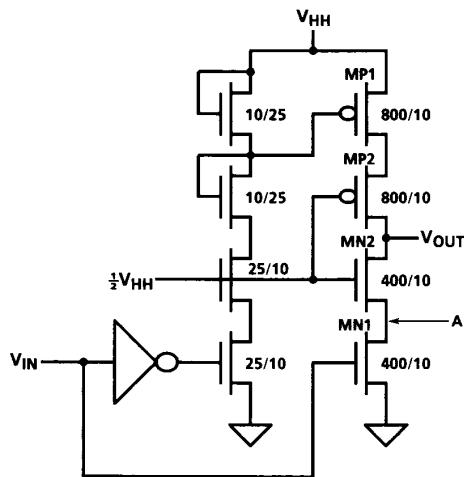
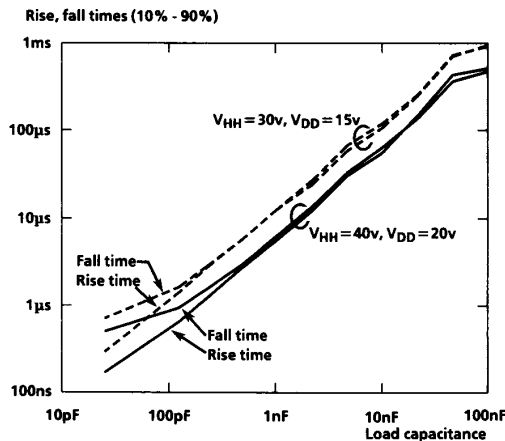


Fig. 8. High-voltage polysilicon TFT CMOS buffer.

Fig. 9. High-voltage polysilicon TFT CMOS buffer rise and fall times. Final stage $W_N = 400 \mu\text{m}$, $W_P = 800 \mu\text{m}$, $L = 10 \mu\text{m}$.

CMOS NAND gate, and again adequate performance is achieved even for loads of greater than 100 pF.

VI. ANALOG CIRCUITS

The circuits described above, and other polysilicon TFT circuits reported elsewhere, are essentially digital. However, the large-area devices where they may be used generally require analog signals in order to reproduce or scan grey-scale or full-color images. Thus there is a need for some analog functionality on the large-area substrates, and in this section the performance of some simple analog circuit elements fabricated with polysilicon TFT's is examined.

A. Pass Gates

The simplest analog circuit element commonly used is a straightforward pass gate. Several data driver architectures have been reported where pass gates are used to de-

liver an externally generated analog signal, such as a corrected video signal [4], [6] or a nonlinear ramp [5], to the display data lines under the control of integrated polysilicon TFT digital circuitry. These schemes require relatively rapid charging of the data line in order to track the external analog voltage accurately.

Fig. 10 shows CMOS pass gate rise and fall times, again as a function of capacitive load, where in this case the transition times are defined for a 10-V swing and settling to within 50 mV of the input voltage. Settling to this accuracy is adequate for a display with at least 32 levels of grey. Again, the higher drive currents of the high-temperature TFT's are reflected in faster settling times, but even with low-temperature devices settling times of less than 3 μs can be achieved with a load of 100 pF.

B. Operational Amplifiers

The range of data driver architectures that can be implemented using simple pass gates as the only analog element is clearly severely limited. Furthermore, in other areas of application, such as optical scanning, signal amplification is often required. Thus, there is a need to implement true analog circuits using TFT's, and the basic building block for those circuits is an operational amplifier. However, in designing operational amplifiers with useful voltage gain and bandwidth, the problems of poor saturation characteristics and low drive current in polysilicon TFT's discussed in Section III must be overcome.

Fig. 11 shows three simple operational amplifiers used in this work that have been designed to achieve this goal. As with the digital circuits discussed in Section V, the circuits have been built using design rules appropriate for large-area substrates. The simple CMOS amplifier (type I in Fig. 11) uses cascodes to overcome the low output impedance of the TFT's in saturation. This circuit used the minimum number of TFT's, and is important since in most applications the area available for the circuits will be limited. The type II circuit provides a differential input and retains the cascode. The type III circuit uses two stages for increased gain and a complementary source-follower output stage for increased drive; it does, however, require compensation to ensure stability.

Fig. 12 shows the frequency response of each amplifier when driving a 30-pF load capacitance. In this case, all the circuits have been fabricated using the high-temperature TFT technology. The single-stage circuits have low-frequency gains of just over 40 dB, and single-pole rolloff characteristics with unity-gain frequencies of about 300 kHz. The two-stage circuit, on the other hand, has a much larger low-frequency gain, approaching 80 dB (the rolloff at low frequency is a measurement artifact related to the relatively high noise level of polysilicon TFT's) and a unity-gain frequency of several megahertz.

C. Switched-Capacitor Amplifier

Fig. 13 shows the schematic of a simple switched-capacitor amplifier with a nominal gain of 10 fabricated us-

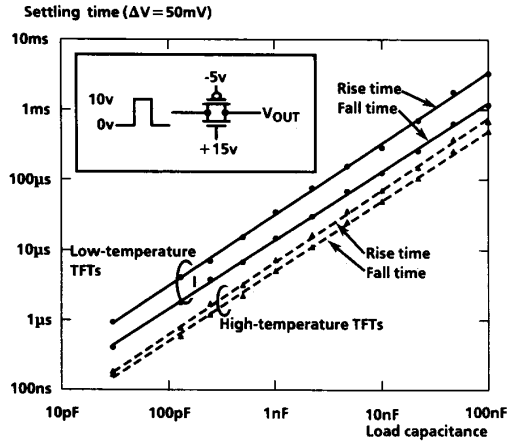


Fig. 10. Polysilicon TFT CMOS pass gate rise and fall times. $W_N = W_P = 600 \mu\text{m}$, $L = 10 \mu\text{m}$.

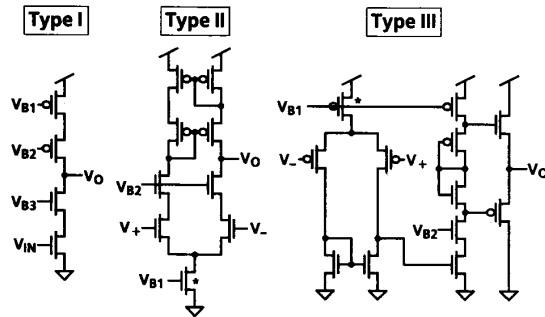


Fig. 11. Polysilicon TFT operational amplifiers. All TFT's have $W = 200 \mu\text{m}$ and $L = 10 \mu\text{m}$ except those marked *, which have $W = 400 \mu\text{m}$ and $L = 10 \mu\text{m}$.

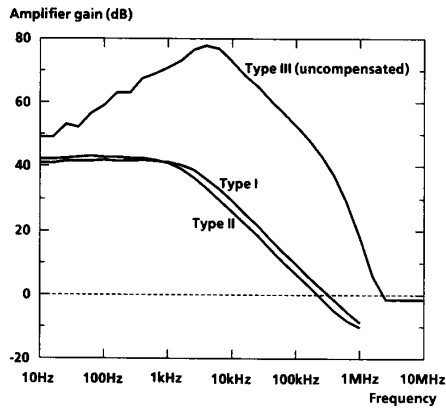


Fig. 12. Polysilicon TFT operational-amplifier frequency response. The load is 30 pF in parallel with 10 MΩ.

ing the thin-film polysilicon technology. The circuit provides input offset and low-frequency noise cancellation. In the reset mode (ϕ high, $n\phi$ low), the integration capacitor C_2 is discharged, and the right-hand plate of C_1 is held at the input offset voltage while its left-hand plate is charged to V_{IN} . In the amplification mode (ϕ low, $n\phi$

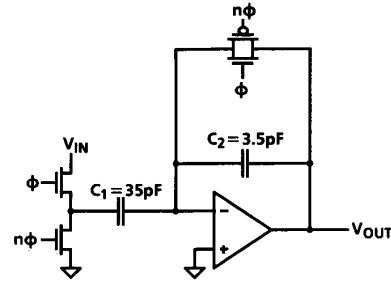


Fig. 13. Polysilicon TFT switched-capacitor amplifier.

high), the switch across C_2 is opened. The left-hand plate of C_1 is switched to ground, injecting a charge of $C_1 \cdot V_{IN}$ to the input of the integrator formed by C_2 and the operational amplifier. An output voltage swing of

$$V_{OUT} = \frac{C_1}{C_2} \cdot V_{IN}$$

is thus obtained (assuming the operational amplifier has very high gain).

Fig. 14 shows transfer curves for this circuit implemented with the type I amplifier shown in Fig. 11 for two bias currents, and in both cases good linearity is obtained for an output swing of about 12 V (the figure also shows the output voltage limits for a deviation from linearity of less than 100 mV). Fig. 15 shows settling times for the switched-capacitor circuit implemented with type I and type II op amps as a function of capacitive load. The total output swing is 10 V in this case, and the settling time is defined as the period required for the output to settle within 50 mV of its final value. The TFT aspect ratios chosen for this comparison are such that the two amplifier designs take up about the same area on the glass. The type III amplifier with the complementary source-follower output stage achieves faster settling at high capacitive loads despite the use of smaller TFT's, but as the load is reduced to about 100 pF, internal settling times dominate and the difference in settling times between the two designs is reduced. In both circuits, increasing the bias current improves settling time as expected, although it should be noted that even the relatively modest bias current of 200 μA corresponds to a significant power dissipation when multiplied by several thousand individual data-line drivers.

As before, it is useful to compare the performance illustrated in Figs. 14 and 15 with the AMLCD driving requirements discussed in Section IV. The amplifier output voltage swing of 10–12 V shown in Fig. 13 is sufficient to cover both data drive polarities. The output voltage error of 50 mV used to define the settling time in Fig. 15 corresponds to at least 32 levels of grey, but the settling time targets depend on the number of display lines. The type I amplifier with a low bias current is adequate for a conventional 480-line display, but for a high-resolution 1024-line display either higher bias currents or the type III circuit will be necessary.

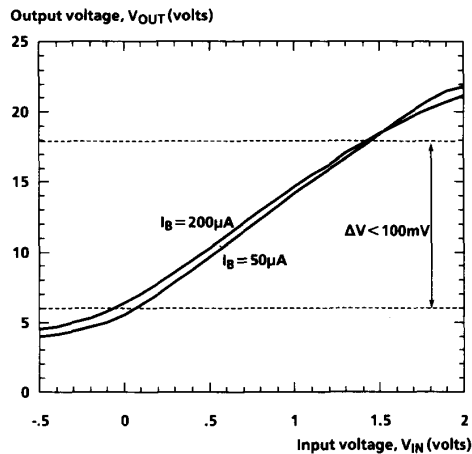


Fig. 14. Polysilicon TFT SC amplifier transfer curves. Type I op amp, settling time = $12 \mu s$, $C_{LOAD} = 30 pF$.

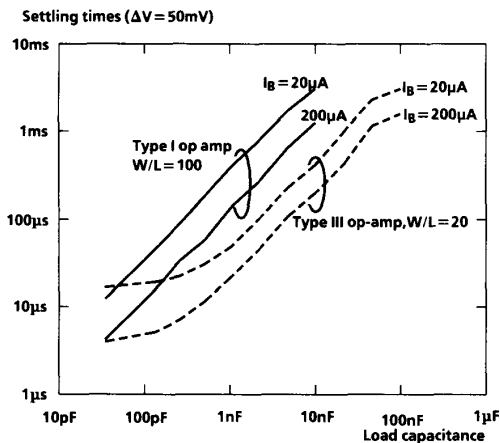


Fig. 15. Polysilicon TFT SC amplifier settling times. Nominal gain = 10, $L = 10 \mu m$, output swing = 10 V, settling defined at $\Delta V = 50 mV$.

D. Charge-Redistribution DAC

An array of switched-capacitor amplifiers such as those described above might be used to sample and amplify an externally supplied analog video signal and drive the data lines of an AMLCD. Generally, however, a digital interface is preferable in terms of bandwidth and noise immunity. The shift registers described in Section V-A have sufficient speed to allow a digital input bus that is only a few pixels wide, even for a high-resolution display, but to use such an interface requires integrated digital-to-analog converters built on the glass using polysilicon TFT's.

Fig. 16 illustrates a straightforward 4-b charge-redistribution DAC that has been implemented using polysilicon TFT technology. The digital control circuits are used to switch the left-hand plate of the input capacitors between a reference voltage and ground under the control of the input data bits. The input capacitors are binary weighted in the usual manner [20], and the overall gain of the circuit can be set by the feedback capacitor C_{FB} .

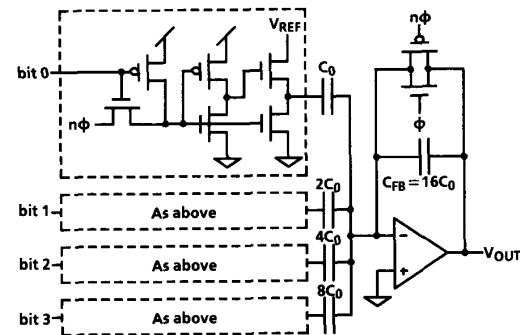


Fig. 16. Polysilicon TFT charge-redistribution DAC.

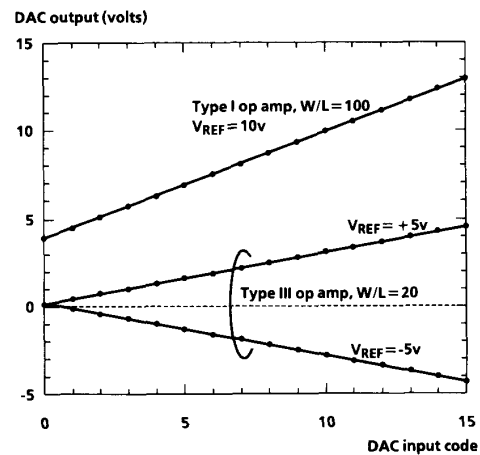


Fig. 17. Polysilicon TFT DAC response. Settling time = $14 \mu s$, $C_{LOAD} = 30 pF$.

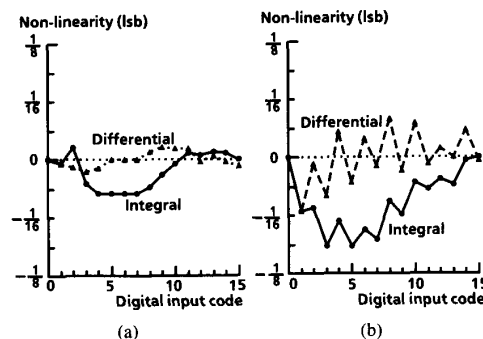


Fig. 18. Polysilicon TFT DAC error. Settling time = $14 \mu s$, $C_{LOAD} = 30 pF$. (a) Type I amplifier, $V_{REF} = 10 V$. (b) Type III amplifier, $V_{REF} = 5 V$.

Fig. 17 shows the response of two such DAC's implemented with the type I and type III op amps. In making these measurements, a settling time of $12 \mu s$ has been allowed, corresponding to the line time of a high-resolution display. In both cases, an output swing of about 10 V is achieved, determined here by the choice of reference voltage, and with the type III operational amplifier, true bipolar operation is obtained.

Finally, Fig. 18 shows the integral and differential nonlinearity of both DAC's. In the case of the type I operational amplifier (Fig. 18(a)), both nonlinearities are better than 1/16th LSB, indicating adequate linearity for an 8-b precision DAC. The nonlinearity with the type III amplifier is a little worse, but still close to being adequate for 8-b operation. Linear DAC's with 8-b resolution are adequate for a 32 or 64 grey level display when corrections for the nonlinear transfer characteristics of the liquid-crystal cell are taken into account. Thus, the polysilicon TFT DAC's show adequate output swing, settling time and precision for driving AMLCD data lines with at least 32 levels of grey.

VII. CONCLUSIONS

This paper describes the performance of a range of digital and analog circuit elements built using polysilicon thin-film devices, including several switched-capacitor circuits that are believed to be the first examples of such devices to be reported. Polysilicon TFT's can be built on large-area (30 cm × 30 cm or larger) glass or quartz substrates, and this allows them to be used in a range of large-area devices such as active-matrix liquid-crystal displays (AMLCD's), page-width optical scanners, or page-width printers. In this paper, the requirements for integrated AMLCD driver circuits have been used as an example to compare with the measured polysilicon TFT circuit performance, and it has been shown that the TFT circuits can achieve the necessary voltage swing, precision and speed for even large high-resolution displays.

The performance of polysilicon TFT's is poor in comparison to conventional single-crystal MOSFET's at present, and in order to remain compatible with large-area processing, relatively coarse design rules have been used in laying out the circuits discussed in this paper. However, despite these limitations, digital circuit speeds of up to 30 MHz have been obtained, along with, for example, 8-b linearity in a charge redistribution DAC with settling times of about 10 μ s. These levels of performance will allow increased functionality on large-area substrates. In the future, as polysilicon TFT performance improves and approaches that of single-crystal SOI, it will become possible to integrate more and more functions on large-area substrates along with displays or input scanners, for example, offering a new range of system design possibilities.

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