

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MIANYANG BOE OPTOELECTRONICS TECHNOLOGY CO., LTD.; WUHAN
CHINA STAR OPTOELECTRONICS SEMICONDUCTOR DISPLAY
TECHNOLOGY CO., LTD.; TIANMA MICROELECTRONICS CO. LTD.; AND
VISIONOX TECHNOLOGY, INC.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Case No. IPR2023-00941
U.S. Patent No. 7,414,599

SUPPLEMENTAL DECLARATION OF DANIEL FOTY, PH.D.

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I. INTRODUCTION

1. I have been retained by counsel for Mianyang BOE Optoelectronics Technology Group Co., Ltd. (“BOE”) et al. (“Petitioner”) in the above-captioned matter as an independent consultant to offer opinions regarding the patentability of the claims in U.S. Patent No. 7,414,599 (“the ‘599 patent”).

2. In my Original Declaration (EX1003), I analyzed and provided examples of how Kimura, combined with the knowledge of a POSITA, rendered obvious the Challenged Claims (*i.e.*, claims 1-18) of the ‘599 patent. I hereby incorporate the entirety of my analysis from my Original Declaration.

3. I have now reviewed Patent Owner’s Response (POR, Paper 33), expert declaration (EX2008), and accompanying exhibits. I have found them to be riddled with errors, misstatements, and misunderstandings of the underlying technology – along with numerous other flaws and misquotations.¹ I will herein respond to the POR and Dr. Wolfe’s declaration as appropriate.

4. The combination of my Original Declaration and this Supplemental

¹ I note that Patent Owner made numerous references to my deposition testimony – mostly unquoted attributions. I have reviewed these instances – and in nearly every instance Patent Owner referenced my testimony improperly by taking the testimony grossly out of context, omitting the key parts of a particular answer, attributing an answer to a question that was not the one actually asked, or simply quoting incorrectly. I do not concede any of the misattributions.

Declaration represents only those opinions that I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein – based on any new information and on my continuing analysis of the materials provided.

II. OVERVIEW OF CONCLUSIONS

5. First, it is my conclusion and opinion that there is not a genuine dispute between the parties over the qualifications of a POSITA. To the extent different qualifications have been proposed, I qualify as a POSITA under each qualification.

6. Second, it is my conclusion and opinion that all-pMOS versions of Kimura's pixel circuits in Figs. 33/36 would have been obvious to a POSITA.

7. Third, it is my conclusion and opinion that Kimura Fig. 36 renders obvious a shared light emitting signal – and that Patent Owner and Dr. Wolfe misunderstood and/or misrepresented my conclusions and opinions with respect to my Original Declaration.

8. Fourth, it is my conclusion and opinion that Kimura renders obvious a reset/initialization transistor.

9. Finally, it is my conclusion and opinion that Patent Owner's purported objective indicia of nonobviousness lack the required nexus to the Challenged Claims of the '599 patent – and, further, lack merit to show any Challenged Claim as being nonobvious. Regardless, it is my conclusion and opinion that Patent Owner's purported objective indicia of nonobviousness cannot overcome Kimura's

strong showing of obviousness.

III. MATERIALS CONSIDERED

10. In preparing this Supplemental Declaration, I reviewed and considered Patent Owner's Response, its accompanying exhibits, and the following materials in addition to those listed in my Original Declaration, along with any other materials referenced in the body herein.

EX1018	Declaration of Thomas L. Credelle
EX1019	Reserved
EX1020	Reserved
EX1021	Reserved
EX1022	<i>Certain Active Matrix Organic Light-Emitting Diode Display Panels & Modules for Mobile Devices</i> , ITC Inv. No. 337-TA-1351, Staff's Prehearing Brief (Public Version) (Excerpt) (Jan. 12, 2024)
EX1023	LinkedIn Profile of Dr. Andrew Wolfe
EX1024	Profile of Dr. Andrew Wolfe on Santa Clara University website
EX1025	Curriculum Vitae of Dr. Andrew Wolfe on Santa Clara University website
EX1026	<i>CMOS Circuits for Peripheral Circuit Integrated Poly-Si TFT LCD Fabricated at Low Temperature Below 600C</i> , Masaru Takabatake et al., IEEE Transactions on Electron Devices, Vol. 38, No. 6, pp. 1303-1309, June 1991
EX1027	<i>Polysilicon TFT Circuit Design and Performance</i> , Alan G. Lewis et al., IEEE Journal of Solid-State Circuits, Vol. 27, No. 12, pp. 1833-1842, December 1992
EX1028	Deposition Transcript of Dr. Andrew Wolfe (May 17, 2024)

EX1029	Supplemental Expert Declaration of Dr. Daniel Foty
EX1030	Google patent search results
EX1031	<i>Current Copier Cells</i> , S.J. Daubert et al., Electronics Letters, Vol. 24, No. 25, December 8, 1988
EX1032	<i>Characteristics of Field-Induced-Drain (FID) Poly-Si TFTs with High On/Off Current Ratio</i> , K. Tanaka et al., IEEE Transactions on Electron Devices, Vol. 39, No. 4, pp. 916 – 920, April 1992
EX1033	<i>A Self-Aligned Offset Polysilicon Thin-Film Transistor Using Photoresist Reflow</i> , J. Han and C. Han, IEEE Electron Device Letters, Vol. 20, No. 9, pp. 476 – 477, September 1999

IV. LEVEL OF SKILL IN THE ART

11. In my Original Declaration, I proposed a qualification for a POSITA based on the '599 patent. EX1003, ¶31. The '599 patent describes a pixel circuit based on field effect transistors (FETs) that drives a light emitting element (with a drive transistor operating as an analog component and the other transistors operating as digital switches). A POSITA should be familiar with the functionalities of FETs, the design and analysis of analog and digital circuits comprised of FETs, and the operational behavior of light emitting devices (such as LEDs) in the context of pixel circuits of a display. Accordingly, I proposed a qualification of “a Bachelor’s degree in electrical engineering or a similar discipline, along with 2-3 years of circuit design/analysis experience. A Master’s or Ph.D. degree in a relevant field may substitute for some work experience and vice versa.” *Id.*

12. I note that Thomas Credelle submitted a declaration (EX1018) in which

he opined on the level of skill in the art, and agreed with the definition I had provided. EX1018, ¶25. Mr. Credelle has decades of experience in active-matrix display and pixel circuit design and electroluminescence, and there is no dispute that he qualifies as a POSITA. *Id.*, ¶¶4-20, 36-37; EX1028, 47:8-11.

13. Patent Owner's expert, Dr. Wolfe, also appears to agree with my proposed qualification. First, he agrees with the degree requirement. EX2008, ¶46; EX1028, 71:12-19. Further, he agrees that an additional, higher degree may substitute for work experience. EX1028, 69:22-70:2, 72:1-3. In addition, he agrees that two to three years of circuit design and/or analysis experience is appropriate. *Id.*, 71:20-72:1.² The field of the applicable circuit experience in his definition (active-matrix display design and electroluminescence) does not meaningfully differ from the context of my proposed qualification. Dr. Wolfe does not dispute my qualification as a POSITA. *Id.*, 47:5-7.

14. I note that there are numerous POSITA topics on which Dr. Wolfe agrees with me. For example, Dr. Wolfe stated that a POSITA would understand the operation of the driving transistor, threshold-voltage compensation and its relationship to image quality, the impact of shared signal lines on aperture ratio, and the initialization, e.g., discharging a capacitor, of a pixel circuit. EX2008, ¶48;

² Patent Owner and Dr. Wolfe's original proposal omits "circuit design and/or analysis" from the work-experience requirement. POR at 7; EX2008, ¶46.

EX1028, 74:18-76:21. I agree that a POSITA would know all of these things.

15. To the extent that Patent Owner insists that some unspecified amount or type of “experience in active matrix display design and electroluminescence” beyond my proposed definition (when understood in its proper context) is required, I disagree with this assertion. The Challenged Claims do not require a display (active-matrix or otherwise); rather, these Claims focus on pixel circuits comprising transistors, capacitor(s), and an LED. *See* EX1028, 83:11-16, 85:6-18 (where Dr. Wolfe offers no opinions as to whether or not the preambles are limiting). The electroluminescent element in the Challenged Claims performs a well-understood, routine function of such an element – namely, emitting light when a current flows through it. Thus, any specific experience beyond my proposed qualifications, understood in its proper context, is unnecessary. To the extent Patent Owner proposes that more specific expertise (beyond my proposal) is required, I note that Mr. Credelle disagrees with such a definition. EX1018, ¶¶31-35.

16. Finally, I note that computer architecture, video research, and multimedia are fields addressing technical issues significantly different from those in pixel circuits, active-matrix display designs, and electroluminescence. For example, video processing such as compression/decompression deals with video data as information and is agnostic to the actual display or electroluminescence used to display video.

17. I note that even under Samsung’s incorrect definition of a POSITA, I possessed electroluminescence experience via fabricating and characterizing semiconductor-based optical emitters (such as LEDs and lasers). Thus, I was very familiar in 2003 with the semiconductor devices that were used in contemporary displays (which basically comprise transistors and LEDs), and how those semiconductor components are organized into circuits that were (and are) used in displays. Further, the types of circuits used in light-emitting display panels (such as shift registers) are circuits used in a wide variety of analog and digital circuit applications.

V. KIMURA RENDERS ALL CHALLENGED CLAIMS OBVIOUS

A. An All-PMOS Pixel Circuit Was Obvious

18. Patent Owner alleges that an all-pMOS pixel circuit would not have been obvious because of concerns over carrier mobility, transistor leakage, and transistor size. I disagree, and note that Patent Owner’s own exhibits contradict Patent Owner’s assertions.

19. *First*, the ’599 patent only discloses an all-pMOS embodiment. EX1001, Figs. 3-7. But it also discloses that its pixel circuit “can be configured of

a NMOS transistor, a CMOS transistor [sic]³ or the like other than the PMOS transistor.” *Id.*, 8:36-38. This passing sentence is indicative that a POSITA would have known that either or both pMOS and nMOS transistors were suitable for pixel circuits, and that no further disclosure was necessary to teach a POSITA to make such modifications – or to show that the inventors possessed knowledge beyond that of a POSITA to make their all-pMOS (or, alternatively, all-nMOS or mixed pMOS/nMOS) pixel circuit work. Moreover, if pMOS transistors truly had the mobility, leakage, and size concerns as Patent Owner alleges (they did not), the silence of the ’599 patent on how to deal with such concerns again indicates that resolving such concerns was within a POSITA’s knowledge and skill.

20. Relatedly, the admitted prior art comprises pMOS transistors, including transistors coupled to the capacitor (and thus performing a similar function as the third transistor, e.g., T33 of the ’599 patent or TFT 3309 of Kimura), which Patent Owner alleges to be especially sensitive to leakage concerns. EX1001, Fig. 1, 2:17-32 (admitted prior art); POR, 14 (Patent Owner’s leakage allegation). Yet the ’599 patent does not identify any concern over carrier mobility, transistor leakage, or

³ There is actually no such thing as a “CMOS transistor” – thus, it is reasonable to interpret this term as indicating a circuit that has the presence of both nMOS transistors and pMOS transistors. Dr. Wolfe admitted that the ’599 patent did not invent a new type of transistor. EX1028, 91:17-19.

transistor size in this admitted prior art. *See id.*, 2:33-3:40. Instead, the '599 patent only identifies the problem remedied using threshold-voltage compensation. *Id.*, 3:19-40.

21. ***Second***, Kimura itself repeatedly discloses that transistors that function as simple switches may be – by virtue of that digital functionality – either pMOS or nMOS. EX1002, [0396], [0434], [0438], [0445], and [0649]. It discloses an all-pMOS pixel circuit (Fig. 22), all-nMOS pixel circuits (Figs. 20/21, 32, 38-40), and mixed pMOS/nMOS pixel circuits (e.g., Figs. 33 and 36). These circuits again demonstrate that either pMOS or nMOS was suitable for pixel circuits. They also demonstrate that single-species (all-pMOS or all-nMOS) pixel circuits are compatible with Kimura's CMOS manufacturing process.⁴

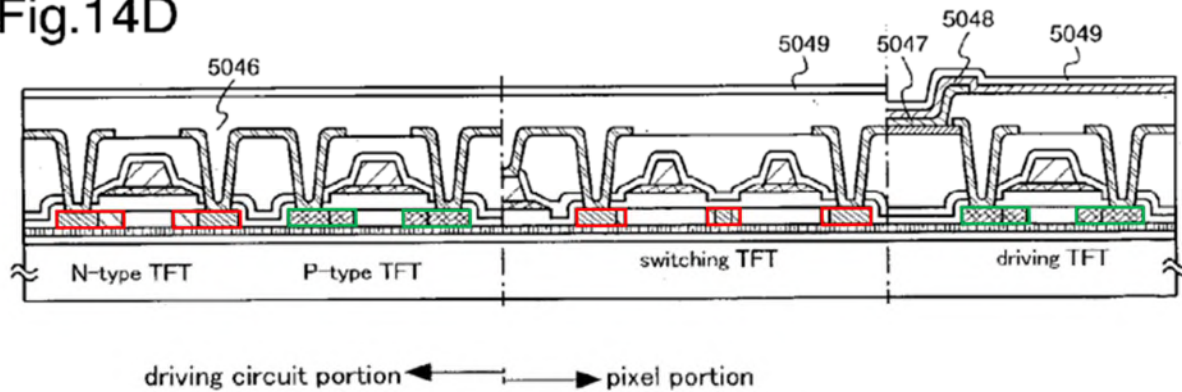
22. Regarding manufacturing processes, Kimura identifies the ability to integrate both nMOS and pMOS TFTs on the same substrate (with the peripheral circuitry and the pixel circuitry being on the same substrate). Kimura teaches that this CMOS manufacturing process is applicable to both the peripheral circuitry and the pixel circuitry. Kimura specifically identifies his peripheral driver circuit

⁴ A “CMOS manufacturing process” means that both nMOS transistors and pMOS transistors can be fabricated together in that process, while a “CMOS circuit” refers to the use of both nMOS transistors and pMOS transistors in a circuit that is configured in a particular (“CMOS”) architectural form. EX2050, 95:15-96:6.

instances as “CMOS circuit composed of the N-channel TFT and the P-channel TFT.” EX1002, [0547], [0582]; *see also id.*, [0502] (similar). But instead of identifying the pixel circuit as CMOS, Kimura instead refers to it as having switching TFTs and a drive TFT. *Id.*, [0502], [0547], [0582]. Kimura’s architecture would have made intrinsic sense to a POSITA – as the driving circuitry performs digital-logic functions to drive the pixel circuitry, and CMOS circuitry is excellent for digital-logic circuitry. Dr. Wolfe evidently agrees that Kimura only discloses its driving circuit – not pixel circuit – to be CMOS. *See* EX2008, ¶53 (“In Embodiments 4 and 5, shown in Figures 13-15, Kimura teaches optimized methods of manufacturing *a CMOS driving circuit alongside its pixel circuits.*”) (emphasis added). A POSITA would have understood that Kimura’s CMOS manufacturing process would not require a pixel circuit comprising both pMOS and nMOS transistors.

23. This conclusion is supported by the figures Kimura uses to illustrate its CMOS manufacturing process. Figure 14D shows both nMOS and pMOS TFTs in the driving circuit as well as in the pixel circuit, as indicated by the cross-hatching pattern (unidirectional for nMOS (red below) and bidirectional for pMOS (green)). *See* EX1028, 157:13-17 (Dr. Wolfe relying on cross-hatching pattern to determine transistor polarity).

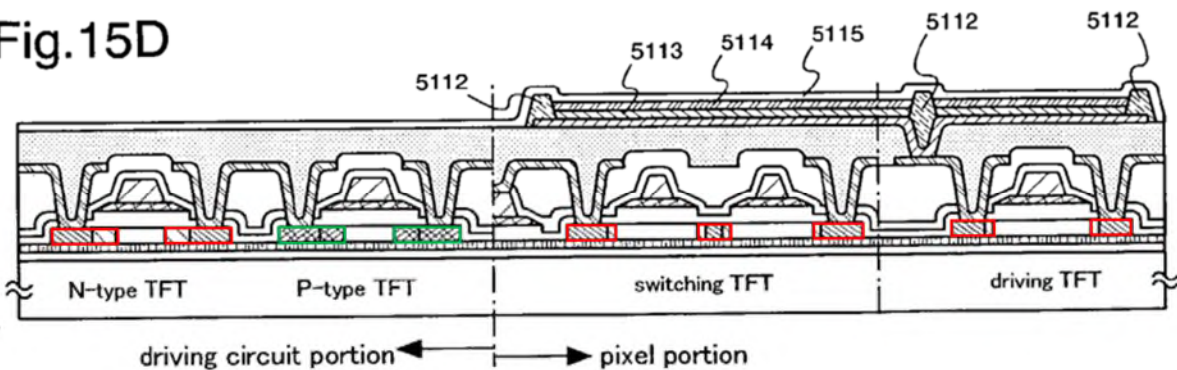
Fig.14D



EX1002, Fig. 14D (annotated); *see also id.*, [0320], [0501]-[0571] (embodiment 4 disclosing CMOS manufacturing-processing steps resulting in Figures 14A-14D).

24. Figure 15D, which similarly shows a device after CMOS manufacturing-processing steps, however, shows a single-species pixel circuit alongside a CMOS driving circuit.

Fig.15D



Id., Fig. 15D (annotated); *see also id.*, [0321], [0572]-[0615] (embodiment 5 disclosing CMOS manufacturing-processing steps resulting in a device illustrated in Figures 15A-15D).

25. Although Figures 14 and 15 only show cross-sections of a portion of

the circuit, it is significant that Kimura shows a mixed pMOS/nMOS pixel circuit in Figure 14D, yet deliberately alters it to a single-species pixel circuit in Figure 15D. Together with Kimura's single-species pixel circuit diagrams (e.g., Figs. 20-22, 38-40), these figures show that Kimura's CMOS manufacturing process is compatible with a single-species pixel circuit. Patent Owner refers to these figures and embodiments to argue Kimura's supposed CMOS restriction relative to the Board's second theory. POR at 21-24 (citing EX1002, ¶¶[0502]-[0615]). But Kimura's disclosure actually contradicts Patent Owner's argument.

26. Further, consistent with Kimura, other prior art shows manufacturing benefits from building an all-pMOS pixel circuit with the surrounding control circuitry on the same substrate using a CMOS manufacturing process. For example, Kimura '798 discloses that "a transistor circuit 100 [in Fig. 1] may consist of a driving TFT 110 (P channel type), a compensating TFT 120 (P channel type), a resetting TFT 130 (N channel type) and a switching TFT 140 (N channel type)." EX1004, 8:3-6; *see also* EX1003, ¶151 (discussing Kimura '798). Kimura '798 further teaches that "the example shown in FIG. 1 is constructed with the mixture of a P channel type TFT and an N channel type TFT," which indicates to a POSITA that a CMOS manufacturing process is being considered. EX1004, 12:30-49. Kimura '798 goes on to explain that "all TFTs can be P channel type TFTs" and "it is often advantageous in manufacturing when all TFTs are of the same type." *Id.*

27. **Third**, Patent Owner’s own exhibits show all-pMOS pixel circuits. Indeed, Dr. Wolfe relied on all-pMOS pixel circuits to argue that others had failed (where the Patent Owner allegedly succeeded). *See* EX2008, ¶¶114, 117, 119. These exhibits show that POSITAs had no concerns over using pMOS transistors in pixel circuits, or at least knew how to resolve such concerns.

28. Further, I note Patent Owner’s misquotations of my testimony in this aspect. I testified that “a CMOS circuit has a particular architecture.” EX2050, 95:15-96:6. I gave an example of a CMOS inverter. *Id.*, 94:21-95:18. As a POSITA would have known, a CMOS inverter comprises a pMOS transistor and an nMOS transistor working in conjunction to perform a logical inversion function. Thus, the pMOS transistor would have had a larger dimension (at a time when pMOS was slower than nMOS) so that the two would have the same speed and would produce a symmetric logic output function. *Id.* Pixel circuits (such as Kimura’s) are not properly called CMOS because they do not have that particular CMOS architecture. They are simply mixed pMOS/nMOS circuits. Thus, my testimony regarding the benefits of CMOS does not apply to the pixel circuits of Kimura – and actually contradicts – Patent Owner’s (mischaracterizing) assertion. *See* POR at 3.

29. Patent Owner’s attempt to say that Kimura’s teachings *require* both nMOS and pMOS transistors in his disclosed pixel circuitry (for them to be “CMOS” (sic)) is thus simply incorrect.

30. In addition, it should be noted that Patent Owner also offers a rather spurious argument (POR, 18-19) to the effect that someone considering changing Kimura's circuitry by replacing nMOS transistors with pMOS transistors would face so many permutations that they would be too befuddled to do anything. This is a rather silly argument as a POSITA would not need to evaluate (or even consider) every possible permutation. For example, a POSITA wanting to use a single-species pixel circuit (e.g., due to either having only a single-species manufacturing process available or to take advantage of more-consistent inter-transistor behavior achieved by single-species circuits) would not look at Kimura's mixed-species pixel circuits and abandon Kimura as unworkable for his/her situation; rather, such a POSITA would be motivated to convert Kimura's pixel circuits to single-species.

31. Finally, Dr. Wolfe asserts that Petitioner's reasoning "fail[s] to take into account the significant structural and operational differences that a POSITA would have understood exist between NMOS and PMOS transistors." EX2008, ¶61. However, this statement is conclusory and unsupported. To the extent Dr. Wolfe is referring to his arguments about mobility, transistor size, and leakage, those arguments are baseless – as I explain in detail below. Similarly, to the extent Dr. Wolfe suggests that inverting the control signals from active high-high (for nMOS TFTs) to active-low (for pMOS TFTs) would be a "significant" challenge for a POSITA, such an assertion is completely baseless; any junior engineer should be

capable of making such a minor change. EX1003, ¶57.

32. The evidence above clearly shows that Patent Owner's alleged concerns over pMOS were nonexistent at the time of the '599 patent. This should be sufficient for a finding against the Patent Owner on the pMOS versus nMOS issue; nonetheless, I will specifically address the alleged concerns.

1. nMOS/pMOS Mobility Was Not a Factor in Pixel Circuit Transistors

33. The dominant consideration for the operating speed of a display is the ability of human eyes to perceive changes in an image. Dr. Wolfe testified that "a typical person would not be able to perceive the difference between 120 Hertz display and a faster one." EX1028, 102:11-13. Accordingly, even today's displays typically do not have a refresh rate of more than a 120 Hz. Dr. Wolfe further testified that displays in 2003 were in the range of 15 to 60 Hz. *Id.*, 99:8-17; 101:13-21. Thus, a pixel circuit need not operate at a speed higher than that.⁵ Indeed, Dr. Wolfe

⁵ As a pixel circuit is refreshed only at the rate of the display refresh rate (e.g., 60 Hz, 120 Hz, etc.), the transistors used in the pixel circuit do not need to operate at speeds faster (or at least *much* faster) than the speeds achievable by the pixel circuit transistors – and pixel circuits are the only topic of the '599 patent (and the discussion here). However, for completeness, it should be noted that the peripheral circuitry will have to be fast enough to also refresh each pixel row of the display – so that, for example, for a display with 1024 rows and a refresh rate of 120 Hz, the

acknowledged why a POSITA would not want to increase the operating speed of a display – higher speed consumes more power, an important product-design factor especially for battery-operated devices (as a higher-than-necessary refresh rate will consume more power with no detectable improvement to the quality of the image(s) on the display). *See id.*, 102:6-18.

34. Patent Owner asserts that a POSITA would not have considered changing an nMOS transistor to a pMOS transistor in a pixel circuit (such as those disclosed by Kimura) – because, allegedly, an nMOS transistor is inherently faster than is a pMOS transistor, since nMOS transistors have a higher carrier mobility than pMOS transistor. Patent Owner’s argument is a red herring on many levels.

35. First, Patent Owner asserts an n:p mobility ratio of 2:1; however, this ratio is taken from (one period in time of) *mainstream silicon MOSFET technology*⁶ – and Patent Owner has cited no references regarding mobility or mobility-ratios in *TFTs*. Second, as “mobility” is a proxy for “switching speed” in transistors, Patent

peripheral circuits would have to be capable of operating at speeds of about 123 kHz or greater. However, as will be shown below, reported TFT speeds were, even a decade prior to 2003, much faster than even this requirement. *See infra* ¶¶36-37. Thus, by 2003, TFTs were already much faster than necessary for use in displays.

⁶ As I explained in my Deposition testimony, this “2:1” ratio in mainstream silicon MOSFETs only applied for a period of time – with the ratio being 3:1 in earlier times, and has become 1:1 in contemporary technology. EX2050, 92:20-93:7.

Owner has cited no references regarding the switching speeds of TFTs with respect to the speeds required (as discussed above) for displays – where, as noted above, a refresh rate of 60 Hz is sufficient in 2003 for acceptable display quality (with higher speeds consuming more power for no detectable (by the human eye) improvement in image quality); thus, Patent Owner has not shown why this “issue” is a problem.

36. In fact, both nMOS and pMOS polysilicon TFT transistors typically operated at *megahertz* speeds many years before the time of the ’599 patent. For example, Takabatake 1991 reported that “(t)he maximum operation frequency of the CMOS shift register was 1.25 MHz.” EX1026, 1. In addition, Lewis 1992 reported “(d)igital circuit speeds in excess of 20 MHz.” EX1027, Abstract. In both of these examples, the “speed” is orders of magnitude larger than the refresh speeds necessary for a pixel circuit.⁷

37. Thus, well prior to 2003, both nMOS and pMOS TFTs ran much faster than was necessary for the refresh rate of a display. The speed of pMOS transistors (and hence the mobility of pMOS carriers) was simply not a concern of a pixel-circuit designer. Moreover, as discussed *infra* (§107 n.15), the well-known ability

⁷ The circuits described in these two papers both use true CMOS (i.e., architecture) circuits. However, CMOS circuit speed cannot exceed the speed of the component transistors – and thus, it is appropriate and correct to use the findings of these papers to infer the speed of individual (nMOS or pMOS) polysilicon-based TFTs.

(in silicon MOS transistor technology) to scale down device sizes – providing circuits that are both smaller *and* faster⁸ – is also available to polysilicon TFT technology; this is something discussed in a Samsung paper that will be considered below in Section V (§107). Thus, as is the case in mainstream silicon MOSFET technology, transistor scaling in polysilicon TFTs will make those devices smaller and faster (as time and technology progress) – causing the degree of “extra” (vs. the pixel circuit requirements) speed to become even larger with time (i.e., by 2003–and even today).

38. Furthermore, Patent Owner’s own arguments and exhibits expose that its mobility argument is another manufactured dispute. Preliminarily, Patent Owner uses a 2:1 nMOS-to-pMOS mobility ratio. POR at 13, EX2008, §64.⁹ Patent Owner

⁸ This is the essence of what is popularly known as “Moore’s Law.”

⁹ I testified regarding this 2:1 ratio in the context of mainstream silicon transistors, not polysilicon TFTs used in displays. EX.2050, 92:15-94:7 (framing the “silicon” context for the discussion); *id.*, 94:2-4 (“two to one”). Further, the ratio was only relevant for a particular period of time, rather than being a general physics-based characteristic. *Id.*, 93:20-94:20. Patent Owner misapplied my testimony without any support to (falsely) try to establish an equivalence between silicon MOS transistors and polysilicon TFT transistors in this regard. Mainstream silicon technology uses crystalline silicon – in which electrical conduction occurs throughout the material (similar to the conduction of current in a metal). In contrast,

acknowledges that amorphous silicon was a viable material for pixel circuits. POR at 3; EX2008, ¶34; *see also, e.g.*, EX1028, 78:1-6, 79:17-21, 165:16-21, 166:22-167:4, 172:3-15.¹⁰ This is consistent with Kimura’s disclosure. *See* EX1002, [0506] (“an amorphous semiconductor film ... may be used as the semiconductor film”). Patent Owner’s exhibit further corroborates this understanding. EX2013, 1 (“From the mass production point of view, [amorphous silicon] is almost perfect” for full color OLED display); EX2010, 27 (“[Low-temperature polysilicon] TFT and [amorphous silicon] TFT have been studied widely as suitable choices for an

“polysilicon” is a contraction of “polycrystalline silicon” – and polycrystalline materials are comprised of grains, with conduction occurring along the grain boundaries. *See* EX1028, 77:7-18. Given the fundamentally different internal structure of the materials which largely determines carrier mobility, Patent Owner has failed to provide any evidence that the carrier mobility ratio in silicon (as I testified) is relevant to the carrier mobility in polysilicon TFTs in pixel circuits.

¹⁰ Dr. Wolfe used the term “amorphous silicon” in his declaration in the context of AMOLED displays, yet he testified that “[he was] not familiar with the use of amorphous silicon in displays [in 2003].” *Compare* EX2008, ¶¶33-34 with EX1028, 169:5-9. Similarly, he used the term “polysilicon” in his declaration and cited a paper with that term in the title. EX2008, ¶¶ 34, 63; EX2011 (“Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display”) (title quoted in EX2008, ¶129). Yet he testified “I’m not sure what you mean by just polysilicon.” EX1028, 170:3-7.

AMOLED backplane.”). Accordingly, nMOS transistors (which according to Patent Owner does not have a mobility concern) in amorphous silicon would be suitable for pixel circuits.

39. But the electron mobility in amorphous silicon is roughly 300 times slower than polysilicon, according to Patent Owner’s textbook: “It is apparent that the electron mobility of [low-temperature polysilicon] TFTs is 300x that of [amorphous polysilicon] TFTs.” EX2010, 28.¹¹ Kimura also discloses that amorphous silicon has lower mobility than polysilicon. EX1002, [0357] (disclosing that polysilicon TFTs are “more suitable as transistors used in light emitting devices” because of their “higher field effect mobility” relative to amorphous silicon). If amorphous silicon (whose electron mobility is 300 times slower than polysilicon) was suitable for TFT display, it follows that polysilicon pMOS transistors (whose mobility is 150 time faster than amorphous silicon nMOS transistors under the 2:1 ratio Patent Owner used) are plenty fast for TFT displays.

40. Thus, the “nMOS/pMOS mobility ratio” (whatever it might have been in *TFTs* in 2003) is a red herring – since neither nMOS mobility nor pMOS mobility itself was an issue in 2003, as both nMOS and pMOS TFTs were more-than-sufficiently-fast for use in displays.

¹¹ Dr. Wolfe was completely unaware of this fact. EX1028, 172:3-15.

2. Samsung’s “Size” Argument is Derivative of its Mobility Argument and Fails for the Same Reasons

41. As an extension to its mobility argument, Patent Owner argues that because the allegedly-faster nMOS transistor could be made smaller to achieve the same speed as a larger pMOS transistor, the use of nMOS transistors would allow for smaller pixel circuitry – and thus for a higher aspect ratio, than if pMOS transistors were used. POR, 14-15.

42. Notably, neither Kimura nor the ‘599 patent mention this issue – indicating that it was not a problem in pixel circuits in 2003. Patent Owner’s “evidence” consists of a single conclusory sentence from Dr. Wolfe, who cited my testimony as support. EX2008, ¶165 (cited in POR, 15) (citing EX2050, 92:20-94:18). But this again misquotes my testimony, which was about mainstream silicon MOS transistors (and CMOS logic circuits made from them), not polysilicon TFTs. EX2050, 92:15-94:18. Dr. Wolfe did not quantify, cite any reference, or provide any example of the purported TFT size difference and any marginal impact it might have on aperture ratio.

43. As discussed above, the TFT operating speed was not at all a concern for pixel circuits in 2003. Thus, a POSITA would have understood that transistor sizing (*viz.*, making pMOS transistors smaller) would not have been material to the refresh rate (60 Hz or similar) necessary for adequate image display quality.

3. Leakage Was Not a Significant Factor in TFT Pixel Circuit Transistors

44. Patent Owner also argues that a POSITA would not have changed Kimura's nMOS transistors to pMOS transistors because pMOS transistors have "greater leakage current." POR, 14. In particular, Samsung contends that replacing Kimura's "third transistor" (3309) with a pMOS transistor was nonobvious because it "could alter the stored brightness level" during light emission due to higher PMOS leakage. POR, 14. This is again a manufactured concern on several fronts.

45. First, it should be noted that the '599 patent makes no mention of "leakage" – and neither does Kimura; this alone indicates that "leakage" is simply not a fundamental issue or a problem in polysilicon-based TFTs (at least by the time of Kimura and the '599 patent). In that vein, in the POR, Patent Owner shows nothing which indicates that this is a fundamental problem – and, in addition, Patent Owner simply asserts the term "leakage" without actually defining what is meant by leakage. Anyone of skill in the transistor art knows that transistors can be subject to various types of leakage – with some types being inherent to field-effect transistors, while others are essentially failure mechanisms that render particular transistors unsuitable for use in real product circuitry (at least until the transistor fabrication can be improved and rendered viable).

46. The operation of pixel circuits involves repeated cycles. As explained above, the duration of each cycle corresponds to the refresh rate of the display. And

the initialization period of each cycle is intended specifically to discharge the voltage on the storage capacitor. Thus, the cyclical operation of the pixel circuit renders a small amount of leakage of no concern. Patent Owner argues otherwise – but does so without any consideration of the refresh rate, or any analysis of a leakage rate. Such an argument is speculative at best.

47. Further, if leakage were a concern (it was not), I explained in my testimony that *for properly-functioning transistors* (such as the one depicted in the I-V curve at Paragraph 63 of my Original Declaration) a simple threshold-voltage adjustment (*e.g.*, a manufacturing process tweak) can reduce leakage. *See* EX2050, 96:8-99:1, *especially* 97:10-98:22; EX1003, ¶63.

48. During my deposition testimony,¹² I was asked several questions about “leakage” in transistors. I answered these questions by referring to a graph that appeared in my original Declaration. I explained “leakage” in terms of the leakage that appears (as a result of basic physics) in all properly-functioning field-effect transistors. I also explained that the specific value of the leakage current is *not* a happenstance that cannot be controlled or changed; rather, I explained that it has been a long-known practice in the field-effect-transistor art to adjust this leakage current level (as desired) by adjusting the threshold voltage of the transistor (by

¹² EX2050, 96:8-99:1.

adjusting the manufacturing process) – with the threshold voltage value selected being adjusted until the desired (or acceptable) leakage current value is reached.

49. Patent Owner provides no evidence that “leakage” (of any type) is a general problem in the art of manufacturable TFTs, or that the problem is universal.

50. Rather, Patent Owner’s entire basis for their assertions regarding “leakage” is provided by reference to a single journal paper¹³ which was published in 1997. Patent Owner further treats this paper as being authoritative – not just for polysilicon TFTs at the time it was published, but also for (at least) the time of the ’599 patent. However, examination of this paper shows that it cannot be treated as authoritative – as the “leakage” in this paper is not the conventional type of transistor leakage that I described in my Original Declaration (and in my deposition testimony), but rather is a very high leakage that is indicative of failed transistors that are unacceptable for use in product circuits (of displays or otherwise).

51. The “leakage current” disclosed in this 1997 paper can be readily-found by examining Figure 1 of this paper.

¹³ C. Angelis et al., J. Appl. Phys. vol. 82, pp. 4095-4101 (1997). Note that the authorship of this paper is shared among two universities in Greece, a university in Bulgaria, and a French national lab – and is thus clearly an academic paper rather than a report from a firm that actually manufactured polysilicon TFTs for use in display products.

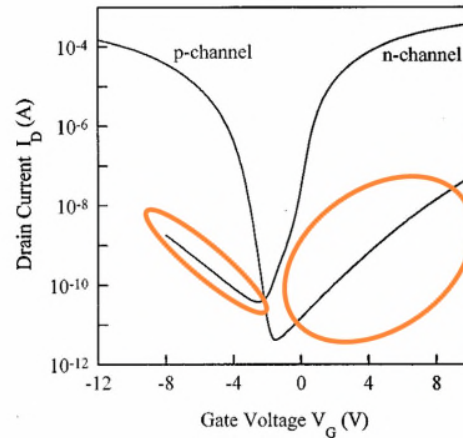


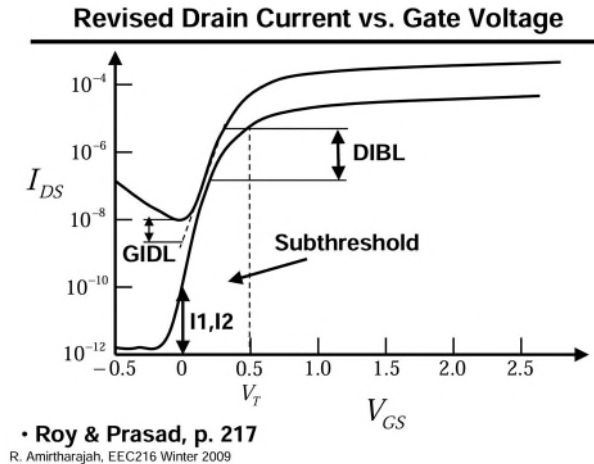
FIG. 1. Typical transfer characteristics of *n*-channel and *p*-channel polysilicon TFTs at drain voltages 5 V and -5 V, respectively. The gate ratio is $W/L = 50/10$.

(Annotations added.) The added annotations identify the “leakage current” that is present in the transistors that were fabricated for the analysis to be presented in this paper. This leakage current occurs when the gate voltage applied to the transistor is pushed to be “more off” than just the voltage necessary to turn the transistor off.

52. The most-notable feature of this leakage behavior is that it represents a failure mechanism – one which renders these transistors unsuitable for use in any real circuitry. The leakage that I described in my Original Declaration and in my deposition testimony is the typical “nuisance” leakage associated with any type of field-effect transistor – similar to a slightly-dripping faucet; in contrast, what Patent Owner is trying to introduce as “evidence” for “leakage” being a problem in TFTs involves leakage that represents an unworkable transistor created by an unworkable manufacturing process – and this is a failure mechanism that is more akin to a burst water main than to a slightly-dripping faucet. Multiple references refute Patent

Owner's assertion that purported "leakage" was a real problem in 2003 for polysilicon TFT pixel circuits. *See, e.g.*, EX1032 and 1033 (1992 and 1999 articles showing de minimus amount (e.g., 1.5 pA/ μm) of polysilicon TFT leakage).

53. For completeness, it can be noted that the leakage current in Figure 1 of the 1997 paper bears a strong resemblance to a mechanism that has long been well-known in the art of mainstream silicon-based transistors – a mechanism known as gate-induced drain leakage ("GIDL," pronounced as "giddle")¹⁴:



27

GIDL was a much-bruited problem in silicon MOSFETs during the 1990s and into the 2000s, and was discussed as a possible limitation on the ability to further scale

¹⁴ Taken from a classroom slide deck: www.ece.ucdavis.edu/~ramirtha/EEC216/W09/lecture9.pdf; while the slide deck is dated "Winter 2009," the reference to "Roy & Prasad" is a reference to K. Roy and S. Prasad, "Low Power CMOS VLSI Circuit Design," Wiley, 2000 – which is prior art to the '599 patent.

down silicon MOS transistors – and thus as a possible limitation on the continuance of “Moore’s Law”; however, this problem was eventually overcome, and (of course) “Moore’s Law” has continued onward. Leakage of this sort in any type of field-effect transistor would be similarly a fatal flaw – and the correspondence between Figure 1 of the 1997 paper and the GIDL graph presented above is striking; even if the leakage mechanism present in the polysilicon-based TFTs of the 1997 paper is not in fact GIDL, the leakage mechanism clearly shows that the fabricated transistors in that 1997 paper (which show similar current-voltage leakage behavior) were unsuitable for product-grade usage, regardless of whether they were pMOS or nMOS transistors.

54. Further, as the figure presented above shows, for properly functioning field-effect transistors, the off-current will go to “ I_{off} ” at some designated gate voltage (such as $V_{\text{gs}} = 0$, as I explained in my Original Declaration and in my deposition testimony) – and if one pushes V_{gs} further in the “off” (voltage) direction, the current will decrease to a very low level and will remain at that low level as V_{gs} is pushed even further in the off direction. Field-effect transistors (such as those depicted in the 1997 paper) which do *not* exhibit this behavior (but rather behave as did those 1997 transistors) are essentially non-functional.

B. Kimura Renders Obvious a Shared Light emitting Signal

55. Dependent claim 13 (which depends from claim 7) requires that the gate

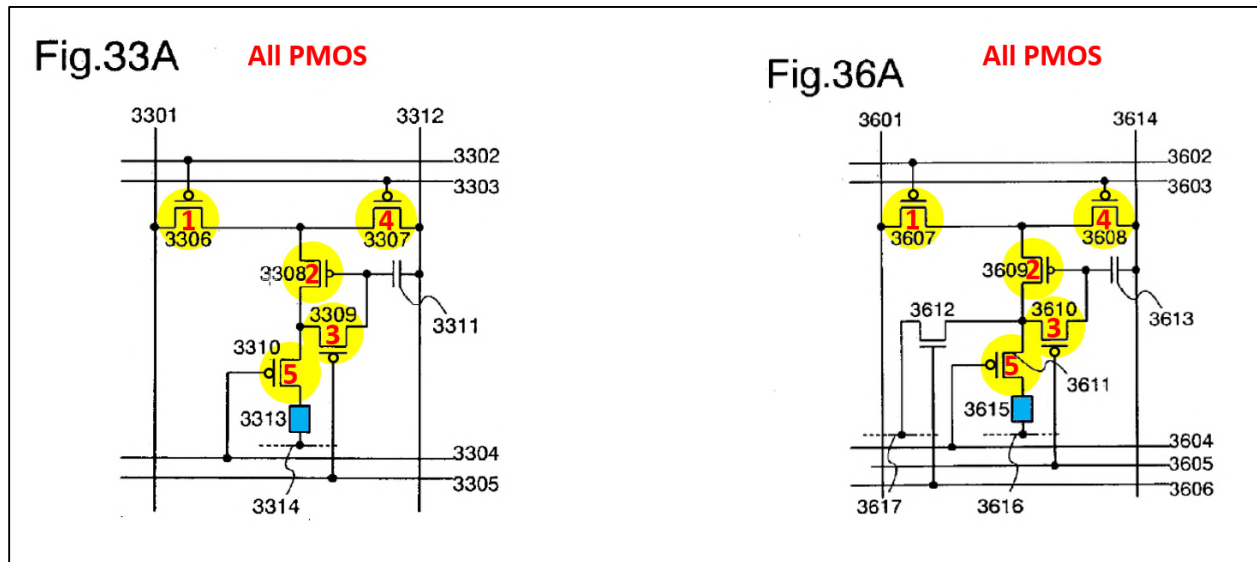
terminals of the “fourth” and “fifth” transistors be controlled by a shared “light emitting signal.” Independent claims 1, 14, 15, and 17 include the same requirement. I analyzed this limitation for claim 13 in my Original Declaration. EX1003, ¶¶255-259; *see also id.*, ¶¶283-288 (claim 14), ¶¶304-310 (claim 15), ¶¶341-348 (claim 17), and ¶¶378-391 (claim 1). In summary, as I stated in my Original Declaration, Kimura Fig. 33 does *not* show the fourth and fifth transistors being controlled by a shared light emitting signal. *Id.*, ¶257 (discussing that in Fig. 33B, “the fourth transistor is ‘OFF’ while the fifth transistor ‘ON’.”). However, Kimura Fig. 36 renders obvious a shared light emitting signal because the fourth and fifth transistors are *always* “ON”/“OFF” together in every operational phase (as shown in “Figure 36B (initialization), Figures 36C and 36D (programming), and Figure 36E (light emission)”). *Id.* Thus, “a POSITA would have been motivated to use a shared light emitting signal to control them” because, *e.g.*, Kimura itself teaches doing so to “reduc[e] the number of control lines.” *Id.*, ¶258 (citing Kimura, [0429], [0421]-[0422]).

56. The Board agreed that “if the fourth and fifth transistors are always turned on and off together, as Petitioner asserts is the case for the embodiment of Figures 36A–36E, there is reason for one of ordinary skill in the art to drive the fourth and fifth transistors by the same control signal, *i.e.*, reducing the number of control lines and improving aperture ratio.” Institution Decision at 51.

57. The most important thing to note is that Figure 36 is merely an extension of Figure 33, and almost everything is the same in both embodiments. The reason my Original Declaration did not repeat all of my Fig. 33 analysis for Fig. 36 is because these two embodiments are identical in most respects. Rather, I “note[d] at the outset that Kimura Figure 36 is just an extension of Kimura Figure 33, and that (unless noted) the analysis and discussion of one figure applies equally to the other throughout this Declaration.” EX1003, ¶ 130; *see also* Pet., 15 n.3. As detailed below, the only thing different about transistors one through five in Fig. 33 versus Fig. 36, is that the ON/OFF states of transistor four *always match* those of transistor five in Fig. 36. Accordingly, the analysis of Figure 33 for claim 7 fully applies to Figure 36 – and thus was used to render obvious claim 13.

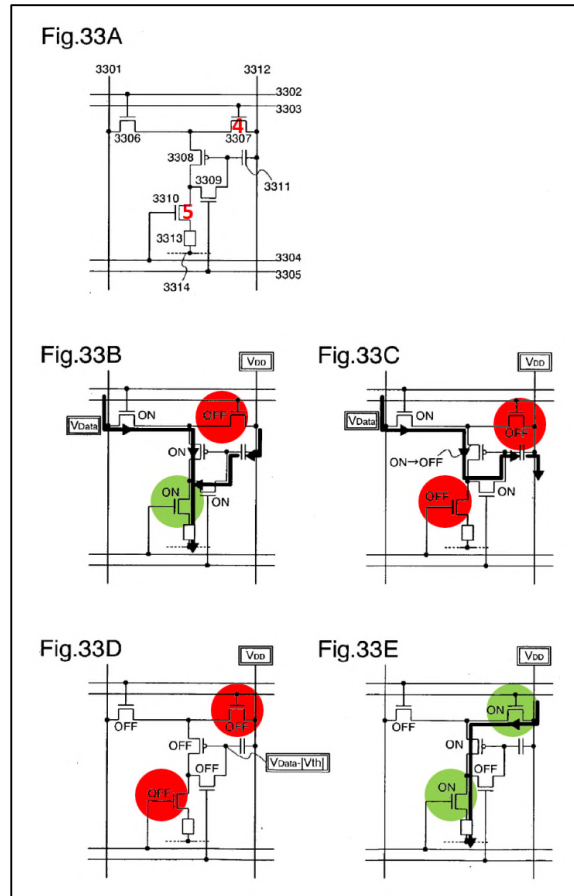
58. The only difference between the embodiments of Figures 33 and 36 is the addition of transistor 3612 to the Figure 33 embodiment (which creates the embodiment of Figure 36). This allows transistor 3611 (in Fig. 36) to always share a common operation state with transistor 3608, which in turn allows transistors 3611 and 3608 (which correspond to the fourth and fifth transistors in claim 7) to use a shared light emitting signal. *See* EX1002, Figs. 36B-36E. It is precisely this slight change in Fig. 36 that enables use of a shared light emitting signal. Moreover, all of the '599 claims are “comprising” claims – and thus they do not preclude the use/presence of an additional transistor in the pixel circuit. I note that most claims,

including claim 7, only require 5 transistors.



59. To provide a more detailed explanation here, I map and compare each operational phase in Figs. 33B, 33C, 33D, and 33E to its respective counterpart in Figs. 36B, 36C, 36D, and 36E to explain the role of transistor 3612 and how/why it allows the transistor 3611 to be “OFF” in Fig. 36B instead of “ON” (as is the case for transistor 3310 in Fig. 33B).

60. Examination of Figure 33 of Kimura shows that there is only one operational phase (Fig. 33B) where the fourth transistor (3608) and the fifth transistor (3611) are *not* operated with the same voltage level (OFF or ON) on their gate electrodes at the same time. Red is used to indicate “OFF” and green indicates “ON.”

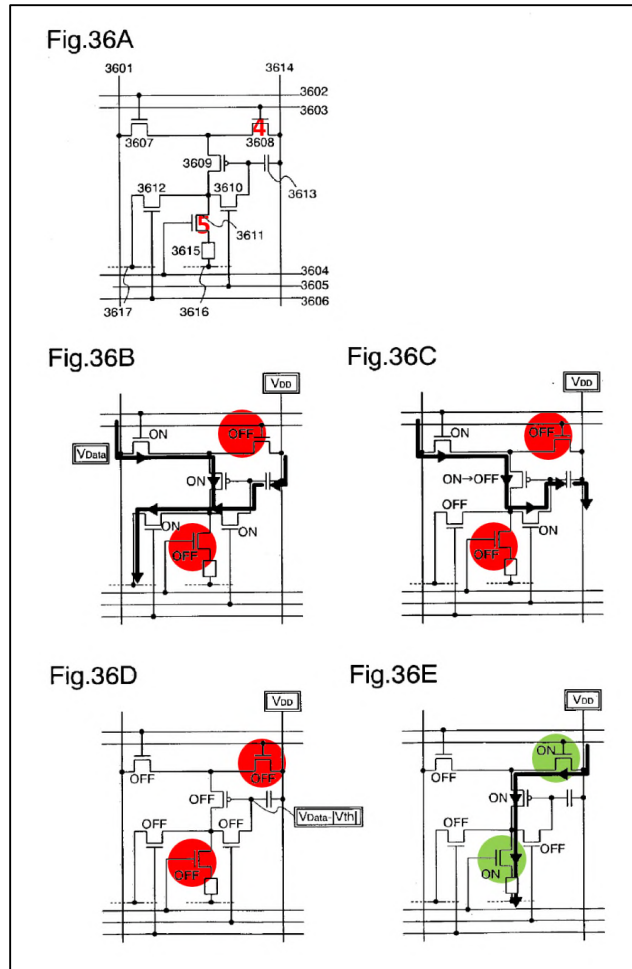


61. As can be seen, the only such instance occurs in the operational phase depicted in Figure 33B. Regardless of whether one calls this “initialization,” “erasure,” or “reset,” this is where the charge (voltage) on the storage capacitor is being drained off, in preparation for the next programming phase. As explained in my Original Declaration, this occurs because the fifth transistor (3310) is tasked with two separate jobs – it is turned on during the light emitting phase (Figure 33E) as part of the current path which directs current through the emitting device (3313) (when it is on together with the fourth transistor), but is *also turned on separately* (Figure 33B) to provide a path for the charge flowing off the storage capacitor during

the initialization/reset/erasure phase of operation. EX1003, ¶¶133, 139.

62. As explained in my Original Declaration, Kimura discusses this discharge path – noting that passing the capacitor-discharge current through the light emitter will cause a small and brief but potentially disruptive (to image quality) emission of light from the light emitter. EX1003, ¶¶155-158, 221. In the Fig. 33 embodiment, this is the price that is paid for having circuitry with one fewer transistor as the trade-off of saving space and simplifying the wiring.

63. As also explained in my Original Declaration, Kimura's Figure 36 embodiment is based upon the embodiment of Figure 33 – but provides the alternative version of the circuitry, in which a transistor is included for the purpose of providing a discharge path for the charge being drained off the storage capacitor during the initialization/reset phase. EX1003, ¶223.



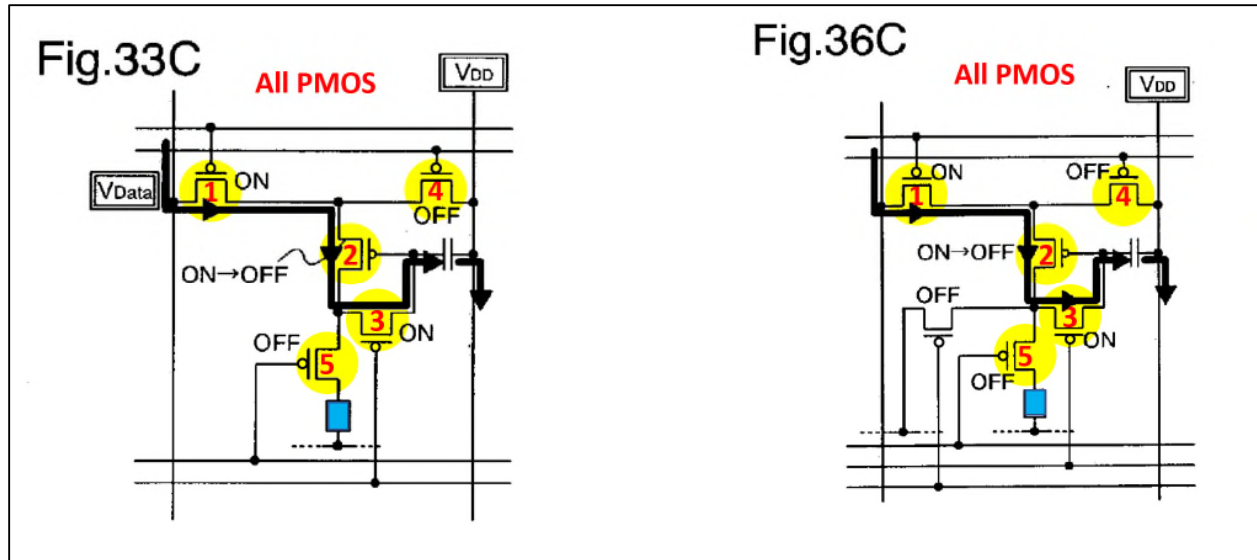
64. At the “cost” of one additional transistor in the circuitry, this discharge path does *not* go through the light emitter – and the undesirable “extra” light emission that occurs during this phase in the Figure 33 embodiment is eliminated. *See also* EX1003, ¶223.

65. In Figure 36, the fifth transistor (3611) is not tasked with two jobs (as was the situation for transistor 3310 of the Figure 33 embodiment). With only one job to do, the ON/OFF state of the fifth transistor will always match that of the fourth transistor (3608). As a result of this synchronized operation of the fourth transistor

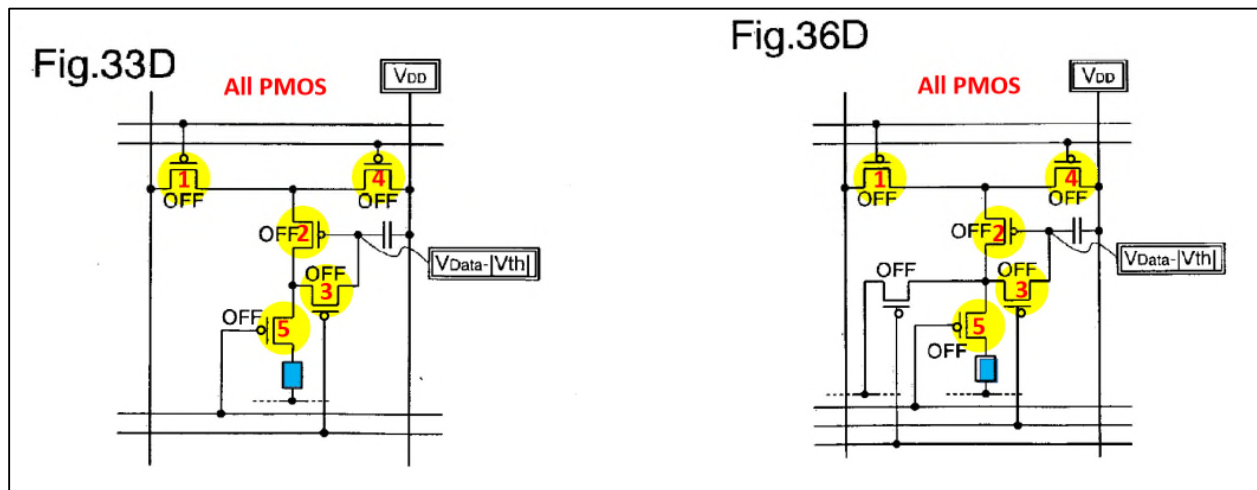
and the fifth transistor, a POSITA would have been motivated to use one control line for the gates of these two transistors – rather than two lines, with one each going to the gate electrode of each transistor; as noted in my Original Declaration, this is explicitly taught in Kimura (at [0421]-[0422] and particularly at [0429] – “The number of signal lines can be kept to a minimum and a high aperture ration [sic] can be obtained by using this type of structure...”). EX1003, ¶225 n.22; ¶258.

66. To summarize, the embodiments of Figures 33 and 36 are nearly identical – with one modification made to the Figure 33 embodiment to create the embodiment of Figure 36, and with that modification being done for a particular and well-explained (by Kimura) reason. And the shared light emitting signal is found using the Figure 36 embodiment and other teachings of Kimura.

67. I have already explained the structural and operational differences between Figures 33B and 36B. As can be seen in the side-by-side comparison below (for the programming operation in Figures 33C and 36C), transistors one, two, three, four, and five operate identically.

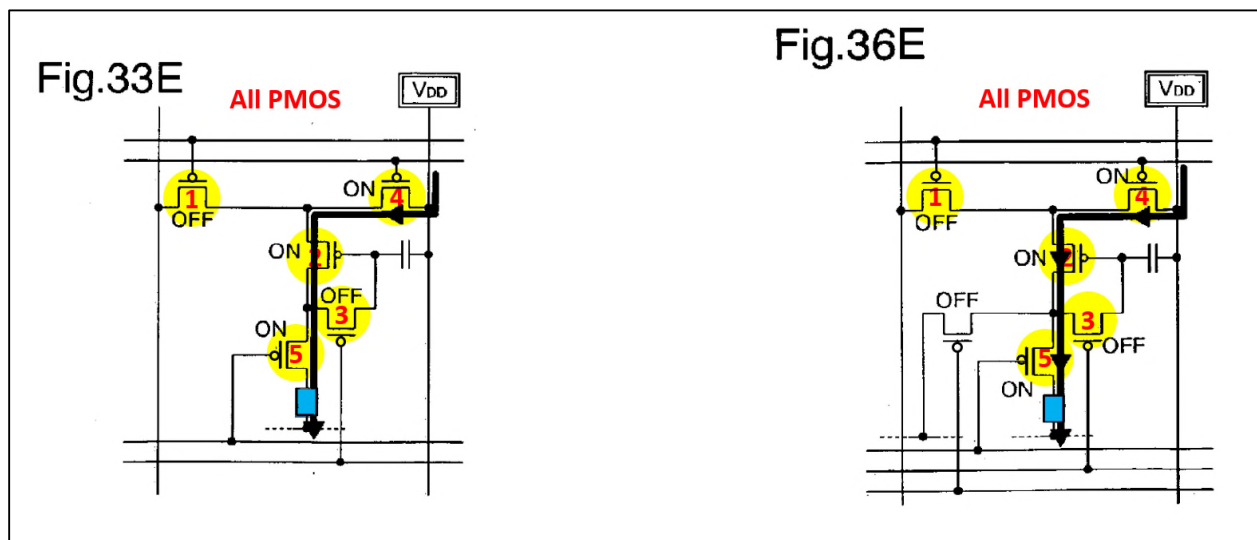


68. As illustrated below, the same is true for Figures 33D and 36D (*i.e.*, identical operation of transistors one through five); these (annotated) figures show that the results of the programming operation in each figure are the same (*i.e.*, the same voltage $V_{Data} - |V_{th}|$ has been stored on the capacitor in each case).



69. Likewise, the side-by-side comparison below shows that transistors one, two, three, four, and five behave identically (*i.e.*, if a given transistor is ON in Figure 33E, it is ON in Figure 36E – and vice versa) during the light emitting phase

in Figures 33E and 36E. Again, the only difference is the presence of the additional discharge transistor in Fig. 36E; however, this addition does not alter the operational behavior of any of the other transistors. In fact, because the additional discharge transistor is turned off (in all operational phases shown in Figs. 36C-36E), functionally it is equivalent to an open circuit, i.e., as if the transistor were not present (as it is absent in Figs. 33C-33E).



70. Patent Owner asserts that the proposed modification that renders obvious a shared light emitting signal results in an inoperable Figure 33 embodiment. POR, 4-5, 39-44; EX1028, 197:17-198:1 (Dr. Wolfe admitting that he did not opine on Figure 36 with respect to the shared light emitting signal limitations). This is a strawman argument – I did not propose modifying Figure 33 to create a shared light emitting signal. Instead, I used Kimura Figure 36 to show that Kimura renders obvious a shared light emitting signal. See EX1003, ¶¶261-65

(claim 13); ¶¶284-88 (claim 14); ¶¶304-10 (referencing claim 13 in discussion of claim 15); ¶¶341-48 (referencing claim 15 in discussion of claim 17); ¶¶382-83, 389 (referencing claim 13 and Figure 36 in discussion of claim 1). As shown above, the “extra” transistor in Fig. 36 is precisely what allows the use of a shared light emitting signal, as Dr. Wolfe admitted. EX1028, 196:18-197:5. Indeed, Dr. Wolfe agreed that Figures 36B-36E show the operation of a pixel circuit where transistors 3608 and 3611 are controlled by a shared light emitting signal. *Id.*, 201:22-202:9.

71. In my Original Declaration, I explained that “the timing diagram of Figure 16B would directly apply to the modified embodiment discussed in Section XII.B,” i.e., the Figure 33 embodiment with an added initialization/reset transistor based on Figures 16/17. EX1003, ¶142 (cited in Pet., 52, 54); *see also id.*, ¶¶169, 223, 336 (same); *id.*, ¶256 (using the timing diagram of Figure 16B to explain the light emitting signal). As further explained, the reset transistor based on Figure 16/17 is functionally the same as transistor 3612. *Id.*, ¶223 (referring to the reset-transistor modification based on Figures 16/17, noting “that at Figure 36, Kimura describes a similar modification – using an initialization transistor (3612) that is placed in a different location.”) (cited in Pet., 50-53). And as shown, the operations of Figures 33 and 36 embodiments are identical except during the initialization phase – where the added initialization/reset transistor 3612 allows the fifth transistor 3611 to be off. Accordingly, and as will be further explained in the next section, the shared

light emitting signal rendered obvious by Figure 36 would directly apply to the Figure 33 embodiment with an added initialization/reset transistor based on Figures 16/17. *Id.*, ¶130 (“Kimura Figure 36 is just an extension of Kimura Figure 33, and that (unless noted) the analysis and discussion of one figure applies equally to the other throughout this Declaration.”). Thus, my Original Declaration challenged claims requiring both a shared light emitting signal and an initialization transistor based on a shared light emitting signal rendered obvious by Kimura Figure 36 and an initialization transistor rendered obvious by Kimura Figures 16/17.

C. Attaching Kimura’s Initialization/Reset Transistor to the Capacitor It Discharges Is Obvious

1. A POSITA would have found the proposed configuration obvious and desirable based on Kimura

72. Claims 2, 8, 16, and 18 require an “initialization transistor” that, e.g., “discharg[es]” (*i.e.*, resets) the voltage stored on the capacitor before the capacitor is programmed. In my Original Declaration, I applied Kimura’s transistor 1607 (in Figs. 16/17) to the pixel circuit of Kimura Figs. 33/36 as the claimed “initialization transistor.” EX1003, ¶¶155-158, 215-230; *see also* Pet., 51-56. I further explained how the timing diagram of Kimura Fig. 16B “would directly apply to the modified embodiment” of Kimura Figs. 33/36. EX1003, ¶142 (highlighted figure correlating “initialization period” in ’599 patent timing diagram to “initialization” period in Kimura Fig. 16B); *see also* Pet., 16, 55-56.

73. Dr. Wolfe acknowledged that a POSITA would have understood initialization of pixel circuits and would have known how to discharge a storage capacitor in pixel circuits. EX1028, 76:4-21. He agreed that Figs. 16/17 show initialization of the storage capacitor. EX1028, 237:14-238:4, 242:9-243:6. Dr. Wolfe also agreed that Fig. 36B depicts discharging of the capacitor. *Id.*, 208:2-13. In fact, Figs. 16/17 and 36B show the same functionality, i.e., the initialization functionality of the '599 patent that sets the capacitor "to ... or near a predetermined level." *Id.*, 179:1-6. A comparison of the relevant figures makes this clear:

Fig.17A

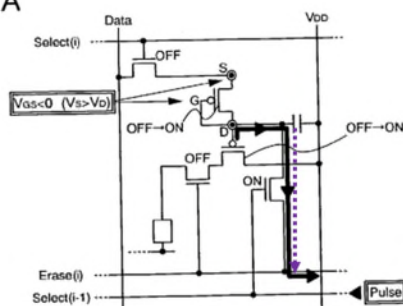


Fig.33A

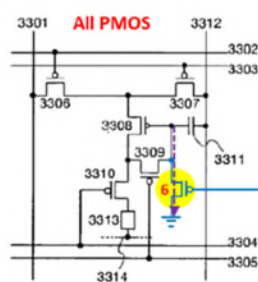
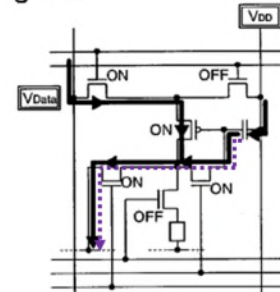


Fig.36B

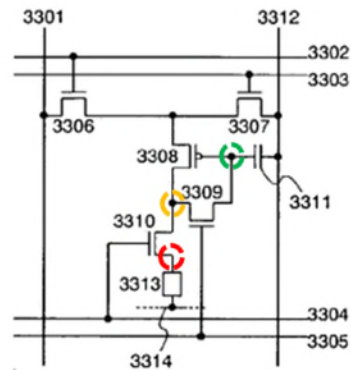


74. In the figures above, annotated purple arrows show the current path of the initialization operation. Kimura Figure 17A (left) shows the discharging/initialization of the storage capacitor to a low voltage line (the Erase(i) signal line). EX1002, Fig. 17A, [0426]; EX1003, ¶223. The modified Kimura Figure 33A (middle) shows the same. EX1003, ¶¶228-229, and Kimura Figure 36B (right) does as well. EX1002, Fig. 36B, [0666]; EX1003, ¶257.

75. There are only a limited number of design choices for initializing the capacitor of Figs. 33/36. The initialization must be performed through the (left)

terminal not connected to the high voltage source V_{DD} . In other words, a current path must be established between the terminal coupled to the gate of the driving transistor (3308 or 3609) and a current sink (or similar). To establish such a current path during only the initialization period (and to cut it off during other operational periods) by adding a transistor is the natural, logical, and most obvious choice – because there are already transistors in the circuit, and a switching transistor can perform the exact, desired function. As to the placement of this additional transistor, there are only limited options. A most obvious path is as shown in the modified Kimura Figure 33A, wherein the left terminal of the capacitor (green circle below) is directly coupled through the additional transistor to a low voltage (during initialization) line. Another obvious path goes through transistor 3309, which is coupled to the capacitor, and through the additional transistor coupled to the left terminal of transistor 3309 (orange). This results in the configuration of Kimura Figure 36A. Another possibility is to establish a current path through both transistors 3309 and 3310, adding an initialization transistor coupled between transistor 3310 and OLED 3313 (red circle). These three are the only possible options.

Fig.33A



76. A POSITA would have understood that these options for initialization incur a similar cost of one additional transistor. The “red” location would be less desirable because there could still be some residual current through the LED even when discharging the capacitor. This leaves only two reasonable options (*i.e.*, the “orange” and “green” locations). Kimura discloses both – the “orange” option is shown in Kimura Fig. 36, and the “green” option is shown in Kimura Fig. 16/17. The “green” placement as proposed in my Original Declaration is the most obvious and the most desirable because the initialization TFT is directly connected to the capacitor it is discharging and the drainage path involves a single TFT.

77. In fact, a POSITA would have recognized a rather natural progression from the embodiment of Figure 33 to the embodiment of Figure 36 – and then using the embodiment of Figure 17 as providing the basis for a superior modification of Figure 33 than is provided by Figure 36. While Figure 36 does include a dedicated, single-purpose “reset” transistor, the charge drainage path (from the capacitor to the

reset voltage terminal) passes through two transistors. This makes the circuit more complicated than necessary because it requires the control of two transistors (rather than one), transfers the “one transistor with two jobs” problem from transistor 3310 to 3610, and increases the resistance in the drainage path (because the current has to traverse two transistors rather than one, which will slow the discharge time). A POSITA would have found it obvious that it would be better to place the reset transistor in a different location in the circuitry – where the spurious emission problem could be avoided, yet the complexity of the circuitry would not be increased to the extent that it does in Figure 36. Further, a POSITA would have recognized that Kimura itself teaches doing just this in the Figs. 16/17 embodiment.

78. Additionally, the Petition and my Original Declaration articulated many reasons that would have motivated a POSITA to place an initialization transistor in the circuit of Figure 33A according to the placement of Figure 16A. Pet., 52-55 (citing EX1003, ¶¶221-30, 155-58, 141-43). For example, the need and techniques for resetting a circuit, especially one running cyclical operations like pixel circuits, were well known to a POSITA. EX1003, ¶155; EX1028, 76:4-10. Kimura’s Figs. 33 embodiment discloses a reset/erasure step, but with an expressly acknowledged shortcoming of spurious emissions. EX1003, ¶¶155, 221, 227. But Kimura also discloses embodiments such as that in Figs. 16/17 with a separate, dedicated reset transistor that does not have a similar shortcoming. *Id.*, ¶¶156-158,

222, 227. Kimura's express disclosure of such a transistor and corresponding timing diagram in Figs. 16/17 would have motivated a POSITA to study them, leading to a conclusion that they are directly applicable to the embodiments in Figs. 33/36. *Id.*, ¶¶141-42, 158, 223-25. And a POSITA would have found the trade-off of adding a dedicated transistor to eliminate the spurious emission to be desirable. *Id.*, ¶¶158, 221, 227. As I explained when asked at my deposition, "That's the point of the [dedicated reset/initialization transistor] modification, to have that *capacitor be drained without having it go through the electroluminescent element.*" EX2050, 120:1–15) (emphasis added).

79. Further, Kimura teaches that the additional initialization/erase transistor as shown in Figs. 16/17 may be controlled by the scan signal of the previous row, which eliminates the need to add a dedicated signal line at the expense of aperture ratio. *Id.*, ¶225; EX1002, [0429]. Kimura also teaches that the termination point of the initialization current path does not require an additional signal line. EX1002, [0430]. All of these reasons demonstrate that a POSITA would have found the proposed configuration obvious and would have been motivated to make it. EX1003, ¶¶228-29. Further, a POSITA would have found this proposed configuration to involve a simple addition, and would have had a reasonable expectation of success. *Id.*

80. Claims 2, 8, 16, and 18 also require that the reset transistor gate be

controlled by the scan signal for the previous cycle. While Kimura does not disclose specific timing diagrams for Figs. 33/36, Kimura does disclose a detailed timing diagram for Fig. 16/17 that shows that the previous scan signal controls the gate of the reset transistor (TFT 1607). Pet., 52; EX1002, [0429], [0426] (“The TFT 1607 turns on when the first gate signal line 1602 of the (i-1)th row is selected.”); EX1003, ¶¶155-158, 224-225; EX1028, 230:4-10. Moreover, as explained in my Original Declaration, the timing diagram for Fig. 16/17 directly applies to modified Kimura Fig. 33/36 with a reset transistor. EX1003, ¶¶141-142, 155-158, 223-225. I also explained how the timing diagram of Fig. 16B directly applies to the modified versions of Figs. 33/36 with a reset transistor directly connected to the capacitor. EX1003, ¶¶141-142, 223-225.

2. A POSITA would not have understood Kimura’s disclosure of “any location” for the erasure transistor as Patent Owner argues

81. As just explained, transistor 1607 in Figs. 16/17 and transistor 3612 in Fig. 36 both perform the same function, providing a current path to discharge the storage capacitor. This is the same function also performed by erasure TFT 3310. *See* EX1002, [0658], Figs. 33A-33B. A POSITA would have found it obvious to modify Figure 33 to add an initialization transistor as Kimura teaches in Figs. 16/17 (or to move the transistor 3612 in Kimura Fig. 36) to attach directly to the capacitor. Further (and notably), Dr. Wolfe calls transistor 3612 “[t]he erase transistor.”

EX1028, 189:14-22. He also says Kimura Fig. 36B shows “the erase phase,” and agrees that it is the only operational phase during which the erase transistor 3612 is turned on. *Id.*, 216:18-217:1. He further acknowledges that, during the erase phase, erase transistor 3612 performs the function of discharging the capacitor prior to the capacitor being programmed for a new cycle. *Id.*, 213:13-214:9, 216:6-217:1. Because Kimura teaches that “the erasure TFT can be placed in any location,” by Dr. Wolfe’s admission, erase transistor 3612 can be placed at the location in the proposed modified Fig. 33/36 configuration, as shown below. EX1003, ¶228 (citing EX1002, [0658]). The modified version of Fig. 36A below is identical to Fig. 33A with a reset/initialization transistor, as shown in my Original Declaration (¶¶223, 228).

Fig.36A All PMOS

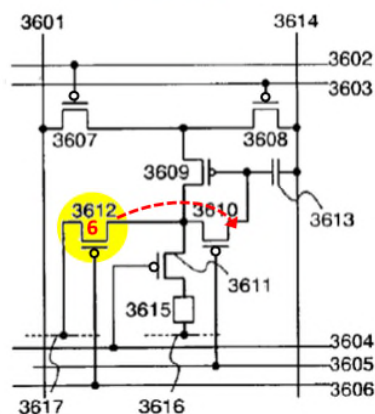
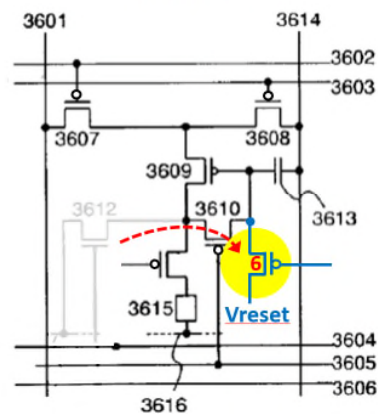


Fig.36A All PMOS



82. Samsung’s primary argument against this is based on a misunderstanding of part Kimura [0658], which states:

In addition, the erasure TFT can be placed in any location, provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing. (EX1002, [0658].)

83. Based on its interpretation of this disclosure, Patent Owner argues that an erasure transistor must be placed “along the current path to the EL device.” POR, 32; EX2008, ¶86. Patent Owner confuses the issues by incorrectly interpreting something that Kimura states – and then attempts to (falsely) conflate that misinterpretation into a general teaching in Kimura that supports the argument that Kimura forbids the suggested modification to Figure 33/36.

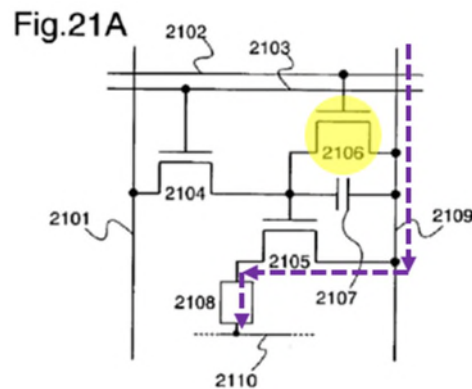
84. In my original Declaration (¶¶221, 228), I cited Kimura [0658] – as indicating that the “erasure TFT” need not be located where the Figure 33 embodiment places it, as transistor 3310 is located where it has two jobs (during the initialization period and emitting period as explained in ¶¶133 and 139 of my Original Declaration). Kimura teaches that the erasure transistor can be placed elsewhere (as Kimura does in the Figure 36 embodiment). However, Patent Owner misinterprets the statement that “provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing” – as stating that the “erasure transistor” must be the actor that is cutting off the electrical current to the emitter.

85. However, as mentioned above, this attempt by Patent Owner is misplaced – as Kimura is not stating (as Patent Owner attempts to conclude) that the

“erasure transistor” must be positioned so that it is able to be the actor which can cut off current to the emitter. This actually makes no sense – since it applies a very tight restriction on the location of the “erasure transistor” (i.e., directly in a path that connects to the emitter) rather than the “any location” that Kimura specifies. Further, “provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing” simply means that the only restriction on the placement at “any location” of the “erasure transistor” is that it cannot be placed at a location where it would *prevent* the cutting-off of the flow of current to the emitter (via the actions of the other parts of the circuitry). This actually makes sense – since (in both Kimura *and* in the ’599 patent) the capacitor is deprogrammed outside (temporally) of the light emitting phase of operation; since the deprogramming of the capacitor is *removing threshold voltage compensation from the pixel circuit*, doing so during the light emitting phase of operation would be self-defeating – and would make no sense with respect to how the circuit is described as operating.

86. Samsung’s argument limiting the meaning of an “erase” transistor is inconsistent with Kimura, which Dr. Wolfe conceded. For example, Kimura specifically identifies TFT 2106 in Figure 21A as “an erasure TFT.” EX1002, [0404]. Dr. Wolfe testified that TFT “2106 is described as an erasure TFT, and I believe that its role is to discharge the capacitor.” EX1028, 221:11-16; *see also id.*, 220:3-10 (“during the erasure period, [TFT] 2106 discharges the capacitor.”); *id.*,

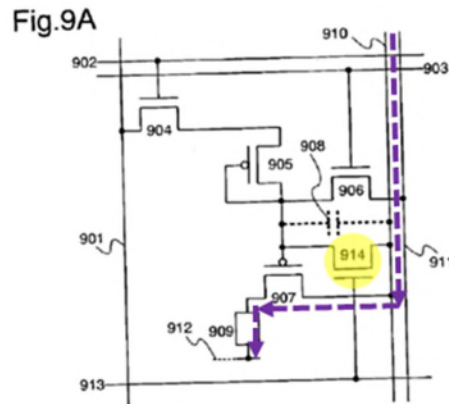
225:12-226:14 (stating that the only function of erasure TFT 2106 is to discharge the node coupling the capacitor 2107 and the gate of TFT 2105). And as a POSITA would have understood from Figure 21A, erasure TFT 2106 is *not* along the current path to the EL device because that current path (annotated purple below) runs through driver TFT 2105 (i.e., between its source and drain), whereas the current path of erasure TFT 2106 is coupled to the gate of TFT 2105:



Moreover, turning “erasure TFT 2106” on would normally turn on “driver TFT 2105” and cause current to flow through the LED, the *opposite* of what Patent Owner says an erasure TFT will do. EX1028, 221:17-223:12. Turning on “erasure TFT 2106” resets the capacitor 2107 to a known value, so it can then be programmed to a desired value using transistor 2104. EX1028, 221:11-16, 225:12-226:3. Turning “erasure transistor 2106” off will not cut off current to the LED, unless the power supply line 2109 has a low voltage. EX1028, 224:12-19. But in this circumstance, the LED cannot conduct current anyway since there would be no current available due to the power rail 2109 having a low voltage. In other words, the “erasure

transistor 2106” is performing an initialization/reset function (i.e., setting the storage capacitor to a known voltage before programming). *Id.*

87. Similarly, erasure TFT 914 (EX1002, [0407]-[0408], [0412]-[0416]) is *not* along the current path to the EL device:



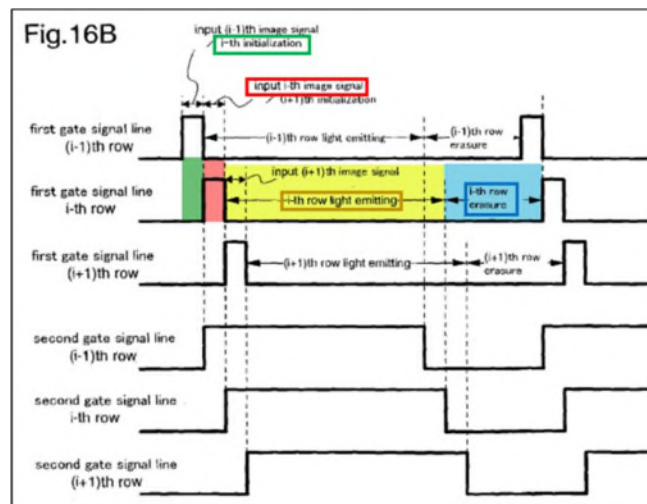
88. Relatedly, Kimura’s disclosure that “[i]t is also possible to use the TFT 3611 as an erasure TFT in this case” indicates that TFT 3611 is not necessarily used as an erasure TFT, but can be. EX1002, [0667] (emphasis added). This is consistent with Dr. Wolfe’s identification of TFT 3612 as the erasure TFT. When TFT 3611 is used as an erasure TFT (EX1002, [0667]), it is placed at a location that can cut off current to the EL device, and, consistent with the correct interpretation of Kimura, *not* at a location where it would *prevent* the cutting-off of the flow of current to the EL device. EX1002, [0658].

3. A POSITA would not have understood “initialization period” and “erasure period” in Kimura to be distinct as Patent Owner argues

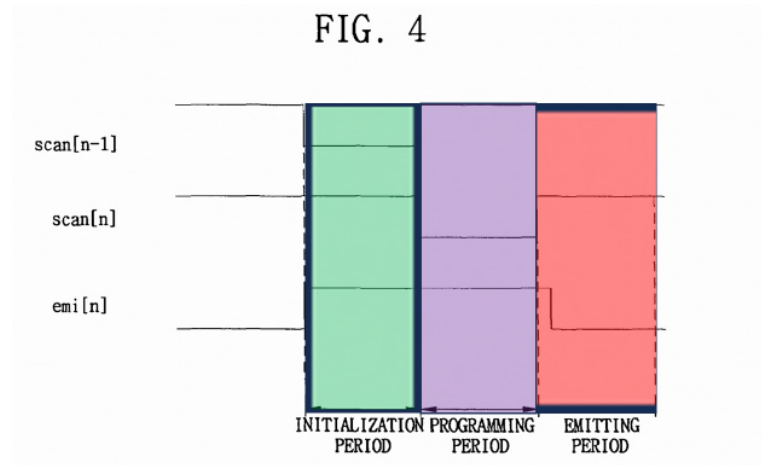
89. Patent Owner’s argument against the proposed configuration

incorporating an initialization/reset transistor focuses on a supposed distinction between “initialization” and “erasure.” POR, 26-33. However, Patent Owner’s argument is simply incorrect.

90. Dr. Wolfe asserts that “the timing diagram of Figure 16B of Kimura ... identifies an ‘initialization’ period that is distinct from the ‘erasure’ period, i.e., the two periods are not co-extensive.” EX2008, ¶83. This is the same flawed argument as the one that appeared in the POPR – where Samsung color-coded Fig. 16B (shown below) and asserted that “this figure separately identifies ‘erasure’ and ‘initialization’ as distinct operational phases.” POPR, 17-18.

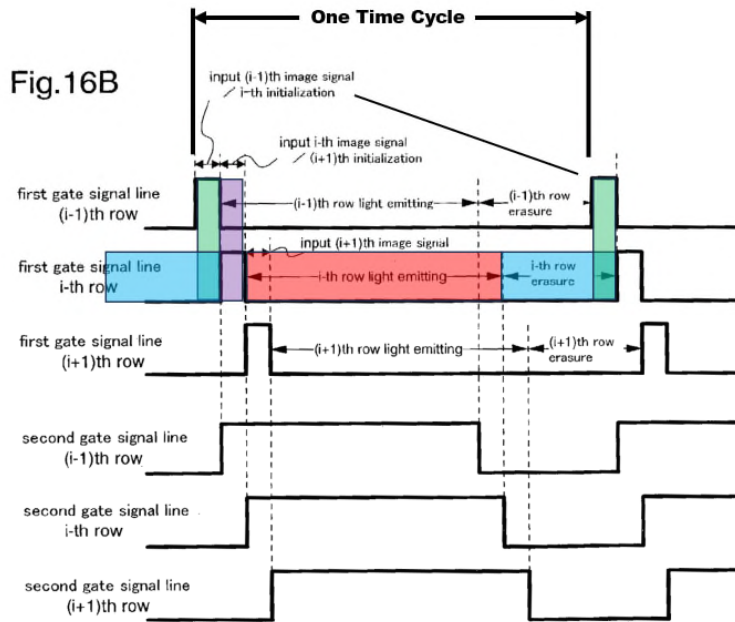


91. The '599 patent discloses a single circuit embodiment – and a single timing diagram (Figure 4) describing the operation of that circuit:



EX1001, Fig. 4 (annotations added). This timing diagram details the three (repetitive) phases of operation of the pixel circuitry of the '599 patent – the “initialization period” (annotated in green), the “programming period” (purple), and the “emitting period” (red). Implicit in this diagram is that the functions of this one cycle will be repeated in the next cycle, in the same way as the current cycle. Note that, as can readily be seen in both the original (unannotated) Figure 4 and in the annotated version above, the “emitting period” begins as soon as the “programming period” ends – but the actual signal change that initiates light emission occurs after the “emitting period” has already begun. Stated another way, light emission occurs during the “emitting period,” but light emission is not occurring during the entirety of the “emitting period.”

92. Kimura provides a similar timing diagram in Figure 16:



EX1002, Fig. 16B (annotations added). As a preliminary note, unlike the '599 patent, Kimura provides a timing diagram that is longer than a single (repetitive) cycle – and thus, an annotation is provided to identify a single time cycle.

93. Comparing Figure 4 of the '599 patent to Figure 16B of Kimura, it can readily be seen that, while the period definitions and name labeling are different, both the '599 patent and Kimura are describing the same operations.

94. First, as per the time periods annotated in red in both figures above, what the '599 patent calls the “emitting period” is called the “light emitting” period by Kimura – but the same function (the feeding of a threshold-compensation-adjusted current to the emitter to cause it to emit light) is being carried out.

95. Second, as per the time periods annotated in purple in both figures above, what the '599 patent calls the “programming period” is called the “image

signal” period by Kimura – but, once again, the same function (the programming of the capacitor) is being carried out.

96. Third, as per the time periods annotated in green in both figures above, what the ’599 patent calls the “initialization period” is also called the “initialization” period by Kimura – and the same function (the deprogramming of the capacitor in preparation for its programming in the succeeding “programming period” (’599 patent) / “image signal” period (Kimura)) is being carried out.

97. The ’599 patent and Kimura differ in this last function in a way that does not affect how the claims of the ’599 patent read on Kimura – in that the ’599 patent describes an “initialization period” (in green above), while Kimura describes an “initialization” period (also in green) that is a subset of a larger time period that Kimura describes as the “erasure” period. Dr. Wolfe agrees that the “erasure” period overlaps with the “initialization period.” EX1028, 232:2-233:6.

98. Therefore, both the ’599 patent and Kimura describe the same three time periods in a single cycle, being carried out in the same order – with the only difference (that the initialization in Kimura occurs within the erasure period, while in ’599 patent the initialization covers the entire period) being immaterial to the comparison of the functionalities of the ’599 patent and Kimura. Note also that, as detailed above, the ’599 patent actually describes a similar situation (of a function occurring as a temporal subset of a larger time period) – where, a function (light

emission) is not being carried out over the entirety of the time period (the emitting period) in question, but only during part of the time of that defined period.

4. No Additional Signal is Required

99. Contrary to Patent Owner's assertion (POR at 33-34), this option for the initialization transistor does not necessarily incur a cost of an additional signal line, e.g., Erase(i) or the ground terminal.

100. I explained in my Original Declaration that the initialization current path may terminate at "ground (or similar)." EX1003, ¶229; EX2050, 129:17-130:1. That termination point of the current path simply needs to be low for the charge on the capacitor to drain away. EX1003, ¶321 (explaining that the termination point "is to drain charge to a known default value"); EX2050, 127:20-128:11. Kimura discloses that the initialization transistor "may [instead] be connected to other signal lines, provided that the other signal lines become L level at the same timing as the [initialization] TFT 1607 turns on." EX1002, [0430]. Accordingly, I explained in my Original Declaration that an option for the termination point is to "connect[] to the light emitting signal (i.e., the second gate signal labeled 1604)," as shown in Figure 16A. EX1003, ¶321. In the Figure 33 embodiment, the light emitting signal is the existing signal line 3303, which is low during the initialization period to turn off transistor 3307 as required:

Fig.33A

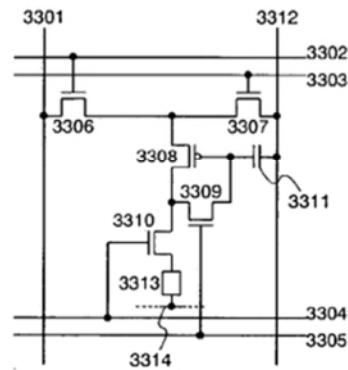
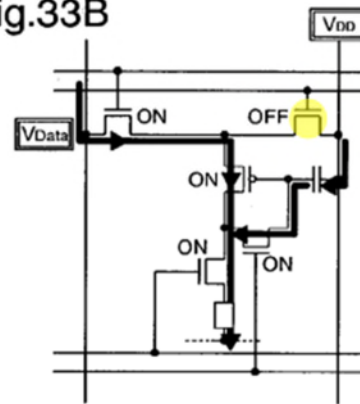


Fig.33B



Accordingly, Kimura teaches that the termination point of the initialization current path does not require an additional signal line. Specifically, in the modified Figs. 33/36 configuration, the initialization transistor may be coupled to line 3303 (or, equivalently, 3603). Patent Owner asserts that I testified to the contrary. POR, 27. That assertion is incorrect, as the actual cited testimony reveals. EX2050, 117:21-118:14 (cited by POR, 27). Even if an additional signal line is used (e.g., due to other design considerations since doing so is not necessary), that would simply be an aspect of the engineering trade-off between adding a control line versus eliminating the spurious light emission that occurs during capacitor reset. Which implementation to choose is an engineering decision, which depends on a variety of factors (such as the manufacturing process in use, the type of display being designed and manufactured, etc.).

VI. SAMSUNG'S SECONDARY CONSIDERATIONS FAIL

101. In the POR, Patent Owner makes an extensive effort to assert non-

obviousness via secondary considerations. However, examination of this effort indicates that is fatally flawed.

102. As an initial matter, it should be noted that in my Original Declaration, I provided no discussion of secondary considerations – as at that point, Patent Owner had not provided any assertions regarding secondary considerations.

103. It is my understanding that in order to demonstrate secondary considerations of non-obviousness, the patent owner must demonstrate what I understand is known as a *nexus* – that is basically, they must show clearly how the inventions claimed by the particular patent actually enabled and facilitated that success. The recitations by Patent Owner do not do that; while Patent Owner lists product success, product recognition, and employee recognition, there is no showing of how the Challenged Claims enabled that success.

104. For example, Samsung's Galaxy S21 smartphone contains a myriad of other components and features beyond a pixel circuit. Thus, even if the pixel circuit on Galaxy S21 practices the Challenged Claims as Patent Owner asserts, the success of the smartphone may very well be the result of components and features other than the pixel circuit. Patent Owner has shown no evidence tying the success of the Galaxy S21 to the pixel circuit. To the contrary, it is my understanding that Patent Owner has also asserted in other, related proceedings that the Galaxy S21 practices other, unrelated patents of Patent Owner. Thus, absent evidence to the contrary

(which Patent Owner has not shown), it is an overreach to attribute success of the Galaxy S21 (or any other smartphone) to the '599 patent. Even if the circuitry disclosed in the '599 patent is contained in the recited products, that does not amount to showing a nexus – as presence alone cannot be taken as indicating enablement of success.

105. Patent Owner focused on two “benefits” it says the '599 patent provides: (1) “display uniformity”; and (2) “aperture ratio.” *See, e.g.*, POR, 63; *see also id.*, 49-50 (uniformity), 51 (aperture ratio), 57-58. I discuss each below.

106. Patent Owner asserts that display uniformity enabled by the threshold-voltage compensation scheme of the '599 patent supports non-obviousness. However, neither Dr. Wolfe nor Patent Owner has disputed that threshold-voltage compensation was known in the prior art. *See generally* POR; EX2008. My Original Declaration cited four references on threshold-voltage compensation. EX1003, ¶¶77-78. In fact, using diode-connected transistors to “mak[e] practically identical copies of [a circuit] without the need for accurately matched components” was known at least since 1988. EX1031 (“Daubert”), 1; EX1028, 213:9-12 (Dr. Wolfe conceding that diode-connected configuration in '599 patent was known in the prior art). I understand that known techniques cannot provide nexus between a claimed invention and alleged evidence of secondary considerations.

107. Regarding aperture ratio, I understand that Patent Owner in another IPR

proceeding attributed aperture ratio achieved by Galaxy smartphones to unrelated patents on pixel layout. Furthermore, Patent Owner's own exhibit attributed aperture ratio of Samsung's displays to a different technology, not the pixel circuit of the '599 patent. Specifically, Dr. Wolfe characterized Yoo as a paper "submitted to the Society of Information Display" by "Samsung SDI (... a predecessor to [Patent Owner] Samsung Display) researchers." EX2008, ¶132 (citing EX2015). Dr. Wolfe further stated that the pixel circuit in Yoo "is the same pixel circuit as the one shown in Figure 3 of the '599 Patent." *Id.*, ¶133. Dr. Wolfe then proceeded to state how, in his view, Yoo supports the non-obviousness of the '599 patent. An examination of Yoo, however, reveals a different story. Specifically, while Yoo attributes "improve[d] image quality" to "Vth compensating pixel circuit" (which, as just explained, was known in the prior art), Yoo attributed a "40% aperture ratio" to "2µm design rule in LTPS [low-temperature polysilicon] TFT fabrication process."¹⁵ EX2015, 3. Yoo also attributed a high display resolution and aperture

¹⁵ Note that here, Samsung is describing the use of a faster, denser TFT manufacturing process (with smaller minimum feature sizes); as noted in Section V.A, this is the same sort of transistor scaling that is known in popular parlance as "Moore's Law" – whereby transistor-based circuitry becomes smaller and faster by coherently scaling-down the size of transistors. This ability to make smaller transistors allows (among other things) for improvements in the aperture ratio – as this paper discusses.

ratio to an LITI (laser induced thermal imaging) method. *Id.*, 1-2. Yoo did not attribute aperture ratio to the pixel circuit, a fact that Patent Owner ignored.

108. Patent Owner makes further attempts to show secondary considerations of non-obviousness – but those attempts fail as well.

109. Patent Owner asserts that the all-pMOS embodiment of the '599 patent overcame skepticism. POR, 52. This makes no sense – as Patent Owner's own exhibit (which Dr. Wolfe relied upon) shows all-pMOS pixel circuits. *See* EX2008, ¶¶114, 117, 119. So, too, does Kimura. EX1002, Fig. 22.

110. Patent Owner contends that others have engaged in “slavish copying” of Patent Owner's display products – not just “copying,” but “*slavish* copying.” POR, 47. This would clearly imply that the resulting alleged “copies” would be identical to the content of Patent Owner's products – and Patent Owner provides comparative teardown analyses (of their own products and the products of competitors who allegedly “slavish(ly)” copied Patent Owner's products). However, even cursory examination of these results (from teardowns) shows that the Patent Owner's products and the products of those who supposedly “slavish(ly)” copied Patent Owner's products are notably different.

111. For example, the alleged BOE copy has an extra signal line in its pixel circuit. POR, 60, EX1028, 256:7-16. Without knowing what the extra signal is or even where the image came from, Dr. Wolfe alleged copying. EX1028, 256:1-6,

256:17-257:1. As “slavish copying” would produce identical results, Patent Owner’s assertion is simply false. Similarly, Dr. Wolfe cited a number of teardown images allegedly of displays from other manufacturers. EX2008, ¶¶160-61. But he did not create these images himself. *Id.*, ¶159. He did not know any of the entities associated with the displays (e.g., MobileSentry, Mengtor, etc.). EX1028, 260:3-262:10. He did not know the person who created the images, Dr. Silzars. *Id.*, 29:22-30:2. He did not speak to Dr. Silzars. *Id.*, 254:12-13. He did not ask Dr. Silzars to perform the teardown. *Id.*, 254:14-19. These allegations are not the product of a reliable method.

112. At p. 47 and p. 50 of the POR, Patent Owner attempts to assert secondary considerations of non-obviousness based on the “failure of others” – by listing several supposed competitors, and asserting that their failure to produce display products equal to Patent Owner’s is a demonstration of this failure. However, this list of “competitors” is actually misplaced – as none of the organizations listed are manufacturers of displays. For example, “Sarnoff” is a research entity, not a display manufacturer. I further note that the assignee of Kimura was the aforementioned Semiconductor Energy Laboratory (EX1002, 1), and that public sources indicate that Semiconductor Energy Lab licensed its display

patent portfolio to LG.¹⁶ This is significant – because few, if any, of the roster of “competitors” that Patent Owner has provided are actually competitors, and Samsung is silent about companies (such as LG) that are active participants in OLED display manufacturing and that have achieved commercial success. Thus, Patent Owner has failed to show secondary considerations of non-obviousness.

113. On pp. 48-49 of the POR, Patent Owner attempts to show secondary considerations of non-obviousness by referring to a textbook that states “pixel-to-pixel level device variation is the key issue that makes the AMOLED panel a concern for certain applications” as evidence that pixel non-uniformity during emission was a long-known problem. EX2010, 30. However, it is notable that this textbook was published in 2008 – three years after publication of the ’599 patent application and five years after the priority date that the ’599 patent claims. In addition, this textbook was published five years after the publication of Kimura’s patent application. Thus, this textbook cannot be regarded as authoritative – as it is referring to “long-known problems” that had, in fact, already been solved by Patent Owner and others. Therefore, this textbook clearly fails to provide evidence of secondary considerations of non-obviousness.

114. In summary, while Patent Owner has provided several assertions of

¹⁶ See https://www.koreatimes.co.kr/www/tech/2021/10/129_317669.html.

secondary considerations of non-obviousness, all of them fail.

VII. CONCLUSION

115. I am aware that this declaration will be filed as evidence in an IPR proceeding before the PTAB. I am aware that making willfully false statements in my declaration are punishable by fine or imprisonment, or both (under 18 U.S.C. § 1001), and thus such actions may compromise the validity of the IPR proceeding. All statements herein made by me of my own knowledge are true, and all statements made on information and belief are believed to be true.

116. I declare under penalty of perjury that the foregoing is true and correct.
Executed this 31st day of May, 2024 in Fletcher, Vermont.



Daniel Foty, Ph.D.