

III. RESULTS AND DISCUSSION

A. FID TFT Characteristics

The I_d - V_g characteristics of an n-channel FID TFT at $V_s = 60$ V are shown in Fig. 3(a). For comparison, those of a conventional TFT are shown in Fig. 3(b). The conventional TFT has a large I_{OFF} that increases as negative gate voltage and positive drain voltage increase. On the other hand, the FID TFT has a sufficiently low I_{OFF} that remains almost constant regardless of gate voltage. I_{OFF} is as low as $1.5 \text{ pA}/\mu\text{m}$ ($V_d = 10$ V, $V_g = -20$ V), and I_{ON} is sufficiently high. Thus an ON/OFF current ratio of 10^7 is achieved at $V_d = 10$ V.

However, a sub-gate voltage of 60 V is too high for the application of an FID TFT. It is necessary to obtain a low-resistivity inversion layer at low sub-gate voltage. There are two methods considered to realize that. One is the use of a thinner interlayer or a higher dielectric constant interlayer. The other is the reduction of the threshold voltage in the sub-gate region. We use a SiN_x interlayer deposited by plasma CVD to reduce the threshold voltage in the sub-gate region. The I_d - V_g characteristics of a conventional TFT with a SiN_x gate insulator are shown in Fig. 4. This TFT has a lower threshold voltage (-3 V) than does a TFT with an SiO_2 gate insulator (Fig. 3(b)). The V_s dependence of I_{ON} and I_{OFF} for an FID TFT with an SiO_2 interlayer and an FID TFT with a SiN_x interlayer are shown in Fig. 5. In the FID TFT with a SiO_2 interlayer, a sub-gate voltage of more than 60 V is necessary to obtain an ON/OFF current ratio of 10^7 . On the other hand, using a SiN_x interlayer, a high I_{ON} and a low I_{OFF} can be obtained even at a sub-gate voltage of about 10 V.

The I_d - V_g characteristics of a three-terminal FID TFT with its sub-gate connected to the drain ($V_d = 10$ V) are shown in Fig. 6. In the FID TFT with a SiO_2 interlayer, the I_{ON} is very low. I_{ON} of the FID TFT with a SiN_x interlayer was successfully increased while maintaining a sufficiently low I_{OFF} . This means that a simple circuit configuration is applicable to the FID TFT.

B. FID Junction Characteristics

FID junction characteristics were investigated to clarify the reason why a low I_{OFF} is obtained in the FID TFT. The I_d - V_s characteristics of the FID TFT at $V_g = 20$ V are shown in Fig. 7(a). Under this condition, an inversion layer is formed under the main gate and two reverse-biased junctions are formed in the OFF state ($V_s < 0$ V). One is a conventional drain junction (J1). The other is a junction between and the n-type inversion layer induced under the main gate and the p-type inversion layer induced under the sub-gate (J2). This result shows that the inversion layer under the main gate also reduces I_{OFF} . On the other hand, the I_d - V_s characteristics of a conventional TFT with a sub-gate only are shown in Fig. 7(b). This result shows that the conventional drain junction (J1) is leaky. Therefore, in Fig. 7(a), the anomalous leakage current is blocked at the junction J2, that is, an FID junction.

The temperature dependence of the I_{OFF} of the FID TFT

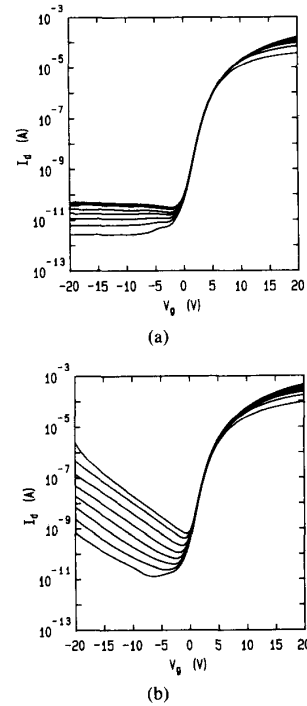


Fig. 3. I_d - V_g characteristics of n-channel FID TFT ($V_s = 60$ V) (a) and conventional TFT (b). ($V_d = 2.5$ -20 V, 2.5-V step.)

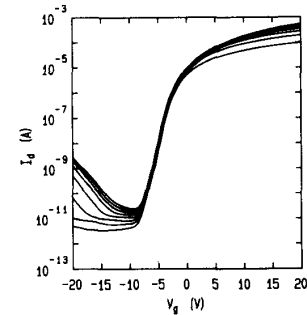


Fig. 4. I_d - V_g characteristics of conventional TFT with SiN_x gate insulator. ($V_d = 2.5$ -20 V, 2.5-V step.)

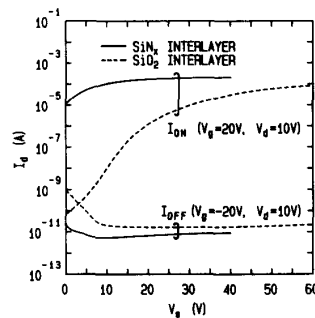


Fig. 5. V_s dependence of I_{ON} and I_{OFF} in FID TFT with SiO_2 interlayer or SiN_x interlayer.

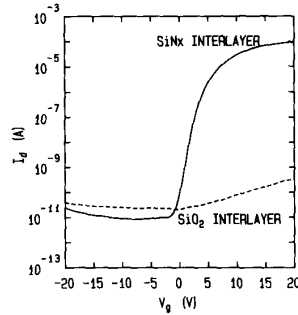


Fig. 6. I_d - V_g characteristics of FID TFT with sub-gate connected to drain ($V_d = 10$ V).

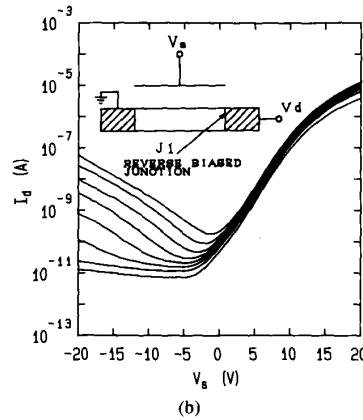
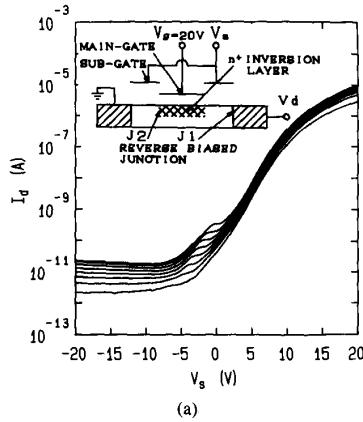


Fig. 7. I_d - V_s characteristics of FID TFT at $V_g = 20$ V (a) and conventional TFT with sub-gate only (b). ($V_d = 2.5$ -20 V, 2.5-V step.)

($V_s = 60$ V) and a conventional TFT are shown in Fig. 8. I_{OFF} was measured at $V_g = -20$ V, $V_d = 10$ V. The I_{OFF} of the conventional TFT shows a weak temperature dependence due to field emission current [5]. On the other hand, the FID TFT has a strong temperature dependence at an activation energy E_a of 0.52 eV. It is considered that this current is due to generation-recombination of carriers at mid-gap states.

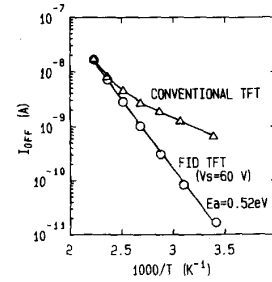


Fig. 8. Temperature dependence of I_{OFF} in FID TFT ($V_s = 60$ V) and conventional TFT. (I_{OFF} : $V_g = -20$ V, $V_d = 10$ V.)

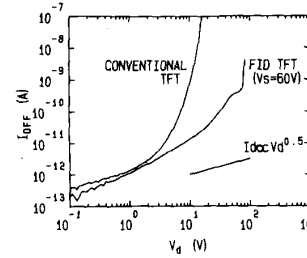


Fig. 9. V_d dependence of I_{OFF} in FID TFT ($V_s = 60$ V) and conventional TFT. (I_{OFF} : $V_g = -20$ V.)

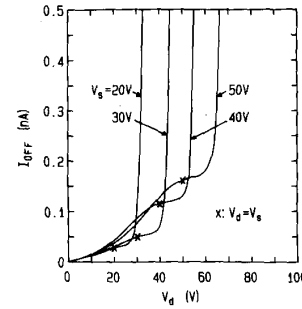


Fig. 10. V_s dependence of V_d - I_{OFF} characteristics.

The V_d dependence of I_{OFF} of the FID TFT ($V_s = 60$ V) and a conventional TFT are shown in Fig. 9. I_{OFF} was measured at $V_g = -20$ V. In the conventional TFT, I_{OFF} abruptly increases with increasing V_d because of the field emission current at drain junction. On the other hand, the I_{OFF} of the FID TFT increases proportional to V_d^x ($x = 0.5$ -1), and exhibits breakdown characteristics at about $V_d = 70$ V. The V_d dependence of I_{OFF} also suggests that the I_{OFF} of the FID TFT is dominated by the generation-recombination current at the drain junction.

The V_s dependence of the V_d - I_{OFF} characteristics is shown in Fig. 10. The strong dependence is observed between breakdown voltage (V_B) and V_s . Increasing V_s makes V_B high. The increase I_{OFF} is suppressed at $V_d = V_s$, and the breakdown occurs at higher V_d . To explain this V_s dependence of V_B , we consider the changing of the

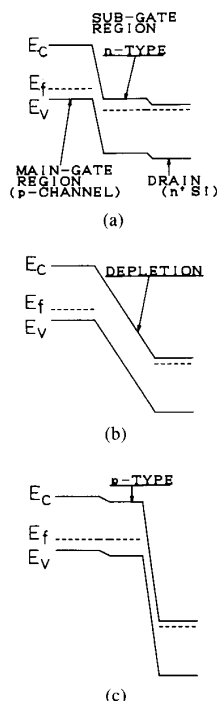


Fig. 11. Band diagram of sub-gate region at drain side. (a) $V_d < V_s$. (b) $V_d = V_s$. (c) $V_d > V_s$.

band-bending in the sub-gate region, as shown in Fig. 11. The V_s dependence of V_B results from the band-bending in the sub-gate region being changed by V_s . When V_d is lower than V_s , an n^+ inversion layer is formed under the sub-gate. Under this condition, I_{OFF} is blocked at the FID junction as shown in Fig. 11(a). However, when V_d is near V_s , the energy band of poly-Si under the sub-gate region does not bend and the depletion region extends from the drain to the p channel induced by negative V_g as shown in Fig. 11(b). In this condition, the V_d dependence of I_{OFF} decreases because the electric field caused by drain voltage is distributed in the depletion region. When V_d is larger than V_s , the energy band bends to induce hole carriers. In this condition, a reverse-biased conventional drain junction is formed as shown in Fig. 11(c), and high-leakage current flows. This is the reason for the abrupt I_{OFF} increase resulting in breakdown.

The improvement in the drain junction characteristic of the FID TFT over the conventional TFT is considered to be due to a reduction in the trap density at the drain junction. The junction in the FID TFT is free from additional defects caused by the doping process. This is considered to be the reason for the low trap density and low I_{OFF} .

IV. CONCLUSION

The characteristics of an FID TFT using an inversion layer as a drain were investigated. An I_{OFF} of 1.5 pA/ μm ($V_d = 10$ V, $V_g = -20$ V), and an ON/OFF current

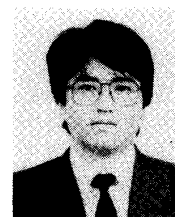
ratio of 10^7 were successfully obtained with the FID TFT. Furthermore, reducing the threshold voltage of the sub-gate region allows a simple circuit configuration to be applied to these TFT's. Measurement of the junction characteristics proved that the I_{OFF} of the FID TFT is dominated by generation-recombination current, not by the field-emission current. These results indicate that FID TFT's can improve the characteristics of poly-Si TFT circuits such as active-matrix circuits of LCD's.

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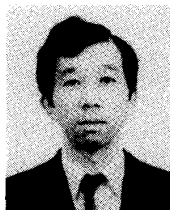


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