

A Self-Aligned Offset Polysilicon Thin-Film Transistor Using Photoresist Reflow

Jung-In Han and Chul-Hi Han

Abstract—A simple fabrication method for a self-aligned offset structure, which uses photoresist reflow, is developed to reduce the leakage current of polysilicon thin-film transistors (poly-Si TFT's). The reflow of photoresist can be controlled by varying photoresist thickness and reflow temperature. It is found that the reflow length increases in proportion to the photoresist thickness, and increases with increasing reflow temperature at less than 200 °C for the AZ5214A photoresist. Poly-Si TFT's are successfully demonstrated with offset lengths of 0.4 and 0.6 μm , which show apparent reduction of the leakage current.

Index Terms—Offset, photoresist, polysilicon, reflow, TFT.

I. INTRODUCTION

POLYSILICON thin-film transistors (poly-Si TFT's) are widely used as switching devices in active-matrix liquid crystal displays (AMLCD's) and load devices in static random access memories (SRAM's). However, the poly-Si TFT has a large leakage current, which is a major disadvantage for AMLCD and SRAM applications. It is well known that the leakage current is mostly determined by generation via trap states in the depletion region near the drain [1]. The generation is enhanced by high electric field near the drain junction. An offset or lightly doped drain (LDD) structure has been widely used to reduce the leakage current by suppressing the electric field near the drain junction [2], [3]. Several approaches to realize self-aligned offset structures have been investigated [4]–[6]. However, the fabrication processes are still complex and the offset length is limited to a small value.

In this work, we propose a new fabrication method for the self-aligned offset structure. The offset structure is achieved by thermally baking the photoresist film, which is used to pattern and form the gate poly-Si. The method does not require new masking material and an additional mask. The offset length can be controlled by varying photoresist thickness and reflow temperature.

II. EXPERIMENTS

Fig. 1 shows schematically the fabrication process for the self-aligned offset poly-Si TFT's. A 1000-Å thick amorphous Si film was deposited by low-pressure chemical vapor deposition (LPCVD), and crystallized at 600 °C for 24 h. A 500-Å thick gate oxide was thermally grown at 1100 °C. Then, a 3000-Å thick poly-Si film as a gate electrode was deposited at 580 °C and doped with phosphorus using a

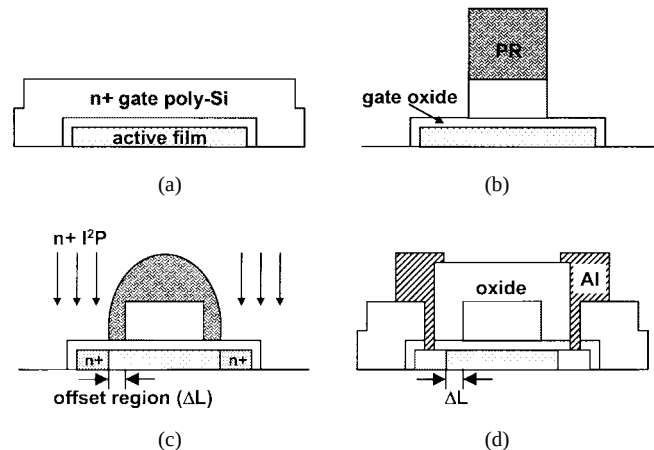


Fig. 1. Process sequence for proposed self-aligned offset poly-Si TFT's: (a) Active poly-Si and gate oxide formation, followed by gate poly-Si deposition, (b) gate lithography and gate poly-Si etching, (c) photoresist reflow and source/drain ion implantation, and (d) interlayer oxide deposition and metallization.

solid diffusion source (PH-1000N) at 950 °C [Fig. 1 (a)]. The photoresist film, AZ5214A, Hoechst Co., was coated in 1000 or 2000 r/min for 30 s. Then, soft-baking, exposure, and development were performed for the gate electrode pattern. We could define 1- μm patterns. After photoresist patterning, the poly-Si film was etched in a mixed solution of HNO_3 , H_2O , and HF [Fig. 1(b)]. After wet etching, the samples were baked at 200 °C for 40 min for the reflow of photoresist [Fig. 1 (c)]. The measured reflow lengths are 0.6 and 0.4 μm for 1000 r/min and 2000 r/min, respectively. After the reflow process, phosphorus ions were implanted to form the source and drain. Since the reflowed photoresist acts as a mask, the ions are not implanted in the reflowed region, which results in the offset structure. After a passivation film of SiO_2 was deposited, dopant activation and metallization were performed [Fig. 1 (d)]. The wafers were alloyed at 420 °C for 30 min in 10% H_2/N_2 ambient. For comparison, poly-Si TFT's without the reflow step were also fabricated.

III. RESULTS AND DISCUSSION

To control the offset length using the photoresist reflow process, the dependence of the reflow length (ΔL) on spin speed, reflow temperature, and reflow time has been investigated. Fig. 2(a) shows the measured photoresist thickness and the reflow length as a function of the coating speed. The reflow was performed at 200 °C for 40 min. As the coating speed increases, the thickness and the reflow length of the photoresist film decrease. The reflow length is almost propor-

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The authors are with the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology, Taejeon 305-701, Korea (e-mail: ygyhji@samsung.co.kr.).

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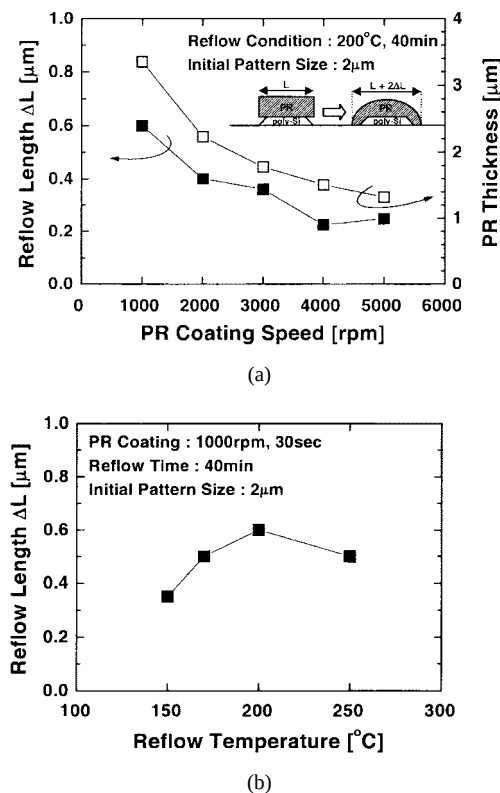


Fig. 2. (a) Reflow length and photoresist thickness versus coating speed. (b) Reflow length versus temperature.

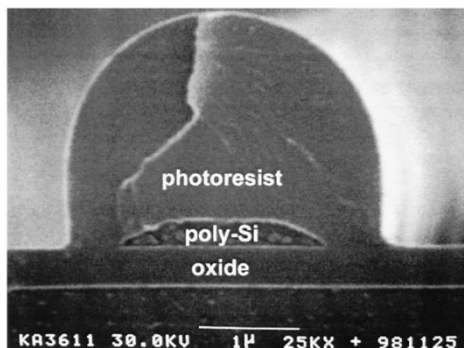


Fig. 3. Cross-sectional view of the gate pattern after reflow step. The photoresist was coated in 1000 r/min for 30 s and the reflow was performed at 200 $^{\circ}\text{C}$ for 40 min.

tional to the initial thickness of photoresist. Fig. 2(b) shows the reflow length versus reflow temperature. The reflow length increases with increasing temperature from 150 to 200 $^{\circ}\text{C}$. The reflow length does not change with the reflow time of longer than 5 min. Fig. 3 shows a cross-sectional scanning electron microscopy (SEM) picture of the gate pattern after the reflow step. The photoresist was coated in 1000 r/min for 30 s and reflowed at 200 $^{\circ}\text{C}$ for 40 min after etching of poly-Si.

I_D - V_G characteristics of the fabricated poly-Si TFT's with different reflow lengths are shown in Fig. 4. The channel width and length of the poly-Si TFT's are 10 and 2 μm , respectively. The device without offset ($\Delta L = 0$ μm) shows an exponential dependence of the leakage current on V_G and short-channel effects in high V_D region, that is, the increase of the subthreshold current and threshold voltage shift [4],

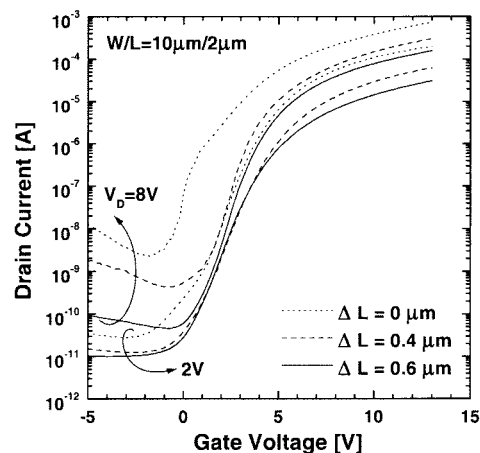


Fig. 4. Measured I_D - V_G characteristics of poly-Si TFT's with the self-aligned offset structure, and a typical nonoffset TFT.

[7], [8]. With the reflow length (ΔL), the leakage current is effectively reduced and becomes less dependent on V_G . Compared to the device without offset, the leakage current is reduced by an order of magnitude when the reflow length of 0.4 μm is introduced, and by two orders of magnitude when the reflow length is 0.6 μm . For ΔL of 0.6 μm , the ON/OFF current ratio is $\sim 10^6$, and the short-channel effects are suppressed, but the ON current is reduced about four times due to the series resistance of the offset region [5].

IV. CONCLUSION

We have developed a simple process for poly-Si TFT's with a self-aligned offset structure. The self-aligned offset structure has been achieved without any additional mask and masking material. The process is based on the photoresist reflow, which can be controlled by photoresist thickness and reflow temperature. The reflow length of photoresist increases with increasing reflow temperature and photoresist thickness. We have demonstrated that the leakage current and short channel effects of poly-Si TFT's can be significantly reduced with proper control of the reflow length.

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