

## But Petitioner Relied on Fig. 36

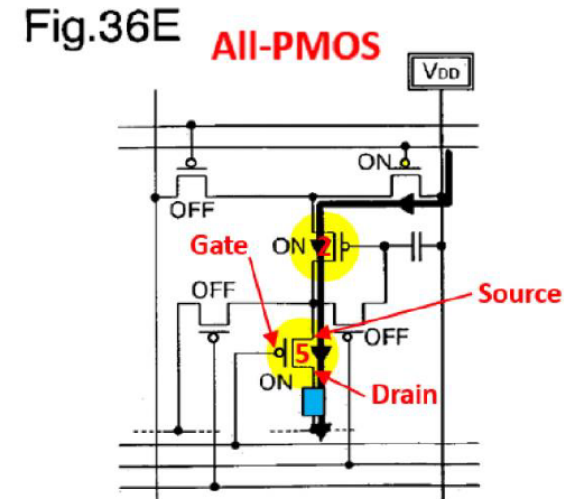
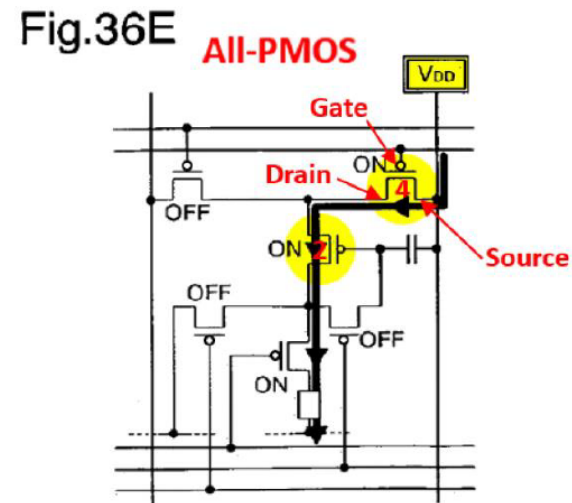
<sup>3</sup> It should be noted to Kimura Fig. 36 is merely an extension of Fig. 33 and discussion of one applies equally to the other unless noted.

130. This particular embodiment in Kimura is contained in Figure 33 and described at [0654] – [0657]. It is important to note at the outset that Kimura Figure 36 is just an extension of Kimura Figure 33, and that (unless noted) the analysis and discussion of one figure applies equally to the other throughout this Declaration.

discussion of one figure applies equally to the other.”). Petitioner cited Fig. 33 for claim 7 instead of Fig. 36 because Kimura itself used Fig. 33 to explain circuit operation and simply noted differences when describing subsequent figures, like Fig. 36, that build off Fig. 33. *See* Kimura, [0652]-[0668].

## But Petitioner Relied on Fig. 36

are already PMOS in the all-PMOS version of Fig. 33. And the all-PMOS version of Kimura Fig. 36, discussed below, renders claim 13 obvious.



Pet. (Paper 1), 62-63 (top); 66 (left); *Id.*, 67 (right)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE PDX-46

## The Motivation is to Modify Fig. 36, not Fig. 33

36B (initialization), Figs. 36C-D (programming), and Fig. 36E (light emission)), the fourth and fifth transistors are always ON/OFF together. EX1003, ¶257. Thus, a POSITA would have understood (or at least found it obvious) that Kimura uses a shared light-emitting signal to control them. EX1003, ¶256-259. Kimura itself provides one reason for doing so—reducing the number of control lines improves aperture ratio. See, e.g., EX1002, [0429]; see also *id.*, [0421]-[0422] (control scheme with fewer signals reduces “surface area occupied by wirings in a pixel”). Additionally, the fourth and fifth transistors must both be active during light emission, otherwise the electroluminescent element will not emit light. EX1003, ¶¶138-140; see also EX1002, [0659] (signals “turn[ing] on and off at the same timing...can therefore be controlled by using the same gate signal line”). This, too, would have naturally led a POSITA to use a shared light-emitting signal. EX1003, ¶¶258-259.

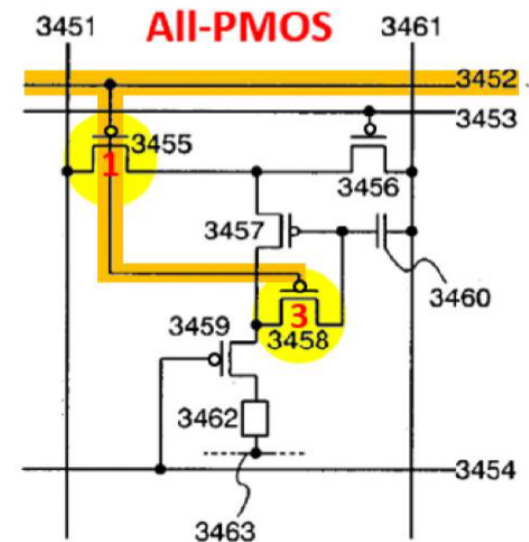
## The Motivation is to Modify Fig. 36, not Fig. 33

Moreover, Kimura discloses a timing diagram and control scheme utilizing only two signals (*i.e.*, first and second gate signals which map to the claimed “scan line signal” and “light emitting signal” respectively). *See* EX1002, Figs. 16-17 and explanation at [0420]-[0429]; EX1003, ¶259. This disclosure would have motivated a POSITA to use a shared light emitting signal for the fourth and fifth transistors and provided a reasonable expectation of success. EX1003, ¶259.

## The Motivation is to Modify Fig. 36, not Fig. 33

[0659] Furthermore, a gate signal line for controlling a TFT can be shared among a plurality of TFTs, as shown in FIGS. 34A and 34B. For example, the TFT 3306 and the TFT 3307 are controlled so as to turn on and off at mutually

Fig.34B



## Dr. Wolfe has No Opinion Fig. 36 is “Inoperable”



3 Q And in Paragraph 263 of his declaration,  
4 Dr. Foty mapped the fifth transistor onto Kimura  
5 Figure 36, correct?

6 A **He does.**

7 Q Okay. Going back to the Kimura reference  
8 itself, is it your opinion that Figure 36 in Kimura  
9 is inoperable?

10 A **No. Only that it operates differently**  
11 **than Figure 33.**

## Dr. Wolfe Agrees a Shared Light Signal in Fig. 36 is Operable



22 Q Okay. How, if at all, would the  
1 operational states depicted in Figure 36B, C, D and E  
2 be any different if transistors 3608 and 3611 were  
3 controlled by a shared light-emitting signal?

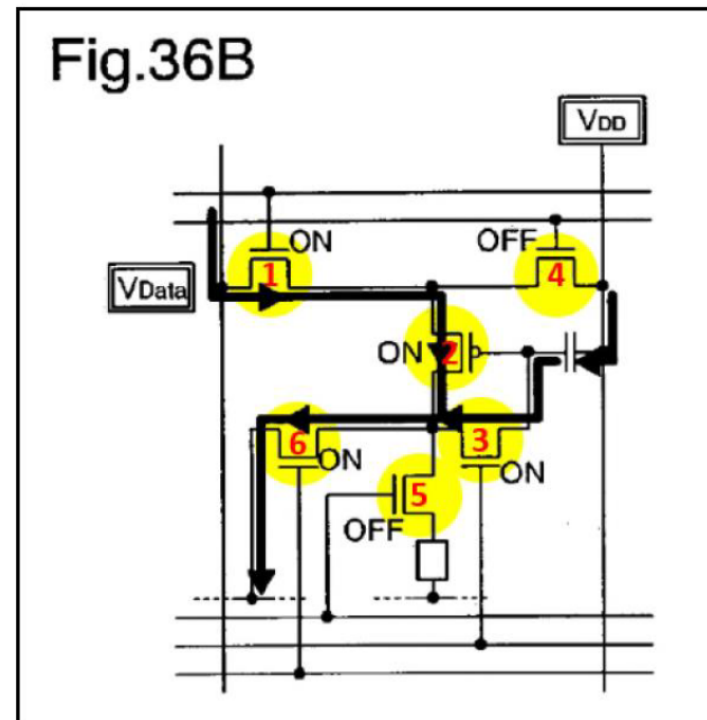
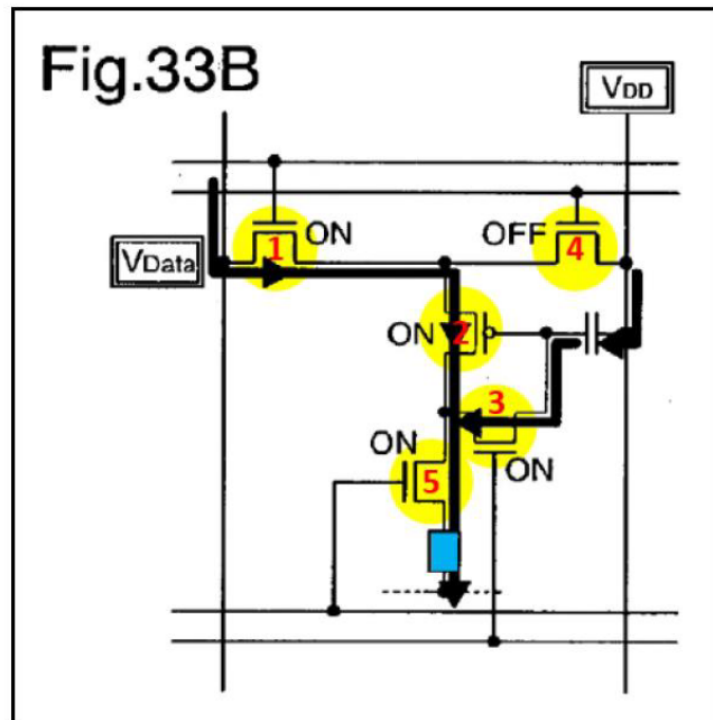
4 MR. GARR: Objection.

5 THE WITNESS: If you start from  
6 Figure 36 and you combine them and you  
7 only have the illustrated operations,  
8 then I don't think there would be a  
9 difference.

## PO's Procedural Argument Fails

This attempt to rely on the “extra” transistor circled in red—i.e., TFT 3612—is effectively the same new theory that Petitioner attempted to introduce in its Motion to Submit Supplemental Information. In denying that motion, the Board credited Patent Owner’s explanation that the “supplemental declaration relies on an additional transistor from Figure 36, transistor 3612, which was neither referenced nor discussed in the Petition or Dr. Foty’s original declaration with respect to claim 13.” Paper 27, 10 (quoting Paper 19, 5). As the Board explained, the “additional modifications including adding

# The Role of TFT 3612



Pet. (Paper 1), 19 (citing EX1002 (Kimura), Figs. 33 and 36)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE PDX-53

# The Role of TFT 3612

Fig.33A All PMOS

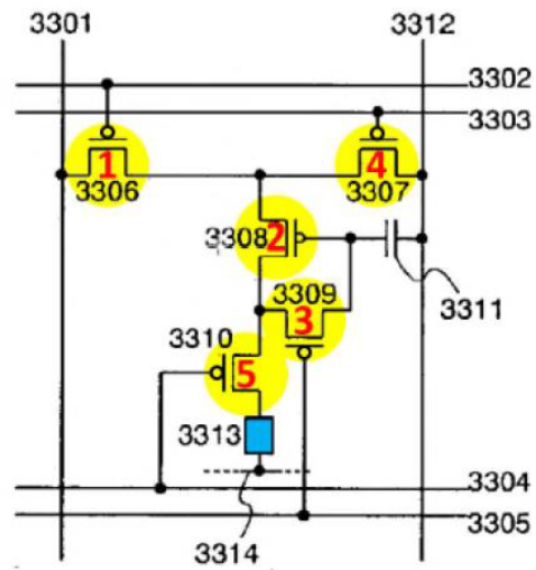
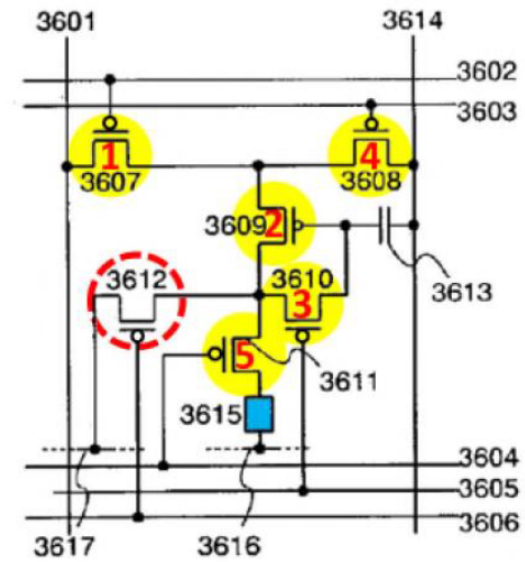


Fig.36A All PMOS

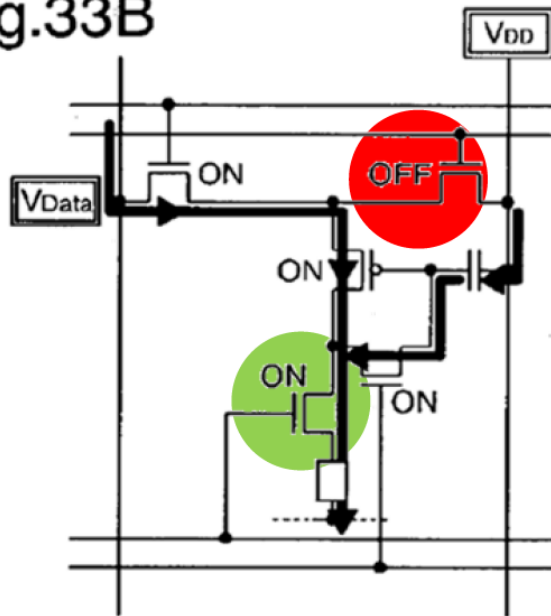


Reply (Paper 41), 11 (left); *Id.*, 13 (right)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE PDX-54

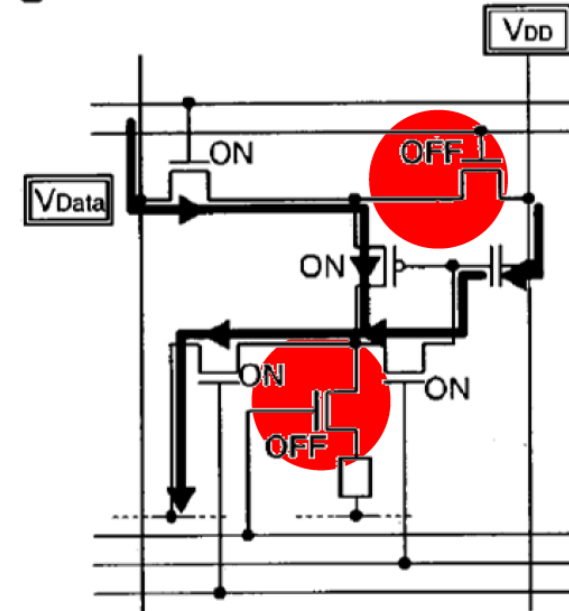
# The Role of TFT 3612

Fig.33B



Reply (Paper 41), 11 (left); *Id.*, 13 (right)

Fig.36B



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE PDX-55

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Background / Intro

All-PMOS

Shared Light Signal

**Initialization/Reset TFT**

Secondary Considerations

POSITA Issues

CITE

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE PDX-56

## The “Initialization” Claims

- The parties agree dependent claims 2, 8, 16, and 18 require an “initialization transistor” (or a “sixth transistor” that receives an “initialization voltage”). *See* POR (Paper 33), 26
- And that claims 1, 3-7, 9-15, and 17 do NOT require such a transistor

## The “Initialization” Claims

8. The pixel circuit in the organic light emitting device of claim 7, further comprising:

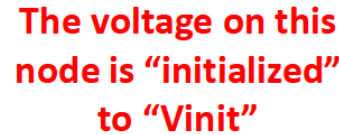
a sixth initialization transistor for discharging the data signal voltage stored in the capacitor in response to a scan signal just before the current scan signal upon initialization.

16. The pixel circuit in the organic light emitting device of claim 15, further comprising:

a sixth transistor including a gate to which a scan signal just before the current scan signal is applied;  
a source coupled to the one terminal of the capacitor; and  
a drain to which an initialization voltage is applied.

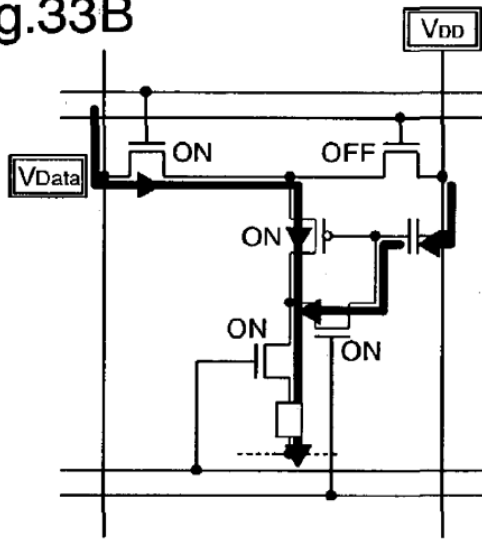
## The '599 Specification – Fig. 5 (the Claimed Embodiment)

FIG. 5



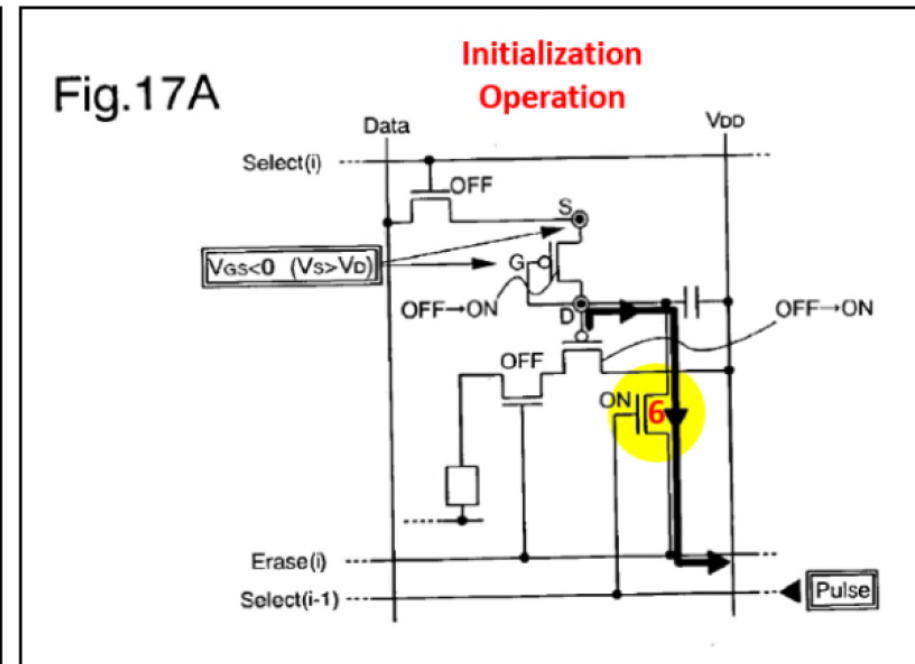
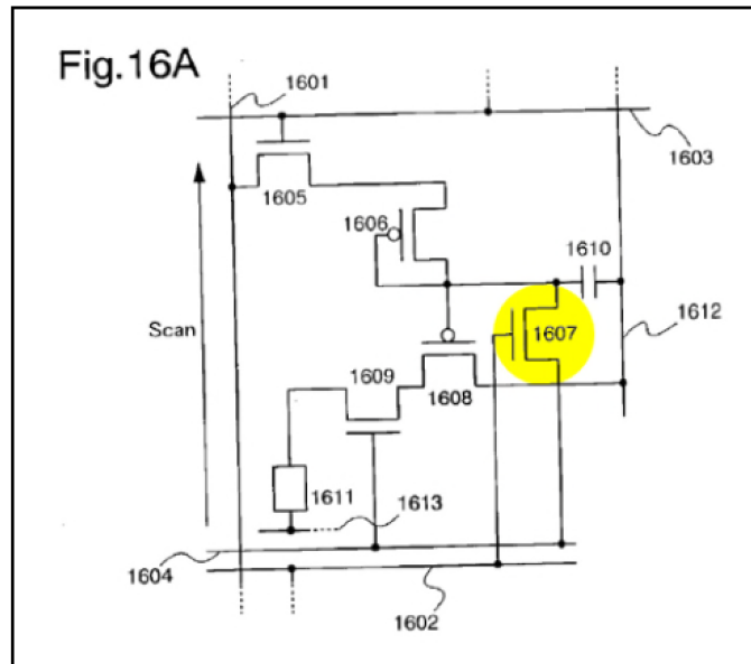
## Kimura Fig. 33 has Spurious Light Emission

**Fig.33B**



[0665] In the structures shown FIGS. 33 to 35, there are cases in which electric current flows in the EL device to cause light emission, before or after threshold voltage acquisition, that is during a period that is not the normal light emitting period. In these cases the value of the electric current flowing in the EL device is not necessarily equal to the image signal plus the correct threshold value, and this therefore causes errors to develop between the actual brightness and the target brightness.

# Kimura Fig. 16/17 and Fig. 36 Solve this Problem



## Dr. Wolfe Admits Kimura Fig. 16/17 Discloses “Initialization”



14 Q Okay. And you would agree with me that  
15 Figure 17A is the same circuit shown in Kimura Figure  
16 16A?

17 A Yes.

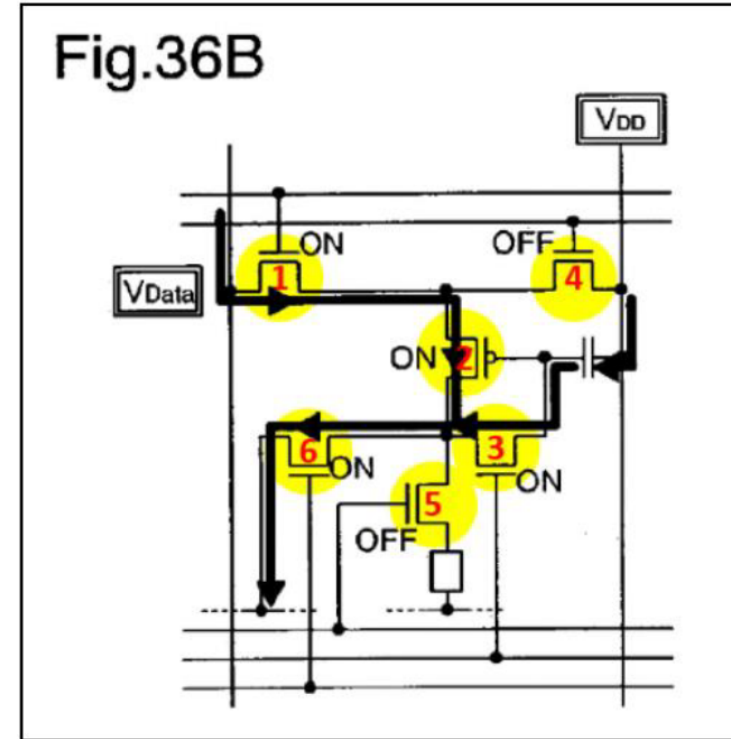
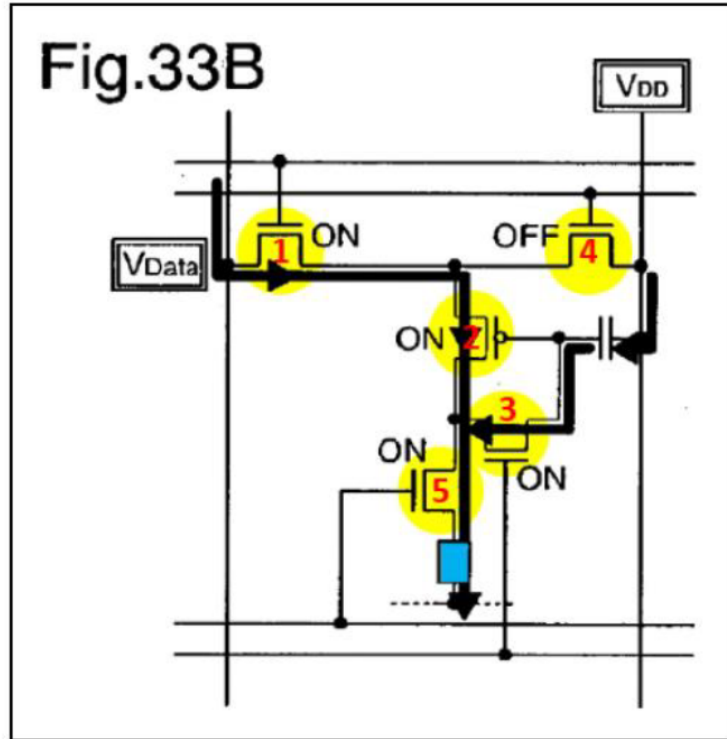
18 Q And in Kimura Figure 17A, the transistor  
19 1607 is on, correct?

20 A Yes.

21 Q And what is happening to the charge  
22 stored on the capacitor during the phase shown in  
1 Figure 17A?

2 A The voltage on that node that connects  
3 the capacitor to 1308 drops, and that's what's  
4 described as initialization in Paragraph 426.

## Kimura Fig. 16/17 and Fig. 36 Solve this Problem

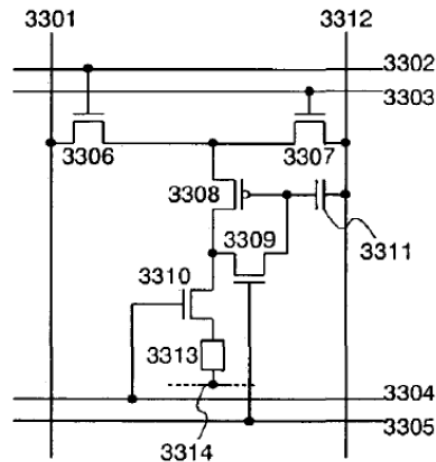


Pet. (Paper 1), 19 (citing EX1002 (Kimura), Fig. 33B, 36B)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE PDX-63

## Kimura Renders Obvious the “Initialization” Claims

Fig.33A



[0658] Further, the TFT 3310 can also be used as an erasure TFT when applying a driving method that uses a digital time gray scale method. In addition, the erasure TFT can be placed in any location, provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing.

# Dr. Wolfe Confirms the Erase Transistor Discharges the Capacitor



14 Q So Kimura Figure 36 has one additional  
15 transistor relative to Kimura Figure 33, correct?

16 A **Yes, the erase transistor.**

17 Q And is that transistor 3612 that you're  
18 referring to?

19 A **Yes.**

20 Q And what did you call transistor 3612?

21 A **The erase transistor. I believe that's**  
22 **correct.**

6 Q Okay. Very good. So let's go back to  
7 Kimura Figure 36. So with the understanding that we  
8 just discussed that the line 3617 is the -- oops, I  
9 lost it -- is the electric power source line, would  
10 you agree that in Figures 36B, that current is  
11 flowing off of the capacitor through the transistor  
12 3612 to the line 3617?

13 MR. GARR: Objection.

14 THE WITNESS: I think that's the  
15 typical case that they are trying to  
16 illustrate.

Fig.36A

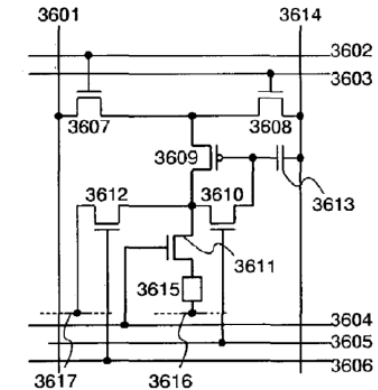
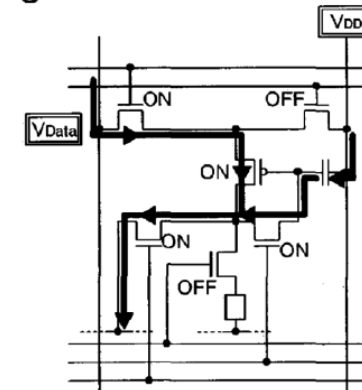


Fig.36B



## Dr. Wolfe Admits Fig. 36B is the “Erase Phase”



18 Q What is the state of the transistor at  
19 3612 in Kimura Figures 36C, D and E?

20 A It is turned off.

21 Q So the only time that the transistor 3612  
22 is shown as being turned on is in Kimura Figure 36B?

1 A Yes, to illustrate the erase phase.

Fig.36A

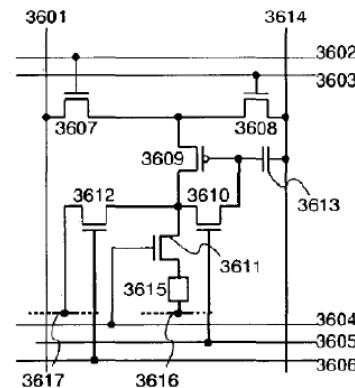
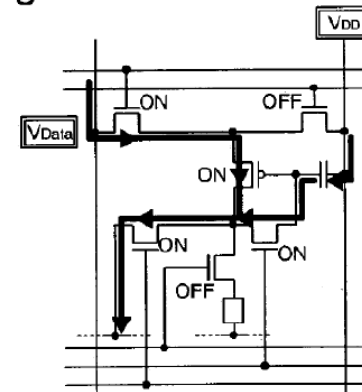


Fig.36B



# Kimura Renders Obvious the “Initialization” Claims

Fig.17A

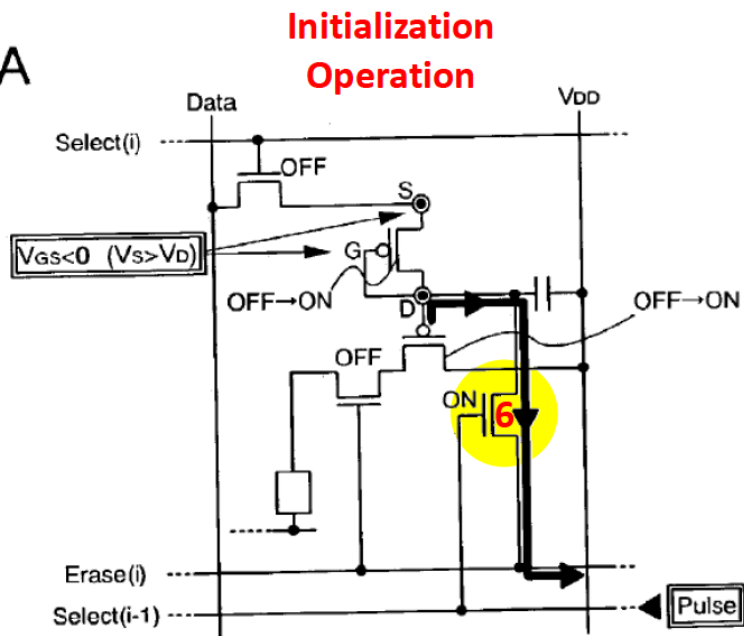
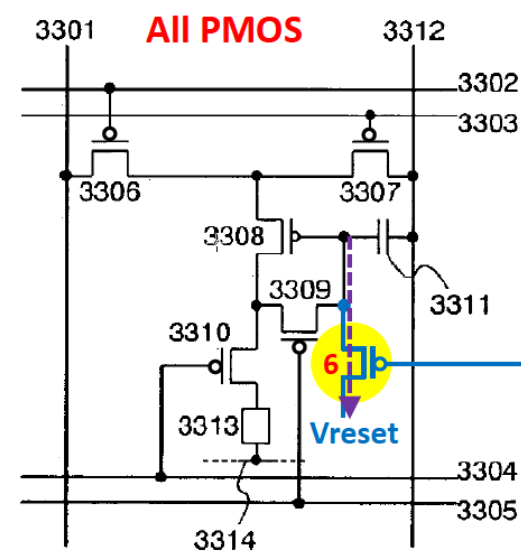


Fig.33A



# It Makes No Difference Whether “Fig. 33” or “Fig. 36” is Modified

EX1002, [0658]). The modified version of Fig. 36A below is identical to Fig. 33A with a reset/initialization transistor, as shown in my Original Declaration (¶¶223, 228).

Fig.36A All PMOS

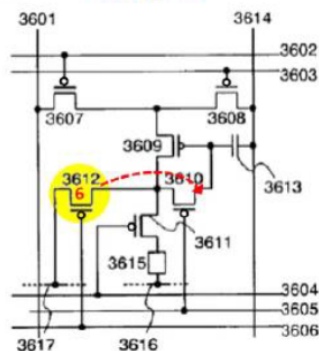


Fig.36A All PMOS

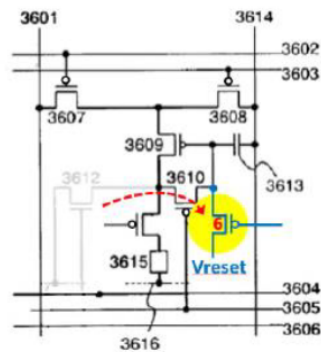
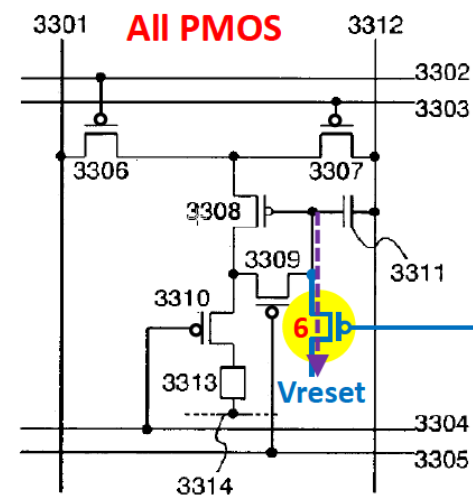
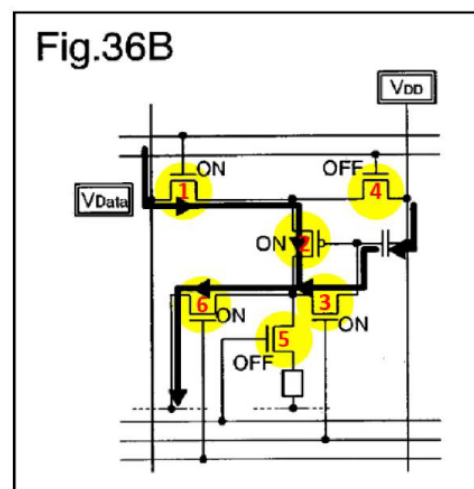
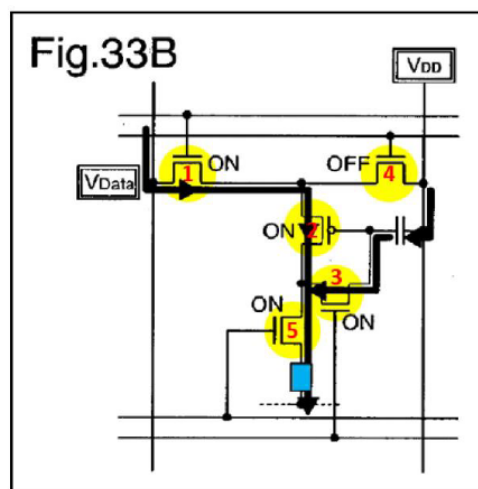


Fig.33A



# It Makes No Difference Whether “Fig. 33” or “Fig. 36” is Modified

One way Kimura solves this problem is adding a dedicated initialization transistor (labelled sixth transistor) as shown in Fig. 36B below where, during initialization, the capacitor discharges through the sixth transistor instead of the light emitting element. EX1002, [0666]-[0667] (“A [sixth transistor] is therefore added as shown in FIG. 36[]...Light emission by the EL device during unnecessary periods can thus be prevented.”). As reflected in Figs. 33 and 36, initialization is



Pet. (Paper 1), 19 (citing EX1002 (Kimura), Fig. 33B, 36B)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE PDX-69

# Many Other Reasons for the Proposed Modification

- Extensive discussion of the dedicated initialization transistor approach in Figs. 16-17, including detailed control signal/timing waveforms. *See* Kimura [0420]-[0430]; EX1003, ¶¶141-143.
- The simplicity of the solution and ease of implementation (*viz.*, no other transistors or circuit elements require changing) creates a reasonable expectation of success. EX1003, ¶229. And Kimura Fig. 36 (discussed *infra*) confirms this by showing a similar modification vis-à-vis initialization transistor 3612 (placed in another location).
- Kimura's express teachings about the flexible location of the transistor and the fact that adding a dedicated initialization transistor solves a known drawback in Fig. 33 (*i.e.*, spurious light emission during initialization). EX1002, [0658] and [0666].
- Initializing/resetting circuits (including OLED drivers) was a common and well-known practice at the relevant time. EX1003, ¶155. While other initialization protocols were available (discussed elsewhere in Kimura), selecting one was a mere design choice and there were limited options/locations for initialization transistor placement. EX1003, ¶158.
- Adding the initialization transistor as described in Fig. 16-17 does not require any additional control signals. *See* EX1002, [0422] (only two total control signals needed for pixel circuit); *id.*, [0429] (“[T]o perform initialization of a certain row, it utilizes the selection pulse of the gate signal line of the previous row in controlling the [sixth transistor]...The number of signal lines can be kept to a minimum.”).

# PO's "Erasure" Argument

**1. Petitioner's rationale for adding an "initialization transistor" to Kimura Figure 33 hinges on its misunderstanding of "erasure."**

As the Board noted, the Petition's theory for the "initialization transistor" claims is premised on a fundamental technical flaw, stemming from Petitioner's error in portraying "erasure" in Kimura as being synonymous with "initialization." *See* ID at 47–48 ("The record evidence does not support Petitioner's assertion that the fifth transistor, when used as an erasure transistor, resets the capacitor voltage to a default initialization value."). In Kimura, "erasure" means "forcibly plac[ing] [the EL device] in a non-light-emitting state." Kimura at ¶410. And an "erasure TFT" is a transistor that permits "electric current supplied to the EL device [to] be cut off at an arbitrary timing." Kimura at ¶658. Kimura does not use "erasure" to refer to "reset[ting] the capacitor voltage to a default initialization value" (i.e., initialization) as Petitioner mistakenly asserts. Pet. at 18; Ex. 2008, ¶84.

# Dr. Wolfe Confirms Identity of the Erase Transistor

Fig.36A

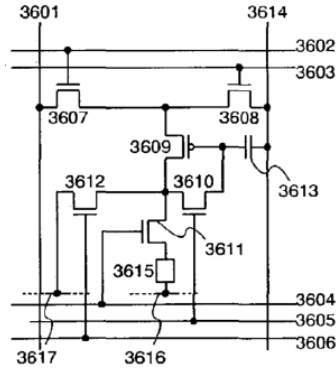
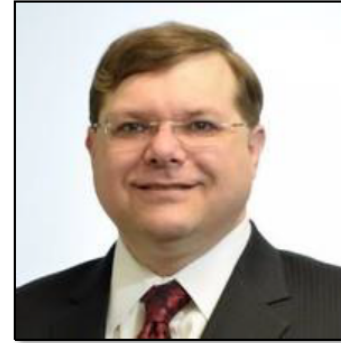
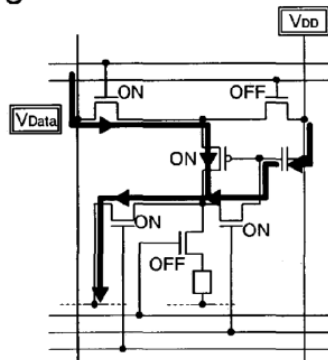


Fig.36B



14 Q So Kimura Figure 36 has one additional  
15 transistor relative to Kimura Figure 33, correct?

16 A **Yes, the erase transistor.**

17 Q And is that transistor 3612 that you're  
18 referring to?

19 A Yes.

20 Q And what did you call transistor 3612?

21 A **The erase transistor. I believe that's**  
22 correct.

## TFT 3611, Not TFT3612, Cuts Off Current Flow

Fig.36A

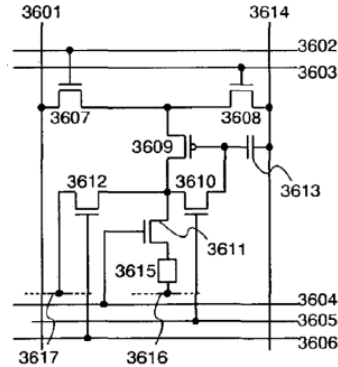
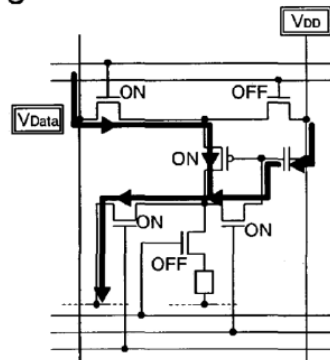


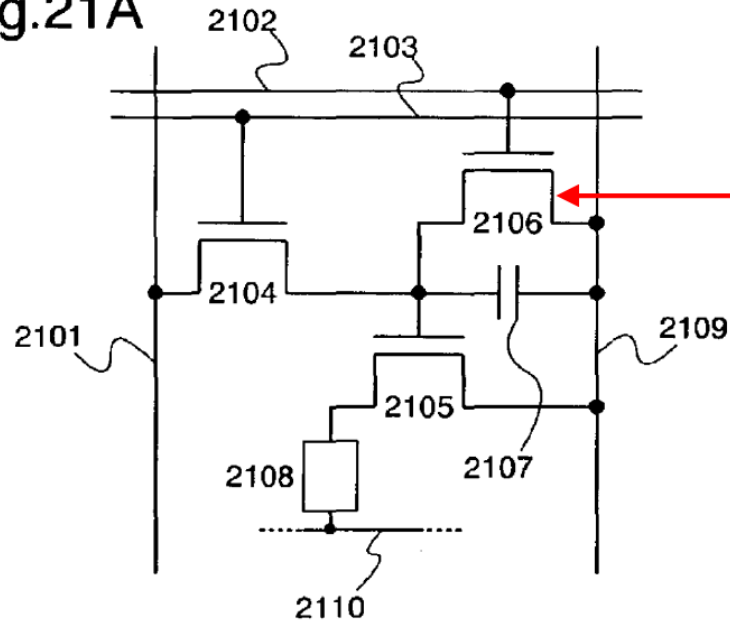
Fig.36B



[0666] A TFT 3612 is therefore added as shown in FIG. 36A. Electric current flowing in the TFT 3609 during input of the image signal flows through the TFT 3612 and to an electric power source line 3617. An electric current path to the EL device 3615 is cut off by a TFT 3611, and therefore the EL device 3615 does not emit light. Light emission by the EL device during unnecessary periods can thus be prevented by using this type of structure.

## Kimura Fig. 21 Supports Obviousness

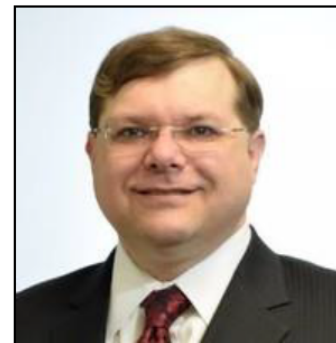
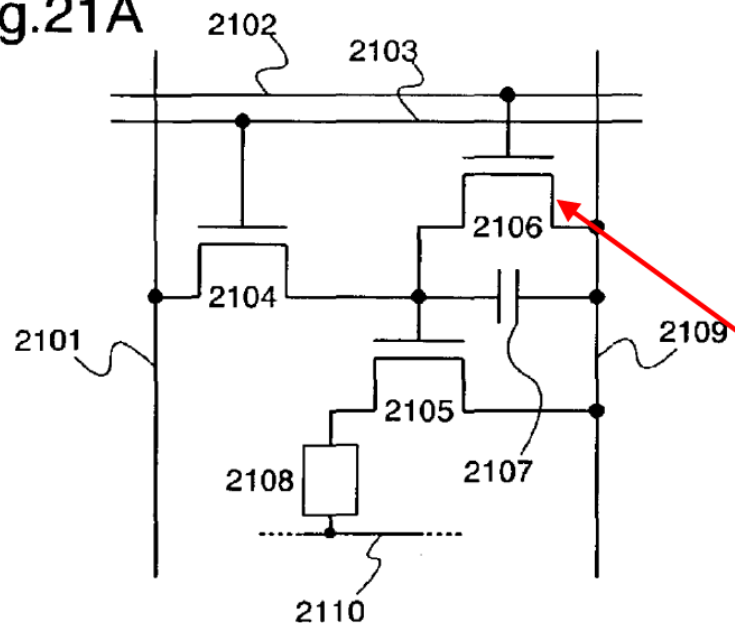
Fig.21A



[0404] The structure of a pixel of a semiconductor device for a case of using a method in which a digital gray scale method and a time gray scale method are combined is shown in **FIG. 21A**. It becomes possible to finely control the length of a light emitting period by using an erasure TFT **2106** in addition to a switching TFT **2104** and a driver TFT **2105**.

## Dr. Wolfe Admits PO is Wrong About the “Erase” TFT

Fig.21A



11 Q And did I hear you correctly to say that  
12 the purpose of transistor 2106 is to discharge the  
13 capacitor 2107?

14 A 2106 is described as an erasure TFT, and  
15 I believe that its role is to discharge the  
16 capacitor.

# The “Erase” TFT Need Not Cutoff Current to the LED

by TFT 3310 (Fig. 33) or TFT 3611 (Fig. 36). Regardless, Kimura shows Samsung is wrong that the “erasure” transistor must be “along the current path to the [LED]” (POR, 32). For example, “erasure” TFTs 914 and 2106 in Kimura Figs. 9 and 21 respectively, are plainly not in the LED current path. See Kimura, [0407], [404].<sup>12</sup>

Fig.9A

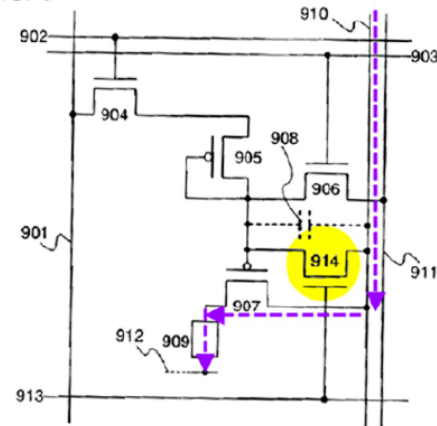
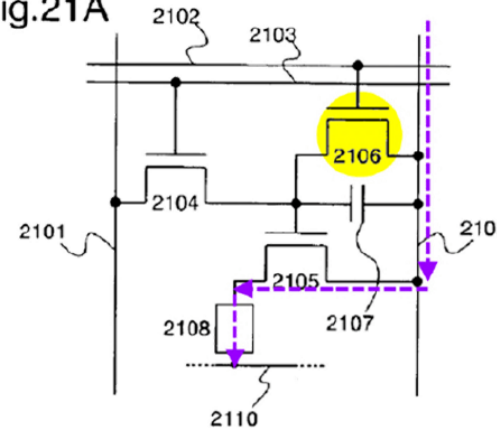


Fig.21A



## The “Initialization” Claims

8. The pixel circuit in the organic light emitting device of claim 7, further comprising:

a sixth initialization transistor for discharging the data signal voltage stored in the capacitor in response to a scan signal just before the current scan signal upon initialization.

16. The pixel circuit in the organic light emitting device of claim 15, further comprising:

a sixth transistor including a gate to which a scan signal just before the current scan signal is applied;  
a source coupled to the one terminal of the capacitor; and  
a drain to which an initialization voltage is applied.

# PO's "Erasure" Argument

**1. Petitioner's rationale for adding an "initialization transistor" to Kimura Figure 33 hinges on its misunderstanding of "erasure."**

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# Kimura Need Not Use the Same Words as the '599 Patent

We acknowledge Kuhno discusses these concepts in different terms and with different points of emphasis than the '967 patent. But the district court erred in interpreting these linguistic differences as fatal to a finding of anticipation. "The invention is not the language of the [claim] but the subject matter thereby defined." *Dow Chem. Co. v. Astro-Valcour, Inc.*, 267 F.3d 1334, 1341 (Fed. Cir. 2001). Thus, a prior art inventor need not "conceive of its invention using the same words as the patentee would later use to claim it." *Teva Pharm. Indus. Ltd. v. AstraZeneca Pharms. LP*, 661 F.3d 1378, 1384 (Fed. Cir. 2011). These disclosures

*ADASA Inc. v. Avery Dennison Corp.*, 55 F.4th 900, 913 (Fed. Cir. 2022)



## Dr. Wolfe Admits Fig. 36B is the “Erase Phase”



18 Q What is the state of the transistor at  
19 3612 in Kimura Figures 36C, D and E?

20 A It is turned off.

21 Q So the only time that the transistor 3612  
22 is shown as being turned on is in Kimura Figure 36B?

1 A Yes, to illustrate the erase phase.

Fig.36A

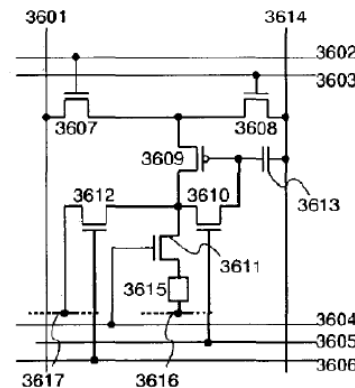
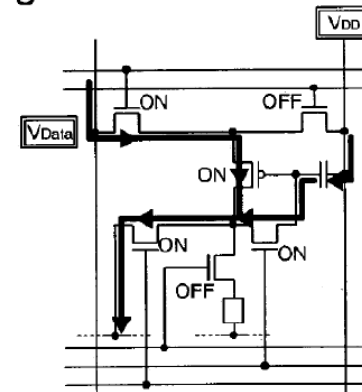
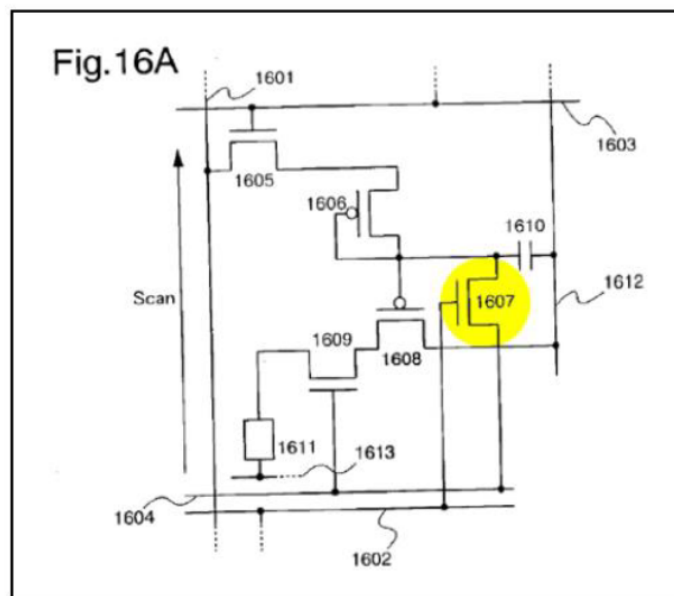


Fig.36B



## Kimura Fig. 16/17 Plainly Discloses “Initialization”



[0425] With the electric potential of the source signal line 1601 taken as VDD, the electric potential of the electric current supply line taken as VDD, and the electric potential when a gate signal line is L level taken as VReset ( $<VDD - |V_{th}|$ ), a gate Q a source (S), a drain D of the TFT 1606 are defined as shown in FIG. 17A.

EX1002 (Kimura), [0425]

it is necessary for the second gate signal line of the i-th row to be L level when the TFT 1607 is on and initialization is performed, and that it is necessary for the TFT 1609 to be off at this time.

EX1002 (Kimura), [0424]

TFT 1608 drops as shown in FIG. 17A. The electric potential of the gate electrode of the TFT 1608 is thus initialized.

EX1002 (Kimura), [0426]

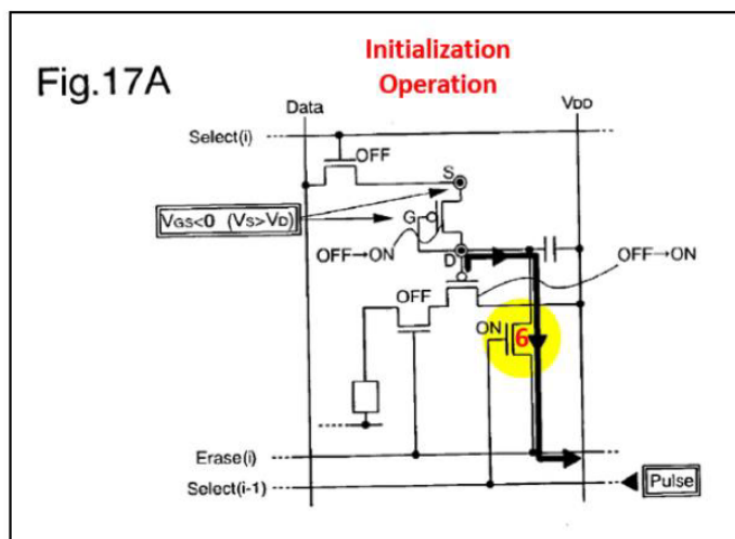
becomes ( $\tilde{V}_{Data} - V_{th}$ ). Initialization is performed at this point in an (i+1)th row, similar to that discussed above (FIG. 17B).

EX1002 (Kimura), [0427]

[0429] Embodiment Mode 4 is characterized in that in order to perform initialization of a certain row, it utilizes the selection pulse of the gate signal line of the previous row in controlling the TFT 1607, and that it utilizes non-selected

EX1002 (Kimura), [0429]

## Dr. Wolfe Admits Kimura Fig. 16/17 Discloses “Initialization”



3 Q Do you know the purpose of the VReset  
4 voltage in Figure 17A?

5 A I believe it's intended to initialize the  
6 voltage on the capacitor prior to programming.

7 Q Do you know why Kimura calls that voltage  
8 VReset?

9 A No.

10 Q Is it because --

11 A I mean, it's also called erase sub i, and  
12 it has other names.

## PO's Definition of Erasure is Incorrect

If Samsung contends Figs. 33/36 must maintain “erasure” capability as Samsung defines it (*i.e.*, cutting off LED at any time), that is already accomplished by TFT 3310 (Fig. 33) or TFT 3611 (Fig. 36). Regardless, Kimura shows Samsung is wrong that the “erasure” transistor must be “along the current path to the [LED]” (POR, 32). For example, “erasure” TFTs 914 and 2106 in Kimura Figs. 9 and 21 respectively, are plainly not in the LED current path. *See* Kimura, [0407], [404].<sup>12</sup>

## PO's Erasure/Initialization Distinction Misses the Point

*First*, by arguing that “erasure” and “initialization” are “separate and distinct operations,” (POR, 27), Samsung wishes to draw the inference that those functions are necessarily performed by “separate and distinct” transistors. That is plainly not the case—Fig. 33B shows the capacitor discharging through “erasure” TFT 3310 (circled in red). *See* EX1028, 203:2-22, 205:15-206:2.

## PO's "Extra" Signal Line Argument is Wrong

Samsung makes one secondary argument, asserting that “the Petition’s proposed modification would also require adding at least one additional signal line connected to the drain of the [reset/initialization transistor].” POR, 33-34. Not so. *See* Pet., 79; EX1003, ¶321. As Dr. Foty’s original declaration explained, “[t]he actual voltage used for VReset is simply a design choice for the circuit designer” and that “[one] obvious option is disclosed in connection with Kimura Figures 16 and 17 where the drain of the reset transistor is connected to the light emitting signal (i.e., the second gate signal labeled 1604).” EX1003, ¶321. By using an

## The Board's Supplemental Evidence Ruling

*Id.* Although this content of the proposed supplemental declaration of Dr. Foty (Ex. 1019 ¶¶ 25–34) does not change the theory or arguments in the Petition or the first declaration of Dr. Foty, the problem lies in paragraphs 35 and 36 of the proposed supplemental declaration of Dr. Foty, reproduced in

## The Board's Supplemental Evidence Ruling

Petitioner may not now divorce itself from its original reliance on the use of the fifth transistor in Figure 33 as an erasure transistor to account, at least in part, for the initialization transistor of claim 8, and switch to sole reliance on Kimura's disclosure of initialization/reset transistor 1607 in Kimura's Figures 16 and 17. This change is significant, and substantially alters, if not completely eliminates, Petitioner's initial reasoning to use transistor 1607 in Kimura's Figures 16 and 17. *See* Pet. 51–56.

## The Reply Maintains that Kimura [0658] Supports its Position

84. In my original Declaration (¶¶221, 228), I cited Kimura [0658] – as indicating that the “erasure TFT” need not be located where the Figure 33 embodiment places it, as transistor 3310 is located where it has two jobs (during the initialization period and emitting period as explained in ¶¶133 and 139 of my Original Declaration). Kimura teaches that the erasure transistor can be placed elsewhere (as Kimura does in the Figure 36 embodiment). However, Patent Owner misinterprets the statement that “provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing” – as stating that the “erasure transistor” must be the actor that is cutting off the electrical current to the emitter.

[0658] Further, the TFT 3310 can also be used as an erasure TFT when applying a driving method that uses a digital time gray scale method. In addition, the erasure TFT can be placed in any location, provided that it is a location at which electric current supplied to the EL device can be cut off at an arbitrary timing.