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Packaging Challenges for the Next Generation of Mobile Devices

October 10, 2017

Ahmer Syed
Sr Director, Package Engineering
Qualcomm Technologies, Inc.

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Smartphone Trends

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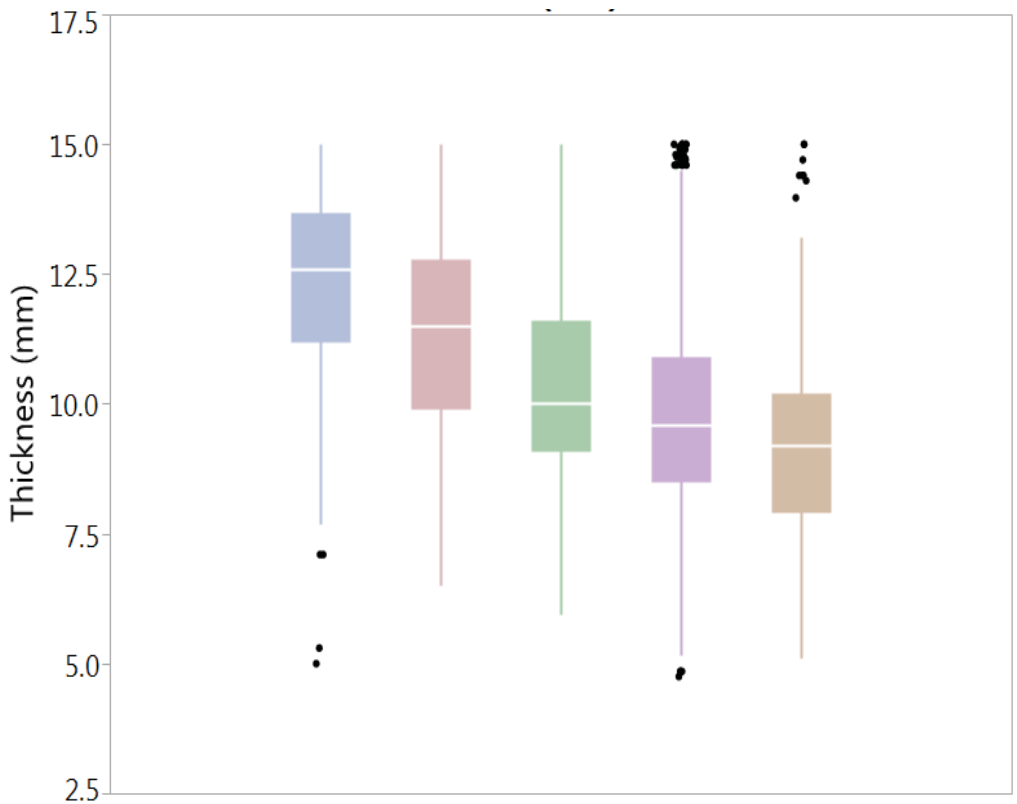
Smartphone Trends

Phone thickness has reduced significantly



Source Data for Analysis: SpecTrax Database from 2011 to mid-2015 (N=7881)

Continuous trend for thinner phones

Thinner Package
Thinner Board

Device Thickness vs. Year for all for 7881 portable electronic devices (display sizes ranging from 0.68" to 27")

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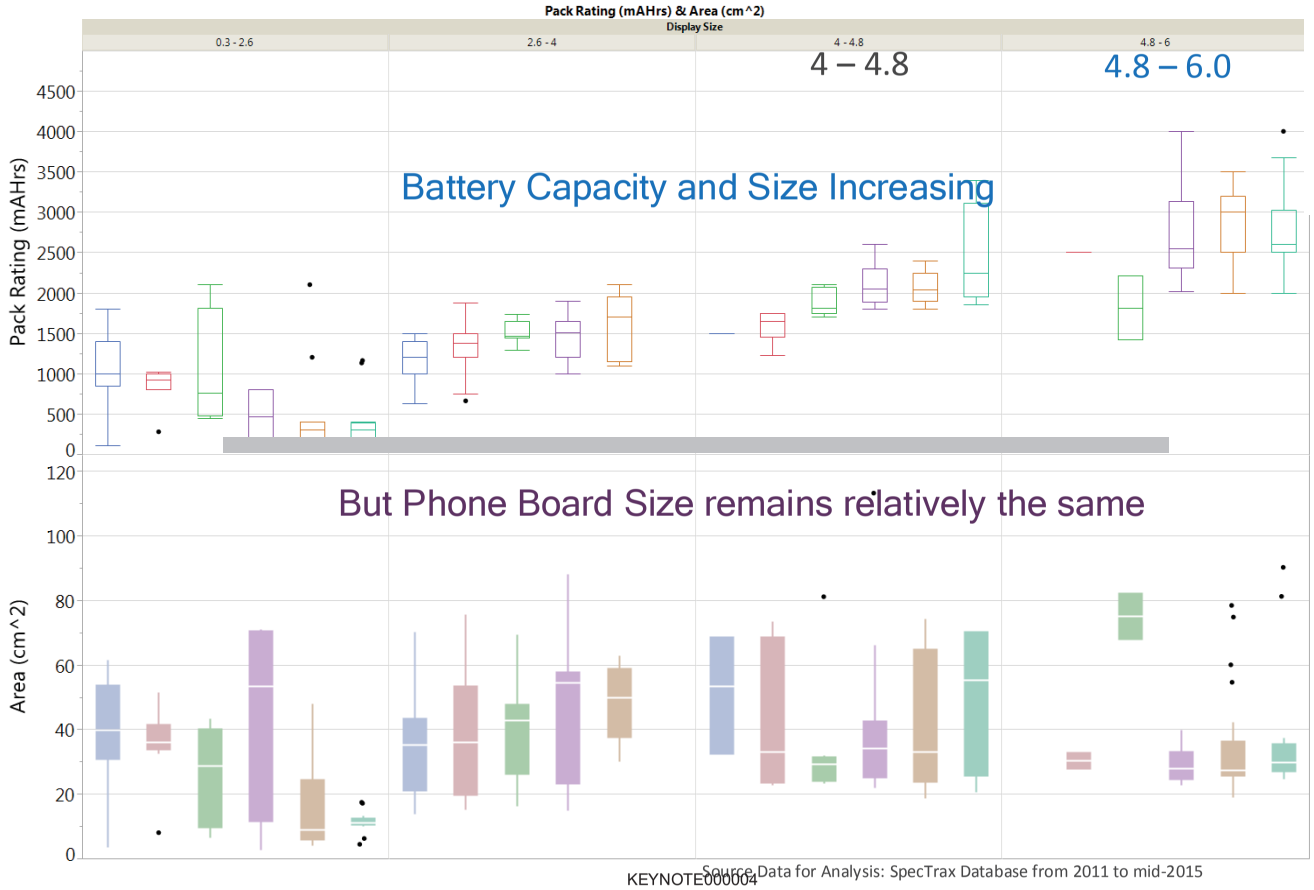
Smartphone Trends

Requirement for Longer Battery Life is Driving Battery Size

Battery Capacity

Board Size



Source Data for Analysis: SpecTrax Database from 2011 to mid-2015

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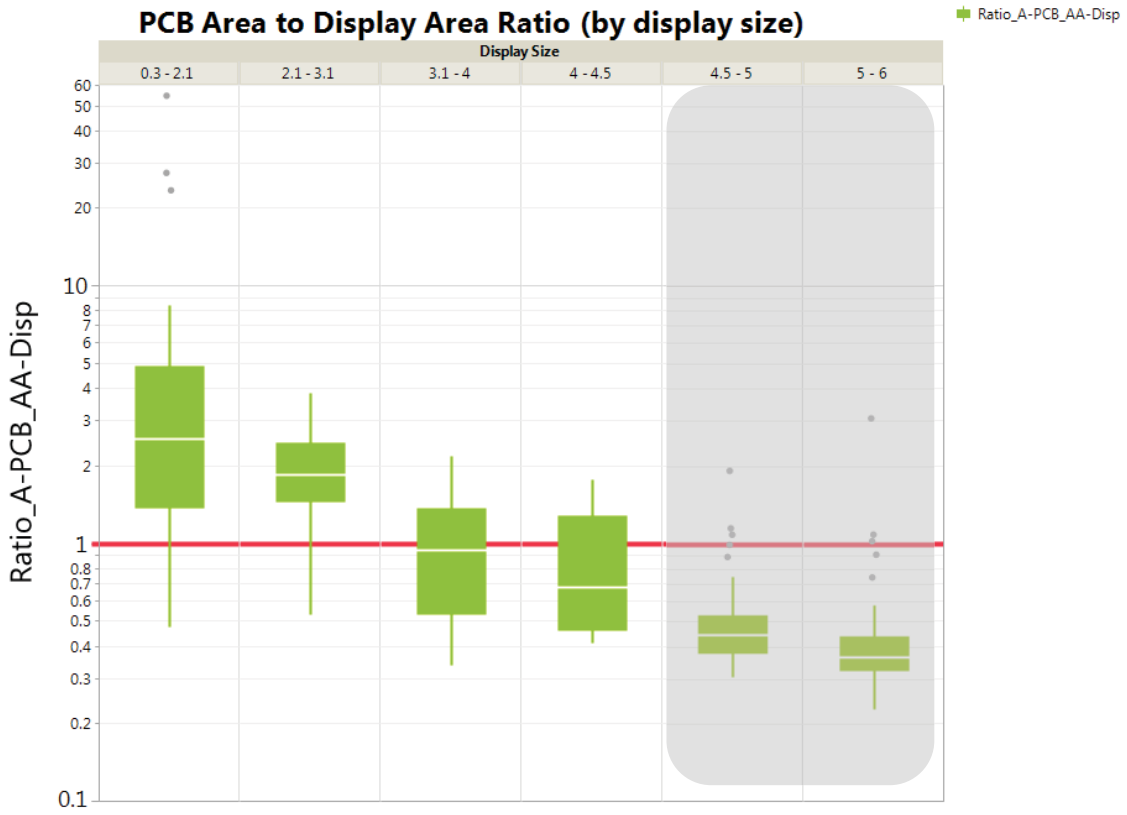
Smartphone Trends

Relatively Smaller Boards for larger displays



Source Data for Analysis: SpecTrax Database from 2011 to mid-2015 (N=7881)
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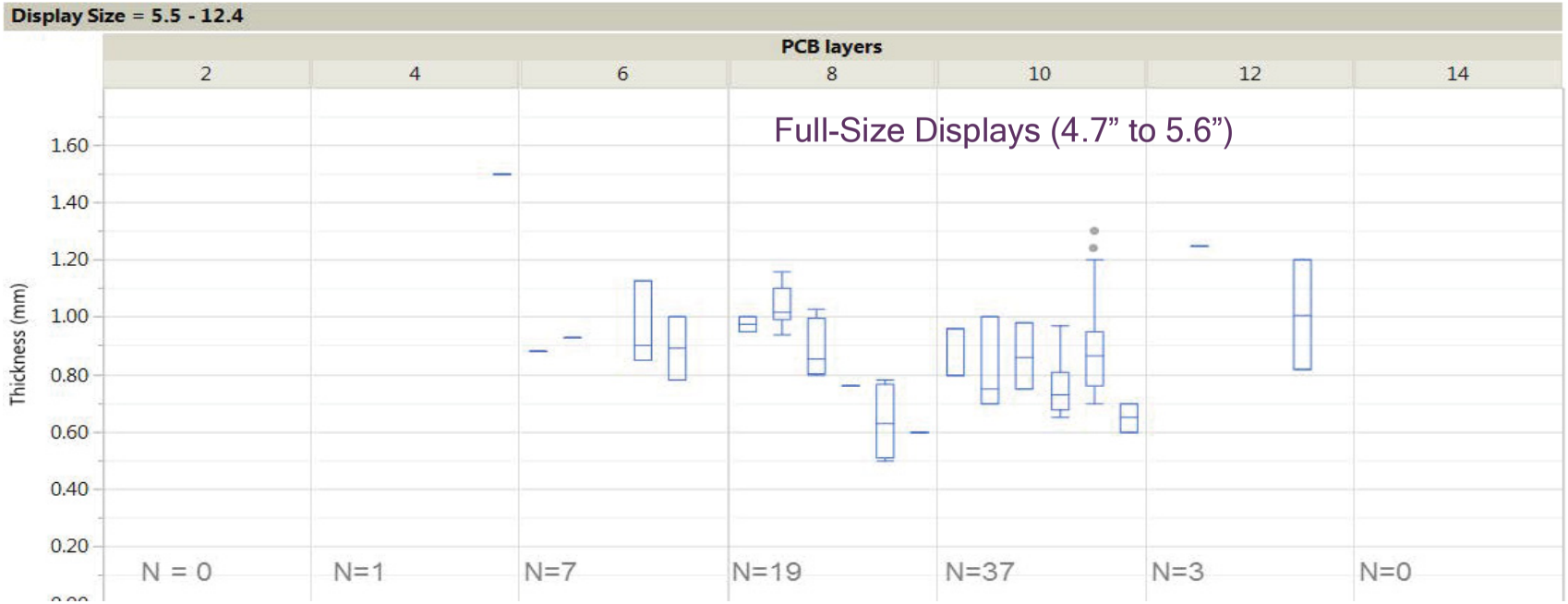
Smartphone Trends

Board Thickness and Layer Count



Source Data for Analysis: SpecTrax Database from 2011 to mid-2015

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Packaging Trends

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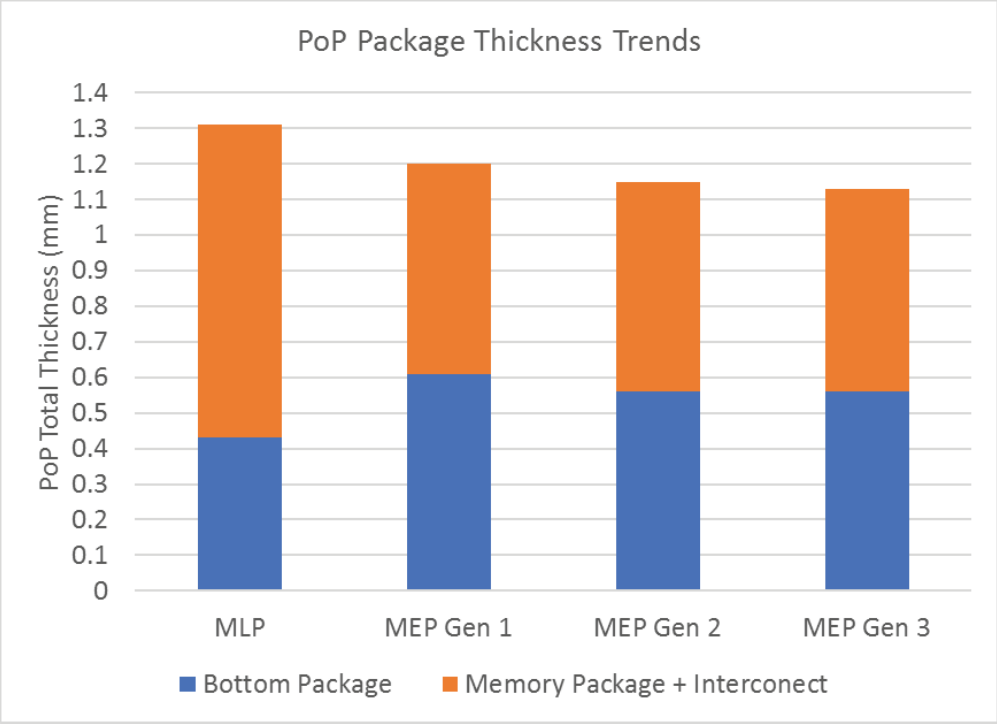
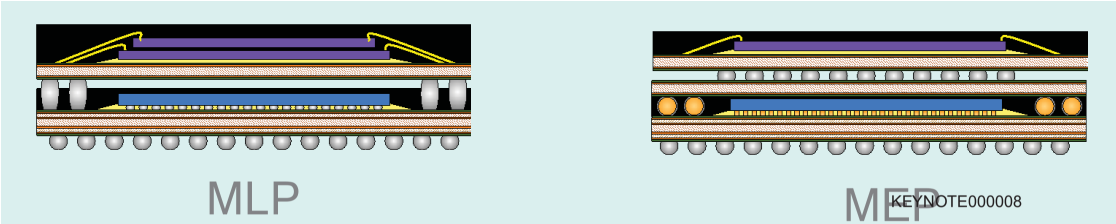
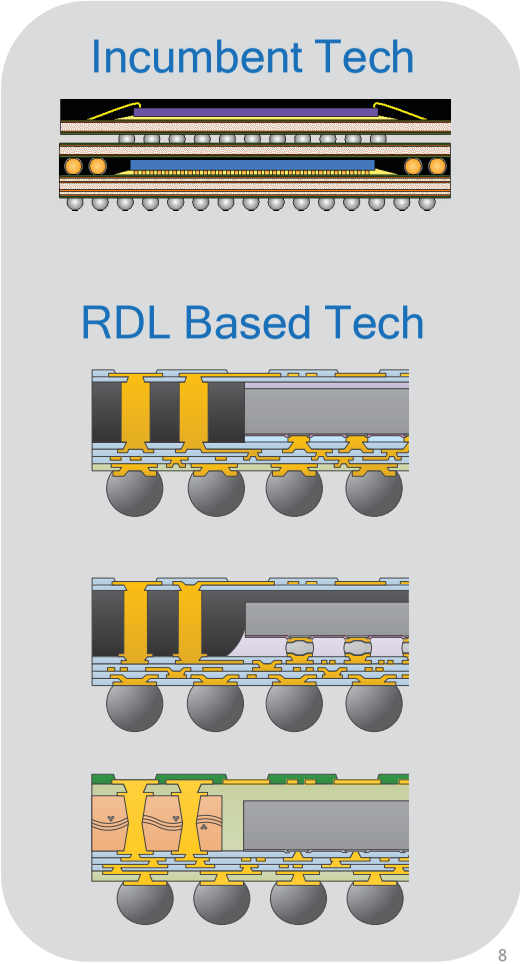
Package z-height by PoP Gen







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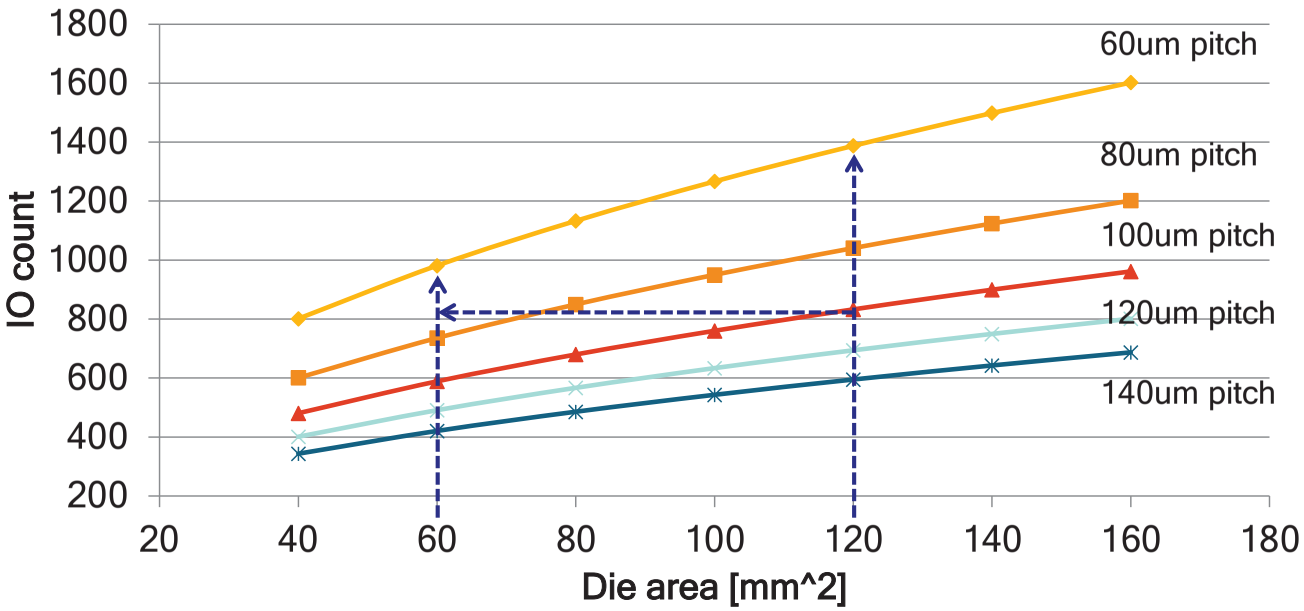
Drives for Bump Pitch Reduction

- More demanding mobile SoC device performance requires higher I/O counts
- Shrinking die size for advance silicon nodes requires fine bump pitch
- Cu pillar bump is a must for fine pitch application, continuously smaller UBM due to pitch shrink



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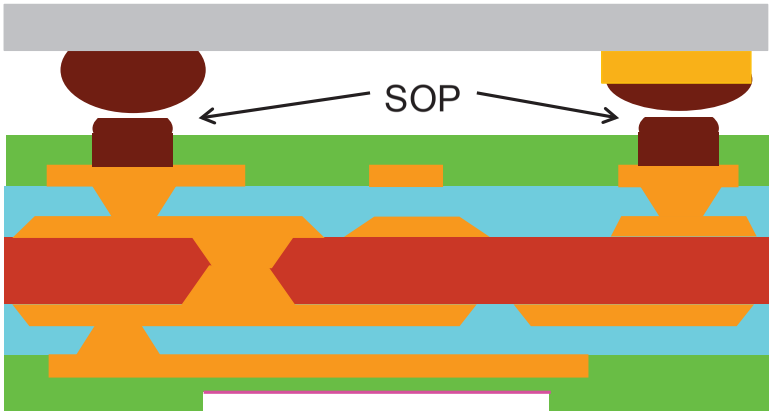
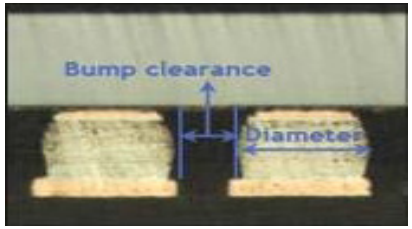
Fine Pitch Flip Chip Interconnect Trends

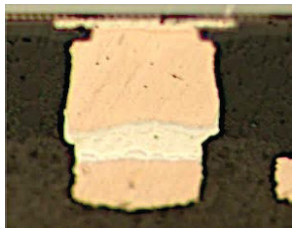
FC Interconnect using SOP

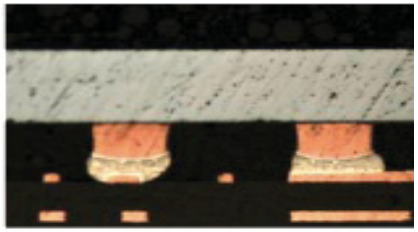


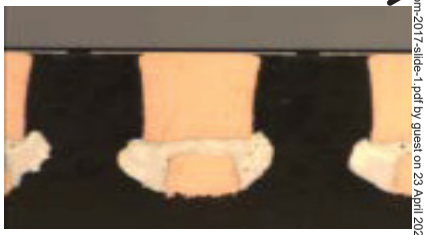
Fine Pitch FC used in mobile devices

Mass Reflow (MR) FC (≥140 um) | CuBOL/ETS (≥100 um) | CuBOL(≥100 um) | TCFC (≤80 um)









- Conventional solder bump flip chip

- Substrate uses narrow bond leads instead of flip chip pads, and die uses Cu pillars w/ SnAg solder cap
  - CuBOL: Cu pillar bond on lead mass reflow chip attach
  - TCFC: thermo-compression flip chip attach
  - CuBOL/ETS - coreless embedded trace substrate with BOL interconnect
  - Capillary and molded underfills are used

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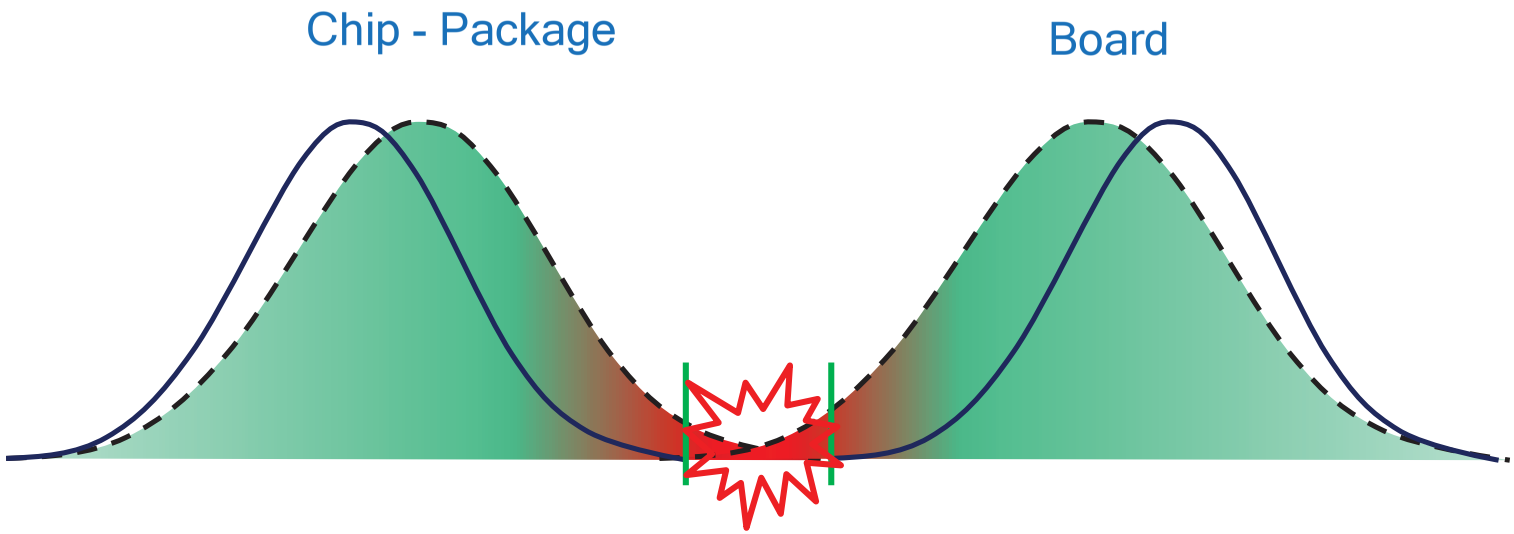
Chip-Package-Board Interaction



- Die package area ratio
- Tighter I/O pitch =>Smaller bumps
- Thinner substrates and Packages >> Higher warpage
- Fab Nodes / Assembly Processes

- Thinner board with higher layer count
- Increased CTE and Stiffness
- Denser boards with double-sided assembly
- SMT Process variations

Stress to Strength Margins are significantly reduced resulting in increased risk of failures

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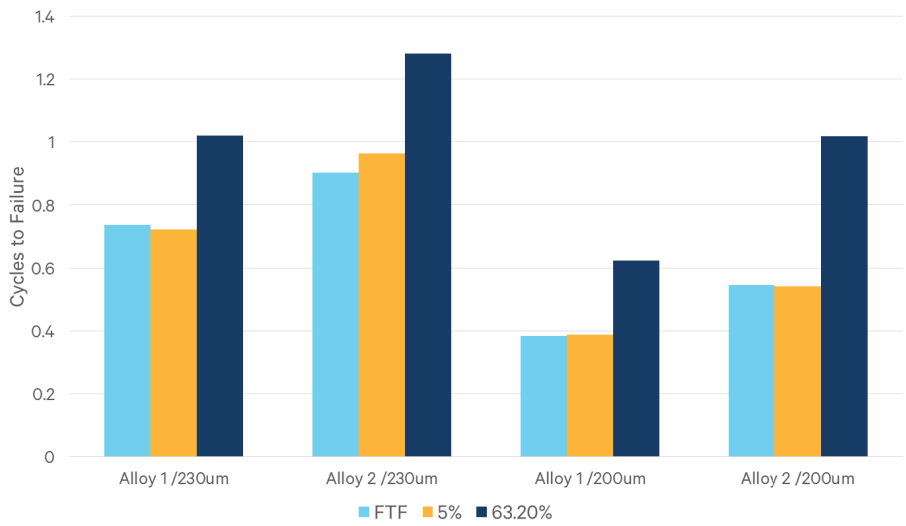
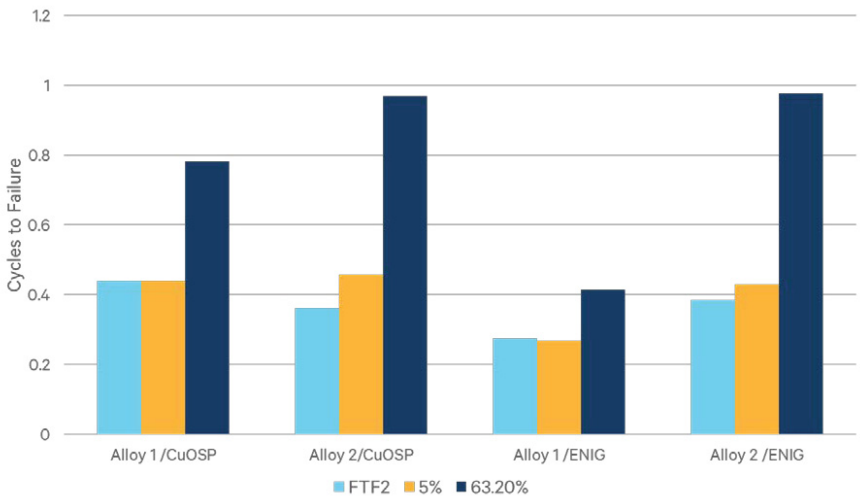
Board Level Reliability Challenges

- WLCSP – Solder ball alloy, Ball Size, and Board Finish
  - Smaller balls > lower reliability
  - ENIG board finish > lower reliability
  - New solder ball alloys needed to improve reliability for smaller balls, larger die, and ENIG board finish



CuOSP Board Finish



230um Ball

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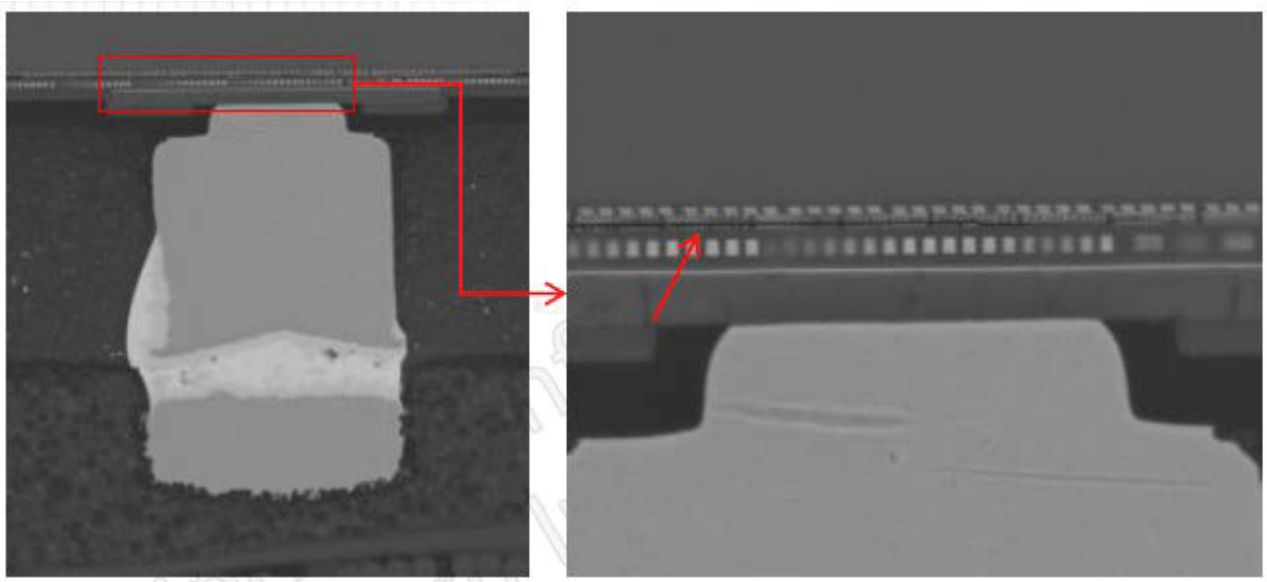
Low K Stress and Delam

- Stress from Si and package substrate CTE Mismatch
- Si node scaling -> low K dielectric -> More porosity -> weak mechanical strength -> susceptible for delamination
- Bump pitch reduction -> Less compliant Cu pillars, smaller UBM



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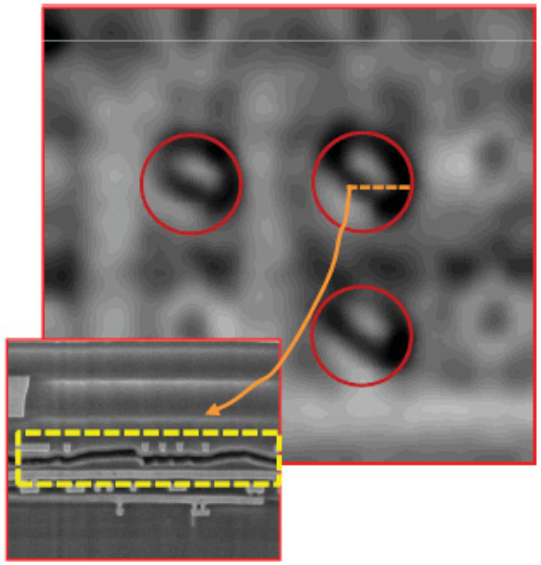
CPI Simulations

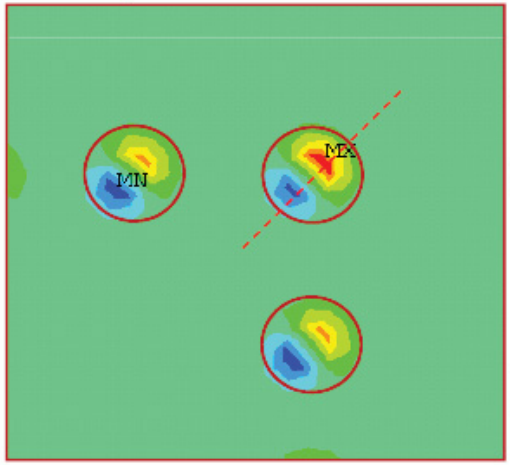
SAT image & FEA Tensile Stress Contour Comparison

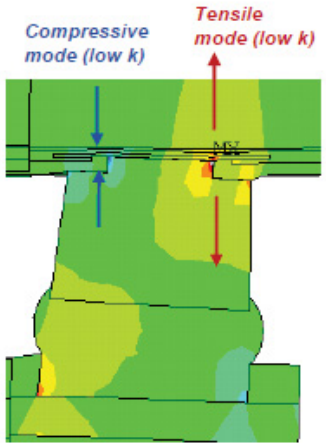
- Half Moon Type low k layer damage shows that the failure mode is governed by the tensile (peeling) stress near the Al to Cu pillar interfacial shoulder

White bump by SAT
(low k damage) at die corner



Simulated Max Tensile stress
of low k layer
after chip attach at die corner





Courtesy: Amkor

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Technical Challenges for Mobile Applications

Materials and Processes
- Low K and Lower K dielectrics
- Fine pitch Cu Pillars/uBumps (<100um pitch)
- Low CTE, High Modulus Substrate Materials
- High CTE Mold Materials

Warpage/Stress/Reliability
- Ultra thin die (<150um)
- Warpage Control
- CTE mismatch and CPI, eCPI
- Thermomechanical and drop Reliability

Thermal Challenges
- Tj and skin T
- Poor thermal paths
- No air flow, Closed system
- 3D integration

Electrical Challenges
- Signal Integrity
- Functional Partitioning
- Power Distribution Network

While meeting Cost and Quality Targets

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Overcoming Packaging Challenges

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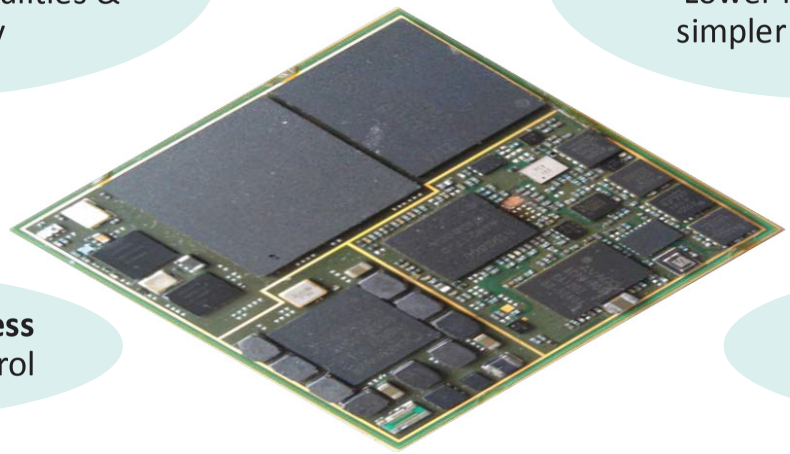
Overcoming Packaging Challenges

Form-Factor Reduction
Free-up more space for adding more functionalities & bigger battery

Lower Complexity for Customer
Lower layer count & simpler board design



Manage Board Level Stress
Materials & process control

Simplified Supply Chain

Better Thermal Performance
Optimized Heat distribution and conduction path

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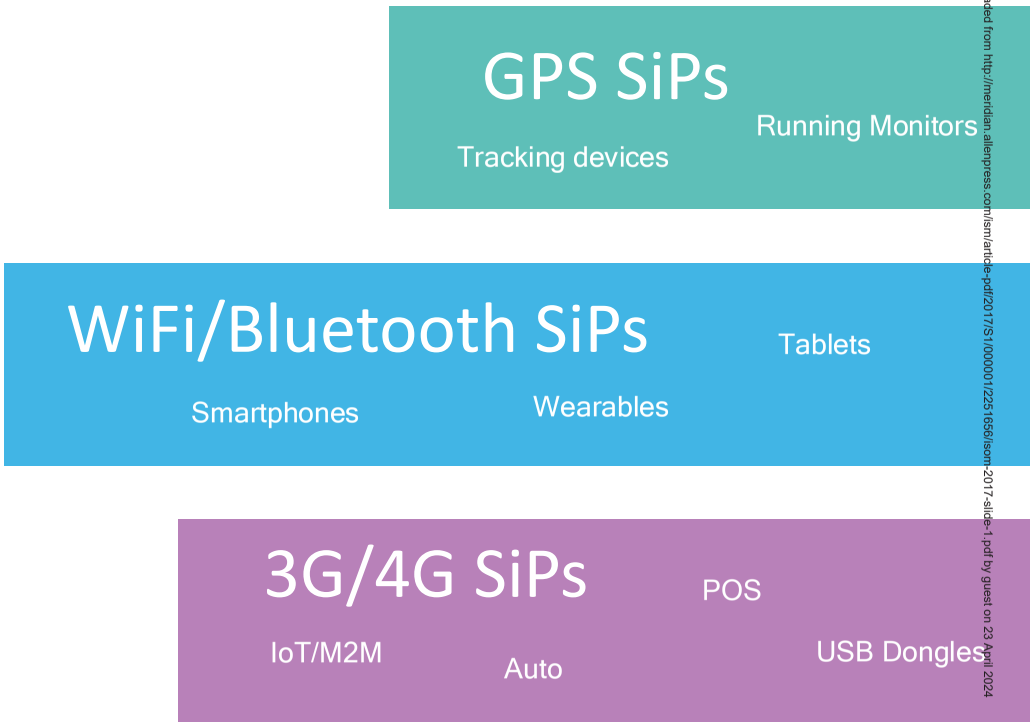
Current SiPs Commercially Available

Most SiPs are sub-systems for mobile devices

- SiP consists of
  - Bare IC die
  - Packaged IC die (2D/3D)
  - SMT active and passive components
  - Integrated passive devices (IPD)
  - Embedded components
  - Performance enhancements
    - Thermal lids
    - Shielding
    - Stiffeners



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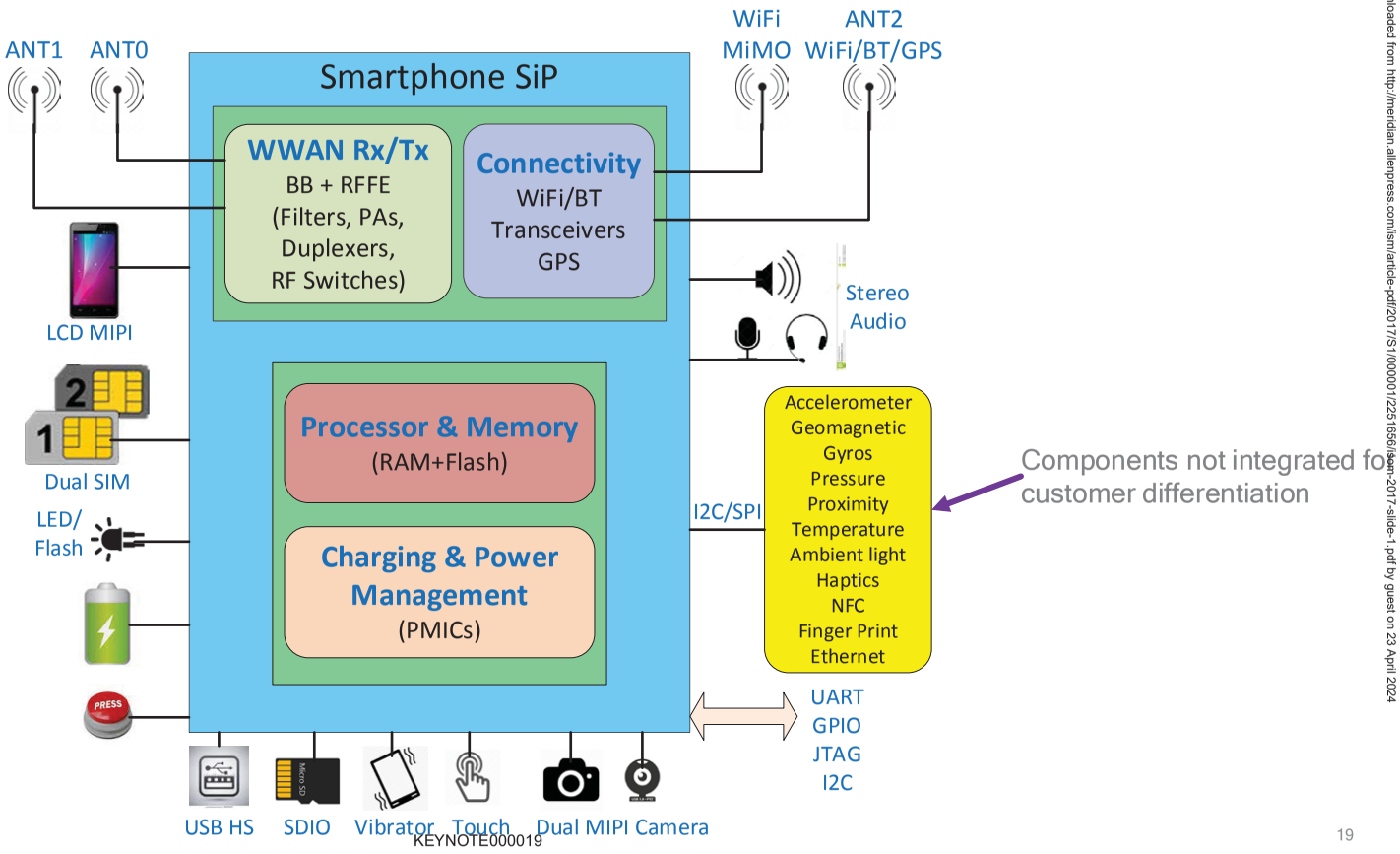
SiP with Complete Mobile System

A Genuine Mobile SiP!



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SIP Benefit for Customers

Simplified Supply Chain

- No large design team and multiple board turns required to design a phone
- No longer need to manage hundreds of suppliers

Help OEMs reduce time-to-market and cost

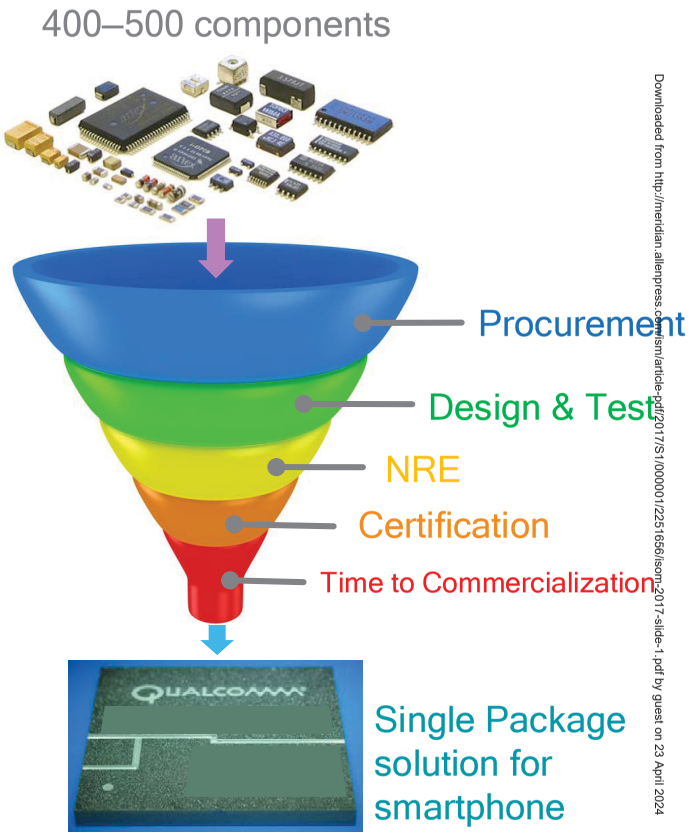
- Comprehensive solution to simplify process of designing, building, and manufacturing
- Reduce phone PCB layer count and burden for system designers

Reduce upfront investment and operating cost

- Simplify complexities of wireless device design and tests
- Flexibility to focus on customization and differentiation

Attractive business model

- Small form factor S-SIP to allow ID design flexibility
- Pre-tested and Pre-certification for cost effective ownership



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SiP Advantages

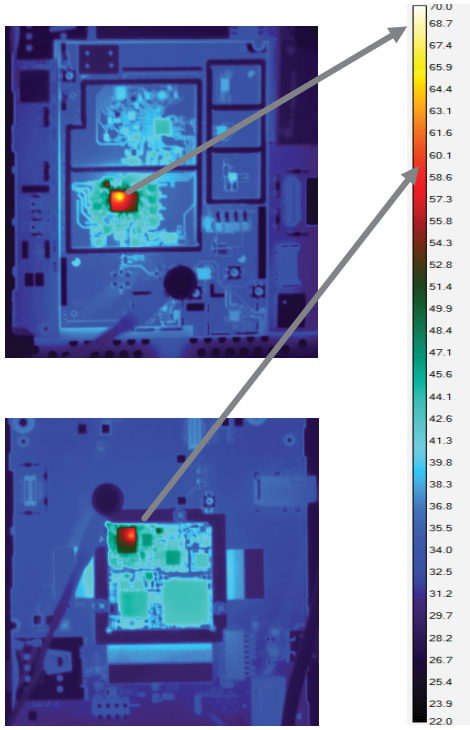
Thermal and Mechanical Performance

System Thermal

Conventional Phone with discrete chips

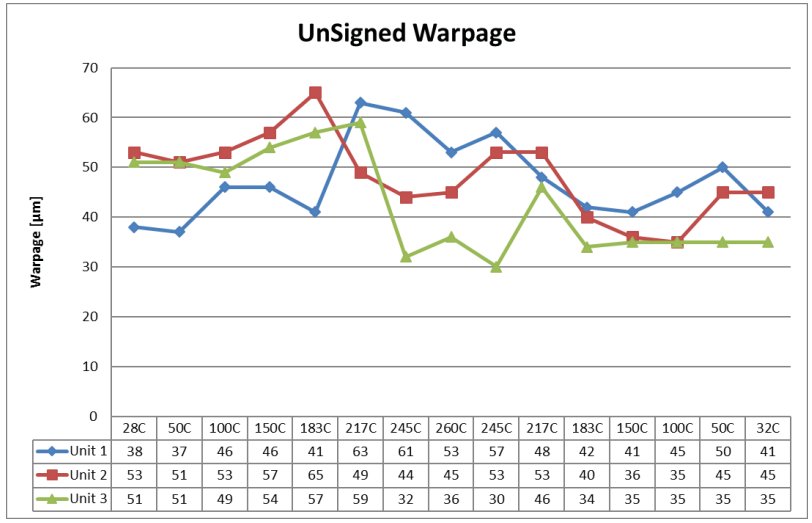
10 C Lower Hot Spot

Phone with SiP (25x25mm)



SIP designed to spread heat more efficiently

System Mechanical



	28C	50C	100C	150C	183C	217C	245C	260C	245C	217C	183C	150C	100C	50C	32C
Unit 1	38	37	46	46	41	63	61	53	57	48	42	41	45	50	41
Unit 2	53	51	53	57	65	49	44	45	53	53	40	36	35	45	45
Unit 3	51	51	49	54	57	59	32	36	30	46	34	35	35	35	35

Module structure engineered to achieve sub-60um max warpage despite large body size!

SIP (25x30mm) Flatness – Shadow Moire Test

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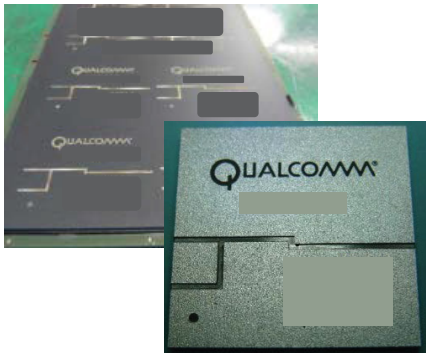
Future SIPs

Key Areas for Innovation

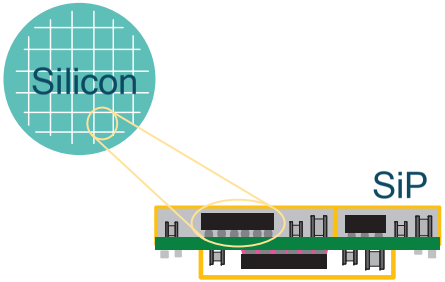
Molding/Shielding

- Single / Double Sided
- Conformal / Compartmental
- Waterproofing



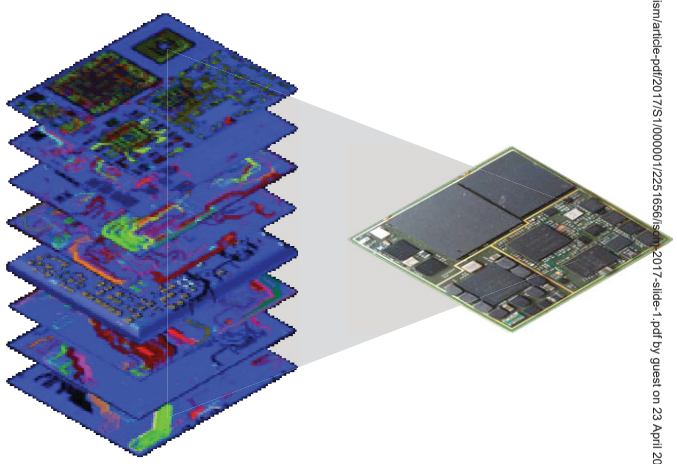
Bare Die Integration

- WLP / Flip Chip / IPDs
- Cost reduction
- Yield improvement



Embedding Components

- Multiple bare IC die
- IPDs
- Passives



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