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Packaging Challenges for the Next Generation of Mobile Devices

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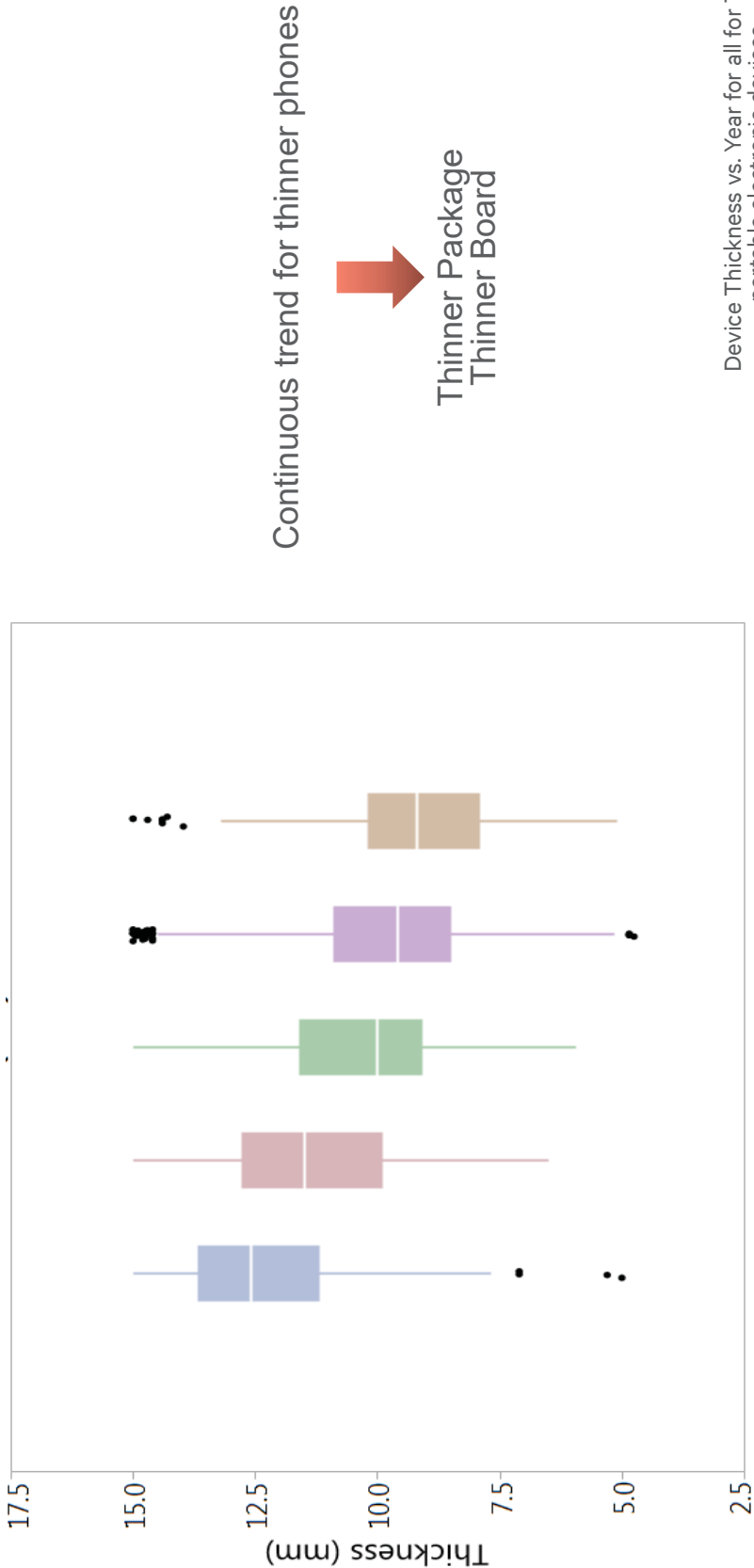
Smartphone Trends



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Smartphone Trends

Phone thickness has reduced significantly

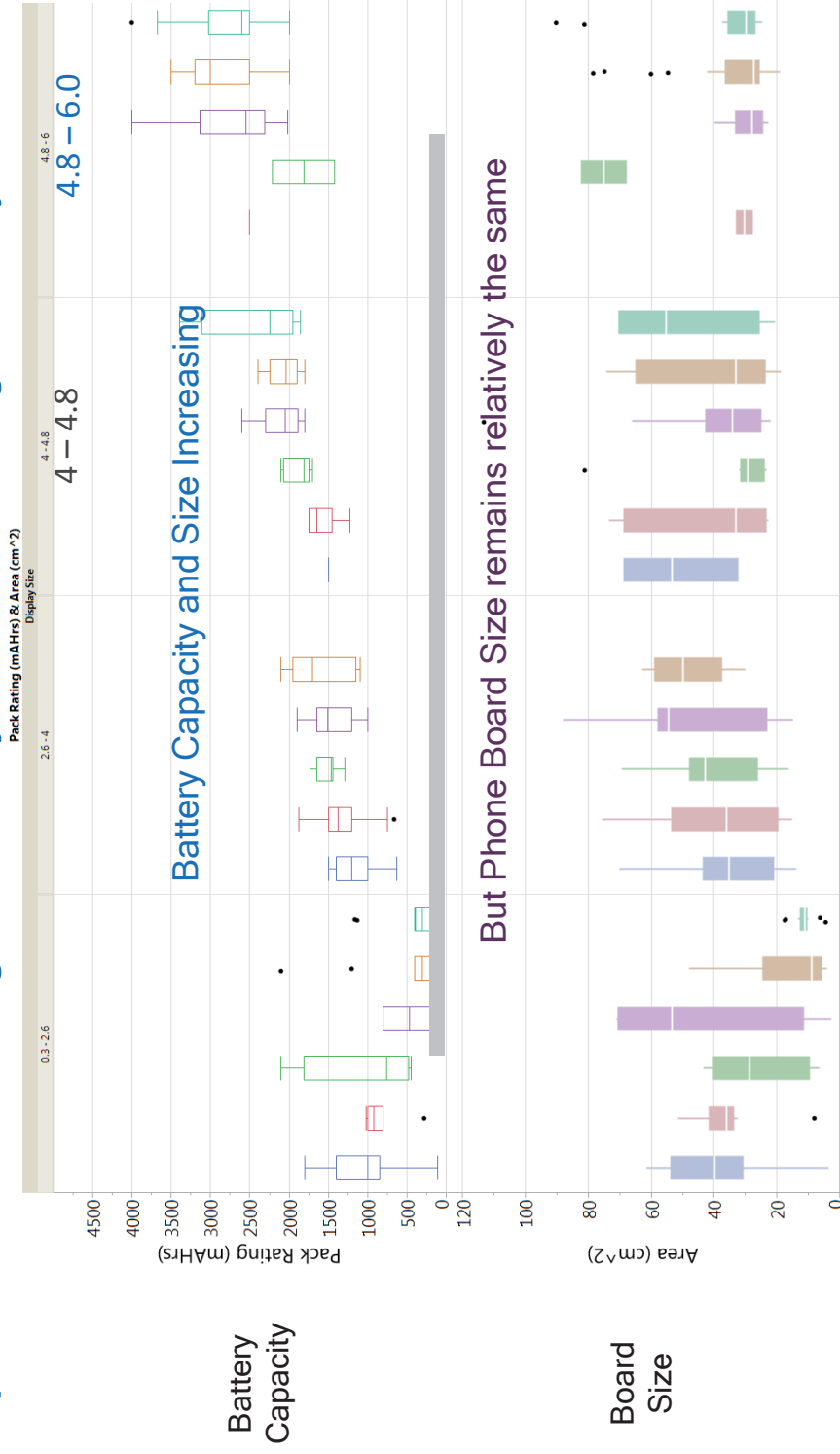


Device Thickness vs. Year for all for 7881 portable electronic devices (display sizes ranging from 0.68" to 27")

Source Data for Analysis: SpecTrax Database from 2011 to mid-2015 (N=7881)

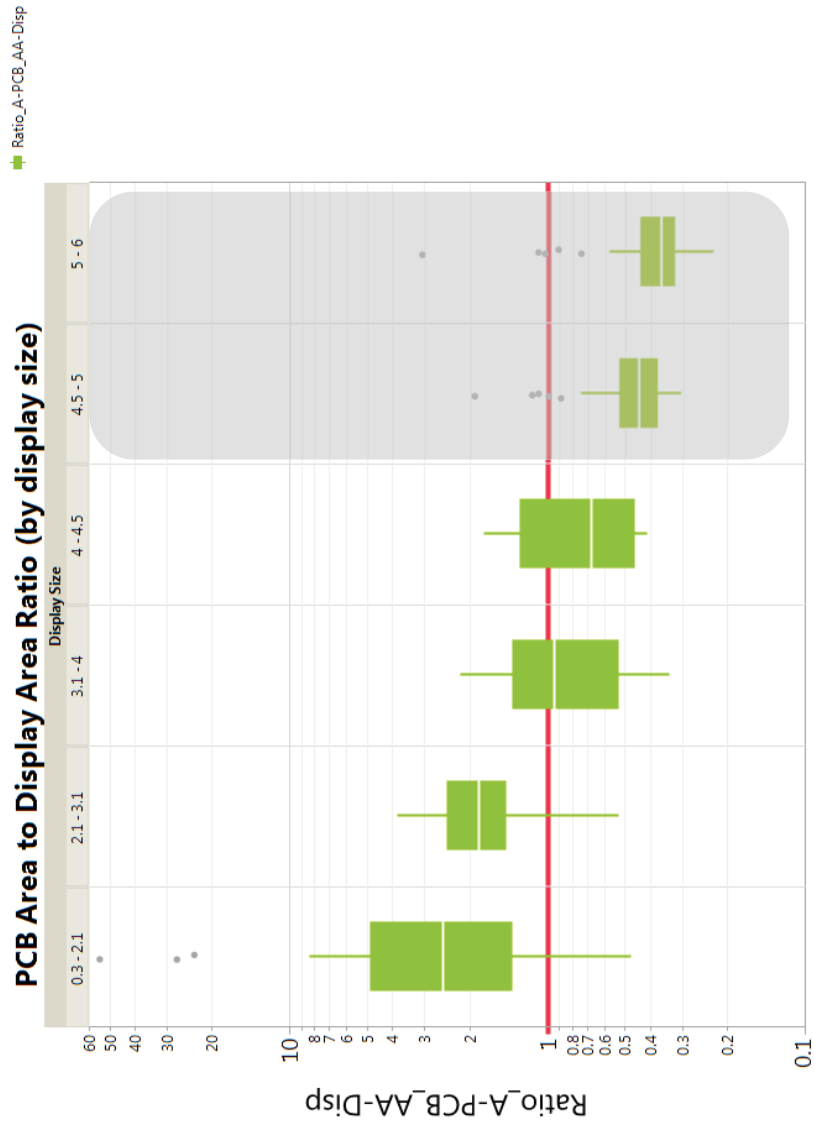
Smartphone Trends

Requirement for Longer Battery Life is Driving Battery Size



Smartphone Trends

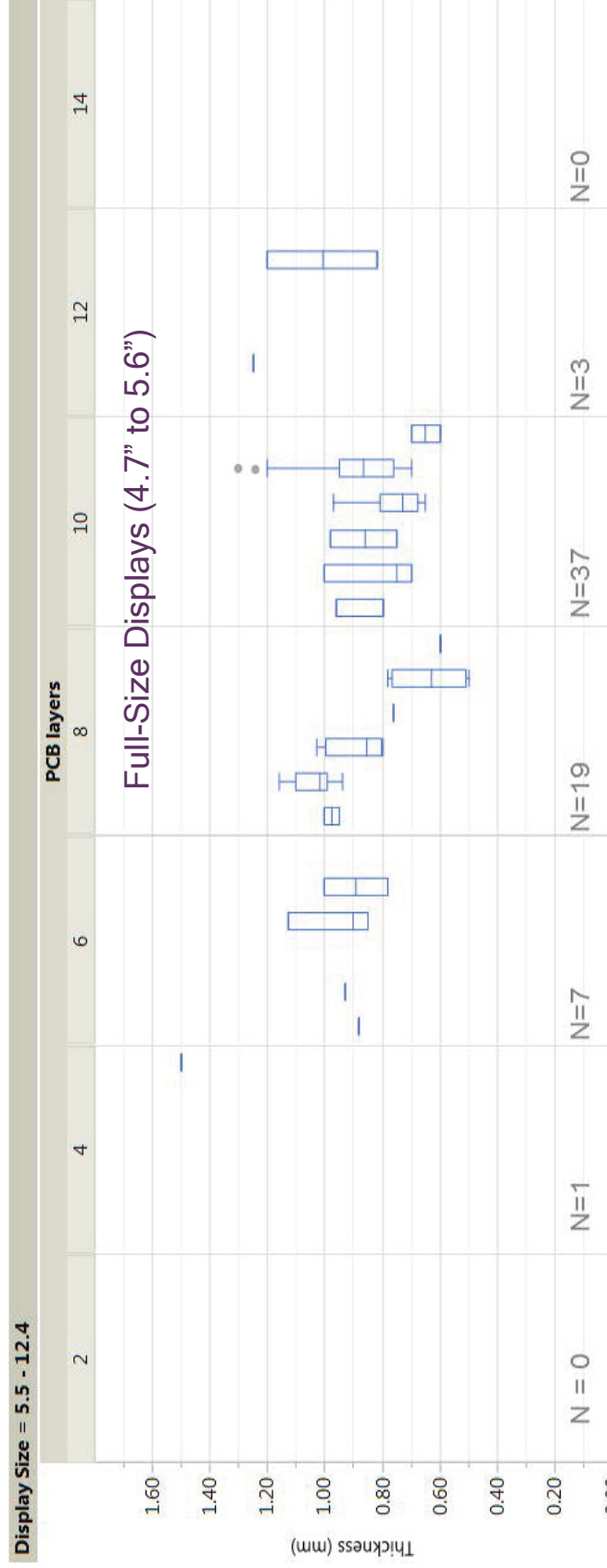
Relatively Smaller Boards for larger displays



Source Data for Analysis: SpecTrax Database from 2011 to mid-2015 (N=7881)
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Smartphone Trends

Board Thickness and Layer Count



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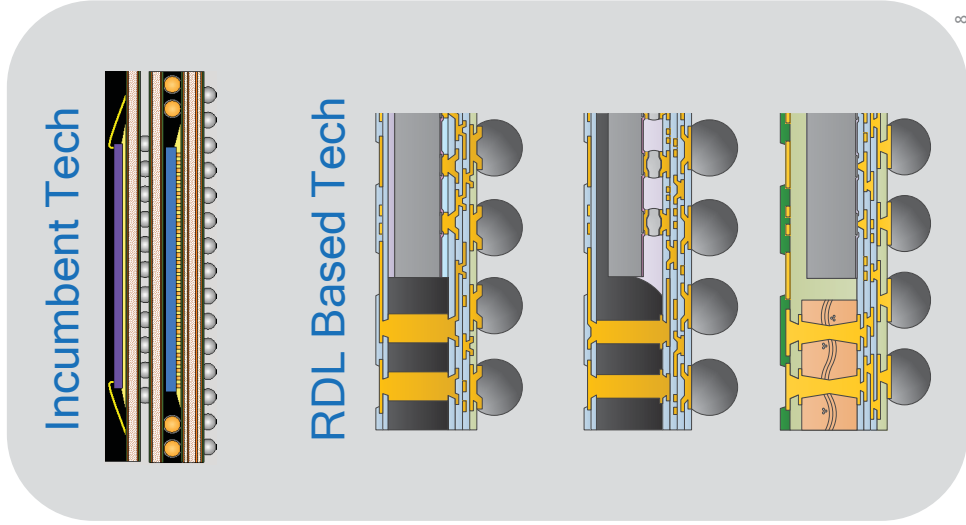
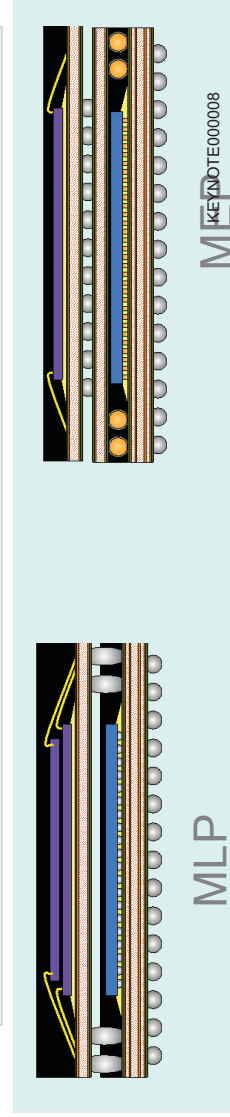
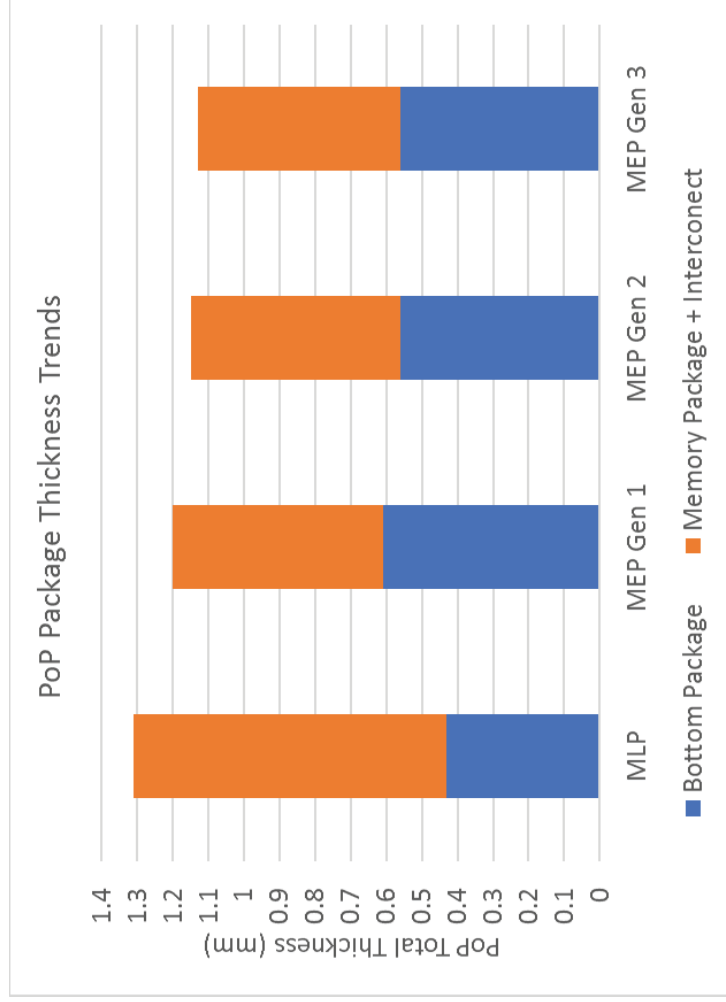
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Packaging Trends



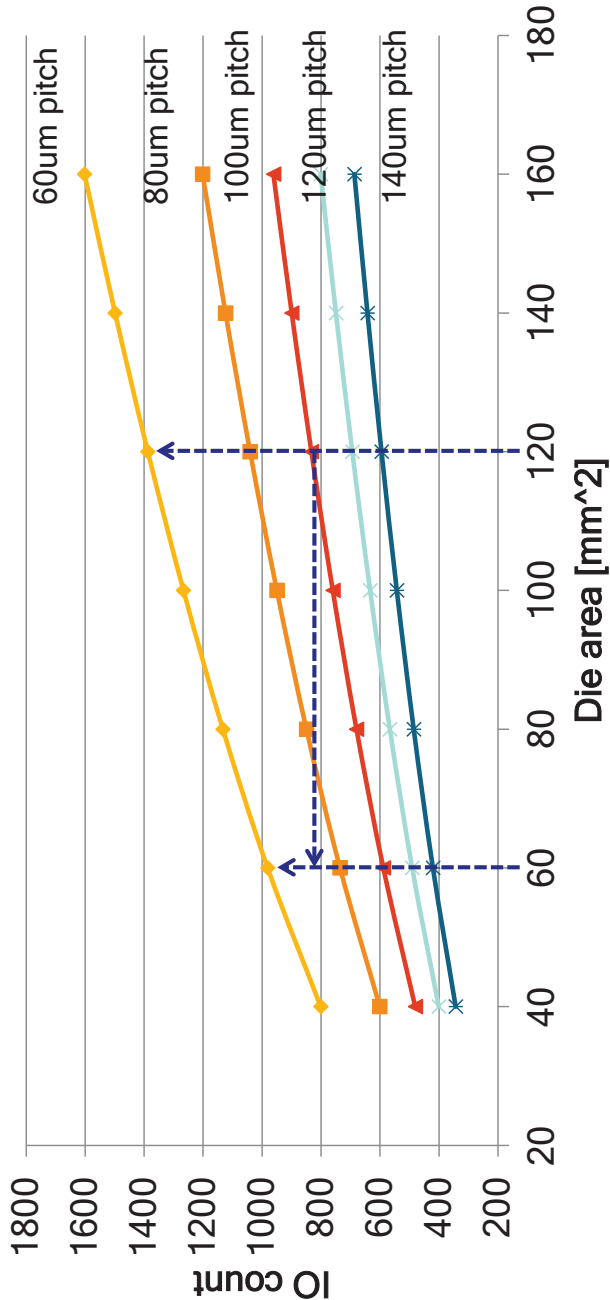
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Package z-height by PoP Gen



Drives for Bump Pitch Reduction

- More demanding mobile SoC device performance requires higher I/O counts
- Shrinking die size for advance silicon nodes requires fine bump pitch
- Cu pillar bump is a must for fine pitch application, continuously smaller UBM due to pitch shrink

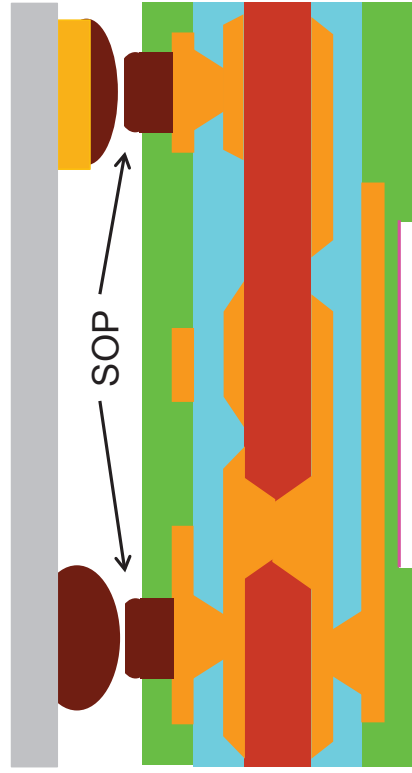


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Fine Pitch Flip Chip Interconnect Trends

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FC Interconnect using SOP



Fine Pitch FC used in mobile devices

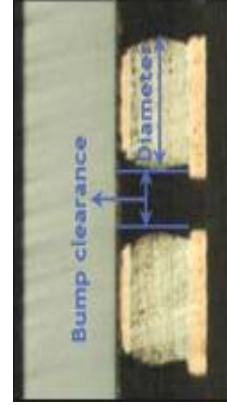


Mass Reflow (MR) FC (≥ 140 μm)

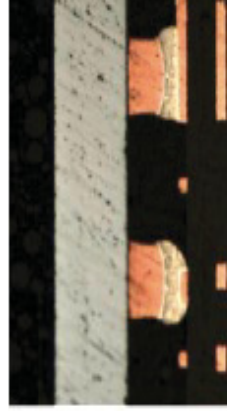
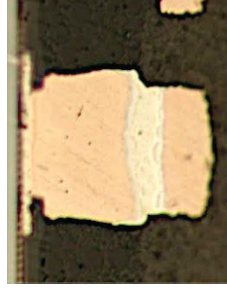
CuBOL/ETS (≥ 100 μm)

CuBOL (≥ 100 μm)

TCFC (≤ 80 μm)



Conventional solder bump flip chip



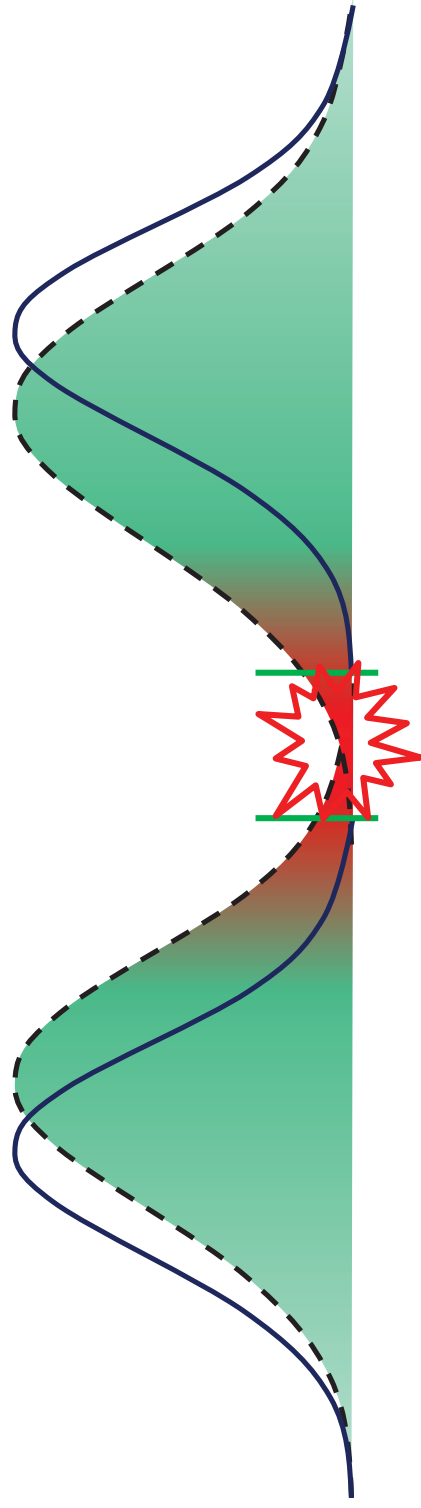
- Substrate uses narrow bond leads instead of flip chip pads, and die uses Cu pillars w/ SnAg solder cap
 - CuBOL: Cu pillar bond on lead mass reflow chip attach
 - TCFC: thermo-compression flip chip attach
 - CuBOL/ETS - coreless embedded trace substrate with BOL interconnect
 - Capillary and molded underfills are used

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Chip-Package-Board Interaction

Chip - Package

Board

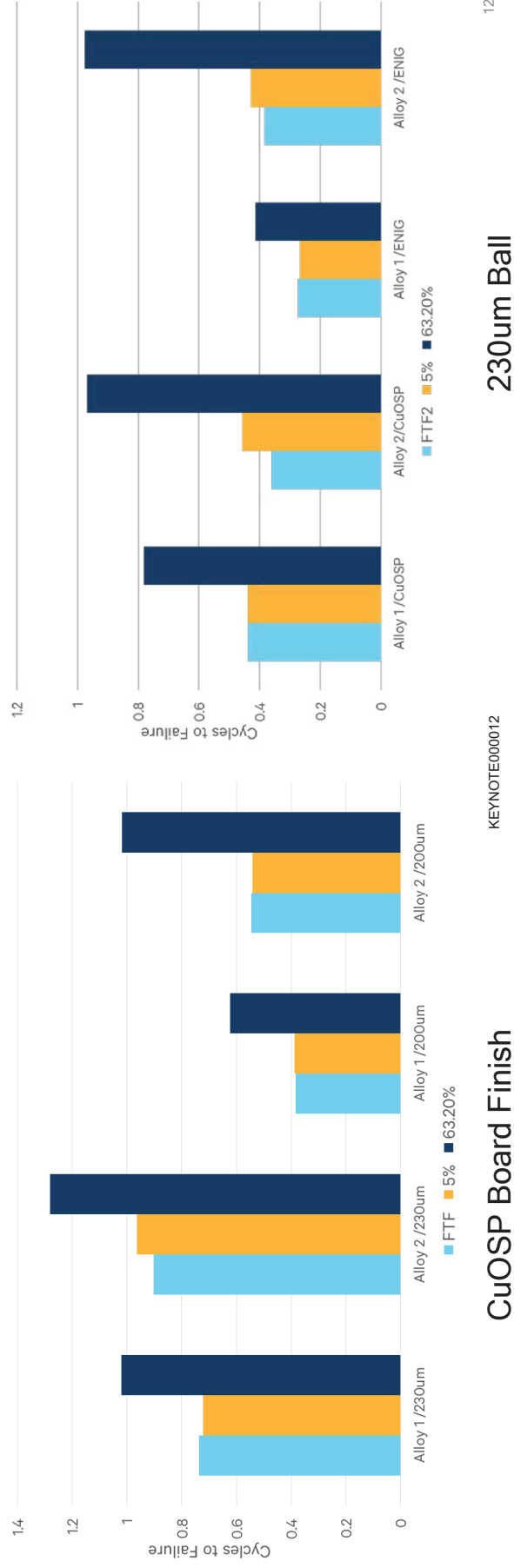


- Die package area ratio
- Tighter I/O pitch => Smaller bumps
- Thinner substrates and Packages >> Higher warpage
- Fab Nodes / Assembly Processes
- Thinner board with higher layer count
- Increased CTE and Stiffness
- Denser boards with double-sided assembly
- SMT Process variations

**Stress to Strength Margins are significantly reduced
resulting in increased risk of failures**

Board Level Reliability Challenges

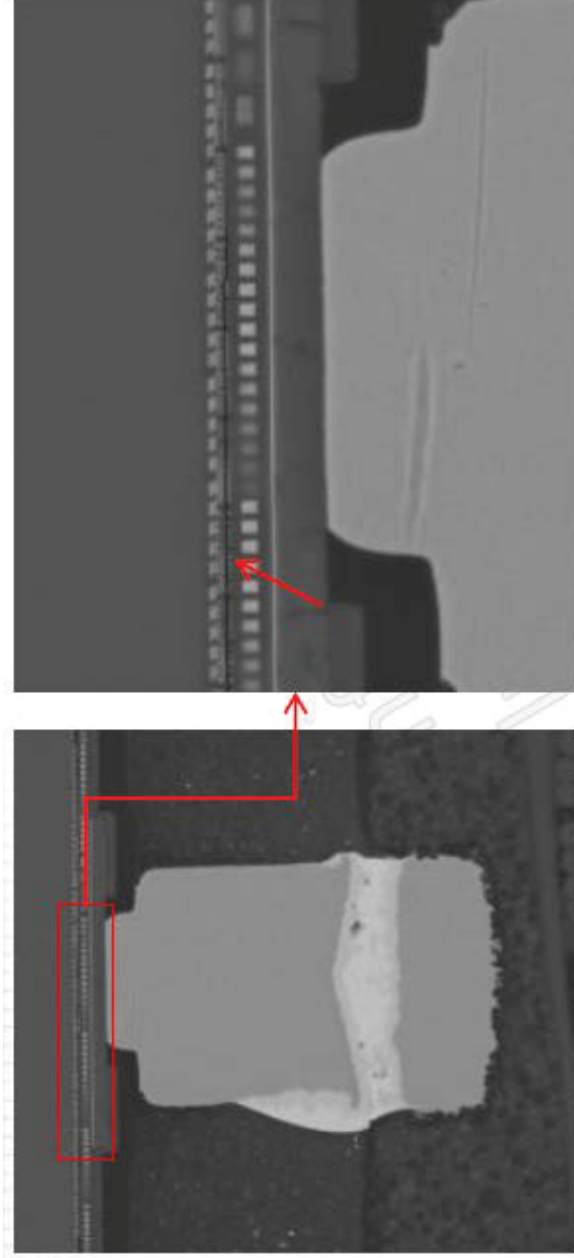
- WLCSP - Solder ball alloy, Ball Size, and Board Finish
 - Smaller balls > lower reliability
 - ENIG board finish > lower reliability
 - New solder ball alloys needed to improve reliability for smaller balls, larger die, and ENIG board finish



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Low K Stress and Delam

- Stress from Si and package substrate CTE Mismatch
- Si node scaling -> low K dielectric -> More porosity -> weak mechanical strength -> susceptible for delamination
- Bump pitch reduction -> Less compliant Cu pillars, smaller UBM



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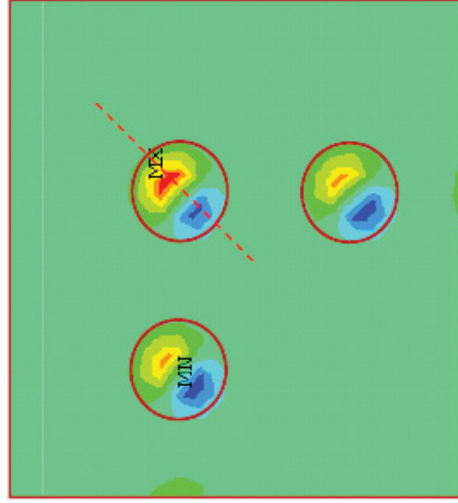
CPI Simulations

SAT image & FEA Tensile Stress Contour Comparison

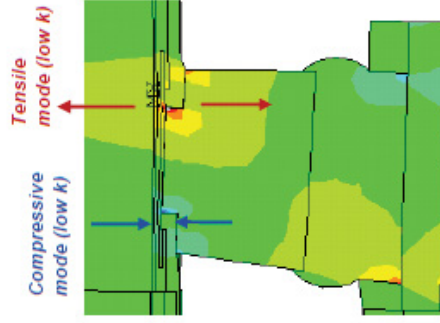
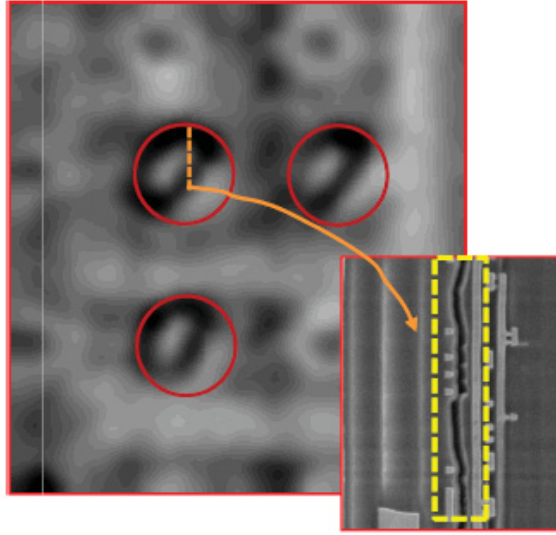
- **Half Moon Type low k layer damage** shows that the failure mode is governed by the **tensile (peeling) stress** near the Al to Cu pillar interfacial shoulder



Simulated Max Tensile stress
of low k layer
after chip attach at die corner



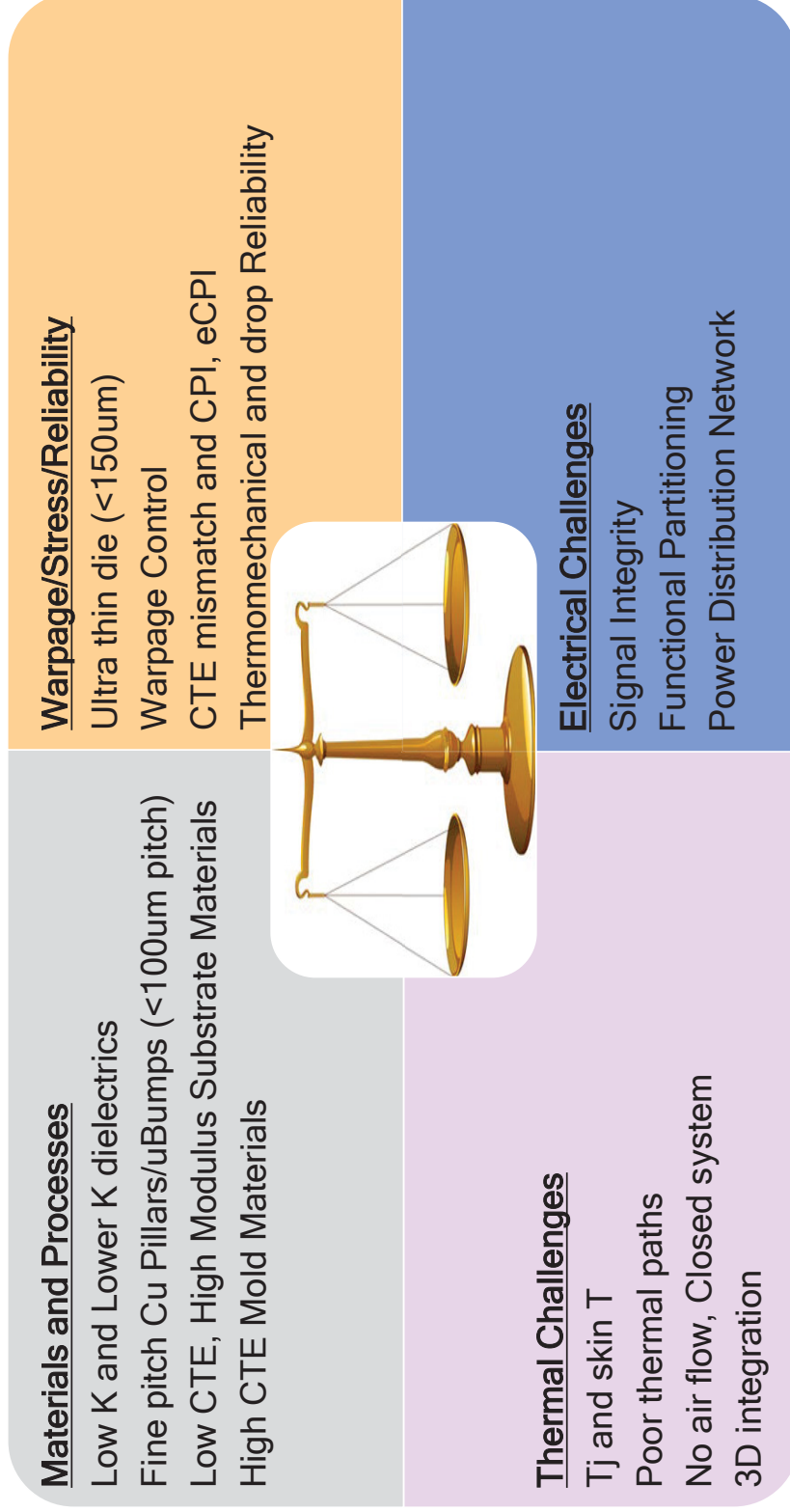
White bump by SAT
(low k damage) at die corner



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Courtesy: Amkor

Technical Challenges for Mobile Applications



While meeting Cost and Quality Targets

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Overcoming Packaging Challenges



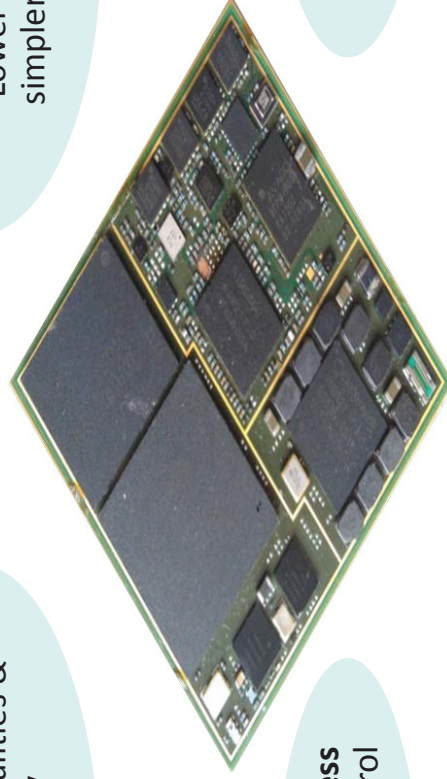
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Overcoming Packaging Challenges

Form-Factor Reduction
Free-up more space for
adding more functionalities &
bigger battery

Manage Board Level Stress
Materials & process control



Lower Complexity for Customer
Lower layer count &
simpler board design

Simplified Supply Chain

Better Thermal Performance
Optimized Heat distribution
and conduction path

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Current SiPs Commercially Available

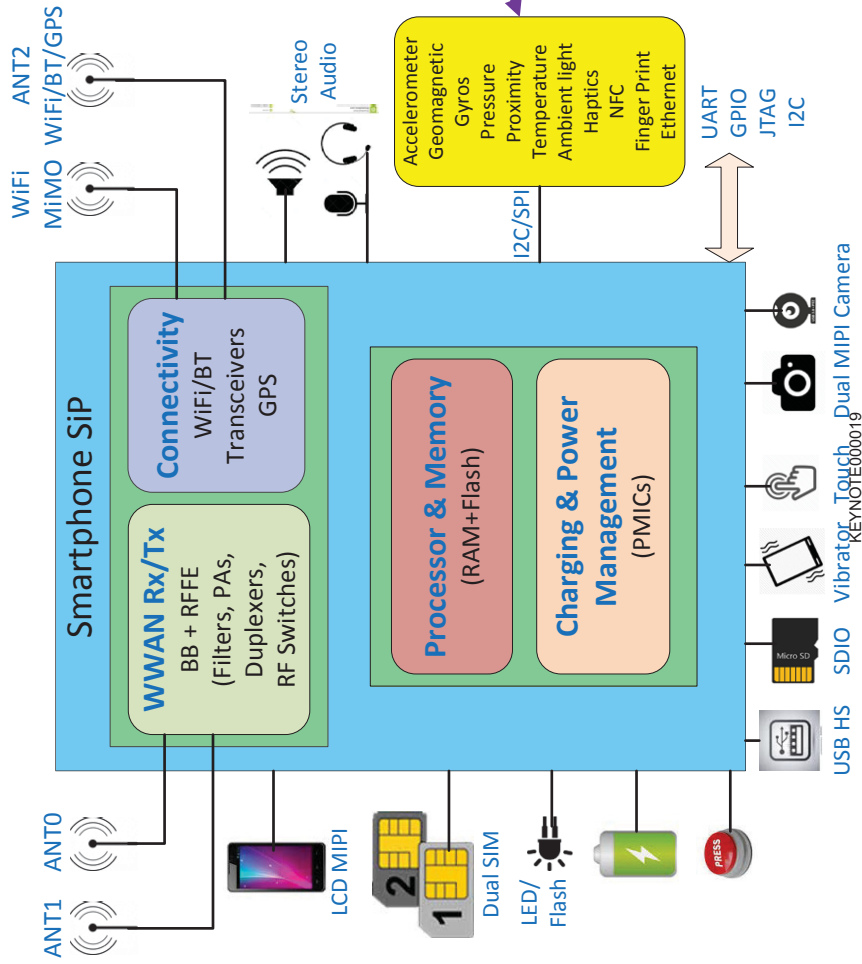
Most SiPs are sub-systems for mobile devices

- SiP consists of
 - Bare IC die
 - Packaged IC die (2D/3D)
 - SMT active and passive components
 - Integrated passive devices (IPD)
 - Embedded components
 - Performance enhancements
 - Thermal lids
 - Shielding
 - Stiffeners



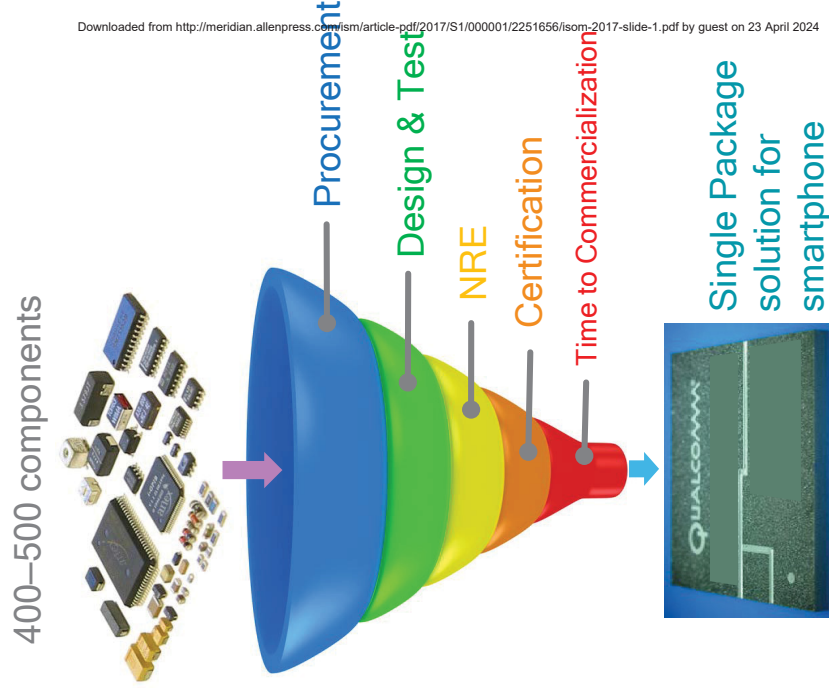
SiP with Complete Mobile System

A Genuine Mobile SiP!



SIP Benefit for Customers

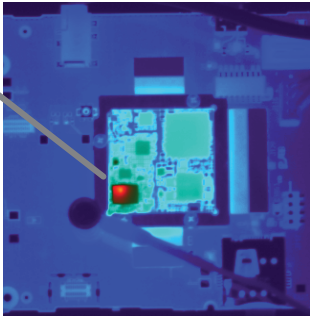
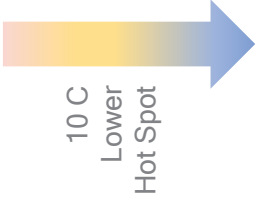
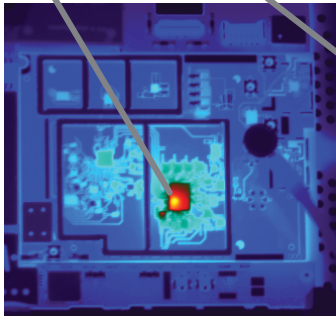
- Simplified Supply Chain**
 - No large design team and multiple board turns required to design a phone
 - No longer need to manage hundreds of suppliers
- Help OEMs reduce time-to-market and cost**
 - Comprehensive solution to simplify process of designing, building, and manufacturing
 - Reduce phone PCB layer count and burden for system designers
- Reduce upfront investment and operating cost**
 - Simplify complexities of wireless device design and tests
 - Flexibility to focus on customization and differentiation
- Attractive business model**
 - Small form factor S-SIP to allow ID design flexibility
 - Pre-tested and Pre-certification for cost effective ownership



SiP Advantages

Thermal and Mechanical Performance

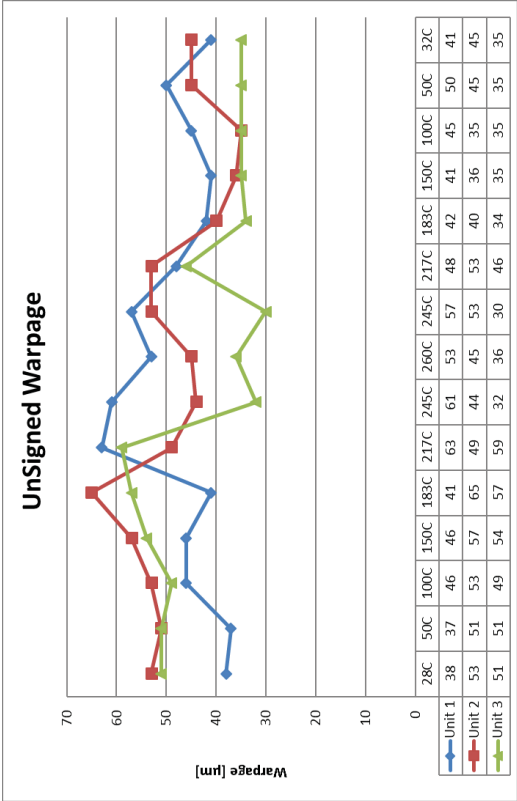
System Thermal



SIP designed to spread heat more efficiently

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System Mechanical



Module structure engineered to achieve sub-60µm max warpage despite large body size!

SIP (25x30mm) Flatness – Shadow Moire Test

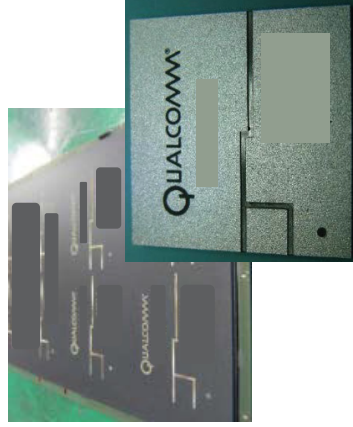
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Future SIPs

Key Areas for Innovation

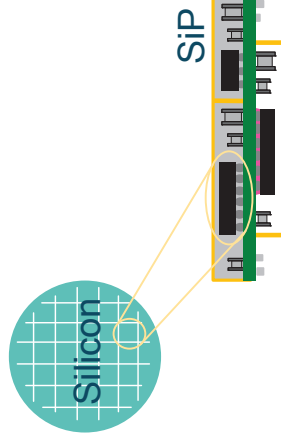
Molding/Shielding

- Single / Double Sided
- Conformal / Compartmental
- Waterproofing



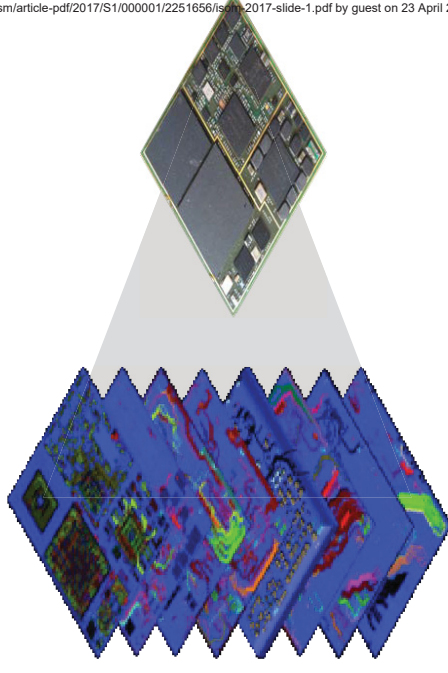
Bare Die Integration

- WLP / Flip Chip / IPDs
- Cost reduction
- Yield improvement



Embedding Components

- Multiple bare IC die
- IPDs
- Passives



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