

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TEXAS INSTRUMENTS INCORPORATED,
Petitioner,

v.

SONRAI MEMORY LIMITED,
Patent Owner.

IPR2022-00801
Patent 6,874,014 B2

Before GREGG I. ANDERSON, STACEY G. WHITE, and
JOHN D. HAMANN, *Administrative Patent Judges*.

HAMANN, *Administrative Patent Judge*.

DECISION
Dismissal Prior to Institution of Trial
35 U.S.C § 314; 37 C.F.R. § 42.71

On April 1, 2022, Texas Instruments Incorporated (“Petitioner”) filed a Petition requesting *inter partes* review of U.S. Patent No. 6,874,014. Paper 2. On August 22, 2022, with our authorization, Petitioner and Sonrai Memory Limited (“Patent Owner”) filed a Joint Motion to Dismiss the Petition. Paper 7 (“Motion”). We denied the parties’ Motion without prejudice because the parties did not submit agreements “between the parties made in connection with, or in contemplation of, the termination of a proceeding.” 37 C.F.R. § 42.74(b). Paper 8, 2–3. On September 29, 2022, the parties filed a Renewed Joint Motion to Dismiss the Petition (Paper 9, Renewed Motion), and a Joint Request to Keep Agreement Confidential and Separate (Paper 10).

In the Renewed Motion, the parties state that they “have settled their dispute,” and “have dismissed their dispute in the district court proceeding.” Renewed Motion 1–2. The parties also filed an unredacted copy of the written Release Agreement between the parties (Ex. 1024), which is the subject of the parties’ request to seal as business confidential information.

We have not instituted trial in this proceeding. Thus, this proceeding is in its initial stages. The parties indicate that they have settled their disputes relating to the challenged patent. Paper 9, 1–2. Under these circumstances, we determine that it is appropriate to dismiss the petition. *See* 37 C.F.R. §§ 42.5(a), 42.71(a). This paper does not constitute a final written decision pursuant to 35 U.S.C. § 318(a).

It is

ORDERED that the parties’ Renewed Joint Motion to Dismiss is *granted* (Paper 9), and the Petition for *inter partes* review of the above-referenced patent is *dismissed*;

FURTHER ORDERED that the “Joint Request to Keep Agreement Confidential and Separate” (Paper 10) is *granted*; and

FURTHER ORDERED that the Release Agreement (Ex. 1024) shall be kept separate from the files of the patents at issue in these proceedings, and made available only to Federal Government agencies on written request, or to any person on a showing of good cause, pursuant to 37 C.F.R. § 42.74(c).

IPR2022-00801
Patent 6,874,014 B2

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-00168	DATE FILED 2/23/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT LG ELECTRONICS INC.; LG ELECTRONICS U.S.A., INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
2 6,724,241	4/20/2004	SONRAI MEMORY LIMITED
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT 9/2/2022 Order Granting Motion to Dismiss - Doc #59

CLERK Philip J Devlin	(BY) DEPUTY CLERK <i>Suzanne Miles</i>	DATE 9/2/2022
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Ex. 1004 - Page 5

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-00167	DATE FILED 2/23/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT GOOGLE, LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
2 6,724,241	4/20/2004	SONRAI MEMORY LIMITED
3		
4		
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT 9/2/2022 - Order Granting Motion to Dismiss - Doc #66

CLERK Philip J Devlin	(BY) DEPUTY CLERK <i>Suzanne Miles</i>	DATE 9/2/2022
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 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

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Ex. 1004 - Page 6

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS INC. and LG ELECTRONICS U.S.A., INC.,
Petitioner,

v.

SONRAI MEMORY LIMITED,
Patent Owner.

IPR2022-00756
Patent 6,874,014 B2

Before GREGG I. ANDERSON, STACEY G. WHITE, and
JOHN D. HAMANN, *Administrative Patent Judges*.

HAMANN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314
Granting Motion for Joinder
35 U.S.C § 315(c); 37 C.F.R. § 42.122

I. INTRODUCTION

LG Electronics Inc. and LG Electronics U.S.A., Inc. (collectively, “Petitioner”) filed a petition for *inter partes* review of claims 1–3, 5–9, 11–13, and 15–19 (“the challenged claims”) of U.S. Patent No. 6,874,014 B2 (Ex. 1001, “the ’014 patent”). Paper 2 (“Pet.”). Sonrai Memory Limited (“Patent Owner”) did not file a Preliminary Response.

Petitioner also filed a Motion for Joinder seeking joinder as a petitioner with Google LLC (“Google”) in *Google LLC v. Sonrai Memory Ltd.*, IPR2021-01454 (the “Google IPR”). Paper 3 (“Motion”). Patent Owner did not file an opposition to the Motion for Joinder.

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018); *see* 37 C.F.R. § 42.108 (2020). For reasons discussed below, we institute an *inter partes* review of the challenged claims and grant Petitioner’s Motion for Joinder.

A. *Real Parties-in-Interest*

The parties identify themselves as the real parties-in-interest. Pet. 1; Paper 5, 1.

B. *Related Matters*

The parties collectively identify the following as matters that may affect, or be affected by, a decision in this proceeding: (i) *Sonrai Memory Ltd. v. Google LLC*, 6-21-cv-00167 (W.D. Tex.); (ii) *Sonrai Memory Ltd. v. LG Electronics Inc.*, 6-21-cv-00168 (W.D. Tex.); (iii) *Sonrai Memory Ltd. v. Samsung Electronics Co., Ltd.*, 6:21-cv-00169-ADA (W.D. Tex.); (iv) *Sonrai Memory Ltd. v. Amazon.com, Inc.*, 6:21-cv-00991-ADA (W.D. Tex.);

(v) *Sonrai Memory Ltd. v. Texas Instruments Inc.*, 6-21-cv-01066 (W.D. Tex.); (vi) *Sonrai Memory Ltd. v. Lenovo Group Ltd.*, 6-22-cv-00029 (W.D. Tex.); (vii) *Sonrai Memory Ltd. v. Samsung Electronics Co.*, 6-22-cv00189 (W.D. Tex.); (viii) *Sonrai Memory Ltd. v. Amazon.com, Inc.*, 6-22-cv-00225 (W.D. Tex.); (ix) *Sonrai Memory Ltd. v. Motorola Mobility LLC*, 1-22-cv-01606 (N.D. Ill.); (x) *Google LLC v. Sonrai Memory Ltd.*, IPR2021-01454 (PTAB); and (xi) *Texas Instruments Inc. v. Sonrai Memory Ltd.*, IPR2022-00801 (PTAB). Pet. 1–3; Paper 5, 1–2.

C. The Challenged Patent

The '014 patent “is generally related to a computer chip architecture having multiple processors on a single die,” and “[m]ore particularly, . . . is related to a multiprocessing chip utilizing multiple operating systems.” Ex. 1001, 1:6–9. The '014 patent teaches having multiple processors mounted on a single die, which “is connected to a memory storing multiple operating systems.” *Id.* at code (57). “Each of the processors or a group of one or more of the processors is operable to execute a distinct one of the multiple operating systems.” *Id.* “Therefore, resources for a single operating system may be dedicated to one processor or a group of processors.” *Id.* “Consequently, a large number of processors mounted on a single die can operate efficiently,” according to the '014 patent. *Id.*

Figure 3, shown below, “illustrates an embodiment of a multiprocessing scheme,” in accordance with the '014 patent. *Id.* at 2:54–55.

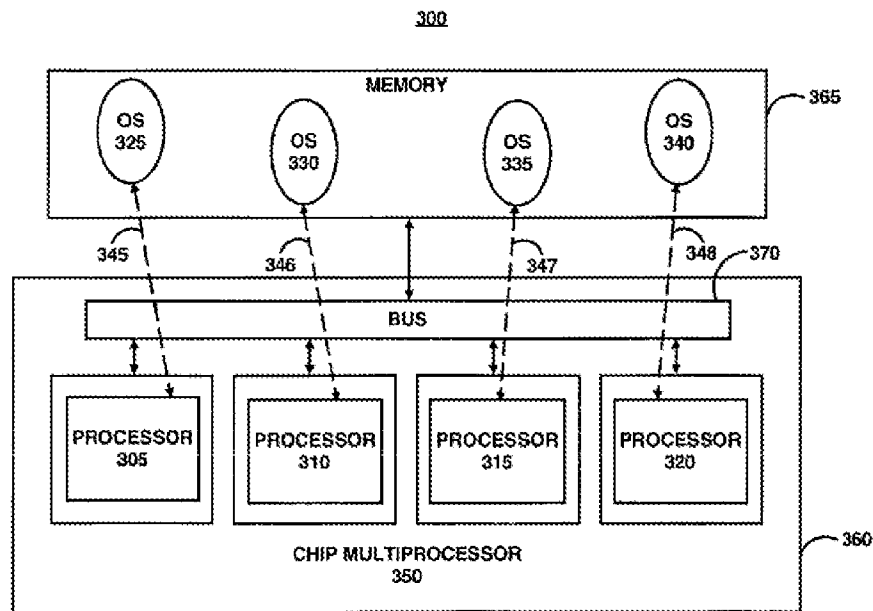


FIG. 3

Figure 3 “illustrates an embodiment including a computer system 300 employing the principles of the” ’014 patent. *Id.* at 3:4–6. As illustrated, “[s]ystem 300 includes a chip multiprocessor 350 having multiple processors 305–320 mounted on a single die 360.” *Id.* at 3:6–7, Fig. 3. “The processors 305–320 function with operating systems 325–340 respectively, as illustrated by connections 345–348.” *Id.* at 3:8–10. “The operating systems 325–340 are stored in a memory 365.” *Id.* at 3:10–11. The ’014 patent discloses that “[d]uring operation, each processor 305–320 may access a respective operating system 325–340 by communicating with the memory 365, for example, via a bus 370.” *Id.* at 3:11–15.

The ’014 patent discloses that “[p]rocessors 305–320 may be configured, such that each processor executes its own operating system,” or “[m]ultiple processors (e.g., multiple processors in a processor group) may . . . be configured to execute a single operating system.” *Id.* at 3:21–24. Moreover, “[e]ach processor may be capable of executing a single operating system, or capable of simultaneously executing multiple operating systems,

for example, by context switching, which may include rapidly switching between multiple operating systems.” *Id.* at 3:46–50.

D. The Challenged Claims

Petitioner challenges claims 1–3, 5–9, 11–13, and 15–19 of the ’014 patent. Claims 1, 7, and 12 are independent claims. Claim 1 is illustrative of the challenged claims and is reproduced below:

1. A multiprocessing system comprising:
 - multiple processors mounted on a single die; and
 - multiple operating systems residing in a memory connected to said multiple processors,
 - wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.

Ex. 1001, 4:14–22.

E. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims of the ’014 patent are unpatentable based on the following grounds:

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1–3, 5–9, 11–13, 15–19	103(a)	Asano, ² Joy ³
1–3, 5–9, 11–13, 15–19	103(a)	Asano, Babaian ⁴

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the ’014 patent issued from an application filed before March 16, 2013, we apply the pre-AIA version of the statutory basis for unpatentability.

² US 2001/0044817 A1, published Nov. 22, 2001 (Ex. 1005, “Asano”).

³ US 6,542,991 B1, issued Apr. 1, 2003 (Ex. 1006, “Joy”).

⁴ US 7,143,401 B2, issued Nov. 28, 2006 (Ex. 1007, “Babaian”).

Pet. 4, 14–74. Petitioner submits in support of its arguments the Declaration of Dr. Martin Walker (Ex. 1002).

II. INSTITUTION OF *INTER PARTES* REVIEW

The Petition in this proceeding asserts the same grounds of unpatentability as the one on which we instituted review in the Google IPR. *Compare* Pet. 14–74, with Google IPR, Paper 6 at 5. Indeed, Petitioner argues that the Petition “is substantively identical to the petition filed by Google, challenging the same claims of the ’014 patent on the same grounds.” Pet. 1. More specifically, Petitioner submits that the “Petition copies verbatim the challenges set forth in the Google Petition and relies on the same expert declaration submitted in the Google IPR.” Motion 4. According to Petitioner, “[t]he only differences between the . . . Petition and the Google Petition relate to formalities of a different party filing the petition; there are no other changes to the facts, citations, evidence, or invalidity arguments introduced in the Google Petition.” *Id.* at 4–5.

Patent Owner did not file a Preliminary Response.

For the same reasons set forth in our institution decision in the Google IPR, we determine that the information presented in the Petition shows a reasonable likelihood that Petitioner would prevail in showing that at least one claim of the ’014 patent is unpatentable. *See* Google IPR, Paper 6, 10–15. Accordingly, we institute an *inter partes* review on all of the challenged claims.

III. GRANT OF MOTION FOR JOINDER

We instituted trial in the Google IPR on March 4, 2022. Google IPR, Paper 6. Petitioner filed the Petition and Motion for Joinder on April 1, 2022. Because joinder was requested no later than one month after

trial was instituted in the Google IPR, Petitioner's Motion for Joinder is timely. *See* 37 C.F.R. § 42.122(b).

The statutory provision governing joinder in *inter partes* review proceedings is 35 U.S.C. § 315(c), which reads:

If the Director institutes an *inter partes* review, the Director, in his or her discretion, may join as a party to that *inter partes* review any person who properly files a petition under section 311 that the Director, after receiving a preliminary response under section 313 or the expiration of the time for filing such a response, determines warrants the institution of an *inter partes* review under section 314.

A motion for joinder should (1) set forth reasons why joinder is appropriate; (2) identify any new grounds of unpatentability asserted in the petition; (3) explain what impact (if any) joinder would have on the trial schedule for the existing review; and (4) address specifically how briefing and discovery may be simplified. *Kyocera Corp. v. Softview LLC*, IPR2013-00004, Paper 15, 4 (PTAB Apr. 24, 2013).

Petitioner asserts the same unpatentability grounds on which we instituted review in the Google IPR. *See* Motion 1, 4–5. Petitioner “submits identical arguments and the same grounds introduced in the existing Google IPR, . . . and relies on the same expert declaration submitted in the Google IPR.” *Id.* at 4. Indeed, the Petition “copies verbatim the challenges set forth in the Google Petition.” *Id.* Thus, this *inter partes* review does not present any ground or matter not already at issue in the Google IPR.

If joinder is granted, Petitioner anticipates participating in the proceeding in a limited capacity absent termination of the Google IPR petitioner as a party. Motion 1–2; *see also id.* at 7–9. Petitioner states that it “will act as an ‘understudy’ unless the current petitioner (Google) ceases to actively participate in the instituted IPR.” *Id.* at 1–2. Because Petitioner

expects to participate only in a limited capacity, Petitioner submits that “the proposed joinder will neither unduly complicate the Google IPR nor delay its schedule. As such, joinder will promote judicial efficiency in determining the patentability of the ’014 Patent without prejudice to Patent Owner.” *Id.* at 2. Petitioner further indicates that Google does not oppose the request joinder. *Id.* at 1.

Patent Owner did not file an opposition to the Motion for Joinder.

We agree with Petitioner that joinder with the Google IPR is appropriate under the circumstances. Accordingly, we *grant* Petitioner’s Motion for Joinder.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–3, 5–9, 11–13, and 15–19 of the ’014 patent is instituted on all asserted grounds in IPR2022-00756;

FURTHER ORDERED that the Motion for Joinder is *granted*, and Petitioner is joined as a party to IPR2021-01454;

FURTHER ORDERED that all further filings by Petitioner and Patent Owner, except for those which concern a request for rehearing of this decision, shall be made only in IPR2021-01454;

FURTHER ORDERED that, subsequent to joinder, the grounds and claims for trial in IPR2021-01454 remain unchanged;

FURTHER ORDERED that, subsequent to joinder, the Scheduling Order in place for IPR2021-01454 (Papers 7, 8) remains unchanged, subject to any change already made by stipulation between Patent Owner and Google;

FURTHER ORDERED that, subsequent to joinder, Petitioner is bound by every paper filed by and every representation made by Google in IPR2021-01454, except for papers and representations regarding settlement between Google and Patent Owner;

FURTHER ORDERED that Petitioner shall make no filing and take no action in the joined proceeding unless (1) Google ceases to be a party in the joined proceeding, or (2) the filing is a motion to terminate the proceeding with respect to Petitioner, a settlement agreement between Petitioner and Patent Owner, or a request to keep settlement agreement separate under 37 C.F.R. § 42.74(c);

FURTHER ORDERED that Petitioner shall not receive any direct, cross examination, or redirect time beyond that permitted for Google alone, under either 37 C.F.R. § 42.53 or any agreement between Google and Patent Owner;

FURTHER ORDERED that the case caption in IPR2021-01454 shall be changed in accordance with the attached example; and

FURTHER ORDERED that a copy of this Decision shall be entered into the record of IPR2021-01454.

IPR2022-00756
Patent 6,874,014 B2

For PETITIONER:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC, LG ELECTRONICS INC.,
and LG ELECTRONICS U.S.A., INC.,
Petitioners,

v.

SONRAI MEMORY LIMITED,
Patent Owner.

IPR2021-01454⁵
Patent 6,874,014 B2

⁵ LG Electronics Inc. and LG Electronics U.S.A., Inc. were joined as parties to this proceeding via the grant of a Motion for Joinder in IPR2022-00756.

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Northern District of Illinois on the following

☒ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 1:22-cv-01606	DATE FILED 3/28/2022	U.S. DISTRICT COURT Northern District of Illinois
PLAINTIFF Sonrai Memory Limited		DEFENDANT Motorola Mobility LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		See Attached
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK Thomas G. Bruton	(BY) DEPUTY CLERK Jennifer Kuldaneck	DATE 8/18/2022
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

US 6,874,014 B2

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memory means for storing said plurality of operating system means.

13. The apparatus of claim 12, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

14. The apparatus of claim 12, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

15. The apparatus of claim 12, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

16. The apparatus of claim 12, wherein said processor means includes a plurality of processor group means,

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wherein each processor group means includes at least two of said plurality of processors.

17. The apparatus of claim 16, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

18. The apparatus of claim 16, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

19. The apparatus of claim 12, wherein at least one of said plurality of processors is operable to simultaneously execute two or more of said plurality of operating system means.

* * * * *

Exhibit 2

U.S. Patent No. 6,874,014 (“’014 Patent”)

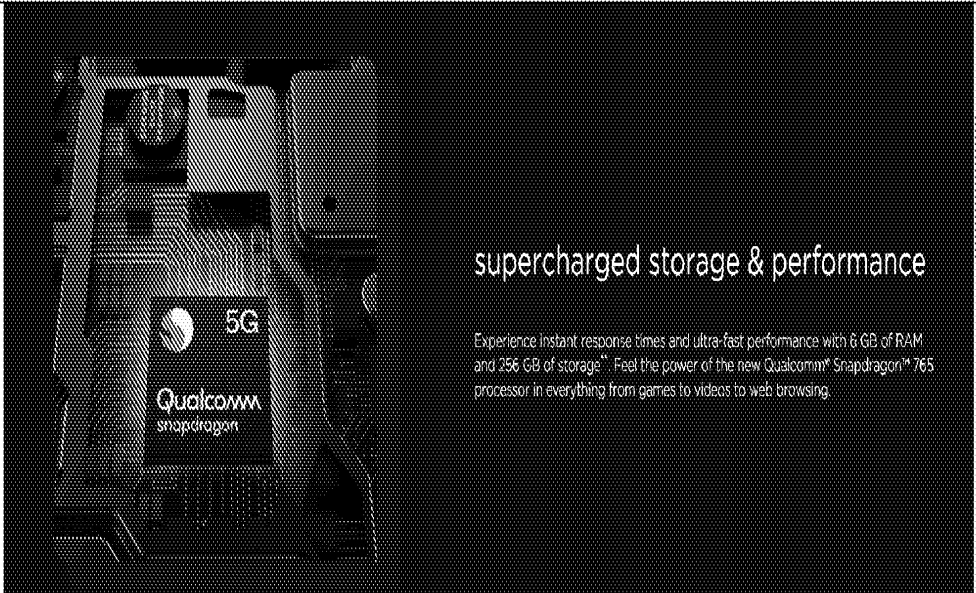
Accused Products

Motorola products with Qualcomm Snapdragon SoCs containing at least one Hexagon DSP, including without limitation the Motorola Edge (“Accused Products”), infringe at least Claim 1 of the ’014 Patent.

Claim 1

Claim 1	Accused Products
1[pre]. A multiprocessing system comprising:	To the extent the preamble is limiting, each Accused Product includes a multiprocessing system. For example, the Edge contains a Qualcomm Snapdragon 765 SoC with multiple processing cores, e.g. Kryo 475 CPU and Hexagon 696 Processor. See, e.g.:  https://www.motorola.com/us/smartphones-motorola-edge/p?skuld=352

Claim 1	Accused Products
	 Snapdragon 765 5G Mobile Platform Qualcomm® Artificial Intelligence (AI) Engine AIE GPU: Qualcomm® Adreno™ 620 GPU AIE CPU: Qualcomm® Kryo™ 475 CPU https://www.qualcomm.com/products/snapdragon-765-5g-mobile-platform
1[a] multiple processors mounted on a single die; and	Each Accused Product includes multiple processors mounted on a single die. For example, the Edge contains a Qualcomm Snapdragon 865 SoC with multiple processing cores, e.g. Kryo 475 CPU and Hexagon 696 Processor. See, e.g.:

Claim 1	Accused Products
	 https://www.motorola.com/us/smartphones-motorola-edge/p?skuld=352  Snapdragon 765 5G Mobile Platform Qualcomm® Artificial Intelligence (AI) Engine AIE GPU: Qualcomm® Adreno™ 620 GPU AIE CPU: Qualcomm® Kryo™ 475 CPU https://www.qualcomm.com/products/snapdragon-765-5g-mobile-platform
1[b] multiple operating systems residing in a memory	Each Accused Product includes multiple operating systems residing in a memory connected to said multiple processors.

Claim 1	Accused Products
connected to said multiple processors,	For example, the Edge contains multiple operating systems, <i>e.g.</i> Android and QuRT. <i>See, e.g.:</i> QuRT™ Software Qualcomm Technologies processors like our Qualcomm® Hexagon™ DSP found on the Qualcomm® Snapdragon™ 8 series mobile platform, have their own embedded RTOS called QuRT. QuRT offers features like multithreading, mutexes, semaphores, timers, interrupt handling, memory management, etc., and enables programs and threads to execute in separate protected address spaces for improved system security and stability. Developers can write user programs designed to utilize QuRT in C/C++ and/or assembly using the Hexagon DSP SDK and use the QuRT APIs to access the RTOS services. Each user program has access to the global heap, and contains a main thread call stack, data and text sections, and the ability to allocate additional heaps and threads. And as stated on our Hexagon DSP SDK page on QDN, the programmer does not need to focus on the underlying threading model since QuRT maps user software threads onto the processor's hardware threads. QuRT can globally schedule the highest-priority runnable software threads and directs interrupts to the lowest-priority hardware thread. QuRT also manages software and hardware watchdog timers to detect and reset system failures. https://developer.qualcomm.com/blog/role-realtime-operating-system-rtos-mobile

Claim 1	Accused Products
	 https://www.motorola.com/us/smartphones-motorola-edge/p?skuId=352
1[c] wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.	In the Accused Products, each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems. For example, the Edge executes the Android 10 operating system on the Kryo 475 CPU within the Qualcomm Snapdragon 765 SoC, and executes the QuRT operating system on the Hexagon DSP within the Qualcomm Snapdragon 765 SoC. The two operating systems run simultaneously, as shown by the fact that both QuRT and Android contain their own independent scheduling systems, running on separate processors, with only indirect serial communication between the two operating systems. <i>See, e.g.:</i>

Claim 1	Accused Products
	QuRT™ Software Qualcomm Technologies processors like our Qualcomm® Hexagon™ DSP found on the Qualcomm® Snapdragon™ 8 series mobile platform, have their own embedded RTOS called QuRT¹. QuRT offers features like multithreading, mutexes, semaphores, timers, interrupt handling, memory management, etc., and enables programs and threads to execute in separate protected address spaces for improved system security and stability. Developers can write user programs designed to utilize QuRT in C/C++ and/or assembly using the Hexagon DSP SDK and use the QuRT APIs to access the RTOS services. Each user program has access to the global heap, and contains a main thread call stack, data and text sections, and the ability to allocate additional heaps and threads. And as stated on our Hexagon DSP SDK page on QDN, the programmer does not need to focus on the underlying threading model since QuRT maps user software threads onto the processor's hardware threads. QuRT can globally schedule the highest-priority runnable software threads and directs interrupts to the lowest-priority hardware thread. QuRT also manages software and hardware watchdog timers to detect and reset system failures. https://developer.qualcomm.com/blog/role-realtime-operating-system-rtos-mobile

Claim 1	Accused Products
	The programmer does not need to focus on the threading since the RTOS maps user software threads onto the processors hardware threads. These hardware threads share the entire memory hierarchy including L1. Thus, it is very beneficial for the software to employ threads that cooperate on shared data. To facilitate this, a very fast RTOS kernel has been designed for Hexagon. The RTOS globally schedules the highest priority runnable software threads and always directs interrupts to the lowest priority hardware thread. Unlike most architectures, the Hexagon instruction set originated and evolved assuming the existence of a multi-threaded implementation. The inherent latency tolerance afforded by multi-threading enabled ISA optimizations that would not otherwise be practical. Hexagon goes beyond conventional VLIW and allows for grouping of both independent and many forms of dependent instructions. As an example, the common load-compare-branch idiom can be expressed in a single Hexagon instruction packet. Such techniques enable extraction of high instruction parallelism even from irregular control-code applications. https://developer.qualcomm.com/software/hexagon-dsp-sdk/dsp-processor

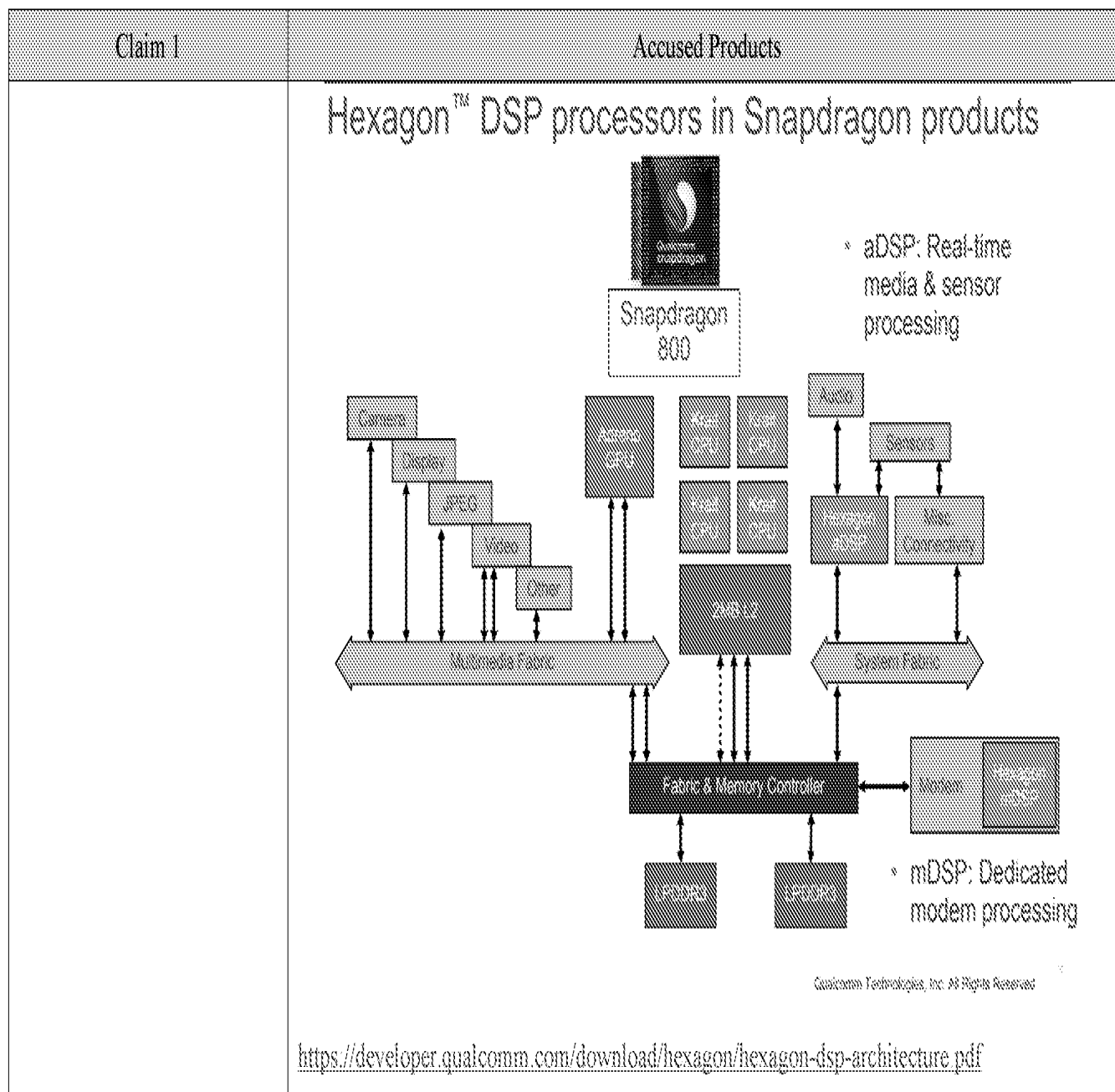
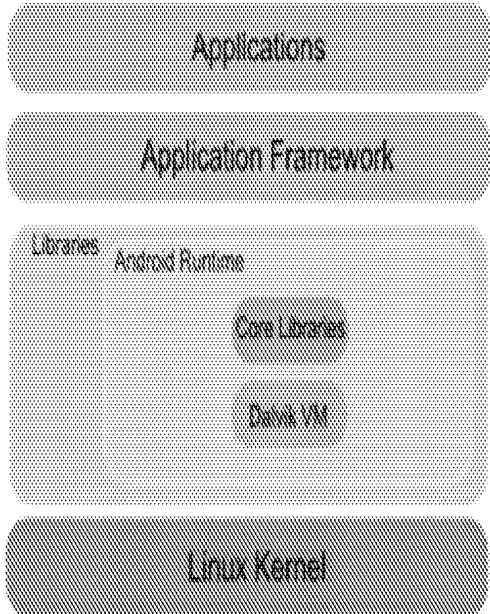


Exhibit 1

Claim 1	Accused Products
	Since version 2.6.23, the standard Linux kernel uses the Completely Fair Scheduler (CFS), which applies fairness in the way that CPU time is assigned to tasks. This balance guarantees that all the tasks will have the same CPU share and that, each time that unfairness is verified, the algorithm assures that task re-balancing is performed. Although fairness is guaranteed, this algorithm does not provide any temporal guarantees to tasks, and therefore, neither Android does it, as its scheduling operations are delegated to the Linux kernel.  Figure 1. Android Architecture Evaluating Android OS for Embedded Real-Time Systems, https://personal.utdallas.edu/~cxl137330/courses/fall13/RTS/papers/4a.pdf

**UNITED STATES DISTRICT COURT
FOR THE Northern District of Illinois – CM/ECF NextGen 1.6.3
Eastern Division**

Sonrai Memory Limited

Plaintiff,

v.

Case No.: 1:22-cv-01606
Honorable Elaine E. Bucklo

Motorola Mobility LLC

Defendant.

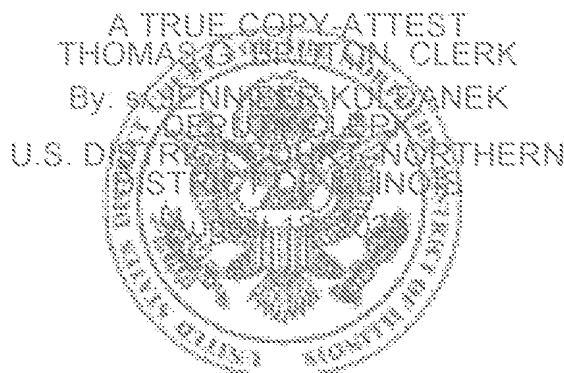
NOTIFICATION OF DOCKET ENTRY

This docket entry was made by the Clerk on Wednesday, August 17, 2022:

MINUTE entry before the Honorable Elaine E. Bucklo: Parties' joint motion to dismiss [32] is granted. Plaintiff's claims for relief against Defendant are dismissed with prejudice and Defendant's claims, defenses or counterclaims for relief against Plaintiff without prejudice, each party bearing its own attorney's fees and costs. All pending dates before this court are stricken. Civil case terminated. Mailed notice (lxx,)

ATTENTION: This notice is being sent pursuant to Rule 77(d) of the Federal Rules of Civil Procedure or Rule 49(c) of the Federal Rules of Criminal Procedure. It was generated by CM/ECF, the automated docketing system used to maintain the civil and criminal dockets of this District. If a minute order or other document is enclosed, please refer to it for additional information.

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(12) **United States Patent**
Richardson et al.

(10) **Patent No.:** **US 6,874,014 B2**
(45) **Date of Patent:** **Mar. 29, 2005**

(54) **CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS**

(56) **References Cited**

U.S. PATENT DOCUMENTS

(75) Inventors: **Stephen E. Richardson**, Los Altos, CA (US); **Gary Vondran**, San Carlos, CA (US); **Stuart Siu**, Castro Valley, CA (US); **Paul Keltcher**, Sunnyvale, CA (US); **Shankar Venkataraman**, Cupertino, CA (US); **Padmanabha Venkitakrishnan**, Sunnyvale, CA (US); **Joseph Ku**, Palo Alto, CA (US)

4,709,325 A	*	11/1987	Yajima	714/10
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6,108,731 A	*	8/2000	Suzuki et al.	710/301
6,314,501 B1	*	11/2001	Gulick et al.	711/153
6,526,462 B1	*	2/2003	Elabd	710/242
6,658,591 B1	*	12/2003	Arndt	714/6
6,772,241 B1	*	8/2004	George et al.	710/36

(73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 627 days.

* cited by examiner

Primary Examiner—Nasser Moazzami

(21) Appl. No.: **09/865,605**

(22) Filed: **May 29, 2001**

(65) **Prior Publication Data**

US 2002/0184328 A1 Dec. 5, 2002

(51) Int. Cl.⁷ **G06F 11/00**

(52) U.S. Cl. **709/213; 709/222; 711/173; 713/2; 718/1; 719/313**

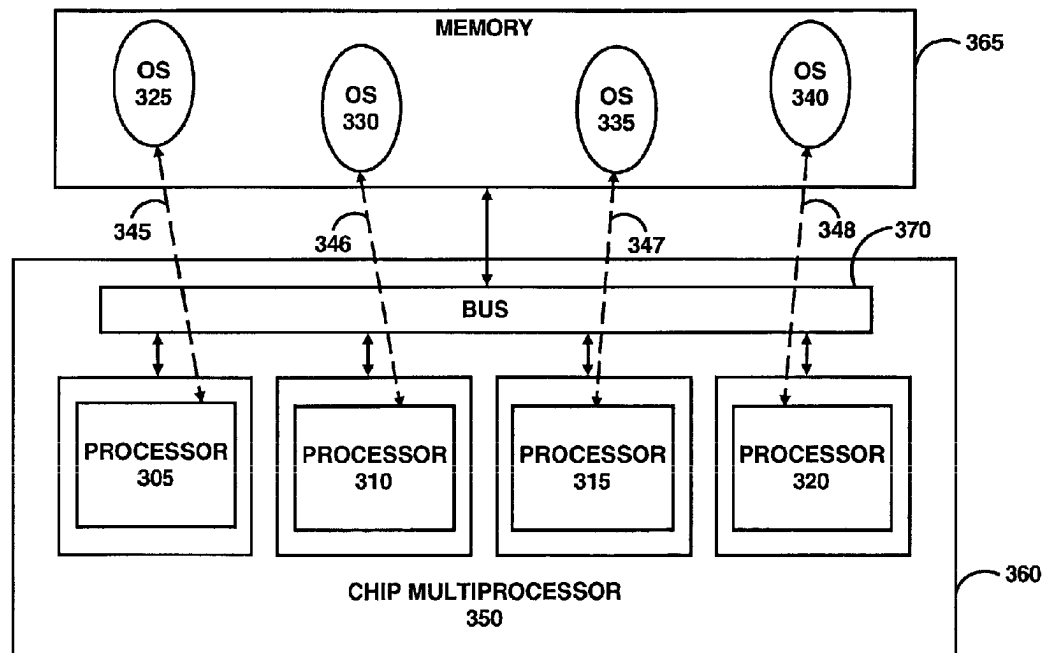
(58) Field of Search **709/220, 222, 709/213-215; 711/173, 147, 153; 713/2; 718/1, 105; 719/313; 714/6, 10**

(57) **ABSTRACT**

Multiple processors are mounted on a single die. The die is connected to a memory storing multiple operating systems or images of multiple operating systems. Each of the processors or a group of one or more of the processors is operable to execute a distinct one of the multiple operating systems. Therefore, resources for a single operating system may be dedicated to one processor or a group of processors. Consequently, a large number of processors mounted on a single die can operate efficiently.

19 Claims, 4 Drawing Sheets

300



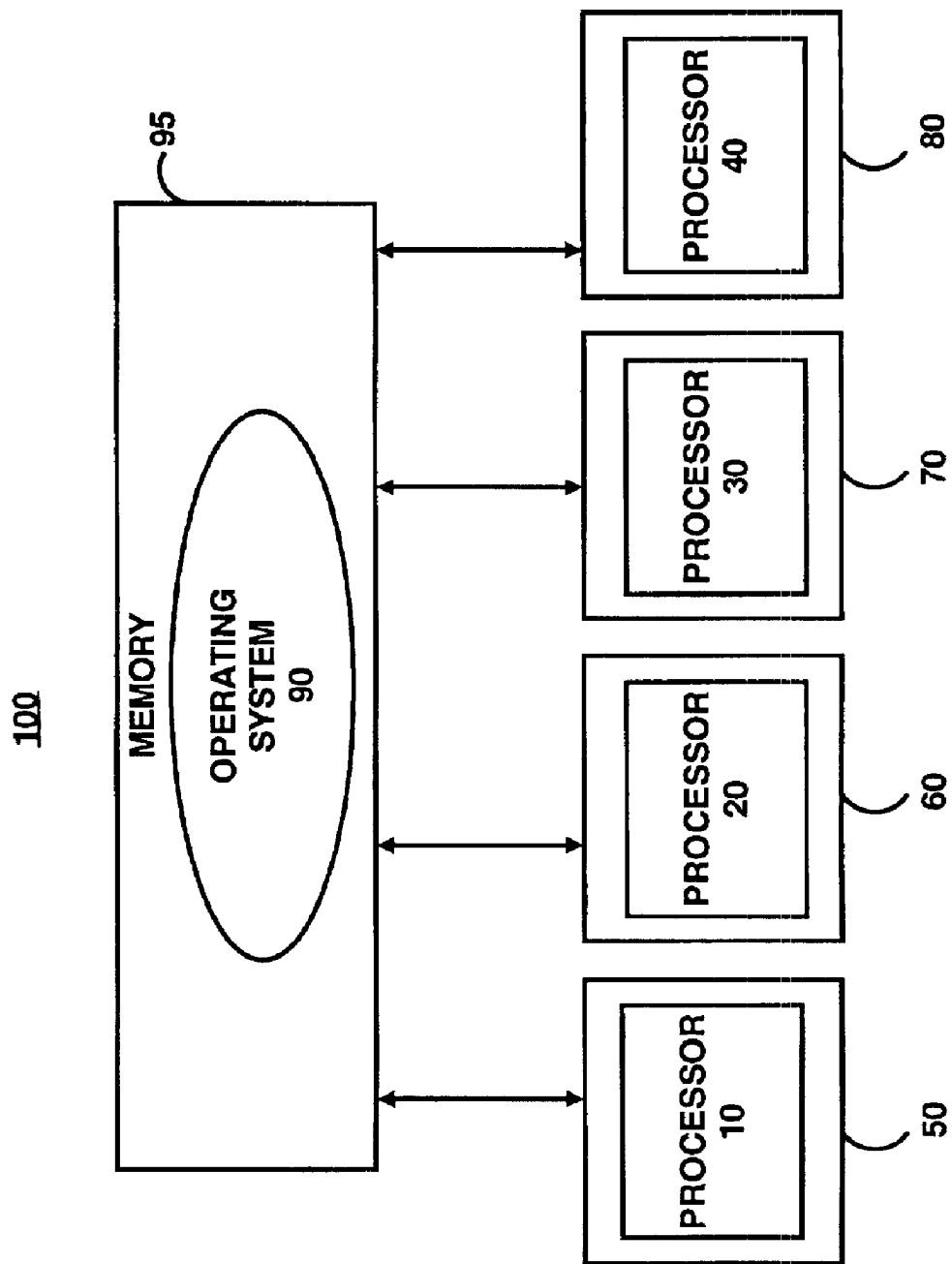


FIG. 1
Prior Art

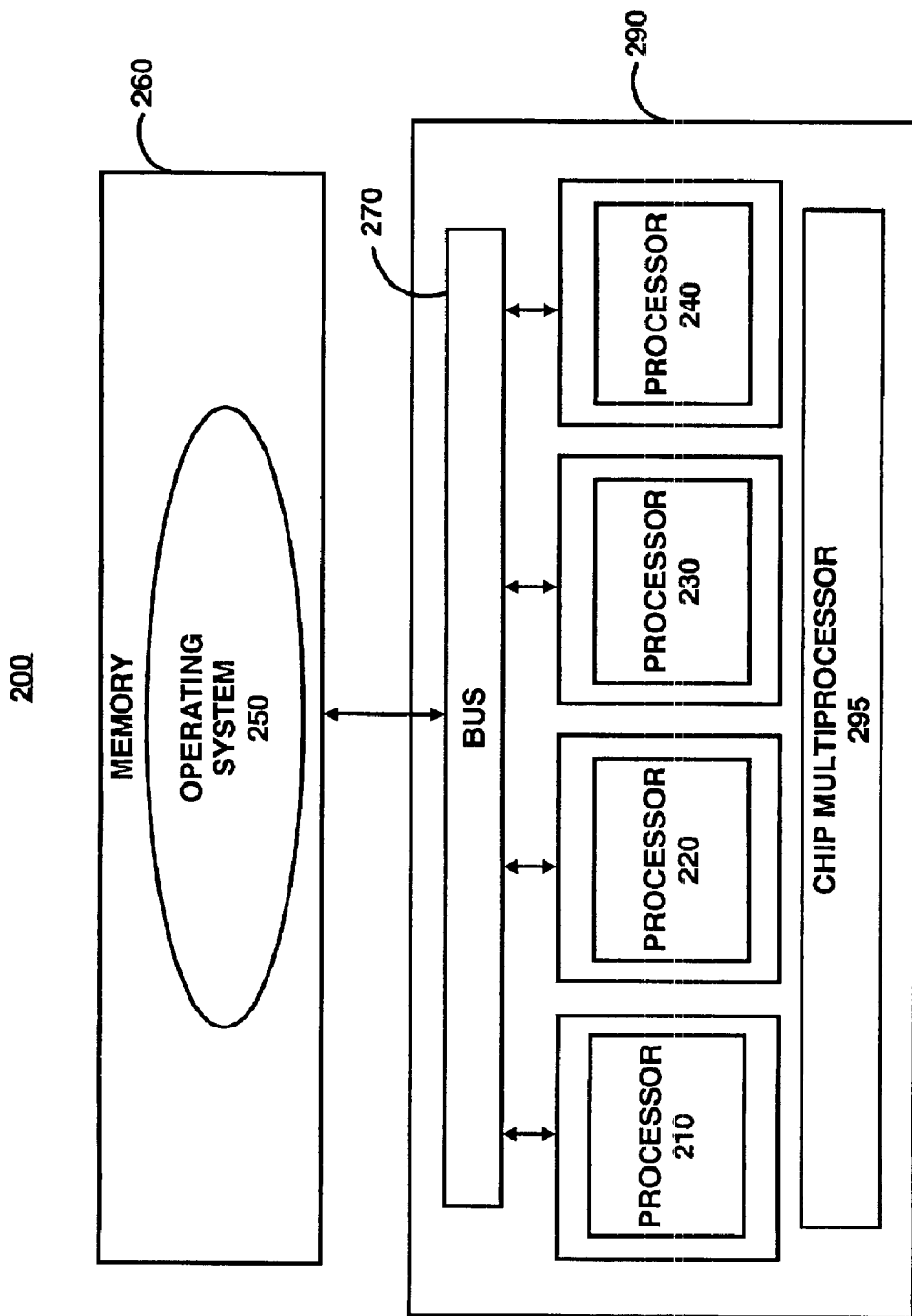


FIG. 2
Prior Art

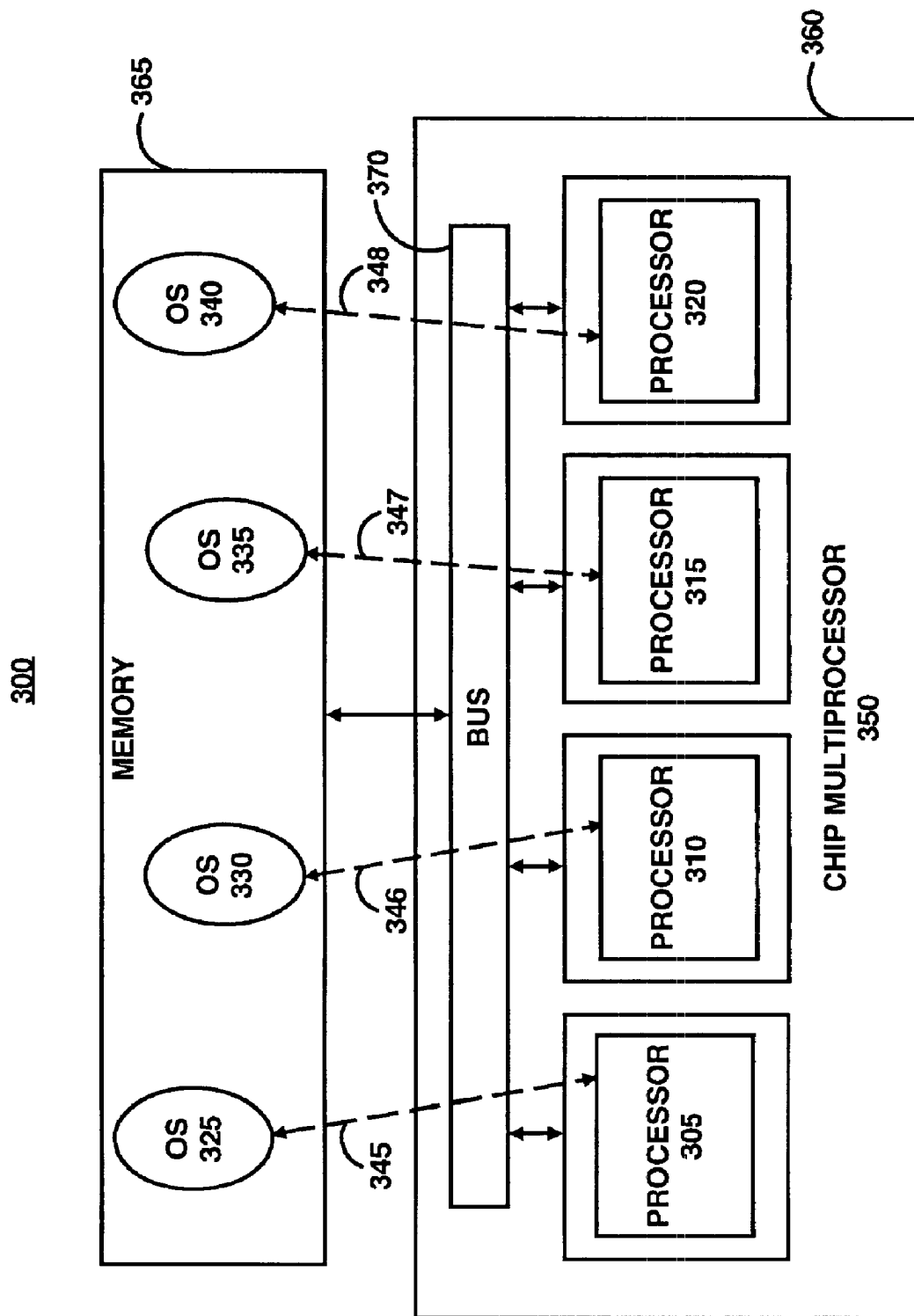


FIG. 3

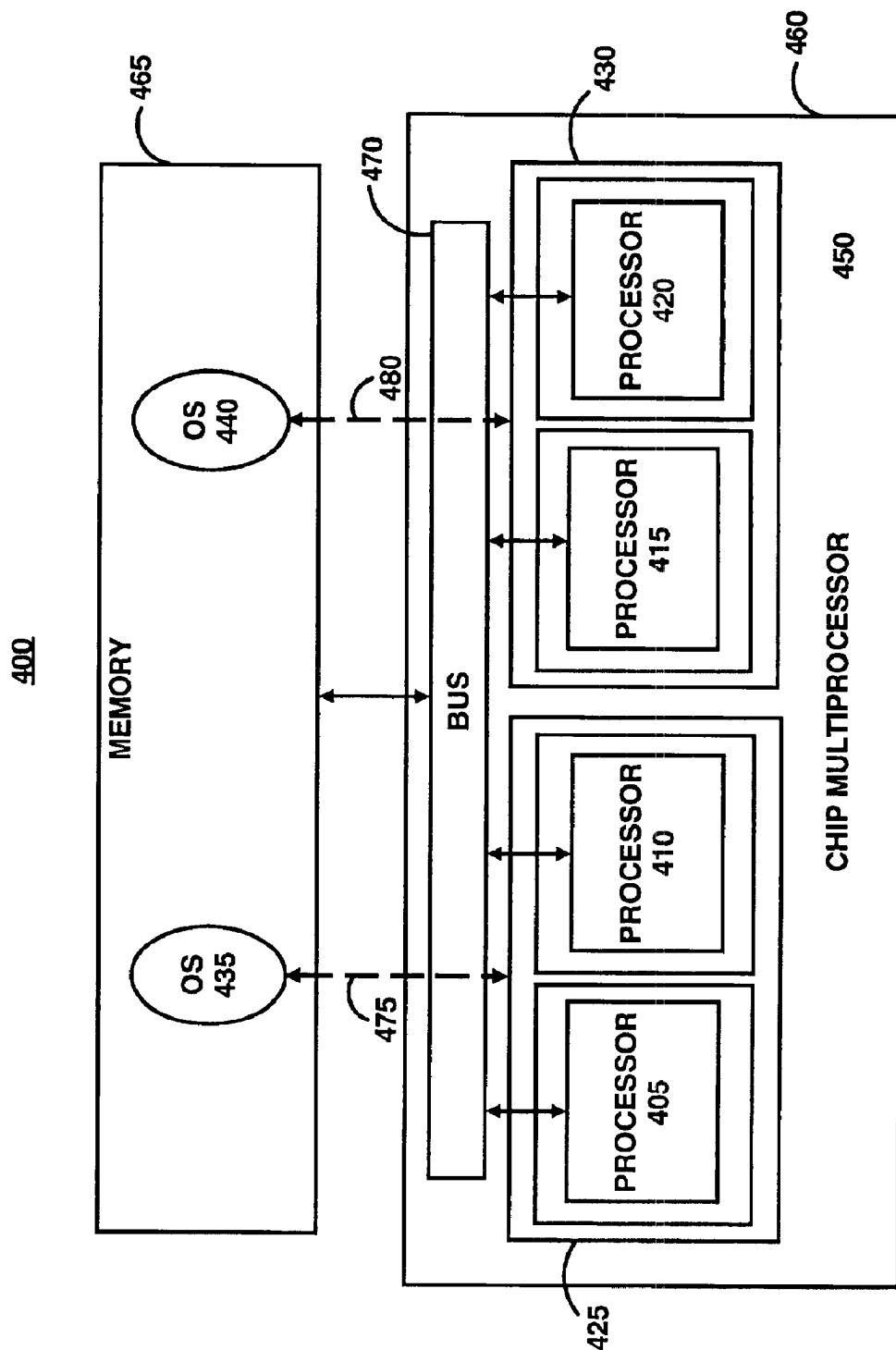


FIG. 4

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**CHIP MULTIPROCESSOR WITH MULTIPLE
OPERATING SYSTEMS****FIELD OF THE INVENTION**

The present invention is generally related to a computer chip architecture having multiple processors on a single die. More particularly, the present invention is related to a multiprocessing chip utilizing multiple operating systems.

BACKGROUND OF THE INVENTION

Existing internet data centers (IDCs) pack hundreds of processors (e.g., servers and the like) in a single building for processing a large volume of data transactions. Generally, the compute density or number of nodes per volume defines the efficiency of the IDC. The compute density effects the amortization of the high cost of the IDC infrastructure (e.g., networking, power, cooling, maintenance, reliability, and availability support). Typically, the greater the compute density, the better the IDC will be able to amortize the high cost of IDC infrastructure. Accordingly, a large compute density may be preferred. However, space may be unavailable or costly for locating a large number of processors necessary for maintaining a large compute density.

To provide increased compute density, multiprocessing schemes that utilize multiple processors have been developed. One conventional multiprocessing scheme (shown in FIG. 1) includes a computer system **100** having multiple processors **10–40**, each on a separate die (i.e., chip) **50–80**, and connected to a single operating system **90** stored in a memory **95**. The system **100** may conserve space if the system is provided in a single housing.

A second conventional multiprocessing scheme (shown in FIG. 2) includes a computer system **200** having a chip multiprocessor **295**. The chip multiprocessor includes multiple processors **210–240** on a single die **290**. Similar to the processors **10–40** in system **100**, the processors **210–240** are connected to a single operating system **250** stored in a memory **260**. The processors **210–240** may communicate with the memory **260** via a bus **270**. System **200** conserves space by providing multiple processors on a single die. However, the systems **100** and **200** suffer from well known scalability problems.

Schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together. A well known limitation of this scheme and other multiprocessing schemes utilizing a single operating system is that an operating system does not scale well to large numbers of processors. That is, as the number of processors managed by a single operating system increases, the efficiency of the operating system goes down dramatically. For example, an operating system typically includes internal data structures that may be limited in the number of processors that can be supported, and limited bandwidth on a bus may slow transactions. Thus, scaling becomes impractical above some small number (e.g., currently about four to at most 64 processors, depending on the operating system in question).

Bugnion et al., in U.S. Pat. No. 6,075,938, discloses using a cache coherent non-uniform memory architecture (CC-NUMA) that supports multiple processors executing multiple operating systems. However, Bugnion et al. discloses multiple virtual processors, implemented in software on a single physical processor. This architecture fails to provide multiple physical processors, implemented in hardware, on a single die. Accordingly, this architecture suffers a perfor-

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mance penalty, because the single physical processor must task switch among multiple virtual processors (only one virtual processor can be running on the physical processor at any given time). Moreover, if this architecture were to support multiple physical processors, it would need space for providing multiple dies, and processing speed would consequently be sacrificed due to the input/output procedures needed to communicate among the multiple separate processors and the memory.

SUMMARY OF THE INVENTION

An aspect of the present invention is to provide a multiprocessing system including multiple processors mounted on a single die. The multiple processors are connected to a memory storing multiple operating systems. Each of the multiple processors may execute one of the multiple operating systems.

Another aspect of the present invention is to provide a multiprocessing system including a plurality of processor groups mounted on a single die. The processor groups are connected to a memory storing multiple operating systems. Each of the processor groups may execute one of the multiple operating systems. The processor group may include one or more processors mounted on the die.

Certain embodiments of the present invention are capable of achieving certain advantages, including some or all of the following: mounting multiple processors on a single die reduces the cabling problem inherent in connecting multiple processors on separate dies in separate housings; mounting multiple processors on a single die reduces the latency required for communication among the processors and improves the efficiency of message passing, potentially enabling a whole new class of applications (e.g., data mining) to run on such a multiprocessing system; mounting multiple processors on a single die reduces chip-to-chip communication costs and leads to further power efficiency; and increased scalability for multiprocessing.

Those skilled in the art will appreciate these and other advantages and benefits of various embodiments of the invention upon reading the following detailed description of a preferred embodiment with reference to the below-listed drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which like numeral references refer to like elements, and wherein:

FIG. 1 illustrates a conventional multiprocessing scheme including multiple processors, each on a separate die;

FIG. 2 illustrates a conventional multiprocessing scheme including multiple processors on a single die;

FIG. 3 illustrates an embodiment of a multiprocessing scheme employing the principles of the present invention; and

FIG. 4 illustrates another embodiment of a multiprocessing scheme employing the principles of the present invention.

**DETAILED DESCRIPTION OF THE
INVENTION**

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one of ordinary skill in the art that these specific details need not be used to practice the present invention. In

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other instances, well known structures, interfaces, and processes have not been shown in detail in order not to unnecessarily obscure the present invention.

FIG. 3 illustrates an embodiment including a computer system 300 employing the principles of the present invention. System 300 includes a chip multiprocessor 350 having multiple processors 305–320 mounted on a single die 360. The processors 305–320 function with operating systems 325–340 respectively, as illustrated by connections 345–348. The operating systems 325–340 are stored in a memory 365. During operation, each processor 305–320 may access a respective operating system 325–340 by communicating with the memory 365, for example, via a bus 370. Alternatively, each processor may be directly connected to the memory 365 without using the bus 370. The memory 365 may include one or more of the following: SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.

Processors 305–320 may be configured, such that each processor executes its own operating system. Multiple processors (e.g., multiple processors in a processor group) may also be configured to execute a single operating system. FIG. 4 illustrates a second embodiment including a computer system 400 employing the principles of the present invention. System 400 includes a chip multiprocessor 450 having multiple processors 405–420 mounted on a single die 460. The processors 405–420 are divided into two processor groups 425 and 430 having processors 405 and 410 in the processor group 425 and processors 415 and 420 in the processor group 430. The processor group 425 executes an operating system 435 stored in a memory 465 (as illustrated by a connection 475), and the processor group 430 executes an operating system 440 stored in the memory 465 (as illustrated by a connection 480). During operation, each processor group 425–430 may access a respective operating system 435–440 by communicating with the memory 465, for example, via a bus 470. Alternatively, each processor and/or processor group may be directly connected to the memory 465 without using the bus 470.

The operating systems shown in FIGS. 3–4 and described above may include conventional operating systems, such as WINDOWS NT, UNIX and the like, and the processors in systems 300 and 400 may include conventional processors. Each processor may be capable of executing a single operating system, or capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems. Systems 300 and 400 may be operable to execute a variety of applications, such as web service, database service and the like. Four processors are shown in FIGS. 3–4 for illustration purposes, and it will be apparent to one of ordinary skill in the art that more or less processors and/or processor groups may be included on the dies 360 and 460. Additionally, as is known in the art, the processors in systems 300 and 400 may access one or more caches (not shown).

It will be apparent to one of ordinary skill in the art that a system employing the principles of the present invention may be operable to support both processor groups and processors on a single die, such that each processor group and processor not within a processor group executes a distinct operating system.

Having each processor (or processor group) executing its own independent operating system minimizes scaling prob-

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lems realized when utilizing a single operating system with multiple processors. For example, one hundred processors independently executing one hundred operating systems may be no more of a problem than one processor executing one operating system. The embodiments described above are operable to provide this type of scaling on a single chip.

While this invention has been described in conjunction with the specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. There are changes that may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A multiprocessing system comprising:

multiple processors mounted on a single die; and
multiple operating systems residing in a memory connected to said multiple processors,

wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.

2. The system of claim 1, wherein at least one of said processors is operable to execute two or more of said multiple operating systems simultaneously.

3. The system of claim 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems.

4. The system of claim 1, wherein said multiple processors are directly connected to said memory to execute said multiple operating systems.

5. The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.

6. The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. A multiprocessing system comprising:

a plurality of processor groups mounted on a single die; and

multiple operating systems residing in a memory connected to said groups, wherein each of said groups executes an operating system of said multiple operating systems, and two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems.

8. The system of claim 7, wherein each of said groups includes multiple processors.

9. The system of claim 8, wherein said multiple processors in each of said groups are connected to said memory via a bus to execute said multiple operating systems.

10. The system of claim 8, wherein said multiple processors in each of said groups are directly connected to said memory to execute said multiple operating systems.

11. The system of claim 7, wherein each of said groups executes a distinct operating system of said multiple operating systems.

12. A multiprocessing apparatus comprising:

processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die, and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means; and

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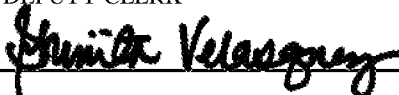
DOCKET NO. 6:21-cv-00169	DATE FILED 2/23/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS AMERICA, INC.,
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
2 6,724,241	4/20/2004	SONRAI MEMORY LIMITED
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT 8/11/2022 Order granting motion to dismiss (document #68).

CLERK Philip J. Devlin	(BY) DEPUTY CLERK 	DATE 08/12/2022
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DOCKET NO.	DATE FILED	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LTD.		DEFENDANT APPLE INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	4/20/2004	SONRAI MEMORY LTD.
2 6,724,241	3/29/2005	SONRAI MEMORY LTD.
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☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 22cv1606	DATE FILED 3/28/2022	U.S. DISTRICT COURT Northern District of Illinois
PLAINTIFF Sonrai Memory Limited		DEFENDANT Motorola Mobility LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		see attached
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DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK Thomas G. Bruton	(BY) DEPUTY CLERK Jannette Nunez	DATE 3/30/2022
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memory means for storing said plurality of operating system means.

13. The apparatus of claim 12, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

14. The apparatus of claim 12, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

15. The apparatus of claim 12, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

16. The apparatus of claim 12, wherein said processor means includes a plurality of processor group means,

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wherein each processor group means includes at least two of said plurality of processors.

17. The apparatus of claim 16, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

18. The apparatus of claim 16, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

19. The apparatus of claim 12, wherein at least one of said plurality of processors is operable to simultaneously execute two or more of said plurality of operating system means.

* * * * *

Exhibit 1



US006874014B2

(12) **United States Patent**
Richardson et al.

(10) **Patent No.:** **US 6,874,014 B2**
 (45) **Date of Patent:** **Mar. 29, 2005**

(54) **CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS**

(56) **References Cited**

U.S. PATENT DOCUMENTS

(75) Inventors: **Stephen E. Richardson**, Los Altos, CA (US); **Gary Vondran**, San Carlos, CA (US); **Stuart Siu**, Castro Valley, CA (US); **Paul Keltcher**, Sunnyvale, CA (US); **Shankar Venkataraman**, Cupertino, CA (US); **Padmanabha Venkitakrishnan**, Sunnyvale, CA (US); **Joseph Ku**, Palo Alto, CA (US)

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5,301,324 A	*	4/1994	Dewey et al.	718/105
5,446,841 A	*	8/1995	Kitano et al.	709/213
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6,075,938 A	*	6/2000	Bugnion et al.	703/27
6,108,731 A	*	8/2000	Suzuki et al.	710/301
6,314,501 B1	*	11/2001	Gulick et al.	711/153
6,526,462 B1	*	2/2003	Elabd	710/242
6,658,591 B1	*	12/2003	Arndt	714/6
6,772,241 B1	*	8/2004	George et al.	710/36

(73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 627 days.

* cited by examiner

Primary Examiner—Nasser Moazzami

(21) Appl. No.: **09/865,605**

(22) Filed: **May 29, 2001**

(65) **Prior Publication Data**

US 2002/0184328 A1 Dec. 5, 2002

(51) Int. Cl.⁷ **G06F 11/00**

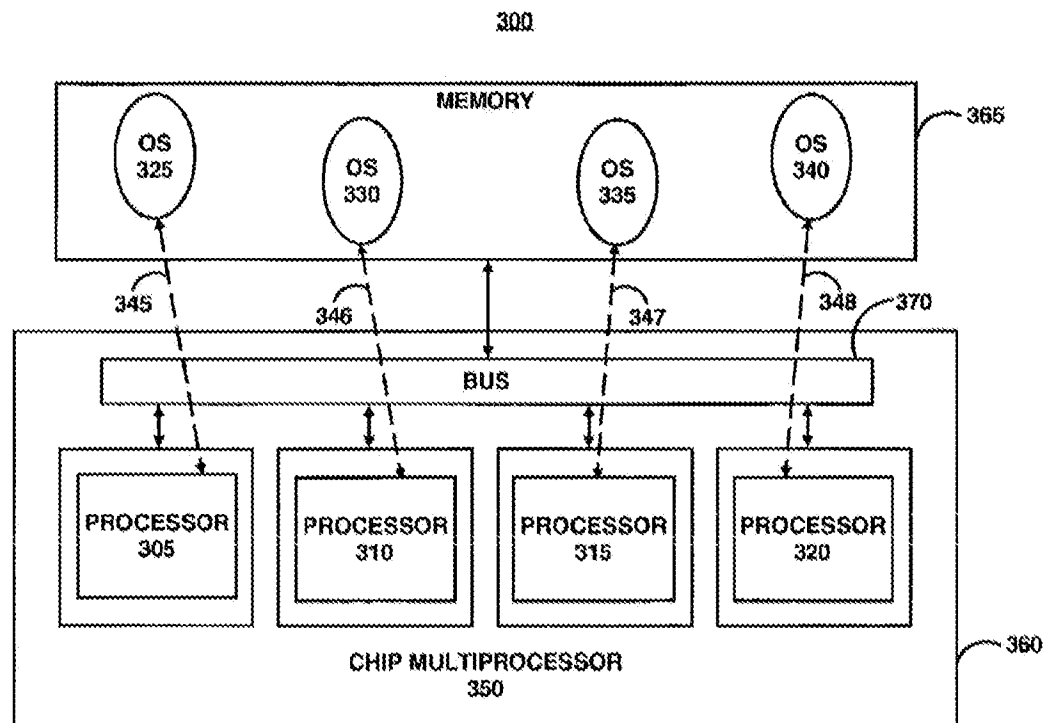
(52) U.S. Cl. **709/213; 709/222; 711/173; 713/2; 718/1; 719/313**

(58) Field of Search **709/220, 222, 709/213-215; 711/173, 147, 153; 713/2; 718/1, 105; 719/313; 714/6, 10**

(57) **ABSTRACT**

Multiple processors are mounted on a single die. The die is connected to a memory storing multiple operating systems or images of multiple operating systems. Each of the processors or a group of one or more of the processors is operable to execute a distinct one of the multiple operating systems. Therefore, resources for a single operating system may be dedicated to one processor or a group of processors. Consequently, a large number of processors mounted on a single die can operate efficiently.

19 Claims, 4 Drawing Sheets



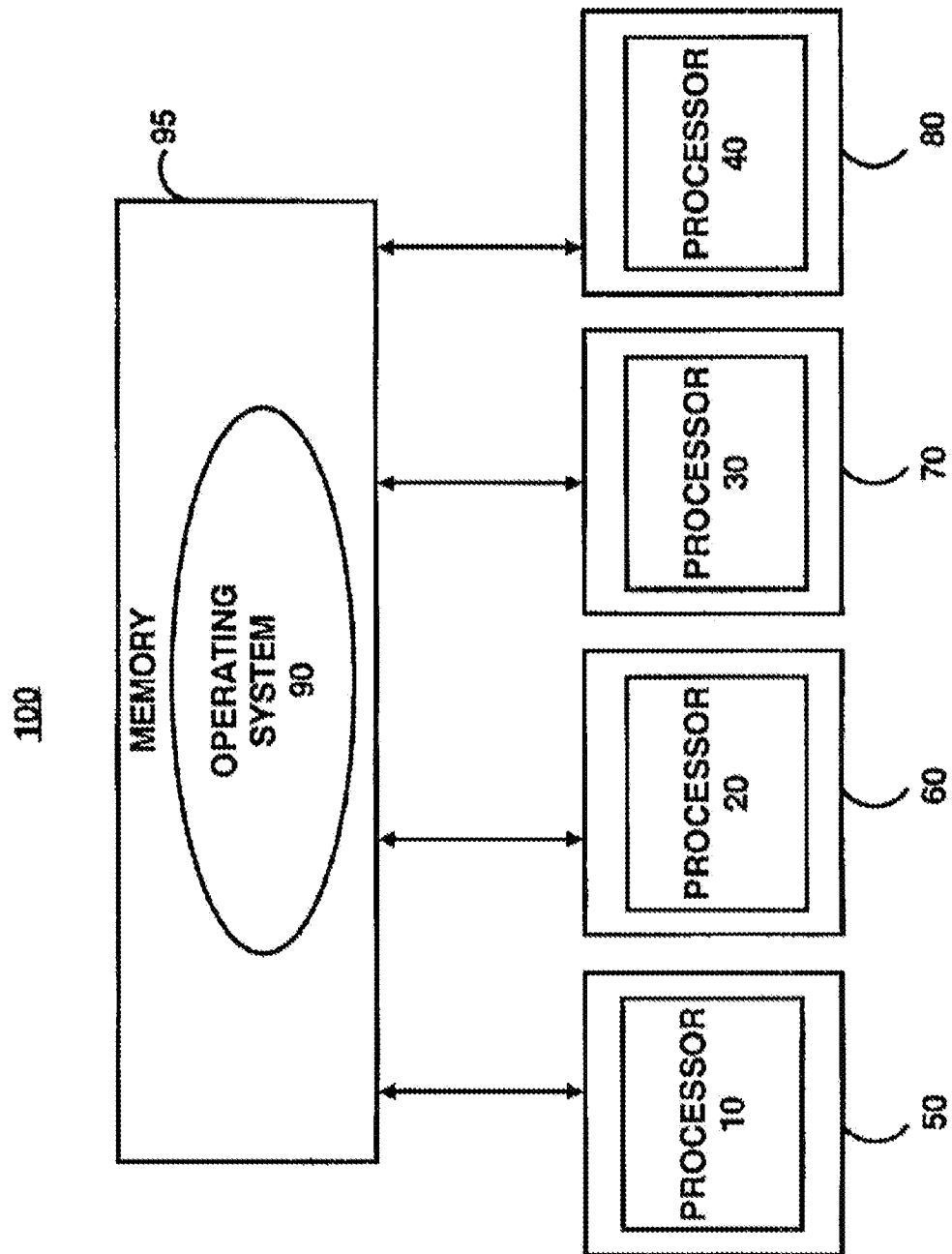


FIG. 1
Prior Art

U.S. Patent

Mar. 29, 2005

Sheet 2 of 4

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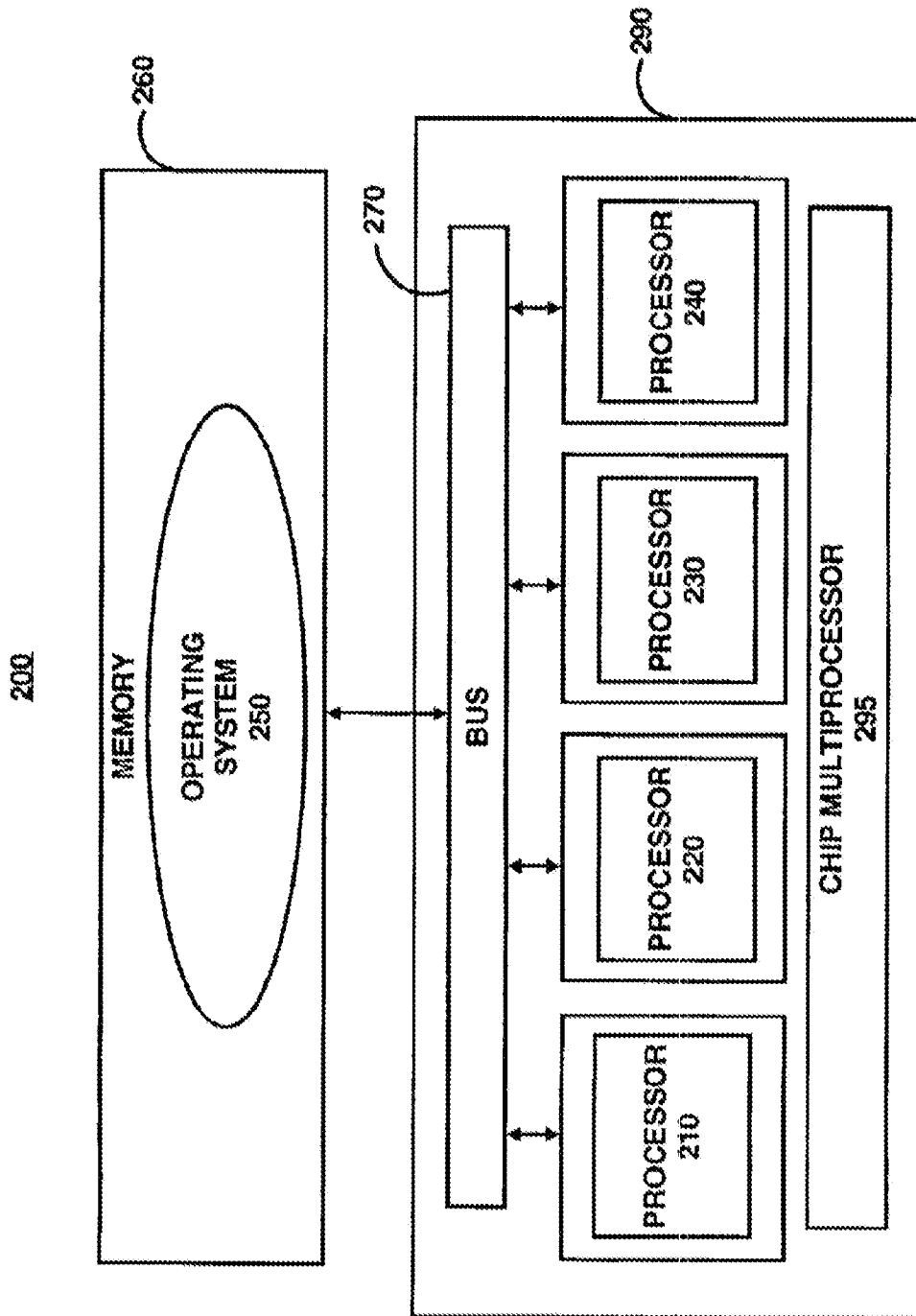


FIG. 2
Prior Art

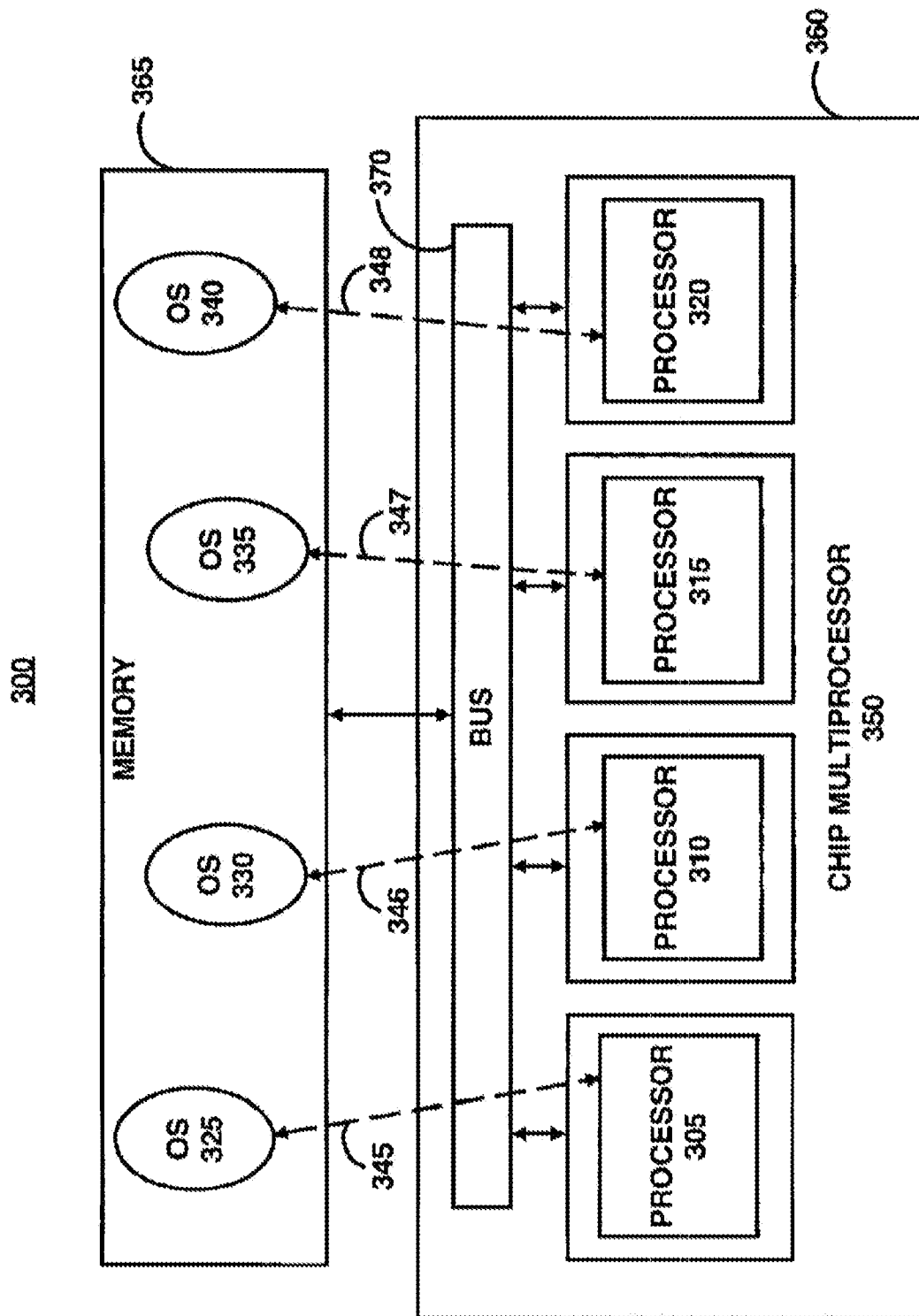


FIG. 3

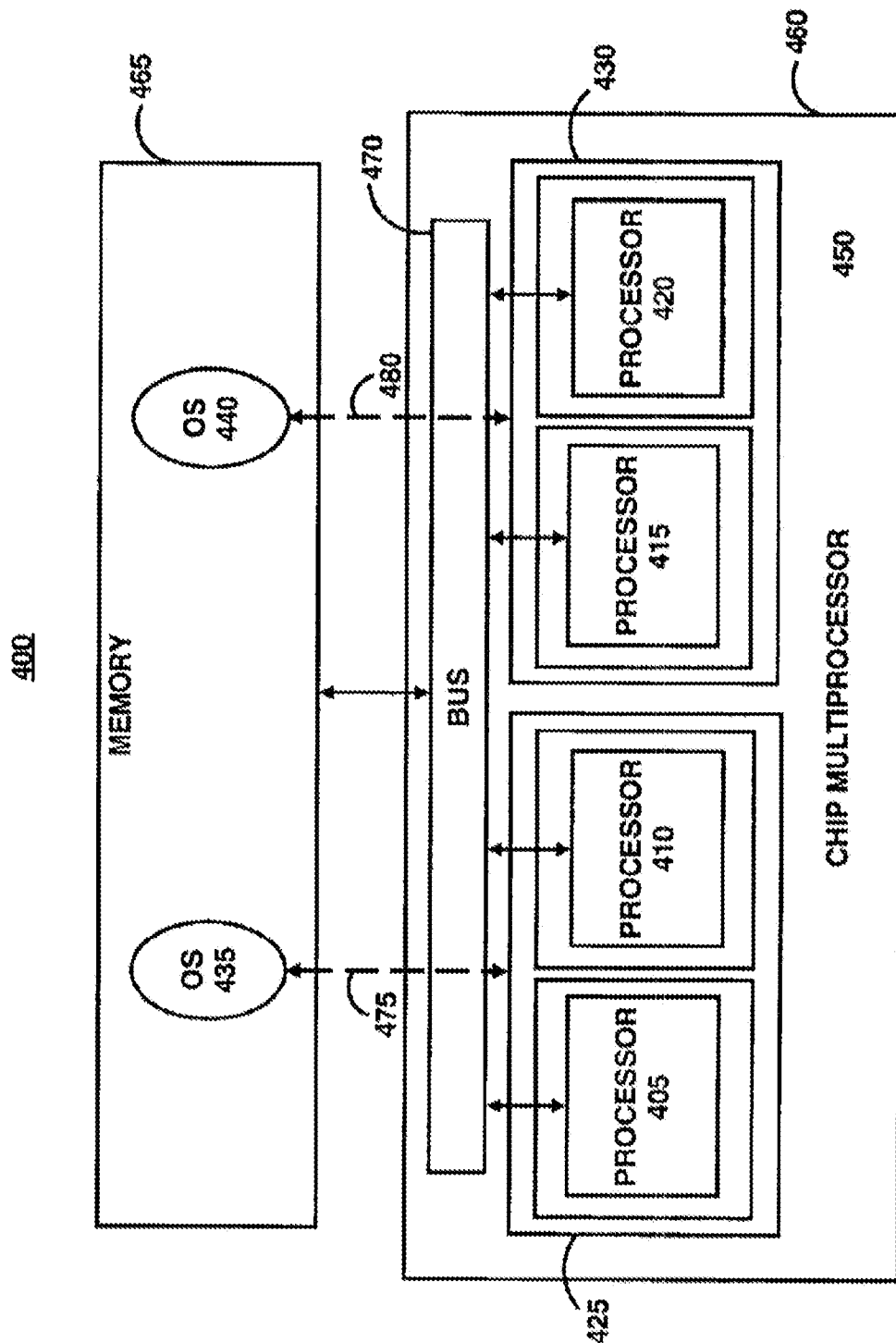


FIG. 4

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CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

FIELD OF THE INVENTION

The present invention is generally related to a computer chip architecture having multiple processors on a single die. More particularly, the present invention is related to a multiprocessing chip utilizing multiple operating systems.

BACKGROUND OF THE INVENTION

Existing internet data centers (IDCs) pack hundreds of processors (e.g., servers and the like) in a single building for processing a large volume of data transactions. Generally, the compute density or number of nodes per volume defines the efficiency of the IDC. The compute density effects the amortization of the high cost of the IDC infrastructure (e.g., networking, power, cooling, maintenance, reliability, and availability support). Typically, the greater the compute density, the better the IDC will be able to amortize the high cost of IDC infrastructure. Accordingly, a large compute density may be preferred. However, space may be unavailable or costly for locating a large number of processors necessary for maintaining a large compute density.

To provide increased compute density, multiprocessing schemes that utilize multiple processors have been developed. One conventional multiprocessing scheme (shown in FIG. 1) includes a computer system 100 having multiple processors 10-40, each on a separate die (i.e., chip) 50-80, and connected to a single operating system 90 stored in a memory 95. The system 100 may conserve space if the system is provided in a single housing.

A second conventional multiprocessing scheme (shown in FIG. 2) includes a computer system 200 having a chip multiprocessor 295. The chip multiprocessor includes multiple processors 210-240 on a single die 290. Similar to the processors 10-40 in system 100, the processors 210-240 are connected to a single operating system 250 stored in a memory 260. The processors 210-240 may communicate with the memory 260 via a bus 270. System 200 conserves space by providing multiple processors on a single die. However, the systems 100 and 200 suffer from well known scalability problems.

Schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together. A well known limitation of this scheme and other multiprocessing schemes utilizing a single operating system is that an operating system does not scale well to large numbers of processors. That is, as the number of processors managed by a single operating system increases, the efficiency of the operating system goes down dramatically. For example, an operating system typically includes internal data structures that may be limited in the number of processors that can be supported, and limited bandwidth on a bus may slow transactions. Thus, scaling becomes impractical above some small number (e.g., currently about four to at most 64 processors, depending on the operating system in question).

Bugnion et al., in U.S. Pat. No. 6,075,938, discloses using a cache coherent non-uniform memory architecture (CC-NUMA) that supports multiple processors executing multiple operating systems. However, Bugnion et al. discloses multiple virtual processors, implemented in software on a single physical processor. This architecture fails to provide multiple physical processors, implemented in hardware, on a single die. Accordingly, this architecture suffers a perfor-

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mance penalty, because the single physical processor must task switch among multiple virtual processors (only one virtual processor can be running on the physical processor at any given time). Moreover, if this architecture were to support multiple physical processors, it would need space for providing multiple dies, and processing speed would consequently be sacrificed due to the input/output procedures needed to communicate among the multiple separate processors and the memory.

SUMMARY OF THE INVENTION

An aspect of the present invention is to provide a multiprocessing system including multiple processors mounted on a single die. The multiple processors are connected to a memory storing multiple operating systems. Each of the multiple processors may execute one of the multiple operating systems.

Another aspect of the present invention is to provide a multiprocessing system including a plurality of processor groups mounted on a single die. The processor groups are connected to a memory storing multiple operating systems. Each of the processor groups may execute one of the multiple operating systems. The processor group may include one or more processors mounted on the die.

Certain embodiments of the present invention are capable of achieving certain advantages, including some or all of the following: mounting multiple processors on a single die reduces the cabling problem inherent in connecting multiple processors on separate dies in separate housings; mounting multiple processors on a single die reduces the latency required for communication among the processors and improves the efficiency of message passing, potentially enabling a whole new class of applications (e.g., data mining) to run on such a multiprocessing system; mounting multiple processors on a single die reduces chip-to-chip communication costs and leads to further power efficiency; and increased scalability for multiprocessing.

Those skilled in the art will appreciate these and other advantages and benefits of various embodiments of the invention upon reading the following detailed description of a preferred embodiment with reference to the below-listed drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which like numeral references refer to like elements, and wherein:

FIG. 1 illustrates a conventional multiprocessing scheme including multiple processors, each on a separate die;

FIG. 2 illustrates a conventional multiprocessing scheme including multiple processors on a single die;

FIG. 3 illustrates an embodiment of a multiprocessing scheme employing the principles of the present invention; and

FIG. 4 illustrates another embodiment of a multiprocessing scheme employing the principles of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one of ordinary skill in the art that these specific details need not be used to practice the present invention. In

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other instances, well known structures, interfaces, and processes have not been shown in detail in order not to unnecessarily obscure the present invention.

FIG. 3 illustrates an embodiment including a computer system 300 employing the principles of the present invention. System 300 includes a chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360. The processors 305-320 function with operating systems 325-340 respectively, as illustrated by connections 345-348. The operating systems 325-340 are stored in a memory 365. During operation, each processor 305-320 may access a respective operating system 325-340 by communicating with the memory 365, for example, via a bus 370. Alternatively, each processor may be directly connected to the memory 365 without using the bus 370. The memory 365 may include one or more of the following: SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.

Processors 305-320 may be configured, such that each processor executes its own operating system. Multiple processors (e.g., multiple processors in a processor group) may also be configured to execute a single operating system. FIG. 4 illustrates a second embodiment including a computer system 400 employing the principles of the present invention. System 400 includes a chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460. The processors 405-420 are divided into two processor groups 425 and 430 having processors 405 and 410 in the processor group 425 and processors 415 and 420 in the processor group 430. The processor group 425 executes an operating system 435 stored in a memory 465 (as illustrated by a connection 475), and the processor group 430 executes an operating system 440 stored in the memory 465 (as illustrated by a connection 480). During operation, each processor group 425-430 may access a respective operating system 435-440 by communicating with the memory 465, for example, via a bus 470. Alternatively, each processor and/or processor group may be directly connected to the memory 465 without using the bus 470.

The operating systems shown in FIGS. 3-4 and described above may include conventional operating systems, such as WINDOWS NT, UNIX and the like, and the processors in systems 300 and 400 may include conventional processors. Each processor may be capable of executing a single operating system, or capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems. Systems 300 and 400 may be operable to execute a variety of applications, such as web service, database service and the like. Four processors are shown in FIGS. 3-4 for illustration purposes, and it will be apparent to one of ordinary skill in the art that more or less processors and/or processor groups may be included on the dies 360 and 460. Additionally, as is known in the art, the processors in systems 300 and 400 may access one or more caches (not shown).

It will be apparent to one of ordinary skill in the art that a system employing the principles of the present invention may be operable to support both processor groups and processors on a single die, such that each processor group and processor not within a processor group executes a distinct operating system.

Having each processor (or processor group) executing its own independent operating system minimizes scaling prob-

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lems realized when utilizing a single operating system with multiple processors. For example, one hundred processors independently executing one hundred operating systems may be no more of a problem than one processor executing one operating system. The embodiments described above are operable to provide this type of scaling on a single chip.

While this invention has been described in conjunction with the specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. There are changes that may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A multiprocessing system comprising:

multiple processors mounted on a single die; and

multiple operating systems residing in a memory connected to said multiple processors,

wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.

2. The system of claim 1, wherein at least one of said processors is operable to execute two or more of said multiple operating systems simultaneously.

3. The system of claim 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems.

4. The system of claim 1, wherein said multiple processors are directly connected to said memory to execute said multiple operating systems.

5. The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.

6. The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. A multiprocessing system comprising:

a plurality of processor groups mounted on a single die; and

multiple operating systems residing in a memory connected to said groups, wherein each of said groups executes an operating system of said multiple operating systems, and two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems.

8. The system of claim 7, wherein each of said groups includes multiple processors.

9. The system of claim 8, wherein said multiple processors in each of said groups are connected to said memory via a bus to execute said multiple operating systems.

10. The system of claim 8, wherein said multiple processors in each of said groups are directly connected to said memory to execute said multiple operating systems.

11. The system of claim 7, wherein each of said groups executes a distinct operating system of said multiple operating systems.

12. A multiprocessing apparatus comprising:

processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die, and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means; and

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:22-cv-00029	DATE FILED 1/7/2022	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT LENOVO GROUP LTD.; MOTOROLA MOBILITY LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY	
	☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
Format m/d/yyyy TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT Notice of Voluntary Dismissal (document #11).

CLERK Jeannette J. Clack	(BY) DEPUTY CLERK <i>Shunika Velasquez</i>	DATE 03/28/2022
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
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Ex. 1004 - Page 51

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

GOOGLE LLC,
Petitioner,

v.

SONRAI MEMORY LIMITED,
Patent Owner.

IPR2021-01454
Patent 6,874,014 B2

Before GREGG I. ANDERSON, STACEY G. WHITE, and
JOHN D. HAMANN, *Administrative Patent Judges*.

HAMANN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Google LLC (“Petitioner”) filed a petition for *inter partes* review of claims 1–3, 5–9, 11–13, and 15–19 (“the challenged claims”) of U.S. Patent No. 6,874,014 B2 (Ex. 1001, “the ’014 patent”). Paper 1 (“Pet.”). Sonrai Memory Limited (“Patent Owner”) did not file a Preliminary Response.

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018); *see* 37 C.F.R. § 42.108 (2020). Upon consideration of the papers, we conclude that the information presented shows that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one challenged claim of the ’014 patent.

A. *Real Parties-in-Interest*

The parties identify themselves as the real parties-in-interest. Pet. 1; Paper 5, 1. In addition, Petitioner states that it “is a subsidiary of XXVI Holdings Inc., which is a subsidiary of Alphabet Inc.,” and that “XXVI Holdings Inc. and Alphabet Inc. are not real parties-in-interest to this proceeding.” Pet. 1 n.1.

B. *Related Matters*

The parties collectively identify the following as matters that may affect, or be affected by, a decision in this proceeding: (i) *Sonrai Memory Ltd. v. Google LLC*, 6-21-cv-00167 (W.D. Tex.); (ii) *Sonrai Memory Ltd. v. LG Electronics Inc.*, 6-21-cv-00168 (W.D. Tex.); (iii) *Sonrai Memory Ltd. v. Samsung Electronics Co., Ltd.*, Case No. 6: 21-cv-00169-ADA (W.D. Tex.); and (iv) *Sonrai Memory Limited v. Amazon.com, Inc.*, Case No. 6:21-cv-00991-ADA (W.D. Tex.). Pet. 1; Paper 5, 1.

C. The Challenged Patent

The '014 patent “is generally related to a computer chip architecture having multiple processors on a single die,” and “[m]ore particularly, . . . is related to a multiprocessing chip utilizing multiple operating systems.”

Ex. 1001, 1:6–9. The '014 patent teaches having multiple processors mounted on a single die, which “is connected to a memory storing multiple operating systems.” *Id.* at code (57). “Each of the processors or a group of one or more of the processors is operable to execute a distinct one of the multiple operating systems.” *Id.* “Therefore, resources for a single operating system may be dedicated to one processor or a group of processors.” *Id.* “Consequently, a large number of processors mounted on a single die can operate efficiently,” according to the '014 patent. *Id.*

Figure 3, shown below, “illustrates an embodiment of a multiprocessing scheme,” in accordance with the '014 patent. *Id.* at 2:54–55.

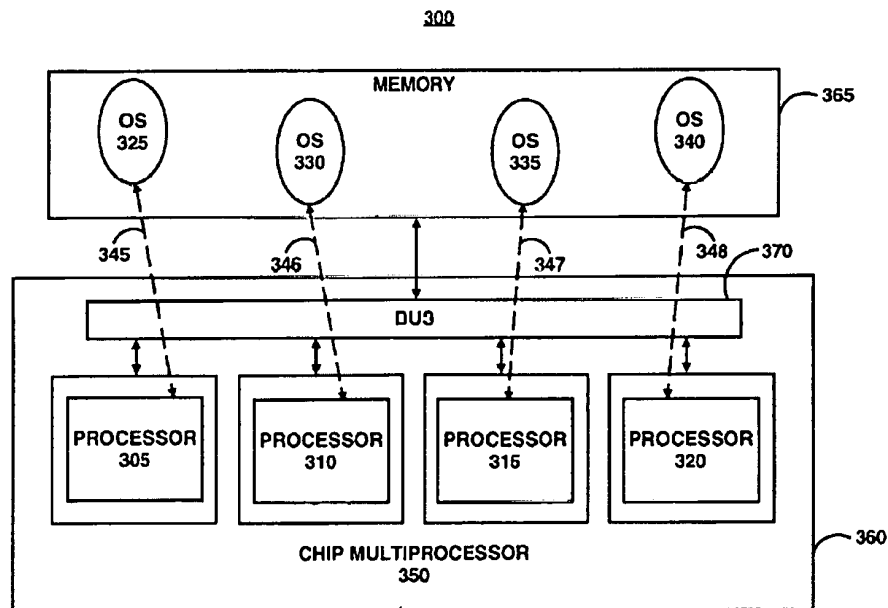


FIG. 3

Figure 3 “illustrates an embodiment including a computer system 300 employing the principles of the” ’014 patent. *Id.* at 3:4–6. As illustrated, “[s]ystem 300 includes a chip multiprocessor 350 having multiple processors 305–320 mounted on a single die 360.” *Id.* at 3:6–7, Fig. 3. “The processors 305–320 function with operating systems 325–340 respectively, as illustrated by connections 345–348.” *Id.* at 3:8–10. “The operating systems 325–340 are stored in a memory 365.” *Id.* at 3:10–11. The ’014 patent discloses that “[d]uring operation, each processor 305–320 may access a respective operating system 325–340 by communicating with the memory 365, for example, via a bus 370.” *Id.* at 3:11–15.

The ’014 patent discloses that “[p]rocessors 305–320 may be configured, such that each processor executes its own operating system,” or “[m]ultiple processors (e.g., multiple processors in a processor group) may . . . be configured to execute a single operating system.” *Id.* at 3:21–24. Moreover, “[e]ach processor may be capable of executing a single operating system, or capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems.” *Id.* at 3:46–50.

D. The Challenged Claims

Petitioner challenges claims 1–3, 5–9, 11–13, and 15–19 of the ’014 patent. Claims 1, 7, and 12 are independent claims. Claim 1 is illustrative of the challenged claims and is reproduced below:

1. A multiprocessing system comprising:
 - multiple processors mounted on a single die; and
 - multiple operating systems residing in a memory connected to said multiple processors,
 - wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously

executing two or more operating systems of said multiple operating systems.

Ex. 1001, 4:14–22.

E. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims of the '014 patent are unpatentable based on the following grounds:

Claim(s) Challenged	35 U.S.C. § ¹	Reference(s)/Basis
1–3, 5–9, 11–13, 15–19	103(a)	Asano, ² Joy ³
1–3, 5–9, 11–13, 15–19	103(a)	Asano, Babaian ⁴

Pet. 2–3, 12–73. Petitioner submits in support of its arguments the Declaration of Dr. Martin Walker (Ex. 1002).

II. LEVEL OF ORDINARY SKILL IN THE ART

To determine whether an invention would have been obvious at the time it was made, we consider the level of ordinary skill in the pertinent art at the time of the invention. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). In assessing the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995)

¹ The Leahy-Smith America Invents Act (“AIA”) included revisions to 35 U.S.C. § 103 that became effective on March 16, 2013. Because the '014 patent issued from an application filed before March 16, 2013, we apply the pre-AIA version of the statutory basis for unpatentability.

² US 2001/0044817 A1, published Nov. 22, 2001 (Ex. 1005, “Asano”).

³ US 6,542,991 B1, issued Apr. 1, 2003 (Ex. 1006, “Joy”).

⁴ US 7,143,401 B2, issued Nov. 28, 2006 (Ex. 1007, “Babaian”).

(citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962–63 (Fed. Cir. 1986)). “[O]ne or more factors may predominate.” *Id.*

Petitioner argues that one of ordinary skill in the art “would have had an undergraduate degree in electrical engineering, computer engineering, computer science, or a related field along with at least two years of work experience in the field of computer processor architecture.” Pet. 3–4 (citing Ex. 1002 ¶¶ 15–17). Petitioner adds that “[m]ore education can supplement practical experience and vice versa.” *Id.* at 4 (citing Ex. 1002 ¶¶ 15–17).

For purposes of this Decision, and based on the current record, we adopt Petitioner’s assessment of the level of skill for one of ordinary skill in the art. This assessment is consistent with the ’014 patent and the asserted prior art, and we apply it in our analysis below.

III. CLAIM CONSTRUCTION

Because the Petition was filed after November 13, 2018, we apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b), following the standard articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b); 83 Fed. Reg. 51,340, 51,340–41, 51,343 (Oct. 11, 2018). In applying such standard, claim terms generally are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art, at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. “In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner does not identify any claim terms that we need to construe in order to determine whether to institute an *inter partes* review. Pet. 10–12. Thus, at this stage of the proceeding, we do not provide any express constructions, and we afford the claim terms relevant to our analysis below their plain and ordinary meaning. *See, e.g., Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’”).

IV. PRINCIPLES OF LAW

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of non-obviousness, if present. *See Graham*, 383 U.S. at 17–18. When evaluating a claim for obviousness, we also must “determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.” *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

V. ALLEGED OBVIOUSNESS OVER ASANO AND JOY

Petitioner argues that the combination of Asano and Joy renders claims 1–3, 5–9, 11–13, and 15–19 of the ’014 patent obvious. Pet. 12–54. Patent Owner did not file a Preliminary Response, and thus, at this stage in

the proceeding, Patent Owner does not address Petitioner’s arguments and evidence. We focus on challenged claim 1, which is illustrative of the challenged claims, for the analysis we provide below. For the reasons that follow, we determine that Petitioner establishes a reasonable likelihood that it would prevail in showing that the combination of Asano and Joy renders at least claim 1 obvious.

A. Summary of Asano

Asano “relates to . . . controlling a computer system in which a plurality of operating systems . . . operate on one computer, and in particular, to . . . controlling a computer system in which computer resources can be efficiently used or operated in an operating state of a plurality of operating systems.” Ex. 1005 ¶ 1. Figure 1, shown below, illustrates Asano’s teachings. *Id.* ¶ 30.

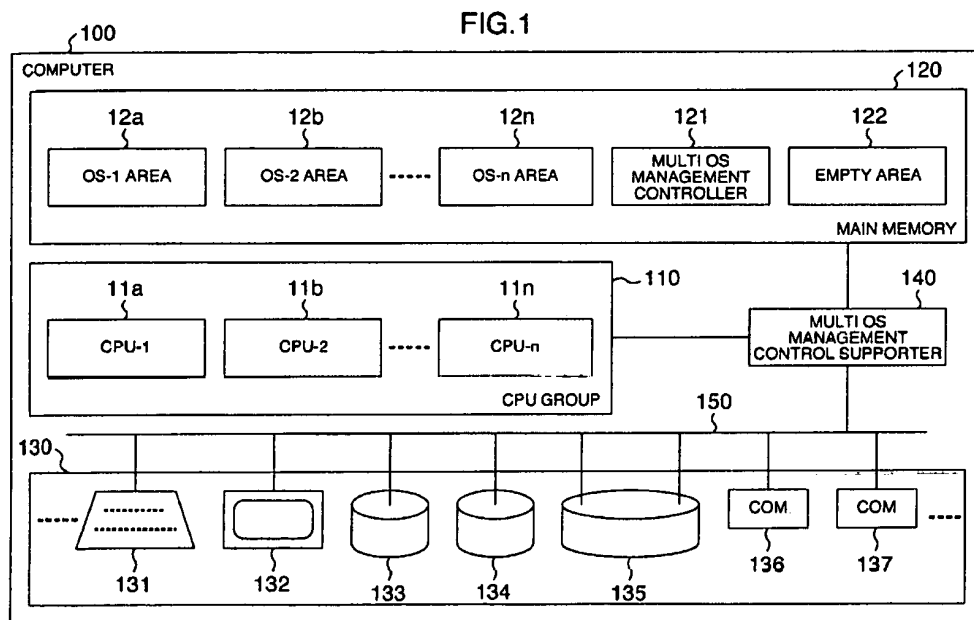


Figure 1 illustrates the structure of an embodiment of a computer system, in accordance with Asano’s teachings. *Id.* As illustrated, “a computer system 100 includes a processor group 110, a main memory 120, an external input/output device group 130, a multiple operating system (multi OS)

management control supporter 140, and a bus 150 establishing connections between the constituent components.” *Id.* ¶ 30, Fig. 1. “The processor group 110 is a set of one or more processors (CPUs) and includes processors 11a, 11b . . . , 11n.” *Id.* ¶ 31. “The main memory 120 includes main memory areas 12a to 12n independent of each other,” and which “are allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n).” *Id.* “The main memory 120 further includes a main storage area 121 for the multiple operating system management controller” *Id.* “The external device group 130 includes an input keyboard 131, an output display 132, external storages 133 to 135 for respective operating systems, and communicating devices 136 and 137, and other devices, not shown.” *Id.* “To enable one computer system to execute a plurality of operating systems, the supporter 140 intervenes between the processor group 110, the main memory 120, and the external device group 130 of the computer system 100.” *Id.*

B. Summary of Joy

Joy relates to “multiple-threading processor architectures and methods of operation and execution.” Ex. 1006, 1:36–39. More specifically, Joy teaches that “[a] processor reduces wasted cycle time resulting from stalling and idling, and increases the proportion of execution time, by supporting and implementing both vertical multithreading and horizontal multithreading.” *Id.* at 2:17–20. Joy teaches that “[i]n vertical multithreading, multiple hardware threads share the same processor pipeline,” and “[h]orizontal multithreading increases parallelism within the processor circuit structure, for example within a single integrated circuit die that makes up a single-chip processor.” *Id.* at 2:22–28. According to Joy, “[t]o further increase system parallelism in some processor embodiments, multiple processor cores are

formed in a single die.” *Id.* at 2:29–31. For example, “[a] horizontal threaded processor, using a technique called chip-multiple processing, combines multiple processors on a single integrated circuit die,” according to Joy. *Id.* at 7:4–6. Joy teaches that “[t]he multiple processors are vertically threaded to form a processor with both vertical and horizontal threading, augmenting executing efficiency and decreasing latency in a multiplicative fashion.” *Id.* at 7:6–9.

C. Challenged Claim 1

1. A Multiprocessing System (Preamble)

Petitioner argues that Asano teaches “[a] multiprocessing system,” as recited in the preamble of claim 1. Pet. 12–13. More specifically, Petitioner argues that Asano teaches a computer system that includes a processor group 110 for executing a plurality of operating systems. *Id.* (citing Ex. 1005 ¶¶ 1, 30–31, Fig. 1). Petitioner adds that “[t]he processor group 110 is a set of one or more processors (CPUs) and includes processors 11a, 11b . . . , 11n.” *Id.* at 13 (quoting Ex. 1005 ¶ 31). According to Petitioner, one of ordinary skill in the art “would have thus understood that *Asano*’s computer system is a multiprocessing system, as claimed because the system includes multiple processors (e.g., processors 11a through 11n).” *Id.* (citing Ex. 1002 ¶ 58).

After reviewing Petitioner’s arguments and evidence, which are not addressed by Patent Owner at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that Asano teaches “[a] multiprocessing system.” In light of our finding, we need not, and thus do not, reach whether claim 1’s preamble is limiting.

2. Multiple Processors

Petitioner argues that the combination of Asano and Joy teaches “multiple processors mounted on a single die,” as recited in claim 1. Pet.

14–23. More specifically, Petitioner argues that Asano teaches a “computer system that includes a processor group 110 that includes multiple processors.” *Id.* at 14 (citing Ex. 1005 ¶¶ 30–31); *see also id.* (citing Ex. 1005 ¶ 31, Fig. 1 (annotating processors 11a, 11b . . . 11n); Ex. 1002 ¶ 60). As to Joy, Petitioner argues that Joy teaches having “multiple processors mounted on a single die.” *Id.* at 15 (citing Ex. 1002 ¶¶ 51–53, 62); *see also id.* (citing Ex. 1006, 2:17–32, 7:4–6) (arguing same).

Petitioner argues that “it would have been obvious to implement *Asano*’s computer system with multiple processors *mounted on a single die* based on the teachings and suggestions of *Joy* and the knowledge of” one of ordinary skill in the art. *Id.* at 14 (citing Ex. 1002 ¶ 61). According to Petitioner, “[s]uch an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results.” *Id.* at 18 (citation omitted). In particular, Petitioner argues that “the benefits of having multiple processors on a single die in a multi-processor system (such as the system in *Asano*) were well known in the art before the ’014 patent.” *Id.* at 19 (citing Ex. 1002 ¶ 72); *see also id.* at 20–21 (citing Ex. 1008,⁵ 1; Ex. 1009,⁶ Abstract; Ex. 1010,⁷ 1:37–60; Ex. 1011,⁸ 292); *id.* at 21 (citing Ex. 1001, 1:34–44, Fig. 2; Ex. 1002 ¶ 72) (arguing that the ’014 patent admits that “using multiple

⁵ Alan Joch, *HOW-TO Chip Multiprocessing*, COMPUTERWORLD, Nov. 27, 2000.

⁶ Kunle Olukotun et al., *The Case for a Single-Chip Multiprocessor*, ACM SIGPLAN Notices, vol. 31, issue 9, Sept. 1996.

⁷ US 6,550,020 B1, issued Apr. 15, 2003.

⁸ Luiz André Barroso et al., *Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing*, Proc. 27th ACM Int’l Symp. Computer Architecture, 2000.

processors mounted on a single die in a computer system as conventional and beneficial”).

Moreover, Petitioner argues that one of ordinary skill in the art “would have . . . recognized that implementing *Joy*’s teachings regarding the multiple processors combined on a single integrated circuit die in *Asano* would have allowed the combined system to allocate (via context switching) each processor from an operating system to another operating system at nanosecond speeds.” *Id.* at 19 (citing Ex. 1006, 7:49–54; Ex. 1002 ¶ 70).

After reviewing Petitioner’s arguments and evidence, which are not addressed by Patent Owner at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that the combination of *Asano* and *Joy* teaches “multiple processors mounted on a single die.” We also find, at this stage of the proceeding, that Petitioner has provided sufficiently articulated reasoning with rational underpinning to support Petitioner’s combining of *Asano* and *Joy* for this limitation. *See Kahn*, 441 F.3d at 988, *cited with approval in KSR*, 550 U.S. at 418.

3. Multiple Operating Systems

Petitioner argues that the combination of *Asano* and *Joy* teaches “multiple operating systems residing in a memory connected to said multiple processors,” as recited in claim 1. Pet. 23–26. More specifically, Petitioner argues that *Asano* teaches “that the computer system 100 includes a main memory 120 (‘memory’),” which “‘includes main memory areas 12a to 12n’ that are ‘allocated respectively to operating systems, i.e., operating system 1 (OS-1) to operating system n (OS-n).’” *Id.* at 23 (citing Ex. 1005 ¶¶ 30–31, Fig. 1); *see also id.* at 24 (citing Ex. 1005, Fig. 1) (highlighting in yellow OS-1 to OS-n and highlighting in blue main memory 120). Petitioner argues that thus one of ordinary skill in the art “would have understood that the

multiple operating systems (e.g., OS-1 to OS-n) reside in memory 120.” *Id.* at 23 (citing Ex. 1002 ¶ 77).

In addition, Petitioner argues that Asano teaches “that the memory 120 is connected to the multiple processors.” *Id.* at 24 (citing Ex. 1002 ¶ 78). More specifically, Petitioner argues that “the computer system 100 includes a bus 150 . . . connecting the processor group 110 . . . , which includes multiple processors (e.g., CPU-1 to CPU-n), and the main memory 120.” *Id.* (citing Ex. 1005 ¶¶ 30–31, Fig. 1). Petitioner adds that “[t]he system further includes a multiple operating system management (multi-OS) control supporter 140 . . . that ‘allocate[s] computer resources to the operating system.’” *Id.* (citing Ex. 1005 ¶ 31, code (57)) (third alteration in original). According to Petitioner, one of ordinary skill in the art “would have thus understood that the multiple operating systems residing in memory 120 are connected to the multiple processors in the processor group 110.” *Id.* at 25 (Ex. 1002 ¶ 80).

After reviewing Petitioner’s arguments and evidence, which are not addressed by Patent Owner at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that the combination of Asano and Joy teaches “multiple operating systems residing in a memory connected to said multiple processors.”

4. Wherein Each of Said Multiple Processors

Petitioner argues that the combination of Asano and Joy teaches “wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as recited in claim 1. Pet. 26–32. More specifically, Petitioner argues that Asano teaches “that each of the

processors is allocated to execute an operating system.” *Id.* at 26 (citing Ex. 1002 ¶ 84). According to Petitioner, Asano teaches, for example, “that the computer system 100 includes a processor group 110 that interacts with a multi-OS control supporter 140 to operate (‘execute’) a plurality of operating systems, OS-1 to OS-n.” *Id.* at 26–27 (citing Ex. 1005 ¶¶ 30–31).

Petitioner adds that Asano’s Figure 2 “illustrates one configuration of the system shown in Figure 1 where two operating systems, OS-1 and OS-2 . . . , are simultaneously running in the computer system 100.” *Id.* at 27 (Ex. 1005 ¶¶ 32–33). More specifically, Petitioner argues that Asano teaches “that processor group 110 is divided into two groups (CPU group 221 and 222 . . .),” and that “[t]hese CPU groups are each allocated to run at least one operating system.” *Id.* at 27–28 (citing Ex. 1005 ¶¶ 32–33, 35, Fig. 2). According to Petitioner, one of ordinary skill in the art “would have understood that the allocation of the processors to the first and second operating systems would have resulted in processors executing the operating systems.” *Id.* at 28 (citing Ex. 1002 ¶ 85; Ex. 1005 ¶¶ 1, 35).

In addition, Petitioner argues that Asano teaches that the “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.” *Id.* (citing Ex. 1002 ¶ 86). Petitioner argues that Asano teaches, for example, “a method of allocating the processors to simultaneously execute multiple operating systems where each CPU within a given CPU group ‘is allocated to another operating system at a predetermined interval of time.’” *Id.* (quoting Ex. 1005 ¶ 35). According to Petitioner, one of ordinary skill in the art “would have understood that this allocation of each of the processors to another operating system is a switching mechanism that provides each processor the capability to switch between multiple operating systems,

which are simultaneously running in the system.” *Id.* (citing Ex. 1002 ¶ 86). Petitioner argues that “[t]he ’014 patent describes a similar process, where ‘[e]ach processor may be ... capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems.’” *Id.* at 28–29 (quoting Ex. 1001, 3:46–51; citing Ex. 1002 ¶ 87; Ex. 1005 ¶ 35) (second and third alterations in original).

After reviewing Petitioner’s arguments and evidence, which are not addressed by Patent Owner at this stage of the proceeding, we are persuaded that Petitioner demonstrates, for purposes of this institution decision, that the combination of Asano and Joy teaches “wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.”

5. *Summary*

In summary, based on the current record, and for purposes of this institution decision, we determine that Petitioner shows a reasonable likelihood that it would prevail in showing that claim 1 would have been obvious to one of ordinary skill in the art in view of Asano and Joy.

D. Challenged Claims 2, 3, 5–9, 11–13, and 15–19

At this stage in the proceeding, Patent Owner does not address Petitioner’s arguments and evidence, as to how the combination of Asano and Joy teaches the limitations of claims 2, 3, 5–9, 11–13, and 15–19. We have reviewed Petitioner’s arguments and evidence regarding these claims, and, on the current record, we find them persuasive for purposes of institution.

VI. ALLEGED OBVIOUSNESS OVER ASANO AND BABAIAN

Petitioner argues that the combination of Asano and Babaian renders claims 1–3, 5–9, 11–13, and 15–19 obvious. Pet. 3, 55–73. At this stage in the proceeding, Patent Owner does not address Petitioner’s arguments and evidence as to how the combination of Asano and Babaian teaches the limitations of these claims. We have reviewed Petitioner’s arguments and evidence regarding these claims, and, on the current record, we find them persuasive for purposes of institution.

VII. CONCLUSION

For the foregoing reasons, we determine that Petitioner has demonstrated that there is a reasonable likelihood that it would prevail in proving the unpatentability of at least one of the challenged claims of the ’014 patent. We thus institute an *inter partes* review of all of the challenged claims of the ’014 patent on all grounds asserted in the Petition. *See* 37 C.F.R. § 42.108(a).

Any findings or conclusions in this Decision are made only for the purposes of institution and are not dispositive of any issue. We have not made a final determination with respect to the patentability of any challenged claim. Our final determination will be based on the record as fully developed during trial, including any evidence or argument timely presented by the parties under our Rules.

VIII. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '014 patent is instituted on all of the challenged claims and all grounds asserted in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial commences on the entry date of this Decision.

IPR2021-01454
Patent 6,874,014 B2

For PETITIONER:

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For PATENT OWNER:

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AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:22-cv-00029	DATE FILED 1/7/2022	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT LENOVO GROUP LTD.; MOTOROLA MOBILITY LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY	
	☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
Format m/d/yyyy TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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AO 120 (Rev. 08/10)

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filed in the U.S. District Court Western District of Texas on the following

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DOCKET NO. 6:21-cv-1066	DATE FILED 10/13/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT TEXAS INSTRUMENTS INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Western District of Texas on the following

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DOCKET NO. 6:21-cv-991	DATE FILED 9/24/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT AMAZON.COM, INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,724,241	4/20/2004	SONRAI MEMORY LIMITED
2 6,829,691	12/7/2004	SONRAI MEMORY LIMITED
3 6,874,014	3/19/2005	SONRAI MEMORY LIMITED
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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
filed in the U.S. District Court Western District of Texas on the following

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DOCKET NO. 6:21-cv-00168	DATE FILED 2/23/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT LG ELECTRONICS INC.; LG ELECTRONICS U.S.A., INC.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
2 6,724,241	4/20/2004	SONRAI MEMORY LIMITED
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-00167	DATE FILED 2/23/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT GOOGLE, LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
2 6,724,241	4/20/2004	SONRAI MEMORY LIMITED
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In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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AO 120 (Rev. 08/10)

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DOCKET NO. 6:21-cv-00169	DATE FILED 2/23/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF SONRAI MEMORY LIMITED		DEFENDANT SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS AMERICA, INC.,
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 6,874,014	3/29/2005	SONRAI MEMORY LIMITED
2 6,724,241	4/20/2004	SONRAI MEMORY LIMITED
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DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
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DECISION/JUDGEMENT

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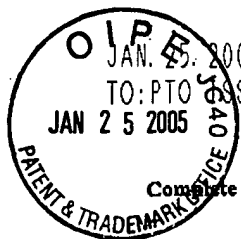
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JEFFANY TURNER (Depositor's name)
(Signature)
1-25-05 (Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,605	05/29/2001	Stephen E. Richardson	10013654-1	4135

TITLE OF INVENTION: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

APPL. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	03/21/2005
EXAMINER	ART UNIT	CLASS-SUBCLASS			
MOAZZAMI, NASSER, G	2187	709-213000			

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Houston, Texas

Hewlett-Packard Development Company, LP.

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 1

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 08-2025 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant, a registered attorney or agent, or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Richard P. Lange
RICHARD P. LANGE

Date 1-25-05

Typed or printed name

Registration No. 27,296

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PTOL-85 (Rev. 11/04) Approved for use through 04/30/2007.

OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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01 FC:1501 1400.00 DA
02 FC:1504 300.00 DA
03 FC:8001 3.00 DA

PAGE 1/1 * RCVD AT 1/25/2005 2:02:22 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-2/3 * DNIS:7464000 * CSID:6508575487 * DURATION (mm-ss):00:46



UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

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EXAMINER

MOAZZAMI, NASSER G

ART UNIT PAPER NUMBER

2187

DATE MAILED: 12/21/2004

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,605	05/29/2001	Stephen E. Richardson	10013854-1	4135

TITLE OF INVENTION: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	03/21/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. **PROSECUTION ON THE MERITS IS CLOSED.** THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN **THREE MONTHS** FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. **THIS STATUTORY PERIOD CANNOT BE EXTENDED.** SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail**

**Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (703) 746-4000**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 12/21/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (703) 746-4000, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,605	05/29/2001	Stephen E. Richardson	10013854-1	4135

TITLE OF INVENTION: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	03/21/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
MOAZZAMI, NASSER G	2187	709-213000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,605	05/29/2001	Stephen E. Richardson	10013854-1	4135

7590 12/21/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

MOAZZAMI, NASSER G

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 12/21/2004

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 627 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 627 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (703) 305-1383. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

Notice of Allowability

Applicant No.

09/865,605

Examiner

Nasser G Moazzami

Applicant(s)

RICHARDSON ET AL.

Art Unit

2187

-- **The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 11/24/2004.
2. ☒ The allowed claim(s) is/are 1-8 and 10-20 now renumbered to 1-19.
3. ☒ The drawings filed on 05/29/2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

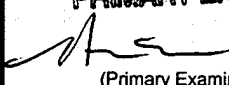
5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

NASSER MOAZZAMI
PRIMARY EXAMINER

Issue Classification *0986560 5*	Applicati n No. 09/865,605	Applicant(s) RICHARDSON ET AL.	
	Examiner Nasser G Moazzami	Art Unit 2187	

ISSUE CLASSIFICATION									
ORIGINAL				CROSS REFERENCE(S)					
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
709		213		709	222				
INTERNATIONAL CLASSIFICATION				711	173				
G	O	G	F	713	2				
				718	1				
				719	313				
(Assistant Examiner) (Date) <i>Ernest Williams</i> 12-15-04 (Legal Instruments Examiner) (Date)				NASSER MOAZZAMI PRIMARY EXAMINER  (Primary Examiner)			Total Claims Allowed: 19 O.G. Print Claim(s) 1 O.G. Print Fig. 3		

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91
2	2		32		62		92
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UNITED STATES PATENT AND TRADEMARK OFFICE

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BIBDATASHEET**CONFIRMATION NO. 4135**

Bib Data Sheet

SERIAL NUMBER 09/865,605	FILING DATE 05/29/2001 RULE	CLASS 709	GROUP ART UNIT 2187	ATTORNEY DOCKET NO. 10013854-1
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APPLICANTS

Stephen E. Richardson, Los Altos, CA;

Gary Lee Vondan JR., San Carlos, CA;
Stuart C. Siu, Castro Valley, CA; Paul Keltcher, Sunnyvale, CA;
Shankar Venkataraman, Cupertino, CA;
Padmanabha I. Venkitakrishnan, Sunnyvale, CA;
Joseph Weiyeh Ku, Palo Alto, CA;

N.H.
** CONTINUING DATA *****

N.H.
** FOREIGN APPLICATIONS *****

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 07/24/2001

Foreign Priority claimed 35 USC 119 (a-d) conditions met	☐ yes ☒ no ☐ yes ☒ no ☐ Met after Allowance	STATE OR COUNTRY CA	SHEETS DRAWING 4	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
Verified and Acknowledged	<i>N.H.</i> Examiner's Signature Initials				

ADDRESS

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO
80527-2400

TITLE

Chip multiprocessor with multiple operating systems

FILING FEE	FEES: Authority has been given in Paper	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (...)
RECEIVED	No. _____ to charge/credit DEPOSIT ACCOUNT	
	No. _____ for following:	

Apple

Index of Claims

09865605

Applicati n No.

09/865,605

Examin r

Nasser G Moazzami

Applicant(s)

RICHARDSON ET AL.

Art Unit

2187

✓	R j cted
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—	(Thr ough numeral) Cancelled
÷	Restricted

N	N n-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date									
Final	Original	121404									
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Search Notes***09865605***

Application No.

09/865,605

Examiner

Nasser G Moazzami

Applicant(s)

RICHARDSON ET AL.

Art Unit

2187

SEARCHED

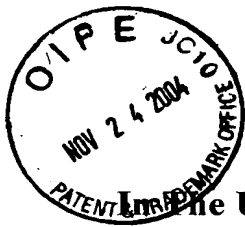
Class	Subclass	Date	Examiner
Search	Updated	12/12/2004	N.M.
709	220, 222		
711	173		
713	2		
718	1		
719	313		

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner
709	213-222	12/14/2004	N.M.
713	2		
718	1		

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
Search Updated	12/12/2004	N.M.



PATENT
Attorney Docket No.: 10013854-1

2187
JH

U.S. Patent and Trademark Office

In Re the Application of:

Inventor(s): Stephen E. RICHARDSON et al. **Confirmation No.:** 4135
Serial No.: 09/865,605 **Examiner:** Nasser G. Moazzami
Filed: May 29, 2001 **Group Art Unit:** 2187
Title: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF HAND-DELIVERY WITH THE USPTO

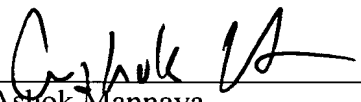
I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office. This correspondence contains the following document(s):

1 sheet of Transmittal Letter for Response/Amendment (2 copies).
11 sheets of Amendment Under 37 C.F.R. § 1.111.

Respectfully submitted,

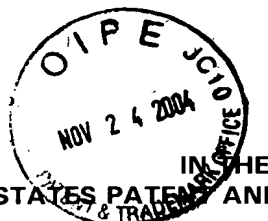
MANNAVA & KANG, P.C.

On November 24, 2004



Ashok Mannava
Registration No.45,301

MANNAVA & KANG, P.C.
8221 Old Courthouse Road
Suite 104
Vienna, VA 22182
(703) 652-3822
(703) 991-1162 (fax)



UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Stephen E. RICHARDSON et al.

Confirmation No.: 4135

Application No.: 09/865,605

Examiner: Moazzami, Nasser

Filing Date: May 29, 2001

Group Art Unit: 2187

Title: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- (X) Response/Amendment () Petition to extend time to respond
() New fee as calculated below () Supplemental Declaration
(X) No additional fee
() Other: _____ (fee \$ _____)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	19	MINUS	20	= 0	X \$18	\$ 0
INDEP. CLAIMS	3	MINUS	3	= 0	X \$88	\$ 0
[] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ \$300	\$ 0
EXTENSION FEE	1ST MONTH \$110.00	2ND MONTH \$430.00	3RD MONTH \$980.00	4TH MONTH \$1530.00		\$ 0
OTHER FEES						\$
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

Respectfully submitted,

Stephen E. RICHARDSON et al.

By

Ashok K. Mannava

Attorney/Agent for Applicant(s)
Reg. No. 45,301

Date: Nov. 24, 2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400



Atty Docket No.: 10013854-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Stephen E. RICHARDSON et al. **Confirmation No.:** 4135
Serial No.: 09/865,605 **Examiner:** Nasser G. Moazzami
Filed: May 29, 2001 **Group Art Unit:** 2187
Title: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Official Action dated August 26, 2004, kindly amend the application identified above as follows.

IN THE CLAIMS:

Please find below a listing of all of the pending claims. The statuses of the claims are set forth in parentheses.

1. (Currently Amended) A multiprocessing system comprising:
multiple processors mounted on a single die; and
multiple operating systems residing in a memory connected to said multiple processors,
wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.

2. (Currently Amended) The system of claim 1, wherein at least one of said processors ~~are~~ is operable to execute two or more of said multiple operating systems simultaneously.

3. (Currently Amended) The system of claim 2 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems.

4. (Currently Amended) The system of claim 2 1, wherein said multiple processors are directly connected to said memory to execute said multiple operating systems.

5. (Original) The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.

6. (Original) The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. (Currently Amended) A multiprocessing system comprising:
a plurality of processor groups mounted on a single die; and
multiple operating systems residing in a memory connected to said groups, wherein each of said groups executes an operating system of said multiple operating systems, and two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems.

8. (Original) The system of claim 7, wherein each of said groups includes multiple processors.

9. (Canceled)

10. (Currently Amended) The system of claim ~~9~~ 8, wherein said multiple processors in each of said groups are connected to said memory via a bus to execute said multiple operating systems.

11. (Currently Amended) The system of claim 9 8, wherein said multiple processors in each of said groups are directly connected to said memory to execute said multiple operating systems.

12. (Original) The system of claim 7, wherein each of said groups executes a distinct operating system of said multiple operating systems.

13. (Currently Amended) A multiprocessing apparatus comprising:
processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die, and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means; and
memory means for storing said plurality of operating system means.

14. (Original) The apparatus of claim 13, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

15. (Original) The apparatus of claim 13, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

16. (Original) The apparatus of claim 13, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

17. (Original) The apparatus of claim 13, wherein said processor means includes a plurality of processor group means, wherein each processor group means includes at least two of said plurality of processors.

18. (Currently Amended) The apparatus of claim ~~13~~ 17, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

19. (Currently Amended) The apparatus of claim ~~13~~ 17, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

20. (Currently Amended) The apparatus of claim 13, wherein at least one of said plurality of processors ~~processor means~~ is operable to simultaneously execute ~~each~~ two or more of said plurality of operating system means.

REMARKS

Favorable reconsideration of this application is respectfully requested in view of the following remarks. Claims 1-8 and 10-20 are pending in the present application, of which claims 1, 7 and 13 are independent. By virtue of this amendment, claim 9 has been canceled, and claims 1-4, 7, 10-11, 13 and 18-20 have been amended. No new matter has been added.

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as allegedly being anticipated by Applicant's background ("the Background"), U.S. Patent No. 6,772,241 to George et al. ("George") and U.S. Patent No. 6,526,462 to Elabd.

Claim Rejection under 35 U.S.C. § 103

The test for determining if a claim is rendered obvious by one or more references for purposes of a rejection under 35 U.S.C. § 103 is set forth in MPEP § 706.02(j):

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Therefore, if the above-identified criteria are not met, then the cited reference(s) fails to render obvious the claimed invention and, thus, the claimed invention is distinguishable over the cited reference(s).

The Official action sets forth a rejection of claims 1-20 under 35 USC 103 (a) as being allegedly unpatentable over the Background of the present application, George and Elabd. This rejection is respectfully traversed for at least the following reasons.

Initially, it is respectfully submitted that the Background does not disclose or teach the subject matter of independent claims 1, 7 or 13. More specifically, the Background does not disclose

multiple processors mounted on a single die; and
multiple operating systems residing in a memory connected to said multiple processors,
wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,

as recited in claim 1;

a plurality of processor groups mounted on a single die; and
multiple operating systems residing in a memory connected to said groups,
wherein each of said groups executes an operating system of said multiple operating systems, and two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems,

as recited in claim 7; or

processor means for executing a plurality of operating system means,
wherein said processor means includes a plurality of processors mounted on a single die, and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means,

as recited in claim 13.

The Background recites that Fig. 1 shows “a computer system 100 having multiple processors 10-40, each on a separate die (i.e., chip) 50-80, and connected to a single

operating system 90 stored in a memory 95.” Page 1, lines 20-21. The Background does not describe the claimed multiprocessor system on a single die.

George discloses “a method of and apparatus for selective delivery of an interrupt to one of multiple processors having independent operating systems.” Abstract. George further discloses a computer system 200 including a processor 210 and a co-processor 250. Col. 2, lines 55-61. The co-processor 250 is configured to operate with a mini OS. Col. 3, lines 12-14. The co-processor 250 is “configured as the master device” in the Limited ON mode and in the Listen mode, when the processor 210 is off. Col. 3, lines 28-34. Thus, the two processors are not simultaneously executing two or more operating systems in the Limited ON and the Listen modes since the processor 210 is off.

In the Full ON mode, “processor 210 may function as a master device with co-processor configured as a slave device.” Col. 3, lines 35-37. Since the co-processor is configured as a slave device in the Full ON mode, the co-processor cannot execute an independent operating system in the Full ON mode. For instance, after a sleep event is detected, and a co-processor is determined to exist, the mini OS initializes. Col. 4, lines 23-35.

Thus, George does not teach or suggest a multiprocessing system in which “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as recited in claim 1.

Further, George does not teach or suggest a multiprocessing system which comprises “a plurality of processor groups mounted on a single die” where “two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as recited in claim 7.

Also, George does not teach or suggest a multiprocessing apparatus where a “processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means,” as recited in claim 13.

The Examiner cites *In re Larson*, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965) to argue that “to make integral is not generally given patentable weight.” Office Action, page 4, lines 3-4. In *In re Larson*, the prior art disclosed a brake disc and clamp comprised of “several parts rigidly secured together as a single unit.” MPEP, 2144.04, V.B. The court in *In re Larson* held “that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice.” *Id.* In the present case, neither the processors of the Background section nor the processors of George are disclosed to be rigidly secured together as a single unit.

Further, multiple processors cannot be merely integrated together. Thus, it would not be merely a matter of obvious engineering choice for a multiprocessing system to comprise “multiple processors mounted on a single die.” Also, it would not merely be a matter of obvious engineering choice for a multiprocessing system to comprise “multiple processors mounted on a single die” where “each of said multiple processors executes an operating system of said multiple operating systems,” as recited in claim 1. The Examiner has not recited any teaching or suggestion of such a combination.

The Examiner cites Elabd as evidence that an entire system “can be implemented or embedded on a single chip.” Col. 1, lines 27-29. However, in the passage cited by the Examiner, Elabd does not discuss multiple operating systems. Thus, there is no teaching or suggestion in the Background, George or Elabd as to how to implement, for example, a multiprocessing system including multiple processors mounted on a single die “wherein each

of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.”

Further, none of the passages cited by the Examiner in the Background, George or Elabd teaches or suggests a multiprocessor system where “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as recited in claim 1. Also, none of the cited passages teach or suggest a multiprocessing system where “two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as recited in claim 7 or a multiprocessing apparatus where a “processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means,” as recited in claim 13. Thus, any alleged combination of the Background, George and Elabd would not result in the subject matter recited in claims 1, 7 or 13.

As discussed above, claims 1, 7 and 13 are patentable over the Background, George and Elabd. Thus, claims 2-6, 8, 10-12 and 14-20, which depend from claims 1, 7 and 13, are also patentable over the Background, George and Elabd. These claims are also allowable over the references cited by the Examiner because cited references fail to teach or suggest the elements recited in these claims. For instance, with respect to claim 2, the cited references fail to teach or suggest that “at least one of said processors is operable to execute two or more of said multiple operating systems simultaneously.”

PATENT

Atty Docket No.: 10013854-1
App. Ser. No.: 09/865,605

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

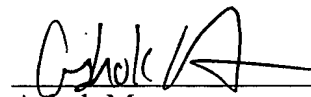
Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Stephen E. RICHARDSON et al.

Dated: November 24, 2004

By



Ashok Mannava

Registration No.: 45, 301

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,605	05/29/2001	Stephen E. Richardson	10013854-1	4135

7590 08/26/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

MOAZZAMI, NASSER G

ART UNIT PAPER NUMBER

2187

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/865,605

Applicant(s)

RICHARDSON ET AL.

Examiner

Nasser G Moazzami

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated 07/16/2004 in response to PTO Office Action dated 11/28/2003. The applicant's remarks and amendment were considered with the results that follows.
2. Claims 1-20 have been presented in this application for examination. No claims has been canceled or added. Therefore, claims 1-20 remain pending in the application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted Prior Art, hereinafter AAPA in view of George et al., hereinafter George (U.S. Patent No. 6,772,241) and further in view of Elabd (U.S. Patent No. 6,526,462).

As per claims 1-6, AAPA teaches a multiprocessing system comprising: multiple processors **[processors 10, 20, 30 and 40 (see Fig. 1)]**; and an operating system residing in a memory connected to said multiple processors **[memory 95 and operating system 90 (see Fig. 1)]**.

AAPA discloses the claimed invention, but fails to specifically teach the computer system have multiple operating system resided in the memory, wherein each of said multiple processors execute an operating system of said multiple operating systems

George teaches a computer system having multiple processors running independent operating systems, wherein each processor is configured to operate with an independent operating system **[Microsoft Windows, real time operating system or other operating systems (column 3, lines 17-24)]**. George further discloses that the processors are operable to execute two or more of said multiple operating systems simultaneously **[Full ON mode]** since a single operating system may limit the flexibility of the computer system **[column 1, lines 27-28; column 2, lines 55-57; column 3, lines 11-15 and column 3, lines 27-29)]**.

Accordingly, it would have been obvious to one having ordinary skill in the art to include an operating system for each processor as being taught by George's computer system into the combination of the AAPA's computer system in order to enhance the computer system's felexibility.

Combination of the AAPA and George teaches the claimed invention, but fails to specifically teach that the multiple processors are embedded in a single die.

As for multiple processors embedded in the same chip and multiple processors are connected to said memory via a bus to execute said multiple operating systems (it is noted that according to In re Larson 144 USPQ 347, CCPA 1965, to make integral is not generally given patentable weight; in fact this decision was later upheld for the integration of electrical components In re Tomoyuki Kohno 157 USPQ 275, CCPA 1968; thus, for purposes of rejection, integration on the same chip is not seen to alter the scope of the present claim), furthermore as it is evident by Elabd (U.S. Patent No. 6,526,462) an entire system (processors, memory, etc) can be implemented or embedded on a single chip to produce a product that is smaller, faster, and more efficient than the separate IC product [column 1, lines 22-34].

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to integrate the plurality of processors onto a single chip as being taught by Elabd. Since by doing so, it would decrease the distance between elements that allowing for faster access, decreasing the size of the overall system space and power requirements, therefore being advantageous.

As per claims 7-20, claims 7-20 encompass the same scope of the invention as those of claims 1-6 in addition of some units and means for performing the above said functions as being stated above with respect to claims 1-6. Therefore, claims 7-20 are rejected for the same reasons as stated above with respect to claims 1-6.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,108,731 (Suzuki et al.)

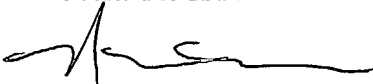
U.S. Patent No. 5,513,346 (Satagopan et al.)

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nasser G Moazzami whose telephone number is (703) 305-0017. The examiner can normally be reached on 7:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NASSER MOAZZAMI
PRIMARY EXAMINER



08/23/2004

Best Available Copy

Notice of References Cited	Application/Control No. 09/865,605	Applicant(s)/Patent Under Reexamination RICHARDSON ET AL.	
	Examiner Nasser G Moazzami	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,772,241	08-2004	George et al.	710/36
	B	US-6,526,462	02-2003	Elabd, Hammam	710/242
	C	US-6,108,731	08-2000	Suzuki et al.	710/301
	D	US-5,513,346	04-1996	Satagopan et al.	714/48
	E	US-			
	F	US-			
	G	US-			
	H	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims



Application No.

09/865,605

Examiner

Nasser G Moazzami

Applicant(s)

RICHARDSON ET AL.

Art Unit

2187

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
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Claim		Date									
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Search Notes

Application No.

09/865,605

Examiner

Nasser G Moazzami

Applicant(s)

RICHARDSON ET AL.

Art Unit

2187

SEARCHED

Class	Subclass	Date	Examiner
Search	Updated	8/21/2004	N.M.

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
Search Updated	8/21/2004	N.M.

Freeform Search

Database:	US Pre-Grant Publication Full-Text Database
	US Patents Full-Text Database
	US OCR Full-Text Database
	EPO Abstracts Database
	JPO Abstracts Database
	Derwent World Patents Index
	IBM Technical Disclosure Bulletins

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Search History

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<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u>
side by side			result set
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
<u>L8</u>	mini adj os	4	<u>L8</u>
<u>L7</u>	l5 and L6	2	<u>L7</u>
<u>L6</u>	coprocessor	4170	<u>L6</u>
<u>L5</u>	mini adj operating adj system	14	<u>L5</u>
<u>L4</u>	l2 and L3	22	<u>L4</u>
<u>L3</u>	61\$5.pn.	10000	<u>L3</u>
<u>L2</u>	(multiple or plurality) near3 (operating adj system)	2595	<u>L2</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>			
<u>L1</u>	(multiple or plurality) near3 (operating adj system)	4550	<u>L1</u>

END OF SEARCH HISTORY

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Intellectual Property Administration
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Fort Collins, Colorado 80527-2400



Atty Docket No.: 10013854-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Stephen E. RICHARDSON et al. **Confirmation No.:** 4135
Serial No.: 09/865,605 **Examiner:** Nasser G. Moazzami
Filed: May 29, 2001 **Group Art Unit:** 2187
Title: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

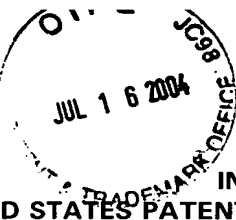
MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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JUL 20 2004
Technology Center 2100

REQUEST FOR RECONSIDERATION

Sir:

Applicants respectfully submit this Request for Reconsideration in response to the
Official Action mailed on April 16, 2004.



IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Stephen E. RICHARDSON et al.

Confirmation No.: 4135

Application No.: 09/865,605

Examiner: Nasser Moazzami

Filing Date: May 29, 2001

Group Art Unit: 2187

Title: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

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TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT

Sir:

Transmitted herewith is/are the following in the above-identified application:

- (X) Response/Amendment () Petition to extend time to respond
() New fee as calculated below () Supplemental Declaration
(X) No additional fee (Address envelope to "Mail Stop Non-Fee Amendment")
() Other: (fee \$)

CLAIMS AS AMENDED BY OTHER THAN A SMALL ENTITY						
(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
TOTAL CLAIMS	20	MINUS	20	= 0	X \$18	\$ 0
INDEP. CLAIMS	3	MINUS	3	= 0	X \$86	\$ 0
[] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					+ \$290	\$ 0
EXTENSION FEE	1ST MONTH \$110.00	2ND MONTH \$420.00	3RD MONTH \$950.00	4TH MONTH \$1480.00		\$ 0
OTHER FEES						\$
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT						\$ 0

Charge \$ 0 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

Date of Deposit:

Typed Name:

Signature: _____

Respectfully submitted,

Stephen E. RICHARDSON et al.

By *Timothy Kang* *Timothy Kang*
Reg. No. 46,423

Ashok K. Mannava

Attorney/Agent for Applicant(s)
Reg. No. 45,301



PATENT

Attorney Docket No.: 10013854-1

In The U.S. Patent and Trademark Office

In Re the Application of:

Inventor(s): Stephen E. RICHARDSON et al. **Confirmation No.:** 4135
Serial No.: 09/865,605 **Examiner:** Nasser G. Moazzami
Filed: May 29, 2001 **Group Art Unit:** 2187
Title: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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JUL 20 2004

Technology Center 2100

CERTIFICATE OF HAND-DELIVERY WITH THE USPTO

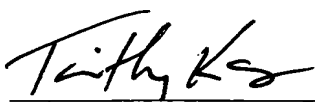
I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office. This correspondence contains the following document(s):

1 sheet of Transmittal Letter for Response/Amendment (2 copies).
10 sheets of Request for Reconsideration.

Respectfully submitted,

MANNAVA & KANG, P.C.

On July 16, 2004

 *Timothy Kang*
Reg. No. 46,423
Ashok Mannava
Registration No. 45,301

MANNAVA & KANG, P.C.
281 Murtha Street
Alexandria, VA 22304
(703) 628-1461
(703) 991-1162 (facsimile)

IN THE CLAIMS:

Please find below a listing of all of the pending claims. The statuses of the claims are set forth in parentheses.

1. (Original) A multiprocessing system comprising:

multiple processors mounted on a single die; and

multiple operating systems residing in a memory connected to said multiple processors,

wherein each of said multiple processors executes an operating system of said multiple operating systems.
2. (Original) The system of claim 1, wherein said processors are operable to execute two or more of said multiple operating systems simultaneously.
3. (Original) The system of claim 2, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems.
4. (Original) The system of claim 2, wherein said multiple processors are directly connected to said memory to execute said multiple operating systems.
5. (Original) The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.

6. (Original) The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. (Original) A multiprocessing system comprising:
a plurality of processor groups mounted on a single die; and
multiple operating systems residing in a memory connected to said groups,
wherein each of said groups executes an operating system of said multiple operating systems.

8. (Original) The system of claim 7, wherein each of said groups includes multiple processors.

9. (Original) The system of claim 8, wherein said groups are operable to execute two or more of said multiple operating systems simultaneously.

10. (Original) The system of claim 9, wherein said multiple processors in each of said groups are connected to said memory via a bus to execute said multiple operating systems.

11. (Original) The system of claim 9, wherein said multiple processors in each of said groups are directly connected to said memory to execute said multiple operating systems.

12. (Original) The system of claim 7, wherein each of said groups executes a distinct operating system of said multiple operating systems.

13. (Original) A multiprocessing apparatus comprising:
processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die; and
memory means for storing said plurality of operating system means.

14. (Original) The apparatus of claim 13, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

15. (Original) The apparatus of claim 13, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

16. (Original) The apparatus of claim 13, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

17. (Original) The apparatus of claim 13, wherein said processor means includes a plurality of processor group means, wherein each processor group means includes at least two of said plurality of processors.

18. (Original) The apparatus of claim 13, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

19. (Original) The apparatus of claim 13, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

20. (Original) The apparatus of claim 13, wherein said processor means is operable to simultaneously execute each of said plurality of operating system means.

REMARKS

Favorable reconsideration of this application is respectfully requested in view of the following remarks. Claims 1-20 are pending in the present application, of which claims 1, 7 and 13 are independent.

Claims 1-20 were rejected under 35 U.S.C. § 102(a) as allegedly being anticipated by Applicant's background ("the Background") and U.S. Patent No.6,075,938 to Bugnion et al. ("Bugnion").

Claim Rejection under 35 U.S.C. § 102

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereof functioning in substantially the same way to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrick GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

The Official Action sets forth a rejection of claims 1-20 under 35 USC 102 (a) as allegedly being anticipated by the Background of the present application and the disclosure

contained in Bugnion. This rejection is respectfully traversed for at least the following reasons.

Initially, it is respectfully submitted that the Background does not anticipate the subject matter of independent claim 1. More specifically, the Background does not disclose “multiple processors mounted on a single die; and multiple operating systems residing in a memory connected to said multiple processors,” as recited in claim 1. Instead, the Background discloses a scheme including multiple processors on a single die and recites that Bugnion discloses multiple operating systems. Page 2, lines 1-23. However, these are two different approaches, and thus can not anticipate the invention of claim 1. Further, the Background goes on to say that Bugnion “fails to provide multiple physical processors, implemented in hardware, on a single die.” Page 2, lines 20-21. The background further states, in referring to Bugnion, that “if this architecture were to support multiple physical processors, it would need space for providing multiple dies.” Page 3, lines 1-2. Thus, claim 1 is not anticipated by the Background.

The Examiner switches between different approaches mentioned in the Background to reject claims 2-6. For example, the Examiner refers to Bugnion to reject claims 2, 5 and 6; Fig. 2 of the Application to reject claim 3; and Fig. 1 of the Application to reject claim 4. These represent three different approaches. For example, Bugnion discloses a layer of software between the hardware and operating system for scalable multiprocessor machines that “acts like a virtual machine monitor.” Col. 4, lines 6-16. Fig. 2 shows a multiprocessing scheme including multiple processors on a single die, but connected to a single operating system 250. Background, page 2, lines 1-7. Fig. 1 shows a multiprocessing scheme “having

multiple processors 10-40, each on a separate die (that is, chip) 50-80, and connected to a single operating system 90 stored in memory 95. Background, page 1, lines 19-22.

As discussed above, claim 1 is not anticipated by the Background. Thus, claims 2-6 are not anticipated by different approaches recited in the Background and Bugnion. For example, Bugnion does not disclose “multiple processors mounted on a single die,” as recited in claim 1. Thus, claims 2, 5 and 6 are not anticipated by Bugnion. Fig. 2 does not disclose “operating systems residing in a memory connected to said multiple processors” (as recited in claim 1) since Fig. 2 shows a single operating system. Thus, claim 3 is not anticipated by Fig. 2. Further, Fig. 1 does not disclose “multiple processors mounted on a single die” (as recited in claim 1) since it shows multiple processors each on a separate die. Thus, claim 4 is not anticipated by Fig. 1.

Therefore, independent claim 1 and its dependent claims 2-6 are believed to be allowable over both the Background and Bugnion.

The Official Action does not specifically reject claims 7-20. However, neither the Background nor Bugnion discloses “a plurality of processor groups mounted on a single die; and multiple operating systems residing in a memory connected to said groups,” as recited in claim 7 or “processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die” as recited in claim 13. Neither the Background nor Bugnion discloses the combination of multiple processors on a single die nor multiple operating systems connected to the multiple processors, as discussed above. Thus, neither the Background nor Bugnion discloses processor means for executing a plurality of operating system means, wherein the processor

means includes a plurality of processors mounted on a single die. Therefore, neither the Background nor Bugnion anticipates claim 13.

Further, because neither the Background nor Bugnion discloses multiple processors on a single die in combination with multiple operating systems connected to the multiple processors, neither the Background nor Bugnion discloses the combination of a plurality of processor groups mounted on a single die and multiple operating systems residing in a memory connected to those groups. Therefore, neither the Background nor Bugnion anticipates claim 7.

Therefore, claims 7, 13 and their dependent claims 8-12 and 14-20 are believed to be allowable over both the Background and Bugnion. Although Applicants believe that neither the Background nor Bugnion disclose the features of dependent claims 8-12 and 14-20, Applicants respectfully reserve the right to pursue such arguments at a later date.

Conclusion

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified

PATENT

Atty Docket No.: 10013854-1
App. Ser. No.: 09/865,605

application, please contact the undersigned at the telephone number listed below. Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Stephen E. RICHARDSON et al.

Dated: July 16, 2004

By

 *Timothy Kang*
Reg. No. 46,423
Ashok Mannava
Registration No. 45,301

MANNAVA & KANG, P.C.
281 Murtha Street
Alexandria, VA 22304
(703) 628-1461
(703) 991-1162 (facsimile)

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2000

Application or Docket Number

69865605

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	26	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	24 minus 20 =	4
INDEPENDENT CLAIMS	3 minus 3 =	0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	20	Minus	20 = 0
Independent	3	Minus	3 = 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	355.00
X\$ 9=	
X40=	
+135=	
TOTAL	

RATE	FEE
BASIC FEE	710.00
X\$18=	
X80=	
+270=	
TOTAL	710

SMALL ENTITY

OR OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL	
ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL	
ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	20	Minus	20 = 0
Independent	3	Minus	3 = 0
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL	
ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL	
ADDIT. FEE	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total		Minus	
Independent		Minus	
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL	
ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL	
ADDIT. FEE	

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
- ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
- *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/865,605	05/29/2001	Stephen E. Richardson	10013854-1	4135

7590 04/16/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

MOAZZAMI, NASSER G

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/865,605

Applicant(s)

RICHARDSON ET AL.

Examiner

Nasser G Moazzami

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 4.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement submitted by applicant on 08/29/2001 has been considered. Please see attached PTO-1449.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-20 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant admitted Prior Art, hereinafter AAPA.

As per claim 1, AAPA teaches a multiprocessing system comprising: multiple processors mounted on a single die [**chip multiprocessor 295 includes multiple processors 210-240 on a single die 290 (see page 2, lines 2-3)**]; and multiple operating systems residing in a memory connected to said multiple processors, wherein each of said multiple processors executes an operating system of said multiple

operating systems [**multiple processors executing multiple operating systems (page 2, lines 18-19)**].

As per claim 2, AAPA discloses that said processors are operable to execute two or more of said multiple operating systems simultaneously [**Bugnion discloses that multiple operating systems can run simultaneously (see Bugnion, column 5, lines 62-63)**].

As per claim 3, AAPA discloses that said multiple processors are connected to said memory via a bus to execute said multiple operating systems [**see Fig. 2 of AAPA**].

As per claim 4, AAPA discloses that said multiple processors are directly connected to said memory to execute said multiple operating systems [**see Fig. 1 of AAPA**].

As per claim 5, AAPA discloses that each of said processors executes a distinct operating system of said multiple operating systems [**running different operating systems, wherein each virtual machine is configured with the resources that the operating system can handle (see Bugnion, column 4, lines 46-48)**].

As per claim 6, AAPA discloses that the system further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems **[some virtual machines can run commodity uniprocessor or multiprocessor operating systems (see Bugnion, column 4, lines 32-33)]**.

As per claims 7-20, claims 7-20 encompass the same scope of the invention as those of claims 1-6 in addition of some units and means for performing the above said functions as being stated above with respect to claims 1-6. Therefore, claims 7-20 are rejected for the same reasons as stated above with respect to claims 1-6.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,658,591 (Arndt)

U.S. Patent No. 6,314,501 (Gulick et al.)

U.S. Patent No. 5,446,841 (Kitano et al.)

U.S. Patent No. 5,301,324 (Dewey et al.)

U.S. Patent No. 5,201,040 (Wada et al.)

U.S. Patent No. 4,709,325 (Yajima)

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nasser G Moazzami whose telephone number is (703) 305-0017. The examiner can normally be reached on 7:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NASSER MOAZZAMI
PRIMARY EXAMINER


04/14/2004

Notice of References Cited	Application/Control No. 09/865,605	Applicant(s)/Patent Under Reexamination RICHARDSON ET AL.	
	Examiner Nasser G Moazzami	Art Unit 2187	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,658,591	12-2003	Arndt, Richard Louis	714/6
	B	US-6,314,501	11-2001	Gulick et al.	711/153
	C	US-5,446,841	08-1995	Kitano et al.	709/213
	D	US-5,301,324	04-1994	Dewey et al.	718/105
	E	US-5,201,040	04-1993	Wada et al.	711/147
	F	US-4,709,325	11-1987	Yajima, Seiichi	714/10
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

FORM PTO-1449

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION DISCLOSURE
STATEMENT

(Use several sheets if necessary)

ATTY. DOCKET NO.

10013854-1

SERIAL NO.

APPLICANT

Stephen E. RICHARDSON et al.

FILING DATE

Herewith

GROUP

N/A 2187

11002 U.S. PRO
09/865605

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
J. M.	1A	6,075,938	June 13, 2000	BUGNION, E. et al.	305-703	27 500.48
	1B					
	1C					
	1D					
	1E					
	1F					
	1G					
	1H					
	1I					
	1J					
	1K					

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	TRANSLATION	
							YES	NO
	1L							
	1M							
	1N							
	1O							
	1P							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

	1Q	
	1R	
	1S	

EXAMINER

DATE CONSIDERED

104/12/04

Refine Search

Search Results -

Terms	Documents
L5 or L6	7

Database:
 US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search: L7

Refine Search

Recall Text

Clear

Interrupt

Search History

DATE: Tuesday, April 13, 2004 [Printable Copy](#) [Create Case](#)

Set Name Query

side by side

Hit Count Set Name
result set

DB=USPT; PLUR=YES; OP=ADJ

<u>L7</u>	15 or 16	7	<u>L7</u>
<u>L6</u>	5,201,040.pn.	1	<u>L6</u>
<u>L5</u>	13 and L4	6	<u>L5</u>
<u>L4</u>	(6516372 or 6075938 or 5590301 or 5446841 or 5301324 or 4709325).pn.	6	<u>L4</u>
<u>L3</u>	11 same L2	16	<u>L3</u>
<u>L2</u>	multi-processors or multiprocessor	13008	<u>L2</u>
<u>L1</u>	independent near2 ((os) or (operating adj system))	1531	<u>L1</u>

END OF SEARCH HISTORY

Freeform Search

Database:	US Pre-Grant Publication Full-Text Database US Patents Full-Text Database US OCR Full-Text Database EPO Abstracts Database JPO Abstracts Database Derwent World Patents Index IBM Technical Disclosure Bulletins
Term:	11 and L4
Display:	15 Documents in <u>Display Format:</u> - Starting with Number 1
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<i>DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ</i>			
<u>L5</u>	11 and L4	38	<u>L5</u>
<u>L4</u>	12 with simultan\$6	9602	<u>L4</u>
<u>L3</u>	11 and L2	509	<u>L3</u>
<u>L2</u>	(multiple or several or plurality) with ((os) or (operating adj system))	313489	<u>L2</u>
<u>L1</u>	directly with (coupl\$5 or connect\$5 or access\$5) with memory with ((os) or (operating adj system))	1176	<u>L1</u>

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L3 and L4	6

Database:
 US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
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Search: L5

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DATE: Tuesday, April 13, 2004 [Printable Copy](#) [Create Case](#)

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result set

DB=USPT; PLUR=YES; OP=ADJ

<u>L5</u>	13 and L4	6	<u>L5</u>
<u>L4</u>	(6516372 or 6075938 or 5590301 or 5446841 or 5301324 or 4709325).pn.	6	<u>L4</u>
<u>L3</u>	11 same L2	16	<u>L3</u>
<u>L2</u>	multi-processors or multiprocessor	13008	<u>L2</u>
<u>L1</u>	independent near2 ((os) or (operating adj system))	1531	<u>L1</u>

END OF SEARCH HISTORY

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L5: Entry 1 of 6

File: USPT

Feb 4, 2003

DOCUMENT-IDENTIFIER: US 6516372 B1

TITLE: Partitioning a distributed shared memory multiprocessor computer to facilitate selective hardware maintenance

Abstract Text (1):

A distributed shared memory multiprocessor computer system is provided, which has a number of processors and is divided into partitions. Each partition has within it one or more of the processors, and may also have memory or cache and other related hardware. Although each partition works together and communicates with other partitions to share computational load, the partitions each are independently operable and execute an independent copy of the operating system. The partitions comprise additional features to enable removal of a partition from the operating computer system, and to enable insertion of hardware into the operating computer system.

Brief Summary Text (14):

A distributed shared memory multiprocessor computer system is provided, which has a number of processors and is divided into partitions. Each partition has within it one or more of the processors, and may also have memory or cache and other related hardware. Although each partition works together and communicates with other partitions to share computational load, the partitions each are independently operable and execute an independent copy of the operating system. The partitions comprise additional features as described herein, to enable removal of a partition from the operating computer system, and to enable insertion of hardware into the operating computer system.

CLAIMS:

1. A distributed shared memory multiprocessor computer system, comprising: a plurality of processors; a plurality of partitions, each of which comprises one or more of the plurality of processors, executes an operating system independent of other partitions, and is independently removable from and insertable into the computer system while the computer system remains in operation; a system interconnection network, linking the plurality of partitions; a control module, operable to disable hardware before removal from the operating computer system and to enable hardware after insertion into the operating computer system; and a reset fence that prevents partition reset signals from propagating outside the partition.

7. A distributed shared memory multiprocessor computer system, comprising: a plurality of processors; a plurality of partitions, each of which comprises one or more of the plurality of processors, executes an operating system independent of other partitions, and is independently removable from and insertable into the computer system while the computer system remains in operation, wherein each partition further comprises one or more c-bricks, each c-brick comprising one or more processors, and each partition further comprises one or more routers, such that each router is connected to one or more c-bricks and to at least one other router; a system interconnection network, linking the plurality of partitions; a control module, operable to disable hardware before removal from the operating computer system and to enable hardware after insertion into the operating computer system.

8. A distributed shared memory multiprocessor computer system, comprising: a plurality of processors; a plurality of partitions, each of which comprises one or more of the plurality of processors, executes an operating system independent of other partitions, and is independently removable from and insertable into the computer system while the

Apple

computer system remains in operation; a system interconnection network, linking the plurality of partitions; and a control module operable to disable hardware before removal from the operating computer system and to enable hardware after insertion into the operating computer system, wherein the control module is further operable to tristate connections between the partition and the computer system such that the computer system is logically detached from the partition.

9. A distributed shared memory multiprocessor computer system, comprising: a plurality of processors; a plurality of partitions, each of which comprises one or more of the plurality of processors, executes an operating system independent of other partitions, and is independently removable from and insertable into the computer system while the computer system remains in operation; a system interconnection network, linking the plurality of partitions; and a control module, operable to disable hardware before removal from the operating computer system and to enable hardware after insertion into the operating computer system, wherein the control module is further operable to handle errors generated as a result of removal of hardware.

11. A distributed shared memory multiprocessor computer system, comprising: a plurality of processors; a plurality of partitions, each of which comprises one or more of the plurality of processors, executes an operating system independent of other partitions, and is independently removable from and insertable into the computer system while the computer system remains in operation; a system interconnection network, linking the plurality of partitions; a control module operable to disable hardware before removal from the operating computer system and to enable hardware after insertion into the operating computer system; and a cache, wherein the cache is not coherent with cache in other partitions, so that removal of one cache from an operating computer system will not result in the computer system crashing.

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L5: Entry 2 of 6

File: USPT

Jun 13, 2000

DOCUMENT-IDENTIFIER: US 6075938 A

TITLE: Virtual machine monitors for scalable multiprocessors

Brief Summary Text (6):

The second approach to dealing with the system software challenges of scalable shared-memory multiprocessors is to statically partition the machine and run multiple, independent operating systems that use distributed system protocols to export a partial single system image to the users. An example of this approach is the Sun Enterprise10000 machine that handles software scalability and hardware reliability by allowing users to hard partition the machine into independent failure units each running a copy of the Solaris operating system. Users still benefit from the tight coupling of the machine, but cannot dynamically adapt the partitioning to the load of the different units. This approach favors low implementation cost and compatibility over innovation. Digital's announced Galaxies operating system, a multi-kernel version of VMS, also partitions the machine relatively statically like the Sun machine, with the additional support for segment drivers that allow applications to share

Drawing Description Text (2):

FIG. 1 is a schematic diagram illustrating the architecture of a computer system according to the invention. Disco, a virtual machine monitor, is a software layer between a multiprocessor hardware layer and multiple virtual machines that run independent operating systems and application programs.

Detailed Description Text (57):

Using this mechanism, multiple virtual machines accessing a shared disk end up sharing machine memory. The copy-on-write semantics means that the virtual machine is unaware of the sharing with the exception that disk requests can finish nearly instantly. Consider an environment running multiple virtual machines for scalability purposes. All the virtual machines can share the same root disk containing the kernel and application programs. The code and other read-only data stored on the disk will be DMA-ed into memory by the first virtual machine that accesses it. Subsequent requests will simply map the page specified to the DMA engine without transferring any data. The result is shown in FIG. 4 where all virtual machines share these read-only pages. Effectively we get the memory sharing patterns expected of a single shared memory multiprocessor operating system even though the system runs multiple independent operating systems.

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L5: Entry 3 of 6

File: USPT

Dec 31, 1996

DOCUMENT-IDENTIFIER: US 5590301 A

TITLE: Address transformation in a cluster computer system

Detailed Description Text (10):

The 30-bit register 15 in the primary cache of the CPU 11 can specify one gigabyte of address locations which is the family limit of the exemplary CPUs. There is value in reserving a portion of the addressable space in main memory 8 to the private use of the CPUs on each multiprocessor board for, among other reasons, permitting each multiprocessor board to operate under an independent operating system. (These independent operating systems may be the same or different operating systems.) On the other hand, there is a need for establishing direct communication among the clusters and CPUs operating under the different operating systems in order that they can function with the full power of a cluster system architecture. One way in which this feature can be achieved is by providing shared memory space in main memory 8.

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L5: Entry 4 of 6

File: USPT

Aug 29, 1995

DOCUMENT-IDENTIFIER: US 5446841 A

TITLE: Multi-processor system having shared memory for storing the communication information used in communicating between processors

Brief Summary Text (4):

On the other hand, for example to an information processing system in which a plurality of processors are operated by independent operating systems, respectively, and are loosely coupled to one another through a common memory (shared memory), is described in Japanese patent un-examined publication No. JP-A-64-78361 (corresponding to copending U.S. patent application Ser. No. 07/209,073 filed Jun. 20, 1988), U.S. Pat. No. 5,201,040. In JP-A-64-78361, it is described that an instruction equal to a signal processor instruction, used for communication between the processors, is used between the processors by the loosely coupled multi-processor system through the shared memory to perform the communication. However, it is not described that a processor number and a shared memory number are dynamically changed to perform the communication. Further, in JP-A-64-78361, it is not also described that when a processor of a virtual machine (hereinafter, referred to as simply "a virtual processor" when applicable) simulated on a real machine performs the communication with another 10 virtual processor through the shared memory, that communication is performed without reading out the storage data of the shared memory in order to recognize a virtual processor number.

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L5: Entry 5 of 6

File: USPT

Apr 5, 1994

DOCUMENT-IDENTIFIER: US 5301324 A

TITLE: Method and apparatus for dynamic work reassignment among asymmetric, coupled processors

Detailed Description Text (15):

FIG. 1 shows the system environment within which the present invention operates. FIG. 1 shows a tightly coupled multiprocessor system consisting of four processors (CPUs), processor W, 100, processor X, 101, processor Y, 102, processor Z, 103, sharing a common memory, 130. Each of the processors, 100-103, contain features, 110, 111, 112, 113. Processor W, 100 contains features C and E, 110. Processor X, 101, contains features A and D, 111. Processor Y, 102, contains features B, C, and D, 112. Processor Z, 103, contains features A and B, 113. Each of the processors are currently executing work units. The work units are, WU4, 120, on processor W, 100, WU3, 121 on processor X, 101, WU1, 122, on Processor Y, 102, and WU2, 123, on Processor Z, 103. Shown as residing in the common memory, 130, are key data for assigning work units to processors, 131, 132, and 133. These data are the Work Unit Table, 131, the Ready Queue, 132, and the Processor Feature table, 133. In the preferred embodiment the multiprocessor computing system as shown is executing with a hypervisor, 140, such as IBM's Processor Resource/System Manager, PR/SM, facility in Logical Partitioning, LPAR, mode. The Assignment means, 141, and the Promotion mechanism, 142, are, in the preferred embodiment, a program within the hypervisor. In this example the work units being assigned are actually operating systems which are independent of each other. The invention works equally as well, in an alternative embodiment, in a multiprocessor computing system environment running under control of an operating system, such as IBM's MVS/ESA. In this case the Assignment means and the Promotion mechanism are within the operating system and the work units are tasks, address spaces or jobs. The processors use conventional communication paths for signalling each other.

End of Result Set

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Nov 24, 1987

TITLE: Loosely coupled multiprocessor system capable of transferring a control signal set by the use of a common memory

A conventional loosely coupled multiprocessor system of the type described is disclosed by James A. Katzman in "A Fault-Tolerant Computing System" published on January, 1979 (first revision), by Tandem Computers Inc., Calif. The conventional loosely coupled multiprocessor system comprises a plurality of processor units having independent operating systems and a plurality of peripheral devices used by the processor units in common. At any rate, each of the processor units can individually carry out a processing operation by the use of a set of control signals.

Referring to FIG. 1, a loosely coupled multiprocessor system according to a first embodiment of this invention comprises first and second processor units 11 and 12 which individually have independent operating systems in the manner known in the art. Each of the first and the second processor units 11 and 12 is operable in accordance with a predetermined program which is similar for the processor units 11 and 12. The program of each processor unit 11 and 12 is executed by using a set of control signals variable with time to process a job imposed on each processor unit 11 or 12. Therefore, the control signal sets of the first and the second processor units 11 and 12 are different from each other and will be referred to as first and second control signal sets, respectively. The first and the second processor units 11 and 12 are coupled to each other through a processor interface line 14.



IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Stephen E Richardson et al

Confirmation No.: 4135

Application No.: 09/865605

Examiner: Unknown

Filing Date: May 29, 2001

Group Art Unit:

Title: Chip Multiprocessor With Multiple Operating Systems

Box MISSING PARTS
COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL LETTER FOR SUBMITTAL OF MISSING PARTS

Sir:

This is in response to a Notice to File Missing Parts of Application under 37 CFR 1.53(f) mailed on 07/25/2001. Enclosed is a copy of said Notice and the following documents and fees to complete the filing requirements of the above-identified application.

(X) Executed Declaration and Power of Attorney. The above-identified application is the same application which the inventor executed by signing the enclosed declaration.

() Statutory basic filing fee () Utility \$710.00 () Design \$320.00

() Additional claim fees of \$

(X) Missing Parts Surcharge \$130.00

() A Petition for Extension of Time for reply to Notice of Missing Parts is attached.

() one month \$110.00
() two months \$390.00
() three months \$890.00
() four months \$1390.00

Please charge to Deposit Account 08-2025 the sum of \$130.00. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.

(X) A duplicate copy of this transmittal letter is enclosed.

Respectfully submitted,

Stephen E Richardson et al

By [Signature]

Lloyd E. Dakin, Jr.

Attorney/Agent for Applicant(s)
Reg. No. 38,423

Date: 08/07/2001

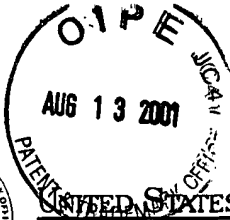
Telephone No.: (650) 857-2295

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit: 08/07/2001

Typed Name: Amy Jesus

Signature: [Signature]



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/865,605	05/29/2001	Stephen E. Richardson	10013854-1

CONFIRMATION NO. 4135

FORMALITIES LETTER



OC000000006337924

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

Date Mailed: 07/25/2001

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The signature of the following inventor(s) is missing from the oath or declaration:
Padmanabha Venkitakrishnan
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.
- The balance due by applicant is \$ 130.

*A copy of this notice **MUST** be returned with the reply.*

Customer Service Center

Initial Patent Examination Division (703) 308-1202

PART 2 - COPY TO BE RETURNED WITH RESPONSE

08/15/2001 SMINASS1 00000020 082025 09865605

01 FC:105 130.00 CH

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATIONATTORNEY DOCKET NO. 10013854-1

AUG 13 2001

#3

As a below named inventor, I hereby declare that
My residence/post office address and citizenship are as stated below next to my name;
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

the specification of which is attached hereto unless the following box is checked:

() was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: _____ NO: _____
			YES: _____ NO: _____

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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Send Correspondence to:
HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Direct Telephone Calls To:

Lloyd E. Dakin, Jr.
(650) 857-2295

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Stephen E. RICHARDSON Citizenship: USResidence: 668 Vera Cruz Avenue, Los Altos, CA 94022Post Office Address: Same as Residence

Inventor's Signature [Signature] Date 5/22/01

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 10013854-1

Full Name of # 2 joint inventor: Gary VONDRAN Citizenship: US

Residence: 1400 Magnolia Avenue, San Carlos, CA 94070

Post Office Address: Same as Residence

Inventor's Signature [Signature]

Date 5/22/01

Full Name of # 3 joint inventor: Stuart SIU Citizenship: US

Residence: 20943 Elbridge Court, Castro Valley, CA 94552

Post Office Address: Same as Residence

Inventor's Signature [Signature]

Date 5/24/01

Full Name of # 4 joint inventor: Paul KELTCHER Citizenship: US

Residence: 878 Hollenbeck Avenue, Sunnyvale, CA 94087

Post Office Address: Same as Residence

Inventor's Signature [Signature]

Date 5/22/01

Full Name of # 5 joint inventor: Shankar VENKATARAMAN Citizenship: US

Residence: 1111 Derbyshire Drive, Cupertino, CA 95014

Post Office Address: Same as Residence

Inventor's Signature [Signature]

Date 22-may-2001

Full Name of # 6 joint inventor: Padmanabha VENKITAKRISHNAN Citizenship: US

Residence: 961 Bermuda Court, Sunnyvale, CA 94086

Post Office Address: Same as Residence

Inventor's Signature [Signature]

Date 07-JUNE-2001

Full Name of # 7 joint inventor: Joseph KU Citizenship: US

Residence: 4102 Amaranta Avenue, Palo Alto, CA 94306

Post Office Address: Same as Residence

Inventor's Signature [Signature]

Date 5/22/01

Full Name of # 8 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

Inventor's Signature _____

Date _____



Hewlett-Packard Company
1501 Page Mill Road, ms 4u-10
Palo Alto, CA 94304-1126

650.852.8063 Fax

August 2, 2001

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Technology Center 2100

Commissioner for Patents
Office of Initial Patent Examination
Customer Service Center
Washington, D.C. 20231

RE: Correction of Filing Receipt
Application No: 09/865,605; Filing Date 05/29/2001
HP Docket No: 10013854-1

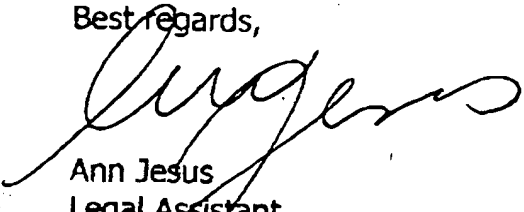
Dear Sirs:

We hereby request a correction to the enclosed filing receipt. Please correct the names of inventors as follow:

Gary Lee Vondan, Jr
Stuart C. Siu
Padmanabha I. Venkitakrishnan
Joseph Weiyeh Ku

Thank you for your prompt attention to this request.

Best regards,


Ann Jesus
Legal Assistant
Corporate Legal Department
Intellectual Property Section



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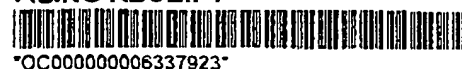
APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/865,605 ✓	05/29/2001 ✓	2152	710	10013854-1 ✓	4	20	3

CONFIRMATION NO. 4135

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

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FILING RECEIPT



OC00000006337923

Date Mailed: 07/25/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Stephen E. Richardson, Los Altos, CA; ✓
Y. Gary Vondran, San Carlos, CA; ✓ Gary Lee Vondran, Jr.
Stuart Siu, Castro Valley, CA; ✓ Stuart C. Siu
Paul Keltcher, Sunnyvale, CA; ✓
Shankar Venkataraman, Cupertino, CA; ✓
Padmanabha Venkitakrishnan, Sunnyvale, CA; ✓ Padmanabha I. Venkitakrishnan
Joseph Ku, Palo Alto, CA; ✓ Joseph Weiye Ku

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted 07/24/2001

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Chip multiprocessor with multiple operating systems ✓

Apple

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Bib Data Sheet

CONFIRMATION NO. 4135

SERIAL NUMBER 09/865,605	FILING DATE 05/29/2001 RULE	CLASS 709	GROUP ART UNIT 2152	ATTORNEY DOCKET NO. 10013854-1
APPLICANTS Stephen E. Richardson, Los Altos, CA; Gary Lee Vondan JR., San Carlos, CA; Stuart C. Siu, Castro Valley, CA; Paul Keltcher, Sunnyvale, CA; Shankar Venkataraman, Cupertino, CA; Padmanabha I. Venkitakrishnan, Sunnyvale, CA; Joseph Weiyeh Ku, Palo Alto, CA;				
** CONTINUING DATA ***** ** FOREIGN APPLICATIONS *****				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/24/2001				
Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance		STATE OR COUNTRY CA	SHEETS DRAWING 4	TOTAL CLAIMS 20
Verified and Acknowledged _____ Examiner's Signature _____ Initials _____			INDEPENDENT CLAIMS 3	
ADDRESS HEWLETT-PACKARD COMPANY Intellectual Property Administration P.O. Box 272400 Fort Collins ,CO 80527-2400				
TITLE Chip multiprocessor with multiple operating systems				
FILING FEE RECEIVED 710	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit	



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APPLICATION NUMBER	FILING/RECEIPT DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
09/865,605	05/29/2001	Stephen E. Richardson	10013854-1

CONFIRMATION NO. 4135

FORMALITIES LETTER



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Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

Date Mailed: 07/25/2001

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The signature of the following inventor(s) is missing from the oath or declaration:
Padmanabha Venkitakrishnan
- To avoid abandonment, a late filing fee or oath or declaration surcharge as set forth in 37 CFR 1.16(e) of \$130 for a non-small entity, must be submitted with the missing items identified in this letter.
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Intellectual Property Administration

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Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 10013854-1

IN THE U.S. PATENT AND TRADEMARK OFFICE
Patent Application Transmittal LetterASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): ☒ Utility ☐ Design☒ original patent application,☐ continuation-in-part application

INVENTOR(S): Stephen E. RICHARDSON et al.

TITLE: CHIP MULTIPROCESOR WITH MULTIPLE OPERATING SYSTEMS

Enclosed are:

- ☒ The Declaration and Power of Attorney. ☐ signed ☒ unsigned or partially signed
☒ 4 sheets of drawings (one set) ☐ Associate Power of Attorney
☐ Form PTO-1449 ☒ Information Disclosure Statement and Form PTO-1449
☐ Priority document(s) ☐ (Other) (fee \$)

CLAIMS AS FILED BY OTHER THAN A SMALL ENTITY				
(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) TOTALS
TOTAL CLAIMS	20 — 20	0	X \$18	\$ 0
INDEPENDENT CLAIMS	3 — 3	0	X \$78	\$ 0
ANY MULTIPLE DEPENDENT CLAIMS	0		\$260	\$ 0
BASIC FEE: Design (\$310.00); Utility (\$710.00)				\$ 710
TOTAL FILING FEE				\$ 710
OTHER FEES				\$
TOTAL CHARGES TO DEPOSIT ACCOUNT				\$ 710

Charge \$ 710 to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16, 1.17, 1.19, 1.20 and 1.21. A duplicate copy of this sheet is enclosed.

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By _____

Typed Name:

Respectfully submitted,

Stephen E. RICHARDSON et al.

By John W. Ryan

John W. Ryan

Attorney/Agent for Applicant(s)

Reg. No. 33,771

Date: May 29, 2001

Telephone No.: (202) 663-6446

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT APPLICATION FOR:

CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING
SYSTEMS

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CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

FIELD OF THE INVENTION

The present invention is generally related to a computer chip architecture having multiple processors on a single die. More particularly, the present invention is related to a multiprocessing chip utilizing multiple operating systems.

BACKGROUND OF THE INVENTION

Existing internet data centers (IDCs) pack hundreds of processors (e.g., servers and the like) in a single building for processing a large volume of data transactions. Generally, the compute density or number of nodes per volume defines the efficiency of the IDC. The compute density effects the amortization of the high cost of the IDC infrastructure (e.g., networking, power, cooling, maintenance, reliability, and availability support). Typically, the greater the compute density, the better the IDC will be able to amortize the high cost of IDC infrastructure. Accordingly, a large compute density may be preferred. However, space may be unavailable or costly for locating a large number of processors necessary for maintaining a large compute density.

To provide increased compute density, multiprocessing schemes that utilize multiple processors have been developed. One conventional multiprocessing scheme (shown in Fig. 1) includes a computer system 100 having multiple processors 10-40, each on a separate die (i.e., chip) 50-80, and connected to a single operating system 90 stored in a memory 95. The system 100 may conserve space if the system is provided in a single housing.

A second conventional multiprocessing scheme (shown in Fig. 2) includes a computer system 200 having a chip multiprocessor 295. The chip multiprocessor includes multiple processors 210-240 on a single die 290. Similar to the processors 10-40 in system 100, the processors 210-240 are connected to a single operating system 250 stored in a memory 260. The processors 210-240 may communicate with the memory 260 via a bus 270. System 200 conserves space by providing multiple processors on a single die. However, the systems 100 and 200 suffer from well known scalability problems.

Schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together. A well known limitation of this scheme and other multiprocessing schemes utilizing a single operating system is that an operating system does not scale well to large numbers of processors. That is, as the number of processors managed by a single operating system increases, the efficiency of the operating system goes down dramatically. For example, an operating system typically includes internal data structures that may be limited in the number of processors that can be supported, and limited bandwidth on a bus may slow transactions. Thus, scaling becomes impractical above some small number (e.g., currently about four to at most 64 processors, depending on the operating system in question).

Bugnion et al., in U.S. Pat. No. 6,075,938, discloses using a cache coherent non-uniform memory architecture (CC-NUMA) that supports multiple processors executing multiple operating systems. However, Bugnion et al. discloses multiple virtual processors, implemented in software on a single physical processor. This architecture fails to provide multiple physical processors, implemented in hardware, on a single die. Accordingly, this architecture suffers a performance penalty, because the single physical processor must task switch among multiple virtual processors (only one virtual processor can be running on the physical processor at any

given time). Moreover, if this architecture were to support multiple physical processors, it would need space for providing multiple dies, and processing speed would consequently be sacrificed due to the input/output procedures needed to communicate among the multiple separate processors and the memory.

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SUMMARY OF THE INVENTION

An aspect of the present invention is to provide a multiprocessing system including multiple processors mounted on a single die. The multiple processors are connected to a memory storing multiple operating systems. Each of the multiple processors may execute one of the multiple operating systems.

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Another aspect of the present invention is to provide a multiprocessing system including a plurality of processor groups mounted on a single die. The processor groups are connected to a memory storing multiple operating systems. Each of the processor groups may execute one of the multiple operating systems. The processor group may include one or more processors mounted on the die.

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Certain embodiments of the present invention are capable of achieving certain advantages, including some or all of the following: mounting multiple processors on a single die reduces the cabling problem inherent in connecting multiple processors on separate dies in separate housings; mounting multiple processors on a single die reduces the latency required for communication among the processors and improves the efficiency of message passing, potentially enabling a whole new class of applications (e.g., data mining) to run on such a multiprocessing system; mounting multiple processors on a single die reduces chip-to-chip

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communication costs and leads to further power efficiency; and increased scalability for multiprocessing.

Those skilled in the art will appreciate these and other advantages and benefits of various embodiments of the invention upon reading the following detailed description of a preferred embodiment with reference to the below-listed drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which like numeral references refer to like elements, and wherein:

Fig. 1 illustrates a conventional multiprocessing scheme including multiple processors, each on a separate die;

Fig. 2 illustrates a conventional multiprocessing scheme including multiple processors on a single die;

Fig. 3 illustrates an embodiment of a multiprocessing scheme employing the principles of the present invention; and

Fig. 4 illustrates another embodiment of a multiprocessing scheme employing the principles of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one of ordinary skill in the art that these specific details need not be used to practice the present

invention. In other instances, well known structures, interfaces, and processes have not been shown in detail in order not to unnecessarily obscure the present invention.

Fig. 3 illustrates an embodiment including a computer system 300 employing the principles of the present invention. System 300 includes a chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360. The processors 305-320 function with operating systems 325-340 respectively, as illustrated by connections 345-348. The operating systems 325-340 are stored in a memory 365. During operation, each processor 305-320 may access a respective operating system 325-340 by communicating with the memory 365, for example, via a bus 370. Alternatively, each processor may be directly connected to the memory 365 without using the bus 370. The memory 365 may include one or more of the following: SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.

Processors 305-320 may be configured, such that each processor executes its own operating system. Multiple processors (e.g., multiple processors in a processor group) may also be configured to execute a single operating system. Fig. 4 illustrates a second embodiment including a computer system 400 employing the principles of the present invention. System 400 includes a chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460. The processors 405-420 are divided into two processor groups 425 and 430 having processors 405 and 410 in the processor group 425 and processors 415 and 420 in the processor group 430. The processor group 425 executes an operating system 435 stored in a memory 465 (as illustrated by a connection 475), and the processor group 430 executes an operating system 440 stored in the memory 465 (as illustrated by a connection 480). During operation, each

processor group 425-430 may access a respective operating system 435-440 by communicating with the memory 465, for example, via a bus 470. Alternatively, each processor and/or processor group may be directly connected to the memory 465 without using the bus 470.

The operating systems shown in Figs. 3-4 and described above may include conventional operating systems, such as WINDOWS NT, UNIX and the like, and the processors in systems 300 and 400 may include conventional processors. Each processor may be capable of executing a single operating system, or capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems. Systems 300 and 400 may be operable to execute a variety of applications, such as web service, database service and the like. Four processors are shown in Figs. 3-4 for illustration purposes, and it will be apparent to one of ordinary skill in the art that more or less processors and/or processor groups may be included on the dies 360 and 460. Additionally, as is known in the art, the processors in systems 300 and 400 may access one or more caches (not shown).

It will be apparent to one of ordinary skill in the art that a system employing the principles of the present invention may be operable to support both processor groups and processors on a single die, such that each processor group and processor not within a processor group executes a distinct operating system.

Having each processor (or processor group) executing its own independent operating system minimizes scaling problems realized when utilizing a single operating system with multiple processors. For example, one hundred processors independently executing one hundred operating systems may be no more of a problem than one processor executing one operating system. The embodiments described above are operable to provide this type of scaling on a single chip.

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What is claimed is:

1. A multiprocessing system comprising:
multiple processors mounted on a single die; and
multiple operating systems residing in a memory connected to said multiple processors,
5 wherein each of said multiple processors executes an operating system of said multiple operating systems.
2. The system of claim 1, wherein said processors are operable to execute two or more of said multiple operating systems simultaneously.
3. The system of claim 2, wherein said multiple processors are connected to said memory
via a bus to execute said multiple operating systems.
4. The system of claim 2, wherein said multiple processors are directly connected to said
15 memory to execute said multiple operating systems.
5. The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.
- 20 6. The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. A multiprocessing system comprising:
a plurality of processor groups mounted on a single die; and
multiple operating systems residing in a memory connected to said groups, wherein each
of said groups executes an operating system of said multiple operating systems.

5

8. The system of claim 7, wherein each of said groups includes multiple processors.

9. The system of claim 8, wherein said groups are operable to execute two or more of said
multiple operating systems simultaneously.

10. The system of claim 9, wherein said multiple processors in each of said groups are
connected to said memory via a bus to execute said multiple operating systems.

11. The system of claim 9, wherein said multiple processors in each of said groups are
directly connected to said memory to execute said multiple operating systems.

12. The system of claim 7, wherein each of said groups executes a distinct operating system
of said multiple operating systems.

20 13. A multiprocessing apparatus comprising:
processor means for executing a plurality of operating system means, wherein said
processor means includes a plurality of processors mounted on a single die; and
memory means for storing said plurality of operating system means.

14. The apparatus of claim 13, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

5 15. The apparatus of claim 13, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

16. The apparatus of claim 13, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

17. The apparatus of claim 13, wherein said processor means includes a plurality of processor group means, wherein each processor group means includes at least two of said plurality of processors.

18. The apparatus of claim 13, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

19. The apparatus of claim 13, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

20. The apparatus of claim 13, wherein said processor means is operable to simultaneously execute each of said plurality of operating system means.

ABSTRACT

Multiple processors are mounted on a single die. The die is connected to a memory storing multiple operating systems or images of multiple operating systems. Each of the processors or a group of one or more of the processors is operable to execute a distinct one of the multiple operating systems. Therefore, resources for a single operating system may be dedicated to one processor or a group of processors. Consequently, a large number of processors mounted on a single die can operate efficiently.

10013854-1

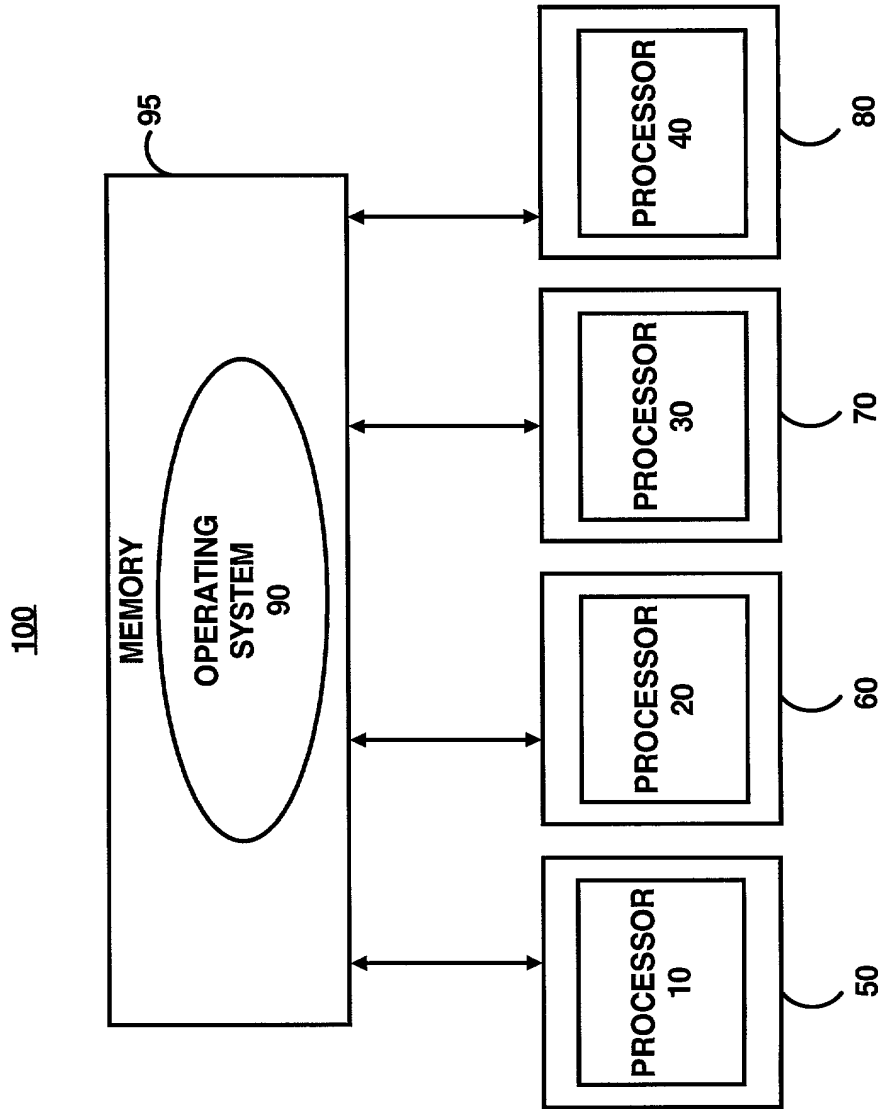


FIG. 1
Prior Art

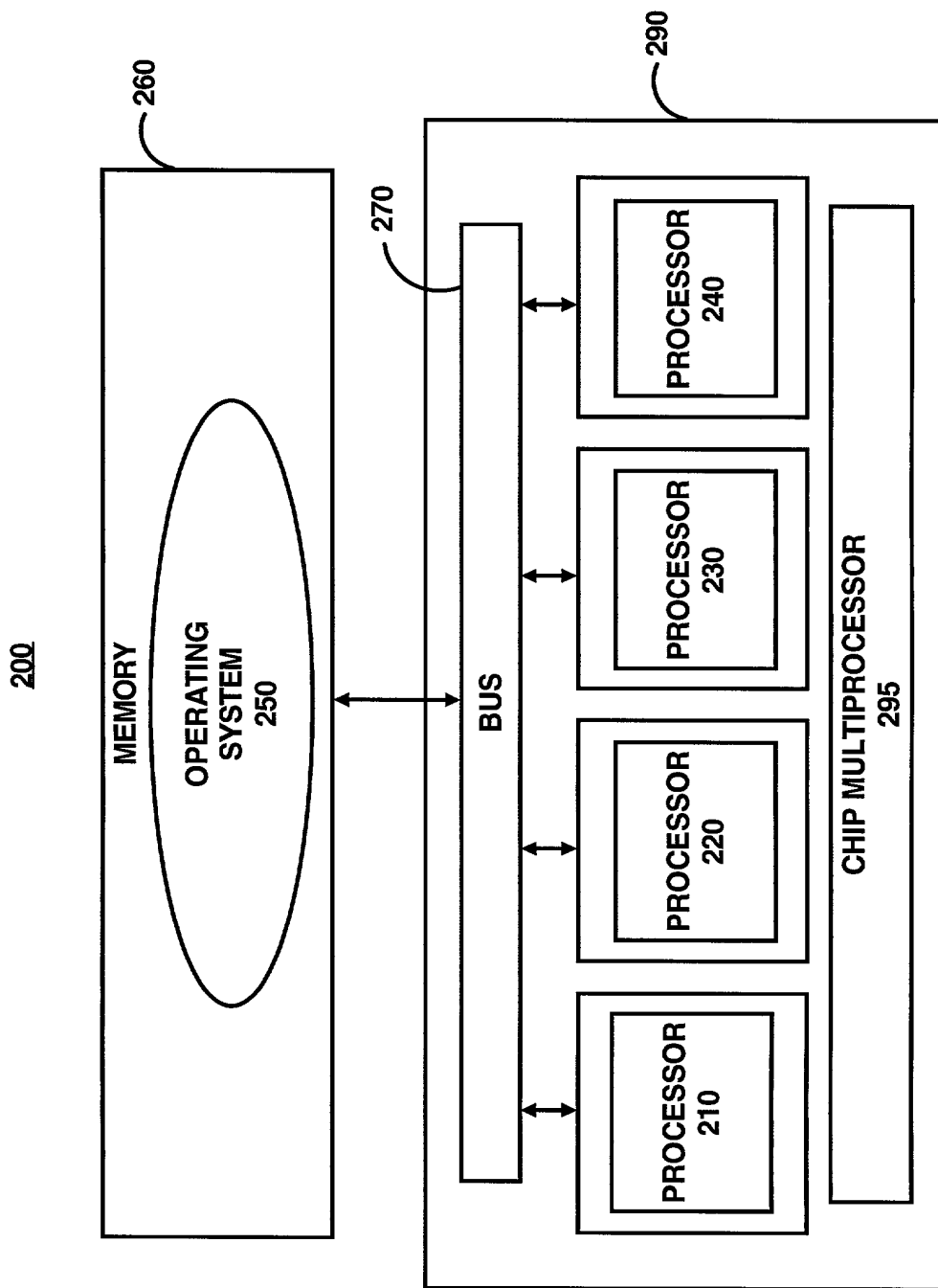


FIG. 2
Prior Art

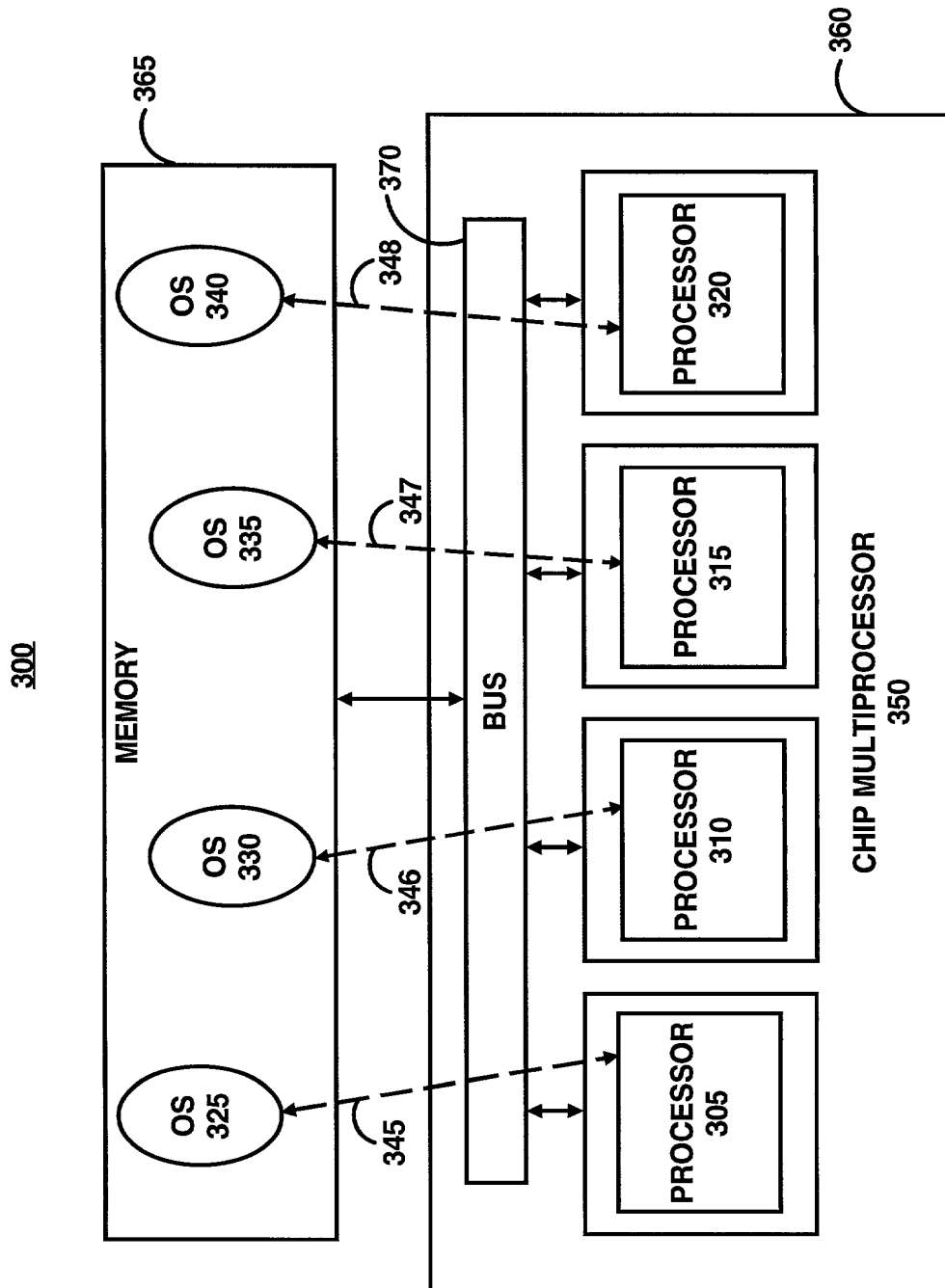


FIG. 3

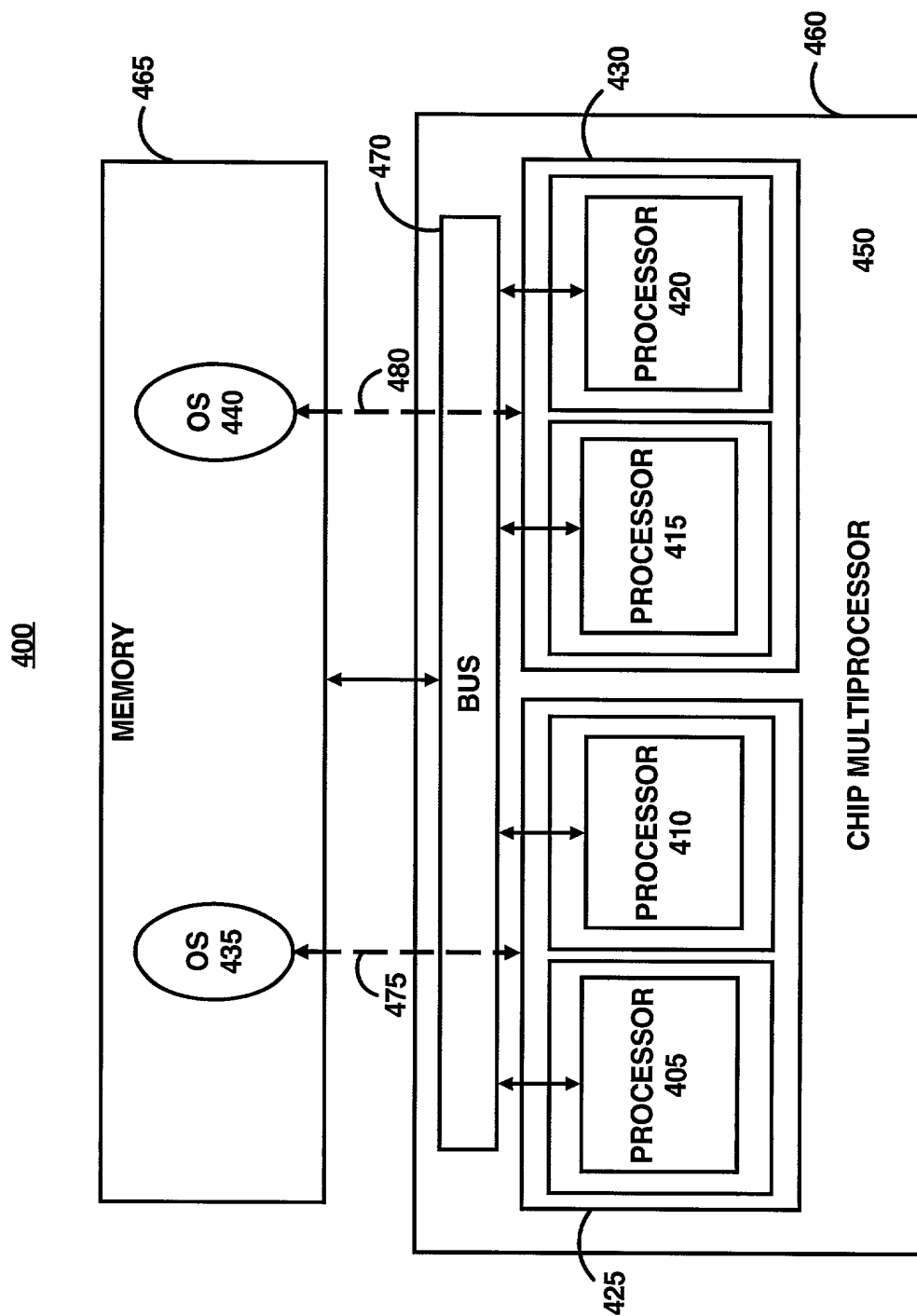


FIG. 4

**DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION**ATTORNEY DOCKET NO. 10013854-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

The specification of which is attached hereto unless the following box is checked:

() was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
			YES: _____ NO: _____
			YES: _____ NO: _____

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

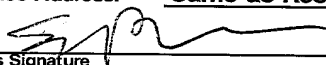
As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

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Lloyd E. Dakin, Jr.
(650) 857-2295

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: Stephen E. RICHARDSON Citizenship: USResidence: 668 Vera Cruz Avenue, Los Altos, CA 94022Post Office Address: Same as ResidenceInventor's Signature Date 5/22/01

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (continued)

ATTORNEY DOCKET NO. 10013854-1

Full Name of # 2 joint inventor: Gary VONDRAN Citizenship: US

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Inventor's Signature [Signature] Date 5/22/01

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Post Office Address: Same as Residence

Inventor's Signature _____ Date _____

Full Name of # 7 joint inventor: Joseph KU Citizenship: US

Residence: 4102 Amaranta Avenue, Palo Alto, CA 94306

Post Office Address: Same as Residence

Inventor's Signature [Signature] Date 5/22/01

Full Name of # 8 joint inventor: _____ Citizenship: _____

Residence: _____

Post Office Address: _____

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APPLICATION NO. 09/865605	CONT/PRIOR	CLASS 709	SUBCLASS 213	ART UNIT 2187 2152	EXAMINER MOAZZAMI
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APPLICANTS

Stephen Richardson
Gary Vondan
Stuart Siu
Paul Keltcher

Chip multiprocessor with multiple operating systems

TITLE

PTO-2040
12/89

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
INTERNATIONAL CLASSIFICATION							

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	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
☐ The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		NOTICE OF ALLOWANCE MAILED	
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709	213-	04-09	N.H.
↓	215	↓	↓
711	147	↓	↓
↓	153	↓	↓
714	6, 10	↓	↓
718	105	↓	↓

INTERFERENCE SEARCHED			
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SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	Date	Exmr.
Text search	04-09	N.H.
" "	↓	↓
" "	04-13	↓
INVENTOR SEARCH	↓	↓
IBM	↓	↓
FEES	↓	↓
INTEREST	↓	↓

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POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION			
O.I.P.E. CLASSIFIER		49	6/11/01
FORMALITY REVIEW	H.S.	866	07-24-01
RESPONSE FORMALITY REVIEW	Zm	927	09/24/01

INDEX OF CLAIMS

✓ Rejected N Non-elected
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Claim	Date
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Patent Application Transmittal Letter

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Washington, D.C. 20231

Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is a(n): ☒ Utility ☐ Design

☒ original patent application,

☐ continuation-in-part application

INVENTOR(S): Stephen E. RICHARDSON et al.

TITLE: CHIP MULTIPROCESOR WITH MULTIPLE OPERATING SYSTEMS

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Respectfully submitted,

Stephen E. RICHARDSON et al.

By John W. Ryan
John W. Ryan

Attorney/Agent for Applicant(s)

Reg. No. 33,771

Date: May 29, 2001

Telephone No.: (202) 663-6446

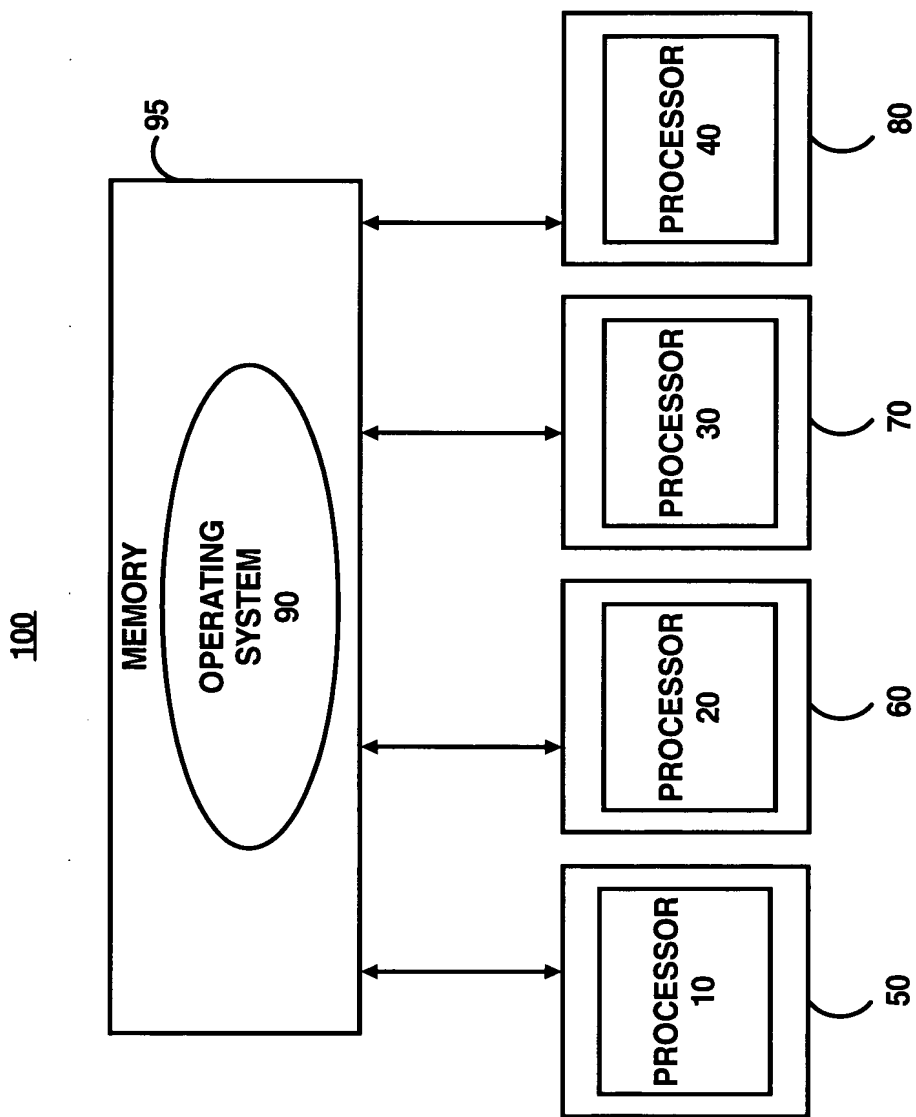


FIG. 1
Prior Art

200

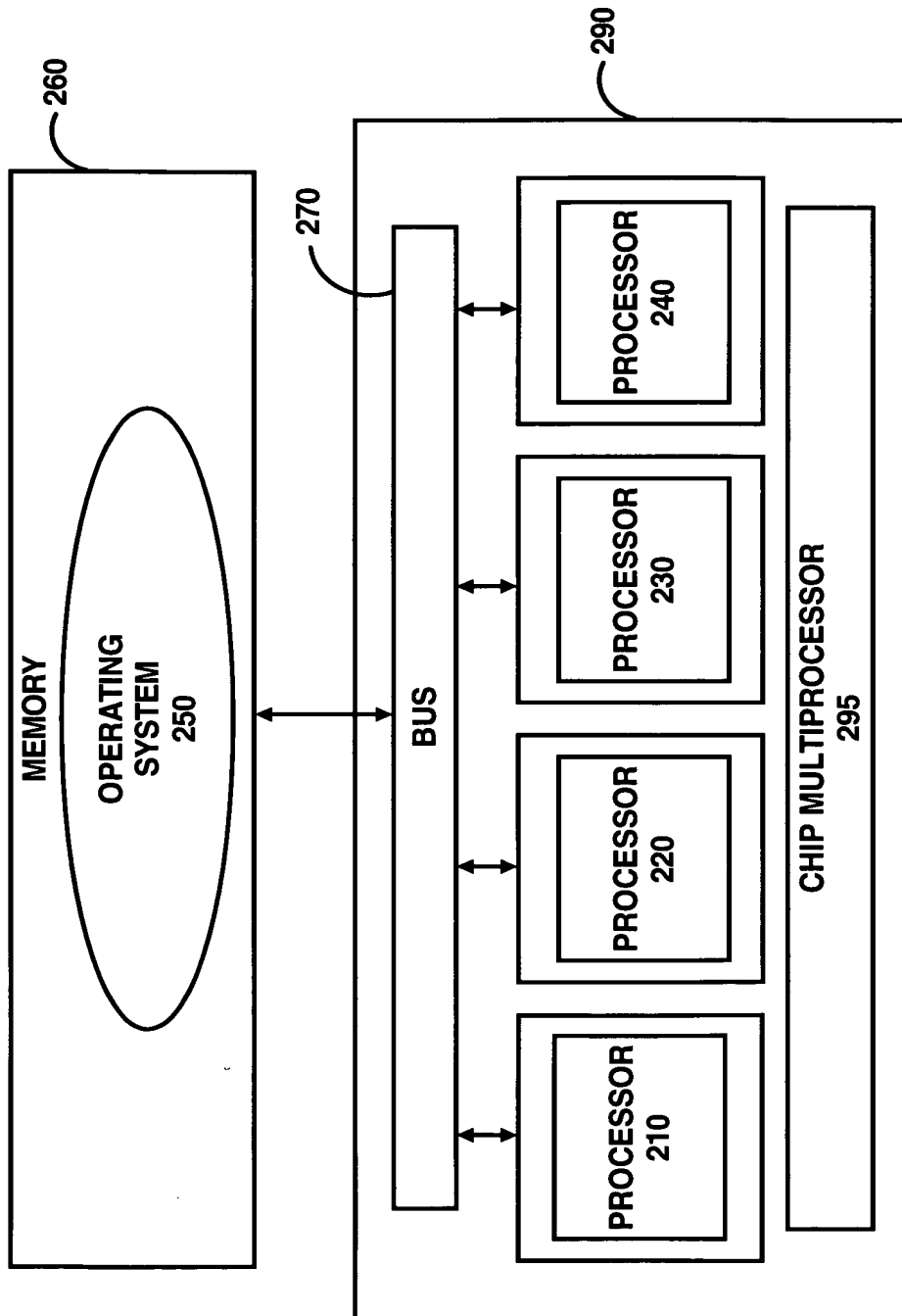


FIG. 2

Prior Art

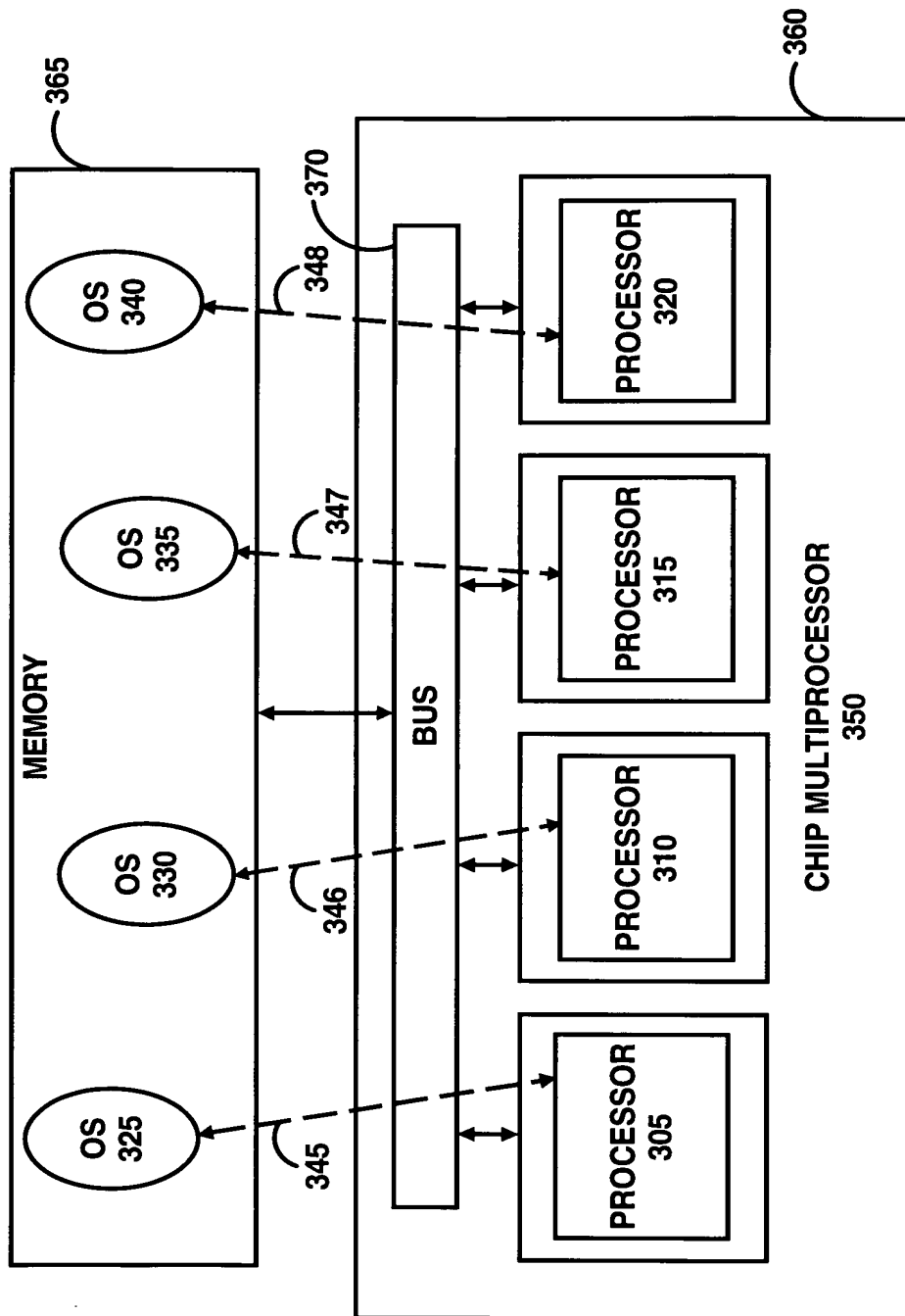


FIG. 3

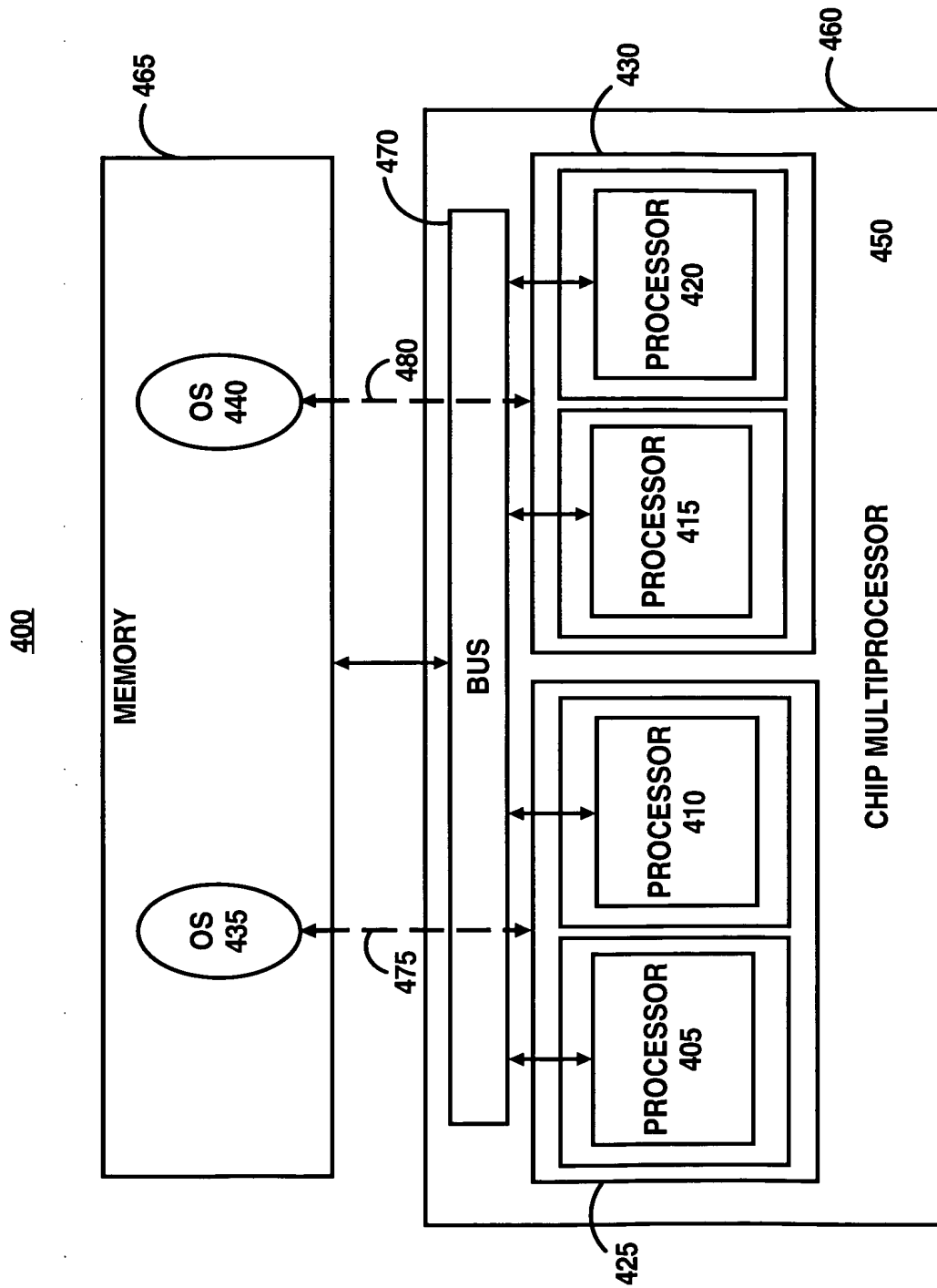


FIG. 4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

UTILITY PATENT APPLICATION FOR:

CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING
SYSTEMS

Inventors:

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CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

FIELD OF THE INVENTION

The present invention is generally related to a computer chip architecture having multiple processors on a single die. More particularly, the present invention is related to a multiprocessing chip utilizing multiple operating systems.

BACKGROUND OF THE INVENTION

Existing internet data centers (IDCs) pack hundreds of processors (e.g., servers and the like) in a single building for processing a large volume of data transactions. Generally, the compute density or number of nodes per volume defines the efficiency of the IDC. The compute density effects the amortization of the high cost of the IDC infrastructure (e.g., networking, power, cooling, maintenance, reliability, and availability support). Typically, the greater the compute density, the better the IDC will be able to amortize the high cost of IDC infrastructure. Accordingly, a large compute density may be preferred. However, space may be unavailable or costly for locating a large number of processors necessary for maintaining a large compute density.

To provide increased compute density, multiprocessing schemes that utilize multiple processors have been developed. One conventional multiprocessing scheme (shown in Fig. 1) includes a computer system 100 having multiple processors 10-40, each on a separate die (i.e., chip) 50-80, and connected to a single operating system 90 stored in a memory 95. The system 100 may conserve space if the system is provided in a single housing.

A second conventional multiprocessing scheme (shown in Fig. 2) includes a computer system 200 having a chip multiprocessor 295. The chip multiprocessor includes multiple processors 210-240 on a single die 290. Similar to the processors 10-40 in system 100, the processors 210-240 are connected to a single operating system 250 stored in a memory 260. The processors 210-240 may communicate with the memory 260 via a bus 270. System 200 conserves space by providing multiple processors on a single die. However, the systems 100 and 200 suffer from well known scalability problems.

Schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together. A well known limitation of this scheme and other multiprocessing schemes utilizing a single operating system is that an operating system does not scale well to large numbers of processors. That is, as the number of processors managed by a single operating system increases, the efficiency of the operating system goes down dramatically. For example, an operating system typically includes internal data structures that may be limited in the number of processors that can be supported, and limited bandwidth on a bus may slow transactions. Thus, scaling becomes impractical above some small number (e.g., currently about four to at most 64 processors, depending on the operating system in question).

Bugnion et al., in U.S. Pat. No. 6,075,938, discloses using a cache coherent non-uniform memory architecture (CC-NUMA) that supports multiple processors executing multiple operating systems. However, Bugnion et al. discloses multiple virtual processors, implemented in software on a single physical processor. This architecture fails to provide multiple physical processors, implemented in hardware, on a single die. Accordingly, this architecture suffers a performance penalty, because the single physical processor must task switch among multiple virtual processors (only one virtual processor can be running on the physical processor at any

given time). Moreover, if this architecture were to support multiple physical processors, it would need space for providing multiple dies, and processing speed would consequently be sacrificed due to the input/output procedures needed to communicate among the multiple separate processors and the memory.

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SUMMARY OF THE INVENTION

An aspect of the present invention is to provide a multiprocessing system including multiple processors mounted on a single die. The multiple processors are connected to a memory storing multiple operating systems. Each of the multiple processors may execute one of the multiple operating systems.

Another aspect of the present invention is to provide a multiprocessing system including a plurality of processor groups mounted on a single die. The processor groups are connected to a memory storing multiple operating systems. Each of the processor groups may execute one of the multiple operating systems. The processor group may include one or more processors mounted on the die.

Certain embodiments of the present invention are capable of achieving certain advantages, including some or all of the following: mounting multiple processors on a single die reduces the cabling problem inherent in connecting multiple processors on separate dies in separate housings; mounting multiple processors on a single die reduces the latency required for communication among the processors and improves the efficiency of message passing, potentially enabling a whole new class of applications (e.g., data mining) to run on such a multiprocessing system; mounting multiple processors on a single die reduces chip-to-chip

communication costs and leads to further power efficiency; and increased scalability for multiprocessing.

Those skilled in the art will appreciate these and other advantages and benefits of various embodiments of the invention upon reading the following detailed description of a preferred embodiment with reference to the below-listed drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the accompanying figures in which like numeral references refer to like elements, and wherein:

Fig. 1 illustrates a conventional multiprocessing scheme including multiple processors, each on a separate die;

Fig. 2 illustrates a conventional multiprocessing scheme including multiple processors on a single die;

Fig. 3 illustrates an embodiment of a multiprocessing scheme employing the principles of the present invention; and

Fig. 4 illustrates another embodiment of a multiprocessing scheme employing the principles of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one of ordinary skill in the art that these specific details need not be used to practice the present

invention. In other instances, well known structures, interfaces, and processes have not been shown in detail in order not to unnecessarily obscure the present invention.

Fig. 3 illustrates an embodiment including a computer system 300 employing the principles of the present invention. System 300 includes a chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360. The processors 305-320 function with operating systems 325-340 respectively, as illustrated by connections 345-348. The operating systems 325-340 are stored in a memory 365. During operation, each processor 305-320 may access a respective operating system 325-340 by communicating with the memory 365, for example, via a bus 370. Alternatively, each processor may be directly connected to the memory 365 without using the bus 370. The memory 365 may include one or more of the following: SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.

Processors 305-320 may be configured, such that each processor executes its own operating system. Multiple processors (e.g., multiple processors in a processor group) may also be configured to execute a single operating system. Fig. 4 illustrates a second embodiment including a computer system 400 employing the principles of the present invention. System 400 includes a chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460. The processors 405-420 are divided into two processor groups 425 and 430 having processors 405 and 410 in the processor group 425 and processors 415 and 420 in the processor group 430. The processor group 425 executes an operating system 435 stored in a memory 465 (as illustrated by a connection 475), and the processor group 430 executes an operating system 440 stored in the memory 465 (as illustrated by a connection 480). During operation, each

processor group 425-430 may access a respective operating system 435-440 by communicating with the memory 465, for example, via a bus 470. Alternatively, each processor and/or processor group may be directly connected to the memory 465 without using the bus 470.

The operating systems shown in Figs. 3-4 and described above may include conventional operating systems, such as WINDOWS NT, UNIX and the like, and the processors in systems 300 and 400 may include conventional processors. Each processor may be capable of executing a single operating system, or capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems. Systems 300 and 400 may be operable to execute a variety of applications, such as web service, database service and the like. Four processors are shown in Figs. 3-4 for illustration purposes, and it will be apparent to one of ordinary skill in the art that more or less processors and/or processor groups may be included on the dies 360 and 460. Additionally, as is known in the art, the processors in systems 300 and 400 may access one or more caches (not shown).

It will be apparent to one of ordinary skill in the art that a system employing the principles of the present invention may be operable to support both processor groups and processors on a single die, such that each processor group and processor not within a processor group executes a distinct operating system.

Having each processor (or processor group) executing its own independent operating system minimizes scaling problems realized when utilizing a single operating system with multiple processors. For example, one hundred processors independently executing one hundred operating systems may be no more of a problem than one processor executing one operating system. The embodiments described above are operable to provide this type of scaling on a single chip.

While this invention has been described in conjunction with the specific embodiments thereof, it is evident that many alternatives, modifications and variations will be apparent to those skilled in the art. There are changes that may be made without departing from the spirit and scope of the invention.

[illegible]

What is claimed is:

1. A multiprocessing system comprising:

multiple processors mounted on a single die; and

multiple operating systems residing in a memory connected to said multiple processors,

5 wherein each of said multiple processors executes an operating system of said multiple operating systems.

2. The system of claim 1, wherein said processors are operable to execute two or more of said multiple operating systems simultaneously.

3. The system of claim 2, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems.

4. The system of claim 2, wherein said multiple processors are directly connected to said memory to execute said multiple operating systems.

5. The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.

6. The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. A multiprocessing system comprising:
a plurality of processor groups mounted on a single die; and
multiple operating systems residing in a memory connected to said groups, wherein each
of said groups executes an operating system of said multiple operating systems.

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8. The system of claim 7, wherein each of said groups includes multiple processors.

9. The system of claim 8, wherein said groups are operable to execute two or more of said
multiple operating systems simultaneously.

10. The system of claim 9, wherein said multiple processors in each of said groups are
connected to said memory via a bus to execute said multiple operating systems.

11. The system of claim 9, wherein said multiple processors in each of said groups are
directly connected to said memory to execute said multiple operating systems.

12. The system of claim 7, wherein each of said groups executes a distinct operating system
of said multiple operating systems.

13. A multiprocessing apparatus comprising:
processor means for executing a plurality of operating system means, wherein said
processor means includes a plurality of processors mounted on a single die; and
memory means for storing said plurality of operating system means.

14. The apparatus of claim 13, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

5 15. The apparatus of claim 13, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

16. The apparatus of claim 13, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

17. The apparatus of claim 13, wherein said processor means includes a plurality of processor group means, wherein each processor group means includes at least two of said plurality of processors.

18. The apparatus of claim 13, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

19. The apparatus of claim 13, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

20. The apparatus of claim 13, wherein said processor means is operable to simultaneously execute each of said plurality of operating system means.

ABSTRACT

Multiple processors are mounted on a single die. The die is connected to a memory storing multiple operating systems or images of multiple operating systems. Each of the processors or a group of one or more of the processors is operable to execute a distinct one of the multiple operating systems. Therefore, resources for a single operating system may be dedicated to one processor or a group of processors. Consequently, a large number of processors mounted on a single die can operate efficiently.

5

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATIONATTORNEY DOCKET NO. 10013854-1

As a below named inventor, I hereby declare that:

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS

the specification of which is attached hereto unless the following box is checked:

() was filed on _____ as US Application Serial No. or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119	
			YES: _____	NO: _____
			YES: _____	NO: _____

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith:

Customer Number **022879**Place Customer
Number Bar Code
Label hereSend Correspondence to:
HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Direct Telephone Calls To:

Lloyd E. Dakin, Jr.
(650) 857-2295

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: Same as Residence
Inventor's Signature: [Signature] Date: 5/22/01

DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (Continued)

ATTORNEY DOCKET NO. 10013854-1

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Inventor's Signature: [Signature] Date: 5/22/01

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Post Office Address: Same as Residence
Inventor's Signature: [Signature] Date: 5/24/01

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Inventor's Signature: [Signature] Date: 5/22/01

Full Name of # 5 joint inventor: Shankar VENKATARAMAN Citizenship: US
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Inventor's Signature: [Signature] Date: 22-may-2001

Full Name of # 6 joint inventor: Padmanabha VENKITAKRISHNAN Citizenship: US
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Inventor's Signature: _____ Date: _____

Full Name of # 7 joint inventor: Joseph KU Citizenship: US
Residence: 4102 Amaranta Avenue, Palo Alto, CA 94306
Post Office Address: Same as Residence
Inventor's Signature: [Signature] Date: 5/22/01

Full Name of # 8 joint inventor: _____ Citizenship: _____
Residence: _____
Post Office Address: _____
Inventor's Signature: _____ Date: _____



UNITED STATES PATENT AND TRADEMARK OFFICE



Bib Data Sheet

SERIAL NUMBER 09/865,605		FILING DATE 05/29/2001	CLASS 709	GROSS UNIT	COMMISSION STATES PATENT AND TRADE WASHINGTON 131 0V	CONFIRMATION	ATTORNEY DOCKET # 10013854-
APPLICANTS Stephen E. Richardson, Los Altos, CA; Gary Lee Vondan JR., San Carlos, CA; Stuart C. Siu, Castro Valley, CA; Paul Keltcher, Sunnyvale, CA; Shankar Venkataraman, Cupertino, CA; Padmanabha I. Venkitakrishnan, Sunnyvale, CA; Joseph Weiyeh Ku, Palo Alto, CA;							
** CONTINUING DATA *****							
** FOREIGN APPLICATIONS *****							
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/24/2001							
Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions ☐ yes ☐ no ☐ Met after Allowance				STATE OR COUNTRY CA	SHEETS TOTAL DRAWINGS 4 20	INDEPENDENT CLAIMS 3	
Verified and Acknowledged Examiner's Signature _____ Initials _____							
ADDRESS HEWLETT-PACKARD COMPANY Intellectual Property Administration P.O. Box 272400 Fort Collins , CO 80527-2400							
TITLE Chip multiprocessor with multiple operating systems							
FILING FEE RECEIVED 840		FEES: Authority has been given in Paper to charge/credit DEPOSIT ACCOUNT for following: No. _____ No. _____					
☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit _____							

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

05/31/2001 MABDI1 00000006 082025 09865605

01 FC:101 710.00 CH

PTO-1556
(5/87)

*U.S. GPO: 2000-468-987/39595

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2000

Application or Docket Number

69865605

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

TOTAL CLAIMS	20	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	20 minus 20 =	* 0
INDEPENDENT CLAIMS	3 minus 3 =	* 0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
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	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

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TYPE ☐

OR

OTHER THAN
SMALL ENTITY

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BASIC FEE	355.00
X\$ 9=	
X40=	
+135=	
TOTAL	

OR

RATE	FEE
BASIC FEE	710.00
X\$18=	
X80=	
+270=	
TOTAL	710

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
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	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL ADDIT. FEE	

OR

RATE	ADDI- TIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
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	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDI- TIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL ADDIT. FEE	

OR

RATE	ADDI- TIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL ADDIT. FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDI- TIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL ADDIT. FEE	

OR

RATE	ADDI- TIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

CLAIMS ONLY

SERIAL NO.

09865605

FILING DATE

APPLICANT(S)

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1	/					
2		/				
3		/				
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TOTAL IND.	3	↙		↙		↙
TOTAL DEP.	17	↘		↘		↘
TOTAL CLAIMS	20					

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TOTAL IND.		↙		↙		↙
TOTAL DEP.		↘		↘		↘
TOTAL CLAIMS						

* MAY BE USED FOR ADDITIONAL CLAIMS OR ADMMENDMENTS

BEST AVAILABLE COPY

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Stephen E. RICHARDSON et al.

Serial No.: Unknown

Examiner: Not Yet Assigned

Filing Date: Herewith

Group Art Unit: N/A

Title: CHIP MULTIPROCESSOR WITH MULTIPLE OPERATING SYSTEMS



ASSISTANT COMMISSIONER FOR PATENTS

Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

- ☒ under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)
- ☐ under 37 CFR 1.97(c) together with either a:
☐ Statement under 37 CFR 1.97(e), or
☐ a \$240.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)
- ☐ under 37 CFR 1.97 (d) together with a:
☐ Statement under 37 CFR 1.97(e), and
☐ a petition under 37 CFR 1.97(d)(2), and
☐ a \$130.00 petition fee set forth in 37 CFR 1.17(i).
(Filed after final action or notice of allowance, whichever occurs first, but before payment of the issue fee)

Please charge to Deposit Account 08-2025 the sum of \$0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25.

☒ Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Citation together with copies, of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

☐ A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no.

Date of Deposit

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

By _____

Typed Name:

Respectfully submitted,

Stephen E. RICHARDSON et al.

By John W. Ryan
John W. Ryan

Attorney/Agent for Applicant(s)

Reg. No. 33,771

Date: May 29, 2004

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2000

Application or Docket Number

69865605

CLAIMS AS FILED - PART I

(Column 1)

(Column 2)

TOTAL CLAIMS	20	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	20 minus 20 =	0
INDEPENDENT CLAIMS	3 minus 3 =	0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

SMALL ENTITY
TYPE ☐OR OTHER THAN
SMALL ENTITY

RATE	FEE		RATE	FEE
BASIC FEE	355.00	OR	BASIC FEE	710.00
X\$ 9=		OR	X\$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL		OR	TOTAL	710

CLAIMS AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	20	Minus	20 = 0
	Independent	3	Minus	3 = 0
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**
	Independent	*	Minus	***
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**
	Independent	*	Minus	***
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDI- TIONAL FEE		RATE	ADDI- TIONAL FEE
X\$ 9=		OR	X\$18=	
X40=		OR	X80=	
+135=		OR	+270=	
TOTAL ADDIT. FEE		OR	TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.