

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,

Petitioner

v.

SONRAI MEMORY LIMITED,

Patent Owner

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 6,874,014**

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I. INTRODUCTION

Apple Inc. (“Apple” or “Petitioner”) petitions for *inter partes* review of U.S. Patent No. 6,874,014 (“’014 patent”) (EX1001). The ’014 patent describes a chip architecture having multiple processors on a single die that utilizes multiple operating systems. As shown below, the system described in the ’014 patent was known in the prior art.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Pursuant to 37 C.F.R. § 42.8(b)(1), Petitioner certifies that Apple is the real party-in-interest, and further certifies that no other party exercised control or could exercise control over the filing of this petition or Apple’s participation in any proceeding instituted on this petition.

B. Related Matters

According to assignment records at the United States Patent and Trademark Office, the ’014 patent is currently owned by Sonrai Memory Limited (“Patent Owner” or “PO”).

The ’014 patent is asserted in the matter *Sonrai Memory Ltd. v. Apple Inc.*, 6:22-cv-00787 (WDTX).

The ’014 patent was the subject of a previously filed *inter partes review* – IPR 2021-01454 (hereinafter “’1454 IPR”). In the ’1454 IPR, prior Petitioner requested

institution of inter partes review of the '014 patent under the same grounds proposed in the present Petition. On March 4, 2022, the Board issued their decision instituting *inter partes* review of all of the challenged claims of the '014 patent on all grounds asserted in the former Petition. On October 12, 2022, the Board granted the joint Motion to Terminate the '1454 IPR proceeding following a settlement agreement between the parties. Although the Board had instituted *inter partes* review of the challenged claims, the Board did not decide the merits of the proceedings.

The present petition for *inter partes* review is also related to IPR2023-00819 that is substantially similar to the '1454 IPR. The '819 IPR was filed by Petitioner and presents substantially the same grounds as the '1454 IPR. The present petition presents different grounds from the '819 and '1454 IPRs.

C. Counsel

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D. Service Information, Email, Hand Delivery, and Postal

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III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies pursuant to Rule 42.104(a) that the patent for which review is sought is available for *inter partes* review, and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

Pursuant to Rules 42.22(a)(1) and 42.104(1)-(2), Petitioner challenges claims 1, 3, 5, 7, 11-13, and 15 of the '014 patent.

A. Prior Art Patents and Printed Publications

The '014 patent issued from U.S. Patent Application No. 09/865,605 ("'605 application"), filed on May 29, 2001. Petitioner applies prior art with a priority date earlier than the '605 application's filing date, May 29, 2001 ("Critical Date").

The following references are pertinent to the grounds of unpatentability:¹

1. U.S. Patent No. 6,314,501 ("Gulick"), filed as Application No. 09/215,424 on December 18, 1998, and issued on November 6, 2001, is prior art under at least 35 U.S.C. § 102(e).
2. Applicant Admitted Prior Art ("AAPA") in the '014 Patent.

¹ Because the '014 patent issued from an application filed prior to enactment of the America Invents Act ("AIA"), the pre-AIA statutory framework applies.

B. Grounds for Challenge

This Petition, supported by the declaration of Dr. Martin G. Walker (“Walker Decl.”) (EX1002), requests cancellation of claims 1, 3, 5, 7, 11-13, and 15 as being unpatentable under 35 U.S.C. § 103. *See* 35 U.S.C. § 314(a). The grounds for challenge include the following:

	Grounds	References	Challenged Claims
1.	§103	Gulick in view of Applicant Admitted Prior Art (AAPA)	1, 3, 5, 7, 11-13, 15
2.	§103	AAPA in view of Gulick	1, 3, 5, 7, 11-13, 15

V. OVERVIEW OF THE '014 PATENT AND THE PRIOR ART

A. Summary of the Alleged Invention

The '014 patent relates to “a multiprocessing chip utilizing multiple operating systems.” EX1001, 1:6-10. The '014 patent admits that multiprocessing systems with multiple processors on a single die were well-known, and it depicts an example of this known prior art single die multiprocessing system in Figure 2. EX1001, 1:34-59; 1:41-42 (explaining that it was well-known in the art to use “multiple processors on a single die” to conserve space in a system). EX1002, ¶38.

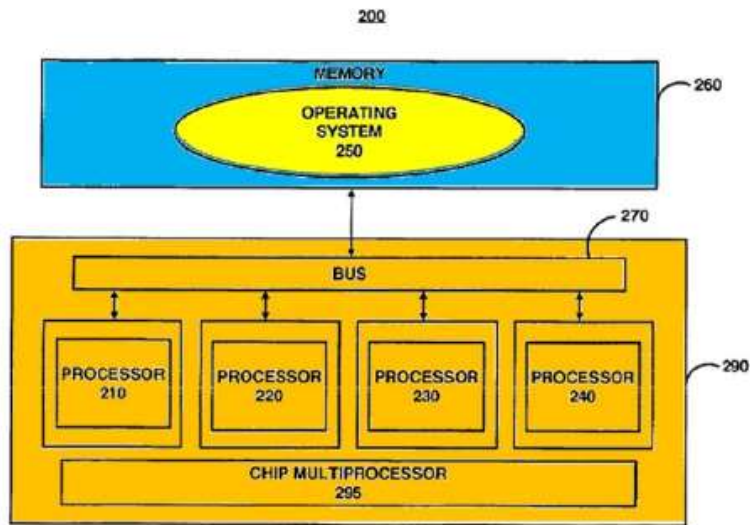


FIG. 2
Prior Art

EX1001, FIG. 2 (annotated).

The prior art multiprocessing system (200) includes a chip multiprocessor 295 that “includes multiple processors 210-240 on a single die 290” (highlighted orange). EX1001, 1:34-37. The processors 210-240 use an operating system 250 (highlighted yellow) stored in memory 260 (highlighted blue). EX1001, 1:37-40. The processors “may communicate with the memory 260 via a bus 270.” EX1001, 1:40-41. The ’014 patent states that “schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together.” EX1001, 1:44-47. The ’014 patent also acknowledges that it was known in the art that multiprocessor systems could “support[] multiple processors executing multiple operating systems.” EX1001, 1:60-63; EX1002, ¶39.

Unlike the AAPA system of FIG. 2 with multiple processors on a die and a

single operating system, the '014 patent discloses a “multiprocessing system” where “multiple processors are connected to a memory storing *multiple* operating systems,” as illustrated in Figure 3 below. EX1001, 2:12-16 (emphasis added)²; EX1002, ¶40.

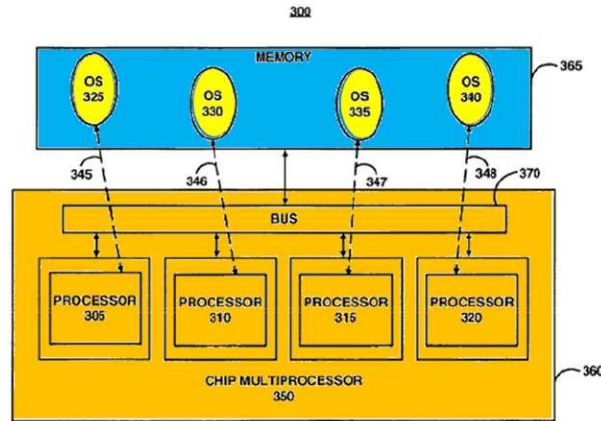


FIG. 3

EX1001, FIG. 3 (annotated), 2:54-55.

Like the prior-art system in FIG. 2, the computer system 300 in FIG. 3 includes a chip multiprocessor 350 having multiple processors 305-320 mounted on a single die (highlighted orange). EX1001, 3:4-7. The purported advance of the multiprocessing system is that it further includes multiple operating systems 325-340 (highlighted yellow) stored in a memory 365 (highlighted blue), rather than a single operating system 250 as shown in FIG. 2 above. EX1001, 3:10-11. The '014

² Unless otherwise noted, all emphases are added.

patent explains that “[d]uring operation, each processor 305-320 may access a respective operating system 325-340 by communicating with the memory 365, for example, via a bus 370.” EX1001, 3:11-14. The ’014 patent also explains that “[e]ach processor may be ... capable of simultaneously executing multiple operating systems, for example, by context switching, which may include rapidly switching between multiple operating systems.” EX1001, 3:47-51; EX1002, ¶41.

As explained below, all the limitations in the challenged claims were known in the prior art and obvious. *See infra* Section VII; EX1002, ¶42; *see also* EX1002 ¶¶18-.7 (technology background, citing Exhibits 1007-1017), ¶¶43-56 (discussing the prior art at issue in this petition), ¶¶71-275 (discussing prior art disclosures in view of each claim’s limitations).

B. Level of Ordinary Skill in the Art

A person having ordinary skill in the art (“POSITA”) for the ’014 patent would have had at least a bachelor’s degree in electrical engineering, computer science, computer engineering, or an equivalent, and at least two years of experience relating to the field of computer processor architecture. Additional education could substitute for experience in the field, and vice versa. EX1002, ¶¶15-17

C. Prosecution History

During prosecution, the Examiner issued a first Office Action mailed April 16, 2004. In the first Office Action, the pending claims were rejected under 35

U.S.C. § 102 as being anticipated by AAPA. EX1004, 121-126. In response, Applicant argued over the rejection without amendments. EX1004, 110-119. The Examiner issued a second Office Action mailed August 26, 2004. EX1004, 98-103. In the second Office Action, the pending claims were rejected as obvious over AAPA in view of US Patent No. 6,772,241 (“George”) (EX1011) and US Patent No. 6,526,462 (“Elabd”) (EX1012). *See id.* In distinguishing prior art, Applicant amended claim 1 to include the limitation “wherein . . . two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.” EX1004, 87-97 (PO amended claims 7 and 13 in a similar fashion). PO argued that the prior art of record did not disclose the “simultaneously executing” limitation. *Id.* Subsequently, the claims were allowed. EX1004, 77-80.

D. Overview of Gulick

Gulick discloses a multi-processor computer system that includes “one or more processor modules and a main memory having one or more memory storage units . . . that allows a plurality of operating systems to concurrently execute in different partitions within the computer system and allows the different partitions to communicate with one another through shared memory.” EX1005, 8:47-53. Gulick discloses a “multi-processor system that includes processor modules 110, 112, and 114” that “share access to main (or global) memory 160 . . . through a

system interconnection mechanism, such as system interconnection 130.”

EX1005, 10:53-67. Such arrangement allows processor modules 110-114 to

“communicate with each other through main memory 160.” EX1005, 10:64-67;

EX1002, ¶43.

Gulick discloses that the processor modules 110-114 “may be configured as a separate partition within the computer system, such that multiple partitions may exist within the computer system.” EX1005, 11:1-3. Each partition operates “under the control of a separate operating system.” EX1005, 11:4-5. For example, as shown below and disclosed in Gulick, “each processor module 110, 112, and 114 . . . can be defined as a separate partition controlled via a separate operating system 170, 172, and 174.” EX1005, 11:5-10, FIG. 1; EX1002, ¶44.

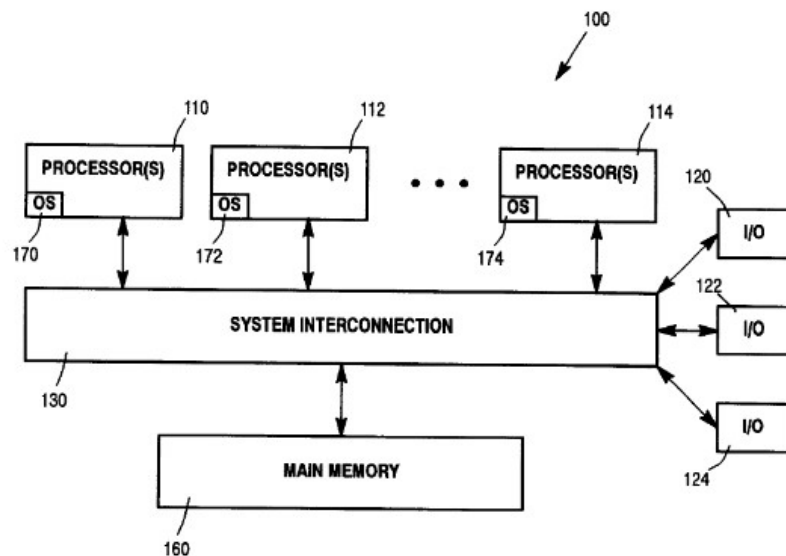


Figure 1

EX1005, FIG. 1.

Gulick disclose that “[e]ach operating system 170, 172 and 174 views main memory separately as though each is the only entity accessing main memory 160.”

EX1005, 11:8-10; EX1002, ¶45.

FIG. 2 illustrates components of an embodiment of the computing system shown in FIG. 1 in more detail. Computer system 200 includes main memory 160 and a plurality of processing modules 240 connected to main memory via third level cache modules 230 and crossbar interconnects 290. EX1005, 11:24-26; EX1002, ¶46.

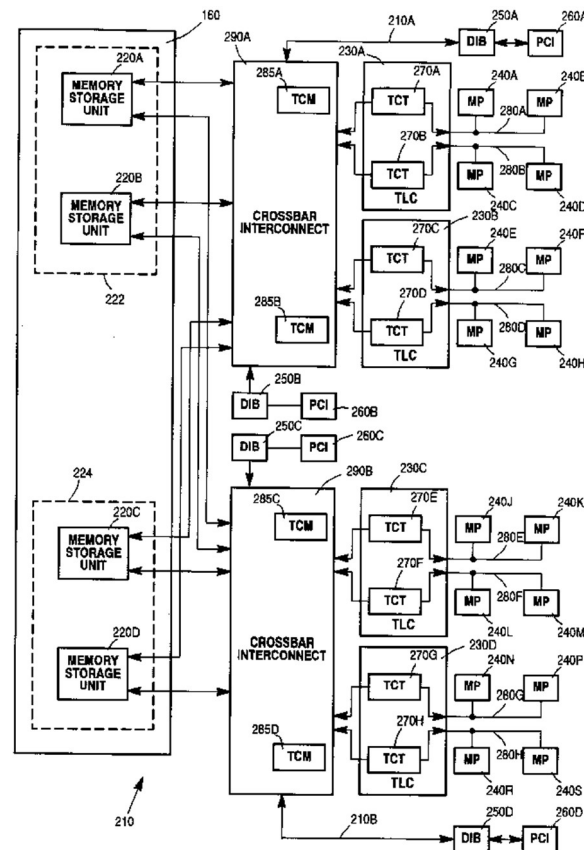
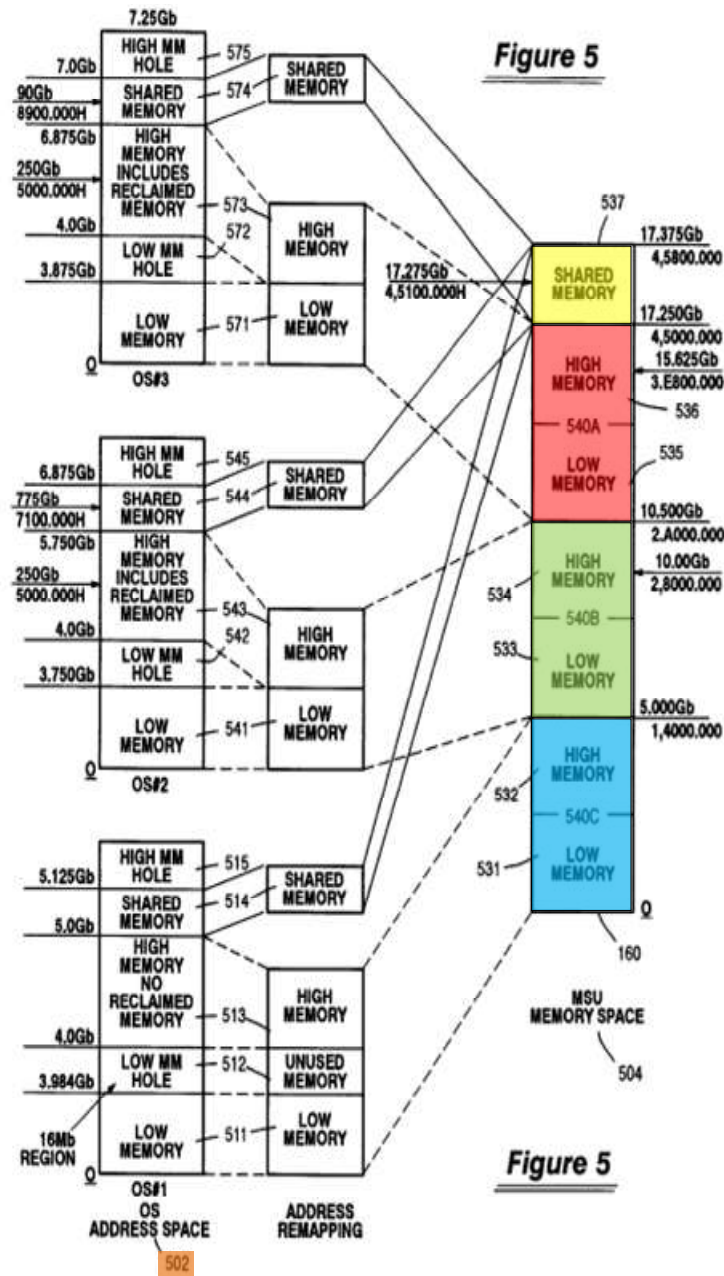


Figure 2

EX1005, FIG. 2.

Computer system 200 includes pairs of processors – processor 240A/processor 240B. Processor 240A and processor 240B “share a common bus (e.g., 280A) with a single [third level cache application specific integrated circuits] TCT (e.g., 270A) within a given [third level cache] TLC (e.g., 230A).” EX1005, 11:45-54. Gulick discloses that “each TLC 230 is connected to four processors” and that “[e]ach TLC 230 and its respective four processors define a sub-Pod.” EX1005, 11:57-60. Two sub-Pods “are connected via crossbar interconnect (e.g., crossbar interconnect 290A or 290B) to form a Pod.” EX1005, 11:60-62; EX1002, ¶47.

Computer system 200 includes “multiple partitions . . . each of which may comprise one or more Pods or sub-pods, each operates under the control of a separate operating system.” EX1005, 13:21-24. As shown in FIG. 5 (reproduced below), the memory configuration of computer system 200 includes “three operating systems” each of which “has its own address space 502.” EX1005, 13:30-36; EX1002, ¶48.



EX1005, FIG. 5.

FIG. 5 illustrates three memory windows (annotated red, green, blue, respectively) that “are defined within the address space 504 of main memory 160”

and a shared memory (annotated yellow), “which is accessible by all three operating systems.” EX1005, 13:37-43; FIG. 5. Gulick discloses that “the present invention contemplates an environment wherein at least two of the operating systems are different and one or more operating systems does not control or manage the second operating system.” EX1005, 13:26-29. In this manner, Gulick discloses a multi-processor computer system and method that allows for “multiple operating systems, including different operating systems, to operate in different partitions on the computer system.” EX1005, 2:37-56; EX1002, ¶49.

E. Overview of AAPA

The Memorandum entitled “Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311” (hereinafter, “AAPA Memo”) (EX1006) published by Katherine Vidal on June 9, 2022, establishes that it is appropriate for Petitioners to use AAPA as either a primary reference or a secondary reference. EX1006, 5.

The '014 patent admits that multiprocessing systems with multiple processors on a single die were well-known, and it depicts a known prior art system in FIG. 2 below. EX1001, 1:34-59; 1:41-42 (explaining that it was well-known in the art to use “multiple processors on a single die” to conserve space in a system); EX1002, ¶50.

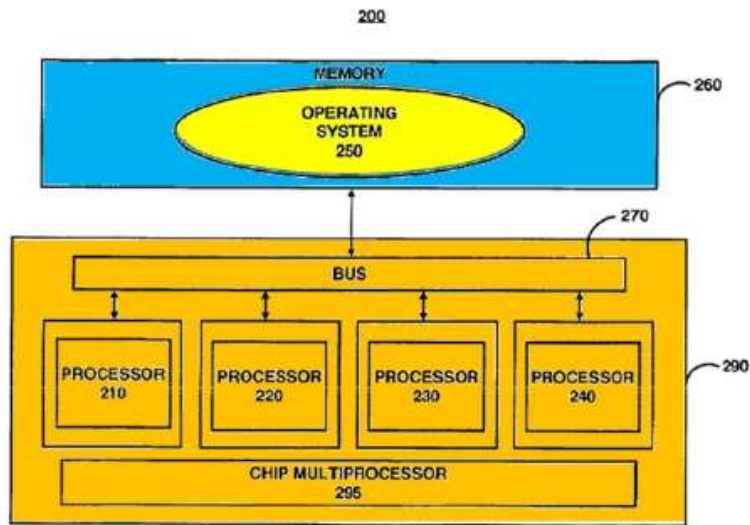


FIG. 2
Prior Art

EX1001, FIG. 2 (annotated).

Multiprocessing system 200 includes a chip multiprocessor 295 that “includes multiple processors 210-240 on a single die 290” (highlighted orange). EX1001, 1:34-37. Processors 210-240 use a single operating system 250 (highlighted yellow) stored in memory 260 (highlighted blue). EX1001, 1:37-40. Processors “may communicate with the memory 260 via a bus 270.” EX1001, 1:40-41. The ’014 patent states that “schemes that have placed multiple processors on a single chip typically utilize a single operating system for tying all the processors together.” EX1001, 1:44-47. The ’014 patent also admits that it was known in the art that multiprocessor systems could “support[] multiple processors executing multiple operating systems”. EX1001, 1:60-63; EX1002, ¶51.

VI. CLAIM CONSTRUCTION

Claims subject to *inter partes* review are to be “construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b), including construing the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-16 (Fed. Circ. 2005). The Board, however, only construes the claims when necessary to resolve the controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper no. 11 at 16 (Aug. 14, 2015). Aside from the terms addressed below, Petitioner submits that no express constructions of any of the terms are necessary and that the challenged claims should be interpreted according to their plain and ordinary meaning.³

³ Petitioner reserves all rights to raise claim construction and other arguments, including challenges under 35 U.S.C. §§ 101 or 112, in district court as relevant to those proceedings. *See, e.g., Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 11-13 (November 10, 2020). A comparison of the claims to

A. "simultaneously executing two or more operating systems"

In the currently pending litigation, Petitioner and PO have agreed that “simultaneously executing two or more operating systems” should be construed as “simultaneously executing two or more *independent* operating systems.” The Petition demonstrates that the challenged claims are obvious under this construction or under the plain meaning of the claim language. EX1002, ¶¶58-59.

B. “multiple operating systems residing in a memory”

In the currently pending litigation, Petitioner and PO have agreed that “multiple operations systems residing in a memory” should be construed as “multiple operating system residing in the same memory.” The Petition demonstrates that the challenged claims are obvious under this construction or under the plain meaning of the claim language. EX1002, ¶¶60-61.

**C. “multiple processors are connected to said memory via a bus”
(claim 3)**

In the currently pending litigation, Petitioner and PO have agreed that “multiple processors are connected to said memory via a bus” should be construed as “multiple processors are connected to said memory via the same bus.” The

any accused products in litigation may raise controversies that are not presented here given the similarities between the references and the patent.

Petition demonstrates that the challenged claims are obvious under this construction or under the plain meaning of the claim language. EX1002, ¶¶62-63.

D. “processor means for executing a plurality of operating system means” (claim 12)

In the currently pending litigation, Petitioner and PO have an agreed upon 35 U.S.C. § 112 ¶6 construction for “processor means.” The agreed-upon function is “executing a plurality of operating system means.” The agreed-upon structure is “chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360 as shown in Figure 3 and associated descriptions in the specification; or chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460 shown in Figure 4 and associated descriptions in the specification; and equivalents thereof.” The function and corresponding structure are substantially similar to those proposed by petitioner in the ’1454 IPR. EX1002, ¶64.

Further, to the extent the Board does not adopt the agreed upon construction, Petitioner submits that an alternative function of “processor means” is “simultaneously execute two or more operating system means of said plurality of operating system means.” The structure corresponding to this function is the same as the agreed-upon construction. EX1002, ¶65.

Additionally, to the extent that “processor means” is not a means plus function limitation, “processor means” should be construed according to its plain meaning. EX1002, ¶66.

E. “operating system means” (claim 12)

The “operating system means” phrase does not recite “means for” language. Instead, the “operator system means” only recites “means” and does not recite a function corresponding to the means. EX1001, 4:66, Claim 12. Accordingly, “operating system means” does not invoke 35 U.S.C. § 112 ¶6 and should be given its plain and ordinary meaning. *See Rodime PLC v. Seagate Tech., Inc.*, 174 F.3d 1294, 1302 (Fed. Cir. 1999). Further, this term is not subject to any claim construction dispute in the current litigation. EX1002, ¶68.

F. “memory means for storing said plurality of operating system means” (claim 12)

The “memory means” phrase recites “means for” language, which invokes 35 U.S.C. § 112 ¶6. EX1001, 5:1, Claim 12. The identified function of the “memory means” is “storing said plurality of operating system means.” EX1001, 5:1-2, Claim 12. The ’014 patent identifies as corresponding structure “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” EX1001, 3:15-20. EX1002, ¶69.

VII. SPECIFIC GROUNDS FOR PETITION

Pursuant to Rule 42.104(b)(4)-(5), the following sections, detail the grounds of unpatentability, the limitations of the challenged claims of the '014 patent, and how these claims are obvious in view of the prior art.

A. Ground 1: Claims 1, 3, 5, 7, 11-13, 15 are obvious over the combination of Gulick and AAPA

Gulick is highly relevant to claims 1, 3, 5, 7, 11-13, and 15 of the '014 patent. EX1002, ¶71.

1. Claim 1

a. A multiprocessing system comprising

To the extent the preambles are limiting, the Gulick-AAPA combination (hereinafter “Gulick-AAPA”) discloses the limitations therein. EX1002, ¶72.

Gulick discloses “a multi-processor system that includes processor modules 110, 112, and 114.” EX1005, 10:53-54; EX1002, ¶73.

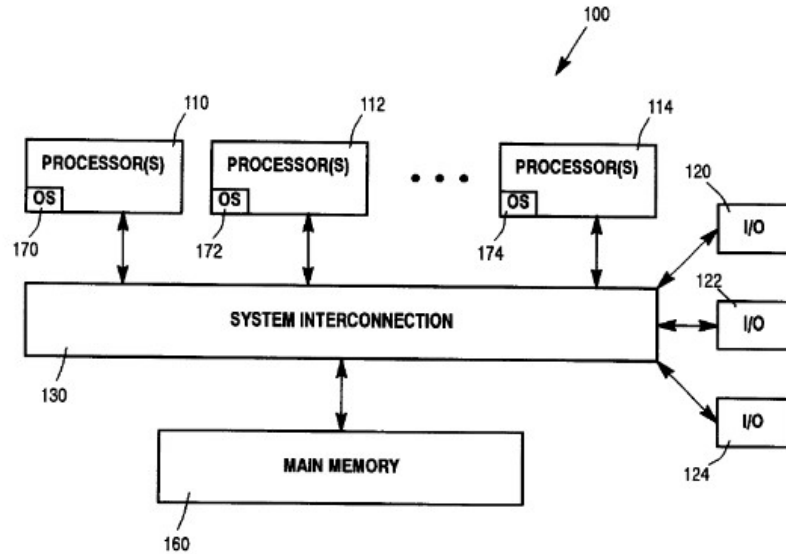


Figure 1

EX1005, FIG. 1.

Gulick discloses a more detailed description of an embodiment of the multi-processor system of FIG. 1. For example, as shown below, Gulick discloses “a computing system 200 . . . [that] includes a main memory . . . and a plurality of processing modules 240 connected to the main memory.” EX1005, 11:22-26, FIG. 2; EX1002, ¶74.

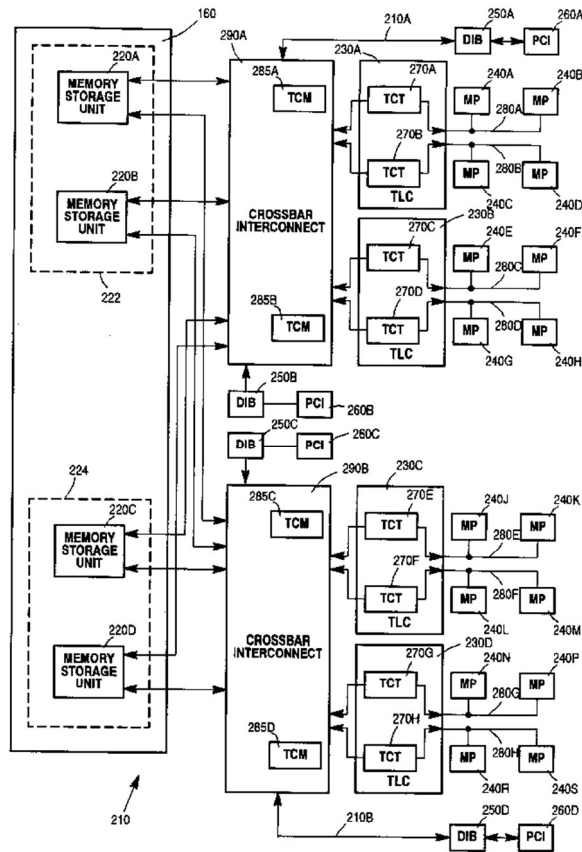


Figure 2

EX1005, FIG. 2.

Gulick states that “the processing modules and the main memory [as shown in FIG. 2] are arranged in a symmetrical *multiprocessing architecture*. EX1005, 11:28-32; EX1002, ¶75.

AAPA Fig. 2 likewise shows a conventional chip multiprocessor 295 in a computer system 200. EX1001, 1:34-59; 1:41-42; EX1002, ¶76.

Therefore, Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶77.

b. multiple processors mounted on a single die

Gulick-AAPA discloses this limitation. EX1002, ¶78.

Gulick discloses a computer system that includes processor modules 110-114 (highlighted green) labeled as “processor(s)” in Fig. 1. EX1005, 10:53-54. Each processor module 110-114 “can . . . include a plurality of processors.” EX1005, 10:59-60; EX1002, ¶79.

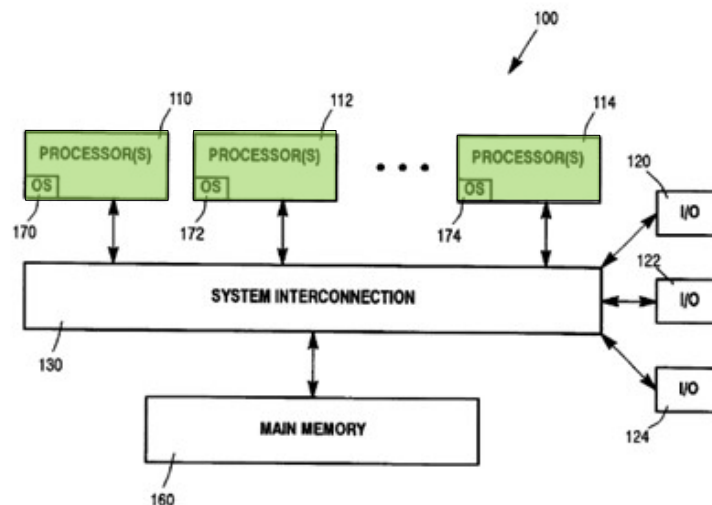


Figure 1

EX1005, FIG. 1 (annotated).

Gulick discloses computer system 200 that includes a plurality of processing modules 240 comprising processors 240A/240B-240R/240S (highlighted green). EX1005, 11:24-26; EX1002, ¶80.

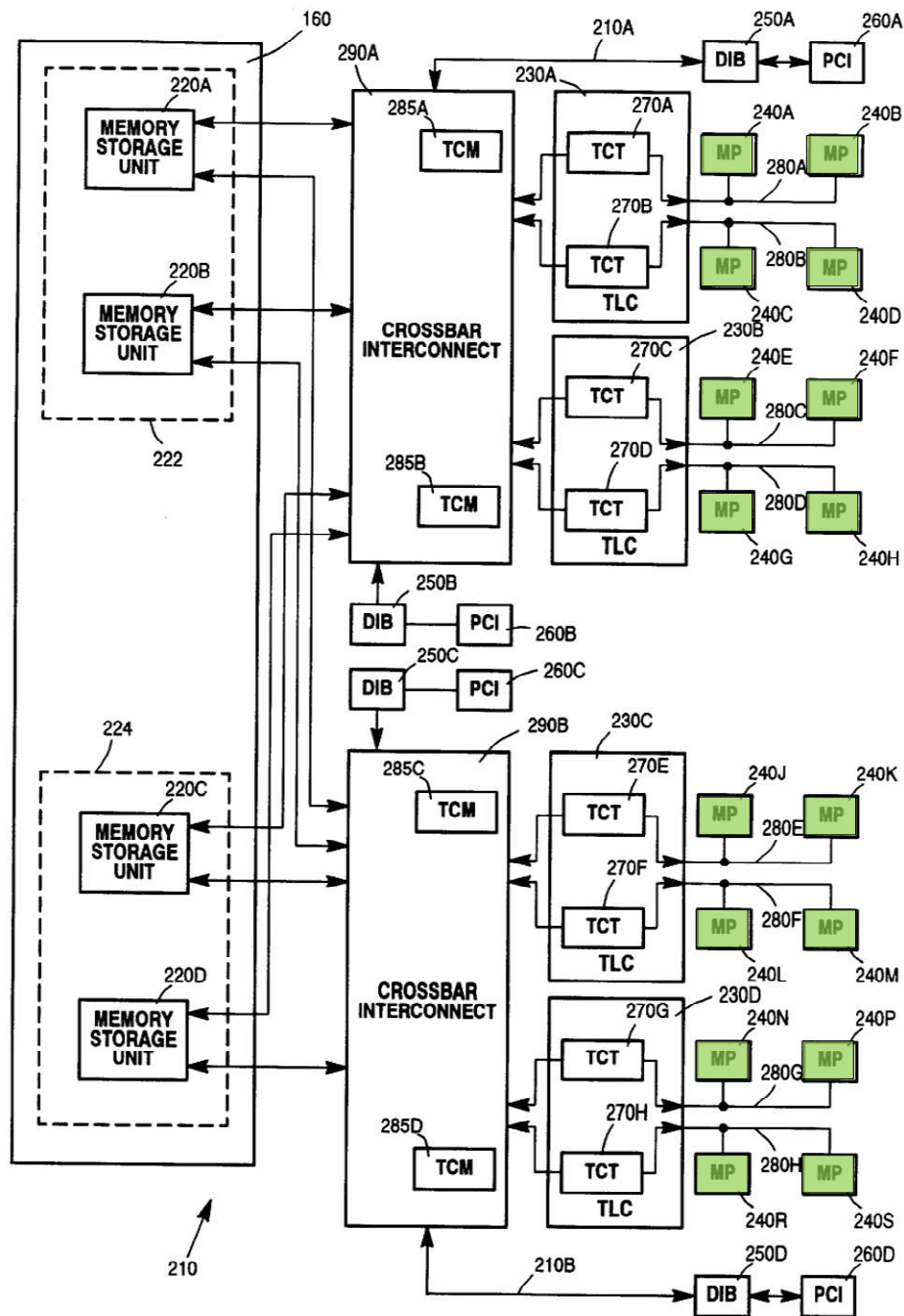


Figure 2

EX1005, FIG. 2 (annotated).

Computer system 200 includes “multiple partitions . . . each of which may comprise one or more Pods or sub-pods, each operates under the control of a

separate operating system.” EX1005, 13:21-24. Gulick discloses that a pod is formed from multiple sub-pods. EX1005, 11:60-62 (Two sub-Pods “are connected via crossbar interconnect (e.g., crossbar interconnect 290A or 290B) to form a Pod”). Gulick’s pods and sub-pods are “both examples of processing modules.” EX1005, 10:35-42. One or more processing modules form a partition operating under the control of its own operating system. EX1005, 9:41-46, 10:27-34; EX1002, ¶81.

Gulick also teaches that “the present invention contemplates other multiprocessing environments and configurations.” EX1005, 13:12-14. This further demonstrates to a POSITA that Gulick contemplates implementing a plurality of operating systems on a variety of conventional multiprocessors, including those disclosed in the AAPA. EX1002, ¶82.

To the extent that Gulick does not explicitly provide that the multiple processors are mounted on a single die, AAPA teaches doing so. EX1002, ¶83.

The ’014 patent discloses that it is well known for a computer system to have multiple processors mounted on a single die. For example, the ’014 patent discloses a “conventional multiprocessing scheme . . . [that] includes a computer system having a chip multiprocessor 295.” EX1001, 1:34-36; EX1002, ¶84.

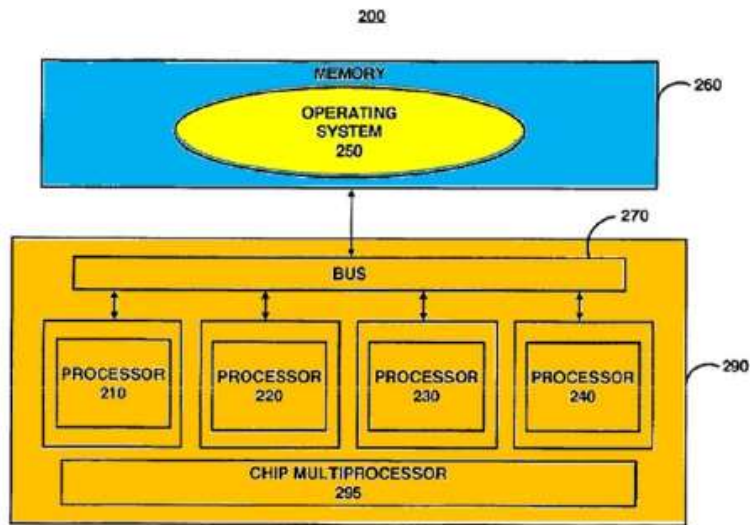


FIG. 2
Prior Art

EX1001, FIG. 2 (annotated).

The '014 patent provides that conventional multiprocessing schemes include a chip multiprocessor 295 that “includes multiple processors 210-240 on a single die 290” (highlighted orange). EX1001, 1:34-37; EX1002, ¶85.

As set forth in the AAPA Memo, patentee’s admissions regarding the scope and content of the prior art can be used to supply missing claim limitations that were generally known in the art prior to the invention. EX1006, 4. Accordingly, Petitioner’s use of AAPA to supply a missing claim limitation (i.e., use of a single die) is entirely proper.

A POSITA would have found it obvious in light of AAPA to configure the system in Gulick so that its multiple processors are “mounted on a single die,” as claimed, and would have had a reasonable expectation of success in so doing.

Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007). EX1002 ¶86.

A POSITA would have recognized that Gulick and AAPA disclose features in a similar technological field. For example, both Gulick and AAPA relate to multi-processor computing systems. EX1005, 10:53-54 (“FIG. 1 illustrates a multi-processor system that includes processor modules 110, 112, and 114”); EX1005, 11:28-32 (“the processing modules and the main memory [as shown in FIG. 2] are arranged in a symmetrical *multiprocessing architecture*”); EX1001, 1:34-36 (“A second conventional multiprocessing scheme (shown in FIG. 2) includes a computer system 200 having a chip multiprocessor 295.”). EX1002, ¶87.

Further, a POSITA would have been motivated to configure the system in Gulick so that its multiple processors are “mounted on a single die” to obtain benefits associated with using multiple processors on a single integrated circuit die that are applicable to any multiprocessing architecture, including Gulick’s, that the AAPA admits were known to a POSITA. For example, utilizing a single die is beneficial because it allows system 200 to conserve space by providing multiple processors on a single die. EX1001, 1:41-42. Additionally, in the AAPA “mounting multiple processors on a single die reduces the cabling problem inherent in connecting multiple processors on separate dies in separate houses,”

“reduces the latency for communication among the processors”, “improves the efficiency of message passing”, “reduces chip-to-chip communication costs”, “leads to further power efficiency”, and increases “scalability for multiprocessing.” EX1001, 2:26-38; EX1002, ¶88.

Therefore, consistent with the AAPA Memo, the patentee’s admissions both support a motivation to combine particular disclosures and demonstrates the knowledge of the ordinarily-skilled artisan at the time of the invention. EX1006, 4. Thus, Petitioner’s reliance on AAPA is proper. EX1002, ¶89.

Moreover, the following discussion includes examples that show that, consistent with AAPA, the benefits of having multiple processors on a single die in a multi-processor system were well known in the art. EX1002, ¶90. For example:

- combining processors on a single piece of silicon “outperforms multiple discrete processors by 50% or more” (EX1007, 1) and allows engineers to “take advantage of shorter distances and faster bus speeds when shuttling data between” the processors (*Id.*);
- “[s]ingle-chip multiprocessor architectures have the advantage in that they offer localized implementation of a high-clock rate processor for inherently sequential applications and low latency interprocessor communication for parallel applications.” EX1008, Abstract;

- “[m]ulti-core microprocessors feature a single integrated circuit that includes two or more main processing cores, each of which may be utilized as if it was a separate central processing unit” (EX1009, 1:37-47) and “each of the main cores provides computing power that equals or exceeds that of a conventional high-performance single core processor” (*Id.*);
- “[a]mong the benefits provided by multi-core processors is an increase in physical processing core density within multiprocessor data processing systems, in that more processing cores may operate within a given amount of space, which leads to improvements in overall multiprocessor system performance” (EX1009, 1:48-60); and
- “[t]he key questions for designers of future processors will not be whether to use chip multiprocessing, but the appropriate trade-off between the number of cores and the power of each core” (EX1010, 292).⁴

⁴ To show that claim 1 is obvious, Petitioner relies here on the teachings of Gulick and AAPA only. Exhibits 1007-1010 demonstrate what a POSITA would have known at the time of the alleged invention of the ’014 patent regarding the benefits

The '014 patent acknowledges using multiple processors mounted on a single die in a computer system as conventional and beneficial. For instance, the '014 patent describes a “conventional multiprocessing scheme (shown in FIG. 2) includes a computer system 200 having a chip multiprocessor 295” where “[t]he chip multiprocessor includes multiple processors 210-240 on a single die 290,” which saves space in the computer system. EX1001, 1:34-44, FIG. 2; EX1002, ¶91.

Thus, placing Gulick’s multiple processors (e.g., one or more pods) on a single die would have been a common-sense approach. EX1002, ¶92. For example, it was obvious to implement one or both pods comprising processors 240 in Fig 2 on a single die. EX1005, 11:33-54; EX1002, ¶92. (As discussed in more detail hereinbelow, Gulick discloses multiple operating systems operating on the processors of exemplary system of Fig. 2, with each operating system in a partition of one or more sub-pods. EX1005, 13:21-43.) A POSITA was motivated to do so by the many known advantages of single-die multiprocessors, including those

of having multiple processors on a single die. *Int’l Bus. Machines Corp. v. Intellectual Ventures II, LLC*, IPR2015-00089, Paper No. 44 at 15 (Apr. 25, 2016).

expressly taught by the AAPA: “mounting multiple processors on a single die reduces the cabling problem inherent in connecting multiple processors on separate dies in separate houses,” “reduces the latency for communication among the processors”, “improves the efficiency of message passing”, “reduces chip-to-chip communication costs”, “leads to further power efficiency”, and increases “scalability for multiprocessing.” EX1001, 2:26-38; EX1002, ¶92.

A POSITA would have had a reasonable expectation of success in implementing Gulick’s multiprocessing system on a single die as taught by AAPA because doing so was within the ordinary skill of a POSITA and did not require undue experimentation. Notably, the ’014 patent itself does not provide detail of how an AAPA single-die multiprocessor in FIG. 2 is configured to comprise multiple operating systems disclosed in embodiments of FIGs. 3 and 4. This is indicative of the fact that a POSITA understood how to implement a plurality of operating systems on a multiprocessor, including a single-die multiprocessor. EX1002 ¶93.

Moreover, Gulick provides details for implementing a plurality of operating systems that is applicable to any multiprocessor, including a modification of Gulick in view of AAPA to arrange processors 240 on a single die. For example, Gulick’s teaching of using dedicated memory windows for each operating system partition and a shared memory window for inter-OS communication functions

(e.g., Gulick, FIG. 5) enables implementation of multiple operating systems on a multiprocessor, including a single-die multiprocessor. EX1002, ¶94.

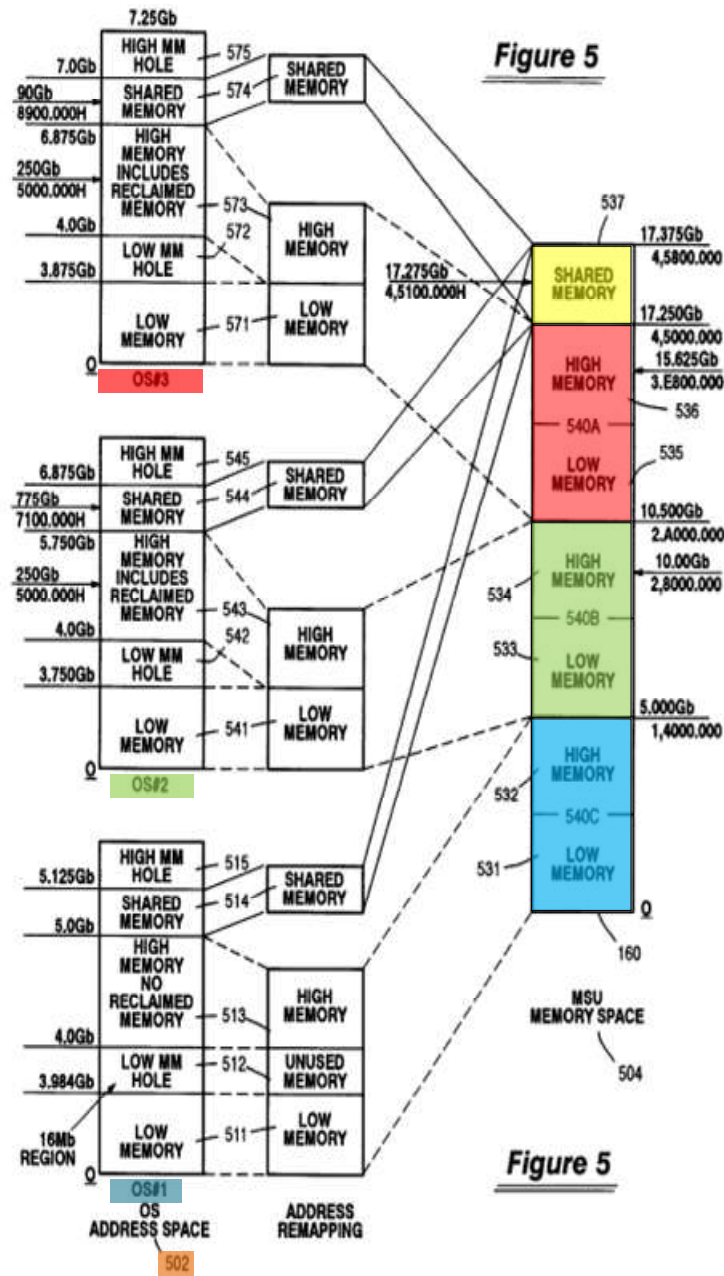
Therefore, based on AAPA and the knowledge in the art, it would have been obvious for the multiple processors in Gulick-AAPA to be mounted on a single die. EX1002, ¶95-96.

c. multiple operating systems residing in a memory connected to said multiple processors

Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶97.

Gulick discloses that its multi-processor system includes main memory 160. EX1005, 10:53-67. Main memory 160 “is a directory-based memory system and is capable of supporting various memory consistency models.” EX1005, 11:33-37. Main memory 160 “includes a plurality of memory storage units (MSUs) 220, such as memory storage units 220A, 220B, 220C, and 220D.” EX1005, 11:37-39; EX1002, ¶98.

FIG. 5 illustrates “an exemplary memory configuration that can be generated on the computer system of FIG. 2.” EX1005, 13:30-31. For example, as shown below, the memory configuration of computer system 200 includes “three operating systems” each of which “has its own address space 502.” EX1005, 13:30-36; EX1002, ¶99.



EX1005, FIG. 5 (annotated).

FIG. 5 illustrates three exclusive memory windows (annotated red, green, blue, respectively) that “are defined within the address space 504 of main memory

160” and a shared memory (annotated yellow), “which is accessible by all three operating systems.” EX1005, 13:37-43; FIG. 5. Gulick discloses that a memory window “is defined within the main memory to which multiple partitions have shared access.” EX1005, abstract. Thus, Gulick discloses that a memory window is a portion of the main memory. EX1002, ¶100.

Gulick discloses that each operating system resides in a respective memory window in main memory. Gulick discloses that “[f]or each different partition configured within the computer system, the main memory may further have defined therein an exclusive memory window to which only that partition has access and *in which* the operating system of that partition executes.” EX1005, 2:66-3:5; EX1002, ¶101.

A POSITA understands that if an operating system executes within a memory window assigned to the partition, then that operating system is stored in the memory window because the processor executes the operating system from the memory address where it is stored. EX1002, ¶102. In this regard Gulick also discloses that the “operating system is the first program code loaded into the main memory of a computer system after the computer system is turned on” and that the “central core of the operating system resides in the memory space *at all times*.” EX1005, 10:7-11. A POSITA would understand this teaching to refer to each

operating system residing in its memory window during operation. Thus, Gulick discloses “multiple operating systems residing in a memory.” EX1002, ¶102.

Further, Gulick discloses that the memory is “connected to said multiple processors.” EX1002, ¶103.

Gulick discloses that the processor modules 110-114 “may be configured as a separate partition within the computer system, such that multiple partitions may exist within the computer system.” EX1005, 11:1-3. Each partition operates “under the control of a separate operating system.” EX1005, 11:4-5. For example, as shown below, “each processor module 110, 112, and 114 . . . can be defined as a separate partition controlled via a separate operating system 170, 172, and 174.” EX1005, 11:5-10, FIG. 1; EX1002, ¶104.

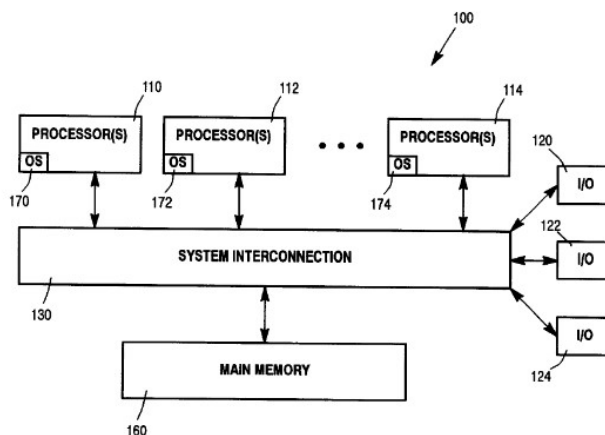


Figure 1

EX1005, FIG. 1.

Further, Gulick's computer system 200 includes main memory 160 (annotated red) and a plurality of processing modules 240 (annotated green) connected to main memory. EX1005, 11:24-28 ("Computer system 200 includes a main memory, illustrated here as main memory 160, and a plurality of processing modules 240 connected to the main memory via respective third level cache modules 230 and crossbar interconnects 290."). EX1002, ¶105.

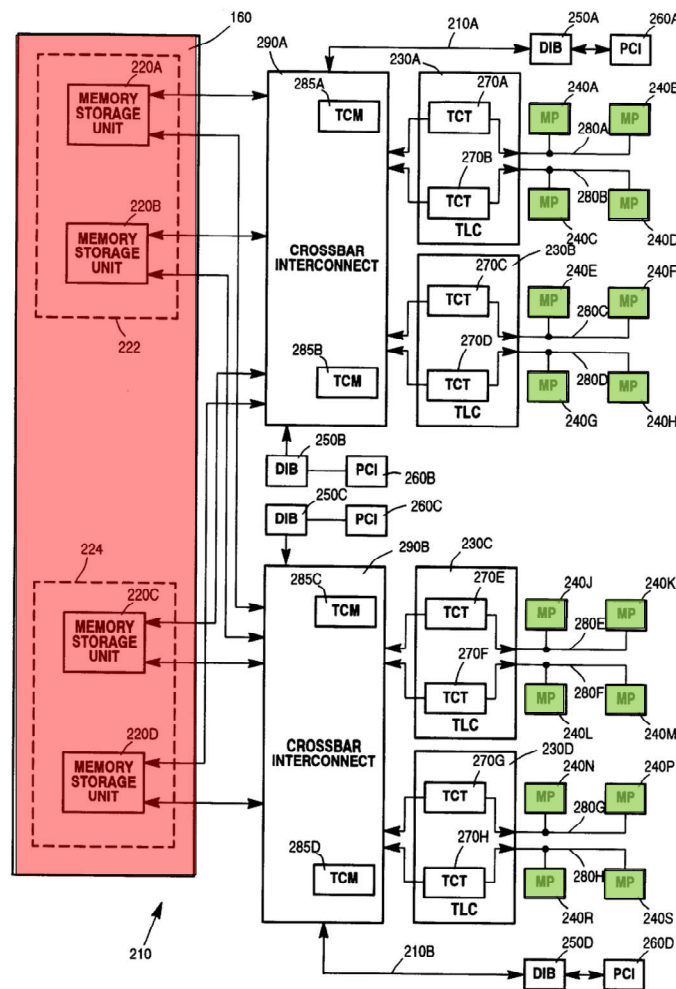


Figure 2

EX1005, FIG. 2 (annotated).

Thus, Gulick teaches that the memory is “connected to said multiple processors.” EX1002, ¶106.

Furthermore, a POSITA would have understood that placing the multiple processors on a single chip (*see supra* Section VII.A.1.b) would not have detracted from or changed the connection between the processors and memory in Gulick. Indeed, a POSITA would have recognized that in Gulick-AAPA, the processing modules 240, which comprise multiple processors mounted on a single die, would be connected to the memory (such as the main memory 160) where the multiple operating systems reside. EX1002, ¶107.

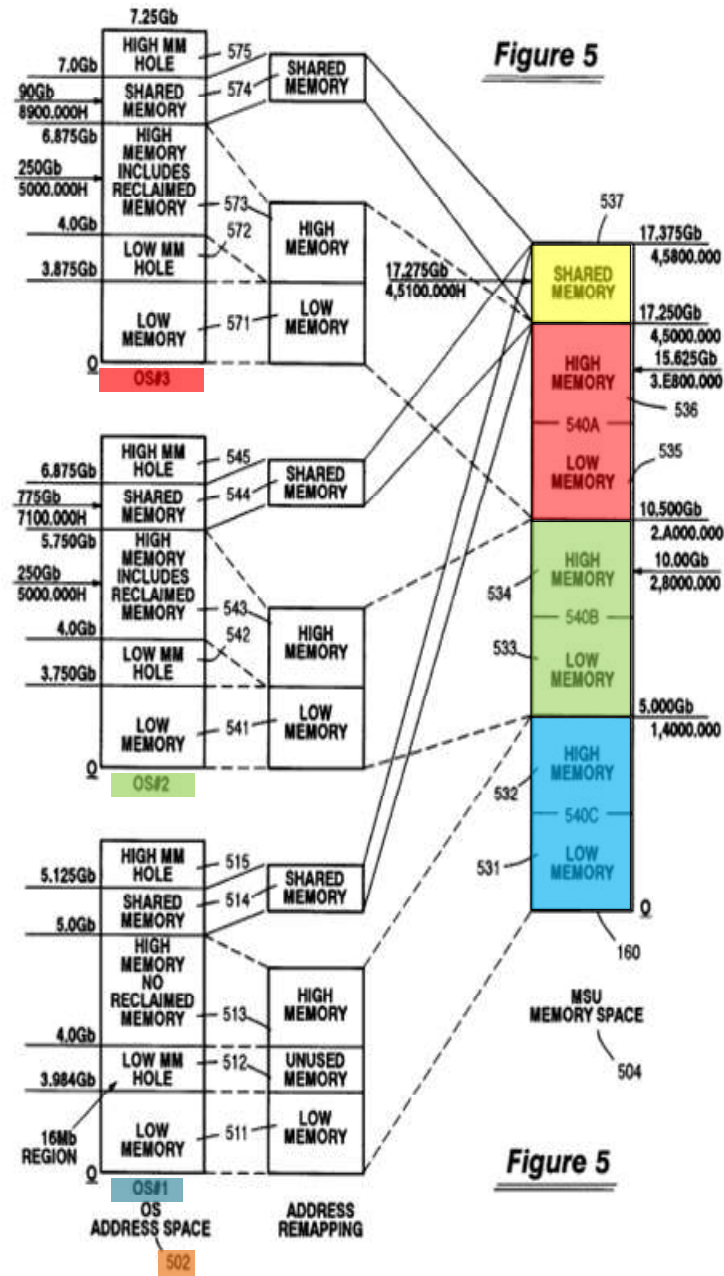
Thus, Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶108.

Further, to the extent that the Board adopts the agreed-upon District Court construction (“multiple operating systems residing in the same memory”) rather than plain meaning, Gulick-AAPA still discloses and/or suggests this limitation. EX1002, ¶109.

As stated, and shown in FIG. 5 above, “three exclusive memory windows 540A, 540B and 540C, one for each operating system (i.e., partition), and one shared memory window 537, which is accessible by all three operating systems 540A, 540B and 540C (i.e., partitions), are defined within the address space 504 of the main memory 160.” EX1005, 13:37-43; FIG. 5. A POSITA understands this

disclosure to teach that each operating system resides in the same main memory

160 as illustrated in the annotated FIG. 5 below. EX1002, ¶1110.



EX1005, FIG. 5 (annotated).

To emphasize this further, Gulick also discloses that the “central core of the operating system resides in the memory space at all times.” EX1005, 10:7-11. Accordingly, Gulick teaches that the multiple operating systems reside in the “same memory.” EX1002, ¶111.

Furthermore, there is no teaching in Gulick that would preclude the multiple operating systems from residing in the same memory. EX1002 ¶112.

Therefore, Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶113.

- d. wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems**

Gulick-AAPA discloses and/or suggests this limitation. EX1002 ¶114.

Gulick-AAPA includes multiple processors mounted on a single die and multiple operating systems connected to these multiple processors. *See supra* Sections VII.A.1.b-c. Each of these processors executes a respective operating system from the multiple operating systems, whereby two or more of the processors are capable of simultaneously executing two or more of the operating systems. EX1002, ¶115.

Gulick discloses that one or more processors is allocated to execute each operating system. For example, Gulick discloses “one or more processor modules and a main memory having one or more memory storage units . . . that allows a plurality of operating systems to concurrently execute in different partitions within the computer system.” EX1005, 8:47-53. Processor modules 110-114 “may be configured as a separate partition within the computer system, such that multiple partitions may exist within the computer system.” EX1005, 11:1-3. Each partition operates “under the control of a separate operating system.” EX1005, 11:4-5. For example, Gulick disclose that “each processor module 110, 112, and 114 . . . can be defined as a separate partition controlled via a separate operating system 170, 172, and 174.” EX1005, 11:5-10, FIG. 1; EX1002, ¶116.

Gulick further discloses that the “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as claimed. For example, Gulick discloses that the foregoing arrangement of components “allows a plurality of operating system to *concurrently execute* in different partitions within the computer system.” EX1005, 8:47-53; EX1002, ¶117.

Further, to the extent that the Board adopts the agreed-upon District Court construction of “simultaneously executing two or more operating systems” as

“simultaneously executing two or more independent operating systems,” Gulick-AAPA still teaches this limitation. EX1002, ¶118.

Gulick clearly states that “each partition operates under the control of its own operating system” and that “[t]he operating system executing on different ones of the partitions may be different operating systems, or different instances of the same operating system.” EX1005, 9:42-46; *see also* 13:27-29 (“the present invention contemplates an environment wherein at least two of the operating systems are different and one operating system does not control or manage the second operating system.”); EX1002, ¶119.

Thus, Gulick teaches this limitation under the agreed-upon construction. EX1002, ¶120.

Therefore, Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶121.

2. Claim 3

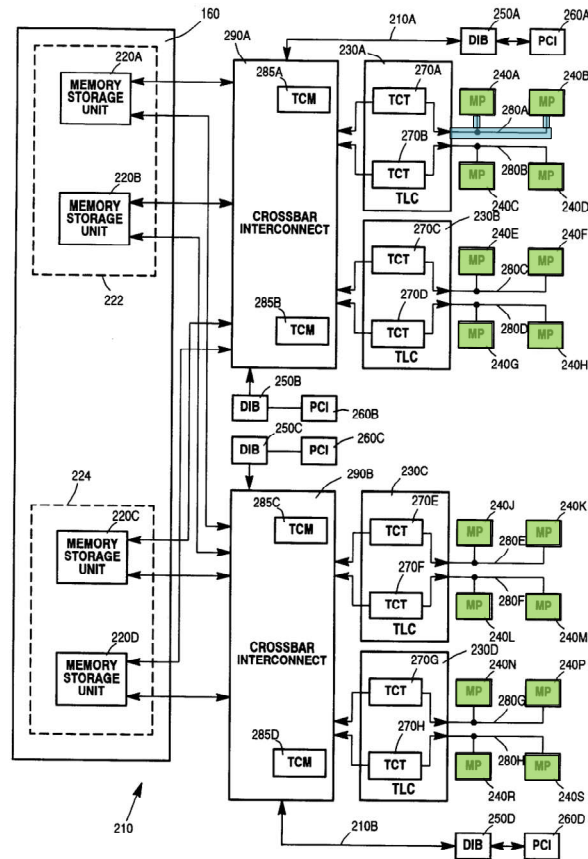
a. The system of claim 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems

Gulick-AAPA discloses and/or suggests this limitation. EX1002 ¶122.

As discussed for claim 1, Gulick discloses that the multiple processors are connected to the memory to execute the operating systems. *See supra* Sections VII.A.1.b-d. Gulick teaches that “[m]ain memory 160 includes a plurality of

memory storage units (MSUs) 220, such as memory storage units 220A, 220B, 220C, and 220D.” EX1005, 11:37-39. Each MSU 220A-22D “includes sixteen semi-independent banks that share four double-wide data busses and eight unidirectional address busses.” EX1005, 11:41-44. Each pair of processors (e.g., 240A and 240B) (annotated green) “share a common bus (e.g., 280A [annotated blue]) with a single TCT (e.g., 270A) within a given TLC (e.g., 230A).” EX1005, 11:48-51; EX1002, ¶123.

As shown in FIG. 2 below, such common bus allows processors 240A and 240B, for example, to be connected to memory. EX1002, ¶124.



EX1005, FIG. 2 (annotated).

Bus 280A connects processors 240A, 240B to third level cache module 230A. EX1005, 11:55-57 (“Each third level cache module 230A through 230D is connected to a respective plurality of processors (MPs) 240A through 240S.”). Each TLC 230A-230D is connected memory 160 via crossbar interconnects 290A-290B. EX1005, 11:24-28 (“Computer system 200 includes a main memory, illustrated here as main memory 160, and a plurality of processing modules 240 connected to the main memory via respective third level cache modules 230 and

crossbar interconnects 290.”); *see also* 11:66-12:1 (“Cross bar interconnects 290 interface processors 240, through third level caches 230, with memory storage units 220.”). EX1002, ¶125.

Moreover, the main memory 160 comprises MSU units 220A-D where each MSU “includes sixteen semi-independent banks that share four double-wide data busses and eight unidirectional address busses.” EX1005, 11:41-44. A POSITA would understand this disclosure to teach that the MSU banks are accessed by processors 240 via a memory bus comprising one or more data and address busses, as is conventional in the art. Accordingly, a POSITA would understand that the full main memory 160 is accessed by the processors through a memory bus. This arrangement in Gulick is consistent with the AAPA memory bus 270 which a POSITA would understand to comprise address and data busses. EX1002, ¶126.

Further, to the extent that the Board adopts the agreed-upon District Court construction (“multiple processors are connected to said memory via the same bus”), Gulick-AAPA likewise discloses and/or suggests this limitation. EX1002, ¶127.

Gulick discloses that processing modules 240 are “connected to the main memory via . . . crossbar interconnects 290.” EX1005, 11:24-28. For example, as shown in FIG. 2 below, multiple sub-pods (e.g., MP 240A-D = first sub-pod; MP

240E-H = second sub-pod) are connected to memory 160 via crossbar interconnect 290A. EX1002, ¶128.

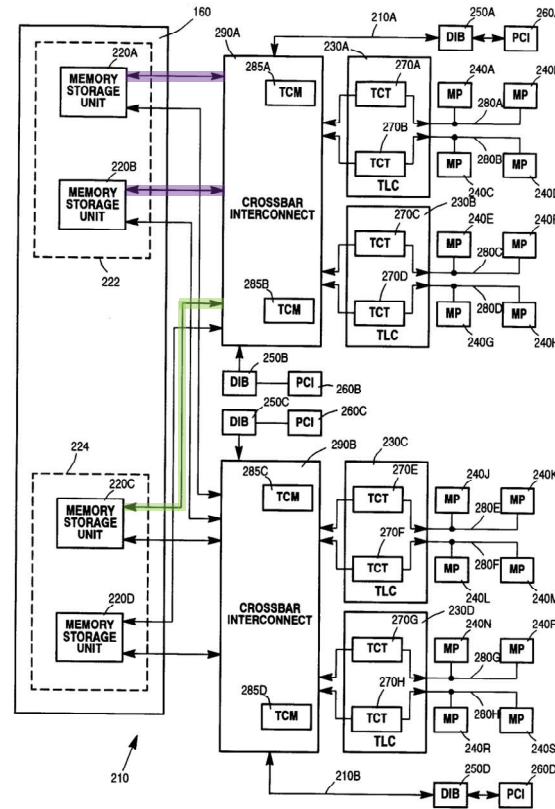


Figure 2

EX1005, FIG. 2 (annotated).

FIG. 2 illustrates first communication lines (annotated purple). First communication lines are bi-directional communications lines that relay address and data communications in two directions between the sub-pods and main memory 160. Although FIG. 2 of Gulick illustrates two lines (one for each MSU 220A-B), a POSITA would find it obvious to use the same bus to access shared memory. More specifically, a POSITA would understand that multiple sub-pods associated

with crossbar interconnect 290A would use the same bus to access MSU pair 222, with the bus connecting processors 240 to main memory 160 via crossbar interconnect 290A. EX1002, ¶129.

Gulick also discloses several other communication lines originating from crossbar interconnect 290A. For example, a second communication line (annotated green) connect crossbar interconnect 290A to MSU pair 224. Similar to the first communication lines discussed above, second communication line is bidirectional. A POSITA would understand that the first communication lines and the second communication line represent shared memory access that allows processors and sub-pods associated with crossbar interconnect 290 to access MSU pair 224 in addition to MSU pair 222. Such functionality allows for interleaved memory access, where each processor 240 distributes memory requests “over the global address space of main memory 160” in order to minimize contention. *See* EX1005, 22:24-30; *see also* 22:20-24; 23:44-24:56; EX1002, ¶130.

A POSITA would find it obvious to implement processor access to memory, such as MSU pairs 222/224, with the same memory bus. This conventional implementation was well-known and is illustrated in the AAPA as bus 270. A shared bus, such as AAPA bus 270, was obvious in Gulick because it is an efficient manner of connecting multiple processors to a shared memory, such as Gulick’s main memory 160, that avoids the duplication of resources if separate busses are

used to access memory. For example, a POSITA would understand that the crossbar interconnects 290 in Gulick were efficient to implement with a shared memory access bus to provide access to the entire memory space of main memory 160. On the other hand, an implementation with two busses would unnecessarily duplicate address, data and control line resources. A POSITA was therefore be motivated to implement the same memory access bus in Gulick between processors 240 and main memory 160 – a conventional solution illustrated by AAPA bus 270. EX1002, ¶131.

Accordingly, Gulick-AAPA discloses and/or suggests this limitation under the agreed-upon construction. EX1002, ¶132.

3. Claim 5

a. The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems

Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶133.

Gulick discloses “one or more processor modules and a main memory having one or more memory storage units . . . that allows a plurality of operating systems to concurrently execute in different partitions within the computer system and allows the different partitions to communicate with one another through shared memory.” EX1005, 8:47-53. Gulick also discloses that “each partition operates under the control of its own operating system” and that “[t]he operating system

executing on different ones of the partitions may be *different operating systems*, or *different instances* of the same operating system.” EX1005, 9:42-46; *see also* EX1005, 13:27-29 (“the present invention contemplates an environment wherein *at least two of the operating systems are different* and one operating system does not control or manage the second operating system.”); EX1002, ¶134.

Therefore, Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶135.

4. Claim 7

a. A multiprocessing system comprising:

To the extent that the preamble of claim 7 is limiting, Gulick-AAPA discloses this limitation. *See supra* Section VII.A.1.a; *infra* Section VII.A.4.b-d; EX1002, ¶136.

b. a plurality of processor groups mounted on a single die

Claim limitation 7.b varies from claim limitation 1.b in that it recites “groups” while claim limitation 1.b does not. *See supra* Section VII.A.1.b. Gulick-AAPA discloses claim limitation 7.b for at least the same reasons discussed above from claim limitation 1.b. EX1002, ¶137.

Further, each processor in the pairs of processors (e.g., processors 240A/240B-240R/240S) are mounted on a single die. *See supra* Section VII.A.1.b. These pairs of processors are necessarily groups in and of themselves. Even

further, Gulick discloses groups of processors as “one or more Pods or sub-pods” with each pod or sub-pod operating “under the control of a separate operating system.” EX1005, 13:21-24; *see also* EX1005, 11:45-60 (“each TLC 230 is connected to four processors” and “[e]ach TLC 230 and its respective four processors define a sub-Pod.”); EX1005, 11:60-62 (Two sub-Pods “are connected via crossbar interconnect (e.g., crossbar interconnect 290A or 290B) to form a Pod”); EX1002, ¶138.

Thus, Gulick-AAPA discloses and/or suggests this limitation. EX1002, ¶139.

c. multiple operating systems residing in a memory connected to said groups

Claim limitation 7.c varies slightly from claim limitation 1.c in that it recites “groups” while claim limitation 1.c does not. *See supra* Section VII.A.1.c.

Gulick-AAPA discloses claim limitation 7.c for at least the same reasons discussed above from claim limitation 1.c. *See supra* Section VII.A.1.c; EX1002 ¶140.

d. wherein each of said groups . . . two or more operating systems of said multiple operating systems

Claim limitation 7.d varies slightly from claim limitation 1.d in that it recites “groups” while claim limitation 1.d does not. *See supra* Section VII.A.1.d.

Gulick-AAPA system discloses limitation 7.d for at least the same reasons

discussed above from claim limitation 1.d. *See supra* Sections VII.A.1.d; EX1002 ¶141.

5. Claim 11

Claim 11 varies slightly from claim 5 (“wherein each of said processors executes a distinct operating system of said multiple operating systems”) in that it recites “groups” while claim 5 does not. *See supra* Section VII.A.3. Gulick-AAPA system discloses claim 11 for at least the same reasons discussed above from claim 5. *See supra* Section VII.A.3; EX1002, ¶142.

6. Claim 12

a. A multiprocessing apparatus comprising:

To the extent that the preamble of claim 12 is limiting, Gulick-AAPA discloses the limitations of the preamble for at least the reasons set forth above for claim limitation 1.a. *See supra* Section VII.A.1.a; *see infra* Section VII.A.6.b-d; EX1002, ¶143.

b. processor means for executing a plurality of operating system means, wherein said processor means includes a plurality of processors mounted on a single die

Gulick-AAPA discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitations 1.b-1.d, and for the additional reasons provided below. *See supra* Sections VII.A.1.b-VII.A.1.d; EX1002, ¶144.

(1) operating system means

Gulick-AAPA discloses and/or suggests an “operating system means,” as claimed. EX1002, ¶145; *see also supra* Section VI.B (construction of “operating system means” as a conventional operating system, such as WINDOWS NT, UNIX, and the like, or equivalents thereof).

Gulick’s system includes operating systems. *See supra* VII.A.1.c; EX1005, 11:1-10 (“According to the present invention, one or more processor modules may be configured as a separate partition within the computer system . . . each partition operating under the control of a separate operating system. For example, each processor module 110, 112 and 114 of FIG. 1 can be defined as a separate partition controlled via a separate operating system 170, 172 and 174. Each operating system 170, 172 and 174 views main memory separately as though each is the only entity accessing main memory 160.”). Gulick teaches that “the term ‘operating system’ refers to the program code that controls and coordinates the use of the hardware among the various application programs for various users.” EX1005, 10:4-7. The operating system can be inclusive of “off-the-shelf” operating systems “such as a version of Unix or Windows NT.” EX1005, 11:33-44; EX1002, ¶146.

Thus, Gulick-AAPA teaches “operating system means.” EX1002, ¶147.

(2) processor means

Gulick-AAPA discloses and/or suggests a “processor means,” as claimed. *See* Section VI.D (construction of “processor means”). For example, Gulick-AAPA discloses a computer system that includes processor modules 110-114. *See supra* Section VII.A.1.b; EX1005, 10:53-54. Gulick-AAPA also discloses a computer system that includes processor pairs 240A/240B- 240R/240S. *See supra* Section VII.A.1.b; EX1005, FIG. 2. As discussed above, a POSITA would have understood that processor modules 110-114 and/or processor pairs 240A/240B- 240R/240S can be mounted on a single die. *See supra* Section VII.A.1.b; EX1002, ¶148.

Thus, for this reason alone, Gulick-AAPA discloses “processor means.” EX1002, ¶149.

Further, to the extent the Board adopts the agreed-upon District Court construction, Gulick-AAPA likewise discloses this limitation. EX1002 ¶150.

The agreed-upon function for “processor means” is “executing a plurality of operating system means.” *See supra* Section VI.D. Gulick-AAPA system discloses that processors 110-114 and/or processors 240A/240B-240R/240S execute a plurality of operating systems. *See supra* Section VII.A.1.c-VII.A.1.d; *see also* EX1005, 8:47-53 (“one or more processor modules and a main memory having one or more memory storage units . . . that allows a plurality of operating systems to

concurrently execute in different partitions within the computer system and allows the different partitions to communicate with one another through shared memory.”). EX1002, ¶151.

Thus, Gulick-AAPA discloses the agreed-upon function for “processor means.” EX1002, ¶152.

Further, to the extent the Board does not adopt the agreed upon construction, Gulick-AAPA also teaches the function of “simultaneously execute two or more operating system means of said plurality of operating system means” under Petitioner’s proposed alternative construction for the reasons stated above. As indicated above, Gulick teaches that “one or more processor modules and a main memory having one or more memory storage units . . . that allows a plurality of operating systems to concurrently execute in different partitions within the computer system.” EX1005, 8:47-53. Thus, Gulick-AAPA discloses this function as well. The structure corresponding to this alternative function is the same as the agreed-upon construction and is met for the reasons stated below for that construction. EX1002, ¶153.

Gulick-AAPA also discloses the agreed-upon structure for “processor means.” EX1002, ¶154.

The agreed-upon structure for “processor means” is “chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360 as shown in

Figure 3 and associated descriptions in the specification; or chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460 shown in Figure 4 and associated descriptions in the specification; and equivalents thereof.”
See supra Section VI.D; EX1002, ¶155.

The '014 Patent discloses chip multiprocessor 350 (left, green). Similarly, Gulick discloses a chip multiprocessor (right, green). EX1002, ¶156.

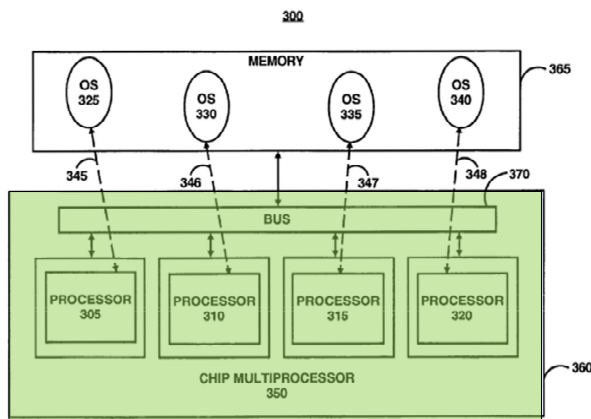


FIG. 3
The '014 Patent

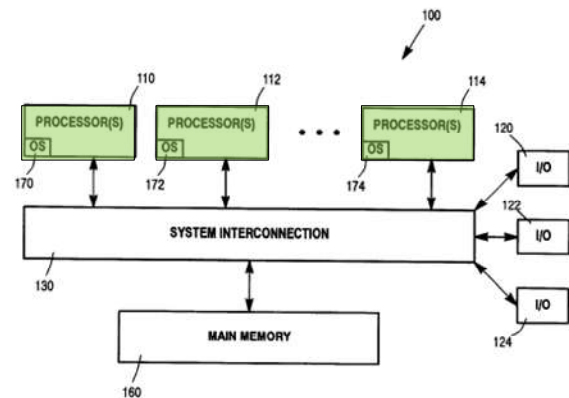


Figure 1
Gulick

The '014 Patent discloses that chip multiprocessor 250 includes four processors 305-320 (left, red). Similarly, Gulick discloses that computer system 200 includes processor pairs 240A/240B-240R/240S. EX1005, FIG. 2. Gulick discloses that computer system 200 includes “multiple partitions . . . each of which may comprise one or more Pods or sub-pods, each operates under the control of a separate operating system.” EX1005, 13:21-24. Gulick discloses that each TLC

230 and its four respective processors define a sub-pod. EX1005, 11:45-60;
EX1002, ¶157.

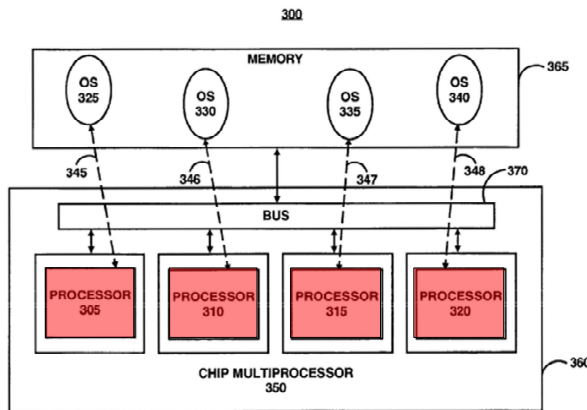


FIG. 3
The '014 Patent

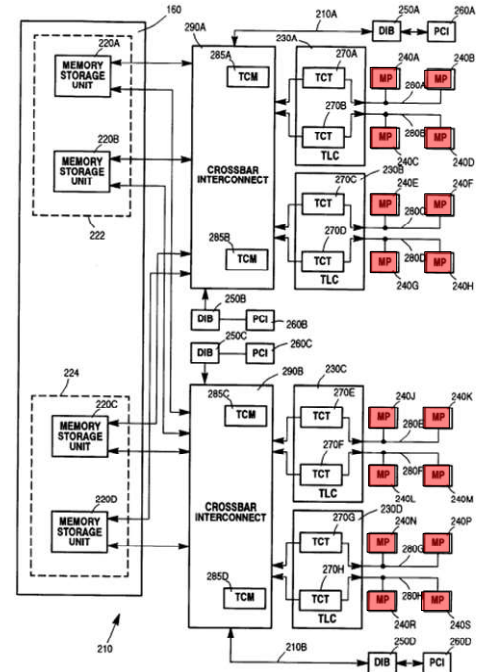


Figure 2

Gulick

Further, as indicated in Section VII.A.1.b, it would be obvious to modify Gulick's teachings with AAPA to have processors 240A/240B-240R/240S mounted on a single die. EX1002 ¶158.

In addition, the structure disclosed by Gulick-AAPA corresponds to the structure disclosed in the '014 patent. The '014 Patent discloses chip multiprocessor 450 (left, green). Similarly, Gulick discloses a chip multiprocessor (right, green). EX1002, ¶159.

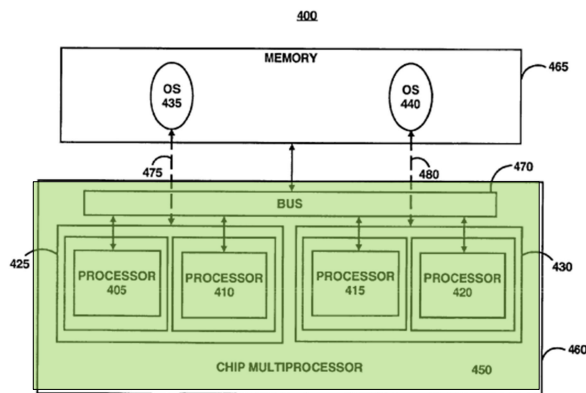


FIG. 4
The '014 Patent

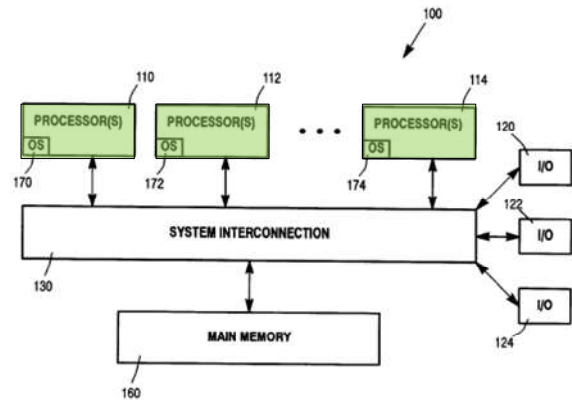


Figure 1
Gulick

The '014 Patent discloses that chip multiprocessor 450 has multiple processors 405-420 (left, red). Similarly, Gulick discloses that computer system 200 includes processor pairs 240A/240B-240R/240S. EX1005, FIG. 2. Gulick discloses that computer system 200 includes “multiple partitions . . . each of which may comprise one or more Pods or sub-pods, each operates under the control of a separate operating system.” EX1005, 13:21-24. Gulick discloses that each TLC 230 and its four respective processors define a sub-pod. EX1005, 11:45-60; EX1002, ¶160.

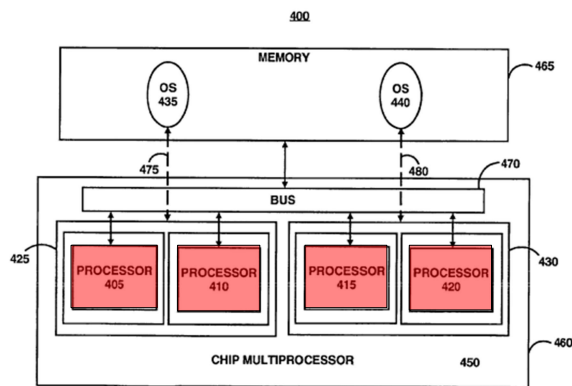


FIG. 4
The '014 Patent

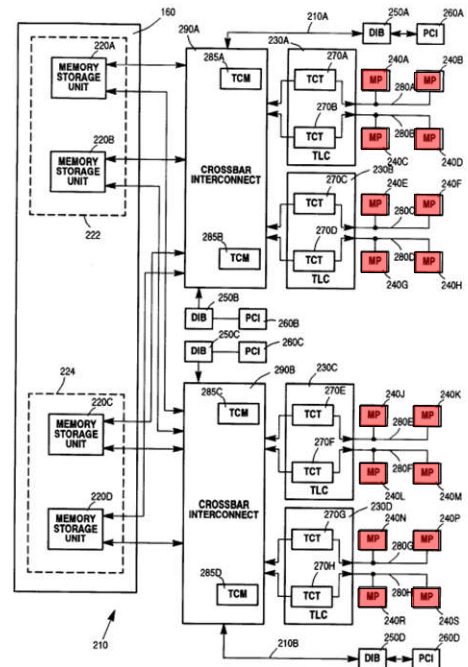


Figure 2

Gulick

Further, as indicated in Section VII.A.1.b, it would be obvious to modify Gulick's teachings with AAPA to have processors 240A/240B-240R/240S mounted on a single die. EX1002 ¶161.

Additionally, to the extent that “processor means” is not a means plus function limitation, “processor means” should be construed according to its plain meaning. *See supra* Section VI.D. The plain meaning is disclosed by Gulick-AAPA for the reasons already discussed. *See supra* Section VII.A.6.b; EX1002, ¶162.

Thus, Gulick-AAPA system discloses the corresponding structure. EX1002, ¶163.

- c. and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means**

Gulick-AAPA discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitation 1.d. *See supra* Section VII.A.1.d; EX1002, ¶164.

- d. memory means for storing said plurality of operating system means**

Gulick-AAPA discloses and/or suggests this limitation for at least the same reasons discussed above from claim limitations 1.c-1.d and for the additional reasons explained below. *See supra* Section VII.A.1.c-VII.A.1.d; EX1002, ¶165.

Gulick-AAPA discloses and/or suggests a “memory means for storing said plurality of operating system means” as claimed. EX1002, ¶166; *see also supra* Section VI.C.

Gulick-AAPA teaches the identified function of “memory means.” The identified function of “memory means” is “storing said plurality of operating system means.” *See supra* Sections VII.A.1.c-VII.A.1.d; EX1002, ¶167.

Gulick discloses that main memory 160 “includes a plurality of memory storage units (MSUs) 220, such as memory storage units 220A, 220B, 220C, and 220D.” EX1005, 11:37-39. In FIG. 5 of Gulick, the memory configuration of

computer system 200 includes “three operating systems” each of which “has its own address space 502.” EX1005, 13:30-36; EX1002, ¶168.

Thus, Gulick-AAPA discloses the identified function of “memory means.” EX1002, ¶169.

Gulick-AAPA also discloses the identified structure of “memory means.” The identified structure of “memory means” is “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” *See supra* Section VI.F; EX1002, ¶170.

Gulick defines the term “memory storage unit” as “a memory space capable of storing information.” EX1005, 10:21-22. Gulick teaches that “[e]ach memory storage unit includes a plurality of memory storage units, sometimes referred to as banks of DRAM (Dynamic Random Access Memory).” EX1005, 10:22-25; EX1002, ¶171.

Thus, Gulick-AAPA discloses the identified structure of “memory means.” EX1002, ¶172.

Therefore, Gulick-AAPA discloses this limitation. EX1002, ¶173.

7. Claim 13

Claim 13 varies slightly from claim 3 in that it recites a “processor means” and “memory means” while claim 3 does not. *See supra* Section VII.A.3. As

discussed above, Gulick-AAPA discloses a “processor means” (*see supra* Section VII.A.6.b) and “memory means” (*see supra* Section VII.A.6.d); EX1002, ¶174.

Accordingly, Gulick-AAPA discloses claim 13 for at least the same reasons discussed above from claim 3. *See supra* Section VII.A.2; EX1002, ¶175.

8. Claim 15

Claim 15 varies slightly from claim 5 in that it recites a “processor means” and “operating system means” while claim 5 does not. *See supra* Section VII.A.3. Gulick-AAPA system discloses a “processor means” (*see supra* Section VII.A.6.b(2)) and “operating system means” (*see supra* Section VII.A.6.b(1)). EX1002, ¶176.

Accordingly, Gulick-AAPA discloses claim 15 for at least the same reasons discussed above from claim 5. *See supra* Section VII.A.3; EX1002, ¶177.

B. Ground 2: Claims 1, 3, 5, 7, 11-13, 15 are obvious over the combination of AAPA and Gulick⁵

As indicated above, the AAPA memo clarifies that AAPA may be used in combination with reliance on at least one prior art patent or printed publication. *See supra* Section V.E. The AAPA memo makes clear that Petitioner’s reliance on

⁵ The subheadings in Section VII.A provide the claim language for all corresponding claims and claim limitations in Section VII.B

AAPA is proper because, as shown below, the Petitioner is using the admission as modified by the prior art Gulick reference. *See id.*

1. Claim 1

a. Limitation 1.a

To the extent the preambles are limiting, the AAPA-Gulick combination (hereinafter “AAPA-Gulick”) discloses the limitations therein. EX1002, ¶179.

AAPA discloses that multiprocessing systems with a multiprocessing chip were well-known, and it depicts a known prior art system single-die multiprocessor in Figure 2 below. EX1001, 1:34-59; EX1002, ¶180.

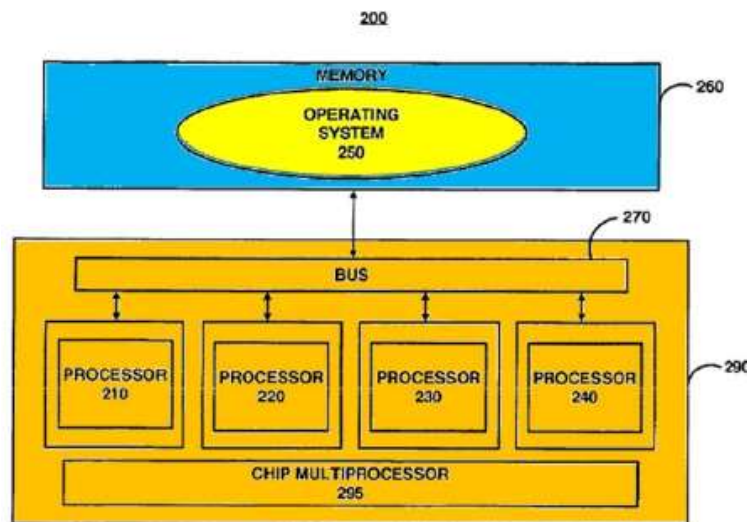


FIG. 2
Prior Art

EX1001, FIG. 2 (annotated).

AAPA discloses a multiprocessing system 200 that includes a chip multiprocessor 295 that “includes multiple processors 210-240 on a single die 290” (highlighted orange). EX1001, 1:34-37; EX1002, ¶181.

Therefore, AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶182.

b. Limitation 1.b

AAPA-Gulick discloses this limitation. EX1002, ¶183.

AAPA discloses that chip multiprocessor 295 includes “multiple processors 210-240 on a single die 290.” EX1001, 1:36-37, 1:41-42; EX1002, ¶184.

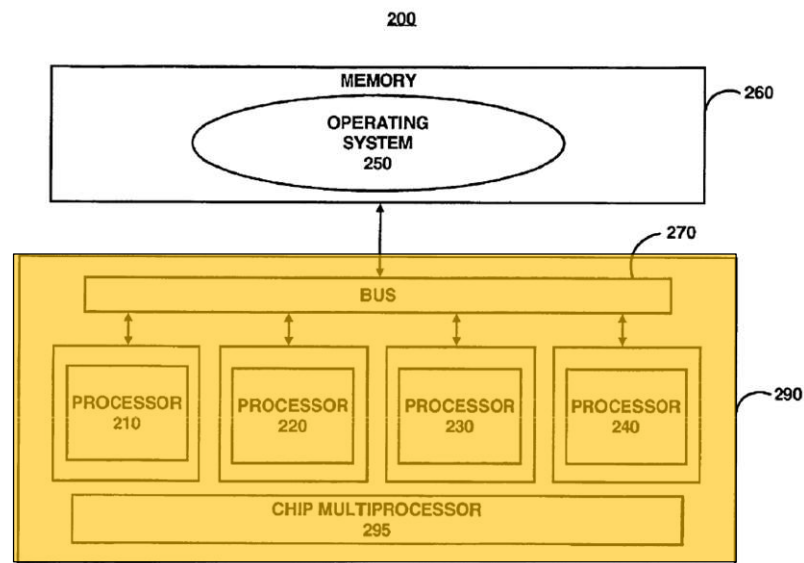


FIG. 2
Prior Art

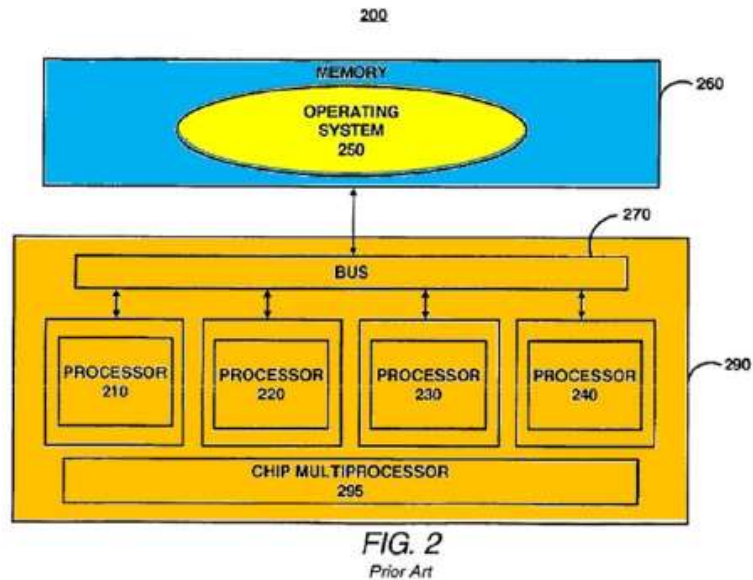
EX1001, FIG. 2 (annotated).

Therefore, AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶185.

c. Limitation 1.c

AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶186.

AAPA discloses that “processors 210-240 are connected to a single operating system 250 stored in a memory 260.” EX1001, 1:38-40; EX1002, ¶187.



EX1001, FIG. 2 (annotated).

Accordingly, AAPA discloses that multiple processors 210-240 on a single die 290 communicate with an operating system 250 residing in memory 260. EX1002, ¶188.

To the extent that AAPA does not disclose that there are multiple operating systems residing in memory, Gulick teaches doing so. EX1002, ¶189.

Gulick discloses, as shown below, “a multi-processor system that includes processor modules 110, 112, and 114.” EX1005, 10:53-54; EX1002, ¶190.

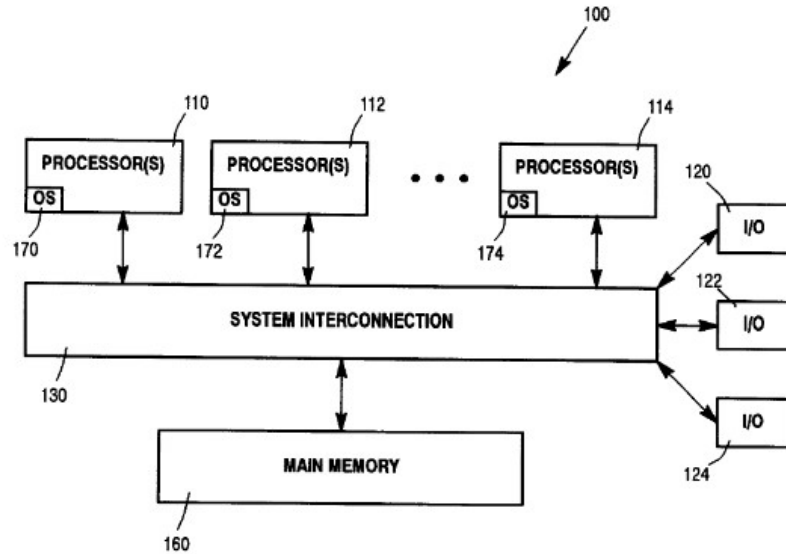


Figure 1

EX1005, FIG. 1.

Gulick discloses a more detailed description of an embodiment of the multi-processor system of FIG. 1 in FIG. 2. As shown below, Gulick discloses “a computing system 200 . . . [that] includes a main memory . . . and a plurality of processing modules 240 connected to the main memory.” EX1005, 11:22-26, FIG. 2; EX1002, ¶191.

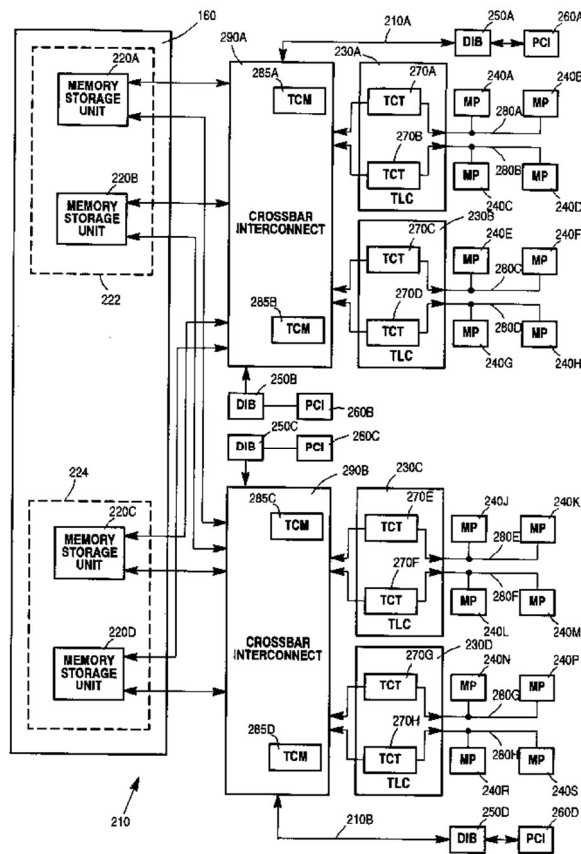


Figure 2

EX1005, FIG. 2.

Gulick discloses that multi-processor system includes main memory 160.

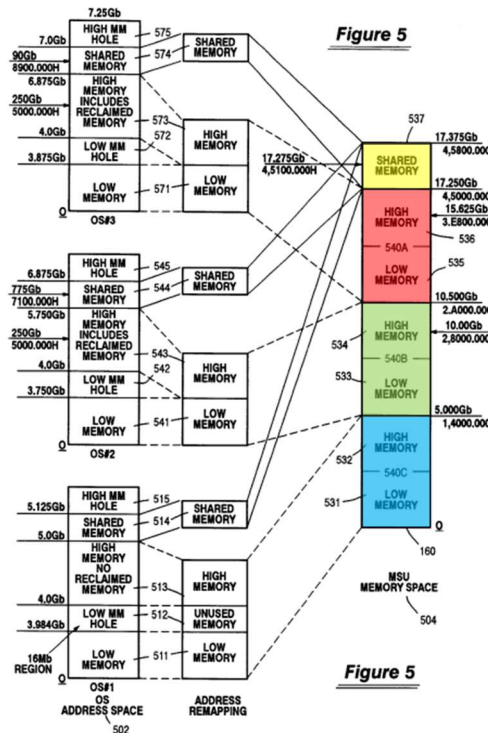
EX1005, 10:53-67. Main memory 160 “is a directory-based memory system and is capable of supporting various memory consistency models.” EX1005, 11:33-37.

Main memory 160 “includes a plurality of memory storage units (MSUs) 220, such as memory storage units 220A, 220B, 220C, and 220D.” EX1005, 11:37-39;

EX1002, ¶192.

FIG. 5 (reproduced below) illustrates “an exemplary memory configuration that can be generated on the computer system of FIG. 2.” EX1005, 13:30-31. The

memory configuration of computer system 200 includes “three operating systems” each of which “has its own address space 502” in the main memory. EX1005, 13:30-36; EX1002, ¶193.



EX1005, FIG. 5 (annotated).

FIG. 5 illustrates three exclusive memory windows (annotated red, green, blue, respectively) that “are defined within the address space 504 of main memory 160” and a shared memory (annotated yellow), “which is accessible by all three operating systems.” EX1005, 13:37-43; FIG. 5. Gulick discloses that a memory window “is defined within the main memory to which multiple partitions have shared access.” EX1005, abstract. Thus, Gulick discloses that a memory window is a portion of the main memory. EX1002, ¶194.

Gulick discloses that each operating system resides in a respective memory window in main memory. Gulick discloses that “[f]or each different partition configured within the computer system, the main memory may further have defined therein an exclusive memory window to which only that partition has access and *in which* the operating system of that partition executes.” EX1005, 2:66-3:5; EX1002, ¶195.

A POSITA understands that if an operating system executes within a memory window assigned to the partition, then that operating system is stored in the memory window because the processor executes the operating system from the memory address where it is stored. In this regard, Gulick also discloses that the “operating system is the first program code loaded into the main memory of a computer system after the computer system is turned on” and that the “central core of the operating system resides in the memory space *at all times*.” EX1005, 10:7-11. A POSITA would understand this teaching to refer to each operating system residing in its memory window during operation. Thus, Gulick discloses “multiple operating systems residing in a memory.” EX1002, ¶196.

A POSITA would have been motivated in light of Gulick to configure the system in the AAPA so that multiple processors reside in its memory as claimed. EX1002, ¶197.

Specifically, Gulick discloses that conventional computer systems typically employ a single operating system. EX1005, 2:29-31. Gulick further discloses that there are limitations with conventional computer systems employing a single operating system. As one example, Gulick discloses that “[a]s modern computer systems grow, and the demands of the user increases, the necessity of employing a plurality of operating systems increases.” EX1005, 2:32-34. Gulick then provides that “[w]hat is needed is a computer system and method for allowing multiple operating systems, including different operating systems, to operate in different partitions on the computer systems.” EX1005, 2:37-40; EX1002, ¶198.

The solution in Gulick addresses the very problems described in the ’014 Patent. For example, AAPA describes that as modern systems grow, the efficiency of operating systems goes down dramatically. EX1001, 1:50-53 (“as the number of processors managed by a single operating increases, the efficiency of the operating system goes down dramatically.”); EX1002, ¶199.

In other words, the solution in Gulick provides a known technique (e.g., increasing the number of operating systems employed by a multiprocessor computing device) to a known device (e.g., AAPA’s multiprocessor computer system 200) ready for improvement (as conceded by the AAPA) to yield predictable results (e.g., increasing the efficiency of the operating system of

computer system 200 by increasing the number of operating systems employed by computer system 200). *See* MPEP 2143(I)(D); EX1002, ¶200.

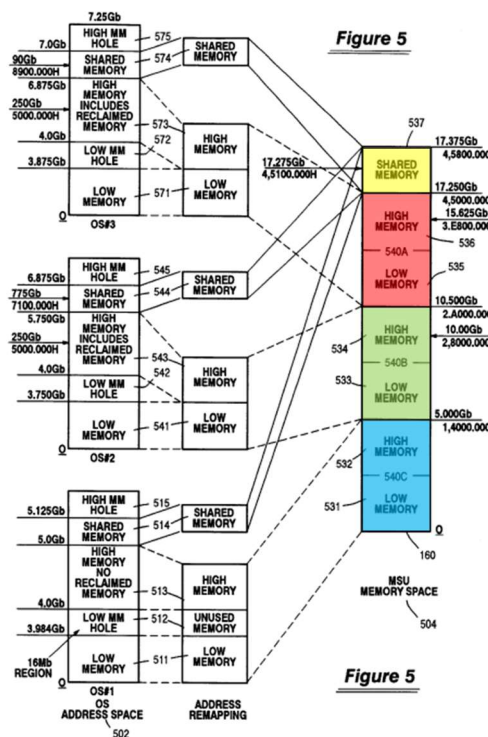
For this reason alone, a POSITA would have been motivated in light of Gulick to configure the memory as described by AAPA so that its memory includes multiple operating systems residing therein as claimed. EX1002, ¶201.

Further, as indicated above, in order to facilitate use of multiple operating systems, Gulick partitions its main memory 160. EX1005, 2:46-50 (“The present invention is directed to a computer system and methods for allowing multiple operating systems to operating in different partitions within a single computer architecture and for allowing the different partitions to communicate with one another through shared memory”); 8:47-53 (“The present invention is directed to a multi-processor computer system, having . . . a main memory having one or more storage units . . . that allows a plurality of operating systems to concurrently execute in different partitions within the computer system”); 8:53-56 (“The main memory is divided into a plurality of memory storage units”); 8:55-56 (“The main memory is allocated among the different partitions.”); 8:67-9:2. EX1002, ¶202.

Gulick broadly defines the term partition as “one or more processing module(s) that are under the control of a single operating system. The term partition is used herein to refer, in whole or in part, to the processing module(s) of

the partition, the operating system executing on the partition, any exclusive memory window assigned to the partition, other clients or application programs executing on the partition, or any combination thereof.” EX1005, 10:28-34; EX1002, ¶203.

Gulick shows an exemplary partitioned memory in FIG. 5, which illustrates “an exemplary memory configuration that can be generated on the computer system of FIG. 2.” EX1005, 13:30-31. For example, as shown in the memory configuration illustrated in FIG. 5 (reproduced below), the memory configuration of computer system 200 includes “three operating systems” each of which “has its own address space 502.” EX1005, 13:30-36; EX1002, ¶204.



EX1005, FIG. 5 (annotated).

A POSITA would be motivated to partition memory 250 of the AAPA into the multiple memory windows disclosed by Gulick in order to allow computer system 200 to employ multiple operating systems taught by Gulick. For example, as described above and exemplified in an annotated FIG. 2 of the AAPA below, partitioning memory 260 of computer system 200 would involve applying the known partitioning techniques described in Gulick in order for computer system 200 to employ multiple operating systems in its memory 260. EX1002, ¶205.

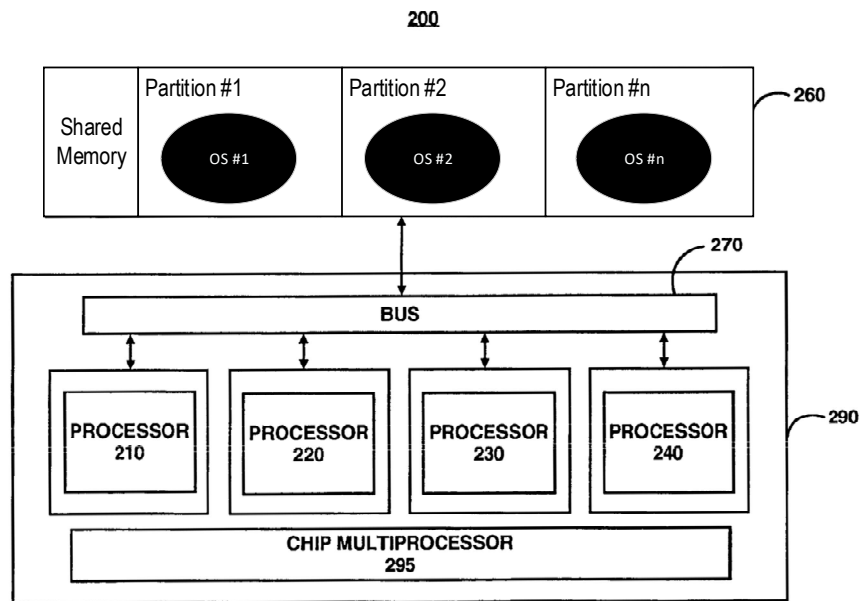


FIG. 2

Prior Art

Annotated
based on
Gulick

FIG. 2 (annotated).

Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable

results. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007). EX1002, ¶206.

Further, to the extent that the Board adopts the narrower agreed-upon District Court construction (“multiple operating systems residing in the same memory”) rather than plain meaning, AAPA-Gulick still discloses and/or suggests this limitation. As illustrated above, the multiple operating systems are stored in the same memory 260. *See supra* Section VII.A.1.d; EX1002, ¶207.

Therefore, AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶208.

d. Limitation 1.d

AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶209.

AAPA-Gulick includes multiple processors mounted on a single die and multiple operating systems residing in memory that are connected to these multiple processors. *See supra* Sections VII.B.1.b-c. Each processor executes an operating system from the multiple operating systems, whereby two or more of the processors are capable of simultaneously executing two or more of the operating systems. EX1002, ¶210.

AAPA discloses that processors 210-240 are connected to memory 260. EX1001, 1:37-40. A POSITA would understand that, when AAPA’s memory 260 is partitioned as taught by Gulick to include multiple operating systems, each of the

processors 210-240 would execute at least one of the operating systems. EX1002, ¶211.

To the extent that AAPA does not explicitly disclose that processors 210-240 are capable of simultaneously executing two or more of the operating systems, Gulick teaches doing so. EX1002, ¶212.

Gulick discloses that one or more processors is allocated to execute an operating system. Processor modules 110-114 “may be configured as a separate partition within the computer system, such that multiple partitions may exist within the computer system.” EX1005, 11:1-3. Each partition operates “under the control of a separate operating system.” EX1005, 11:4-5. Gulick discloses that “each processor module 110, 112, and 114 . . . can be defined as a separate partition controlled via a separate operating system 170, 172, and 174.” EX1005, 11:5-10, FIG. 1; EX1002, ¶213.

Gulick further discloses that the “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems,” as claimed. For example, Gulick disclose that the foregoing arrangement of components “allows a plurality of operating system to *concurrently execute* in different partitions within the computer system.” EX1005, 8:47-53. Thus, Gulick teaches multiple processors capable of

concurrently or simultaneously executing two or more operating systems.

EX1002, ¶214.

A POSITA would be motivated by the teachings of Gulick to modify the operations of the AAPA such that the operating systems 210-240 of AAPA could simultaneously execute two or more operating systems residing in memory 260. Such combination involves applying a known technique (e.g., executing two or more operating systems concurrently as described in Gulick) to a known device (e.g., AAPA's computer system 200) to yield predictable results (e.g., executing two or more operating systems within AAPA's computer system 200). EX1002, ¶215.

Thus, AAPA-Gulick discloses this limitation. EX1002, ¶216.

Further, to the extent that the Board adopts the agreed-upon District Court construction of “simultaneously executing two or more operating systems” as “simultaneously executing two or more independent operating systems,” AAPA-Gulick still teaches this limitation. EX1002, ¶217.

Gulick clearly states that “each partition operates under the control of its own operating system” and that “[t]he operating system executing on different ones of the partitions may be different operating systems, or different instances of the same operating system.” EX1005, 9:42-46; *see also* EX1005, 13:27-29 (“the present invention contemplates an environment wherein at least two of the operating systems are different and one operating system does not control or

manage the second operating system.”). A POSITA would recognize that Gulick’s disclosure of different operating systems that do not control or manage other operating systems is an example of independent operating systems. EX1002, ¶218.

Thus, AAPA-Gulick teaches this limitation under the agreed-upon construction. EX1002, ¶219.

2. Claim 3

AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶220.

AAPA-Gulick discloses that multiple processors are connected to memory to execute the operating systems. *See supra* Section VII.B.1. AAPA further discloses that the computer system 200 establishes connections between processors 210-240 and memory 260 via a bus 270. EX1001, 1:40-41 (“The processors 210-240 may communicate with the memory 260 via a bus 270”); EX1002, ¶221.

Accordingly, a POSITA would have understood that the system in AAPA-Gulick would have included a bus that connects the multiple processors with the main memory to execute instructions from the various operating systems and process data. EX1002, ¶222.

Thus, AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶223.

Further, to the extent that the Board adopts the agreed-upon District Court construction (“multiple processors are connected to said memory via the same

bus”), AAPA-Gulick likewise discloses and/or suggests this limitation. EX1002, ¶224.

AAPA discloses that “processors 210-240 may communicate with the memory 260 via a bus 270.” EX1001, 1:40-41; FIG. 2. Only a single bus 270 (highlighted purple) is illustrated in FIG. 2 of the ’014 Patent. EX1001, FIG. 2; EX1002, ¶225.

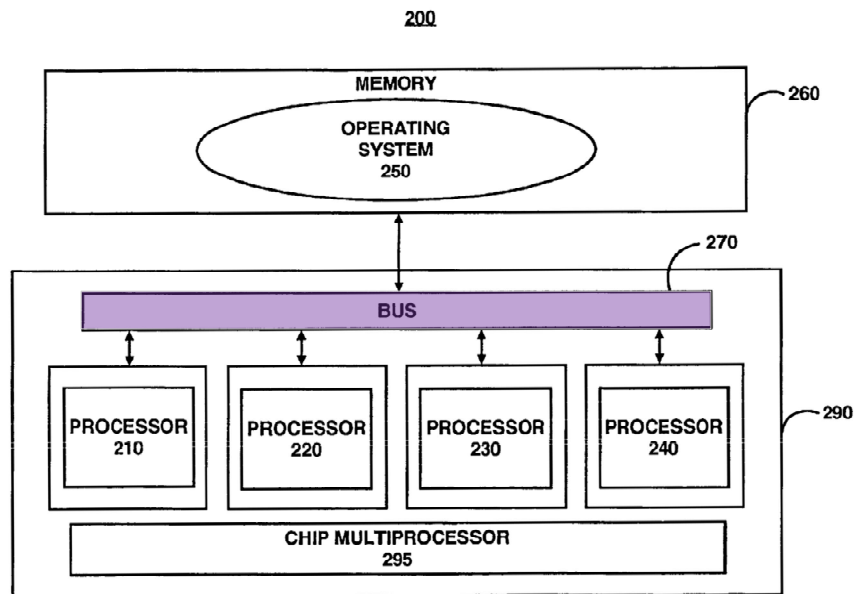


FIG. 2
Prior Art

EX1001, FIG. 2 (annotated).

Accordingly, under the agreed-upon construction, AAPA-Gulick still discloses and/or suggests this limitation. EX1002, ¶226.

3. Claim 5

AAPA-Gulick discloses and/or suggests this limitation. EX1002, ¶227.

AAPA-Gulick discloses that multiple processors are connected to memory to execute multiple operating systems. *See supra* Section VII.B.1. AAPA-Gulick further discloses that the computer system 200, or, more specifically, processors 210-240, are capable of “simultaneously executing two or more independent operating systems.” *See supra* Section VII.B.1.d; EX1002, ¶228.

Gulick further discloses that the operating systems residing in memory may be different operating systems. For example, Gulick discloses “[t]he operating systems executing on different ones of the partitions may be different operating systems, or different instances of the same operating system.” EX1005, 9:42-46. Gulick further discloses that “the present invention contemplates an environment wherein at least two of the operating systems are different and one operating system does not control or manage the second operating system.” EX1005, 13:27-29; EX1002. ¶229.

A POSITA would be motivated by the teachings of Gulick to modify the operations of the AAPA such that the processors 210-240 of AAPA could execute a distinct operating system of the operating systems residing in memory 260. As discussed for claim 1 above, such a combination involves a simple substitution of one known element for another to obtain predictable results. *See supra* Section VII.A.1.c; EX1002, ¶230.

4. Claim 7

a. Limitation 7.a

To the extent that the preamble of claim 7 is limiting, AAPA-Gulick discloses the limitations of the preamble for at least the reasons set forth above for claim limitation 1.a. *See supra* Section VII.B.1.a; *infra* Section VII.B.4.b-d; EX1002, ¶231.

b. Limitation 7.b

Claim limitation 7.b varies from claim limitation 1.b in that it recites “groups” while claim limitation 1.b does not. *See supra* VII.B.1.b. AAPA-Gulick discloses claim limitation 7.b for at least the same reasons discussed above for claim limitation 1.b. EX1002, ¶232.

Further, to the extent that “group” is construed as containing more than one processor (which Petitioner does not concede), AAPA-Gulick still discloses claim limitation 7.B. EX1002, ¶233.

AAPA discloses that multiple processors are managed by a single operating system. EX1001, 1:50-54 (“as the number of processors managed by a single operating system increases, the efficiency of the operating system goes down dramatically.”). Further, AAPA shows, in FIG. 2 reproduced below, a group of processors 210-240 on a single die 290. EX1001, FIG. 2; EX1002, ¶234.

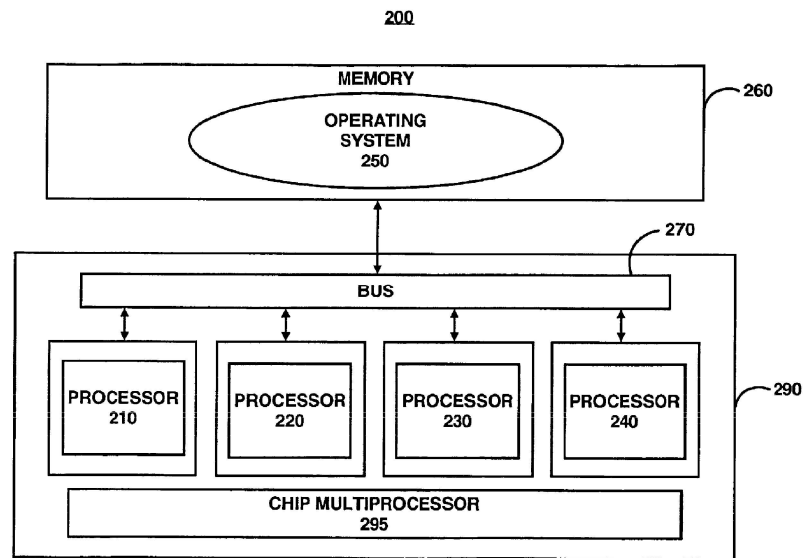


FIG. 2
Prior Art

EX1001, FIG. 2.

As used in the '014 patent, the term “processor group may include one or more processors mounted on the die.” EX1001, 2:24-25. Therefore, a POSITA would understand that AAPA processors 210-240 in FIG. 2 comprise processor groups. EX1002, ¶235.

Accordingly, AAPA discloses “processor groups mounted on a single die.” EX1002, ¶236.

To the extent that AAPA does not explicitly disclose *a plurality* of processor groups mounted on a single die, Gulick teaches doing so. EX1002, ¶237.

For example, AAPA-Gulick discloses each processor in the pairs of processors (e.g., processor 240A/240B-240R/240S) are mounted on a single die.

See supra Section VII.B.1.b. These pairs of processors are groups. For example, Gulick discloses groups of processors as “one or more Pods or sub-pods” with each pod or sub-pod operating “under the control of a separate operating system.” EX1005, 13:21-24; *see also* EX1005, 11:45-60 (“each TLC 230 is connected to four processors” and “[e]ach TLC 230 and its respective four processors define a sub-Pod.”); 11:60-62 (Two sub-Pods “are connected via crossbar interconnect (e.g., crossbar interconnect 290A or 290B) to form a Pod”). EX1002, ¶238.

A POSITA would be motivated by the teachings of Gulick to modify the multiprocessing system of the AAPA such that the processors 210-240 of AAPA could be combined into groups (e.g., pods or sub-pods) as taught by Gulick to improve, for example, overall performance of the AAPA’s multiprocessor system by devoting multiple processors to each operating system instance. *See e.g.*, EX1005, 13:21-24; 11:45-62; EX1002, ¶239.

Further such modification of AAPA based on the teachings of Gulick involves a simple substitution of one known element for another to obtain predictable results. EX1002, ¶240.

Thus, AAPA-Gulick discloses this limitation. EX1002, ¶241.

c. Limitation 7.c

Claim limitation 7.c varies slightly from claim limitation 1.c in that it recites “groups” while claim limitation 1.c does not. *See supra* Section VII.B.1.c. AAPA-Gulick discloses claim limitation 7.c for at least the same reasons discussed above from claim limitation 1.c. *See supra* Section VII.B.1.c; EX1002 ¶242.

d. Limitation 7.d

Claim limitation 7.d varies slightly from claim limitation 1.d in that it recites “groups” while claim limitation 1.d does not. *See supra* Section VII.B.1.d. AAPA-Gulick system discloses limitation 7.d for at least the same reasons discussed above from claim limitation 1.d. *See supra* Sections VII.B.1.d; EX1002 ¶243.

5. Claim 11

Claim 11 varies slightly from claim 5 in that it recites “groups” while claim 5 does not. *See supra* Section VII.B.3. AAPA-Gulick discloses claim 11 for at least the same reasons discussed above from claim 5. *See supra* Section VII.B.3; EX1002, ¶244.

6. Claim 12

a. Limitation 12.a

To the extent that the preamble of claim 12 is limiting, AAPA-Gulick discloses the limitations of the preamble for at least the reasons set forth above for

claim limitation 1.a. *See supra* Section VII.B.1.a; *see infra* Section VII.B.6.b-d; EX1002, ¶245.

b. Limitation 12.b

AAPA-Gulick discloses and/or suggests this limitation for at least the same reasons discussed above for claim limitations 1.b-1.d, and for the additional reasons provided below. *See supra* Sections VII.B.1.b-VII.B.1.d; EX1002, ¶246.

(1) Operating system means

AAPA-Gulick discloses and/or suggests “operating system means,” as claimed. EX1002, ¶247; *see also supra* Section VI.E (construction of “operating system means” as a conventional operating system, such as WINDOWS NT, UNIX, and the like, or equivalents thereof).

AAPA discloses computing system 200 that includes an “operating system 250 stored in memory 260.” EX1001, 1:39-40. AAPA describes computing system 200 and its components as a “second conventional multiprocessing scheme.” EX1001, 1:34. A POSITA would understand that, at the time of invention, “operating system 250” of the AAPA would be inclusive of “a conventional operating system, such as WINDOWS NT, UNIX, and the like, or equivalents thereof.” EX1002, ¶248.

Thus, AAPA-Gulick teaches “operating system means.” EX1002, ¶249.

(2) Processor means

AAPA-Gulick discloses and/or suggests “a processor means” as claimed. EX1002, ¶250; *see supra* Section VI.D (construction of “processor means”).

AAPA-Gulick discloses the agreed-upon function. The agreed-upon function for “processor means” is “executing a plurality of operating system means.” *See supra* Section VI.D. AAPA discloses that “processors 210-240 are connected to a single operating system 240 stored in memory 260.” EX1001, 1:38-40. As a POSITA understands, processors 210-240 execute operating system 240 stored in memory 260. EX1002, ¶251.

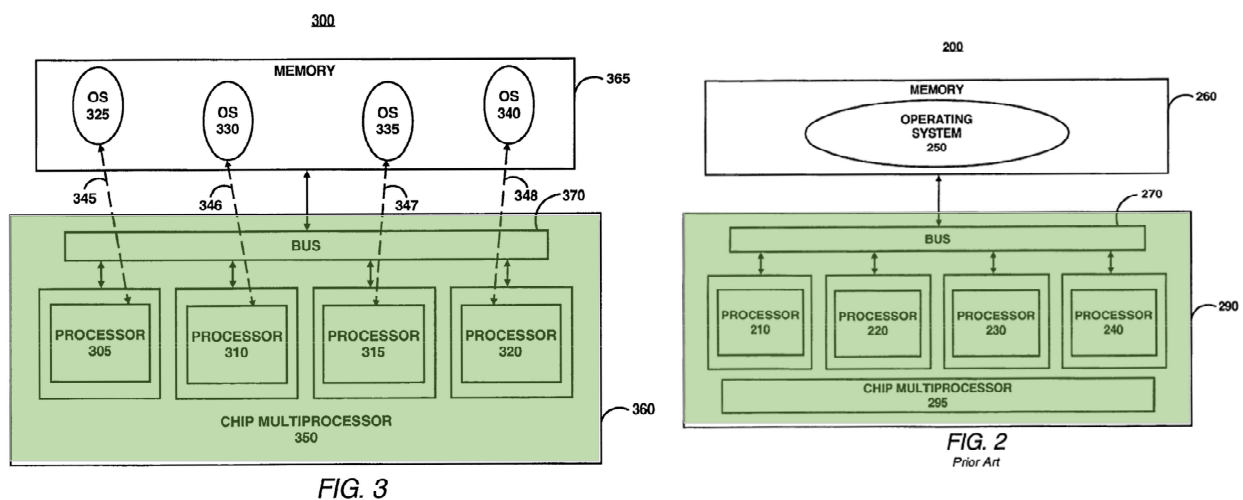
Although AAPA does not explicitly state that processors 210-240 execute a *plurality* of operating system means, a POSITA would find it obvious to modify the AAPA to do so based on the teachings of Gulick, as described above. *See supra* Section VII.B.1.c; EX1002, ¶252.

Further, to the extent the Board does not adopt the agreed upon construction, AAPA-Gulick also teaches the function of “simultaneously execute two or more operating system means of said plurality of operating system means” under Petitioner’s proposed alternative construction for the reasons stated above. Thus, AAPA-Gulick discloses this function as well. The structure corresponding to this alternative function is the same as the agreed upon construction and is met for the reasons stated below for that construction. EX1002, ¶253.

Thus, AAPA-Gulick discloses the agreed-upon function for “processor means.” EX1002, ¶254.

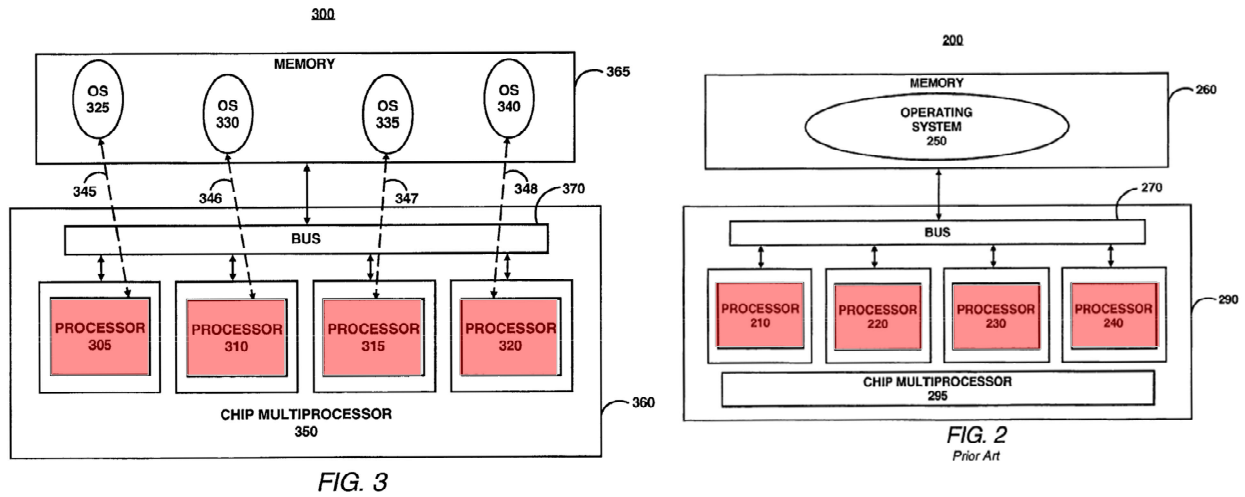
AAPA-Gulick also discloses the corresponding structure for “processor means.” As indicated above, the agreed-upon structure for “processor means” is “chip multiprocessor 350 having multiple processors 305-320 mounted on a single die 360 as shown in Figure 3 and associated descriptions in the specification; or chip multiprocessor 450 having multiple processors 405-420 mounted on a single die 460 shown in Figure 4 and associated descriptions in the specification; and equivalents thereof.” *See supra* Section VI.D; EX1002, ¶255.

As shown below, the '014 Patent discloses computing system 300 having chip multiprocessor 350 (left, green). Similarly, AAPA discloses computing system 200 having chip multiprocessor 295 (right, green). EX1002, ¶256.



The '014 Patent discloses that chip multiprocessor 350 includes four

processors 305-320 (left, red). Similarly, AAPA discloses that computer system 200 includes four processor 210-240 (right, red). EX1002, ¶257.



Thus, AAPA-Gulick system discloses the agreed upon structure of chip multiprocessor 350. EX1002, ¶258.

Further, as shown below, the '014 Patent discloses chip multiprocessor 450 (left, green). Similarly, AAPA discloses a chip multiprocessor (right, green). EX1002, ¶259.

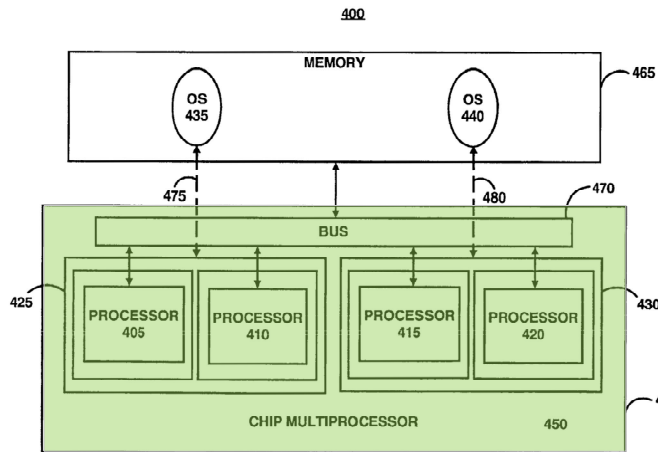


FIG. 4

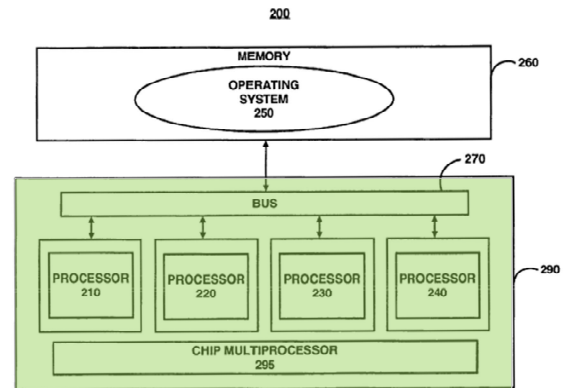


FIG. 2
Prior Art

The '014 Patent discloses that chip multiprocessor 450 includes four processors 405-420 (left, red). Similarly, AAPA discloses that computer system 200 includes four processor 210-240 (right, red). EX1002, ¶260.

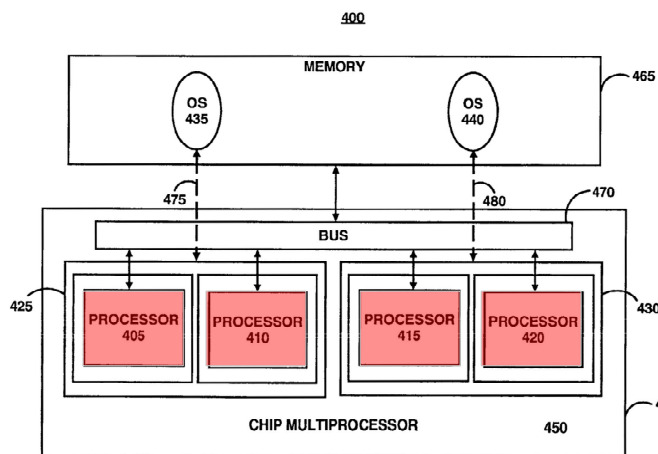


FIG. 4

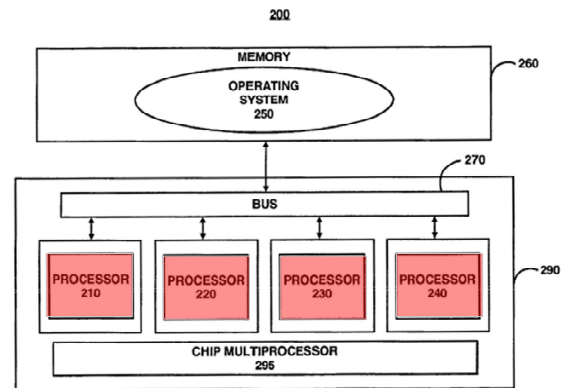


FIG. 2
Prior Art

Further, as indicated in section VII.B.4.b, it would be obvious to modify AAPA's teachings with Gulick to include groups of processors, similar to chip multiprocessor 450. See *supra* VII.B.4.b; EX1002, ¶261.

Thus, AAPA-Gulick discloses the corresponding structure of chip multiprocessor 450. EX1002, ¶262.

Therefore, to the extent “processor means” is construed under the agreed-upon construction, AAPA-Gulick teaches this limitation. EX1002 ¶263.

Additionally, to the extent that “processor means” is not a means plus function limitation, “processor means” should be construed according to its plain meaning, which has previously been discussed. *See supra* Section VII.B.6.b(2); EX1002, ¶264.

c. Limitation 12.c

AAPA-Gulick discloses and/or suggests limitation 12.c for at least the same reasons discussed above from claim limitation 1.d. *See supra* Section VII.B.1.d; EX1002, ¶265.

d. Limitation 12.d

AAPA-Gulick discloses and/or suggests limitation 12.d for at least the same reasons discussed above for claim limitations 1.c-1.d and for the additional reasons explained below. *See supra* Sections VII.B.1.c-VII.B.1.d; EX1002, ¶266.

AAPA-Gulick teaches the identified function of “memory means.” EX1002, ¶267. The identified function of the “memory means” is “storing said plurality of operating system means.” *See supra* Section VI.F. AAPA discloses this function. For example, the combined AAPA-Gulick system discloses that the memory

means is configured for “storing said plurality of operating systems.” *See supra* Sections VII.B.1.c-VII.B.1.d; EX1002, ¶267.

Thus, AAPA-Gulick discloses the identified function of “memory means.” EX1002, ¶268.

AAPA-Gulick also discloses the identified structure of “memory means.” The identified structure of “memory means” is “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” *See supra* Section VI.F. AAPA discloses computing system 200 that includes a “memory 260.” EX1001, 1:39-40. AAPA describes computing system 200 and its components as a “second conventional multiprocessing scheme.” EX1001, 1:34. A POSITA would understand that, at the time of invention, “memory 260” of the AAPA would be inclusive of “SRAM and/or DRAM on the same chip as one or more processors; SRAM and/or DRAM on separate chips connected to one or more processors; magnetic media, such as tape or disk; optical media, such as CD-ROM; and the like.” EX1002, ¶269.

Thus, AAPA-Gulick discloses the corresponding structure of “memory means.” EX1002, ¶270.

Therefore, AAPA-Gulick discloses this limitation. EX1002, ¶271.

7. Claim 13

Claim 13 varies slightly from claim 3 in that it recites a “processor means” and “memory means” while claim 3 does not. *See supra* Section VII.B.3. AAPA-Gulick system discloses a “processor means” (*see supra* Section VII.B.6.b) and “memory means” (*see supra* Section VII.B.6.d). EX1002, ¶272.

Accordingly, AAPA-Gulick discloses claim 13 for at least the same reasons discussed above from claim 3. *See supra* Section VII.B.2; EX1002, ¶273.

8. Claim 15

Claim 15 varies slightly from claim 5 in that it recites a “processor means” and “operating system means” while claim 5 does not. *See supra* Section VII.B.3. As discussed above, Gulick-AAPA system discloses a “processor means” (*see supra* Section VII.B.6.b(2)) and “operating system means” (*see supra* Section VII.B.6.b(1)). EX1002, ¶274.

Accordingly, AAPA-Gulick discloses claim 15 for at least the same reasons discussed above from claim 5. *See supra* Section VII.B.3; EX1002, ¶275.

VIII. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. General Plastic Denial is Inappropriate

The Board has previously instituted *inter partes* review of the ’014 patent; however, the Board never issued a final written decision because the parties to the instituted *inter partes* review filed a joint motion to terminate the proceedings. As

such, the '014 patent has not previously been substantively challenged in a post-grant proceeding. Additionally, the Petitioner was not a party to the prior *inter partes* review of the '014 patent. Accordingly, the *General Plastic* factors weigh against discretionary denial.

B. *Fintiv* Discretionary Denial is Inappropriate

The *Fintiv* factors (enumerated below) weigh against discretionary denial. IPR2020-00019, Paper 11, 5-6 (PTAB Mar. 20, 2020) (precedential). The “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation” dated June 21, 2022 (“Interim Guidance”) and recent board decisions applying these factors confirm discretionary denial is not warranted here.

1. *Fintiv* Factor 1: Institution Will Enable a Stay

The litigation is based in the Western District of Texas. Neither party has requested a stay. Thus, Factor one is neutral.

2. *Fintiv* Factor 2: District Court Schedule

Under, the Interim Guidance, Factor two favors institution. As set forth in the Interim Guidance, “when considering the proximity of the district court’s trial date to the date when the PTAB final written decision will be due, the PTAB will consider the median time from filing to disposition of the civil trial for the district in which the parallel litigation resides. Interim Guidance, 3. Here, the anticipated

trial date, as computed in accordance with the Interim Guidance, is November 2024 (28.2 months from July 15, 2022) [EX1019, 37]. The due date for a final written decision is also approximately November 2024.

3. *Fintiv* Factor 3: Parallel Proceeding Considerations

The District Court in the underlying litigation has not yet issued any substantive order related to the challenged patent. The District Court held the claim construction hearing and issued an order construing terms on April 6; none of the terms addressed in that claim construction order involve the '014 patent. Further, fact discovery is in its early stages and expert discovery has not yet begun.

Moreover, this petition was filed approximately two (2) months before the one-year statutory bar date. Overall, this factor weighs against discretionary denial.

4. *Fintiv* Factor 4: The Petition Raises Unique Issues

To eliminate any potential overlap of issues, Petitioner stipulates that if the Board institutes IPR, Petitioner will not assert invalidity of the challenged claims in the district court litigation using the grounds asserted in this petition. This stipulation weighs against discretionary denial. *See Sand Revolution II, LLC v. Cont'l Intermodal Group-Trucking LLC*, IPR2019-01393, Paper 24 at 11-12; *Apple Inc. v. Maxell, Ltd.*, IPR2020-00204, Paper 11 at 15-16 (PTAB June 19, 2020).

5. *Fintiv* Factor 5: The Petition Will Enable Cancellation of Claims that Might Be Reasserted

Apple’s petition is potentially helpful to future defendants. Apple’s status as both Petitioner and Defendant therefore is, at worst, a neutral factor. Institution would serve overall efficiency, enabling the Board to determine invalidity of claims that Patent Owner might otherwise later assert against others.

Further, members of the Board have noted that *Fintiv* addresses only the scenario in which the petitioner is unrelated to a defendant in a parallel proceeding, finding this should weigh against denying institution, but that *Fintiv* “says nothing about situations in which the petitioner is the same as, or is related to, the district court defendant.” *Cisco Sys., Inc. v. Ramot at Tel Aviv Univ. Ltd.*, IPR2020-00122, Paper 15, at *10-11 (PTAB May 15, 2020) (APJ Crumbley, dissenting) (noting that disfavoring a “defendant in the district court” is “contrary to the goal of providing district court litigants an alternative venue to resolve questions of patentability”).

6. *Fintiv* Factor 6: Other Considerations Support Institution

Petitioner submits that there is compelling evidence to institute *inter partes* review of the ’014 patent application. As set forth above, the Petition goes beyond merely providing sufficient evidence to meet the statutory institution threshold; instead, the Petition presents compelling evidence of unpatentability in light of the combinations of AAPA-Gulick and Gulick-AAPA, such that, if unrebutted in trial,

would lead to a conclusion that claims 1, 3, 5, 6, 11-13, and 15 are unpatentable by a preponderance of the evidence. Interim Guidance, 4-5.

In summary, the *Fintiv* factors altogether weigh against discretionary denial. Even if the Board were to determine that *Fintiv* factors on balance weigh in favor of denial, institution should nonetheless be granted because this Petition satisfies the compelling merits standards. Interim Guidance at 4; *Vizio, Inc. v. Maxell, Ltd.*, IPR2022-01458, Paper 8, at 62.

IX. CONCLUSION

For the foregoing reasons, Petitioner requests *inter partes* review of claims 1, 3, 5, 7, 11-13, and 15 of the '014 patent.

Dated: May 23, 2023

Respectfully Submitted,

/Joseph W. Wolfe/

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Table of Exhibits for U.S. Patent 6,874,014 Petition for *Inter Partes* Review

Exhibit	Description
1001	U.S. Patent No. 6,874,014
1002	Declaration of Dr. Martin G. Walker
1003	Curriculum Vitae of Dr. Martin G. Walker
1004	Prosecution History of U.S. Patent No. 6,874,014
1005	U.S. Patent No. 6,314,501 to Gulick et al. (“Gulick”)
1006	Updated Guidance on the Treatment of Statements of the Applicant in the Challenged Patent in Inter Partes Reviews Under § 311 (“AAPA Memo”) published by Katherine Vidal on June 9, 2022
1007	Joch, “HOW-TO Chip Multiprocessing,” Computerworld, November 27, 2000
1008	Olukotun et al., “The Case for a Single-Chip Multiprocessor,” ACM SIGPLAN Notices, Vol. 31, Issue 9, Sept. 1996
1009	U.S. Patent No. 6,550,020 to Floyd et al. (“Floyd”)
1010	Barroso et al., “Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing”, Proc. 27th ACM Int’l Symp. Computer Architecture, 2000
1011	U.S. Patent No. 6,772,241 to George et al.
1012	U.S. Patent No. 6,526,462 to Elabd
1013	Hammond et al., “A Single-Chip Multiprocessor,” Computer, vol. 30, no. 9, pp. 79-85, Sept. 1997
1014	U.S. Patent No. 6,178,503 to Madden et al.

1015	U.S. Patent No. 6,085,247 to Parsons, Jr. et al.
1016	U.S. Patent No. 6,247,109 to Kleinsorge et al.
1017	U.S. Patent No. 6,397,242 to Devine et al.
1018	<i>Sonrai Memory Ltd. v. Apple Inc.</i> , Case No. 6:22-cv-00787-ADA, Dkt. 22, Agreed Scheduling Order.
1019	U.S. District Courts—Combined Civil and Criminal Federal Court Management Statistics (March 31, 2023)

CERTIFICATION UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR §42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,634 words, which is less than the 14,000 allowed under 37 CFR §42.24(a)(i).

Dated: May 23, 2023

Respectfully Submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(b), the undersigned certifies that, on April 12, 2023, a true and correct copy of the foregoing materials were served on Patent Owner electronically, by agreement, by emailing a copy to the following attorneys for the Patent Owner:

- Petition for *Inter Partes* Review of U.S. Patent No. 6,874,014 under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibit List
- Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 6,874,014 (EX1001 – EX1019)
- Power of Attorney
- Word Count Certification under 37 C.F.R. § 42.24(d)
- Appendix of claim listing

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APPENDIX

1. A multiprocessing system comprising:
multiple processors mounted on a single die; and
multiple operating systems residing in a memory connected to said multiple processors,
wherein each of said multiple processors executes an operating system of said multiple operating systems, and two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems.
2. The system of claim 1, wherein at least one of said processors is operable to execute two or more of said multiple operating systems simultaneously.
3. The system of claim 1, wherein said multiple processors are connected to said memory via a bus to execute said multiple operating systems.
4. The system of claim 1, wherein said multiple processors are directly connected to said memory to execute said multiple operating systems.
5. The system of claim 1, wherein each of said processors executes a distinct operating system of said multiple operating systems.
6. The system of claim 1, further comprising multiple processor groups, wherein each processor group includes at least two of said multiple processors executing one of said multiple operating systems.

7. A multiprocessing system comprising:
a plurality of processor groups mounted on a single die; and
multiple operating systems residing in a memory connected to said groups,
wherein each of said groups executes an operating system of said multiple
operating systems, and two or more of said plurality of processor groups are
capable of simultaneously executing two or more operating systems of said
multiple operating systems.

8. The system of claim 7, wherein each of said groups includes multiple
processors.

9. The system of claim 8, wherein said multiple processors in each of said
groups are connected to said memory via a bus to execute said multiple operating
systems.

10. The system of claim 8, wherein said multiple processors in each of said
groups are directly connected to said memory to execute said multiple operating
systems.

11. The system of claim 7, wherein each of said groups executes a distinct
operating system of said multiple operating systems.

12. A multiprocessing apparatus comprising:
processor means for executing a plurality of operating system means,
wherein said processor means includes a plurality of processors mounted on a

single die, and wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means; and

memory means for storing said plurality of operating system means.

13. The apparatus of claim 12, wherein said processor means is connected to said memory means via a bus to execute said multiple operating systems.

14. The apparatus of claim 12, wherein said processor means is directly connected to said memory means to execute said multiple operating systems.

15. The apparatus of claim 12, wherein each of said processors of said processor means is operable to execute a distinct one of said plurality of operating system means.

16. The apparatus of claim 12, wherein said processor means includes a plurality of processor group means, wherein each processor group means includes at least two of said plurality of processors.

17. The apparatus of claim 16, wherein said plurality of processor group means is operable to execute one or more of said plurality of operating system means.

18. The apparatus of claim 16, wherein each of said plurality of processor group means is operable to execute a distinct one of said plurality of operating system means.

19. The apparatus of claim 12, wherein at least one of said plurality of processors is operable to simultaneously execute two or more of said plurality of operating system means.