

**UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

SONRAI MEMORY LIMITED,

Plaintiff,

v.

APPLE INC.,

Defendant.

Civil Action No. 6:22-cv-00787-ADA

JURY TRIAL DEMANDED

FIRST SUPPLEMENTAL INVALIDITY CONTENTIONS

Defendant Apple Inc. hereby provides its First Supplemental Invalidity Contentions.

INVALIDITY CONTENTIONS

Defendant Apple Inc. (“Defendant” or “Apple”) hereby provides its First Supplemental Invalidity Contentions.

I. CLAIM CHARTS - ANTICIPATION

A. ’241 Patent

Attached hereto are the following charts setting forth where in the prior art references each element of the claims 1-3, 6, 9-11, and 24 (“the invalid claims”) of U.S. Patent No. 6,724,241 (“’241 Patent”) are found with regard to at least one asserted claim, at least under Sonrai’s apparent interpretation of the invalid claims as construed by the Court and as evidenced by Sonrai’s preliminary infringement contentions. Nothing in these invalidity contentions should be taken as an admission that Defendant agrees with Sonrai’s interpretation of the claims or Sonrai’s infringement contentions.

Exhibit	Description	Date	Bates Numbers
A-1	U.S. Patent No. 6,091,613 (“Yang”)	Filed 4/20/99 Issued 7/18/00	APL-SON787-PA-00002293 - APL-SON787-PA-00002300
A-2	U.S. Patent No. 6,356,488 (“Kang”)	Filed 11/27/00 Issued 3/12/02	APL-SON787-PA-00002589 - APL-SON787-PA-00002599
A-3	U.S. Patent No. 6,937,517 (“Pekny”)	Filed 7/18/02 Issued 8/30/05	APL-SON787-PA-00003680 - APL-SON787-PA-00003691
A-4	Japan Patent Application Publication S61-24094 (“Ujiie”)	Published 2/1/86	APL-SON787-PA-00000665 - APL-SON787-PA-00000686
A-5	U.S. Patent No. 6,404,274 (“Hosono”)	Filed 4/9/99 Issued 6/11/02	APL-SON787-PA-00002738 - APL-SON787-PA-00002754
A-6	U.S. Patent No. 6,643,151 (“Nebragic”)	Filed 10/9/01 Issued 11/4/03	APL-SON787-PA-00003161 - APL-SON787-PA-00003195

A-7	U.S. Patent No. 5,699,312 (“Wong”)	Filed 4/18/96 Issued 12/16/97	APL-SON787-PA-00002075 - APL-SON787-PA-00002080
A-8	Toshiba TC58256FT Product (“TC58256FT”)	Date of first US sale: no later than 10/25/01	APL-SON787-PA-00000001 - APL-SON787-PA-00000084
A-9	Toshiba TC58256AFT Product (“TC58256AFT”)	Date of first US sale: no later than 10/25/01	APL-SON787-PA-00001119 - APL-SON787-PA-00001154
A-10	U.S. Patent No. 6,597,235 (“Choi ’235”)	Filed 1/9/02 Published 8/1/02	APL-SON787-PA-00003973 - APL-SON787-PA-00003979
A-11	U.S. Patent No. 6,535,051 (“Kim”)	Filed 5/21/01 Published 12/20/01	APL-SON787-PA-00003961 - APL-SON787-PA-00003972
A-12	Samsung K9F5608UOM-YCBO 256M NAND Flash product	Date of first US sale: no later than June 2001	APL-SON787-PA-00003980 - APL-SON787-PA-00004005
A-13	U.S. Patent No. 5,986,947 (“Choi ’947”)	Filed: 4/9/98 Published: 11/16/99	APL-SON787-PA-00003946 - APL-SON787-PA-00003960
A-14	U.S. Patent No. 5,673,223 (“Park”)	Filed: 6/10/96 Published: 9/30/97	APL-SON787-PA-00003939 - APL-SON787-PA-00003945
A-15	U.S. Patent No. 6,069,518 (“Nakai”)	Filed 12/1/1994 Issued 5/30/2000	APL-SON787-PA-00005146 - APL-SON787-PA-00005164
A-16	U.S. Patent No. 4,769,784 (“Doluca”)	Filed 8/19/1986 Issued 9/6/1988	APL-SON787-PA-00001570 - APL-SON787-PA-00001579
A-17	U.S. Patent No. 6,373,325 (“Kuriyama”)	Filed 3/13/2000 Issued 4/16/2002	APL-SON787-PA-00002671 - APL-SON787-PA-00002690
A-18	U.S. Patent No. 6,724,241 (“AAPA-241”)	Filed: 1/27/03 Issued: 4/20/04	SONRAI-APPLE-WDTX_00003734 - SONRAI-APPLE-WDTX_00003747

Much of the art identified in the attached Exhibits reflects common knowledge and the state of the art prior to the filing date of the ’241 Patent. The references discussed in the Exhibits herein may be relied upon to show the state of the art in the relevant time frame. This prior art

identification is only exemplary and is not in any way intended to limit the scope of what one of ordinary skill in the art would have understood at the relevant time period of the alleged inventions or the breadth of the state of the art to which the alleged inventions of the '241 Patent relate. Defendant reserves the right to rely upon additional prior art, information, testimony, and/or knowledge to demonstrate what one of ordinary skill in the art would have understood prior to the date of the alleged invention of the invalid claims of the '241 Patent.

Defendant reserves the right to supplement these contentions with prior art or additional information not currently known to Defendant, or as otherwise permitted by Local Rules or the Court. For example, Defendant may modify or supplement these contentions in the event that additional invalidity grounds or information becomes available, whether in response to any allowed amendment by Sonrai of its infringement contentions, or through discovery of additional prior art or material information, including third-party prior art systems or information. Defendant also incorporates herein by reference the IPR Petition and exhibits in Case IPR2021-01561, the institution decision by the Patent Trial and Appeals Board ("PTAB"), and subsequent filings in that proceeding. Defendant also incorporates herein by reference the IPR Petition and exhibits in Case IPR2023-00909 currently pending at the PTAB. The petition and accompanying exhibits set forth additional reasons claims 1-3, 6, 9-11 and 24 of the '241 Patent are invalid. Defendant further reserves the right to rely on additional references and expert testimony to explain the knowledge of a person of skill in the art ("POSITA") and how a POSITA would interpret the disclosures of the '241 Patent or the prior art references.

B. '014 Patent

Attached hereto are the following charts setting forth where in the prior art references each element of the claims 1, 3, 5, 7, 11, 12-13, and 15 ("the invalid claims") of U.S. Patent No.

6,874,014 (“’014 Patent”) are found with regard to at least one asserted claim, at least under Sonrai’s apparent interpretation of the invalid claims as evidenced by Sonrai’s preliminary infringement contentions. Nothing in these invalidity contentions should be taken as an admission that Defendant agrees with Sonrai’s interpretation of the claims or Sonrai’s infringement contentions.

Exhibit	Description	Date	Bates Numbers
B-1	U.S. Patent No. 6,542,926 (“Zalewski”)	Filed 6/10/98 Issued 4/1/03	APL-SON787-PA-00004178 - APL-SON787-PA-00004213
B-2	U.S. Patent No. 6,931,640 (“Asano”)	Filed 1/9/01 Issued 8/16/05	APL-SON787-PA-00004742 - APL-SON787-PA-00004765
B-3	U.S. Patent No. 6,957,435 (“Armstrong”)	Filed 4/19/01 Issued 10/18/05	APL-SON787-PA-00004036 - APL-SON787-PA-00004053
B-4	U.S. Patent No. 6,772,419 (“Sekiguchi”)	Filed 9/11/98 Issued 8/3/04	APL-SON787-PA-00004006 - APL-SON787-PA-00004035
B-5	U.S. Patent No. 6,839,849 (“Ugon”)	Filed 12/23/99 Issued 1/4/05	APL-SON787-PA-00004525 - APL-SON787-PA-00004537
B-6	U.S. Patent No. 7,073,044 (“Willis”)	Filed 3/30/01 Issued 7/4/06	APL-SON787-PA-00004831 - APL-SON787-PA-00004851
B-7	U.S. Patent No. 5,910,987 (“Ginter”)	Filed 12/4/96 Issued 6/8/99	APL-SON787-PA-00004214 - APL-SON787-PA-00004524
B-8	U.S. Patent No. 6,799,202 (“Hankinson”)	Filed 12/16/99 Issued 9/28/04	APL-SON787-PA-00004538 - APL-SON787-PA-00004584
B-9	U.S. Patent No. 6,385,727 (“Cassagnol”)	Filed 9/25/98 Issued 5/7/02	APL-SON787-PA-00005084 - APL-SON787-PA-00005111
B-10	U.S. Patent Pub. No. 2004/0210738 (“Kato”)	Filed 4/27/04 Published 10/21/04	APL-SON787-PA-00005310 - APL-SON787-PA-00005339

B-11	Kunle Olukotun et. al., <i>The Case for a Single-Chip Multiprocessor, Proceedings Seventh International Symp. Architectural Support for Programming Languages and Operating Systems</i> (ASPLOS VII), October 1996 (“Olukotun”)	October 1996	APL-SON787-PA-00000745 - APL-SON787-PA-00000754
B-12	Texas Instruments OMAP and/or documents descriptive thereof (“OMAP”)	Date of first US sale: no later than July 2000 Published: 2000-2001	APL-SON787-PA-00004970 - APL-SON787-PA-00004981; APL-SON787-PA-00005036 - APL-SON787-PA-00005043; APL-SON787-PA-00004947 - APL-SON787-PA-00004952; APL-SON787-PA-00005112 - APL-SON787-PA-00005114; APL-SON787-PA-00005115 - APL-SON787-PA-00005119; APL-SON787-PA-00005120 - APL-SON787-PA-00005122; APL-SON787-PA-00005123 - APL-SON787-PA-00005124; APL-SON787-PA-00005125 - APL-SON787-PA-00005127; APL-SON787-PA-00005183 - APL-SON787-PA-00005189 <i>See also</i> TI Production Documents listed in Exhibit B-12.
B-13	U.S. Patent No. 6,751,698 (“Deneroff”)	Filed: 9/29/99 Issued: 6/15/04	APL-SON787-PA-00004076 - APL-SON787-PA-00004177
B-14	U.S. Patent No. 5,144,692 (“Baker”)	Filed: 5/17/89 Issued: 9/1/92	APL-SON787-PA-00004585 - APL-SON787-PA-00004741
B-15	U.S. Patent Pub. No. 2002/0173344 (“Cupps”)	Filed: 3/16/01 Published 11/21/02	APL-SON787-PA-00004805 - APL-SON787-PA-00004830

B-16	Bilge Saglam and Vincent Mooney, <i>System-on-a-Chip Processor Synchronization Support in Hardware, IEEE Computer Society, Proceedings, Designation, Automation and Test in Europe</i> (IEEE March 13-16, 2001) ("Saglam")	Published: at least by March 16, 2001	APL-SON787-PA- 00004862 - APL- SON787-PA-00004868
B-17	U.S. Patent No. 6,314,501 ("Gulick")	Filed: 12/18/98 Issued: 11/6/01	APL-SON787-PA- 00004869 - APL- SON787-PA-00004946
B-18	U.S. Patent No. 6,542,991 ("Joy")	Filed: 5/11/99 Issued: 4/1/03	APL-SON787-PA- 00002959 - APL- SON787-PA-00002997
B-19	U.S. Patent No. 7,143,401 ("Babaian")	Filed: 2/20/01 Issued: 11/28/06	APL-SON787-PA- 00004054 - APL- SON787-PA-00004075
B-20	U.S. Patent No. 6,874,014 ("AAPA")	Filed: 5/29/01 Issued: 3/29/05	APL-SON787-PA- 00005218 - APL- SON787-PA-00005225
B-21	Texas Instruments'/Nokia MAD Systems	No later than Feb. 2001	TI-0008314-0008324, TI- 0008087-0008313, TI- 0007431-0007624, TI- 0007319-0007430, TI- 0007770-8041
B-22	U.S. Patent No. 7,111,177 ("Chauvel")	Filed: 10/5/00 Issued: 9/19/06	TI-0007170 - 0007183
B-23	U.S. Patent No. 7,076,551 ("Gary")	Filed: 3/30/01 Issued: 7/11/06	TI-0007154 - 0007169
B-24	U.S. Patent No. 6,711,700 ("Armstrong 700")	Filed: 4/23/01 Issued: 3/23/04	TI-0007215-0007222
B-25	U.S. Patent Pub. No. 2002/0029301 ("Toda")	Filed: 4/10/01 Pub: 3/7/02	TI-0007223 - 0007246
B-26	U.S. Patent No. 6,226,734 ("Kleinsorge")	Filed: 6/10/98 Issued: 5/1/01	TI-0007270 – 0007306
B-27	U.S. Patent No. 7,098,899 ("Ginosar")	Filed: 9/21/99 Issued: 8/29/06	TI-0007096 – 0007112
B-28	Japanese Patent No. JP H0793267 ("Miyamoto")	Pub. 9/22/93	TI-0007113-0007120 TI-0002747-0007269
B-29	U.S. Patent No. 7,509,391 ("Chauvel 391")	Filed: 11/23/99 Issued: 3/24/09	TI-0007184-0007196
B-30	U.S. Patent No. 6,029,000 ("Woolsey")	Filed: 12/22/97 Issued: 2/22/00	TI-0007138-0007153

Much of the art identified in the attached Exhibits reflects common knowledge and the state of the art prior to the filing date of the '014 Patent. The references discussed in the Exhibits herein may be relied upon to show the state of the art in the relevant time frame. This prior art identification is only exemplary and is not in any way intended to limit the scope of what one of ordinary skill in the art would have understood at the relevant time period of the alleged inventions or the breadth of the state of the art to which the alleged inventions of the '014 Patent relate. Defendant reserves the right to rely upon additional prior art, information, testimony, and/or knowledge to demonstrate what one of ordinary skill in the art would have understood prior to the date of the alleged invention of the invalid claims of the '014 Patent.

Defendant reserves the right to supplement these contentions with prior art or additional information not currently known to Defendant, or as otherwise permitted by Local Rules or the Court. For example, Defendant may modify or supplement these contentions in the event that additional invalidity grounds or information becomes available, whether in response to any allowed amendment by Sonrai of its infringement contentions, or through discovery of additional prior art or material information, including third-party prior art systems or information. With respect to the '014 Patent, on information and belief, the additional systems include at least the Texas Instruments' OMAP systems (B-12), the Texas Instruments'/Nokia MAD Systems (B21), Power4 by IBM¹; the Stanford Hydra CMP²; and the HP MPOC³. Defendant also incorporates herein by reference the IPR Petitions and exhibits in Case IPR2021-01454, Case IPR2022-00756, Case IPR2022-00801, Case IPR2023-00819, and Case IPR2023-00975, the institution decisions

¹ e.g., <https://www.ibm.com/ibm/history/ibm100/us/en/icons/power4/>

² e.g., <http://bwrcs.eecs.berkeley.edu/Courses/CS252/Notes/cs252.lecture.20.pdf>

³ e.g., <https://www.hpl.hp.com/techreports/2002/HPL-2002-186.html>

by the Patent Trial and Appeals Board (“PTAB”), and filings in those proceedings. Defendant further reserves the right to rely on additional references and expert testimony to explain the knowledge of a person of skill in the art (“POSITA”) and how a POSITA would interpret the disclosures of the ’014 Patent or the prior art references.

II. CLAIM CHARTS – OBVIOUSNESS

A. ’241 Patent

If the Judge or Jury finds that a particular prior art reference described in the charts referred to in Section I, above, does not teach or disclose a particular claim limitation, that limitation and the claims in which it appears still are rendered obvious for the reasons stated for that limitation in Exhibit C-1, which explains where each particular limitation is found in other prior art references and/or in the knowledge of a POSITA, at least under Sonrai’s apparent interpretation of the invalid claims as evidenced by Sonrai’s preliminary infringement contentions. Nothing in these invalidity contentions should be taken as an admission that Defendant agrees with Sonrai’s interpretation of the claims or Sonrai’s infringement contentions. Moreover, Ex. C-1 provides some exemplary motivations to modify and/or combine the primary prior art reference with the other listed prior art.

Much of the art identified in the attached exhibits A-1 through A-18 and C-1 reflects common knowledge and the state of the relevant art at the time of the earliest filing date of the ’241 patent. Indeed, many of the exemplary citations in the exhibits identify relevant disclosures characterizing what was considered the background art at the time the prior art reference was authored, or alternatively are citations in undergraduate level textbooks and thus constitute contemporaneous evidence as what was wide-spread and well-known by POSITA even at the time the reference was written (Known in the Art, or “KITA”). The state of the art at the relevant

time expressly taught and suggested combining various techniques for augmenting various well-known charge pump circuits to regulate the output voltage to provide a more stable voltage supply as appropriate for a given application. *See* Exhibits A-1 through A-18 and C-1. As a result, one skilled in the art would have known to combine or modify references that described known systems and methods which one of skill in the art would have recognized as offering improvements to solutions at that time. Each of the prior art references identified herein and in Exhibits A-1 through A-18 and C-1 described systems and methods that were known to offer such improvements, and, accordingly, one of skill in the art would have been motivated to combine or modify the references as described herein.

Reasons exist to combine one or more of the references included in these invalidity contentions with each other. Generally, reasons to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. For example, many of these references identify and address the same technical issues and suggest very similar solutions to those issues in the field of microprocessor systems. *See* Exhibits A-1 through A-18 and C-1. Moreover, several of these references have common inventions, cross-reference and/or discuss one another, thereby providing an explicit motivation to combine such references and further illustrating the close technical relationship among this group of references.

Applicant admitted prior art and/or textbook disclosures demonstrate much of the claimed subject matter were well-known in the prior art and part of the basic knowledge base of POSITA at the relevant time. Indeed, the '241 Patent itself characterizes the object of the purported invention is to maintain the same basic structure of charge pump and regulator known in the prior art, with the improvement being to provide a minimum-ripple pump output voltage.

However, as construed by the Court, the language in the preamble of claim 1 directed to “generating a charge pump voltage having minimal voltage ripples” is not limiting. Therefore, the claims (as construed broadly without any requirement to minimize voltage ripples) encompass even prior art charge pump circuits that the ’241 Patent admits share the same structure as what is claimed in the invalid claims. At a minimum, each of the prior art references identified in Exhibits A-1 through A-18 and C-1 alone, or in combination with one or more additional prior art references cited therein, render the invalid claims obvious, because any limitation that is not expressly or inherently disclosed by any of the prior art references recite well-known circuit elements that a POSITA would understand is suitable for serving the corresponding intended purpose as disclosed in that prior art. As demonstrated in Exhibits A-1 through A-18 and C-1, many of these elements are well-known textbook circuit elements, and a POSITA would have known to use such known elements to obtain the same predictable results.

For example, regulator circuits were well known to POSITA in the art for regulating the output of a system in general, as was the specific use a regulator circuit to regulate the output of a charge pump circuit. To the extent any prior art reference fails to expressly disclose a regulator circuit for regulating the disclosed charge pump circuit, it would have been obvious to modify the disclosed charge pump circuit with any one of numerous known regulator circuits to improve upon the disclosed circuit to provide a more stable and predictable output voltage. Likewise, a POSITA would have been aware of various known design trade-offs for the different regulator circuits. Accordingly, depending on the design objective, a POSITA would have been motivated to modify the charge pump circuit with a suitable regulator circuit. As another example, a POSITA would have appreciated that in a typical integrated circuit device (“IC chip”), the IC chip is provided with only a few supply voltages (often, only one). However, in many IC chips,

the different circuitries that are integrated into the IC chip may require different operating voltages, with many that exceed the voltage level of the IC chip supply voltage. In some applications, the same circuit elements may require a plurality of supply voltage levels. Accordingly, for such applications, it was already well known and would have been obvious to use a charge pump circuit that is configured to allow outputting a plurality of output pump voltage levels, with the capability to selectively transition between the different desired output pump voltage levels. For such circuits, it would also have been obvious to adapt these output voltage regulation techniques suitable for charge pump circuits that only output a single voltage level to charge pump circuits that can output multiple output pump voltage levels.

As another example, it would be well known to POSITA that many of these well-known circuits can be implemented by using various interchangeable circuit elements, and furthermore, that using any of these circuit elements can achieve the same intended design objective of the circuit. Thus, a given choice for a particular circuit element may simply reflect different trade-offs. For example, a switch is a well-known circuit element for selectively coupling or decoupling elements from a circuit. Switches can be implemented in numerous forms, as would be well known by POSITA. For switches integrated into IC chips, these can be in the form of integrated transistor switches, including bipolar junction transistors (“BJT”) or field effect transistors (“FET”) including MOSFETs (both NMOS type and PMOS type), and any of these can be used to selectively couple circuit elements to one another in a circuit. A POSITA would have known how to adapt the circuits to use these exemplary elements as a switch to achieve the intended objective of the circuit. Similarly, impedance networks can be used in a circuit as a voltage divider network, and the impedance can be implemented using for example, capacitor elements, or resistor elements. The use of these well-known circuit elements for such purposes is

common knowledge for those of ordinary skill in the art. Accordingly, each of the invalid claims is rendered obvious at least by any one of the primary references in combination with the knowledge of POSITA and/or applicant admitted prior art (collectively, “KITA”). Other exemplary combinations of prior art reference that render the invalid claims obvious are disclosed in IPR2021-01561 and IPR2023-00909 and incorporated herein. As further exemplary combinations, each of the invalid claims is also rendered obvious at least by Yang, KITA and Ujiie; Yang, KITA, Ujiie and Hosono; Yang, KITA, Ujiie and Nakai; Yang, KITA, Doluca and Nakai; Yang, KITA, Usami and Nakai; Ujiie, KITA and Doluca; Ujiie, KITA, and Kuriyama; Ujiie, KITA, and Hosono; Ujiie, KITA, and Nakai; Ujiie, KITA, and Buti; Ujiie, KITA, Le; Hosono, KITA and Buti; Hosono, KITA and Le; Hosono, KITA and Kuriyama; Hosono, KITA, and Nakai; Nakai, KITA and Buti; Kakai, KITA and Le; Nakai, KITA, and Usami. These obviousness combinations are merely exemplary and not exhaustive. Indeed, as expressly set forth in these contentions and for the exemplary reasons articulated herein and in the accompanying exhibits, to the extent any limitation is not expressly or inherently disclosed by any given primary reference, it would have been obvious to combine the teachings of that primary reference with the disclosure in any one or more of the other references identified in the corresponding limitation in Exhibit C-1, thereby rendering the claim as a whole obvious, for the reasons set forth herein.

Defendant also incorporates herein by reference the IPR Petition and exhibits in Case IPR2021-01561 and Case IPR2023-00909. Defendant further reserves the right to rely on additional references and expert testimony to explain the knowledge of a POSITA and how a POSITA would interpret the disclosures of the '241 Patent or the prior art references. Sonrai has not disclosed any nexus between its purported evidence of alleged secondary considerations for

non-obviousness and the claims of the '241 patent. To the extent Sonrai is later able to identify and rely on any such alleged secondary considerations, including attempting to cite to purported evidence in support thereof, Defendant reserves the right to respond

B. '014 Patent

If the Judge or Jury finds that a particular prior art reference described in the charts referred to in Section I, above, does not teach or disclose a particular claim limitation, that limitation and the claims in which it appears still are rendered obvious for the reasons stated for that limitation in Exhibit C-2, which explains where each particular limitation is found in other prior art references and/or in the knowledge of a POSITA, at least under Sonrai's apparent interpretation of the invalid claims as evidenced by Sonrai's preliminary infringement contentions. Nothing in these invalidity contentions should be taken as an admission that Defendant agrees with Sonrai's interpretation of the claims or Sonrai's infringement contentions. Moreover, Ex. C-2 provides exemplary motivations to modify and/or combine the primary prior art reference with the other listed prior art.

Much of the art identified in the attached exhibits B-1 through B-30 and C-2 reflects common knowledge and the state of the relevant art at the time of the earliest filing date of the '014 Patent. The state of the art at the relevant time expressly taught and suggested combining various techniques for creating and operating multiprocessor systems having multiple operating systems. *See* Exhibits B-1 through B-30 and C-2. As a result, one skilled in the art would have known to combine or modify references that described known systems and methods which one of skill in the art would have recognized as offering improvements to solutions at that time. Each of the prior art references identified herein and in Exhibits B-1 through B-30 and C-2 described systems and methods that were known to offer such improvements, and, accordingly,

one of skill in the art would have been motivated to combine or modify the references as described herein.

Reasons exist to combine one or more of the references included in these invalidity contentions with each other. Generally, reasons to combine any of these references with others exists within the references themselves, as well as within the knowledge of those of ordinary skill in the art at the relevant time. For example, many of these references identify and address the same technical issues and suggest very similar solutions to those issues in the field of microprocessor systems. *See* Exhibits B-1 through B-30 and C-2. Moreover, several of these references have common inventions, cross-reference and/or discuss one another, thereby providing an explicit motivation to combine such references and further illustrating the close technical relationship among this group of references.

In the '014 Patent, the Applicant also makes admissions as to what was known at the relevant time. For example, the '014 Patent admits, in a “conventional multiprocessing scheme,” it was known that “chip multiprocessor [may] include[] multiple processors... on a single die.” '014 Patent, 1:34-37, *see also* Fig. 2. Such a prior art system was known to have an operating system stored in a memory as well as a bus connecting the processors and the memory. Likewise, the '014 Patent explains that prior art teachings “support[] multiple processors executing multiple operating systems,” using virtual processors. *Id.* at 1:60-65.

One would be motivated to combine the identified prior art because the references address the same or similar issues. For example, Gulick discloses a multi-processor computer system that includes “one or more processor modules and a main memory having one or more memory storage units... that allows a plurality of operating systems to concurrently execute in different partitions within the computer system and allows the different partitions to

communicate with one another through shared memory.” Gulick, 8:47-53. Gary explains that “[d]ata processing systems (including single-chip systems) which utilize one or more host processors (for example microprocessors) and one or more co-processors (for example further microprocessors or digital signal processors) under control of the host processor(s) are well known in the art.” Gary, 1:15–20. Gary also dealt with the specific task of managing resources between various processors and operating systems. *See generally, e.g.*, Gary at Abstract, 2:20-46. Likewise, Chauvel focused on “controlling the execution of tasks in a processor comprising a plurality of processing modules” which improved prior art multiprocessor designs that used “microprocessor units (MPUs), co-processors and digital signal processors (DSPs).” Chauvel, 1:29-32, 2:10-16, 3:1-26 (describing multiprocessor system with multiple operating systems and a shared memory). Kleinsorge too discloses a “single physical machine with multiple physical processors and resources is subdivided by software into multiple partitions, each with the ability to run a distinct copy, or instance, of an operating system.” Kleinsorge at Abstract. Each of these multi-processing systems could be implemented by fabricating each of the “multiple processors... on a single die,” in a “conventional multiprocessing scheme” as the ’014 Patent admits. ’014 Patent, 1:34-37, Fig. 2. Woolsey recognizes similar problems involving multiprocessor systems with multiple operating systems—explaining that “a need exists for a data processing architecture which can be upgraded and optimizes use of multiple processors and coprocessors.” Woolsey, 1:42-44; *see also* 45-67. Chauvel 391 likewise recognizes that “a multi-processor architecture with heterogeneous processor including an MPU (micro-processor unit), one or several DSPs (digital signal processors) as well as a co-processor or hardware accelerator and DMA provides significant advantages” and that “DSP platforms will benefit from a RTOS (real time operating system) to schedule multiple applications.” Chauvel 391, 1:20-58. Chauvel

391 is directed to innovations related to memory management units to control bus access to shared memory. *Id.* at Abstract, Fig. 1a.

Armstrong 700 teaches further benefits to such multiprocessor/multi-OS systems, describing “[a]n apparatus and method for monitoring the state of a computer system running multiple operating systems shared by a partition manager” Armstrong 700 at Abstract. Toda describes means for “partition[ing] hardware resources that are necessary to the operation of a second operating system” in a multiprocessing system. Toda at Abstract. As such, persons of ordinary skill in the art would have recognized that there were no significant impediments (technological or otherwise) to combining elements and features from different references and would have been motivated to do so. *See also, e.g.,* Chauvel at 1:29-42; 1:60-2:6; Chauvel 391 at 1:20-58; 1:62-2:10; Woolsey at 1:23-45, 1:57-67; Gary at 1:15-54; Toda at [0004]-[0017]; Miyamoto at [0002]-[0003] and [0006]-[0009]; Ginosar at 1:11-2:27; Armstrong 700 at 1:16-2:4. Armstrong at 1:54-2:6; Ugon at 4:23-29, 4:47-49, 10:56-59, 6:22-43, Figures 3, 7; Hankinson at 10:2-25; Kato at 72, 24, 61-62, 89, 96-97, 102-103, 110-116, 123, 128, 132-135, 139-140, Figures 1- 3, 7-11; Olukotun at 2, 4, Figure 3; Shalan at 180, 182; Deneroff at 2:52-57; Joy at 2:17-57, 7:9-27, 7:31-39, 7:49-57, 14:64-67, Fig. 2C; Babaian at 3:56-62, 4:8-36, 7:34-39, 13:65-14:3. Indeed, the prior art references evidence that multiple companies in this time frame were working on technology to improve devices and systems with multiprocessors and multi-operating system, such as Texas Instruments. As such, a POSITA would have been motivated to combine the ideas and technologies disclosed in the prior art.

Developments in the art would also provide motivation to combine prior art references in ways that would take advantage of those developments. For example, in the late 1990s through early 2000s, many companies were creating multiprocessor systems that used multiple operating

systems. Texas Instruments made and sold several multiprocessor systems at the time for use in mobile devices where multiple processors and operating systems were needed to efficiently run the tasks on such devices. *See, e.g.*, Exhibits B-12, B-21. Such devices include MAD1, MAD2x, MAD3, MAD4, UPPx, PDCharm, Breaker, Martha, Heather, Hele, Perseus, OMAP710, OMAP1510DC, OMAP1509, OMAP 1510 and various prototypes and evaluation models associated with the same. On information and belief, other industry participants were also working on relevant prior art systems. For example, Intel was also creating multiprocessor products in this market segment including the Intel Personal Client Architecture (IPCA). *See, e.g.*, <https://www.eetimes.com/intels-xscale-platform-takes-shot-at-ti-dsps/#>. Similarly, IBM was also working on its Power4 system at this time. *See, e.g.*, <https://www.ibm.com/ibm/history/ibml00/us/en/icons/power4/>. As such, a POSITA would have been further motivated to combine the ideas and technologies disclosed in the prior art

A POSITA would also have been motivated to perform these modifications and/or combinations to make the underlying device described in the reference more compact, faster, more energy efficient, and more economically viable for the reasons provided above and in the accompanying Exhibit C-2. For example, the claims are rendered obvious at least by the following non-exhaustive list of exemplary combinations: Kleinsorge and KITA, Gulick and KITA, Woolsey and KITA, Olukotun, KITA, and Zalewski; Olukotun, KITA, and OMAP; Olukotun, KITA, and Cupps; Olukotun, KITA, and Gulick; Olukotun, KITA, and Gary; Olukotun, KITA, and Toda; Olukotun, KITA, and Miyamoto; Olukotun, KITA, and Zalewski; Olukotun, KITA, and OMAP; Olukotun, KITA, and Asano; Zalewski, KITA, and Cupps; Zalewski, KITA, and Gulick; Zalewski, KITA, and Gary; Zalewski, KITA, and Toda; Zalewski, KITA, and Miyamoto; Zalewski, KITA, and OMAP; OMAP and KITA; OMAP, KITA, and

Cupps; OMAP, KITA, and Gulick; OMAP, KITA, and Gary; OMAP, KITA, and Toda; OMAP, KITA, and Miyamoto; OMAP, KITA, and Asano; Joy, KITA, and Zalewski; Joy, KITA, and OMAP; Joy, KITA, and Cupps; Joy, KITA, and Gulick; Joy, KITA, and Gary; Joy, KITA, and Toda; Joy, KITA, and Miyamoto; Joy, KITA, and Zalewski; Joy, KITA, and OMAP; OMAP, KITA, and Asano; Gary, KITA, and Zalewski; Gary, KITA, and OMAP; Gary, KITA, and Cupps; Gary, KITA, and Gulick; Gary and KITA; Gary, KITA, and Toda; Gary, KITA, and Miyamoto; Gary, KITA, and Asano; Killian, KITA, and Zalewski; Killian, KITA, and OMAP; Killian, KITA, and Cupps; Killian, KITA, and Gulick; Killian, KITA, and Gary; Killian, KITA, and Toda; Killian, KITA, and Miyamoto; Killian, KITA, and Zalewski and KITA; Killian, KITA, and OMAP; Killian, KITA, and Asano.

Defendant also incorporates herein by reference the IPR Petitions and exhibits in Cases IPR2021-01454, IPR2022-00756, IPR2022-00801, IPR2023-00819, and IPR2023-00975.

Defendant further reserves the right to rely on additional references and expert testimony to explain the knowledge of a POSITA and how a POSITA would interpret the disclosures of the '014 Patent or the prior art references.

More specifically, the asserted claims of the '014 Patent are rendered obvious by the prior art combinations identified in Exhibit C-2, which a POSITA would have had reasons to make as discussed above. Defendant may rely on cited or uncited portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. In the event Sonrai challenges the motivation to combine particular prior art references, Defendant reserves the right to supplement these contentions to further specify the motivation to combine the prior art to the extent necessary.

In addition to the charted '014 Patent obviousness references and other prior art references disclosed herein, Defendant may also rely on background materials to demonstrate the state of the art, which is relevant to obviousness of the asserted claims. The concepts claimed in the '014 Patent were prevalent in the field of multiprocessing systems, and well-known to ordinary artisans long before the earliest alleged conception date of the '014 Patent. While there are too many examples of background materials to list (and the OGP imposes no obligation to disclose materials used purely for background or state of the art), representative examples include all references cited in the '014 Patent and prosecution history of the related patent applications, all references cited herein, all references charted herein and within Exhibits B-1 through B-30, all references cited within the references cited and charted herein and within Exhibits B-1 through B-30, and documents included listed above, as well as productions by third parties and Sonrai itself, and other documents identified in the accompanying exhibits. The long-known concepts recited in these and similar background materials describe the background knowledge of one of skill in the art, which taken alone or in combination with prior art references described herein, render the asserted claims of the '014 Patent obvious.

Defendant's contentions that the references in this section, in various combinations, render the asserted claims of the '014 Patent obvious under 35 U.S.C. § 103 are in no way an admission or suggestion that each reference does not independently anticipate the asserted claims under 35 U.S.C. § 102. Any of the references disclosed herein, may be combined with other references disclosed herein, to render obvious, and therefore invalid, each of the asserted claims of the '014 Patent.

Sonrai has not alleged any nexus between its purported evidence of alleged secondary considerations for non-obviousness and the claims of the '014 Patent. To the extent Sonrai is

later able to identify and rely on any such alleged secondary considerations, including attempting to cite to purported evidence in support thereof, Defendant reserves the right to respond.

III. SECTION 112 DEFENSES

A. '241 Patent

Based on the Court's claim construction Order and Sonrai's apparent interpretation of claim terms in the '241 Patent as evidenced by the allegations in its complaints and preliminary infringement contentions, Defendant hereby provides the following contentions regarding invalidity under 35 U.S.C. § 112. The following contentions, made pursuant to the procedural schedule in this case, are subject to revision and amendment, including pursuant to the Orders issued in this case, to the extent appropriate in light of further investigation and discovery regarding the defenses, the review and analysis of expert witnesses, and/or the testimony of fact witnesses, including the named inventors, and any final or amended infringement contentions served by Sonrai. As stated above, the claim charts provided are based on the Court's claim construction Order and Sonrai's apparent interpretation of the claim scope, and should not be taken as an admission that the claims comply with 35 U.S.C. § 112.

Subject to the reservation of rights above, Defendant provides below an identification of asserted claims along with an identification of the specific limitations that are invalid pursuant to 35 U.S.C. § 112 ¶ 1 as lacking written description and/or enablement support.

1. Lack of Written Description

The claims of the '241 Patent are invalid because they fail to meet the written description requirement of 35 U.S.C. § 112. The '241 Patent does not describe the claimed invention in sufficient detail that a POSITA can reasonably conclude that the inventors had possession of the claimed invention, at least under the Court's constructions and Sonrai's apparent interpretations

as to their scope based on its preliminary infringement contentions, for at least the following claim terms or phrases:

- “a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage” (claims 1-3, 6, 9-11)
- “a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages” (claims 1-3, 6, 9-11);
- “a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” (claims 1-3, 6, 9-11);
- “wherein the load selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 2);
- “wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (V_{cfrb}) greater than the reference voltage (V_{ref}) then the maximum ripple on the target output selector means adds additional loads until the V_{cfrb} voltage is less than or equal to the reference voltage (V_{ref})” (claim 3);
- “each load selector means comprises an elevator circuit having an input terminal and an output terminal” (claim 9); and
- “turning on a load associated with the selected V_{pump} ” (claim 24)

2. Lack of Enablement

The claims of the ‘241 Patent are invalid because they fail to meet the enablement requirement of 35 U.S.C. § 112. The ‘241 Patent does not permit a POSITA to make or use the

alleged full scope of the claimed invention from the disclosures of the '241 Patent without undue experimentation, at least under the Court's constructions and Sonrai's apparent interpretations as to the claim scope based on its preliminary infringement contentions, for at least the following limitations:

- “a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage” (claim 1-3, 6, 9-11)
- “a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages” (claim 1-3, 6, 9-11);
- “a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit” (claim 1-3, 6, 9-11);
- “wherein the load selector means includes a target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (V_{cfra}) is greater than or equal to a reference voltage (V_{ref})” (claim 2);
- “wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (V_{cfrb}) greater than the reference voltage (V_{ref}) then the maximum ripple on the target output selector means adds additional loads until the V_{cfrb} voltage is less than or equal to the reference voltage (V_{ref})” (claim 3)
- “each load selector means comprises an elevator circuit having an input terminal and an output terminal” (claim 9); and
- “turning on a load associated with the selected V_{pump} ” (claim 24)

3. Indefiniteness

Although the Court's Markman Order denied Defendant's indefiniteness defenses, Defendant is not waiving those defenses. Defendant preserves its right to appeal the Court's Markman Order and, pending any such appeal, Defendant does not waive its indefiniteness defenses as set forth in its Preliminary Invalidity Contentions.

B. '014 Patent

Based on the Court's claim construction Order and Sonrai's apparent interpretation of claim terms in the '014 Patent as evidenced by the allegations in its complaints and preliminary infringement contentions, Defendant hereby provides the following contentions regarding invalidity under 35 U.S.C. § 112. The following contentions, made pursuant to the procedural schedule in this case, are subject to revision and amendment, including pursuant to the Orders issued in this case, to the extent appropriate in light of further investigation and discovery regarding the defenses, the review and analysis of expert witnesses, and/or the testimony of fact witnesses, including the named inventors, and any final or amended infringement contentions served by Sonrai. As stated above, the claim charts provided are based on the Court's claim construction Order and Sonrai's apparent interpretation of the claim scope, and should not be taken as an admission that the claims comply with 35 U.S.C. § 112.

Subject to the reservation of rights above, Defendant provides below an identification of asserted claims along with an identification of the specific limitations that are invalid pursuant to 35 U.S.C. § 112 ¶ 1 as lacking written description and/or enablement support.

1. Lack of Written Description

The claims of the '014 Patent are invalid because they fail to meet the written description requirement of 35 U.S.C. § 112. The '014 Patent does not describe the claimed invention in sufficient detail that a POSITA can reasonably conclude that the inventors had possession of the

claimed invention, at least under Sonrai's apparent interpretations as to their scope based on its preliminary infringement contentions, for at least the following claim terms or phrases:

- “multiple operating systems residing in a memory connected to said multiple processors” (claim 1)
- “wherein each of said multiple processors executes an operating system of said multiple operating systems” (claim 1)
- “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems” (claim 1)
- “multiple operating systems residing in a memory connected to said groups” (claim 7)
- “wherein each of said groups executes an operating system of said multiple operating systems” (claim 7)
- “two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems” (claim 7)
- “processor means for executing a plurality of operating system means” (claim 12)
- “wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means” (claim 12)
- “memory means for storing said plurality of operating system means” (claim 12)

2. Lack of Enablement

The claims of the '014 Patent are invalid because they fail to meet the enablement requirement of 35 U.S.C. § 112. The '014 Patent does not permit a POSITA to make or use the alleged full scope of the claimed invention from the disclosures of the '014 Patent without undue

experimentation, at least under Sonrai's apparent interpretations as to the claim scope based on its preliminary infringement contentions, for at least the following limitations:

- “multiple operating systems residing in a memory connected to said multiple processors” (claim 1)
- “wherein each of said multiple processors executes an operating system of said multiple operating systems” (claim 1)
- “two or more of said multiple processors are capable of simultaneously executing two or more operating systems of said multiple operating systems” (claim 1)
- “multiple operating systems residing in a memory connected to said groups” (claim 7)
- “wherein each of said groups executes an operating system of said multiple operating systems” (claim 7)
- “two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems” (claim 7)
- “wherein each of said groups executes a distinct operating system of said multiple operating systems” (claim 11)
- “processor means for executing a plurality of operating system means” (claim 12)
- “wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means” (claim 12)
- “memory means for storing said plurality of operating system means” (claim 12)

3. Indefiniteness

The claims of the '014 Patent include the following claim limitations that are indefinite for informing a POSITA with reasonable certainty as to the full scope of the claims, at least

under Sonrai's apparent interpretation of the claims. Accordingly, the claims in which they appear are invalid under 35 U.S.C. § 112 ¶ 2.

- “two or more of said plurality of processor groups are capable of simultaneously executing two or more operating systems of said multiple operating systems” (claim 7)
- “wherein each of said groups executes a distinct operating system of said multiple operating systems” (claim 11)
- “processor means for executing a plurality of operating system means” (claim 12)
- “wherein said processor means is operable to simultaneously execute two or more operating system means of said plurality of operating system means” (claim 12)
- “memory means for storing said plurality of operating system means” (claim 12)

IV. SECTION 101 DEFENSES

The Asserted Claims of the '014 patent are directed to ineligible subject matter under 35 U.S.C. § 101. Whether an invention is eligible for patent protection under 35 U.S.C. § 101 is a “threshold test.” *See Bilski v. Kappos*, 130 S. Ct. 3218, 3225 (2010). Under this “threshold test,” the court “must first determine whether the claims at issue are directed to a patent-ineligible concept,” such as an abstract idea, a law of nature, or a natural phenomenon. *Alice Corp. Pty. Ltd. v. CLS Bank Int'l*, 134 S. Ct. 2347, 2355 (2014). If so, the court must then “consider the elements of each claim both individually” and “as an ordered combination” to determine whether the additional elements “transform the nature of the claim” into a patent eligible application.” *See id.* (quoting *Mayo Collaborative Servs. v. Prometheus Labs., Inc.*, 132 S. Ct 1289, 1297 (2012)).

In *Alice*, the Supreme Court set forth a two-part test to analyze patent eligibility: (1) determine whether the claims are directed to an abstract idea or other patent-ineligible concept, and (2) if so, determine whether the claim has an “inventive concept” sufficient to transform the claim into a patent-eligible concept. *Id.* at 2355. But “well-understood, routine, conventional activity” or technology, including general purpose computers and computer networks, do not provide an “inventive concept.” *Id.* at 2357-59. “Thus, if a patent's recitation of a computer amounts to a mere instruction to implement an abstract idea on a computer, that addition cannot impart patent eligibility.” *Id.* at 2358; *see also Bancorp Servs., L.L.C. v. Sun Life Assur. Co. of Canada (U.S)*, 687 F.3d 1266 (Fed. Cir. 2012).

The asserted claims of the '014 patent are directed to unpatentable subject matter. First, the claims are directed to the abstract idea of having microprocessors execute their own operating systems in a multiprocessing computer system. Given the claim language and the specification, the claims are “directed to a result or effect that itself is the abstract idea and merely invokes generic processes and machinery rather than a specific means or method that improves the relevant technology.” *Yu v. Apple Inc.*, 1 F.4th 1040, 1043 (Fed. Cir. 2021).

. The '014 patent articulates no “inventive concept” sufficient to transform the abstract idea into a patent-eligible concept. Using multiple operating systems in a multiprocessor system was well known in the prior. *See* Exhibit C-2. For example, the '014 patent admits, in a “conventional multiprocessing scheme,” it was known that “chip multiprocessor [may] include[] multiple processors ... on a single die.” '014 patent 1:34-37, *see also* Fig. 2. Such a prior art system was known to have an operating system stored in a memory as well as a bus connecting the processors and the memory. Likewise, the '014 patent explains that prior art teachings “support[] multiple processors executing multiple operating systems,” using virtual processors.

Id. at 1:60-65. The '014 patent does not claim to have invented any new multiprocessor, nor does it claim to have improved upon existing computer hardware to address any of the problems of implementing virtual machines on single die multi-processors, which already existed. Moreover, memory schemes for dealing with systems with multiple processors and operations systems that shared memory were well known, routine, conventional and understood in the industry. *See* Exhibit C-2. The solution proposed by the '014 patent—simply the abstract idea of using two operating systems with a single die multiprocessor—was also long understood in the industry. *See id.*; '014 patent 1:25-2:4; Fig. 1, Fig. 2. People with ordinary skill in the art had known of the claimed systems for years—they are conventional systems aimed at solving conventional problems in the art. *See* Exhibit C-2; '014 patent 1:25-2:4; Fig. 1, Fig. 2.

V. TECHNICAL DOCUMENT PRODUCTION

Defendant has produced the following technical documents sufficient to show the operation of the accused products identified in Sonrai's preliminary infringement contentions: APL-SON787-00000001-APL-SON787-00775966. Defendant has further identified additional technical documents that contain confidential information of third-party SK Hynix and Defendant will produce those additional third-party SK Hynix confidential documents upon approval by SK Hynix.

Dated: June 15, 2023

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CERTIFICATE OF SERVICE

The undersigned certifies that on this 15th day of June, 2023, all counsel of record who are deemed to have consented to electronic service are being served with a copy of this document through email.

/s/ Patrick Park

Patrick Park