

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CURRENT LIGHTING SOLUTIONS, LLC d/b/a GE CURRENT,

Petitioner,

v.

JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD.,

Patent Owner.

INTER PARTES REVIEW NO. IPR2023-00984
PATENT NO. 9,841,174

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §312

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PETITIONER'S EXHIBIT LIST

Exhibit	Shorthand	Description
EX1001	'174 Patent	U.S. Patent No. 9,841,174
EX1002	Lebby	Declaration of Michael Lebby, Ph.D.
EX1003	'174 FH	Excerpts from File History of the '174 Patent
EX1004	Sadwick566	PCT App. Pub. No. WO2015/066566
EX1005	Ivey813	U.S. Patent No. 8,596,813
EX1006	Ivey345	U.S. Patent App. Pub. No. 2014/0015345
EX1007	UL1993	<i>UL 1993 Standard for Safety Self-Ballasted Lamps and Lamp Adapters</i> , Underwriters Laboratories Inc., 2012
EX1008	Sadwick	U.S. Patent App. Pub. No. 2017/0311396
EX1009	Powell	U.S. Patent No. 9,438,165
EX1010	Digi-Key	Wayback Machine capture of <i>Product Index > Discrete Semiconductor Products > FETs – Arrays</i> , Digi-Key (Apr. 10, 2014, 11:03 AM), http://www.digikey.com/product-search/en/discrete-semiconductor-products/fets-arrays/1377094 [https://web.archive.org/web/20140410110347/http://www.digikey.com/product-search/en/discrete-semiconductor-products/fets-arrays/1377094]
EX1011	Fairchild	Wayback Machine capture of <i>FDG6303N Dual N-Channel, Digital FET</i> , Fairchild Semiconductor (Mar. 8, 2014, 4:25 AM), http://www.fairchildsemi.com/ds/FD/FDG6303N.pdf [https://web.archive.org/web/20140308042522/http://www.fairchildsemi.com/ds/FD/FDG6303N.pdf]
EX1012	Premier	Wayback Machine capture of <i>Should You Replace Your T8 Fluorescent Lamps with T8 LED Tubes? (updated)</i> , Premier Lighting (June 27, 2014, 9:59 PM), http://www.premierltg.com/should-you-replace-your-t8-fluorescent-lamps-with-t8-led-tubes-2/ [https://web.archive.org/web/20140627215905/http://www.premierltg.com/should-you-replace-your-t8-fluorescent-lamps-with-t8-led-tubes-2/]

Exhibit	Shorthand	Description
EX1013	Hsia661	U.S. Patent App. Pub. No. 2015/0181661
EX1014	Pyeon	U.S. Patent No. 9,240,227
EX1015	Dedic	U.S. Patent App. Pub. No. 2013/0099948
EX1016	Mandal	M.K. Mandal & B.C. Sarkar, <i>Ring oscillators: Characteristics and applications</i> , 48 Indian J. of Pure & Applied Physics 136 (2010)
EX1017	Sadwick454	U.S. Patent No. 8,502,454
EX1018	Parks	Wayback Machine capture of Michael Parks, <i>Don't Burn Out! Calculating LED Current Limiting Resistor</i> , Mouser Electronics (Oct. 10, 2014, 6:43 AM), http://www.mouser.com/blog/dont-burn-out-calculating-led-current-limiting-resistor [https://web.archive.org/web/20141010064339/http://www.mouser.com/blog/dont-burn-out-calculating-led-current-limiting-resistor]
EX1019	Etkina	Eugenia Etkina & Gorazd Planinšič, <i>Light-Emitting Diodes: Exploration of Underlying Physics</i> , 52 The Physics Teacher 212 (2014)
EX1020	Briggs	U.S. Patent No. 8,564,214
EX1021	Guang	U.S. Patent App. Pub. No. 2017/0303353
EX1022	Physics-Classroom	Wayback Machine capture of <i>Two Types of Connections</i> , The Physics Classroom (Dec. 01, 2011, 12:54 AM), https://www.physicsclassroom.com/Class/circuits/u9l4b.cfm [https://web.archive.org/web/20111201005447/https://www.physicsclassroom.com/Class/circuits/u9l4b.cfm]
EX1023	Nave-1	Wayback Machine capture of Rod Nave, <i>OR Gate</i> , HyperPhysics (Mar. 3, 2004, 3:58 PM), http://hyperphysics.phy-astr.gsu.edu/hbase/Electronic/or.html [https://web.archive.org/web/20040303155843/http://hyperphysics.phy-astr.gsu.edu/hbase/Electronic/or.html]

Exhibit	Shorthand	Description
EX1024	Nave-2	Wayback Machine capture of Rod Nave, <i>Relaxation Oscillator Concept</i> , HyperPhysics (May 1, 2001, 4:38 AM), http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/relaxo.html [https://web.archive.org/web/20010501043853/http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/relaxo.html]
EX1025		Claim Construction Order, <i>Jiaxing Super Lighting Electric Appliance Co., Ltd. v. MaxLite, Inc.</i> , No. 2:19-cv-04047-PSG-MAA, Dkt. No. 117 (C.D. Cal. May 27, 2021)
EX1026		Scheduling Order, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA, Dkt. No. 31 (W.D. Tex. 2022)
EX1027		Draft of Defendant's Stipulation of Invalidity Contentions to be filed in <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA (W.D. Tex. 2022)
EX1028		Plaintiffs Jiaxing Super Lighting Electric Appliance Co., Ltd., and Obert, Inc.'s Preliminary Infringement Contentions, Claim Chart B1, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA (W.D. Tex. Oct. 19, 2022)
EX1029		Plaintiffs Jiaxing Super Lighting Electric Appliance Co., Ltd., and Obert, Inc.'s Preliminary Infringement Contentions, Claim Chart B2, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA (W.D. Tex. Oct. 19, 2022)
EX1030		Declaration of Sylvia D. Hall-Ellis, Ph.D.
EX1031		Declaration of Nathaniel E. Frank-White of the Internet Archive
EX1032	Hsia299	U.S. Patent No. 8,979,299

Exhibit	Shorthand	Description
EX1033		Wayback Machine capture of <i>Catalog of Standards UL 1993 Self-Ballasted Lamps and Lamp Adapters</i> , Underwriters Laboratories (Jan. 21, 2014, 8:37 AM), http://www.ul.com/global/eng/pages/solutions/standards/accessstandards/catalogofstandards/standard/?id=1993_4 [https://web.archive.org/web/20140121083748/http://www.ul.com/global/eng/pages/solutions/standards/accessstandards/catalogofstandards/standard/?id=1993_4]
EX1034		Order Resetting Markman Hearing via Zoom, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA (W.D. Tex. June 7, 2023)

CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1pre]	A light-emitting diode (LED) tube lamp, comprising:
	[1a]	a lamp tube;
	[1b]	two end caps, each having an external connection terminal, and each coupled to a respective end of the lamp tube, wherein the external connection terminals are configured to receive an external driving signal;
	[1c]	a rectifying circuit, coupled to the external connection terminals, for rectifying the external driving signal to produce a rectified signal;
	[1d]	a filtering circuit, coupled to the rectifying circuit, for filtering the rectified signal to produce a filtered signal;
	[1e]	a driving circuit, coupled to the filtering circuit, for converting the filtered signal into a driving signal;
	[1f]	an LED module, coupled to the driving circuit, for emitting light based on the driving signal; and
	[1g]	an installation detection module, configured to detect an installation state between the LED tube lamp and a lamp socket, wherein the installation detection module comprises:
	[1h]	a first circuit, configured to generate a pulse signal, wherein the first circuit comprises a discharge path;
	[1i]	a second circuit, coupled to the first circuit and configured to receive and output the pulse signal; and
	[1j]	a third circuit, coupled to a power loop of the LED tube lamp and the second circuit and configured to determine whether to conduct the power loop according to the pulse signal,
	[1k]	wherein the pulse signal is fed back to the discharge path of the first circuit, and the discharge path is conducted when the pulse signal is pulled to a high level voltage, and

Claim	Limitation No.	Limitation
	[11]	wherein the pulse signal is pulled to a low level voltage after the discharge path has been conducted for a predetermined time period.
2		The LED tube lamp according to claim 1, wherein the predetermined time period is a pulse-on period of the pulse signal.
3		The LED tube lamp according to claim 1, wherein the discharge path is cut off when the pulse signal is pulled to the low level voltage.
5		The LED tube lamp according to claim 1, wherein the installation detection module further comprises: a fourth circuit, configured to detect a sampling signal on the power loop so as to determine the installation state between the LED tube lamp and the lamp socket.
6		The LED tube lamp according to claim 5, wherein the fourth circuit further compares the sampling signal with a predefined signal, the fourth circuit outputs a high level signal when a signal level of the sampling signal is greater than or equal to the predefined signal and outputs a low level signal when the signal level of the sampling signal is smaller than the predefined signal.
7		The LED tube lamp according to claim 6, wherein the third circuit is conducted in response to the high level signal so as to cause the power loop to remain conductive.
8		The LED tube lamp according to claim 6, wherein the third circuit is cut off in response to the low level signal so as to cause the power loop to remain open.
9		The LED tube lamp according to claim 6, wherein the third circuit is cut off in response to the low level signal so as to reduce a current on the power loop less than 5 MIU (Measurement Indication Units).
10	[10pre]	A ballast by-pass light-emitting diode (LED) tube lamp, comprising:
	[10a]	a lamp tube;
	[10b]	two end caps, each having an external connection terminal, and each coupled to a respective end of the lamp tube, wherein the external connection terminals are configured to receive an external driving signal;
	[10c]	an LED module, configured to emit light based on the external driving signal; and

Claim	Limitation No.	Limitation
	[10d]	an installation detection module, coupled on a power loop of the LED tube lamp and configured to detect a transient current on the power loop and compare the transient current with a predefined signal,
	[10e]	wherein when a signal level of the transient current is smaller than the predefined signal, the installation detection module limits a current on the power loop less than 5 MIU by controlling a conduction state of the power loop.
11		The LED tube lamp according to claim 10, wherein the installation detection module comprises: a detection determining circuit, configured to detect the transient current, compare the transient current with the predefined signal, and output a high level signal or a low level signal according to a comparison result.
12		The LED tube lamp according to claim 11, wherein the installation detection module further comprises: a detection pulse generating module, configured to generate a pulse signal, wherein the detection determining circuit detects the transient current on the power loop during a pulse-on period of the pulse signal.
13		The LED tube lamp according to claim 12, wherein the detection pulse generating module comprises a discharge path, the pulse signal is fed back to the discharge path and the discharge path is conducted when the pulse signal is pulled to a high level voltage, and wherein the pulse signal is pulled to a low level voltage after the discharge path has been conducted for a predetermined time period.
14		The LED tube lamp according to claim 13, wherein the predetermined time period is the same as the pulse-on period of the pulse signal.
15		The LED tube lamp according to claim 13, wherein the discharge path is cut off when the pulse signal is pulled to the low level voltage.

Claim	Limitation No.	Limitation
16		The LED tube lamp according to claim 12, wherein the installation detection module further comprises: a switch circuit, coupled to the detection determining circuit and the detection pulse generating module and configured to maintain a conductive state during the pulse-on period of the pulse signal or when receiving the low level signal from the detection determining circuit.
17		The LED tube lamp according to claim 16, wherein the installation detection module further comprises: a detection result latching circuit, coupled to the detection determining circuit, the detection pulse generating module, and the switch circuit, wherein at least one of the pulse signal, the high level signal, and the low level signal is provided to the switch circuit through the detection result latching circuit.
18	[18pre]	A detection method for a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket, the detection method comprising:
	[18a]	generating a pulse signal by a detection pulse generating module;
	[18b]	receiving the pulse signal by a switch circuit coupled on a power loop of the LED tube lamp, wherein the switch circuit is conducted during a pulse-on period of the pulse signal to cause the power loop to be conductive;
	[18c]	detecting a sampling signal on the power loop;
	[18d]	comparing the sampling signal with a predefined signal; and
	[18e]	limiting a current on the power loop less than 5 MIU when a signal level of the sampling signal is smaller than the predefined signal.
19		The detection method according to claim 18, further comprising: conducting the power loop when the signal level of the sampling signal is greater than or equal to the predefined signal.

Claim	Limitation No.	Limitation
20	[20a]	The detection method according to claim 18, wherein the detection pulse generating module comprises a discharge path, and the step of generating the pulse signal by the detection pulse generating module comprises:
	[20b]	pulling the pulse signal to a high level voltage when the detection pulse generating module receives a driving signal;
	[20c]	feeding the pulse signal back to the discharge path, so as to conduct the discharge path when the pulse signal is pulled to the high level voltage; and
	[20d]	pulling the pulse signal to a low level voltage after the discharge path has been conducted for a predetermined time period.
21	The detection method according to claim 20, wherein the predetermined time period is the same as the pulse-on period of the pulse signal.	
22	The detection method according to claim 20, wherein the step of generating the pulse signal by the detection pulse generating module further comprises: cutting off the discharge path when the pulse signal is pulled to the low level voltage.	
23	[23pre]	A light-emitting diode (LED) tube lamp, comprising:
	[23a]	a lamp tube;
	[23b]	two end caps, each having an external connection terminal, and each coupled to a respective end of the lamp tube, wherein the external connection terminals are configured to receive an external driving signal;
	[23c]	an LED module, configured to emit light based on the external driving signal; and
	[23d]	an installation detection module, coupled to a power loop of the LED tube lamp and configured to detect a sampling signal on the power loop and compare the sampling signal with a predefined signal,

Claim	Limitation No.	Limitation
	[23e]	wherein a leakage loop is formed between the external connection terminal on one of the end caps and a ground when the one of the end caps is inserted into a lamp socket but the other one is grounded by an object, and
	[23f]	wherein the installation detection module is activated by a driving voltage on the leakage loop.
24		The LED tube lamp according to claim 23, wherein each end cap further has a dummy terminal for connecting to the lamp socket, and at least one dummy terminal is electrically isolated from the installation detection module.
25		The LED tube lamp according to claim 23, wherein the driving voltage is generated based on the external driving signal when the leakage loop is formed.
26	[26pre]	A light-emitting diode (LED) tube lamp, comprising:
	[26a]	a lamp tube;
	[26b]	two end caps, each having an external connection terminal, and each coupled to a respective end of the lamp tube, wherein the external connection terminals are configured to receive an external driving signal;
	[26c]	an LED module, configured to emit light based on the external driving signal; and
	[26d]	an installation detection module, coupled to a power loop of the LED tube lamp and configured to detect a sampling signal on the power loop and compare the sampling signal with a predefined signal,
	[26e]	wherein the installation detection module comprises: a control module, configured to output a control signal for controlling a conduction state of the power loop and when a signal level of the sampling signal is smaller than the predefined signal, the control module limits a current on the power loop less than 5 MIU by controlling the conduction state,

Claim	Limitation No.	Limitation
	[26f]	wherein the control module generates the control signal having a first waveform during a detection stage and generates the control signal having a second waveform during an operating stage.
27	The LED tube lamp according to claim 26, wherein the control module comprises: a detection result latching circuit, coupled to a detection determining circuit, a detection pulse generating module, a switch circuit, wherein at least one of a pulse signal, a high level signal, and a low level signal is provided to the switch circuit through the detection result latching circuit.	
28	[28pre]	A light-emitting diode (LED) tube lamp, comprising:
	[28a]	a lamp tube;
	[28b]	two end caps, each having an external connection terminal, and each coupled to a respective end of the lamp tube, wherein the external connection terminals are configured to receive an external driving signal;
	[28c]	an LED module, configured to emit light based on the external driving signal; and
	[28d]	an installation detection module, coupled on a power loop of the LED tube lamp and configured to generate a pulse signal for controlling a conduction state of the power loop and detect a sampling signal on the power loop during a pulse-on time of the pulse signal,
	[28e]	wherein the installation detection module limits a current on the power loop to less than 5 MIU by setting the pulse-on time less than or equal to 1 millisecond.
29	The LED tube lamp according to claim 28, wherein the installation detection module limits a current on the power loop to less than 5 MIU by setting the pulse-on time between 10 microseconds to 1 millisecond.	
32	[32pre]	A light-emitting diode (LED) tube lamp, comprising:

Claim	Limitation No.	Limitation
	[32a]	a lamp tube;
	[32b]	two end caps, each having an external connection terminal, and each coupled to a respective end of the lamp tube, wherein the external connection terminals are configured to receive an external driving signal;
	[32c]	an LED module, configured to emit light based on the external driving signal; and
	[32d]	an installation detection module, coupled to a power loop of the LED tube lamp and configured to generate a plurality of pulse signals for controlling a conduction state of the power loop and detect a sampling signal on the power loop during a pulse-on time of each of the pulse signals,
	[32e]	wherein a time interval between at least two consecutive pulse signals of the pulse signals is designed such that at least one of the two consecutive pulse signals occurs when the external driving signal is at non-zero level.

I. INTRODUCTION

Claims 1-3, 5-29, and 32 recite a circuit and related methods for preventing electric shock due to accidental user contact with a light-emitting device (LED) tube lamp's terminals during relamping. EX1006, however, already disclosed such a circuit and how to use it. And to the extent any differences exist, such differences were obvious, including in view of Ivey813, UL1993, Sadwick, and Powell. The Challenged Claims are therefore unpatentable.

II. MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

The real party-in-interest is Current Lighting Solutions, LLC d/b/a GE Current.

B. Related Matters (§42.8(b)(2))

The following proceedings involve the '174 Patent.

Jiaying Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current, No. 6:22-CV-00534-ADA (W.D. Tex. 2022) (the "Litigation").

Jiaying Super Lighting Elec. Appliance Co., Ltd. v. MaxLite, Inc., No. 2:19-cv-04047-PSG-MAA (C.D. Cal. 2019) ("*Maxlite* Action").

C. Lead and Back-Up Counsel (§42.8(b)(3))

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Petitioner consents to electronic service.

III. GROUNDS FOR STANDING

Petitioner certifies that the '174 Patent is available for *inter partes* review ("IPR"), and Petitioner is not barred or estopped from requesting IPR on the grounds identified in this Petition.

IV. STATEMENT OF PRECISE RELIEF REQUESTED

A. Claims for Which Review Is Requested (§42.104(b)(1))

Petitioner requests cancellation of claims 1-3, 5-29, and 32.

B. Statutory Grounds of Challenge (§42.104(b)(2))¹

The Challenged Claims are unpatentable under the following grounds:

Ground	Claims	Statutory Basis	Prior Art
1	10-12, 16-19, 23-29, and 32	§103	Ivey813, Ivey345, UL1993
2	10-12, 16-19, 23-29, and 32	§103	Ivey813, Ivey345, UL1993, Sadwick
3	1-3, 5-9, 13-15, and 20-22	§103	Ivey813, Ivey345, UL1993, Powell
4	1-3, 5-9, 13-15, and 20-22	§103	Ivey813, Ivey345, UL1993, Sadwick, Powell

April 29, 2015 is the '174 Patent's earliest claimed priority date ("ECPD").

EX1001, cover. Accordingly:

- Published December 3, 2013, Ivey813 is prior art under §102(a)(1).
- Published January 16, 2014, Ivey345 is prior art under §102(a)(1).
- UL1993 is prior art under §102(a)(1) as of its December 4, 2012, publication date (EX1007, 3) and at least as of January 21, 2014, when it was publicly accessible from Underwriters Laboratories' website (EX1031, ¶¶1-8 (¶¶1-5: explaining Wayback Machine URL); EX1033,

¹ All Grounds are supported by a person of ordinary skill in the art's ("POSITA's") general knowledge. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020).

1) (*compare* EX1033, 1-4 (“Table of Contents”), *with* EX1007, 9-12).

EX1002, ¶55. Other references confirm UL1993’s pre-ECPD public availability. *E.g.*, EX1032, 6:21-25.

- Filed October 31, 2014, Sadwick is prior art under §102(a)(2).
- Filed October 8, 2014, Powell is prior art under §102(a)(2).

V. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of this IPR, Petitioner submits that the level of ordinary skill in the field would require at least a bachelor’s degree in electrical engineering or a comparable field and 3 years of experience designing lighting fixtures or systems, or equivalents. EX1002, ¶¶23-25. More education could have compensated for less experience, and vice versa.² *Id.*

VI. ’174 PATENT

A. Overview

The ’174 Patent explains that during relamping of an LED tube lamp, when “one end cap thereof is inserted into a lamp socket but the other is not,” a user may

² All Petition statements about the knowledge and skills of, and what would have been understood by, a POSITA are from this perspective as of the ECPD. *See* EX1002, ¶18; *see also id.*, ¶¶17-22 (scope of work, legal understanding, and basis for opinions), 2-16 & 26 (experience/qualifications).

receive an electric shock by making contact with the latter. EX1001, 2:54-59; EX1002, ¶33. To prevent such a shock, the '174 Patent discloses an installation detection module configured in an LED tube lamp. EX1001, Abst., 6:66-7:22, 37:52-38:25, Fig.15A; EX1002, ¶33. Figure 15B depicts one embodiment:

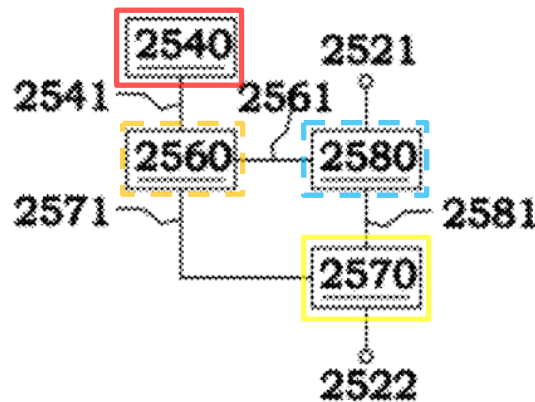


Fig. 15B

EX1001, Fig.15B,³ 38:60-62; EX1002, ¶33. Installation detection module 2520 includes detection pulse generating module 2540 (solid-red), detection result latching circuit 2560 (dotted-orange), switch circuit 2580 (dotted-blue), and detection determining circuit 2570 (solid-yellow). EX1001, Fig.15B, 38:62-65; EX1002, ¶¶33-38. Detection pulse generating module 2540 periodically outputs a pulse signal to detection result latching circuit 2560, which may use the pulse signal

³ All colorized figures are annotated.

as “a time point” for when to store a “detection result signal” received at detection result terminal 2571. EX1001, 39:12-27, 39:4-8, 46:5-18; EX1002, ¶¶33-34.

Detection result latching circuit 2560 outputs the stored detection result to switch circuit 2580 (EX1001, Fig.15B, 39:12-27) and, in some embodiments, may also store and output the pulse signal itself (EX1001, 41:48-58, 39:65-40:1). EX1002, ¶¶34-35. Switch circuit 2580 controls the conducting state across the LED tube lamp such that, when detection result latching circuit 2560’s output is high (such as when the stored detection result is high and/or, in some embodiments, when the pulse is high), the LED tube lamp conducts. EX1001, 39:65-40:3; EX1002, ¶35.

Detection determining circuit 2570 “detects a sampling signal on the power loop” such as “current passing through terminals 2521 and 2522” and detects whether such current “is above or below a specific current value.” EX1001, Fig.15B, 40:3-8, 39:8-11; EX1002, ¶36. When the LED tube “is correctly installed,” such current will be above the specific current value, and detection determining circuit 2570 will output a high logic level detection result signal to detection result latching circuit 2560. EX1001, 43:11-30; EX1002, ¶36. The opposite occurs in an incorrect installation (e.g., shock situation). EX1001, 43:31-37; EX1002, ¶36.

B. Prosecution History

During prosecution, the Office issued one Action that allowed claims 1-8 and rejected claims 9-22 for, *inter alia*, anticipation under §102 over Sadwick566—the

PCT application that corresponds to Sadwick. EX1003, 146-51/389; EX1004, cover; EX1008, cover.

In response, Applicant provided various amendments and traverses, including amending independent claim 10 to recite “[a] ballast by-pass light-emitting diode (LED) tube lamp...” *Id.*, 272-73/389, 281-83/389. Applicant alleged that Sadwick566 failed to disclose the amended language by teaching a “shock hazard protection circuit” used only in a “conventional direct replacement type LED lamp... powered by ballasts” (*id.*, 281/389), and that such a circuit “may easily obtain a wrong detection result if... utilized in [a] ballast by-pass LED tube lamp” (*id.*, 282/389, 286-88/389).

The Examiner then allowed the claims and also newly presented claims 23-32. *Id.*, 275-12/389, 345-48/389.

C. Claim Construction (§42.104(b)(3))

For purposes of this IPR, all terms should be given their plain and ordinary. EX1002, ¶39.

1. “detection result latching circuit”

Claims 17 and 27 recite a “detection result latching circuit.” In the *Maxlite* Action, the court construed the term to mean “circuit that reverses its signal level when the detected result *or pulse signal from the detection pulse generating module* is applied and maintains its signal level based on the detected result.” EX1025, 26-

28.⁴ Petitioner disagrees with the *Maxlite* Court’s construction, particularly the emphasized portion. The claims contain no requirement that the detection result latching circuit necessarily outputs a reversed signal level when receiving a pulse signal from the claimed “pulse generating module.” EX1002, ¶41. In fact, the ’174 Patent explains that, in some embodiments, the pulse signal can be received by the detection result latching circuit simply “to inform the detection result latching circuit 2560 of a time point for latching (storing) the detection result.” *E.g.*, EX1001, 39:12-16; EX1002, ¶41. The prior construction is thus overly narrow and, for purposes of this IPR, the term should instead be given its plain and ordinary meaning. EX1002, ¶41.

VII. REASONS FOR THE RELIEF REQUESTED UNDER 37 C.F.R. §§42.22(A)(2) AND 42.104(B)(4)

A. Ground 1: Ivey813, Ivey345, and UL1993 Render Obvious Claims 10-12, 16-19, 23-29, and 32

1. Ivey813

Ivey813 describes “a light emitting diode (LED) based light tube.” EX1005, 1:13-16; EX1002, ¶42. Figure 1 shows an example:

⁴ All emphasis added unless otherwise indicated.

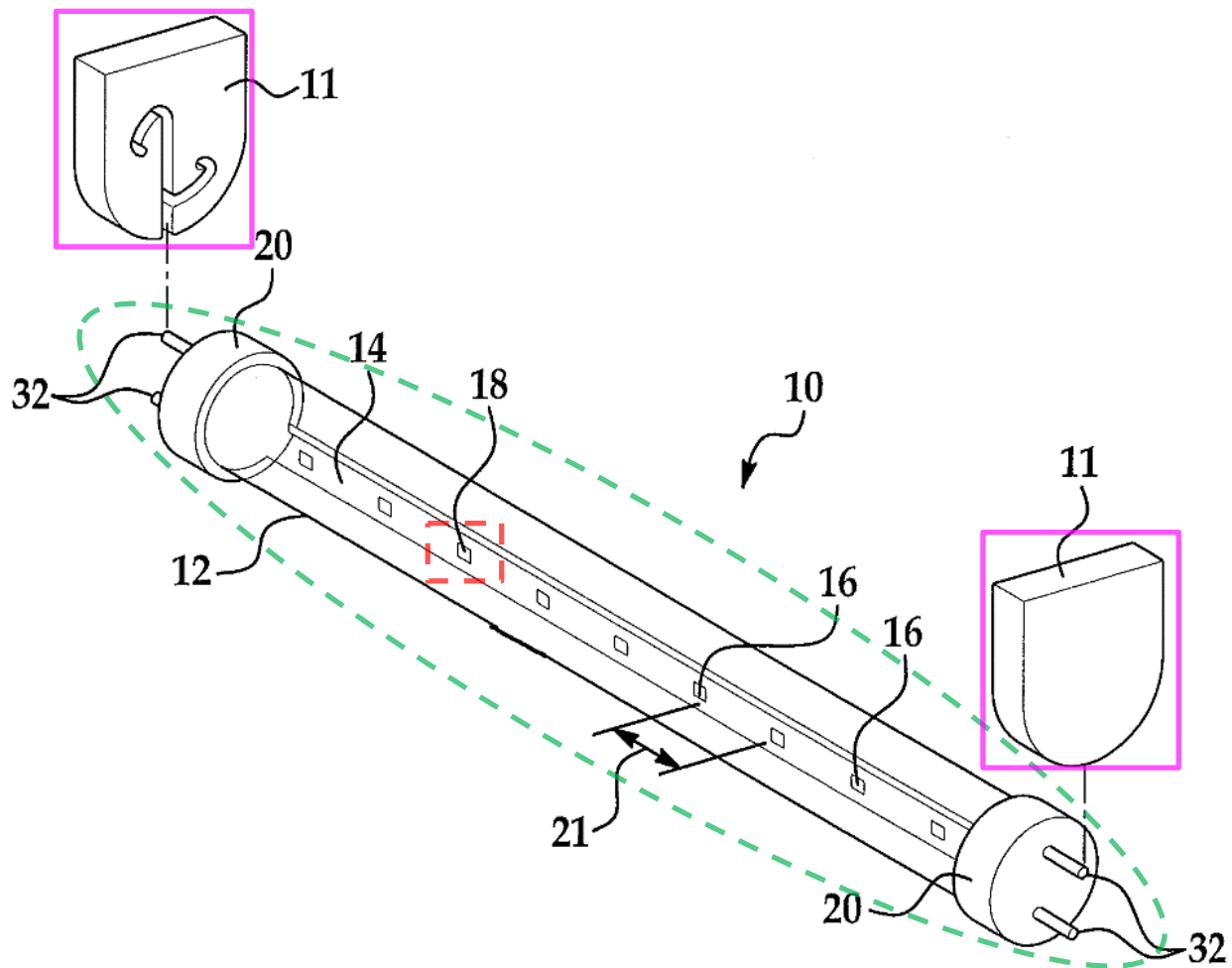


FIG. 1

EX1005, Fig.1; EX1002, ¶42. Figure 1 depicts LED light tube 10 (dotted-green) comprising an elongated housing 12 with two end caps 20 attached at opposing ends of housing 12. EX1005, 1:37-39, 1:50-51; EX1002, ¶42. Each end cap 20 includes pins 32, each of which electrically connect the LED light tube to fixture 11 (solid-pink) or act as a “‘dummy pin’ that does not provide an electrical connection.” EX1005, 5:1-16; EX1002, ¶42. As a POSITA would have recognized, fixture 11 can be, “for example, an existing fluorescent lamp fixture” and thus “can contain a

ballast,” or can instead directly power the LED light tube 10 with mains line power, such as when the LED light tube 10 is a ballast-bypass (“type B”) LED tube. *See* EX1005, 3:51-56; EX1012,⁵ 3-4; EX1001, 2:60-3:3; EX1013, ¶[0006]; EX1002, ¶42. Separately, a POSITA would have also been motivated to modify LED light tube 10 to be a type-B LED tube, because such would have allowed LED light tube 10’s operation to be no longer contingent on a ballast, thereby increasing power efficiency and reducing maintenance cost. *See* EX1013, ¶¶[0006]-[0008] (explaining “ballast-compatible” LED tubes are “more expensive and less efficient” than “AC mains-operable” LED tubes); EX1012, 3-4; EX1002, ¶¶42, 27-30. And a POSITA would have known how to perform such a modification. *See* EX1001, 2:60-3:3 (“**Currently**, LED tube lamps used to replace traditional fluorescent lighting devices can be primarily categorized into two types. One is for ballast-compatible LED tube lamps...; and the other one is for ballast by-pass LED tube lamps....”); EX1013, ¶[0006] (same, reworded); EX1002, ¶42.

The LED light tube 10 also comprises circuit board 14 spanning housing 12. EX1005, 1:37-39; EX1002, ¶43. Circuit board 14 has LEDs 18 (dotted-red)

⁵ *See* EX1031, ¶¶1-8 (¶¶6-7: explaining attachments), pp.17-21 (establishing pre-ECPD public availability).

mounted to its surface and conductive connections from the pins 32 to the LEDs 18.
EX1005, 2:13-17, 3:27-37, 3:63-67; EX1002, ¶43.

Circuit board 14 also includes power converter 36 (solid-brown) near end caps 20 to “convert the power received through the fixture [via the pins] into power usable by and suitable for the LEDs”:

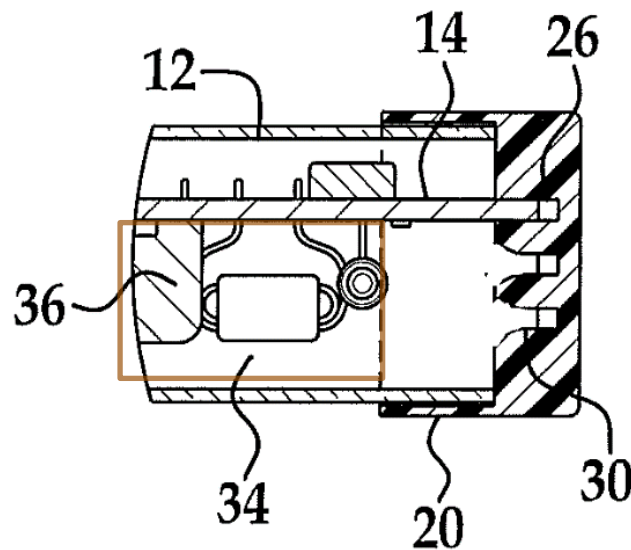


FIG. 7

EX1005, Fig.7, 5:31-35; EX1002, ¶44. Power converter 36 includes various circuits, e.g., “a rectifier circuit” and “main filter circuit.” EX1005, 5:36-39; EX1002, ¶44.

2. Ivey345

Ivey345 is directed to “a system and method for protecting a person from electrical shock when interacting with an electrical device.” EX1006, ¶[0002]; EX1002, ¶45. As Ivey345 teaches, “[c]ompact fluorescent light bulbs (CFLs) and

light emitting diode based (LED-based) lights are gaining popularity,” but such “line-powered electrical devices” also carry certain “drawbacks.” EX1006, ¶¶0004]; EX1002, ¶45. Particularly, “if the power terminal is connected using one connector and the subject, for example a person installing a new bulb, comes into contact with the return terminal in another connector that has not yet been mated, the person may receive a shock by completing the circuit from the return terminal to ground.” EX1006, ¶¶0005]; EX1002, ¶45.

As a solution, Ivey345 describes implementing a “current limiting circuit” that “detect[s] the presence of a foreign object, for example, a person’s body, in the circuit path and limit the flow of current through the object while allowing substantially full current to flow when an intended electrical connection is established between a power source and load.” EX1006, ¶¶0010]; EX1002, ¶46.

Ivey345’s Figure 3 depicts one embodiment:

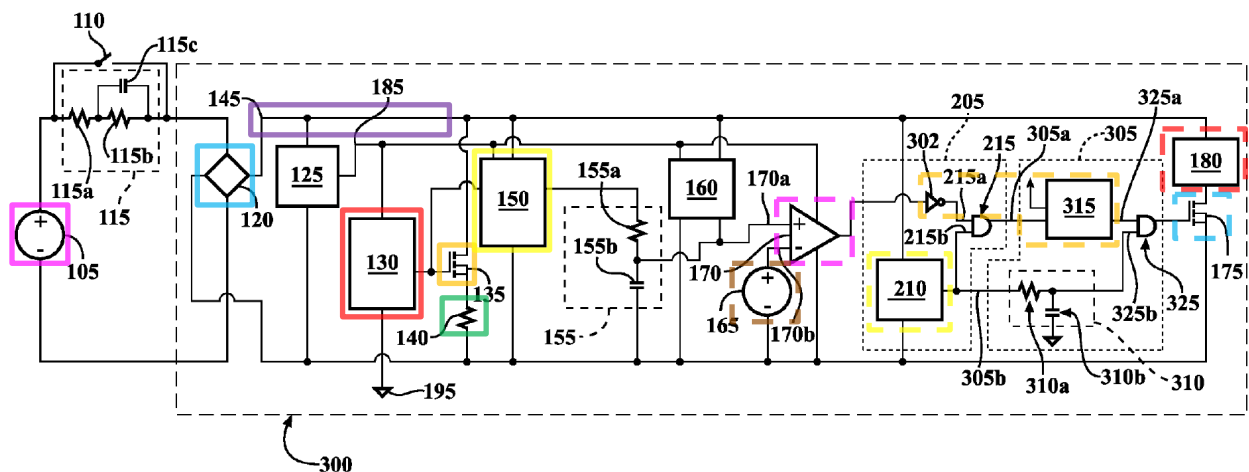


FIG. 3

EX1006, Fig.3; EX1002, ¶46. Here, power input 105 (solid-pink) delivers AC line power to current limiting circuit 300, which includes rectifier 120 (solid-blue) that rectifies the AC power “to a DC wave.” EX1006, ¶¶[0015], [0020], [0041]; EX1002, ¶46. This DC power is provided to device power rail 145 (purple) that connects to main load 180 (dotted-red), which “may be an LED-based light.” EX1006, ¶¶[0016], [0037]; EX1002, ¶46.

Load switch 175 (dotted-blue) controls whether current may flow from rectifier 120 and device power rail 145 through main load 180. EX1006, ¶¶[0010], [0045]; EX1002, ¶47. In a “fault configuration” where power input 105 and the current limiting circuit are connected “through a subject, for example, a person’s body,” load switch 175 “remains off” to prevent current flow through main load 180, “thereby maintaining the current flowing through the subject at a low and safe level.” EX1006, ¶¶[0013], [0010], [0035]-[0036], [0045]; EX1002, ¶47. “For example, a maximum current that can pass through an electrical load simulating the human body may be provided by safety standards promulgated by nationally recognized testing labs.” EX1006, ¶[0023]; EX1002, ¶47. By contrast, in a “normal circuit configuration” where power input 105 and the current limiting circuit are “connected directly,” load switch 175 remains closed, allowing main load 180 to remain powered on. EX1006, ¶¶[0013], [0010], [0035]-[0036], [0045]; EX1002, ¶47.

Ivey345's current limiting circuit includes auxiliary power supply 125, which is directly powered by rectifier 120 over device power rail 145 and provides, e.g., a standard 5V digital supply voltage; and oscillator 130 (solid-red), which is powered by auxiliary power supply 125. EX1006, ¶¶[0016]-[0019]; EX1002, ¶48. “[O]scillator 130 may be configured as a harmonic-type oscillator or a relaxation-type oscillator, a crystal oscillator, a ring oscillator,... or any other type of oscillator.” EX1006, ¶[0019]; EX1002, ¶48.

Oscillator 130's output is “electrically connected to an input of [a] test load switch 135 [(solid-orange)], such that the test load switch 135 is controlled by the oscillator 130.” EX1006, ¶¶[0021]-[0022], [0024]; EX1002, ¶49. Test load switch 135 is connected to device power rail 145 and Z test load 140 (solid-green) such that, while test load switch 135 is closed by oscillator 130's output, current is permitted to flow from device power rail 145 through Z test load 140. *Id.*

An auxiliary-powered detector 150 (solid-yellow), which also receives oscillator 130's clock signal and thus operates synchronously with test load switch 135's activation, “detect[s] a variation in the current draw or voltage across the device power rail 145 due to the oscillating change in the current going through the Z test load 140” and “output[s] a signal in response to a change in the current of the Z test load 140.” EX1006, ¶¶[0024]-[0027]; EX1002, ¶50. Detector 150's output signal “decreases as the variation in the device power rail 145 increases” (fault

configuration) and “increases as the variation in the device power rail 145 decreases” (normal configuration). EX1006, ¶¶[0024]-[0027], [0010]; EX1002, ¶50.

Detector 150’s output signal is then sent to the non-inverting input of an auxiliary-powered comparator 170 (dotted-pink). EX1006, ¶¶[0028]-[0029], Fig.3; EX1002, ¶51. Comparator 170 also receives the output of detection threshold signal source 165 (dotted-brown) at comparator 170’s inverting input, compares these two inputs, “and produces an output relating to the comparison.” EX1006, ¶[0030], Fig.3; EX1002, ¶51. Specifically, if detector 150’s output signal is lower than the threshold signal (fault configuration), comparator 170 outputs a “low” signal, and vice versa. EX1006, ¶¶[0030]-[0032]; EX1002, ¶51.

Comparator 170’s output is inverted by logic inverter 302 and then eventually sent to main load shut-off latch 315 (together in dotted-orange), which “may be constructed from an electrical flip-flop” and, although not depicted in Figure 3, may be synchronized with oscillator 130’s clock signal. EX1006, ¶¶[0041]-[0043]; EX1002, ¶52. Before reaching latch 315, however, the inverted comparator output is first inputted into detection logic circuit 215—an AND gate, which receives its second input from detection validation timer 210 (dotted-yellow). EX1006, ¶¶[0040]-[0041]; EX1002, ¶52. Timer 210 “outputs a ‘low’ signal initially and outputs a ‘high’ signal after an amount of time has lapsed.” EX1006, ¶[0038]; EX1002, ¶52. Thereafter, detection logic circuit 215 passes the inverted comparator

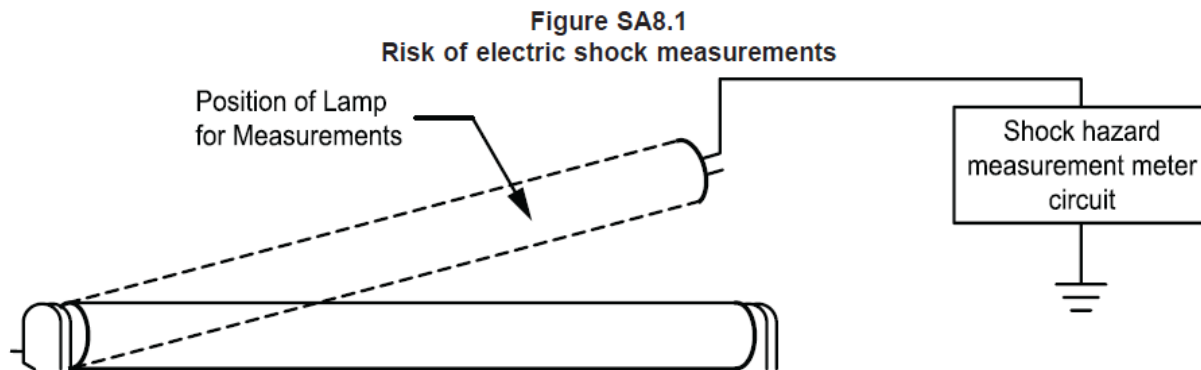
output into latch 315 to control whether latch 315 “should accept a state change.”

EX1006, ¶¶[0044]-[0045], [0039]-[0041]; EX1002, ¶52.

The output of latch 315 is connected to main load detection logic circuit 325—another AND gate, which is located at load switch 175’s input. EX1006, ¶¶[0035]-[0036], [0045]-[0046], [0010]; EX1002, ¶53. Initially, “main load shut-off latch 315 starts at power-up in the ‘on’ state, which would normally energize the main load 180. However, the output of main load logic detection circuit 325 is initially off,” because main load logic detection circuit 325 receives its second input from timer 210. EX1006, ¶[0045]; EX1002, ¶53. Such ensures at startup that “no subject is detected in the electrical circuit” for a “detection valid time” before load switch 175 is allowed to turn on. EX1006, ¶¶[0045], [0038]-[0039]; EX1002, ¶53. If a normal configuration is maintained thereafter, then main load 180 will be energized, as latch 315 will receive a low inverted comparator output signal that will cause latch 315 to continue in the “on” state and pass a high output to load switch 175 through main load logic detection circuit 325. EX1006, ¶¶[0045]-[0046], [0030]-[0032]; EX1002, ¶53. If a fault configuration is detected at any time, however, latch 315 will instead receive a high inverted comparator output signal and thus change to an off state, thereby “latching a low output” and “disabling” load switch 175 until power is “removed... and reapplied.” EX1006, ¶¶[0044]-[0046], [0041], [0030]-[0032]; EX1002, ¶53.

3. *UL1993*

UL1993 is a consumer safety standard for LED tube lamps. *See* EX1007, 1; EX1001, 51:10-12; EX1002, ¶54; *see also, e.g.,* EX1032, 6:21-25. Regarding the “[r]isk of electric shock [during] relamping,” UL1993 mandates that leakage current “shall not exceed 5 M.I.U[.]” when one end of the tube is powered while the other end is “connected to [a] shock hazard measurement meter circuit and, in turn, to earth ground as shown in Figure SA8.1[:.]”



EX1007, 92-93; EX1001, 51:10-12; EX1002, ¶54.

4. *Motivation to Combine*

Ivey813 describes an “LED light tube” that is or obviously would have been mains line powered. EX1005, 2:51-56; §VII.A.1; EX1002, ¶56. And Ivey345 teaches improving “LED-based lights[] and other line-powered electrical devices” by implementing a “current limiting circuit” within such lights for “protecting a person from electrical shock” during relamping. EX1006, ¶¶[0002], [0004]-[0005];

EX1002, ¶56. Thus, Ivey345 expressly teaches combining Ivey345's current limiting circuit into a line-powered LED-based light, such as Ivey813's mains-line-powered LED tube, and therefore contains an express teaching, suggestion, and motivation to combine the two references. EX1002, ¶56.

Such modification also improves user safety. As Ivey345 states, LED-based lights and other line-powered devices carry certain "drawbacks," namely that a subject user may be electrically shocked during relamping by contacting the bulb's "return terminal" while the bulb's "power terminal" is connected. EX1006, ¶¶[0004]-[0005], [0013]; EX1002, ¶57; *accord* EX1012, 4. Such a risk of shock is present in Ivey813's LED-based light tube when mains line powered. *See* EX1012, 4; EX1005, 5:33-39; §VII.A.1; EX1002, ¶57. Ivey345, however, provides a solution by disclosing a "current limiting circuit" that detects whether the above fault configuration is present and, when such is detected, prevents the LEDs in the LED-based light bulb from being energized and thus the user from being shocked. EX1006, ¶¶[0010], [0037]; EX1002, ¶57. Given such teachings, a POSITA would have thus been motivated to modify the line-powered version of Ivey813's LED-based light tube by adding Ivey345's current limiting circuit to power converter 36, because doing so would have enabled power converter 36 to additionally "convert the power received through the fixture" to "a low and safe level" when a fault

configuration occurs, thereby improving user safety during relamping. *See* EX1005, 5:33-35; EX1006, ¶¶[0010], [0004]-[0005]; EX1002, ¶57.

Regarding this “low and safe level,” Ivey345 further teaches that its current limiting circuit allows current to periodically flow despite a fault configuration, but such current is “less than a maximum safe current to avoid harm to the subject. For example, a maximum current that can pass through an electrical load simulating the human body may be provided by safety standards promulgated by nationally recognized testing labs.” EX1006, ¶[0023]; EX1002, ¶58. Such “safety standards” that a POSITA would have been aware of for practicing these teachings include UL1993’s “5 M.I.U[.]” limit for leakage current during relamping. EX1007, 92; EX1001, 51:10-12; EX1002, ¶58. Even setting aside Ivey345’s explicit suggestion to turn to a safety standard like UL1993, a POSITA would have nevertheless been motivated to limit the fault-configuration current draw to UL1993’s 5MIU limit for compliance and safety purposes. EX1002, ¶58.

5. *The Resulting Ivey-UL1993 Combination*

So modified, the combination of Ivey813, Ivey345, and UL1993 (the Ivey-UL1993 Combination) comprises Ivey813’s “LED-based light tube,” which is mains line powered by fixture 11 (Ivey345’s power source 105) and utilizes Ivey345’s current limiting circuit as an additional circuit within power converter 36 to control whether current may flow from power converter 36’s rectifier circuit (Ivey345’s

rectifier 120) through the tube's LEDs 18 (Ivey345's main load 180) based on the detected current draw or voltage across the tube (Ivey345's device power rail 145). *See* EX1005, 5:31-40; EX1006, ¶¶[0024]-[0027], [0010]; EX1002, ¶59. If such detection indicates a fault configuration, current through the tube is limited to a standard-compliant "low and safe level," e.g., <5MIU. *See* EX1006, ¶¶[0010], [0023]; EX1001, 51:10-12, 2:32-37; EX1007, 92; EX1002, ¶59.

6. *Element-by-Element Analysis*

(a) **Limitation [18pre]**

To the extent limiting, the Ivey-UL1993 Combination utilizes, within power converter 36 of Ivey813's LED-based light tube, Ivey345's current limiting circuit that detects during relamping whether a subject user is making contact with the tube's return terminal while the tube's power terminal is connected to fixture 11 (Ivey345's power source 105 (solid-pink)) (claimed "lamp socket"):

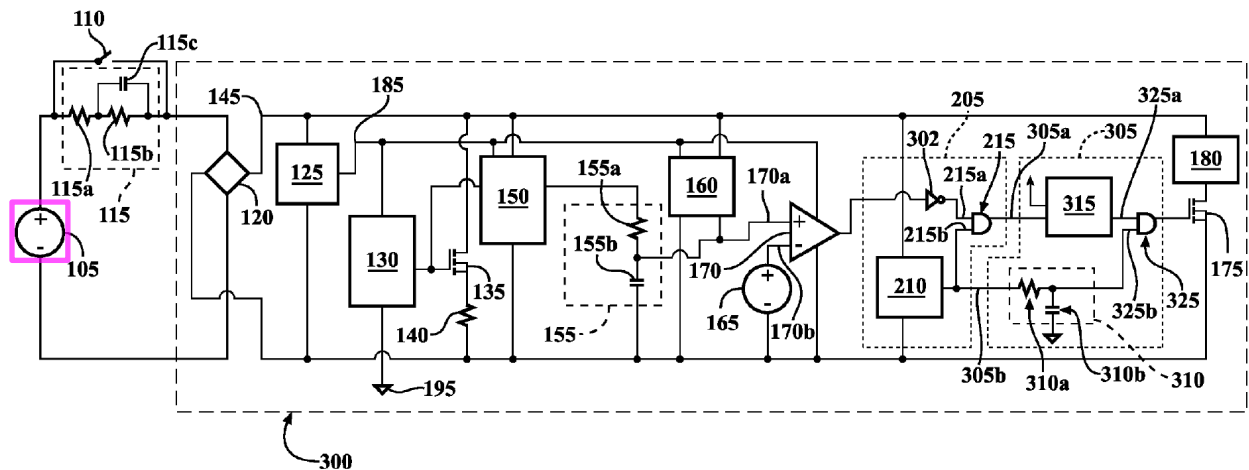


FIG. 3

EX1005, 3:50-56, 5:33-35; EX1006, Fig.3, ¶¶[0010], [0004]-[0005]; §VII.A.5; EX1002, ¶60. If such is detected, the current limiting circuit maintain current “at a low and safe level,” and thus performs the claimed “detection method... for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket.” EX1006, ¶¶[0010], [0004]-[0005]; EX1002, ¶60.

(b) Limitation [18a]

Ivey345’s current limiting circuit includes oscillator 130 (solid-red), which outputs a clock signal (“pulse signal”) that oscillates high and low, e.g., “a digital, continuous time output, a varying sinusoidal output, or another type of output”:

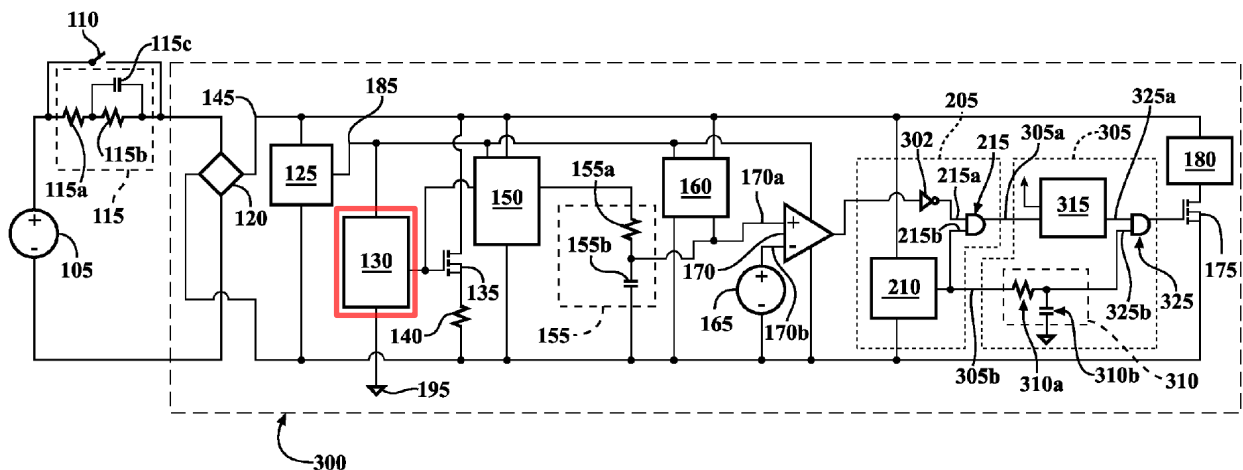
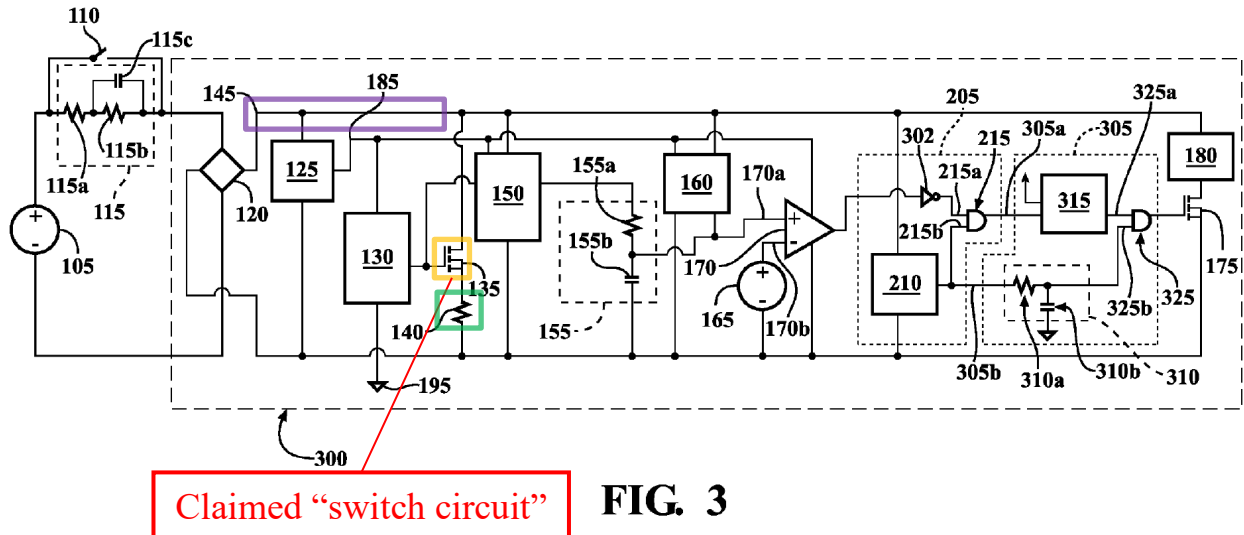


FIG. 3

EX1006, Fig.3, ¶¶[0019], [0044]; EX1002, ¶61; *see also* EX1001, 41:44-48, 41:59-64.

(c) Limitation [18b]

Ivey345's current limiting circuit includes test load switch 135 (solid-orange), which meets the claimed "switch circuit":



EX1006, Fig.3, ¶¶[0010], [0021]-[0023]; EX1002, ¶62. Specifically, test load switch 135's gate receives oscillator 130's clock signal ("receiving the pulse signal by a switch circuit"), causing test load switch 135 to open and close as the clock signal oscillates low and high, respectively. EX1006, ¶¶[0020]-[0022], [0024], Fig.3; EX1002, ¶62. Test load switch 135's drain and source are connected respectively to device power rail 145 (purple) ("coupled on a power loop of the LED tube lamp") and Z test load 140 (solid green), the latter connecting to ground. EX1006, ¶¶[0022]-[0024], Fig.3; EX1002, ¶62. Thus, while test load switch 135 is closed by oscillator 130's high output ("switch circuit is conducted during a pulse-on period of the pulse signal"), current is permitted to flow from device power rail

145 through Z test load 140 to ground (“to cause the power loop to be conductive”).

EX1006, ¶¶[0022]-[0024], Fig.3; EX1002, ¶62.

As a first alternative, test load switch 135 also the claimed “switch circuit” because, in a normal configuration, test load switch 135’s operation causes current to flow through LEDs. Specifically, Ivey345 teaches that the current limiting circuit further includes detector 150 (solid-yellow), which also receives oscillator 130’s clock signal “to synchronize the detector 150 with the activation of the test load switch 135”:

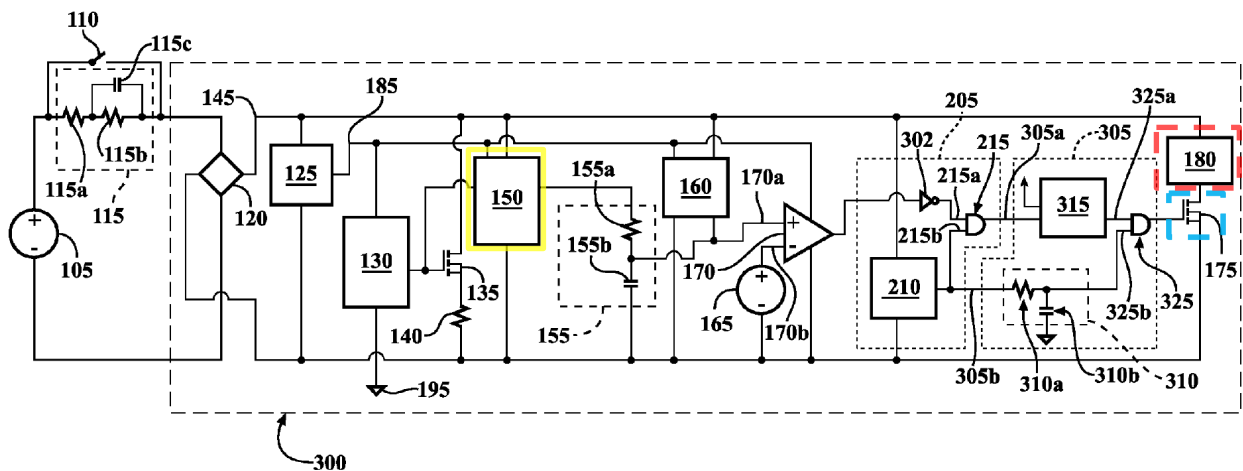


FIG. 3

EX1006, Fig.3, ¶[0024]; EX1002, ¶63. While the clock signal oscillates high, test load switch 135 not only conducts (“receiving the pulse signal by a switch circuit coupled on a power loop of the LED tube lamp, wherein the switch circuit is conducted during a pulse-on period of the pulse signal”), but also allows detector 150 to “detect a variation in the current draw or voltage across the device power rail

145 due to the oscillating change in the current going through the Z test load 140.” EX1006, ¶[0024]; EX1002, ¶63. This detected variation is then used to detect whether a normal configuration exists, and, if such is detected, load switch 175 (dotted-blue) will remain on, allowing current to flow from device power rail 145 through main load 180 (dotted-red), i.e., the LEDs (“to cause the power loop to be conductive”). EX1006, ¶¶[0010], [0024]-[0027], [0030]-[0032], [0037], [0044]-[0045]; EX1002, ¶63; *see also infra* §§VII.A.6(d)-VII.A.6(g).

As a second alternative, test load switch 135 and load switch 175 together also meet the claimed “switch circuit”:

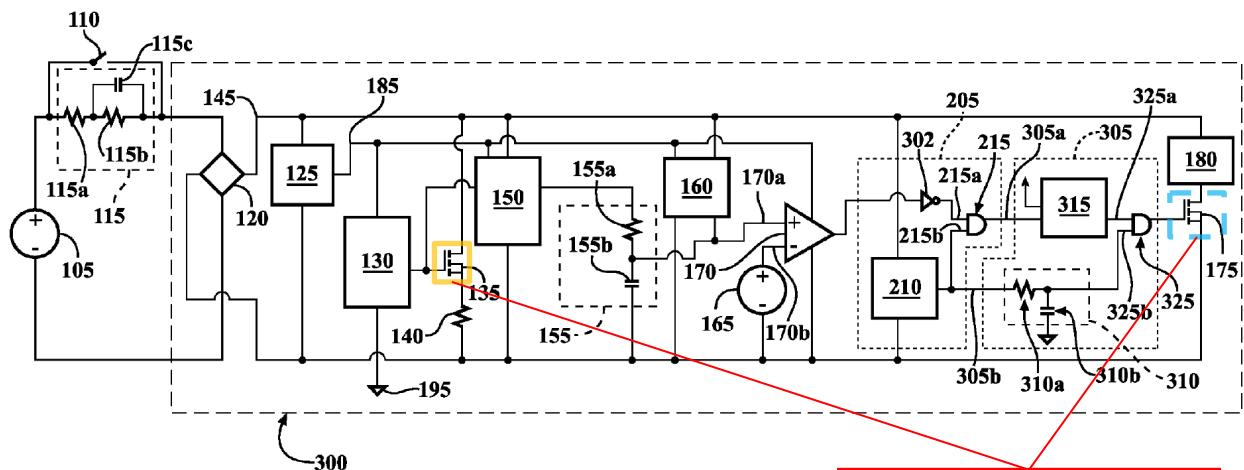


FIG. 3

Together, the claimed
“switch circuit”

EX1006, ¶[0024]; EX1002, ¶64. Specifically, test load switch 135 receives oscillator 130’s clock signal (“receiving the pulse signal by a switch circuit coupled on a power loop of the LED tube lamp”). EX1006, ¶¶[0022]-[0024]; EX1002, ¶64.

As explained, such allows detection of whether a normal configuration exists, and if such is detected, load switch 175 will remain on (“wherein the switch circuit is conducted during a pulse-on period of the pulse signal”), allowing current to flow from device power rail 145 through the LEDs (“to cause the power loop to be conductive”). EX1006, ¶¶[0010], [0024]-[0027], [0030]-[0032], [0037], [0044]-[0045]; EX1002, ¶64; *see also infra* §§VII.A.6(d)-VII.A.6(f).

Regarding this second alternative, a POSITA would have understood that a plurality of separate transistor switches that perform the claimed functions would together meet the claimed “switch circuit.” EX1001, 12:10-34; EX1002, ¶65; *see also, e.g.*, EX1010⁶ (showing numerous “2 N-Channel (Dual)” FET products—i.e., two n-type MOSFETs formed on one integrated *circuit*—were commercially available by the ECPD); EX1011⁷ (datasheet for Fairchild Semiconductor FDG6303N—the first product listed in EX1010).

(d) Limitation [18c]

Ivey345’s detector 150 receives oscillator 130’s clock signal, more precisely, to synchronize detector 150’s operation with test load switch 135’s activation. EX1006, ¶[0024]; EX1002, ¶66. While test load switch 135 is closed by oscillator

⁶ See EX1031, pp.22-23.

⁷ See EX1031, pp.46-51.

130's clock signal, detector 150 "detect[s]" a variation in the current draw or voltage across the device power rail 145" ("detecting a sampling signal on the power loop") based on the current now passing through Z test load 140, and outputs a signal representative of the detected variation. EX1006, ¶¶[0024]-[0027], claim 14; EX1002, ¶66.

(e) Limitation [18d]

When Ivey345's detector 150 detects either an increase or decrease in the variation across device power rail 145 caused by a fault or normal configuration, respectively, detector 150 outputs a correspondingly "decrease[d]" or "increase[d]" signal to comparator 170 (dotted-pink):

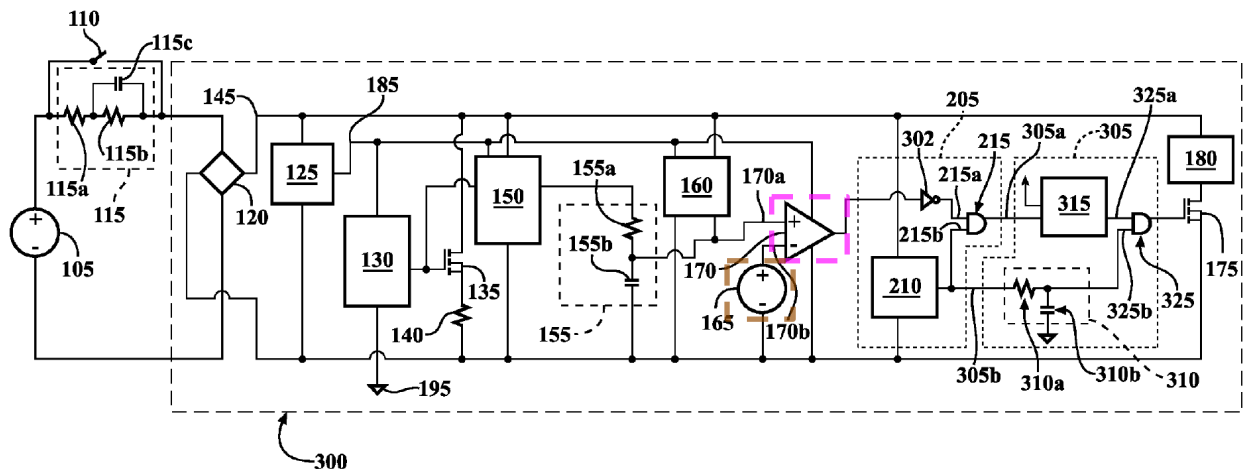


FIG. 3

EX1006, Fig.3, ¶¶[0024]-[0026], [0010], [0028]-[0029], [0034]; EX1002, ¶67. Comparator 170 compares detector 150's output signal to a threshold signal from detection threshold signal source 165 (dotted-brown) ("comparing the sampling

signal with a predefined signal”) and “produces an output relating to the comparison.” EX1006, ¶¶[0030]-[0032]; EX1002, ¶67.

(f) Limitation [18e]

When the output signal of Ivey345’s detector 150 is lower than the threshold signal (fault configuration) (“when a signal level of the sampling signal is smaller than the predefined signal”), comparator 170 outputs a “low” signal that ultimately causes load switch 175 to “remain[] off,” thereby maintaining current “at a low and safe level,” e.g., <5MIU. EX1006, ¶¶[0010], [0023], [0030]-[0032], [0044]-[0045]; §VII.A.5; EX1002, ¶68.

(g) Claim 19

When Ivey345 detector 150’s output signal is higher than the threshold signal (normal configuration) (“when the signal level of the sampling signal is greater than or equal to the predefined signal”), comparator 170 outputs a “high” signal that ultimately causes load switch 175 to remain on, allowing current to flow from device power rail 145 through the LEDs (“conducting the power loop”). EX1006, ¶¶[0010], [0030]-[0032], [0041], [0044]-[0045]; EX1002, ¶69.

(h) Limitation [10pre]

To the extent limiting, Ivey813’s LED-based light tube is mains line powered and thus bypasses a ballast. EX1005, 2:50-56, 5:33-35; EX1006, ¶¶[0010], [0004]-[0005]; §VII.A.5; EX1002, ¶70.

(i) Limitation [10a]

Ivey813's tube includes elongate housing 12. EX1005, 2:57-60; EX1002, ¶71.

(j) Limitation [10b]

Ivey813's housing 12 includes two end caps 20 attached at opposing ends. EX1005, 1:37-39, 1:50-51; EX1002, ¶72. Each end cap 20 includes pins 32 (“external connection terminals”), which may electrically connect the tube to fixture 11 and thus receive mains AC power (“external driving signal”). EX1005, 5:1-16; EX1006, ¶¶[0010], [0004]-[0005]; §VII.A.5; EX1002, ¶72.

(k) Limitation [10c]

Within Ivey813's housing 12 is circuit board 14, on which LEDs 18 are mounted (“LED module”). EX1005, 2:13-17, 3:27-37, 3:63-67; EX1006, ¶¶[0016], [0037]; §VII.A.5; EX1002, ¶73. LEDs 18 produce light and are powered by DC power from power converter 36's rectifier circuit (Ivey345's rectifier 120 (solid-blue)), which rectifies mains AC power:

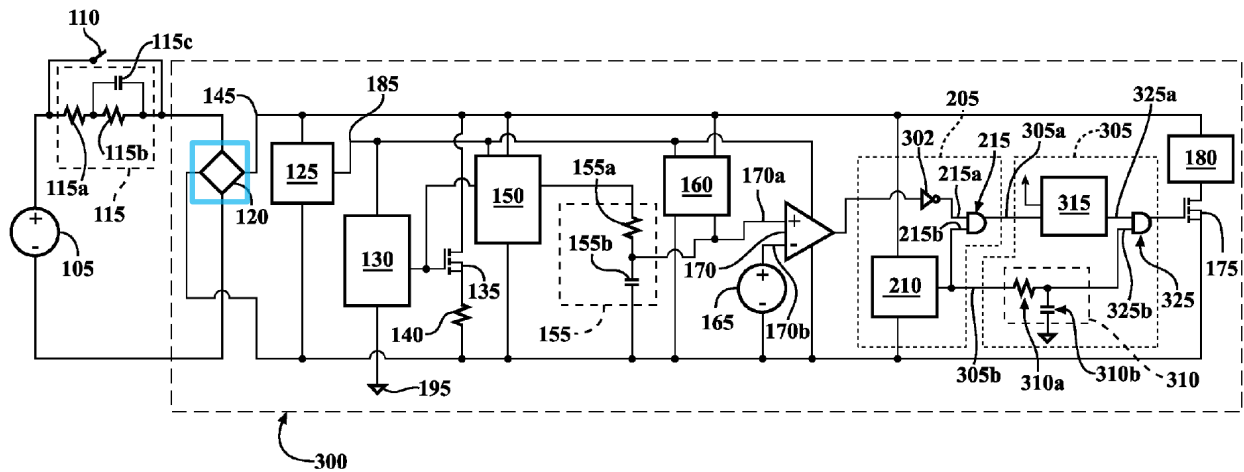


FIG. 3

EX1006, Fig.3, ¶¶[0015]-[0016], [0037]; EX1005, 3:23-37, 3:43-47, 5:33-35; §VII.A.5; EX1002, ¶73.

(I) Limitation [10d]

Ivey345’s current limiting circuit (“installation detection module”) includes various components coupled to the tube’s device power rail 145, such as detector 150 and comparator 170 (“coupled on a power loop of the LED tube lamp”). *See* §§VII.A.6(b)-VII.A.6(d); EX1002, ¶74. Detector 150 detects, e.g., current variation across device power rail 145 (“configured to detect a transient current on the power loop”) and outputs a representative signal, which comparator 170 compares to a threshold signal (“compare the transient current with a predefined signal”). *See* §VII.A.6(e); EX1002, ¶74.

(m) Limitation [10e]

When the representative signal is lower than the threshold signal, the current limiting circuit maintains current flow at a safe level—e.g., <5MIU—by signaling load switch 175 to remain off. *See* §VII.A.6(f); EX1002, ¶75.

(n) Claim 11

Detector 150, comparator 170, and Z test load 140 altogether form the claimed “detection determining circuit.” EX1002, ¶76. *Compare* EX1006, Fig.3 (below), *with, e.g.,* EX1001, Fig.15K, 50:3-54.

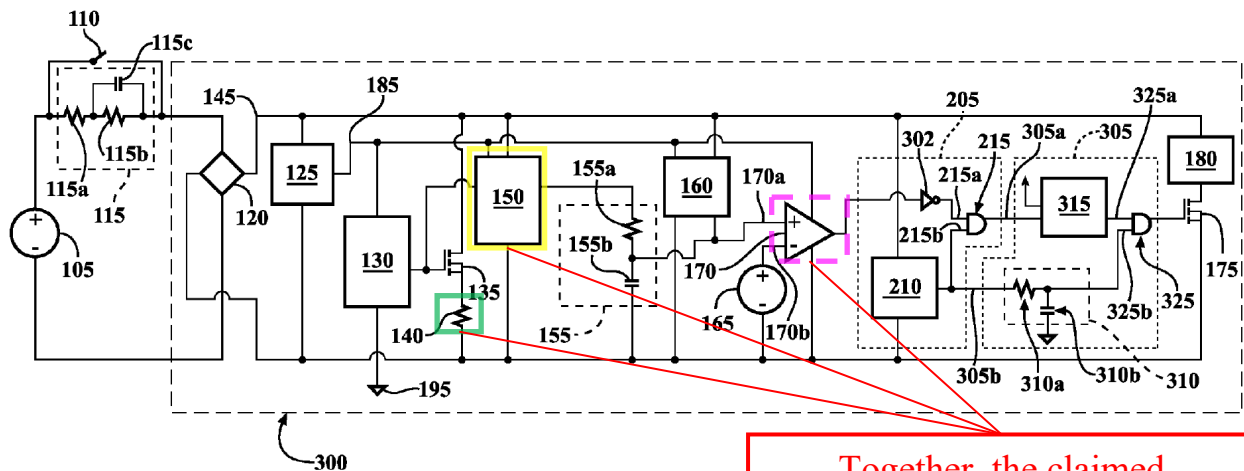


FIG. 3

Together, the claimed
“detection determining circuit”

Specifically, detector 150 detects the variation across device power rail 145 (“configured to detect the transient current”) and outputs a representative signal to comparator 170, which compares detector 150’s output signal to the threshold signal (“compare the transient current with the predefined signal”) and outputs either a low or high signal depending on this comparison (“output a high level signal or a low

level signal according to a comparison result”). *See* §§VII.A.6(d)-VII.A.6(g); EX1002, ¶76.

(o) Claim 12

Ivey345’s current limiting circuit includes oscillator 130 (“detection pulse generating module”), which outputs an oscillating clock signal. *See* §VII.A.6(b); EX1002, ¶77. While the clock signal oscillates high, detector 150 detects the variation across the device power rail 145. *See* §VII.A.6(c); EX1002, ¶77.

(p) Claim 16

For similar reasons discussed in §VII.A.6(c), test load switch 135, alone or in combination with load switch 175, meets the claimed “switch circuit.”

Specifically, test load switch 135 connects to Z test load 140 and oscillator 130. *See* §VII.A.6(c); EX1002, ¶79. Test load switch 135 closes while the clock signal oscillates high (“maintain[s] a conductive state during the pulse-on period of the pulse signal”) and thus, alone, meets the claimed “switch circuit.” *See* §VII.A.6(c); EX1002, ¶79.

As a first and second alternative, while test load switch 135 is closed (“during the pulse-on period of the pulse signal”) and a normal configuration is detected via detector 150’s detection of current or voltage variation across device power rail 145, load switch 175 also remains closed (“maintain[s] a conductive state”), allowing current to flow from device power rail 145 through the LEDs. *See* §VII.A.6(c);

EX1002, ¶80. By causing load switch 175 to remain closed accordingly, test load switch 135 alone (first alternative) or in combination with load switch 175 (second alternative) meets the claimed “switch circuit.” See §VII.A.6(c); EX1002, ¶80.

As a third alternative, load switch 175 alone meets the claimed “switch circuit”:

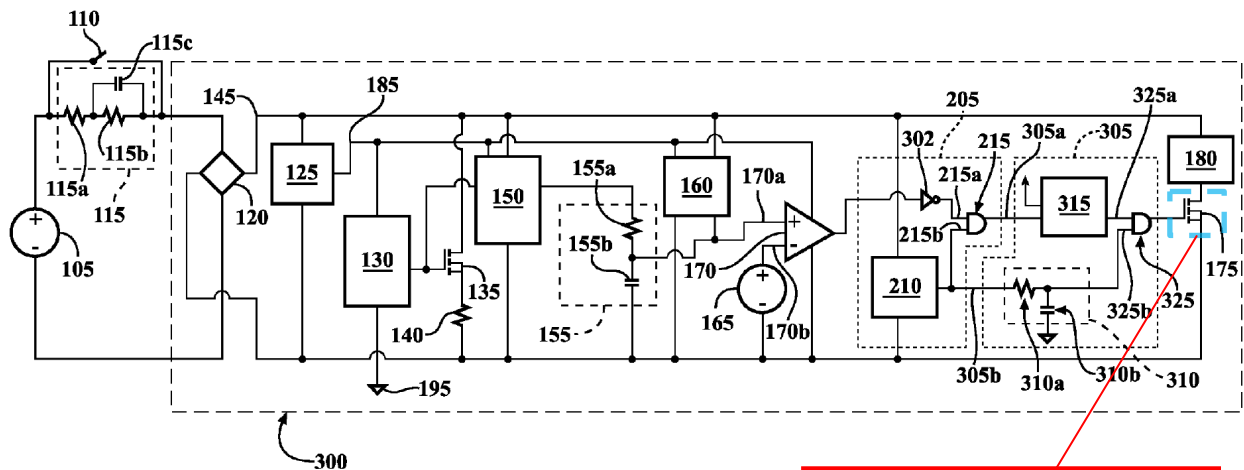


FIG. 3

Claimed “switch circuit”

EX1006, Fig.3; EX1002, ¶81. Specifically, load switch 175’s activation is determined by detector 150’s detection, which is synchronized by oscillator 130’s clock signal. See §§VII.A.6(d)-VII.A.6(g); EX1002, ¶81. Thus, while oscillator 130’s clock signal oscillates high (“during the pulse-on period of the pulse signal”) and a normal configuration is detected, load switch 175 remains closed (“maintain a conductive state”). See §§VII.A.6(d)-VII.A.6(g); EX1002, ¶81.

(q) **Claim 17**

Ivey345's current limiting circuit also includes “logic inverter 302” and “main load shut-off latch 315” (together in dotted-orange), which altogether form the claimed “detection result latching circuit”:

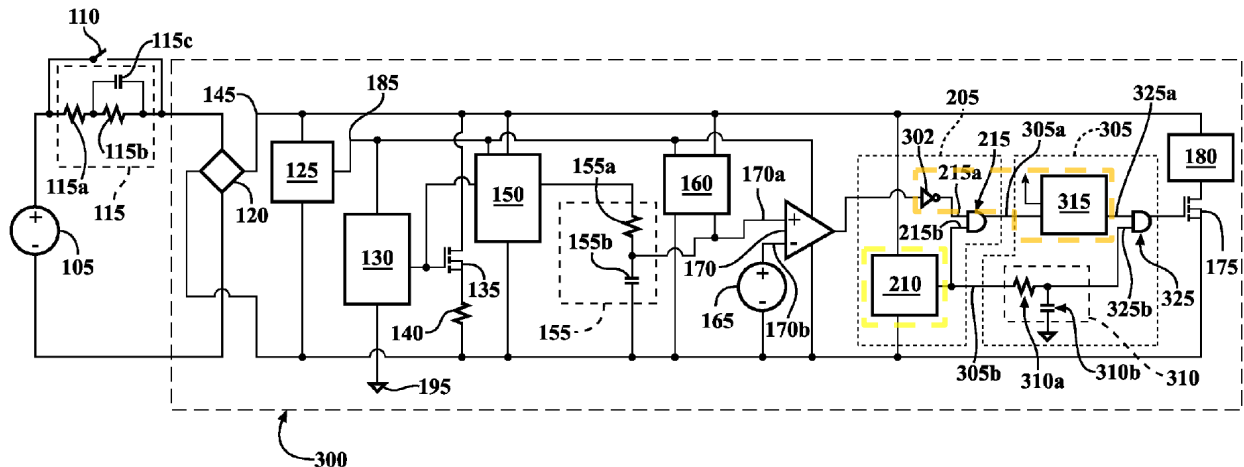


FIG. 3

EX1006, Fig.3, ¶[0041]; EX1002, ¶82; *see also* EX1001, 12:10-34. As Ivey345 teaches, comparator 170's output does not go directly to load switch 175, but is instead inverted by logic inverter 302 and then eventually inputted into latch 315 (“coupled to the detection determining circuit”). EX1006, Fig.3, ¶[0039]-[0041], [0043]; EX1002, ¶82. Though not depicted, latch 315 also receives—and thus synchronizes its operation with—oscillator 130's clock signal (“coupled to... the detection pulse generating module”). EX1006, ¶[0043]; EX1002, ¶82. Latch 315's output passes through “main load detection logic circuit 325”—an AND gate—into the input of load switch 175 (EX1006, Fig.3, ¶[0045]-[0046]), which here, alone or

in combination with test load switch 135, forms the claimed “switch circuit” (“coupled to... the switch circuit”) (*see* §VII.A.6(p)). EX1002, ¶82.

Latch 315 “starts at power-up in the ‘on’ state” and thus initially outputs a high signal to load switch 175 through main load detection logic circuit 325. EX1006, ¶¶[0045]-[0046]; EX1002, ¶83. If the comparator 170’s output signal to logic inverter 302 is likewise high (normal configuration), latch 315’s output to load switch 175 will remain high (“the high level signal... is provided to the switch circuit through the detection result latching circuit”). EX1006, ¶[0045]; EX1002, ¶83. However, if comparator 170’s output signal logic to logic inverter 302 becomes low (fault configuration), latch 315 too will output a low signal to load switch 175, but will also “prevent the activation of the load switch 175... until the device is disconnected and power is reapplied” (“the low level signal is provided to the switch circuit through the detection result latching circuit”). EX1006, ¶¶[0044]-[0045]; EX1002, ¶83.

Alternatively, should the *Maxlite* Court’s construction of “detection result latching circuit” apply (*see* EX1025, 26-28; §VI.C.1), Ivey345 teaches more specifically that latch 315 receives oscillator 130’s clock signal either directly from oscillator 130 or indirectly via another synchronized device, e.g., detection validation timer 210 (dotted-yellow). EX1006, ¶¶[0043], [0039]; EX1002, ¶84. In other words, Ivey345 teaches that oscillator 130’s clock signal is outputted to each

synchronized device either individually using parallel interconnections or serially using “daisy chaining”—a commonly used circuit design technique for synchronizing devices where a first device (e.g., timer 210) receives the clock signal and outputs the clock signal to a second device (e.g., latch 315), which may do the same to a third device, and so forth to establish a serial daisy chain cascade that synchronizes each connected device. EX1006, ¶¶[0043], [0039]; EX1002, ¶84; *see also, e.g.*, EX1014, 5:36-56, Fig.2. And as commonly known, daisy chaining provides numerous advantages over parallel interconnections, including “utilizing fewer and shorter interconnections [to] make[] the overall implementation less vulnerable to undesirable effects, such as propagation delay and crosstalk,” thereby “allow[ing] the devices to be operated at higher speeds,” while also “reduc[ing] complexity [to] enable[] a subsystem containing the devices to be implemented in a smaller area thus allowing the subsystem to occupy a smaller footprint.” EX1014, 2:29-54; EX1002, ¶84.

To gain such advantages, a POSITA would have recognized that, while oscillator 130’s clock signal could be at least partially daisy chained as disclosed in Ivey345 by connecting oscillator 130 to timer 210 to latch 315 (EX1006, ¶¶[0039], [0043]), a more preferable configuration would have been to fully daisy chain the devices to be synchronized—e.g., by then also connecting latch 315 to test load switch 135 to detector 150 (*see id.*, ¶¶[0021], [0024], [0039], [0043])—to maximize

such benefits. EX1002, ¶85. Doing so, latch 315 therefore receives and outputs oscillator 130's clock signal to test load switch 135.⁸ EX1002, ¶85. And while oscillator 130's clock signal oscillates high or low, this output from latch 315 to test load switch 135 would likewise oscillate high or low, respectively. *See* EX1025, 26-28 (“reverses its signal level when the... ***pulse signal from the detection pulse generating module*** is applied”); EX1002, ¶85. At the same time, logic inverter 302 receives comparator 170's output and sends the reverse signal to latch 315 to control whether latch 315 should latch a “high” or “low” output. EX1025, 26-28 (“reverses its signal level when the ***detected result***... is applied and ***maintains its signal level based on the detected result***”); EX1006, ¶¶[0043]-[0046], [0030]-[0032]; EX1002, ¶85.

As a further alternative, should the claim conjunctively require each of the recited “pulse signal,” “high level signal,” and “low level signal” to be “provided to the switch circuit through the detection result latching circuit” regardless of the *Maxlite* Court's construction, test load switch 135 and load switch 175 would together form the claimed “switch circuit.” *See* §VII.A.6(p); EX1002, ¶86. As

⁸ Should a mapping of “switch circuit” be required here, test load switch 135 alone or together with load switch 175 would thus form the claimed “switch circuit.” *See* §VI.A.6(p); EX1002, ¶86 n.3.

explained above, test load switch 135 receives the clock signal through latch 315 via daisy-chaining, while load switch 175 receives a high/low signal from latch 315 when comparator 170's signal is high/low, respectively. EX1002, ¶86.

(r) Limitations [23pre]-[23c]

See §§VII.A.6(h)-VII.A.6(k).

(s) Limitation [23d]

See §VII.A.6(l). The detected variation across device power rail 145 is “a sampling signal on the power loop” as claimed. EX1002, ¶88.

(t) Limitation [23e]

Ivey345's current limiting circuit “maintain[s] the current flowing through the subject at a low and safe level” when a fault configuration occurs, such as “if the power terminal is connected” but the subject user contacts the “return terminal... that has not yet been mated,... completing the circuit from the return terminal to ground” (“a leakage loop”). EX1006, ¶¶[0010], [0005], [0013]-[0014]; EX1002, ¶89.

(u) Limitation [23f]

Oscillator 130, detector 150, comparator 170, threshold signal source 165, and other components of Ivey345's current limiting circuit are powered by “auxiliary power supply 125,” which is directly powered by rectifier 120 over device power rail 145. EX1006, ¶¶[0016]-[0019], [0024], [0029], [0031]; EX1002, ¶90. The

current limiting circuit is powered accordingly even when a fault configuration occurs, as in such a situation the current limiting circuit nevertheless receives sufficient power to detect an increased variation across device power rail 145 and to signal load switch 175 to remain off in response, limiting current flow to a safe and low level (“activated by a driving voltage on the leakage loop”). *See* EX1006, ¶¶[0025]-[0026], [0010], [0016]-[0018]; EX1002, ¶90.

(v) Claim 24

Ivey813 states that “[o]ne of the two pins 32 [of end caps 20] can be a ‘dummy pin’ that does not provide an electrical connection.” EX1005, 5:1-7; EX1002, ¶91.

(w) Claim 25

Auxiliary power supply 125 is powered by rectifier 120—and thus Ivey813 fixture 11’s AC power (“the driving voltage is generated based on the external driving signal”)—and powers the various components of the current limiting circuit even when a fault configuration occurs (“when the leakage loop is formed”). *See* EX1006, ¶¶[0015]-[0019], [0024]-[0026], [0029], [0031], [0010]; EX1002, ¶92.

(x) Limitations [26pre]-[26d]

See §VII.A.6(r)-VII.A.6(s).

(y) Limitation [26e]

Ivey345’s current limiting circuit meets the claimed “control module.” As Ivey345 teaches, the current limiting circuit controls whether current may flow from

device power rail 145 through the LEDs by signaling load switch 175 to remain either on or off (“output a control signal for controlling a conduction state of the power loop”). EX1006, ¶¶[0010], [0044]-[0045]; EX1002, ¶94. When detector 150’s representative signal is lower than threshold signal source 165’s threshold signal, the current limiting circuit maintains current flow at a safe level—e.g., <5MIU—by signaling load switch 175 to remain off. EX1006, ¶¶[0010], [0023] [0030]-[0032], [0044]-[0045]; §VII.A.6(f); EX1002, ¶94.

(z) Limitation [26f]

Ivey345's current limiting circuit includes detection validation timer 210 (dotted-yellow):

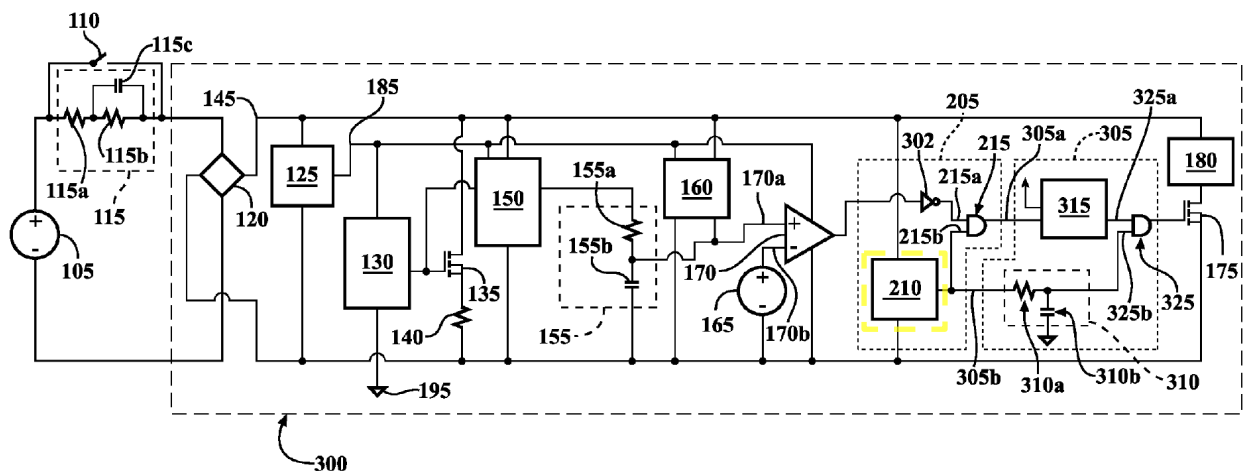


FIG. 3

EX1006, Fig.3; ¶[0039]; EX1002, ¶95. Timer 210 is “a digital counter that outputs a ‘low’ signal initially and outputs a ‘high’ signal after an amount of time has lapsed.” EX1006, ¶[0039]; EX1002, ¶95. Timer 210’s output is received by

detection logic circuit 325—an AND gate—which also receives latch 315’s output, thereby ensuring at startup that “no subject is detected in the electrical circuit” for a “detection valid time” before latch 315 is allowed turn on load switch 175. EX1006, ¶¶[0045], [0038]-[0039]; EX1002, ¶95. Thus, while this initial detection is performed for the detection valid time at startup, a low signal is sent to load switch 175 (“generates the control signal having a first waveform during a detection stage”). EX1006, ¶¶[0044]-[0045], [0038]-[0039]; EX1002, ¶95. If a normal configuration is maintained thereafter, latch 315’s high signal will then be permitted to pass through detection logic circuit 325 to load switch 175, allowing the LEDs to receive power from device power rail 145 and thus operate (“generates the control signal having a second waveform during an operating stage”). EX1006, ¶¶[0044]-[0045], [0038]-[0039], [0010]; EX1002, ¶95.

(aa) Claim 27

See §VII.A.6(q). For the same reasons that Ivey345’s current limiting circuit meets claim 17’s “installation detection module,” the current limiting circuit meets claim 27’s “control module.” EX1002, ¶96.

(bb) Limitations [28pre]-[28c]

See §§VII.A.6(h)-VII.A.6(k).

(cc) Limitation [28d]

See §VII.A.6(l). Additionally, the clock signal from Ivey345’s current limiting circuit’s oscillator 130 controls the activation of both test load switch 135 and load switch 175 (“configured to generate a pulse signal for controlling a conduction state of the power loop”). *See* §VII.A.6(p); EX1002, ¶98. Detector 150 detects the variation across device power rail 145 while the clock signal oscillates high (“configured to... detect a sampling signal on the power loop during a pulse-on time of the pulse signal”). *See* §VII.A.6(o); EX1002, ¶98.

(dd) Limitation [28e]

Oscillator 130 outputs a clock signal with a frequency “for example at or about 1Khz,” which equates to a period of 1ms. EX1006, ¶¶[0019]-[0020]; EX1002, ¶99. Given that such a clock signal oscillates every period between high and low, only a fraction of the clock signal’s 1ms period is high (“setting the pulse-on time less than... 1 millisecond”). EX1002, ¶99. This clock signal allows the current limiting circuit to detect a variation on device power rail 145 and limit current to standard-compliant levels—e.g., <5MIU (*see* §VII.A.6(f))—when a fault configuration is detected. EX1006, ¶¶[0023]-[0024]; EX1002, ¶99.

(ee) Claim 29

Ivey345 teaches that oscillator 130 may generate a “varying sinusoidal output.” EX1006, ¶[0019]; EX1002, ¶100. As a POSITA would have recognized,

such a sinusoidal signal would result in 50% of the period being high and 50% being low—i.e., a 50% duty cycle. *See* EX1015, ¶[0035] (“50% duty cycle... is naturally true of sinusoidal signals”); EX1002, ¶100. Thus, by utilizing the 1ms period sinusoidal signal from Ivey345, the pulse-on time would last 0.5ms. *See* EX1006, ¶¶[0019]-[0020]; EX1002, ¶100.

(ff) Limitations [32pre]-[32c]

See §§VII.A.6(h)-VII.A.6(k).

(gg) Limitation [32d]

See §VII.A.6(cc). By teaching that oscillator 130 outputs “a digital, continuous time output, a varying sinusoidal output, or another type of output” with a specific “oscillation frequency,” Ivey345 thus teaches that oscillator 130 outputs multiple pulses over time. EX1006, ¶¶[0019]-[0020]; EX1002, ¶102. Indeed, Ivey345 teaches that oscillator 130 may be “a ring oscillator” (EX1006, ¶[0019]), which is an oscillator that generates “successive periods” of pulses (EX1016,⁹ 6-7). EX1002, ¶102.

(hh) Limitation [32e]

Oscillator 130’s output oscillates “for example at or about 1 Khz,” while AC mains oscillates at, e.g., “60 Hz.” EX1006, ¶[0020]; EX1002, ¶103. Thus, while

⁹ *See* EX1030, ¶¶45-52 (establishing pre-ECPD public availability).

AC mains oscillates high (“at a non-zero level”), which lasts 8.33ms, 8.33 consecutive pulses occur. EX1002, ¶103.

B. Ground 2: Ivey813, Ivey345, UL1993, and Sadwick Render Obvious Claims 10-12, 16-19, 23-29, and 32

Ground 2 addresses the possibility Ground 1 fails because Ivey345’s test load switch 135 and Z test load 140 are in parallel, not series, with main load 180.

1. Sadwick

Sadwick is directed to a “fluorescent lamp replacement” (“FLR”) for replacing “[c]onventional fluorescent tubes.” EX1008, ¶¶[0004], [0066], [0001]; EX1002, ¶105. The FLR includes “a rectification stage” that “accepts either an AC lines input”—i.e., is type B—“or a ballast output.” EX1008, ¶¶[0066], [0173], [0161]; EX1012, 3-4; EX1002, ¶105; *see also* EX1008, ¶[0061] (incorporating by reference Sadwick454, which discloses an LED tube powered by either a ballast or “AC mains” (EX1017, 4:43-67)). The FLR also includes a “light source” such as one such “made up of LEDs.” EX1008, ¶[0066]; EX1002, ¶105.

Sadwick notes that, during relamping of an FLR, “[a] pin can be exposed and, without protection mechanisms, can shock and injure a user contacting the pin.” EX1008, ¶[0071] (diagram numbering omitted); EX1002, ¶106. Sadwick’s FLR “provid[es] shock hazard protection” to address this “fault hazard condition.”

EX1008, ¶¶[0082], [0073]; EX1002, ¶106. Sadwick’s Figure 14 depicts such “hazard protection circuitry”:

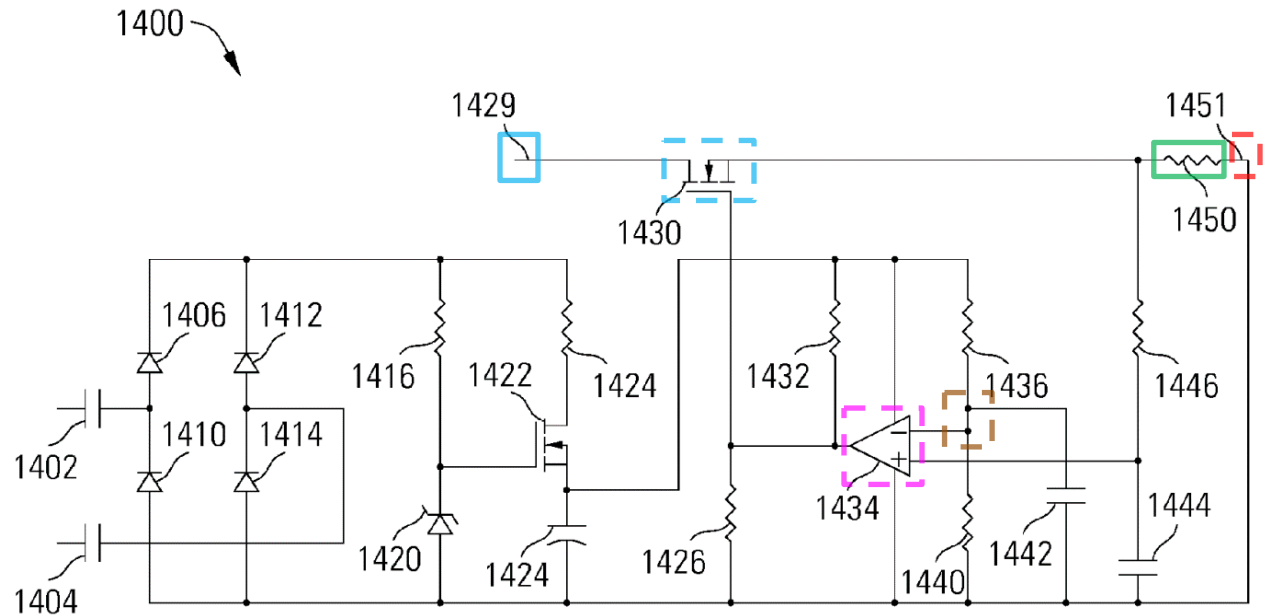


FIG. 14

EX1008, ¶¶[0080], [0082], Fig.14; EX1002, ¶106. As shown, an “input rectification stage of the FLR” is connected to node 1429 (solid-blue). EX1008, ¶[0080]; EX1002, ¶106. The “LED (or OLED or QD) load” is connected to node 1451 (dotted-red). EX1008, ¶[0080]; EX1002, ¶106. Between these nodes is transistor/switch 1430 (dotted-blue) and sense resistor 1450 (solid-green), which are thus “in series with” the FLR’s rectifier and LED load. EX1008, ¶[0080]; EX1002, ¶106.

Sadwick’s hazard protection circuitry detects whether the fault hazard condition above is present by feeding “the voltage across sense resistor 1450” into

“the non-inverting input of [a] comparator 1434” (dotted-pink). EX1008, ¶[0080]; EX1002, ¶107. At the same time, “a reference set point” (dotted-brown) “is fed to the inverting terminal of [the] comparator 1434 such that when the signal from the sense resistor 1450 is larger than the reference set point signal, the comparator 1434 goes high and turns on transistor 1430,” allowing current to flow through the LEDs. EX1008, ¶[0080]; EX1002, ¶107. By contrast, “[i]f the current through the sense resistor 14[5]0 produces too small of a voltage then transistor 1430 is turned off preventing current from flowing and thus limiting and preventing a hazard/shock/leakage current condition from occurring.” EX1008, ¶¶[0080], [0082]; EX1002, ¶107.

Once transistor 1430 is turned off, Sadwick’s hazard protection circuitry causes transistor 1430 to be “complete[ly] turn[ed]-off (i.e., latch[ed] off) until power is cycled... or, as another example, periodically turned back on for a brief moment to see if the hazard fault condition had cleared....” EX1008, ¶[0082]; EX1002, ¶108.

2. Motivation to Combine

First, Sadwick evidences that a POSITA would have found it “obvious to try” modifying the Ivey-UL1993 Combination such that Ivey345’s Z test load 140 is configured in series with the LEDs, thereby eliminating the need for test load switch

135, as load switch 175 would have been used instead to periodically permit current to flow from rectifier 120 through the Z test load 140 to be detected by detector 150.

Sadwick, like the Ivey-UL1993 Combination, is directed to a fluorescent-replacing and potentially mains-line-powered LED-based light tube. EX1002, ¶110. *Compare* EX1008, ¶¶[0004], [0173], [0061], *with* EX1005, 2:11-13, 2:51-56, and §VII.A.5. Sadwick’s FLR utilizes “hazard protection circuitry” that, like Ivey345’s “current limiting circuit” in the Ivey-UL1993 Combination, protects against the fault configuration also identified in Ivey345—that a user may be electrically shocked during relamping if the user makes contact with an “exposed pin” while another is connected. EX1002, ¶110. *Compare* EX1008, ¶¶[0082], [0071], Fig.8, *with* EX1006, ¶¶[0010], [0005], *and* §VII.A.5. And Sadwick’s hazard protection circuitry does so by utilizing the same core circuit components configured in a nearly identical layout as Ivey345’s current limiting circuit. EX1002, ¶110.

Specifically, in both Sadwick’s and Ivey345’s protection circuits, current periodically flows¹⁰ from a line-powered LED-based light tube’s rectifier¹¹ through

¹⁰ *Compare* EX1008, ¶[0082] *with* EX1006, ¶[0021]. EX1002, ¶111 n.4.

¹¹ *Compare* EX1008, ¶[0080] (“input rectification stage”), *with* EX1005, 5:36-39 (“rectifier circuit”), *and* EX1006, ¶¶[0015]-[0016] (“rectifier 120”), *and* §VI.A.4. EX1002, ¶111 n.5.

a test resistor.¹² The voltage across the test resistor represents the current exiting the rectifier, which varies depending on whether a fault configuration exists.¹³ To detect such a fault configuration, the test resistor's voltage is fed into the non-inverting input of a comparator.¹⁴ At the same time, a reference voltage is fed into the comparator's inverting input.¹⁵ The comparator then compares the voltages such that when the test resistor's voltage is respectively lower/higher than the reference voltage, a fault configuration is/is not detected by the comparator, which in response outputs a signal to open/close a transistor in series with the LEDs¹⁶ and thus causes

¹² Compare EX1008, ¶[0080] (“sense resistor 1450”), with EX1006, ¶¶[0023]-[0027] (“Z test load 140”); EX1002, ¶111 n.6.

¹³ Compare EX1008, ¶¶[0080], [0082], with EX1006, ¶¶[0010], [0024]-[0027]. EX1002, ¶111 n.7.

¹⁴ Compare EX1008, ¶[0080] (“comparator 1434”), with EX1006, ¶¶[0024]-[0029] (“comparator 170”), Fig.3. EX1002, ¶111 n.8.

¹⁵ Compare EX1008, ¶[0080] (“reference set point signal”), with EX1006, ¶¶[0030]-[0032] (“detection threshold signal”), Fig.3. EX1002, ¶111 n.9.

¹⁶ Compare EX1008, ¶¶[0080], [0082], with EX1006, ¶¶[0030]-[0032], [0010]. EX1002, ¶111 n.10.

current to be below/above a safe level.¹⁷ Further, the detection of a fault configuration may also cause this transistor to be latched open until power is cycled.¹⁸

The main difference between the two is the placement of each's test resistor. EX1002, ¶112. Specifically, Sadwick's hazard protection circuit configures its test resistor (sense resistor 1450) "in series with" the LEDs, thereby allowing a single transistor 1430 (also "in series with" the LEDs) to be used for both (1) permitting current to flow periodically from the rectifier through sense resistor 1450 to determine whether a fault configuration exists, and (2) respectively disabling/maintaining current flow through the LEDs when the fault configuration is/is not detected. EX1008, ¶¶[0080], [0082]; EX1002, ¶112. By contrast, Ivey345's current limiting circuit in the Ivey-UL1993 Combination configures its

¹⁷ Compare EX1008, ¶¶[0080], [0082] (discussing limiting current to avoid "threat of harm and injury to people"), with EX1006, ¶¶[0010], [0023], and §VI.A.5 (discussing limiting current to a safe level, e.g., <5MIU). EX1002, ¶111 n.11.

¹⁸ Compare EX1008, ¶[0082] (stating transistor 1430 may be "latch[ed] off... until power is cycled"), with EX1006, ¶[0044] (stating latch 315 will "prevent[s] both present and future activation of the load switch 175" until power is "removed" and "reapplied"). EX1002, ¶111 n.12.

test resistor (Z test load 140) in parallel to main load 180 (LEDs), thereby requiring the use of two separate switches for controlling current flow in accordance with the above: (1) test load switch 135 (also parallel to the LEDs) permits current to flow periodically from rectifier 120 through Z test load 140, while (2) load switch 175 (in series with the LEDs) disables/maintains current flow through the LEDs. EX1006, ¶¶[0021]-[0024], [0010], [0041]-[0045], Fig.3; §VII.A.5, EX1002, ¶112. But the above illustrates the two and only two fundamental configurations that such a test resistor can be placed in relation to the LEDs: series or parallel. EX1002, ¶112. Indeed, that circuit components are configured either in series or parallel with one another is a core and known concept in electronics. EX1022¹⁹; EX1002, ¶112.

Accordingly, Sadwick and Ivey³⁴⁵ together identify a finite number of predictable solutions to choose from (two protection circuit layouts utilizing a test resistor configured either in series or parallel with the LEDs) to solve the same problem in line-powered LED-based light tubes with a reasonable expectation of success (protecting a user from being shocked during relamping when accidentally touching an exposed pin), and a POSITA would have therefore found it “obvious to try” modifying Ivey³⁴⁵’s current limiting circuit in the Ivey-UL1993 Combination to be in accordance with Sadwick’s hazard protection circuitry (configuring Z test

¹⁹ EX1031, pp.10-13.

load 140 in series with the LEDs and eliminating test load switch 135, as load switch 175 would be used instead for controlling current flow from rectifier 120 through Z test load 140 and the LEDs in accordance with the above). *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007); EX1008, ¶¶[0080], [0082]; EX1006, ¶¶[0021]-[0024], [0010], [0035]-[0036], [0045]; EX1002, ¶113.

Second, as explained above, Sadwick’s resistor-in-series protection circuit explicitly addresses the same problem addressed in Ivey345—a user accidentally being shocked during relamping (EX1008, ¶¶[0082], [0071]; EX1006, ¶¶[0010], [0005])—and a resistor-in-series configuration was therefore a known, suitable, and thus obvious, technique for addressing that problem. *See Intel Corp. v. PACT XPP Schweiz AG*, No. 2022-1037, 2023 WL 2469631, at *5 (Fed. Cir. Mar. 13, 2023) (“That [two references] address the same problem and that [the second reference presents] a known way to address that problem is precisely the reason that there’s a motivation to combine [the two references] under *KSR* and our precedent.”); EX1002, ¶114. Given applying Sadwick’s resistor-in-series technique to Ivey345’s protection circuit was not beyond a POSITA’s skill (*see, e.g.*, EX1008, ¶¶[0080], [0082]), this alone provides a sufficient motivation to combine the Ivey-UL1993 Combination with Sadwick. *Intel*, 2023 WL 2469631, at *4-5; EX1002, ¶114.

A POSITA would have also been motivated to combine the Ivey-UL1993 Combination with Sadwick because doing so would have (third) simplified

Ivey345's current limiting circuit and, independently, would have (fourth) improved performance. EX1002, ¶115. As a POSITA would have recognized, modifying Ivey345's current limiting circuit in accordance with Sadwick would have allowed a switch to be deleted—specifically test load switch 135—because load switch 175 would have been used instead to control current flow through Z test load 140 and the LEDs as discussed above. *See* EX1006, ¶¶[0021]-[0024], [0010], [0035]-[0036], [0045]; EX1008, ¶¶[0080], [0082]; EX1002, ¶115.

And with test load switch 135 deleted, so too could Ivey345's power-up reset 160. *See* EX1006, ¶¶[0033]-[0034], Fig.3; EX1002, ¶116. Power-up reset 160, “[w]hen power is first applied to the current limiting circuit 100,... turn[s] off main load switch 175... [and] maintains this state until a stable condition is reached and a determination can be made whether a subject is present in the circuit.” EX1006, ¶[0034]; EX1002, ¶116. In other words, power-up reset 160 ensures that load switch 175 remains off until the signal from detector 150, driven by test load switch 135 (*see* EX1006, ¶[0024]), permits detection of a human in the circuit (*id.*, ¶[0034]). EX1002, ¶116. But by modifying the Ivey-UL1993 Combination such that one transistor—load switch 175—performs both the load-control and human-detection functions, there would have been no need for power-up reset 160 to control a non-existent additional transistor. EX1002, ¶116.

Further, the above modification would have also allowed a resistor to be deleted. EX1002, ¶117. Specifically, although the above modification would have resulted in Z test load 140—“a resistor” (EX1006, Fig.3, ¶[0080])—being configured in series with the LEDs rather than parallel (*see* EX1008, ¶¶[0080], [0082]), such a modification would not have required placing an additional resistor in series with the LEDs, because a series resistor would have already existed. EX1002, ¶117. As generally known, LEDs must have what is known as a “current limiting resistor” placed in series, because LEDs will otherwise burn out if directly connected to a power source. EX1018²⁰; EX1021, ¶[0011]; EX1002, ¶117. Given that such a current-limiting series resistor would have thus already existed in Ivey345’s current limiting circuit, a POSITA would have recognized to use such a preexisting resistor as—and for carrying out the functions of—Z test load 140 when making the above modification, rather than adding a superfluous series resistor for serving this same purpose. EX1002, ¶117; *see also* EX1019,²¹ 3 (demonstrating that LED current can be determined by measuring current limiting resistor voltage); EX1021, ¶[0035] (same).

²⁰ *See* EX1031, pp.14-16.

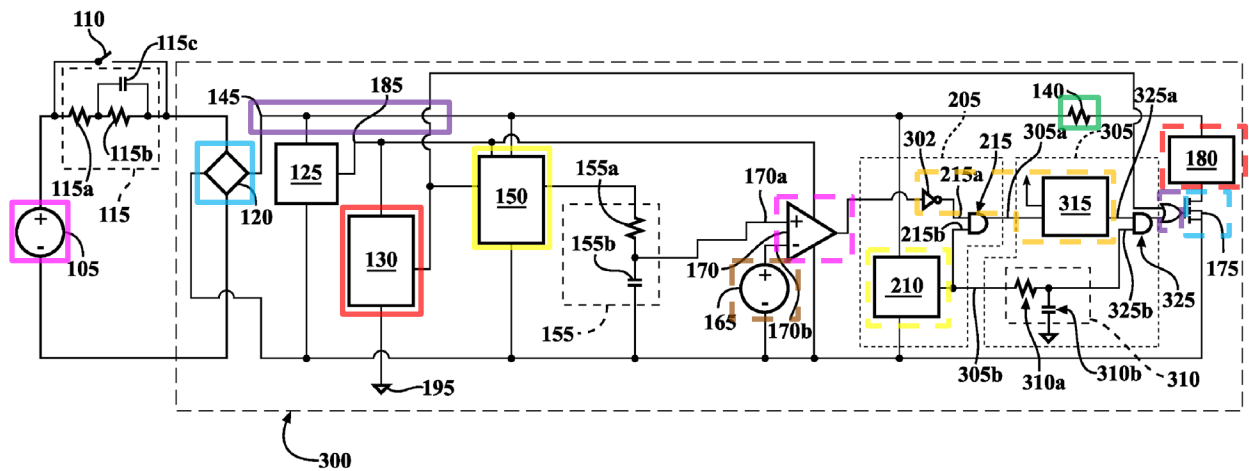
²¹ *See* EX1030, ¶¶14-16.

Independently, the above modification would have improved performance. EX1002, ¶118. Specifically, a POSITA would have recognized that, unlike in the parallel configuration, configuring Z test load 140 in series with the LEDs would have caused the current flowing through Z test load 140 to exactly equal the current flowing from rectifier 120 through the LEDs and thus more accurately represent whether a subject is present in the circuit. *See* EX1020, 3:36-44 (“[T]here are uncertainties within the forward voltages of the LEDs, which in turn creates uncertainty with respect to the current level flowing through the LEDs. To manage these uncertainties, the current flowing through the LEDs is measured by determining a voltage level across a known resistor and calculating the current level.”), 3:51-55 (“As shown, the circuit of FIG. 1 comprises a plurality of LEDs coupled in series with a channel control transistor and a current sense circuit between a supply voltage V_{DD} and a reference ground.” (diagram numbering omitted)); EX1002, ¶118. Such a modification would have thus increased the current limiting circuit’s fault detection accuracy and therefore improved performance, motivating a POSITA to perform the modification. EX1002, ¶118.

3. The Resulting Ivey-UL1993-Sadwick Combination

So modified, Ivey345’s current limiting circuit in the Ivey-UL1993 Combination (*see* §VII.A.5) is modified to be in accordance with Sadwick (the Ivey-UL1993-Sadwick Combination) such that Z test load 140 is configured “in series

with” rectifier 120 and the LEDs (*see* EX1008, ¶[0080]; EX1006, ¶¶[0023]-[0024]). EX1002, ¶119. Ivey345’s Figure 3, modified below, illustrates the Ivey-UL1993-Sadwick Combination:



EX1006, Fig.3 (modified); EX1002, ¶119. As shown, test load switch 135 is eliminated, as load switch 175 (dotted-blue) instead performs test load switch 135’s function of periodically permitting current to flow from rectifier 120 (solid-blue) and device power rail 145 (solid-purple) through Z test load 140 (solid-green), in addition to load switch 175’s original function of respectively disabling/maintaining current flow through main load 180 (LEDs) (dotted-red) when a fault configuration is/is not detected. *See* EX1008, ¶¶[0080], [0082]; EX1006, ¶¶[0021]-[0024], [0010], [0035]-[0037], [0045]; EX1002, ¶119. As such, the output of oscillator 130 (solid-red) is connected to load switch 175 rather than test load switch 135. *See* EX1008, ¶¶[0080], [0082]; EX1006, ¶[0021]-[0024], [0010], [0035]-[0036], [0045]; EX1002,

¶119. Likewise, power-up reset 160 is also eliminated. *See* EX1006, ¶¶[0033]-[0034]; EX1002, ¶119.

The current limiting circuit's remaining operations are unchanged. EX1002, ¶120. Specifically, detector 150 (solid-yellow) synchronously detects a variation across device power rail 145, and comparator 170 (dotted-pink) compares detector 150's detection result to detector threshold signal source 165's (dotted-brown) signal to detect whether a fault configuration exists. *See* EX1008, ¶¶[0080], [0082]; EX1006, ¶¶[0023]-[0032], [0034]-[0035], [0010]; EX1002, ¶120. Respectively, if a fault configuration is/is not detected, comparator 170 outputs a "low"/"high" signal to logic inverter 302 and latch 315 (together in dotted-orange), and latch 315 in response outputs a "low"/"high" signal to load switch 175 through main load detection logic circuit 325 to disable/maintain current flow through the LEDs, causing current to be below/above, e.g., 5MIU. *See* EX1008, ¶¶[0080], [0082]; EX1006, ¶¶[0034]-[0035], [0010], [0023], [0044]-[0046]; §VII.A.5; EX1002, ¶120. Timer 210 (dotted-yellow) prevents latch 315's signal from passing to load switch 175 until a normal configuration is maintained for a "detection valid time." EX1006, ¶¶[0045]-[0046], [0030]-[0032]; EX1002, ¶120.

Once such time elapses, load switch 175 therefore closes when latch 315's output is high, oscillator 130's output is high, or both, and opens otherwise. EX1006, ¶¶[0035]-[0036], [0045]-[0046], [0020]-[0022], [0024], [0010]; EX1008, ¶[0082];

EX1002, ¶121. To enable such “or” control of load switch 315, a POSITA would have recognized to apply the standard practice of placing a logical OR gate (dotted-purple) at the load switch 175’s gate for receiving both latch 315’s output and oscillator 130’s output.²² See EX1023²³; EX1002, ¶121; see also EX1008, ¶[0212]; EX1006, ¶[0046].

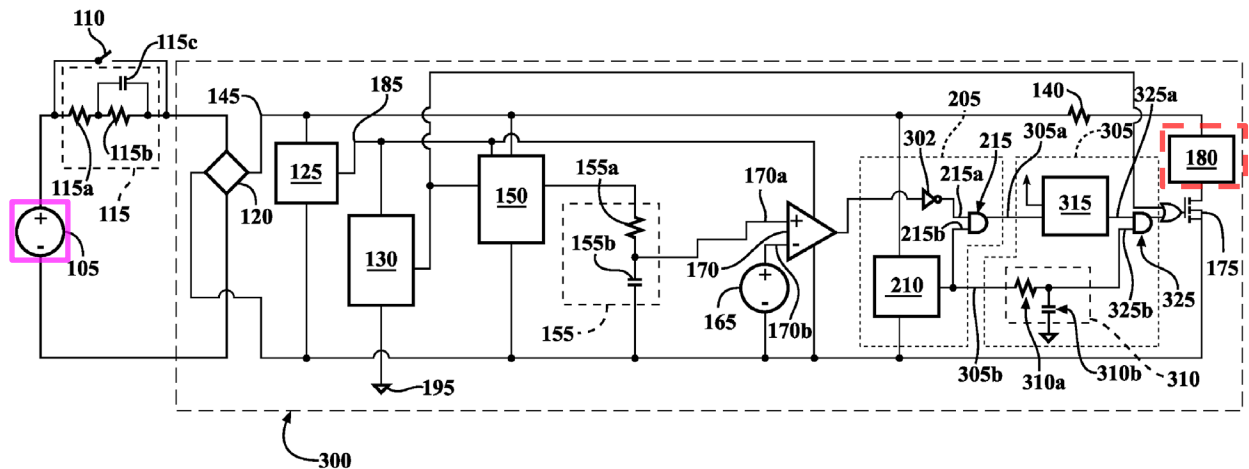
4. *Element-by-Element Analysis*

(a) Limitation [18pre]

To the extent limiting, the Ivey-UL1993-Sadwick Combination utilizes, within power converter 36 of Ivey813’s “LED-based light tube,” Ivey345’s Sadwick-modified “current limiting circuit,” which detects during relamping whether a subject user is making contact with the tube’s return terminal while the tube’s power terminal is connected to fixture 11 (Ivey345’s power source 105 (solid-pink)):

²² Should PO argue that placing this OR gate negates the simplification benefits discussed in §VI.B.2, a POSITA would have recognized that deleting three components from Ivey345’s circuit (switch, resistor, power-up reset) outweighs adding one component (OR gate) and results in a net simplification. EX1002, ¶121 n.13.

²³ See EX1031, pp.7-9.



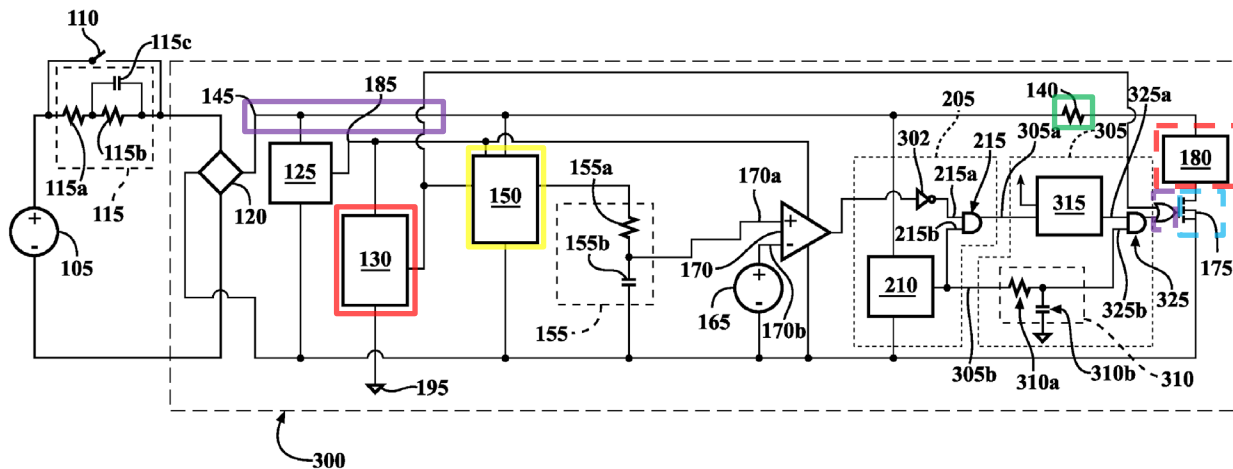
EX1005, 3:50-54, 5:33-35; EX1006, Fig.3 (modified), ¶¶[0010], [0004]-[0005]; EX1008, ¶¶[0080], [0082]; §VII.B.3; EX1002, ¶122. If such is detected, the current limiting circuit maintains current flow “at a low and safe level” and thus performs the claimed “detection method...” EX1006, ¶¶[0010], [0004]-[0005]; EX1008, ¶¶[0080], [0082], [0071]; EX1002, ¶122.

(b) Limitation [18a]

See §§VII.A.6(b), VII.B.3.

(c) Limitation [18b]

See §VII.A.6(c). Differently here, because test load switch 135 is deleted, load switch 175 alone forms the claimed “switch circuit.” §VII.B.3; EX1002, ¶124. The output of oscillator 130 (solid-red) is fed into an OR gate (dotted-purple) at the gate of load switch 175 (dotted-blue), which therefore opens and closes at least while oscillator 130’s clock signal oscillates low and high, respectively:



EX1006, Fig.3 (modified), ¶¶[0020]-[0022], [0024], [0035]-[0036], [0045]; EX1008, ¶¶[0080], [0082]; §VII.B.3; EX1002, ¶124.

Further, Z test load 140 (solid-green) is configured in series with device power rail 145 (solid-purple) and the LEDs. EX1006, ¶[0023]; EX1008, ¶[0080]; §VII.B.3; EX1002, ¶125. Thus, while load switch 175 is closed by oscillator 130's high output accordingly, current flows through Z test load 140 and main load 180 (dotted-red), i.e., the LEDs. EX1006, ¶¶[0020]-[0024], [0035]-[0036], [0045]; EX1008, ¶¶[0080], [0082]; §VII.B.3; EX1002, ¶125.

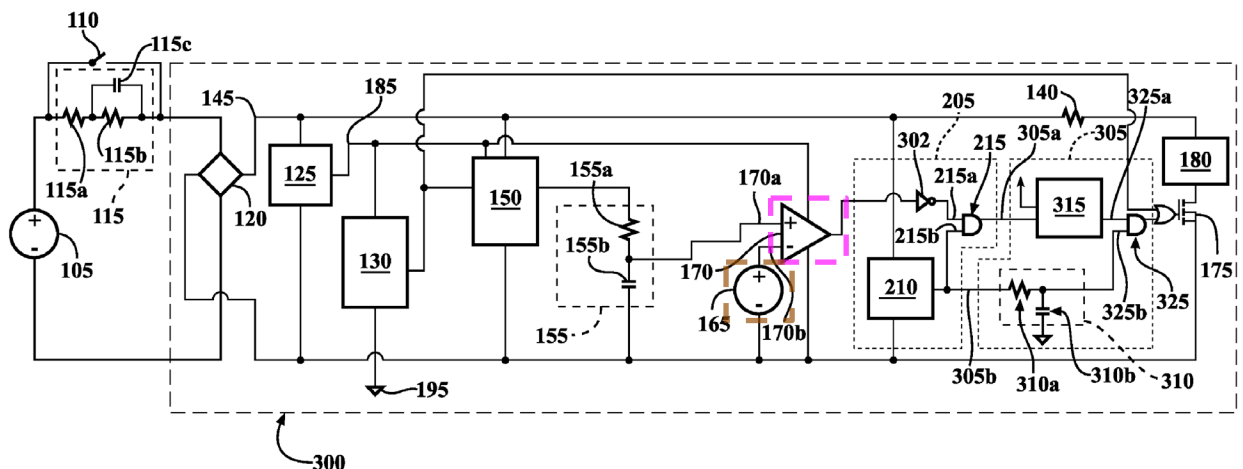
(d) Limitation [18c]

See §VII.A.6(d). Here, although Z test load 140 is configured in series with device power rail 145 and the LEDs, the discussed functions of detector 150 remain unchanged—detector 150 “detect[s] a variation in the current draw or voltage across the device power rail 145” based on current now flowing through Z test load 140, and outputs a representative signal used to determine whether a fault configuration

exists. EX1006, ¶¶[0024]-[0026], [0010]; EX1008, ¶¶[0080], [0082], claim 14; §VII.B.3; EX1002, ¶126.

(e) Limitation [18d]

See §VII.A.6(e). Here, the discussed functions of comparator 170 (dotted-pink) and detection threshold signal source 165 (dotted-brown) also remain unchanged—comparator 170 compares detector 150's output signal to a threshold signal from detection threshold signal source 165 (dotted-brown) and produces an output relating to the comparison:



EX1006, Fig.3 (modified), ¶¶[0030]-[0032]; EX1008, ¶¶[0080], [0082]; §VII.B.3;
EX1002, ¶127.

(f) Limitation [18e]

Comparator 170's functions in the Ivey-UL1993-Sadwick Combination again remain unchanged—when detector 150's output signal is lower than the threshold signal (fault configuration), comparator 170 outputs a “low” signal that ultimately

causes load switch 175 to remain off, causing current to be limited to, e.g., <5MIU. EX1006, ¶¶[0010], [0030]-[0032], [0044]-[0045]; EX1008, ¶¶[0080], [0082]; §§VII.A.6(f), VII.B.3; EX1002, ¶128.

(g) Claim 19

See §VII.A.6(g). Here, comparator 170's discussed functions again remain unchanged—when detector 150's output signal is higher than the threshold signal, comparator 170 outputs a “high” signal, causing load switch 175 to remain closed and current to flow from device power rail 145 through the LEDs. EX1006, ¶¶[0010], [0030]-[0032], [0041], [0044]-[0045]; EX1008, ¶¶[0080], [0082]; §VII.B.3; EX1002, ¶129.

(h) Limitations [10pre]-[10c]

See §§VII.A.6(h)-VII.A.6(k), VII.B.3.

(i) Limitation [10d]

In addition to Ivey813's tube, the Ivey-UL1993-Sadwick Combination utilizes Ivey345's Sadwick-modified current limiting circuit (“installation detection module”), which includes various components coupled to the tube's device power rail 145 such as detector 150 and comparator 170 (“coupled on a power loop of the LED tube lamp”). *See* §§VII.B.4(b)-VII.B.4(d); EX1002, ¶131. The modified current limiting circuit detects a variation across device power rail 145, outputs a

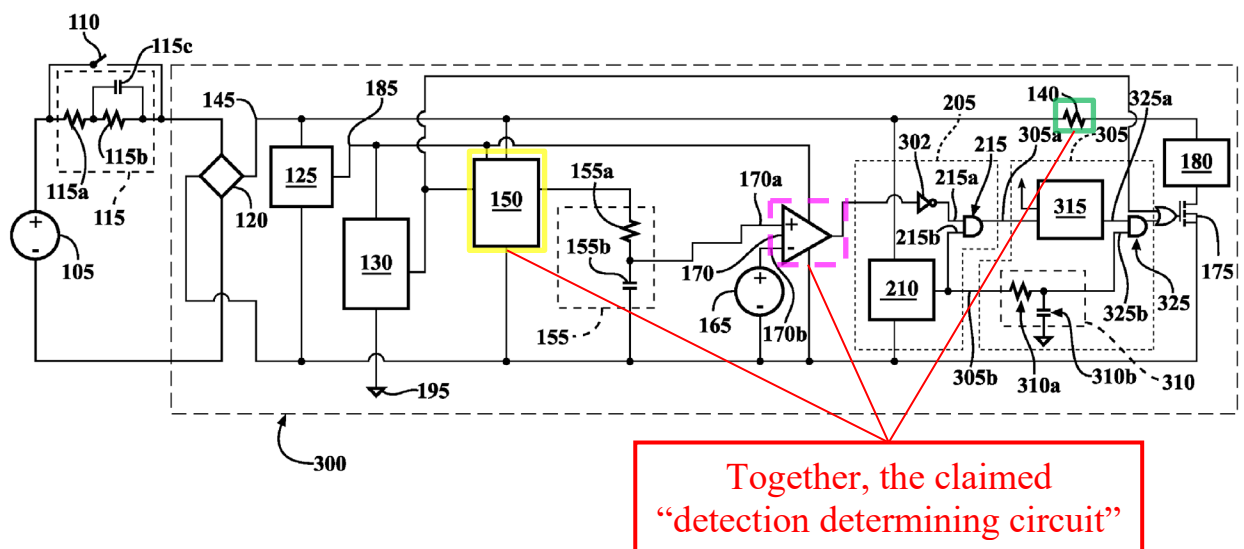
representative signal, and compares this representative signal to a threshold signal. *See* §VII.B.4(e); EX1002, ¶131.

(j) Limitation [10e]

When the representative signal is lower than the threshold signal, the Ivey-UL1993-Sadwick Combination’s current limiting circuit maintains current flow at, e.g., <5MIU by signaling load switch 175 to remain off. *See* §VII.B.4(f); EX1002, ¶132.

(k) Claim 11

As similarly discussed in §VII.A.6(n), detector 150, comparator 170, and Z test load 140 altogether form the claimed “detection determining circuit.” EX1002, ¶133. *Compare* EX1006, Fig.3 (modified below), and EX1008, Fig.14, ¶¶[0080], [0082], and §VII.B.3, with, e.g., EX1001, Fig.15K, 50:3-54.



Detector 150 detects the variation across device power rail 145 and outputs a representative signal to comparator 170, which compares detector 150's output signal to the threshold signal and outputs either a low or high signal depending on this comparison. EX1006, ¶¶[0024]-[0032], [0010]; EX1008, ¶¶[0080], [0082]; §§VII.A.6(n), VII.B.3; EX1002, ¶133.

(l) Claim 12

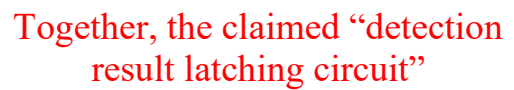
See §§VII.A.6(o), VII.B.3.

(m) Claim 16

See §VII.B.4(c). Load switch 175 is connected to Z test load 140 through the LEDs and receives oscillator 150's clock signal through the OR gate, causing load switch 175 to close at least while the clock signal oscillates high. EX1006, ¶¶[0020]-[0024], [0035]-[0036], [0045]; EX1008, ¶¶[0080], [0082]; §VII.B.3; EX1002, ¶134.

(n) Claim 17

Ivey345's Sadwick-modified current limiting circuit includes logic inverter 302 and latch 315 (together in dotted-orange), which together with the OR gate meet the claimed "detection result latching circuit" under both the term's plain and ordinary meaning and the *Maxlite* Court's construction (*see* EX1025, 26-28; §VI.C.1):



EX1006, Fig.3 (modified); EX1002, ¶135. Specifically, the OR gate receives oscillator 130's clock signal, causing load switch 175 to close at least while oscillator 130's clock signal oscillates high (the recited "coupled to... the detection pulse generating module, and the switch circuit, wherein at least one of... the pulse signal... is provided to the switch circuit through the detection result latching circuit," and the *Maxlite* Court's construction of "circuit that reverses its signal level when the... ***pulse signal from the detection pulse generating module*** is applied").

§VII.B.3; EX1025, 26-28; EX1002, ¶135. The OR gate also receives latch 315's output, which as explained in §VII.A.6(q) is latched either "high" or "low" to turn on or off load switch 175, respectively, depending on comparator 170's output to logic inverter 302 (the recited "coupled to the detection determining circuit,... and the switch circuit, wherein at least one of... the high level signal, and the low level signal is provided to the switch circuit through the detection result latching circuit,"

and the *Maxlite* Court’s construction of “circuit that reverses its signal level when the *detected result*... is applied and *maintains its signal level based on the detected result*”). EX1006, ¶¶[0043]-[0046], [0030]-[0032]; EX1025, 26-28; EX1002, ¶135.

(o) Limitations [23pre]-[23d]

See §§VII.B.4(h)-VII.B.4(i).

(p) Limitation [23e]

See §§VII.A.6(t), VII.B.3.

(q) Limitation [23f]

See §§VII.A.6(u), VII.B.3.

(r) Claim 24

See §§VII.A.6(v), VII.B.3.

(s) Claim 25

See §§VII.A.6(w), VII.B.3.

(t) Limitations [26pre]-[26d]

See §§VII.B.4(h)-VII.B.4(i).

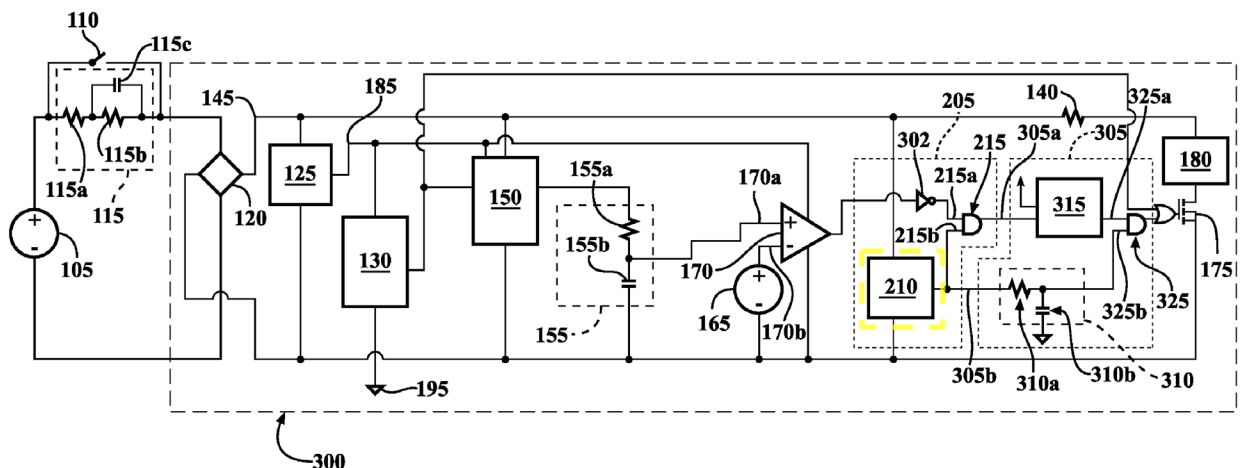
(u) Limitation [26e]

Ivey345’s Sadwick-modified current limiting circuit meets the claimed “control module.” The modified current limiting circuit controls whether current may flow from device power rail 145 through the LEDs by outputting a signal from the OR gate to either turn on or off load switch 175. EX1006, ¶¶[0010], [0044]-[0045]; EX1008, ¶¶[0080], [0082]; §VII.B.3; EX1002, ¶142. When detector 150’s

representative signal is lower than threshold signal source 165's threshold signal, the modified current limiting circuit maintains current flow at a safe level—e.g., <5MIU—by signaling load switch 175 to remain off. EX1006, ¶¶[0010], [0030]-[0032], [0044]-[0045]; EX1008, ¶¶[0071], [0080], [0082]; §§VII.B.3, VII.B.4(f); EX1002, ¶142.

(v) Limitation [26f]

See §VII.A.6(z). Here, the discussed functions of timer 210 (dotted-yellow) also remain unchanged—timer 210 prevents latch 315's signal from passing to load switch 175 until a normal configuration is maintained for a detection valid time:



EX1006, Fig.3 (modified), ¶¶[0045]-[0046], [0038]-[0039]; §VII.B.3; EX1002, ¶143. Thus, for the detection valid time at startup, a low signal is sent from “detection logic circuit 325” to the OR gate at load switch 175's gate. See EX1006, ¶¶[0044]-[0045], [0038]-[0039]; §VII.B.3; EX1002, ¶143. At the same time, oscillator 130's clock signal is also sent to the OR gate, causing the output to load

switch 175 to follow the clock signal (“generates the control signal having a first waveform during a detection stage”). *See* EX1008, ¶¶[0080], [0082]; EX1006, ¶[0021]-[0024], [0010], [0035]-[0036], [0045]; §VII.B.3; EX1002, ¶143. If a normal configuration is maintained thereafter, latch 315’s signal, which is high at startup, will remain high and will also be permitted to pass through detection logic circuit 325 to the OR gate and thus load switch 175, allowing the LEDs to receive constant power from device power rail 145 and thus operate (“generates the control signal having a second waveform during an operating stage”). EX1006, ¶¶[0044]-[0046], [0038]-[0039], [0010]; EX1008, ¶[0082]; §VII.B.3; EX1002, ¶143.

(w) Claim 27

See §VII.B.4(n). For the same reasons that Ivey345’s Sadwick-modified current limiting circuit meets claim 17’s “installation detection module,” the modified current limiting circuit meets claim 27’s “control module.” EX1002, ¶144.

(x) Limitations [28pre]-[28c]

See §VII.B.4(h).

(y) Limitation [28d]

See §VII.B.4(i). Additionally, the clock signal from Ivey345’s Sadwick-modified current limiting circuit’s oscillator 130 controls the activation of load switch 175. *See* §VII.B.4(m); EX1002, ¶146. Detector 150 detects the variation

across device power rail 145 while the clock signal oscillates high. *See* §VII.B.4(l); EX1002, ¶146.

(z) Limitation [28e]

Oscillator 130 outputs an oscillating clock signal with a 1ms period. EX1006, ¶¶[0019]-[0020]; EX1002, ¶147. Thus, only a fraction of the clock signal's 1ms period is high. EX1002, ¶147. This clock signal allows variation to be detected on device power rail 145 and current to be limited—e.g., <5MIU (*see* §VII.B.4(f))—when a fault configuration is detected. EX1006, ¶¶[0023]-[0024]; EX1008, ¶¶[0071], [0080], [0082]; §VII.B.3; EX1002, ¶147.

(aa) Claim 29

See §§VII.B.4(z), VII.A.6(ee).

(bb) Limitations [32pre]-[32c]

See §VII.B.4(h).

(cc) Limitation [32d]

See §§VII.B.4(y), VII.B.3.

(dd) Limitation [32e]

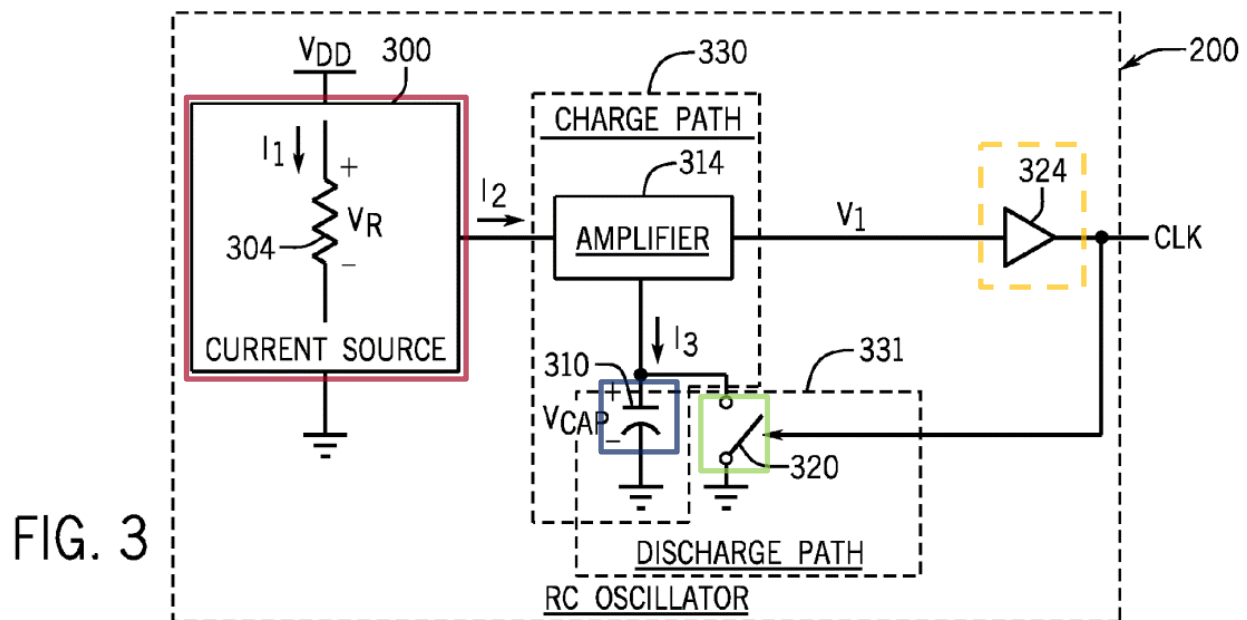
See §§VII.A.6(hh), VII.B.3.

C. Grounds 3-4: Ivey813, Ivey345, UL1993, and Powell—and Optionally Sadwick—Render Obvious Claims 1-3, 5-9, 13-15, and 20-22

1. Powell

Powell is directed to “an RC oscillator.” EX1009, 1:18-22; EX1002, ¶152.

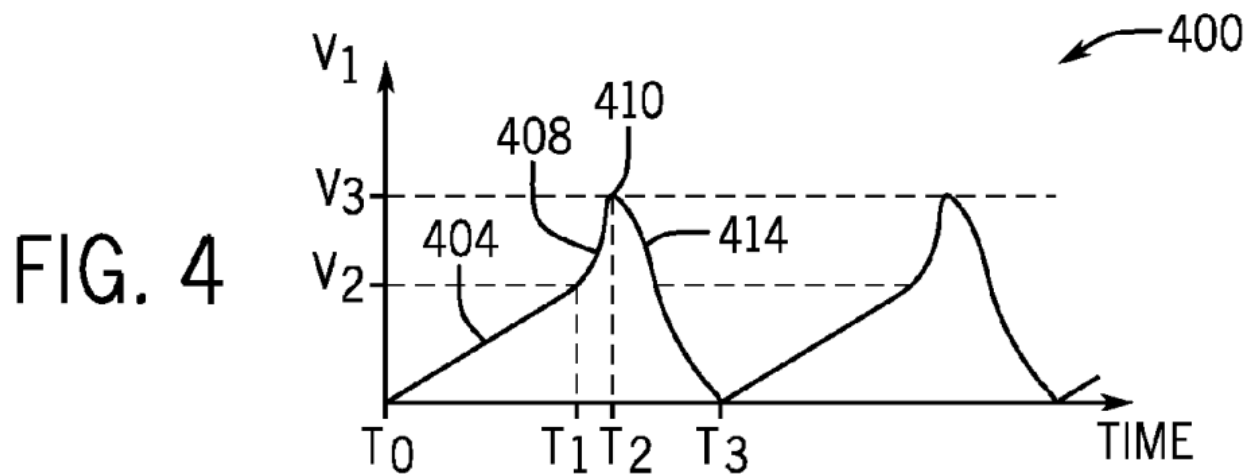
Powell’s Figure 3 provides an example:



EX1009, Fig.3; EX1002, ¶152. As shown, RC oscillator 200 is powered by a standard “ V_{DD} supply voltage” and includes current source 300 (solid-dark-red). EX1009, 7:23-35, 4:62-64; EX1002, ¶152. During a “charging part” of the RC oscillator’s “oscillation cycle,” current source 300 outputs constant current I_2 , which produces charging current I_3 within charge path 330. EX1009, 5:1-6; EX1002, ¶152. Further, “switch 320 [(solid-light-green)] does not conduct,” causing capacitor 310 (solid-dark-blue) to charge and thus its voltage V_{CAP} to increase. EX1009, 5:9-12,

5:23-29; EX1002, ¶152. Amplifier 314 amplified V_{CAP} to produce a voltage V_1 , which is then “pulse shape[d]” by digital buffer 324 (dotted-orange). EX1009, 5:13-22, 6:1-5; EX1002, ¶152.

As capacitor 310 charges, V_1 eventually reaches a voltage that causes switch 320 to conduct, thus beginning the cycle’s “discharging part,” where capacitor 310 is discharged through to ground through switch 320, which thus forms discharge path 331. EX1009, 5:23-34; EX1002, ¶153. This discharging “causes the V_1 and V_{CAP} voltages to decrease; and the lowered V_1 voltage causes the switch 320 to turn off, thereby ending the [dis]charging part of the current cycle” and beginning a new cycle. EX1009, 5:34-39; EX1002, ¶153. Powell’s Figure 4 illustrates V_1 ’s oscillating waveform from charging (T_0 to T_2) and discharging (T_2 to T_3) capacitor 310:



EX1009, Fig.4, 6:34-38; EX1002, ¶153.

Lastly, current source 300 includes resistor 304, which together with capacitor 310 forms the RC oscillator's "RC tank" that "establishes the resonance frequency for the oscillator." EX1009, 4:62-64, 2:34-40; EX1002, ¶154. This configuration allows "die area [to be] preserved" and "current (and therefore power consumption) [to] be reduced...." EX1009, 2:53-58, 6:19-24; EX1002, ¶154.

2. Motivation to Combine

Regarding Ivey345's current limiting circuit in the Ivey-UL1993 (*see* §VII.A.5) and Ivey-UL1993-Sadwick (*see* §VII.B.3) Combinations, Ivey345 states that oscillator 130 may be, e.g., a "relaxation-type oscillator"; is auxiliary-powered by, e.g., standard 5V power; and outputs an oscillating signal (*see* EX1006, ¶¶[0019]-[0020], [0017]). EX1002, ¶155. But Ivey345 provides no specific layout for oscillator 130 (solid-red), instead specifying it as an empty box:

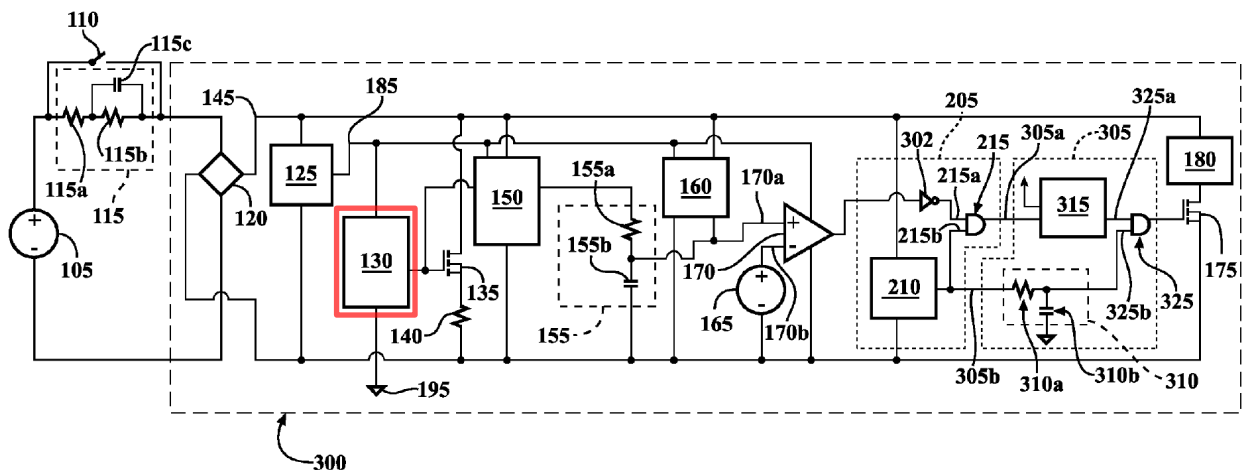


FIG. 3

EX1006, Fig.3; EX1002, ¶155. Such a generic description for oscillator 130 thus teaches no more than using any known oscillator capable of performing oscillator 130's functions of outputting an oscillating signal that opens and closes test load switch 135 and, indirectly, load switch 175 in the Ivey-UL1993 Combination (*see* §§VII.A.5, VII.A.6(c); EX1006, ¶¶[0020]-[0022], [0024]), or simply load switch 175 in the Ivey-UL1993-Sadwick Combination (*see* §VII.B.3; EX1006, ¶¶[0010], [0035]-[0036], [0045]; EX1008, ¶[0082]). EX1002, ¶155.

Powell's RC oscillator is such a known oscillator, as it is indeed a "relaxation-type oscillator" (its output depends on charging and discharging a capacitor) (EX1009, 4:65-67; *see also* EX1024²⁴), is powered by a standard supply voltage V_{DD} (EX1009, 7:23-35), and generates an oscillating signal V_1 (*id.*, 4:65-5:39, 6:34-38, Fig.4). EX1002, ¶156. Thus, Ivey345 teaches using an RC oscillator like Powell's as Ivey345's oscillator 130 within the Ivey-UL1993 and Ivey-UL1993-Sadwick Combinations. EX1002, ¶156. Further, a POSITA would have been otherwise motivated to use Powell's RC oscillator accordingly, because Powell's RC oscillator likewise generates an oscillating clock signal while, e.g., reducing die area and power consumption. EX1009, 6:19-21; EX1002, ¶156.

²⁴ *See* EX1031, pp.4-6.

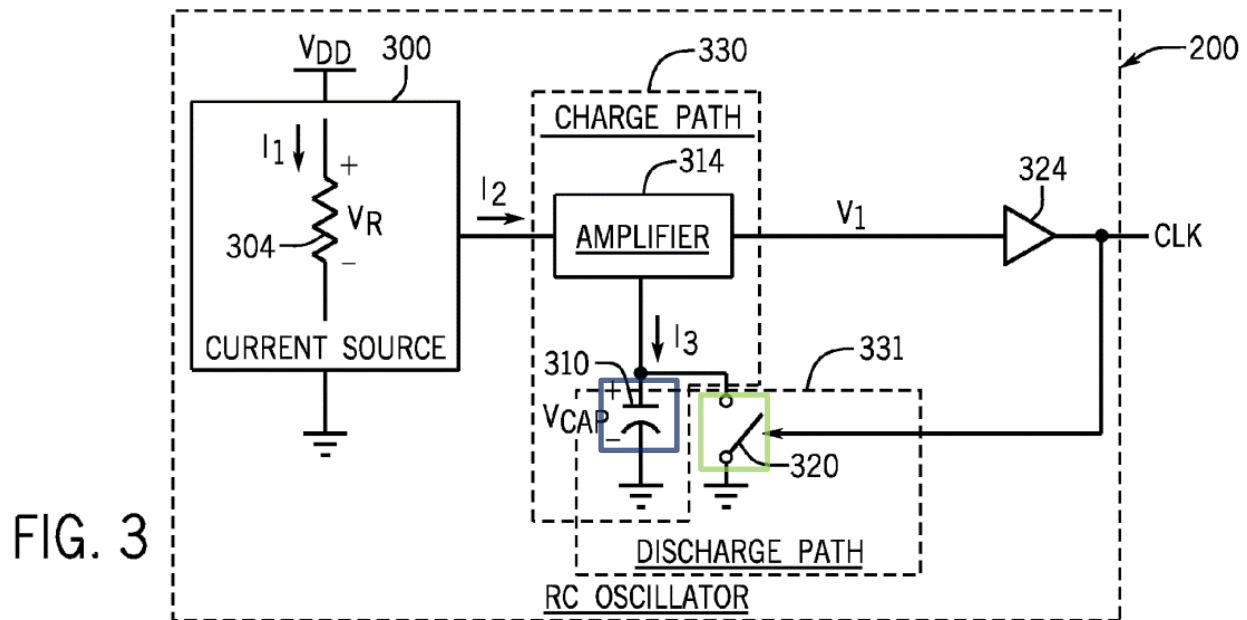
3. *The Resulting Ivey-UL1993-Powell and Ivey-UL1993-Sadwick-Powell Combinations*

So modified, Powell's RC oscillator is used as oscillator 130 in Ivey345's current limiting circuit within the Ivey-UL1993 Combination (*see* §VII.A.5; EX1006, ¶¶[0020]-[0022], [0024]) (the Ivey-UL1993-Powell Combination) and the Ivey-UL1993-Sadwick Combination (*see* §VII.B.3; EX1006, ¶¶[0010], [0035]-[0036], [0045]; EX1008, ¶[0082]) (the Ivey-UL1993-Sadwick-Powell Combination). EX1002, ¶157. Specifically, Powell's RC oscillator is auxiliary-powered—it receives its “V_{DD} supply voltage” from Ivey345's auxiliary power supply 125 (*see* EX1009, 7:23-35; EX1006, ¶¶[0016], [0019])—and outputs an oscillating signal (pulse-shaped V₁) to control the same circuit elements as oscillator 130 (EX1006, ¶[0019]-[0022], [0024], [0027], [0043]; EX1009, 4:65-5:39, 6:34-38, Fig.4). EX1002, ¶157.

4. *Element-by-Element Analysis*

(a) Limitation [20a]

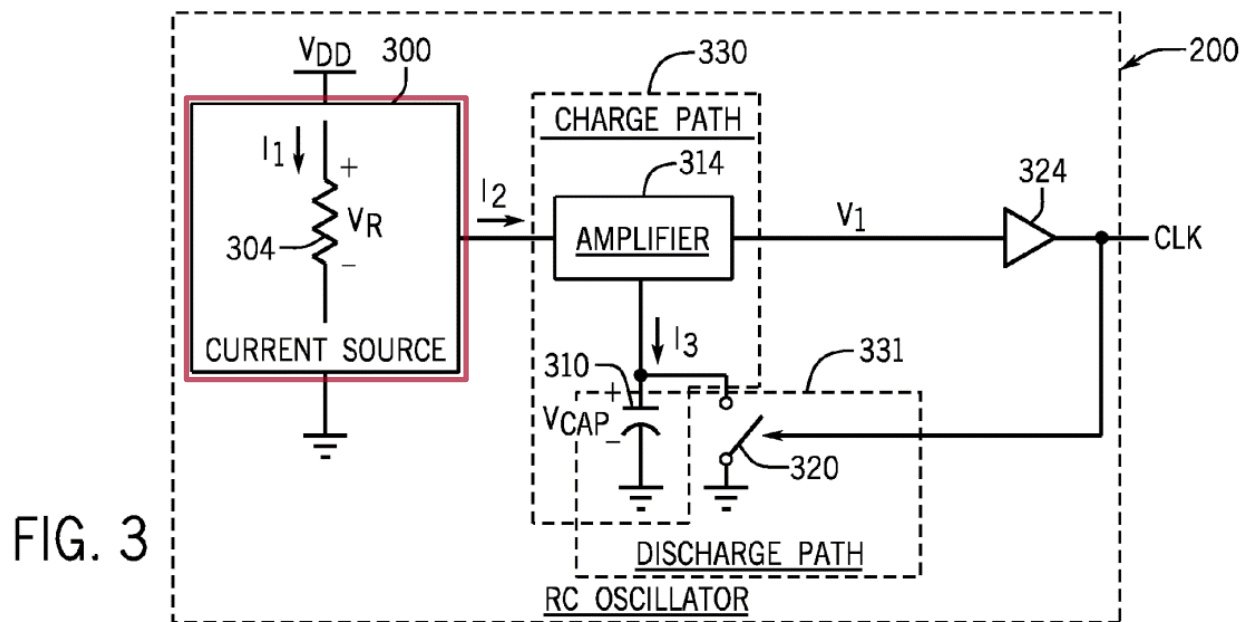
In the Ivey-UL1993-Powell and Ivey-UL1993-Sadwick-Powell Combinations, Powell's RC oscillator is used as oscillator 130, which likewise generates an oscillating signal V₁ (“generating the pulse signal by the detection pulse generating module”). EX1009, 4:65-5:39, 6:34-38, Fig.4; EX1006, ¶[0019]; EX1008, ¶[0082]; §VII.C.3; EX1002, ¶158.



Within Powell’s RC oscillator (“detection pulse generating module”), switch 320 (solid-light-green) forms discharge path 331 for capacitor 310 (solid-dark-blue), over which charge built up in capacitor 310 is periodically discharged (“discharge path”). EX1009, 5:23-39, 4:65-67, Fig.3; EX1002, ¶158.

(b) Limitation [20b]

To generate the oscillating signal V_1 , current source 300 (solid-dark-red), which is powered by V_{DD} supply voltage (and thus from auxiliary power supply 125 of Ivey345’s current limiting circuit) (“receives a driving signal”), charges capacitor 310 during a “charging part” of the RC oscillator’s “oscillation cycle”:

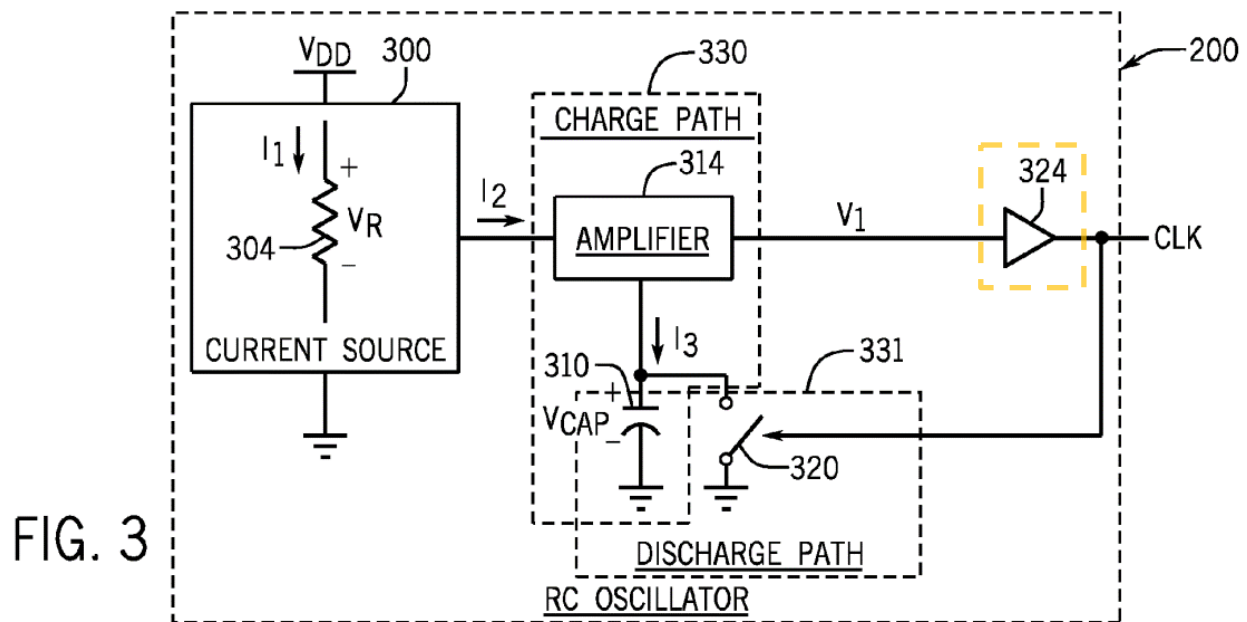


EX1009, Fig.3, 5:1-6; EX1002, ¶159. Accordingly, capacitor 310's voltage V_{CAP} increases. EX1009, 5:9-12, 5:23-29; EX1002, ¶159. V_{CAP} is amplified by amplifier 314 to produce the oscillating signal V_1 , which also rises during the charging part of the cycle until reaching a high logic level ("pulling the pulse signal to a high level voltage"), ending the charging part. EX1009, 5:13-22, 5:25-34; EX1002, ¶159.

(c) Limitation [20c]

V_1 is pulse shaped by buffer 324 (dotted-orange) and then outputted to switch 320 ("feeding the pulse signal back to the discharge path")²⁵:

²⁵ Should PO argue this pulse-shaped V_1 signal outputted from buffer 324 is no longer the claimed "pulse signal" because it is modified—and thus different—from



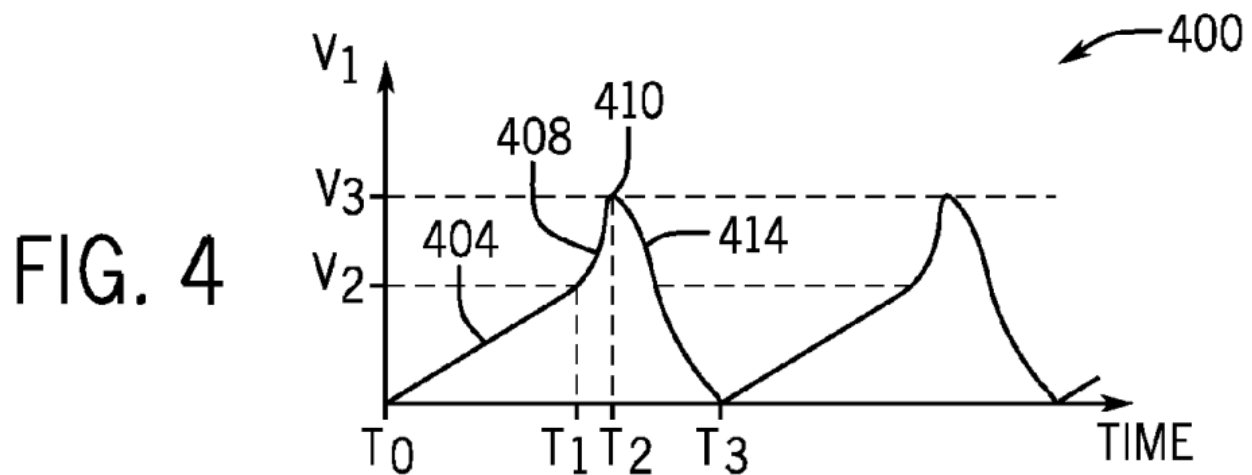
EX1009, Fig.3, 5:13-39, 6:1-5; EX1002, ¶160. Once V_1 reaches a high logic level (“pulled to the high level voltage”), the pulse-shaped V_1 thereafter causes the switch 320 to conduct, beginning a “discharging part” of the cycle where capacitor 310 is discharged through switch 320 to ground (“conduct the discharge path”). EX1009, 5:29-39; EX1002, ¶160.

the inputted V_1 , such would be inconsistent with PO’s infringement contentions, which assert that one signal (“S5”) that enters a “buffer circuit” (“S4 driver”) and another (“S4”) that exits are both the claimed “pulse signal.” See EX1028, 55-59; EX1029, 55-60; EX1002, ¶160 n.14.

(d) Limitation [20d]

The discharging of capacitor 310 “causes the V_1 and V_{CAP} voltages to decrease,” eventually reaching a low logic level that “causes the switch 320 to turn off, thereby ending the [dis]charging part of the current cycle and beginning the charging part of the next cycle” (“pulling the pulse signal to a low level voltage after the discharge path has been conducted”). EX1009, 5:29-39; EX1002, ¶161.

Powell’s Figure 4 illustrates V_1 ’s oscillating waveform before pulse-shaping, where the discharging part occurs from T_2 to T_3 (“predetermined time period”), while the charging part occurs from T_0 to T_2 :



EX1009, Fig.4, 6:34-38; EX1002, ¶162; *see also* EX1009, 6:9-12.

(e) Claim 21

From T_2 to T_3 in Powell’s Figure 4, switch 320 is turned on by the pulse-shaped V_1 signal, which is therefore at a high logic level from T_2 to T_3 (“the

predetermined time period is the same as the pulse-on period of the pulse signal”).

See EX1009, Fig.4, 6:34-38, 5:25-39; EX1002, ¶163.

(f) Claim 22

When V_1 reaches a low logic level at the end of the discharging part of the oscillation cycle, “the lowered V_1 voltage causes the switch 320 to turn off...” (“cutting off the discharge path when the pulse signal is pulled to the low level voltage”). EX1009, 5:29-39; EX1002, ¶164.

(g) Limitation [1pre]

To the extent limiting, the Ivey-UL1993-Powell and Ivey-UL1993-Sadwick-Powell Combinations utilize, within power converter 36 of Ivey813’s mains line powered “LED-based light tube,” Ivey345’s current limiting circuit as modified in accordance with Powell and, in the latter combination, Sadwick. EX1005, 2:50-56, 5:33-35; EX1006, ¶[0010]; EX1008, ¶[0080]; EX1009, 1:18-22; §VII.C.3; EX1002, ¶165.

(h) Limitations [1a]-[1b]

See §§VII.A.6(i)-VII.A.6(j), VII.B.4(h), VII.C.3.

(i) Limitation [1c]

Ivey813’s tube receives mains AC power from fixture 11 and, using power converter 36’s rectifier circuit—i.e., Ivey345’s rectifier 120 (“rectifying circuit”)—rectifies such power “to a DC wave” (“coupled to the external connection terminals,

for rectifying the external driving signal to produce a rectified signal”). EX1005, 2:51-56, 5:36-39; EX1006, ¶¶[0012], [0015]-[0016]; §VII.C.3; EX1002, ¶167.

(j) Limitation [1d]

Ivey345’s rectifier 120 includes “a smoothing capacitor” for filtering the rectified DC power (“filtering circuit, coupled to the rectifying circuit, for filtering the rectified signal to produce a filtered signal”). EX1006, ¶[0015]; EX1002, ¶168; *see also* EX1005, 5:36-39.

(k) Limitation [1e]

Ivey345’s current limiting circuit includes auxiliary power supply 125 (“driving circuit”), which is directly powered by rectifier 120 (and thus its smoothing capacitor) (“coupled to the filtering circuit”) over device power rail 145 and supplies voltage (“for converting the filtered signal into a driving signal”) for detector 150, comparator 170, Powell’s RC oscillator, and other components in the current limiting circuit. EX1006, ¶¶[0016]-[0019], [0024], [0029], [0031]; EX1009, 7:23-35; §VII.C.3; EX1002, ¶169.

(l) Limitation [1f]

See §§VII.A.6(k), VII.B.4(h), VII.C.3. Further, whether current flows through the LEDs—and thus whether the LEDs emit light—is determined by, e.g., detector 150, comparator 170, and Powell’s RC oscillator, which are powered by auxiliary power supply 125’s supply voltage (“coupled to the driving circuit, for

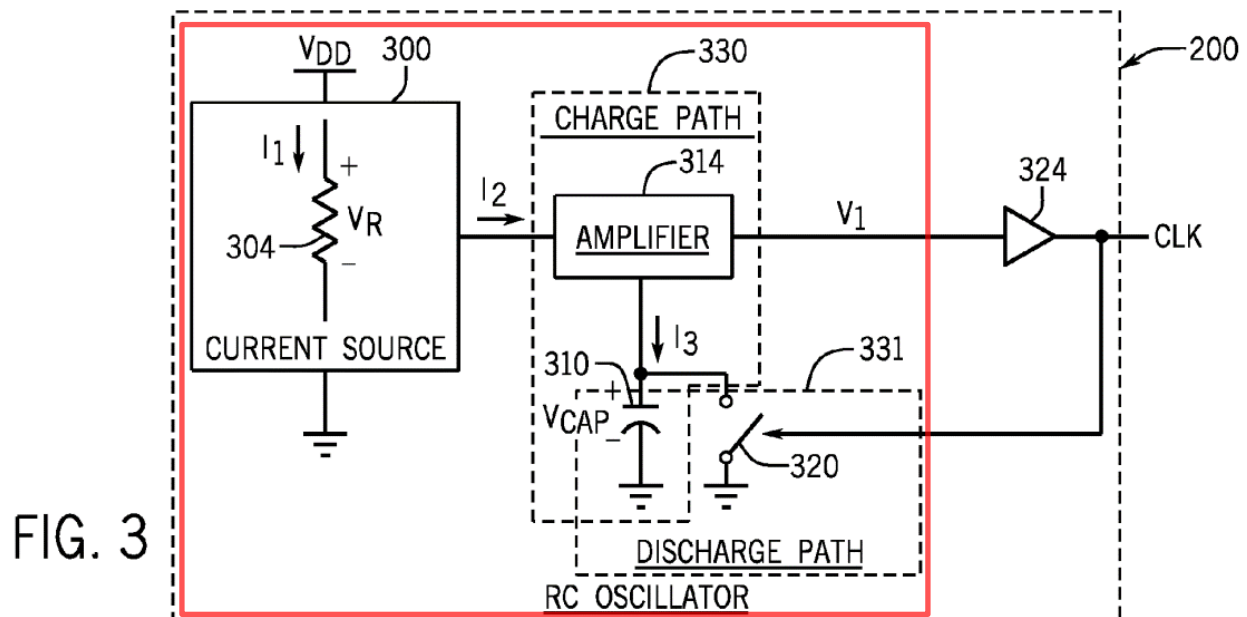
emitting light based on the driving signal”). EX1005, 3:23-37, 3:43-47, 5:33-35; EX1006, ¶¶[0010], [0016]-[0019], [0024], [0029]; EX1009, 7:23-35; §VII.C.3; EX1002, ¶170.

(m) Limitation [1g]

Ivey345’s current limiting circuit (“installation detection module”) detects whether a normal or fault configuration exists. EX1006, ¶¶[0010], [0013]; §VII.C.3; EX1002, ¶171.

(n) Limitation [1h]

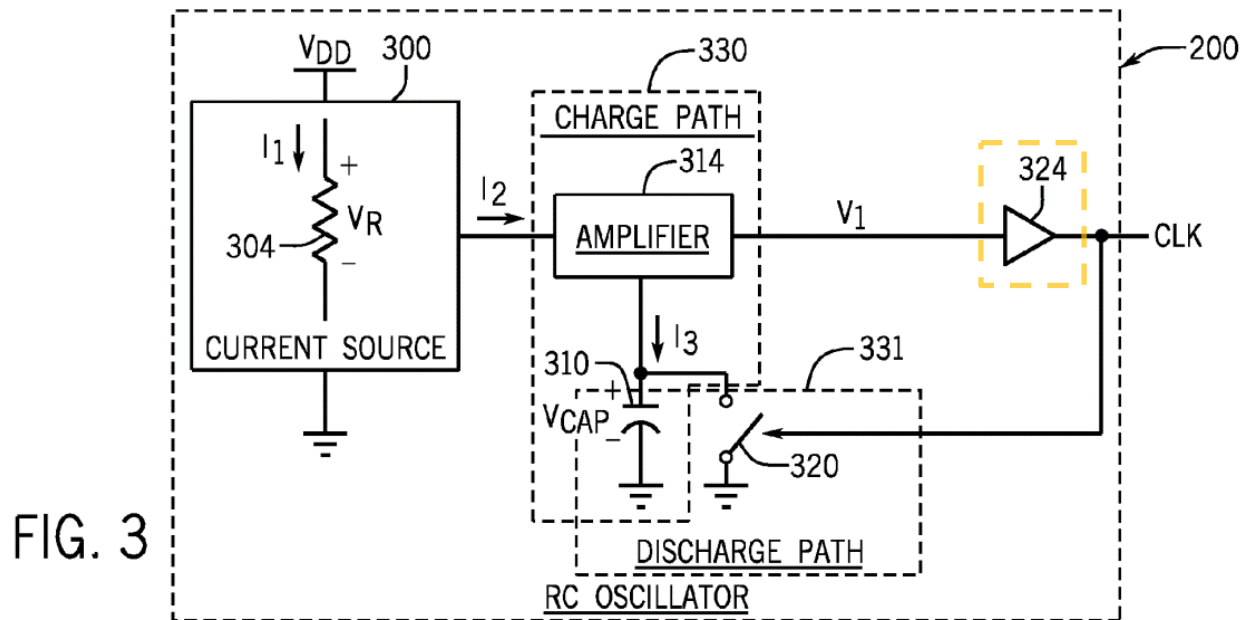
Powell’s RC oscillator generates an oscillating signal V_1 and includes switch 320, which is a discharge path. EX1009, 5:23-39, 4:65-67; EX1002, ¶172. Excluding digital buffer 324, each of the RC oscillator’s other elements (solid-red) form the claimed “first circuit”:



EX1009, Fig.3; EX1002, ¶172; *see also* §VII.C.4(a).

(o) Limitation [1i]

The remaining buffer 324 (dotted-orange) forms the claimed “second circuit”:



EX1009, Fig.3, 6:1-5; EX1002, ¶173. As Powell teaches, buffer 324 receives the oscillating V_1 signal from amplifier 314 (“coupled to the first circuit and configured to receive...”) before pulse-shaping and outputting V_1 to other components such as switch 320 (“and output the pulse signal”). EX1009, 5:13-39, 6:1-5; EX1002, ¶173; *see also* §VII.C.4(c).

(p) Limitation [1j]

In the Ivey-UL1993-Powell Combination, test load switch 135, load switch 175, or both form the claimed “third circuit,” as test load switch 135 opens and closes in response to the oscillations of the clock signal (here, from Powell’s RC oscillator),

while load switch 175's activation is controlled by devices such as detector 150 that are synchronized—and thus controlling load switch 175 according to—the clock signal (“coupled to a power loop of the LED tube lamp and the second circuit and configured to determine whether to conduct the power loop according to the pulse signal”). *See* §§VII.A.6(p), VII.C.3; EX1002, ¶174.

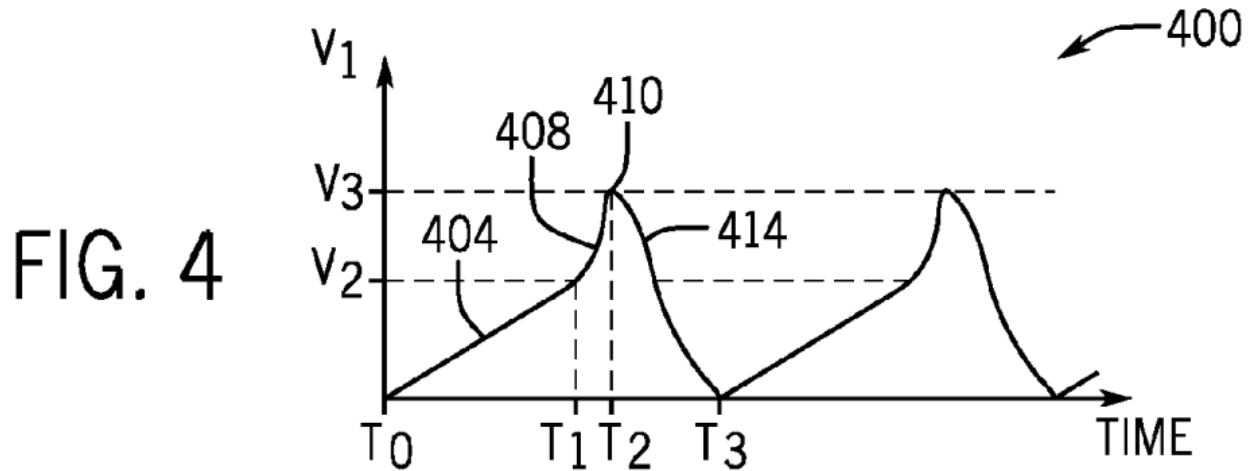
In the Ivey-UL1993-Sadwick-Powell Combination, load switch 175 forms the claimed “third circuit,” as test load switch 135 opens and closes in response to the oscillations of the clock signal from Powell's RC oscillator. *See* §§VII.B.4(m), VII.C.3; EX1002, ¶175.

(q) Limitation [1k]

V_1 is pulse-shaped and outputted to switch 320 of Powell's RC oscillator such that, once V_1 reaches a high logic level, the pulse-shaped V_1 signal causes switch 320 to conduct. EX1009, 5:29-39, 6:1-5; EX1002, ¶176; *see also* §VII.C.4(c).

(r) Limitation [1l]

By conducting switch 320, capacitor 310 discharges and V_1 decreases until reaching a low logic level, causing switch 320 to turn off and the oscillation cycle to repeat. EX1009, 5:29-39; EX1002, ¶177; *see also* §VII.C.4(d). This discharging part of the oscillation cycle occurs from T_2 to T_3 shown in Powell's Figure 4:



EX1009, Fig.4, 6:34-38; EX1002, ¶177; *see also* §VII.C.4(d).

(s) Claim 2

From T_2 to T_3 in Powell's Figure 4, the pulse-shaped V_1 signal turns on switch 302 and is therefore high, while the reverse is true from T_0 to T_2 . *See* EX1009, Fig.4, 6:34-38, 5:25-39; EX1002, ¶178; *see also* §VII.C.4(e).

(t) Claim 3

When V_1 reaches a low logic level at the end of the discharging part of the oscillation cycle, switch 302 is turned off. EX1009, 5:29-39; EX1002, ¶179; *see also* §VII.C.4(f).

(u) Claim 5

See §§VII.A.6(n), VII.B.4(k), VII.C.3. Here, detector 150, comparator 170, and Z test load 140 altogether form the claimed "fourth circuit," as these components detect variations on power rail 145 to determine whether a fault of normal

configuration exists. EX1006, ¶¶[0010], [0013], [0024]-[0026], [0030]-[0032], [0044]-[0045]; EX1008, ¶¶[0080], [0082]; EX1002, ¶180.

(v) Claim 6

More specifically, detector 150 outputs a signal representative of the detected variation to comparator 170, which compares the representative signal to the threshold signal and outputs a high signal when the representative signal is larger and a low signal when the representative signal is smaller. EX1006, ¶¶[0010], [0024]-[0026], [0030]-[0032], [0044]-[0045]; EX1008, ¶¶[0080], [0082]; §VII.C.3; EX1002, ¶181.

(w) Claim 7

Comparator 170's high signal output causes load switch 175 to remain closed. EX1006, ¶¶[0010], [0030]-[0032], [0041], [0044]-[0045]; EX1008, ¶¶[0080], [0082]; §VII.C.3; EX1002, ¶182.

(x) Claim 8

Comparator 170's low signal output turns off load switch 175. *See* §§VII.A.6(m), VII.B.4(j), VII.C.3; EX1002, ¶183.

(y) Claim 9

Comparator 170's low signal output turns off load switch 175, limiting current to a safe level—e.g., <5MIU. *See* §§VII.A.6(m), VII.B.4(j), VII.C.3; EX1002, ¶184.

(z) Claim 13

See §§VII.C.4(n), VII.C.4(q)-VII.C.4(r). For the same reasons that the discussed elements in Powell’s RC oscillator meet limitation [1h]’s “first circuit,” such elements meet claim 13’s “detection pulse generating module.” EX1002, ¶185.

(aa) Claim 14

See §VII.C.4(s).

(bb) Claim 15

See §VII.C.4(t).

VIII. DISCRETIONARY DENIAL IS UNWARRANTED

A. In View of the Litigation (35 U.S.C. §314(a))

Factor 1 is neutral. Petitioner has filed a motion to stay the Litigation pending a ruling on its motion to transfer venue, but the court has not yet ruled.

Factor 2 is neutral or weighs only slightly against institution. Trial is currently scheduled for April 17, 2024. EX1026. However, the Litigation involves 11 patents and the median time-to-trial for the Western District of Texas is 28.3 months,²⁶ meaning a first trial likely will not occur until at least October 2024—only 2 months before a decision here. Moreover, given that the Litigation currently

²⁶ <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/06/30-2>.

includes 11 patents, time-to-trial is highly likely to *exceed* the median, and the Litigation is highly likely to be split into multiple trials extending over a period of additional months.

Factor 3 favors institution. The Litigation is in its early stages. PO filed its original complaint on May 24, 2022, and amended its complaint in September 2022 to add patents. Markman has been delayed until July 19, 2023, and fact discovery is ongoing, having only opened on April 20, 2023. EX1034; EX1019.

Factor 4 favors institution. Upon institution, Petitioner will stipulate not to rely on the same grounds in the Litigation. EX1027.

Factor 5. The parties are the same.

Factor 6 favors institution. This petition is filed within the 12-month statutory period²⁷ and, as shown above, the proposed grounds' merits are compelling.²⁸

B. In View of the *Maxlite* Action (§314(a))

With respect to *Fintiv*, a key underlying concern is whether institution will result in an inefficient use of judicial resources due to “duplication of work.” 5-6 &

²⁷ The '174 Patent is just one of eleven patents asserted by PO and the ninth of eleven petitions Petitioner will ultimately be forced to prepare and file.

²⁸ See https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf

n.7. However, because Petitioner is not a party or related to any party in the *CH* Action, Petitioner's invalidity arguments over the '174 Patent have not yet been—but nevertheless will be—tried and adjudicated, regardless of the *Maxlite* Action. In other words, it is inevitable that judicial resources will be expended on Petitioner's invalidity arguments, either here or otherwise the Litigation, and thus discretionarily denying this Petition will not preserve or optimize expenditure of judicial resources. And PO cannot assert unfairness in allowing Petitioner to mount such a defense because PO voluntarily sued Petitioner in the Litigation after and separate from the *Maxlite* Action. Discretionary denial in view of the *Maxlite* Action is therefore unwarranted.

C. In View of the Prosecution History (§325(d))

Ivey813, Ivey345, and Powell were not considered during prosecution (*see* EX1003, 180/389, 476-480/389), meaning Grounds 1-4 do not present substantially the same prior art or arguments previously presented to the Office.

Should PO argue otherwise, particularly for this Petition's arguments regarding Office-considered Sadwick/Sadwick566 (*see* EX1003, 147-51/389), unconsidered Ivey345 discloses a pulse generating circuit that outputs pulse signals to cause a power loop to be conductive (*see* §VII.A.6(c)), and limiting the power loop current to, e.g., <5MIU (*see* §VII.A.6(f)), which were features the Office found lacking in the prior art—particularly, Sadwick—when allowing the claims (*see*

EX1003, 346-48/389, 281-85/389, 234/389). If a showing of Office error is required, that error is failing to consider these teachings of Ivey³⁴⁵. And the Office further erred by allowing the claims despite Applicant's erroneous argument that Sadwick discloses only LED tube lamps "powered by ballasts" (*see id.*, 281-82/389, 286-88/389), as Sadwick explicitly states that its FLR may accept "an AC lines input" (EX1008, ¶¶[0173], [0175], [0061]).

IX. CONCLUSION

For the above reasons, institution is appropriate.

Dated: June 9, 2023

/Eagle H. Robinson/

Eagle H. Robinson (Reg. No. 61,361)

Lead Counsel for Petitioner

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a)(1)(i), the undersigned certifies that this Paper—exclusive of the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, this certificate off word count, appendix of exhibits, and claim listing—includes 13,980 words based on the word count of the word-processing system used to prepare the paper.

/Eagle H. Robinson/
Eagle H. Robinson (Reg. No. 61,361)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §42.6(e) and 37 C.F.R. §42.105(a), the undersigned certifies that on June 9, 2023, complete copies of this Petition for *Inter Partes* Review, Petitioner's power of attorney, and all exhibits were served on Patent Owner at the correspondence address of record listed below by USPS Priority Mail Express:

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