

Design of an Organic Pixel Addressing Circuit for an Active-Matrix OLED Display

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Abstract—In this paper, we present a design of a flat-panel display (FPD) based on organic light-emitting diodes (OLEDs) and on organic thin-film transistors (OTFTs). Addressing mode, circuit topology, layout, and drive scheme are developed in order to reach the desired frame rate and to control the gray levels against the threshold voltage dispersions of OTFTs and OLEDs. Our design shows that the current OLED and OTFT technology are suitable for FPD technology, though setting serious constraints on driver design.

Index Terms—Displays, plastics, thin film circuits.

I. INTRODUCTION

ORGANIC semiconductors can be deposited and processed into circuits at sufficiently low temperature to allow the use of large-area lightweight flexible plastic substrates. Those substrates make it possible for organic semiconductor devices to be manufactured in a roll-to-roll fashion, this being a continuous production process assumed to cost less than classical batch processes [1]. An important application for organic or “plastic” electronics are active matrix organic light-emitting diode (OLED) displays. To take advantage of plastic substrates, also the driving matrix should be manufactured at temperatures compatible with those substrates. One possibility is to use organic thin-film transistors (OTFT) for the addressing matrix. The integration of one OTFT with one OLED has already been demonstrated [2]–[4]. However, high-quality displays combining specifications regarding display uniformity, resolution, gray scales, power supply, frame rate, and others, require several driving transistors per pixel. In this work, we perform some first-order calculations to assess the use of OTFTs for active matrix OLED displays. Based on those calculations, some design issues are addressed. It is shown that state-of-the-art OTFTs can be used as driving elements in OLED displays. Without further improvements on organic semiconductors and related process technology, the design space is relatively small, though. This work can be used to set a goal for future OTFT development.

II. ASSUMPTIONS

To be able to do simulations and calculations, we have made some assumptions based on values found in literature.

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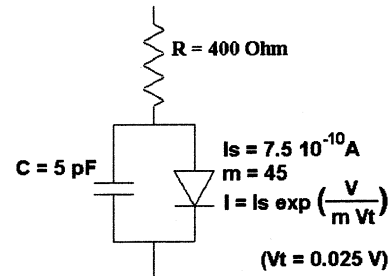


Fig. 1. Model for OLED [12]. The parameter values are obtained by fitting experimental data in the working area of the OLED. The high nonideality factor m shows that this model has no physical background, but is a parametric model. The values are typical for an OLED with area $150 \mu\text{m} \times 150 \mu\text{m}$ and a thickness of the organic layers of 80 nm.

For OTFTs, we used state-of-the-art performance values for pentacene transistors on glass substrates. Hole mobilities higher than $\mu > 1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ have been reported [5], while typical pentacene thin-film transistors do not conduct electrons. Therefore, in simulations and calculations we have taken a value of $1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for the hole mobility and all circuits are based on p-type OTFTs. For the threshold voltage V_T a value of -1 V is reasonable. The I_{ON}/I_{OFF} ratio can be 10^7 . A value of 200 nm is typical for the dielectric thickness. In addition we have neglected the OTFT overlap capacitances, assuming a self-aligned OTFT fabrication process. For SPICE simulations we used the level 3 MOSFET model.

For OLEDs, a typical value for the external quantum efficiency η is 1%. For this efficiency a current density of 20 mA/cm^2 is sufficient to obtain a luminance of 100 cd/m^2 for red and blue OLEDs. For green OLEDs even less current is necessary. For an OLED of $100 \times 100 \mu\text{m}$ the current required for maximum brightness is then $2 \mu\text{A}$. The electron and hole transport and injection phenomena in organic multilayers are not yet fully understood. Recent publications show that the current density versus voltage characteristics are dominated by bulk properties [6]. The equations derived are very complicated and hard to model in SPICE. In addition the transient characteristics of the OLED do not influence much the working of the pixel addressing circuit proposed here. Therefore the OLED can in first order be replaced by a series resistance and a capacitance in parallel with a diode, as shown in Fig. 1. This model, from [12], will be further used in calculations.

A frame rate of 100 Hz is assumed. For an active matrix containing 1000 rows, the selection time per row is then only $10 \mu\text{s}$.

Finally the pixel area is assumed to be $100 \times 100 \mu\text{m}$ and the power supply 25 V.

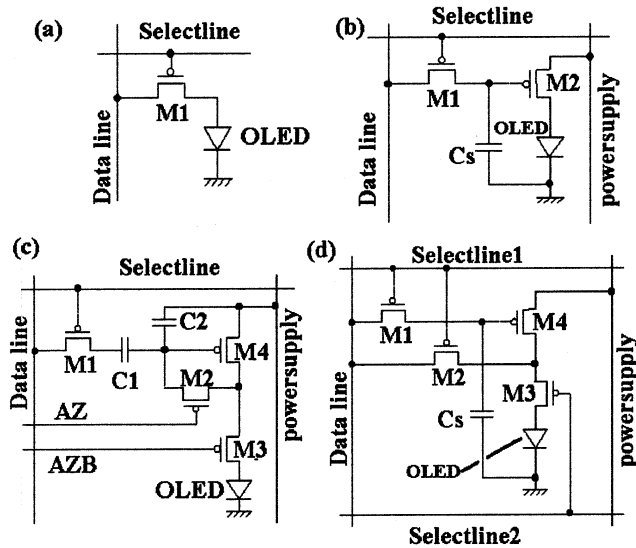


Fig. 2. Different configurations for pixel addressing circuits. (a) One transistor configuration. (b) Two transistor configuration. (c) Voltage driven four transistor configuration. (d) Current driven four transistor configuration.

III. ADDRESSING MODE

Because the luminance of an OLED is proportional to the current density flowing through it, an OLED has to be current driven.

The simplest way to address a matrix array of OLEDs is by passive matrix addressing. In this addressing mode the rows are selected one by one. When a row is selected a current is imposed to each pixel of that row to obtain the desired brightness. The main disadvantage of passive matrix addressing is the high current densities needed for high peak luminance. These high current densities limit the maximum number of rows and columns on the one hand and the lifetime of the OLEDs on the other hand. Another disadvantage of passive matrix addressing is cross-talk. The brightness nonuniformity caused by the onset voltage dispersion of the OLEDs is also an important disadvantage of passive matrix addressing.

Several authors have already stressed the advantages of active matrix addressing as compared to passive matrix addressing [7]. Active matrix addressing means that one or more active devices, in our case OTFTs, are added to each pixel. The disadvantages of pixel driver circuits based on one or two TFTs have already been emphasized in several publications [7]–[9]. In the one-TFT configuration [Fig. 2(a)] a data current is imposed to the OLED. This configuration requires high peak luminance similar to the passive matrix addressing. Moreover, the source of brightness nonuniformity has now shifted to the threshold voltage dispersion of the OTFTs. In the two-TFT configuration [Fig. 2(b)] a voltage is imposed to the gate of a driving transistor M_2 during selection and this voltage is stored on a capacitance C_S . Although this configuration has a built-in memory and therefore does not require high peak luminance, this configuration suffers from TFT threshold voltage dispersion as well, leading to brightness nonuniformity.

To improve the brightness nonuniformity several pixel driver circuits based on four poly-Si TFTs have been proposed [9]–[12]. In the present paper, these circuits will be evaluated

with organic TFTs instead of poly-Si TFTs. Also these circuits can be divided into two categories: voltage driven circuits and current driven circuits.

The working principle of the voltage driven circuits [Fig. 2(c)] is the use of an auto zero cycle to reference the data against the OTFT threshold voltage, eliminating the effect of the OTFT threshold voltage dispersion. The main problem is that this auto zero cycle is slow when a large number of gray levels is demanded, because M_4 has to turn itself off. The necessary accuracy of the auto zero cycle is determined by the smallest step in gate-source voltage of the drive transistor to obtain the desired number of gray levels. To obtain 128 gray levels, the step in current is 16 nA. The smallest step in gate-voltage is then 27 mV. Our SPICE simulations show that in this case the auto zero cycle takes 980 μ s. A solution to accelerate this circuit is the use of a more complex drive scheme. It is possible to spread out the auto zero cycle over more selection times by already turning off the pixel when other pixels are selected. If pixel i is turned off when pixel $i-98$ is selected, the auto zero cycle will be sufficiently accurate when the data for pixel i arrives. The disadvantage of this drive scheme is that the pixel is off during 980 μ s of the frame time (10 ms), i.e., 9.8%. This means that higher luminance is required and thus higher current densities.

The working principle of the current driven circuits is the programming of the gate-source voltage of the drive transistor by a data current. An example circuit was presented by Hattori *et al.* [10]. We present a modified version of this circuit in Fig. 2(d). Compared to the circuit of [10], we added an extra selection line to increase the linearity of the circuit and we placed the OLED between the drain of M_3 and the ground to cancel out the OLED transient characteristics. During selection of the pixel (M_1 and M_2 open) a data current is imposed (through M_2) to the drive transistor M_4 . The feedback loop through M_2 and M_1 settles the necessary gate-source voltage to drive the data current through drive transistor M_4 , independently of the threshold voltage of this transistor. In this way the threshold voltage dispersions are cancelled out. The gate-source voltage of M_4 is stored on a capacitance C_S . The settling of the gate-source voltage of the drive transistor V_{G4} is a slow process. A large part of the settling data current imposed by the data line flows through the drive transistor and hence only a small part $-C_S \cdot \delta V_{G4}(t)/\delta t$ can be used to charge the capacitance C_S . The time t needed to charge C_S starting from V_0 to V can be solved from the conservation of this data current and is given by (1), where V_{TARGET} is the desired gate voltage imposed by the data current. V_{DD} is the power supply, V_T is the threshold voltage of the drive transistor and $C_{DATA LINE}$ is the capacitance of the data line including C_S . K_P is the transconductance parameter of the OTFT. K_P is given by $\mu \cdot C_{OX}/2$: see (1), shown at the bottom of the next page. The time needed to charge a $C_{DATA LINE}$ of only 1 pF starting from a maximum bright pixel ($I_{OLED} = 2 \mu$ A, $V_0 = 16$ V) to a minimum bright pixel ($I_{OLED} = 16$ nA, $V_{TARGET} = 23.5$ V) with an accuracy of 27 mV ($V = 23.473$ V) is 128 μ s. The time to charge C_S starting from a maximally bright pixel ($I_{OLED} = 2 \mu$ A, $V_0 = 16$ V) to an off pixel ($I_{OLED} = 0$ nA, $V_{TARGET} = 24$ V) with an accuracy of 27 mV ($V = 23.973$ V) is 1.25 ms. The solution to accelerate this circuit is to use the

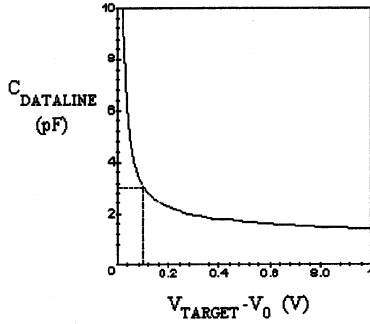


Fig. 3. Maximum capacitance of the data line that allows current driven charging of a voltage $V_{TARGET} - V_0$ (V_0 is $V_{PRECHARGE}$, the voltage precharged during the first part of the selection) on the gate of M_4 within a frame time (10 μ s). The target voltage is 16.00 V according to the maximum current and thus maximum brightness. The accuracy is 13.5 mV, i.e., half the minimum step of the gate voltage. For a data line capacitance of 3.4 pF, the drive current can charge 80 mV within 10 μ s.

more complex drive scheme presented in the following paragraph.

IV. DRIVE SCHEME

The drive scheme presented here divides the selection time into two parts, a voltage driven part and a current driven part. In the first part, the gate of drive transistor M_4 is precharged with a voltage estimated to make M_4 drive the desired current through the OLED. This voltage does not take the threshold voltage dispersion into account. The voltage charging is faster than the current charging could be. In the second part, the drive current only has to charge a small voltage variation ΔV on the gate of M_4 , i.e., the threshold voltage dispersion of M_4 , ΔV_{T4} . Since the voltage on the gate of M_4 is almost exact at the beginning of the second part of the selection time, most of the drive current will be used to flow through M_4 . Only a small part will be used to charge the remaining part of the necessary gate voltage. Within a frame time T_f the voltage that can be charged is limited by the capacitance of the data line. This is shown in Fig. 3, which is obtained out of (1). A realistic minimal value for the dataline capacitance will be shown in the next paragraph to be 3.4 pF. For such data line capacitance of 3.4 pF, it can be read from Fig. 3 that the maximum threshold voltage dispersion of M_4 is 0.08 V. The expected threshold voltage dispersions are of the order of a few Volts. Therefore this drive scheme is not sufficient to compensate for the threshold voltage dispersions.

This drive scheme does however become sufficient if a memory function is added to it. After the second part of the selection time, the voltage variation charged by the drive current, ΔV , can be measured and stored in an external memory. The next time the pixel is selected, the value in the memory can be added to the precharge voltage, which will become more

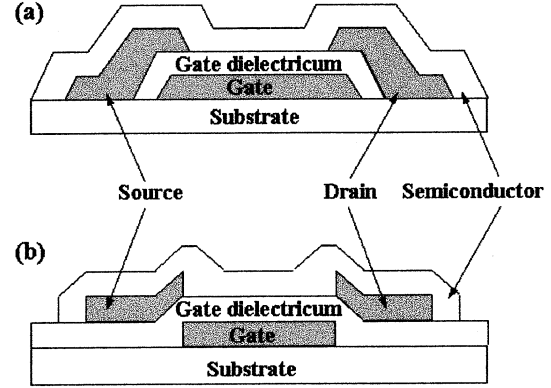


Fig. 4. Two transistor structures. (a) Not self-aligned fabrication process. (b) Self-aligned fabrication process.

precise. Again ΔV is measured and added to the value in the memory. After a few selections the value in the memory equals quite accurately the threshold voltage dispersion of M_4 . As a result, the precharge voltage will be very accurate and during the second part of the selection time the drive current has to adjust the gate voltage only slightly. This little adjustment can be done within a frame time. From (1), it can be calculated that if the precharge voltage has an accuracy of 15 mV, the capacitance of the data line can be as high as 60 pF.

This operation mode strengthens the need for a current driven circuit, because in a voltage driven circuit the pixel threshold voltage dispersion cannot be measured externally.

V. CONTROL LINES

A control line controls at least one transistor per pixel. Therefore the gate-source and gate-drain capacitances of the transistors have to be as small as possible. In a nonself-aligned transistor fabrication process [Fig. 4(a)], the gate-source and gate-drain overlaps can be large. Assuming a 10 μ m resolution process that results in an overlap of 10 μ m, an oxide thickness is 200 nm and a transistor width of 50 μ m, the gate-source overlap capacitance, C_{GS} , is 75 fF. For 1000 rows, this results in 150 pF per data line, which is far too large. In a self-aligned transistor fabrication process [Fig. 4(b)] this capacitance is smaller. In the ideal case, there is only a fringing capacitance. If the thickness of the gate metal is 50 nm, the oxide thickness is 100 nm and the transistor width is 50 μ m, then C_{GS} is 0.38 fF. For 1000 rows, this makes a reasonable 0.38 pF per data line. Several self-aligned processes can be conceived; one example is given in [13], where the self-aligned transistor structure is fabricated by lithography with illumination through the substrate.

The RC constant of the select lines has to be small in order to select the pixels fast. This determines the material choice for the select lines. Indium tin oxide (ITO) has a typical sheet resistance of $R_{SCR} = 10 \Omega/\text{square}$. For a line width of 10 μ m,

$$t = \frac{1}{2} \cdot \frac{\ln \left(\frac{(V_0 - V_{TARGET}) \cdot (V + V_{TARGET} - 2 \cdot V_{DD} - 2 \cdot V_T)}{(V - V_{TARGET}) \cdot (V_{TARGET} - 2 \cdot V_{DD} - 2 \cdot V_T + V_0)} \right) \cdot C_{DATA LINE}}{K_P \frac{W_4}{L_4} (-V_{TARGET} + V_{DD} + V_T)} \quad (1)$$

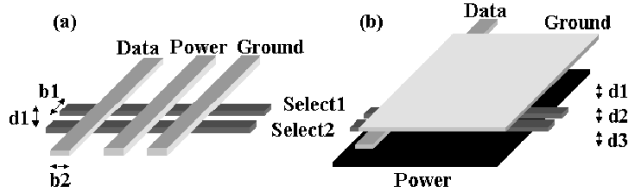


Fig. 5. Different configurations of the control lines. (a) Power and ground are patterned. (b) Power and ground are not patterned.

a three-color pixel of width $300\ \mu\text{m}$ (three subpixels each with a width of $100\ \mu\text{m}$) and 1000 rows, the line resistance is $300\ \text{k}\Omega$. For an RC constant of $0.25\ \mu\text{s}$ (2.5% of the selection time), the line capacitance should only be as small as $0.83\ \text{pF}$. This is not achievable. If the select lines are made of gold or copper ($R_{SCR} \cong 0.1\ \Omega/\text{square}$) the line capacitance can be as large as $83\ \text{pF}$.

The voltage drops over the power supply line and ground have to be small in order not to limit the power dissipation. If all pixels in a column are on maximum brightness, a current of $2\ \text{mA}$ flows through the power supply lines (for 1000 rows). For a regular ITO line with line width of $10\ \mu\text{m}$ the voltage drop is $300\ \text{V}$. Thus, also the power supply lines should be made of metal. For gold or copper, the voltage drop is only $3\ \text{V}$. If the power can be supplied by a layer of conductive material spread over the complete display area, the voltage drop can be further reduced by a factor of 10. In that case, a thick layer of ITO can also be considered to be a viable option.

Fig. 5 shows possible configurations for control lines, ground and power. Fig. 5(b) depicts the situation where ground and power are planes, while data and select are lines. In that case, the capacitances of the data line and select line are given by respectively (2) and (3), where b_1 is the width of the select lines, b_2 is the width of the data line, d_1, d_2 and d_3 are the vertical distances between the control lines and ground and power planes, N is the number of rows and B is the width of one subpixel. We propose as realistic values: $b_1, b_2 = 10\ \mu\text{m}$, $N = 1000$ rows, $B = 100\ \mu\text{m}$, $C_{GS} = 0.77\ \text{fF}$, $C_S = 1\ \text{pF}$ (for $I_{ON}/I_{OFF} = 10^7$) and $d_1, d_2, d_3 = 5\ \mu\text{m}$ of an insulator like benzocyclobutene (BCB, $\epsilon_r = 2.6$). Using these values, the capacitances are respectively $C_{DATALINE} = 24.2\ \text{pF}$ and $C_{SELECTLINE} = 24.4\ \text{pF}$. With these values the drive scheme with memory function presented earlier in this paper is applicable if the accuracy of the precharge part of the selection is $17\ \text{mV}$.

$$C_{DATALINE} = \left(2 \cdot \frac{b_1 \cdot b_2 \cdot \epsilon_0 \cdot \epsilon_r}{d_2} + 2 \cdot C_{GS} \right) \cdot N + C_S + \frac{b_2 \cdot 3 \cdot N \cdot B \cdot \epsilon_0 \cdot \epsilon_r}{d_1} + \frac{b_2 \cdot 3 \cdot N \cdot B \cdot \epsilon_0 \cdot \epsilon_r}{d_2 + d_3} \quad (2)$$

$$C_{SELECTLINE} = 3 \cdot \left(\frac{b_1 \cdot b_2 \cdot \epsilon_0 \cdot \epsilon_r}{d_2} + C_{GS} \right) \cdot N + \frac{b_1 \cdot 3 \cdot N \cdot B \cdot \epsilon_0 \cdot \epsilon_r}{d_3} + \frac{b_1 \cdot 3 \cdot N \cdot B \cdot \epsilon_0 \cdot \epsilon_r}{d_1 + d_2} \quad (3)$$

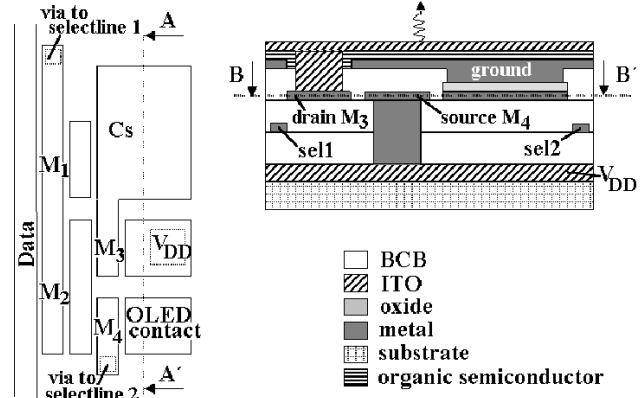


Fig. 6. Layout of the pixel driver circuit. (a) Top view BB' of the layout. (b) Side view AA' of the layout.

If the power supply line and the ground line are patterned [Fig. 5(a)], which complicates the fabrication and increases the series resistance and hence the heat dissipation, the capacitances can be smaller. For the previous technological example, they become respectively $C_{DATALINE} = 3.4\ \text{pF}$ and $C_{SELECTLINE} = 6.45\ \text{pF}$. Thus, even in this case the more complex drive scheme with memory function has to be applied.

VI. LAYOUT

To obtain a three-color pixel, three subpixels have to be placed adjacent to each other. The different colors can be obtained by e.g., filtering a white light-emitting OLED by color band pass filters or by e.g., using different light emitting organic layers [14]. The length:width relation is assumed to be 3:1. This is accomplished by the layout presented in Fig. 6. Neither the power supply nor the ground are patterned in order to ease the fabrication and reduce the heat dissipation. The control lines are separated by a $5\ \mu\text{m}$ thick layer of BCB in order to obtain small line capacitances. We assume self-aligned source/drain electrodes with respect to the drain, e.g., by illumination through the substrate [13], to minimize gate-source overlap capacitances. To allow this, we assume the power supply layer to be made of a thick layer of ITO. The select line and nonselect line lay at the outside of the pixel area in order not to shade the illumination. Finally the OLED is placed on top of the circuit. This implies the use of top-emitting OLEDs [15], [16].

VII. CIRCUIT DIMENSIONING

In this paragraph, we derive the minimum power supply and the dimensions the OTFT pixel engine. We also evaluate the limitations to the display resulting from the use of OTFTs.

The power supply, V_{DD} , has to be large enough to support the current for maximum brightness, $I_{OLEDMAX}$, given that M_4 will have to work in saturation regime and M_3 is working in triode regime. This results in a first boundary condition, expressed by (4), where $V_{OLEDMAX}$ is the voltage drop across the OLED necessary to support $I_{OLEDMAX}$.

$I_{OLEDMAX}$ is proportional to the luminance, H_G and to the area of the pixel, O_{PIX} . This relationship is expressed in (5), where K is typically $2\ \text{A/cd}$ for the emission of Alq_3 .

The area of the pixel, O_{PIX} , can be derived from Fig. 6 as follows.

There are two requirements for the size of C_S . First, C_S has to be large enough to ensure that the charge redistribution of C_S to C_{GS1} (gate-source capacitance of M_1) at the end of the selection time does not introduce an error larger than 27 mV (the smallest step in gate voltage for 128 gray levels). Secondly, C_S has to be large enough to ensure that the leakage voltage during the time the pixel is not selected is smaller than 27 mV. The latter requirement is the most stringent one. For $I_{ON}/I_{OFF} = 10^{-7}$ and a safety margin of 5, C_S has to be larger than 1 pF. For $\epsilon_r = 3.5$, t_{OX} (insulator thickness for C_S) = 100 nm and the lithographically determined minimum dimension = 10 μm , C_S has an area of 40 $\mu\text{m} \times 80 \mu\text{m}$.

M_1 has to charge C_S in half the selection time with its source-drain current I_1 that will induce a change in V_{G4} as $I_1 = C_S \cdot \delta V_{G4}(t)/\delta t$. Solving this equation and demanding that I_1 is large enough to charge C_S within the time $T_f/2N$ even for the toughest case, leads to the requirement of (6) for W_1/L_1 . Here V_0 is the start value of the gate voltage of M_4 , V_{DATA} is the voltage on the data line and wanted to be charged on the gate of M_4 and V_{G4} is the resulting gate voltage of M_4 after half the selection time. The toughest charging is the charging of a maximal bright pixel to a darkest pixel. For $V_{DD} = 37$ V this means that $V_{DATA} = 36$ V, $V_0 = 28$ V. As shown in paragraph V the accuracy of the precharge phase should be 17 mV, thus $V_{G4} = 35.983$ V. This leads to the requirement $W_1/L_1 > 2.4$. For $V_{DD} = 19$ V, $W_1/L_1 > 5$. M_1 is thus shorter than C_S . As M_1 is placed adjacent to C_S , it will not determine the size of the pixel, O_{PIX} .

For M_2 the following reasoning applies. During selection of the pixel, M_4 should be in the saturation regime. Therefore the drain-source voltage of M_2 should be smaller than V_{T4} . This leads to the requirement of W_2/L_2 specified in (7).

The area of the pixel, O_{PIX} , is thus influenced by the dimensions of M_2 , M_3 , and M_4 . Depending on the voltage supply and the current, either the width of M_2 or of $M_3 + M_4$ determines the length of the pixel. In the case that M_2 determines the length of the pixel, the area O_{PIX} is given by (8). We assume that the lithographically determined minimum dimension is D . One space D is foreseen between M_2 and C_S , each control line has width D and at each side of a pixel there is an $D/2$ separation to the adjacent pixel. This amounts to a fixed $4D$ in (8). Taking into account the ratio 1:3 for the pixel width:length, (8) is obtained. In the case that M_3 and M_4 determine the length of the pixel, the area is given by (9):

$$V_{DD} > \sqrt{(V_T + V_{OLEDMAX})^2 + 2 \frac{I_{OLEDMAX}}{K_P \frac{W_3}{L_3}}} + \sqrt{\frac{I_{OLEDMAX}}{K_P \frac{W_4}{L_4}}} - V_T \quad (4)$$

$$I_{OLEDMAX} = K \cdot H_G \cdot O_{PIX} \quad (5)$$

$$\frac{W_1}{L_1} > \frac{\ln \left(\frac{(V_0 - V_{DATA}) \cdot (V_{DATA} + 2 \cdot V_T + V_{G4})}{(V_{G4} - V_{DATA}) \cdot (V_{DATA} + 2 \cdot V_T + V_0)} \right) \cdot C_S \cdot N}{K_P \cdot (V_{DATA} + V_T) \cdot T_f} \quad (6)$$

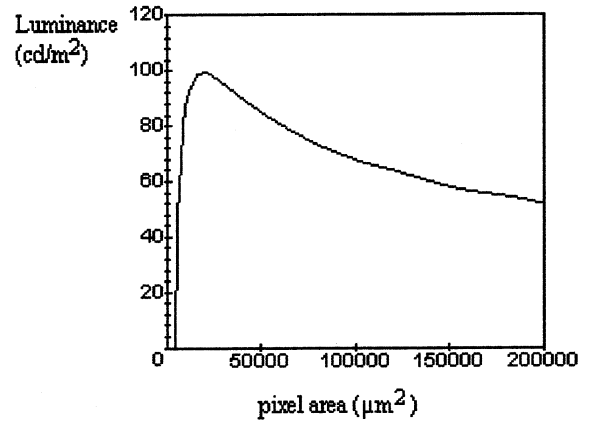


Fig. 7. Luminance as a function of pixel area. The gate length is 10 μm and the supply voltage is 37 V.

$$\frac{W_2}{L_2} > \frac{I_{OLEDMAX}}{2 \cdot K_P \cdot V_T \cdot \left(\sqrt{\frac{I_{OLEDMAX}}{K_P \frac{W_4}{L_4}}} - V_{DD} - \frac{3 \cdot V_T}{2} \right)} \quad (7)$$

$$O_{PIX} = \frac{1}{3} \left(\left(\frac{W_2}{L_2} + 4 \right) \cdot D + 80 \cdot 10^{-6} \right)^2 \quad (8)$$

$$O_{PIX} = \frac{1}{3} \left(\left(2 \cdot \frac{W_4}{L_4} + 5 \right) \cdot D + 80 \cdot 10^{-6} \right)^2 \quad (9)$$

From the set of (4) to (8)–(9), we can derive the achievable luminance H_G as a function of the pixel area. An example is shown in Fig. 7. This figure is calculated for the minimum supply voltage necessary to obtain a luminance of 100 cd/m^2 for a gate length of 10 μm . This + supply voltage is 37 V. Fig. 7 shows that there is a maximum in luminance for a certain pixel area. This can be explained as follows. The transistor width scales with the square root of the area while the channel length remains fixed at 10 μm . The OLED current on the other hand scales proportional with the pixel area. For a smaller pixel area a larger current per unit area is possible and hence a larger luminance is possible. The luminance is thus increasing for decreasing pixel area. However, for a very small pixel area, almost the complete area is occupied by the constant area of C_S , which does not scale with the gate length. The ratio W/L becomes zero, and thus, also the current and the luminance become 0. The area of the pixel at which the luminance is maximal is 245 $\mu\text{m} \times 82 \mu\text{m}$. The sizes of the transistors are $W_1/L_1 = 3.75$, $W_2/L_2 = 12.5$, $W_3/L_3 = W_4/L_4 = 2.65$. The current for maximum brightness, $I_{OLEDMAX}$, is 4 μA .

Keeping the pixel area constant, the influence of the supply voltage can be seen in Fig. 8: increasing V_{DD} allows higher luminance. For small V_{DD} , the dimensions of M_3 and M_4 determine the relationship between pixel area and luminance; for larger V_{DD} , M_2 determines this relationship.

Fig. 9 shows a similar picture, but assuming a technology with minimum dimensions and gate length of 5 μm and a pixel area of 203 $\mu\text{m} \times 68 \mu\text{m}$. For a luminance of 100 cd/m^2 the length of the pixel is determined by the sum of the sizes of M_4 and M_3 . A power supply of only 19 V is needed. The sizes of the transistors are $W_1/L_1 = 3.75$, $W_2/L_2 = 15.7$, $W_3/L_3 = W_4/L_4 = 10.8$. The current for maximum brightness, $I_{OLEDMAX}$, is 2.75 μA .

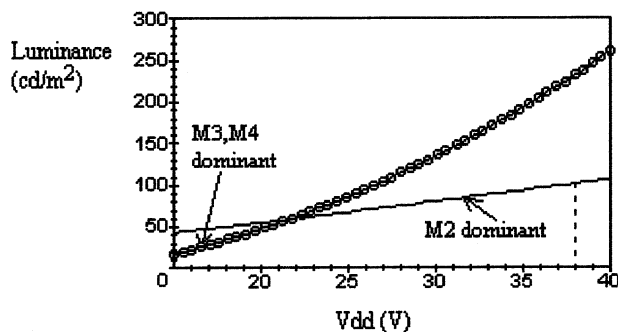


Fig. 8. Luminance as a function of supply voltage. The gate length is $10\ \mu\text{m}$ and the pixel area is $20\,000\ \mu\text{m}^2$ ($245\ \mu\text{m} \times 82\ \mu\text{m}$). The circles are calculated with M_3 , M_4 dominant and the solid line is calculated with M_2 dominant. The lowest line applies. Up to $V_{DD} = 22\ \text{V}$ M_3 , M_4 are dominant, while above $22\ \text{V}$, M_2 is dominant. To obtain $100\ \text{cd/m}^2$ a supply voltage of $37\ \text{V}$ is necessary.

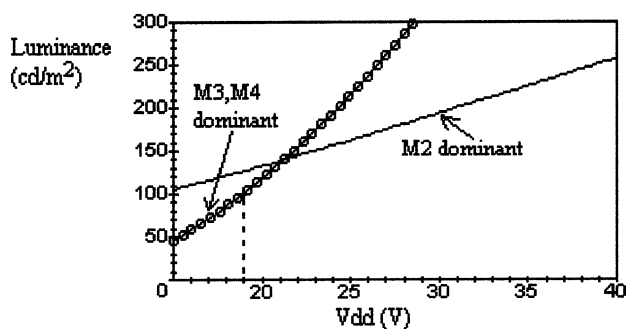


Fig. 9. Luminance as a function of supply voltage. The gate length is $5\ \mu\text{m}$ and the pixel area is $13\,800\ \mu\text{m}^2$ ($203\ \mu\text{m} \times 68\ \mu\text{m}$). The circles are calculated with M_3 , M_4 dominant and the solid line is calculated with M_2 dominant. The lowest line applies. Up to $V_{DD} = 21\ \text{V}$ M_3 , M_4 are dominant, while above $21\ \text{V}$, M_2 is dominant. To obtain $100\ \text{cd/m}^2$ a supply voltage of $19\ \text{V}$ is necessary.

VIII. DISPLAY SIZE

As the number of pixels increases, the capacitances of the control lines increase; see (2) and (3). The available selection time per pixel decreases. If the selection time decreases, $C_{\text{DATA LINE}}$ must also decrease; see (1). The accuracy of the precharge therefore must increase when the number of pixels—hence the size—of the display increases. This relationship is calculated in Fig. 10. From this figure it can be seen that for an accuracy of $17\ \text{mV}$ the number of pixels can be 1100. For pixels with a width of $300\ \mu\text{m}$, the display size is limited to $33\ \text{cm}$. Fig. 10 shows the importance of a very accurate voltage driven part of the selection time. If the accuracy is $15\ \text{mV}$, then the number of pixels can be 1500. For pixels of width $300\ \mu\text{m}$, this limits the display size to $45\ \text{cm}$.

For this size the series resistance of the select line is still sufficiently small. The series resistance is $4.5\ \text{k}\Omega$ and the capacitance of the select line is $36\ \text{pF}$. This leads to an RC constant of $162\ \text{ns}$, which is still only 2.4% of the selection time.

IX. CONCLUSION

We have presented a feasibility study on full-plastic displays, where both the pixel addressing circuit and the light-emitting device consist of organic semiconductors. The two main problems in organic pixel driver design are the threshold voltage dispersions of OTFTs and OLEDs on the one hand and the speed

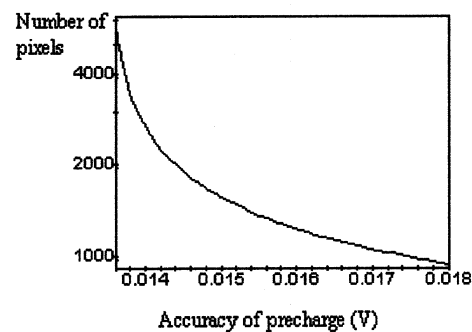


Fig. 10. Number of pixels versus the accuracy of the voltage driven precharge part of the selection. A gate length of $10\ \mu\text{m}$ is assumed. The curve is the limit imposed by the charging of the data line during the current driven part of the selection time.

and current driving capabilities of the OTFTs on the other hand. In order to reach the desired frame rate and to control the gray levels against the threshold voltage dispersions of OTFTs and OLEDs, we have shown the need for a current driven addressing mode and we have presented a new driving scheme with an external memory. We have shown the need for metal addressing lines with very low capacitances. These low capacitances can be obtained by a self-aligned OTFT fabrication process and by the use of a thick layer of insulator between the control lines. We have presented a layout with nonpatterned power supply and ground, necessary for heat dissipation and easy manufacturing. Based on this layout we have shown that large flat panel displays with reasonable power supply are possible. We conclude that the use of full plastic displays as high information displays is possible, but demanding in terms of organic semiconductor technology, matrix addressing circuits and driving schemes.

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