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UTILITY
PATENT APPLICATION
TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.

BeSang-Poolxi

First Inventor

Sang-Yun Lee

Title

Vertical Memory Device

Express Mail Label No.

ED 1107 04 642 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Applicant claims small entity status.
See 37 CFR 1.27.
3. ☒ Specification [Total Pages 22]
(preferred arrangement set forth below)
- Descriptive title of the invention
- Cross Reference to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to sequence listing, a table,
or a computer program listing appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 34]
5. Oath or Declaration [Total Sheets _____]
a. ☒ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 18 completed)
i. ☐ **DELETION OF INVENTOR(S)**
Signed statement attached deleting inventor(s)
name in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76

7. ☐ CD-ROM or CD-R in duplicate, large table or
Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Form (CRF)
b. Specification Sequence Listing on:
i. ☐ CD-ROM or CD-R (2 copies); or
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ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 CFR 3.73(b) Statement ☒ Power of
(when there is an assignee) Attorney
11. ☐ English Translation Document (if applicable)
12. ☐ Information Disclosure ☐ Copies of IDS
Statement (IDS)/PTO-1449 Citations
13. ☐ Preliminary Amendment
14. ☒ Return Receipt Postcard (MPEP 503)
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15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☐ Nonpublication Request under 35 U.S.C. 122
(b)(2)(B)(i). Applicant must attach form PTO/SB/35
or its equivalent.
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:



Continuation



Divisional



Continuation-in-part (CIP)

of prior application No.: 10/813,969

Prior application information:

Examiner _____

Art Unit: 2811For CONTINUATION OF DIVISIONAL APPS only; The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS



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Signature

Raymond J. Werner

Date

03 SEP 2004

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Intel v. BeSang
IPR2023-00991
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FEE TRANSMITTAL
for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☒ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT

(\$) 385

Complete if Known

Application Number

N/A

Filing Date

03 SEP 2004

First Named Inventor

Sang-Yun Lee

Examiner Name

N/A

Art Unit

N/A

Attorney Docket No.

BeSang.P001x1

METHOD OF PAYMENT (check all that apply)☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None☐ Deposit Account:Deposit
Account
Number
Deposit
Account
Name

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Credit any overpayments☐ Charge any additional fee(s) or any underpayment of fee(s)☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	770	2001	385	Utility filing fee	385
1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) (\$) 385

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

Total Claims	Extra Claims	Fee from below	Fee Paid
Independent Claims	-20** =	X	
Multiple Dependent	-3** =	X	

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$) 0

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for ex parte reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$) 0

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34,152

(Complete if applicable)

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Date

03 September 2004

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VERTICAL MEMORY DEVICE STRUCTURES

Cross Reference to Related Applications

This is a continuation-in-part of Application No. 10/873,969, entitled "Three-Dimensional Integrated Circuit Structure and Method of Making Same", filed 21 June 2004; and which is incorporated in its entirety herein by reference.

Field of the Invention

The present invention relates generally to semiconductor structures and manufacturing methods for memory devices and circuits. More particularly, the present invention relates to a semiconductor substrate combined with a relatively thin add-on semiconductor layer in which various vertically oriented memory elements are fabricated.

Background of the Invention

Advances in semiconductor manufacturing and digital systems architecture have provided the means to produce chips, or integrated circuits, with many millions of active and passive circuit elements along with the interconnects needed to create the desired circuit networks. As is well-known, integrated circuits contain transistors that are primarily implemented on a single major surface of a substrate, such as a semiconductor wafer. These laterally oriented devices consume significant amounts of chip area. Over a number of years, manufacturing advances related to transistors and interconnects have primarily been directed to reducing the lateral dimensions thereof, so that more circuitry per unit area could be placed on a chip. However, the manufacturing equipment and technologies required to support the manufacture of such highly integrated chips becomes increasingly expensive with each new generation of smaller devices.

What is needed are structures and methods that are suitable for providing increased circuit density in integrated circuits without necessarily requiring devices to be made smaller.

Summary of the Invention

Briefly, a plurality of vertically oriented semiconductor memory devices, or cells, may be added to a separately fabricated substrate that includes electrical devices and/or interconnect lines. The plurality of vertically oriented semiconductor memory devices, or cells, are physically separated from each other, and therefore are not disposed within a common semiconductor body, or semiconductor substrate. The regions around and between the vertically oriented memory devices, or cells may have dielectric material disposed therein.

In one aspect of the present invention, the plurality of vertically oriented semiconductor memory devices, or cells, are added to the separately fabricated substrate as a thin layer including several doped semiconductor regions which, subsequent to attachment to the substrate, are etched to produce individual doped stack structures. These individual, vertically oriented, doped stack structures are, in various embodiments, fitted out with a variety of structures, such as but not limited to gate dielectric films, gate electrodes, capacitor terminals, contacts, charge trapping multi-layer films, and floating gates. In other embodiments of the present invention, the plurality of vertically oriented semiconductor memory cells may be fabricated prior to attachment to the separately fabricated substrate.

In another aspect of the present invention, Dynamic Random Access Memory (DRAM) cells, Static Random Access Memory (SRAM) cells, non-volatile memory cells, and similar structures may be formed in a stackable add-on layer for use in conjunction with the separately fabricated substrate.

Brief Description of the Drawings

Fig. 1 is a cross-sectional view of an embodiment the present invention that includes a base semiconductor substrate and add-on vertical memory devices.

Fig. 2 is a cross-sectional view of an embodiment of the present invention having a vertical DRAM cell with vertical connection of a capacitor and a MOSFET in the SOI layer.

Fig. 3 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 2.

Fig. 4 is a cross-sectional view of an embodiment of the present invention having two vertical DRAM cells with vertical connection of a capacitor and a MOSFET, respectively in the SOI layer.

Fig. 5 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 4.

Fig. 6 is a cross-sectional view of an embodiment of the present invention having two vertical DRAM cells with vertical connection of a capacitor and two MOSFETs in the SOI layer.

Fig. 7 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 6.

Fig. 8 is a cross-sectional view of an embodiment of the present invention having a vertical DRAM cell with vertical connection of a MOSFET in the SOI layer and an external capacitor.

Fig. 9 illustrates an exemplary DRAM structure formed with devices illustrated in Fig. 8.

Fig. 10 illustrates an exemplary DRAM structure formed with devices illustrated in Fig. 8.

Fig. 11 illustrates another exemplary DRAM structure formed with devices illustrated in Fig. 8.

Fig. 12 is a cross-sectional view of an embodiment of the present invention having two vertical DRAM cells with vertical connection of two MOSFETs in the SOI layer and two external capacitors.

Fig. 13 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 12.

Fig. 14 is a cross-sectional view of an embodiment of the present invention having a Negative Differential Resistance (NDR) based vertical SRAM cell with vertical connection of two MOSFETs in the SOI layer.

Fig. 15 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 14.

Fig. 16 is a cross-sectional view of an embodiment of the present invention having a Negative Differential Resistance based vertical SRAM cell with vertical connection of a Thyristor and a MOSFET in the SOI layer.

Fig. 17 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 16.

Fig. 18 is a cross-sectional view of an embodiment of the present invention having a Negative Differential Resistance based vertical SRAM cell with vertical connection of a bi-stable diode and a MOSFET in the SOI layer.

Fig. 19 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 18.

Fig. 20 is a cross-sectional view of an embodiment of the present invention having two Negative Differential Resistance based vertical SRAM cells with vertical connection of a Thyristor and a MOSFET, respectively in an SOI layer.

Fig. 21 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 20.

Fig. 22 is a cross-sectional view of an embodiment of the present invention having two Negative Differential Resistance based vertical SRAM cells with vertical connection of a Thyristor and a MOSFET, respectively in two SOI layers.

Fig. 23 is a cross-sectional view of an embodiment of the present invention having a vertical memory cell with a vertical MOSFET in the SOI layer, where the vertical memory has a floating gate and a control gate, and could work as a DRAM and a nonvolatile memory device.

Fig. 24 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 23.

Fig. 25 is a cross-sectional view of an embodiment of the present invention having a vertical memory cell with a vertical MOSFET in the SOI layer, where the vertical memory has a charge-trapping gate insulating layer, and could work as a DRAM and a nonvolatile memory devices.

Fig. 26 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 25.

Fig. 27 is a cross-sectional view of an embodiment of the present invention having two vertical memory cells with vertical connection of the two memory cells shown in Fig. 23 in the SOI layer, where the vertical memory could work as a DRAM and a nonvolatile memory devices.

Fig. 28 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 25.

Fig. 29 is a cross-sectional view of an embodiment of the present invention having two vertical memory cells with vertical connection of the two nonvolatile memory cells in the SOI layer.

Fig. 30 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 29.

Fig. 31 is a cross-sectional view of an embodiment of the present invention having four vertical memory cells with vertical connection of the four nonvolatile memory cells in the SOI layer.

Fig. 32 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 31.

Fig. 33 illustrates an exemplary 16-transistor nonvolatile memory structure formed with devices illustrated in Fig. 31.

Fig. 34 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 33.

Detailed Description

Vertically oriented memory structures constituting memory cells, or portions thereof, in a 3-D integrated circuit arrangement in accordance with the present invention, are shown in Fig. 1. Embodiments of the present invention provide a device integration architecture and technology. More particularly, memory cells, or portions thereof, which are vertically oriented with respect to a major surface of a wafer, are provided so that the effective device density, i.e., devices per unit area of the wafer surface, is increased. In this way, greater functionality can be provided in a chip of a given surface area.

Reference herein to "one embodiment", "an embodiment", or similar formulations, means that a particular feature, structure, operation, or characteristic described in connection with the embodiment, is included in at least one embodiment of the present invention. Thus, the appearances of such phrases or formulations herein are not necessarily all referring to the same embodiment. Furthermore, various particular features, structures, operations, or characteristics may be combined in any suitable manner in one or more embodiments.

Terminology

The term "vertical", as used herein, means substantially perpendicular to a major surface of a substrate, such as, for example, a semiconductor wafer.

The term "Vbias" refers to an applied voltage during operation of an illustrated device. Vbias may be ground, or "0" volts, but is not required to be. The acronym "WL" refers to Word Line, and the acronym "BL" refers to Bit Line. The term " V_{DD} " refers to a positive supply voltage. The acronym "SoC" refers to System on a Chip, with "SoCs" being the plural of SoC.

The terms chip, semiconductor device, integrated circuit, LSI device, monolithic integrated circuit, ASIC, SoC, microelectronic device, and similar expressions are sometimes used interchangeably in this field. Microelectronic device may be considered to be the broadest term, encompassing the others. With respect to these microelectronic devices, signals are typically coupled between them and other circuit elements via physical, electrically conductive connections. The point of connection is sometimes referred to as an input, output, terminal, line, pin, pad, port, interface, or similar variants and combinations.

The term "device", as used herein, refers to active and passive circuit elements. "Device" includes, but is not limited to, FETs (n-channel and p-channel), Thyristor, capacitors, varactors, floating gates, charge trap layers, diodes, and resistors.

FET as used herein, refers to metal-oxide-semiconductor field effect transistors (MOSFETs). These transistors are also known as insulated gate field effect transistors (IGFETs). FETs are generally described as three terminal devices having a gate, a source and a drain. Although FETs may be further described as

four terminal devices when the body of the FET is considered.

Source and drain terminals refer to the terminals of a FET, between which conduction occurs under the influence of an electric field, subsequent to the inversion of the semiconductor surface under the influence of an electric field resulting from a voltage applied to the gate terminal.

The acronym "SOI" generally refers to Silicon-on-Insulator. As will be appreciated by those skilled in this field, SOI layers can be formed in a variety of ways. Unless otherwise noted, "SOI layer" is used herein to refer to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate. In this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections. As a stackable add-on layer, the single-crystal layer may have been doped so as to have one or more doped regions vertically adjacent each other. For purposes of this disclosure, doped regions may include intrinsic regions as well as p-type and n-type regions. Individual semiconductor structures may be formed by etching through portions of the doped stack to electrically isolate those structures. These structures may be fitted with contacts, dielectric coatings, or films, gate electrodes, capacitor terminals, and so on. The spaces between such individual structures may be filled with dielectric material so as to re-form a layer without gaps or voids therein, and thereby provide for mechanical stability, and support for additional stacked layers. Various interconnect layers may be formed and patterned at intermediate levels of the dielectric material. In this way, the stackable add-on layer may provide a plurality of memory cells suitable for connections to an underlying substrate.

The expression "high dielectric constant" refers to a dielectric constant that is greater than the dielectric constant of silicon dioxide.

The expression "3-D IC", as used herein, refers to a three-dimensional integrated circuit that includes a semiconductor substrate having devices and/or interconnect structures fabricated thereon, and least one stackable add-on layer, also having devices and/or interconnect, where the semiconductor substrate and the

stackable add-on layer are stacked and bonded to each other.

As shown in Fig. 1, vertical memory devices **656** in accordance with the present invention are separated by isolation **135** and have floating structures in the filled dielectric materials **133a**. Vertical memory devices **656** are referred herein to as floating devices (FLD). Embodiments of the present invention are different from a conventional bonded IC layer, which has a shared well **142** or substrate **143**, wherein an electrically common region is located. Additionally, embodiments of the present invention do not have the physically supporting layer which can be found in a conventional SOI IC substrate where all devices in one IC layer are supported by a substrate under a bottom oxide. The layer that includes FLD **656** is called FLD layer **101**. Inter-layer dielectric (ILD) layers **133** disposed above and below FLD layer **101** have interconnection lines **132** and vias, or contacts, **131**. Interconnection lines **132** and vias **131** connect FLDs directly or indirectly within an FLD layer, or connect devices from an FLD layer to another FLD layer or to a base substrate.

Still referring to Fig. 1, the substrate bonded to lower dielectric layer **151** is called base substrate **103**. The first FLD layer above base substrate **103** is called first FLD layer **101**, and the next FLD layer is called second FLD layer (not shown).

Fig. 1 shows one FLD layer **101** and one base semiconductor substrate **103**. Dashed line **134** denotes a border, or interface, of two ILD layers. First ILD layer **151** has interconnection lines and vias, and base semiconductor substrate **103** shares these interconnections and vias with first FLD layer **101**. Some vias may directly connect to second FLD layer (not shown) from first ILD layer **151**. Also interconnection lines and vias in second ILD layer **152** are shared by first FLD layer **101** and second FLD layers.

Still referring to Fig. 1, the formation of electrodes to floating memory device **656** is by direct connection to the top **122** and bottom **121** of each floating memory device **656**. Also, in various embodiments of the present invention, floating devices may be constructed that have vertically separated single or more intermediate electrodes **123**. These electrodes could be connected to interconnection lines within ILD layers **151**, **152** disposed on the top and/or bottom of the FLD layer.

In Fig. 1, a logic circuit **114** including sense amplifier and column/row selectors may be implemented in base semiconductor substrate **103** while nonvolatile memory devices are implemented in first FLD layer **101**, and SRAM devices are in a second FLD layer, in which case one semiconductor substrate could integrate different types of individually optimized devices without using a difficult and expensive SoC structures or semiconductor processes.

Various embodiments of the present invention do not require a physically supporting substrate for floating devices. Also, without a base substrate, various embodiments could exist along with interconnection lines, vias, and FLDs only.

Various embodiments of the present invention provide floating devices that are separated by dielectric isolation regions. These electrically separated structures do not have the parasitic devices which are typically found in prior art approaches.

Various embodiments of the present invention provide floating devices that may be connected directly or indirectly.

In various embodiments of the present invention, combining the SOI layer with a semiconductor substrate does not require the same type of wafer alignment structures as are used in photolithographic processes, rather, the wafer alignment structure may be implemented as a wafer alignment mark, or as a bump-type alignment structure. Alternatively, without a wafer alignment structure, the SOI layer could be transferred along with a simple notch alignment because the transferred SOI layer does not have structures for multiple devices, such as isolation structure or interconnection lines, which are horizontally divided. The transferred, unpatterned, SOI layer has only a vertically oriented stack of layers.

In various embodiments of the present invention, a FLD can be directly contacted by metal electrodes at top, bottom, and intermediate regions of the individual doped stack structures (i.e., pillar structures). The area of the metal electrodes can be the same as the top and bottom areas of individual doped stack structures of the FLD. Therefore, the voltage drop of the device due to contact resistance can be reduced as compared to conventional laterally oriented devices.

The bottom of the FLD is connected to metal layer **121** which is also directly connected to vias **131** in ILD layer **151**. Therefore, the bottom of FLD essentially has

a pre-formed electrode and contact. The top of the FLD may be connected to metal layer 122 which is also directly connected to vias 131 in ILD layer 152.

Multiple FLD layers can be stacked, thereby increasing the effective device density.

FLDs may, but are not required to, have a pillar structure. Conventional pillar type Surrounding Gate Transistor (SGT) structures are difficult to integrate with optimized horizontal (i.e., lateral, or co-planar) devices. Integration may cause the shadow effect to occur during ion implantation due to the presence of pillar type transistor structures. Also, conventional SGT structures do not provide for high integration density because of processing problems associated with forming electrodes at the source/drain and gate regions. Therefore, these conventional approaches are not suitable for SoC formation. However, the add-on pillar type SGT structures in accordance with the present invention, may be combined with conventionally processed wafers.

An FLD can be fabricated to be in full or partial depletion mode, by control of the FLD width. The depletion mode can also be controlled by the operational voltage and dielectric constant of the gate dielectric material.

An advantage of embodiments of the present invention is that because the detached surface of the SOI substrate typically corresponds to a heavily doped source/drain region of a memory, even though small surface defects may be present, there is little impact on gate oxide quality, device operation, or yield, from these surface defects.

The FLD may have a graded impurity distribution in the channel region. The graded impurity distribution in the channel region of devices in accordance with the present invention may give rise to induced electric fields that accelerate current flow and reduce the Short Channel Effect, as compared to conventional devices. The graded impurity distribution can readily be formed by ion implantation or by an epitaxial process. Increased impurity concentration in the channel region from source to drain side provides for asymmetric operation. For example, a Lightly Doped Drain (LDD) structure could be selectively formed at one of the source/drain terminals (which in operation would be the drain terminal). It is difficult to implement

graded impurity distribution in the channel of conventional horizontal MOSFETs because of difficulties in high tilt ion implantation and device layout.

The FLD, in accordance with the present invention, has a gate dielectric layer which may be implemented with process operations at temperatures below 650 °C. The dielectric layer could be thermal oxide, deposited oxide, oxynitride, or a combination of oxide and nitride, such as an oxide-nitride-oxide (ONO) layer, or a nitride-oxide (NO) layer. Any suitable dielectric material could be used except films requiring processing at temperatures more than 650 °C. Another advantage of embodiments of the present invention is that it is easy to use high dielectric constant (high-k) materials in the gate dielectric layer, such as, but not limited to, Al_2O_3 , ZrO_2 , HfO_2 , Y_2O_3 , La_2O_3 , Ta_2O_5 , TiO_2 , and BST. In conventional manufacturing of MOSFETs, a high temperature heat activation operation is required after the source/drain ion implantation. At this time, the properties of high-k materials can be altered. However, the FLD architecture does not require a high temperature process, and so high-k materials could be used at stable condition. Also, if Atomic Layer Deposition (ALD) is used to provide the gate dielectric layer, then a substantially uniform layer can be obtained.

In order to prevent diffusion of oxidant and undesired oxidation of via **131** and/or interconnection **132** during the thermal gate oxidation process, it may be desired to have 'moisture blocking layer' below the gate insulator layer **183**. The moisture blocking layer may be, but is not limited to, a nitride layer or an oxynitride film. Such a moisture blocking layer may be disposed in ILD layer **151**, or dielectric layer **133a** under gate insulator layer **183**.

In accordance with the present invention, FET threshold voltage can be controlled by changing the gate dielectric thickness and/or the width of the FLD. If different gate dielectric thickness is used or different dielectric constant materials are used at FLD, then multiple operational voltages and threshold voltages could be implemented at the same stackable add-on layer. Also, because the FLD may be produced at low temperature, and a surrounding gate is used, it is less difficult to use a metal gate as compared to conventional manufacturing approaches.

In accordance with the present invention, memory devices could be implemented using FLDs. The following illustrative embodiments of the present

invention use n-type enhancement MOSFETs. As will be appreciated by those skilled in this field, p-type and/or depletion mode FETs, or bipolar transistors could be used in various memory cell implementations.

Fig. 2 shows a DRAM cell with vertical connection of a capacitor and a MOSFET in the stackable add-on layer. A source/drain terminal of the access transistor is extended to the vertical capacitor. Fig. 3 shows a schematic diagram of an equivalent circuit for the structure shown in Fig. 2.

The gate insulators **183** for the transistor and capacitor in Fig. 2 are separated. However, in some embodiments these might be grown at the same time and could be used for the transistor and capacitor as a continuous gate insulator film. Multi-gate devices in accordance with the present invention may use such continuous gate insulator films.

Fig. 4 shows two vertical DRAM cells with vertical connection of a capacitor and a MOSFET, respectively in the stackable add-on layer. The structure shares a single bit line, therefore, the density of DRAM cells increases by a factor of two while the aspect ratio of SOI pillar **124** remains relatively small. Fig. 5 shows a schematic diagram of an equivalent circuit for the structure shown in Fig. 4.

Fig. 6 shows a dual port DRAM cell with vertical connection of a capacitor and two MOSFETs in the stackable add-on layer. As can be seen in Fig. 6, one capacitor **CAP** disposed in the central portion of SOI pillar **124** is shared by two vertical MOSFETs. In this case, the information in the shared capacitor may be accessed through the top and bottom access MOSFETs. Therefore, this structure may function as a dual-port DRAM cell. The structure of Fig. 6 increases density by a factor of two while the aspect ratio of SOI pillar **124** remains relatively small. Fig. 7 shows a schematic diagram of an equivalent circuit for the structure of Fig. 6.

Fig. 8 shows a vertical DRAM cell with vertical connection of a MOSFET in the SOI layer and a external capacitor in bottom dielectric layer **151**. The capacitor may be MIM (Metal-Insulator-Metal), PIP (Poly-Insulator-Poly), MIP (Metal-Insulator-Poly), or Trench capacitor in base substrate **103**. Without external capacitor, the single MOSFET in SOI pillar **124** could work as a DRAM cell because electric charge is temporarily accumulated in the body (p-region) when the body of the MOSFET is floating.

Fig. 9 illustrates an exemplary DRAM structure formed with devices illustrated in Fig. 8. The external capacitor is placed in bottom ILD layer **151**. The external capacitor may alternatively be placed in top dielectric layer **152** as shown in Fig. 10. In a further alternative, the external capacitor may be placed in top **151** and bottom **152** dielectric layers as shown in Fig. 11. In this case, the capacitor takes more space to store more charge, which may increase the time between refresh cycles, and increase the effective operational speed of the DRAM.

Fig. 12 shows two vertical DRAM cells with vertical connection of two MOSFETs in the stackable add-on layer and two external capacitors. Without external capacitor, the MOSFETs in the SOI pillar **124** could work as a DRAM cell either as explained in Fig. 8. Fig. 13 shows a schematic diagram of an equivalent circuit for the structure shown in Fig. 12.

Fig. 14 shows a Negative Differential Resistance based vertical SRAM cell with vertical connection of two MOSFETs in the stackable add-on layer. The top MOSFET has gate insulator **183c** which induces charge trapping and discharging, and therefore, creates negative differential characteristics when the drain bias is higher than the gate bias. Fig. 15 shows a schematic diagram of an equivalent circuit for the structure shown in Fig. 14.

Fig. 16 shows another NDR (Negative Differential Resistance) based vertical SRAM cell with vertical connection of a Thyristor and a MOSFET in the stackable add-on layer. The intermediate gate, WL2, controls diode action between p- and n- regions, therefore, it triggers snapback of the Thyristor to latch SRAM. Fig. 17 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 16.

Fig. 18 shows a cross-sectional view of an embodiment of the present invention having a Negative Differential Resistance based vertical SRAM cell with vertical connection of a bi-stable diode and a MOSFET in the stackable add-on layer. The bi-stable diode, which is implemented as a sandwich of p+/GeSi/n+, uses a tunneling diode property, that creates negative resistance when the applied bias goes up. Other tunneling diodes may be substituted for the p+/GeSi/n+ diode. The output node, Vout, is connected to a load resistor, Rload, or another tunneling diode. Fig. 19 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 18 including load resistor Rload.

Fig. 20 shows a cross-sectional view of an embodiment of the present invention having a Negative Differential Resistance based vertical SRAM cell including the vertical connection of two Thyristor/MOSFET pairs, in the stackable add-on layer. In this embodiment of the present invention, the two Thyristor-type SRAMs are stacked in vertical the direction and a bit line is shared in the middle of SOI pillar **124**. Fig. 21 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 20.

One drawback of the structure in Fig. 20 is its high aspect ratio, which may cause toppling during processing. Therefore, if two stackable add-on layers having a Thyristor-type SRAM cell are vertically stacked as shown in Fig. 22, the problem of high aspect ratio can be decreased.

Fig. 23 shows a vertical memory cell with a vertical MOSFET in a stackable add-on layer, where the vertical memory has a floating gate **123k** and a control gate **123**, and could work as a DRAM and/or a nonvolatile memory device. Nonvolatile memory devices usually have permanent (or relatively long term) charge storage nodes. In this structure, floating gate **123k** is the charge storage node. However, when the body region is floating, charge is temporarily stored in the body region (p-doped region) and could be used for DRAM operation. Fig. 24 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 23.

Fig. 25 shows a cross-sectional view of an embodiment of the present invention having a vertical memory cell with a vertical MOSFET in a stackable add-on layer, where the vertical MOSFET of the memory cell has a charge-trapping gate insulating layer. Such a device could work as a DRAM or as a nonvolatile memory device. The charge-trapping gate insulating layer **183g** may be, for example, an oxide-nitride-oxide film. This nonvolatile memory device has a permanent (or relatively long term) charge storage node within the oxide-nitride-oxide film, which may have a multi-bit property depending on charge storage location. This structure may be used to create a circuit that works as a DRAM, as explained in connection with Fig. 24. Fig. 26 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 25.

Fig. 27 shows two vertical memory cells (of the type shown in Fig. 23) configured to provide a vertical connection between the two memory cells in a

stackable add-on layer. This structure shares a bit line and may reduce aspect ratio of SOI pillar **124**. The dual-gate nonvolatile memory cell could be replaced by single-gate nonvolatile memory cell shown in Fig. 25. Fig. 28 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 27.

Fig. 29 shows two vertical memory cells with vertical connection of the two nonvolatile memory cells in the stackable add-on layer. Each nonvolatile memory cell has a single-gate select gate (SG) MOSFET and a dual-gate charge storage MOSFET. Fig. 30 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 29.

Fig. 31 shows four vertical memory cells with serial connection of the four nonvolatile memory cells in the stackable add-on layer. The nonvolatile could be single-gate instead of dual-gates. Fig. 32 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 31.

Fig. 33 illustrates an exemplary 16-transistor nonvolatile memory structure formed with devices illustrated in Fig. 31. Such a 16-transistor nonvolatile memory may be part of a NAND architecture flash memory product. This type of NAND-type structure is also suitable for use in logic applications. The select transistors may be placed in base substrate **103** or in stackable add-on layer **101**. Fig. 34 is a schematic diagram of an equivalent circuit for the structure shown in Fig. 33.

Conclusion

As disclosed herein, vertical DRAM cells have at least one vertical transistor and a capacitor, where the capacitor temporarily stores electric charges and requires refresh. The capacitor could be implemented as an extension of vertical SOI pillar or may be placed outside of the stackable add-on layer, where the capacitor is serially connected to the transistor. Or, as a body part of the vertical transistor, the capacitor could be placed in parallel with a transistor. Dual-port DRAM shares single capacitor and increases memory density.

Vertical SRAM has at least one vertical transistor and a serially connected NDR device, where the NDR may be a Thyristor, charge-trapping MOSFET, or tunneling (or bi-stable) diode.

Vertical nonvolatile memory has a form of either dual-gate with floating gate or single-gate with charge trapping gate insulator. Since the body of SOI pillar is usually floating, the nonvolatile could work as a DRAM device.

Multiple memory cells may be vertically stacked, either in a single stackable add-on layer, or in two or more stacked stackable add-on layers. Since vertically stacked multiple memory cells may share a bit line, the effective aspect ratio of the SOI pillar could be decreased compared with individually stacked memory structure.

All of the memory devices, or cells, described herein may have redundant devices, or cells, in the stackable add-on layer for replacing defective elements thereof.

It is to be understood that the present invention is not limited to the embodiments described above, but encompasses any and all embodiments within the scope of the subjoined Claims.

What is Claimed is:

1. A semiconductor memory structure, comprising:
 - a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and
 - a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;
 - wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate; and wherein the memory cell is a DRAM having at least one transistor.
2. The semiconductor structure of Claim 1, wherein the vertically oriented memory cell comprises a vertical transistor and a serially connected capacitor in a SOI pillar.
3. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises a vertical transistor in an SOI pillar and a capacitor connected in series therewith, the capacitor disposed external to the first stackable add-on layer.
4. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises a first capacitor, a first access

transistor serially connected to the first capacitor, a second access transistor serially connected to the first access transistor, and a second capacitor serially connected to the second access device; wherein the first capacitor, the first access transistor, the second access transistor, and the second capacitor are all formed in a single vertically oriented SOI pillar.

5. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically oriented, serially connected transistors formed on a SOI pillar, the serially connected transistors further connected to a capacitor disposed external to the stackable add-on layer.

6. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically and serially connected transistors and a shared serially connected capacitor in a SOI pillar.

7. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises:

- a first diode;

- a first access transistor connected in series to the first diode;

- a second access transistor connected in series to the first access transistor;

- a third access transistor connected in series to the second access transistor;

- a fourth access transistor connected in series to the third access transistor;

and

- a second diode connected in series to the fourth access transistor;

wherein the first diode, the first, second, third, and fourth transistors, and the second diode are formed on the same SOI pillar.

8. A semiconductor memory structure, comprising:

a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate;

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material; and

the stackable add-on layer to a layer of the substrate that is the greatest distance from the substrate;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate; and wherein the memory cell is an SRAM having at least one Negative Differential Resistance device.

9. The semiconductor memory structure of Claim 8, wherein the vertically oriented semiconductor memory cell comprises a vertically oriented transistor and a vertically oriented NDR-type Thyristor serially connected to each other.

10. The semiconductor memory structure of Claim 9, wherein the vertically oriented transistor is formed on an SOI pillar and the vertically NDR-type Thyristor is formed on an SOI pillar.

11. The semiconductor memory structure of Claim 9, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on two separated SOI pillars.

13. The semiconductor memory structure of Claim 8, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on the same SOI pillar.

14. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate;

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material; and

the stackable add-on layer to a layer of the substrate that is the greatest distance from the substrate;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate; and wherein the memory cell is a nonvolatile memory having at least one transistor.

15. The semiconductor memory structure of Claim 14, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

16. The semiconductor memory structure of Claim 14, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

17. The semiconductor memory structure of Claim 14, wherein at least two nonvolatile memory cells are vertically and serially connected on a first SOI pillar.

18. The semiconductor memory structure of Claim 17, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected by an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell on a second SOI pillar.

VERTICAL MEMORY DEVICES

ABSTRACT OF THE DISCLOSURE

Vertically oriented semiconductor memory cells are added to a separately fabricated substrate that includes electrical devices and/or interconnect. The plurality of vertically oriented semiconductor memory cells are physically separated from each other, and are not disposed within the same semiconductor body. The plurality of vertically oriented semiconductor memory cells can be added to the separately fabricated substrate as a thin layer including several doped semiconductor regions which, subsequent to attachment, are etched to produce individual doped stack structures, which are then supplied with various dielectric coatings, gate electrodes, and contacts by means of further processing operations. Alternatively, the plurality of vertically oriented semiconductor memory cells may be completely fabricated prior to attachment. DRAMs, SRAMs, non-volatile memories, and combinations of memory types can be provided.

Fig. 1

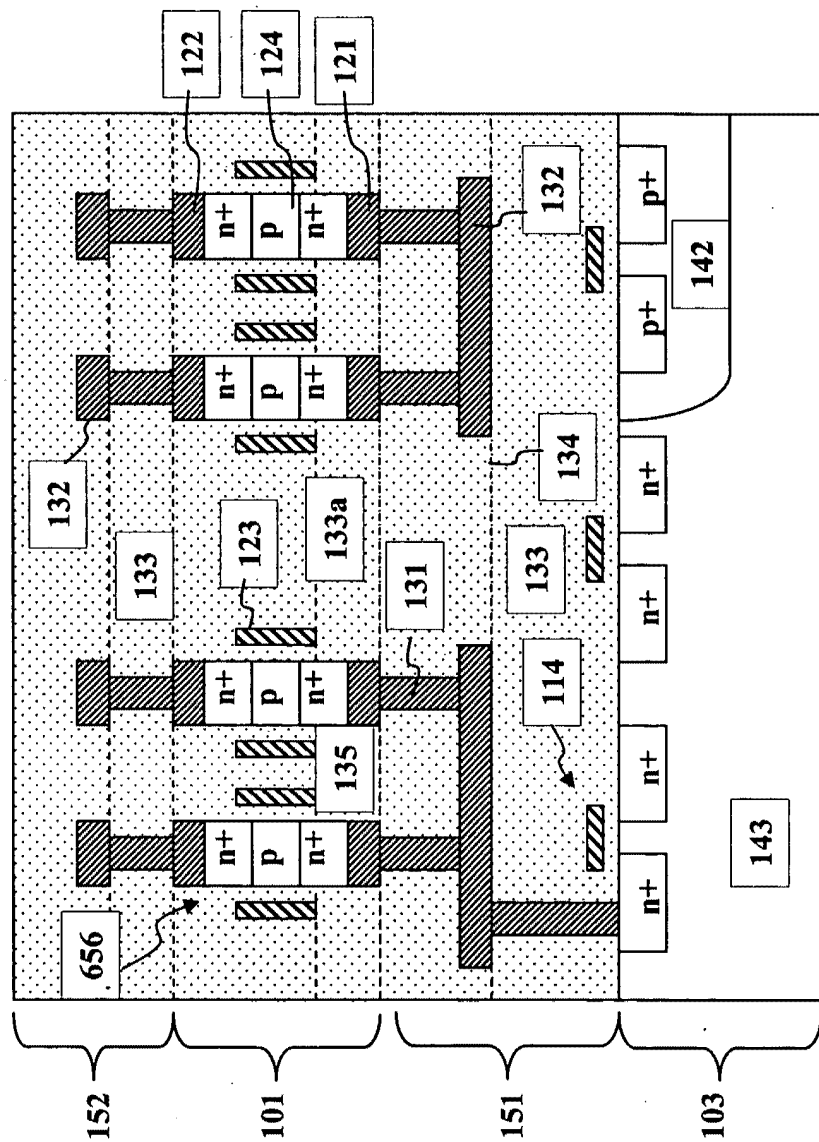


Fig. 2

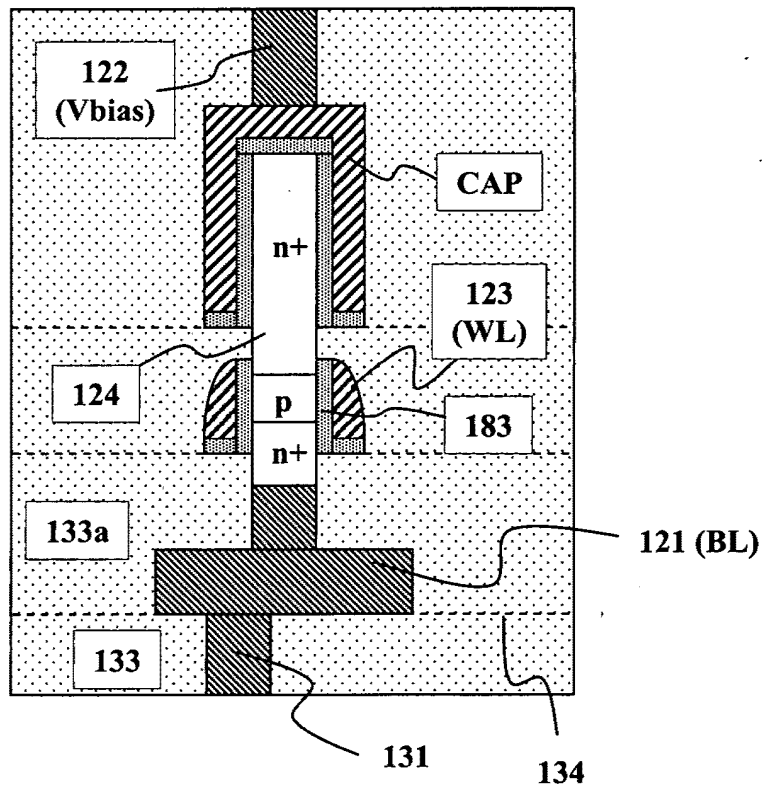


Fig. 3

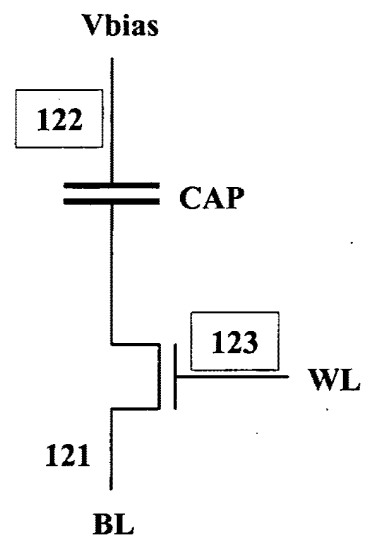


Fig. 4

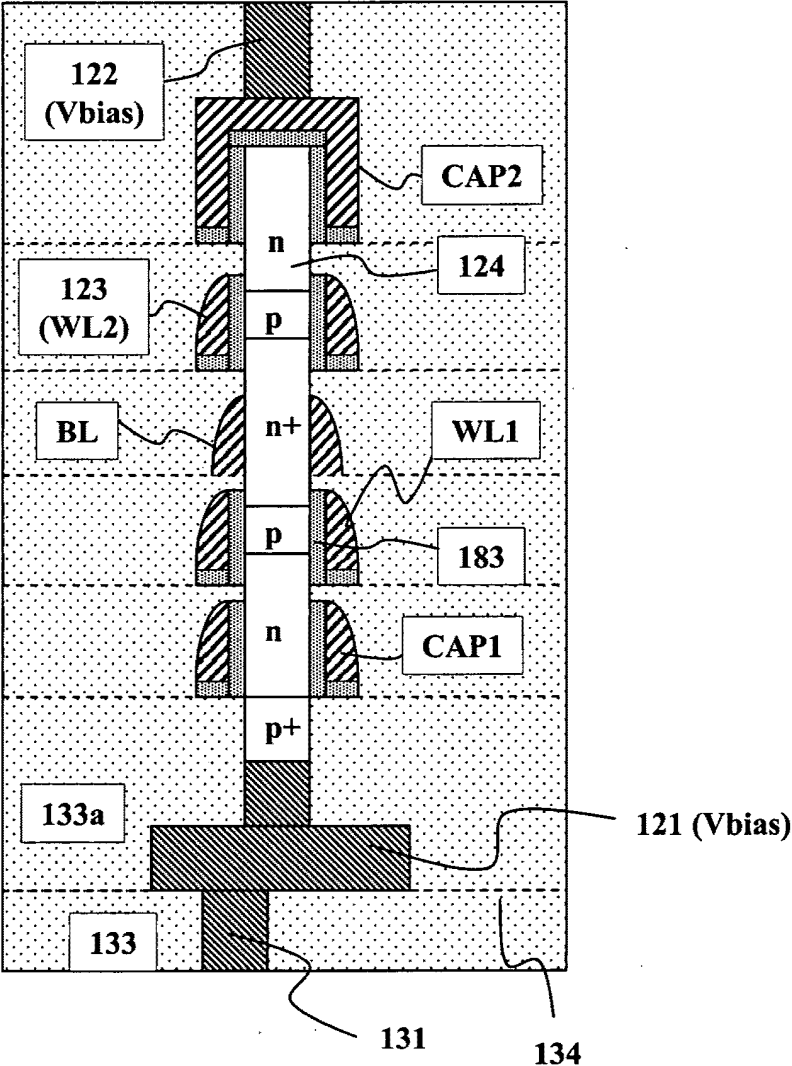


Fig. 5

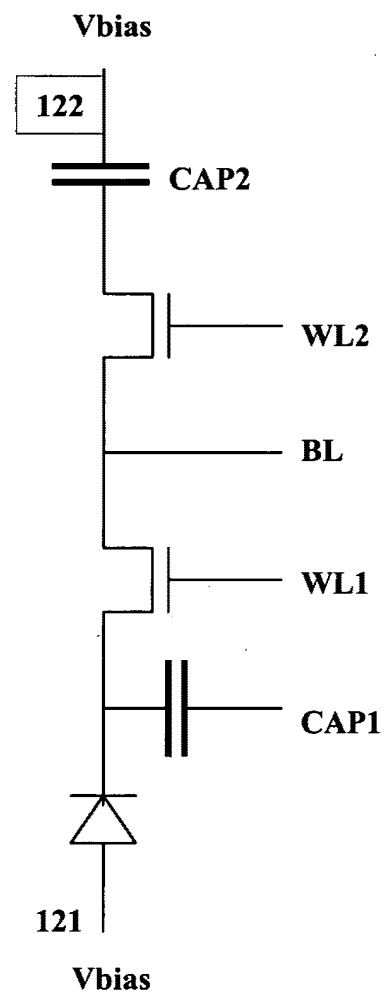


Fig. 6

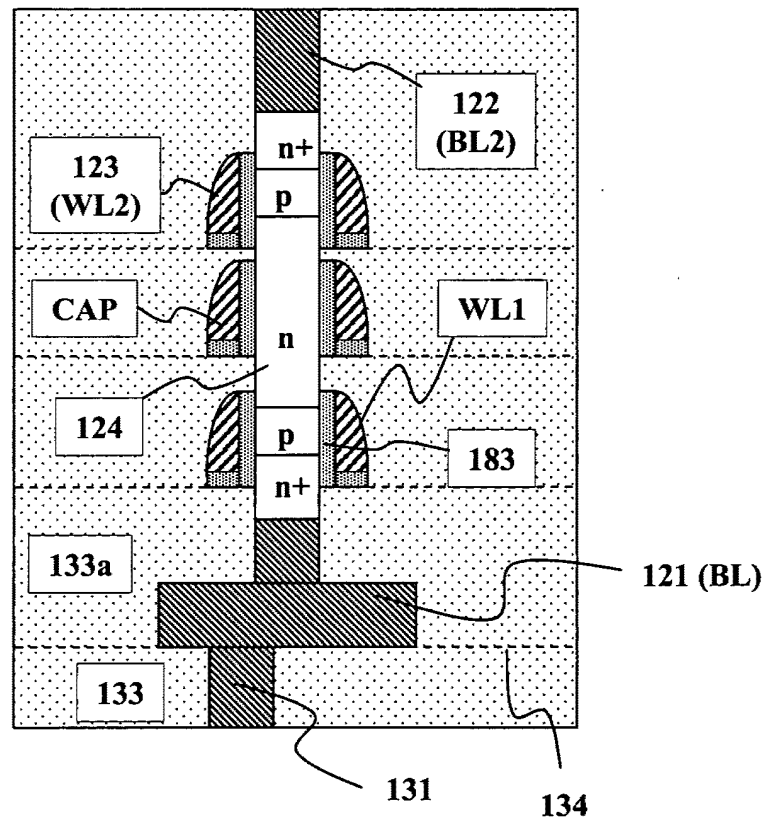


Fig. 7

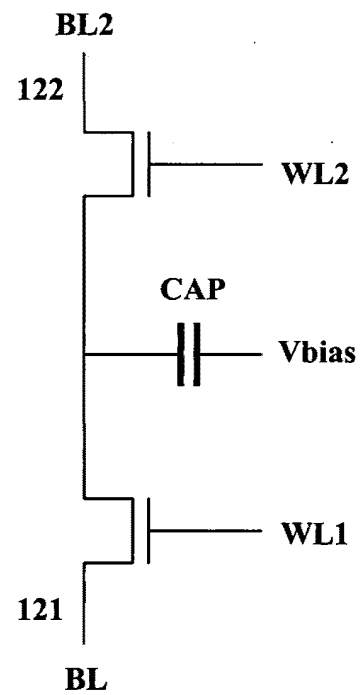


Fig. 8

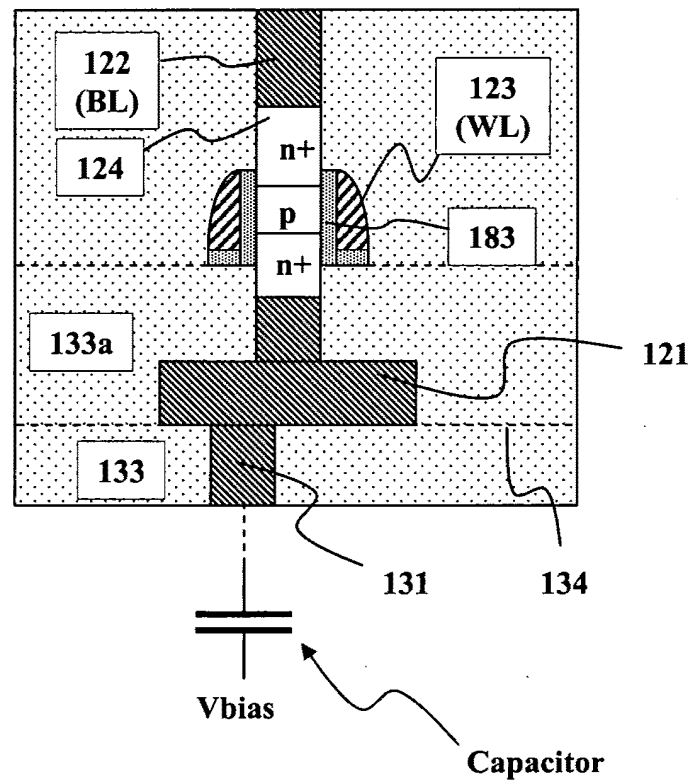


Fig. 9

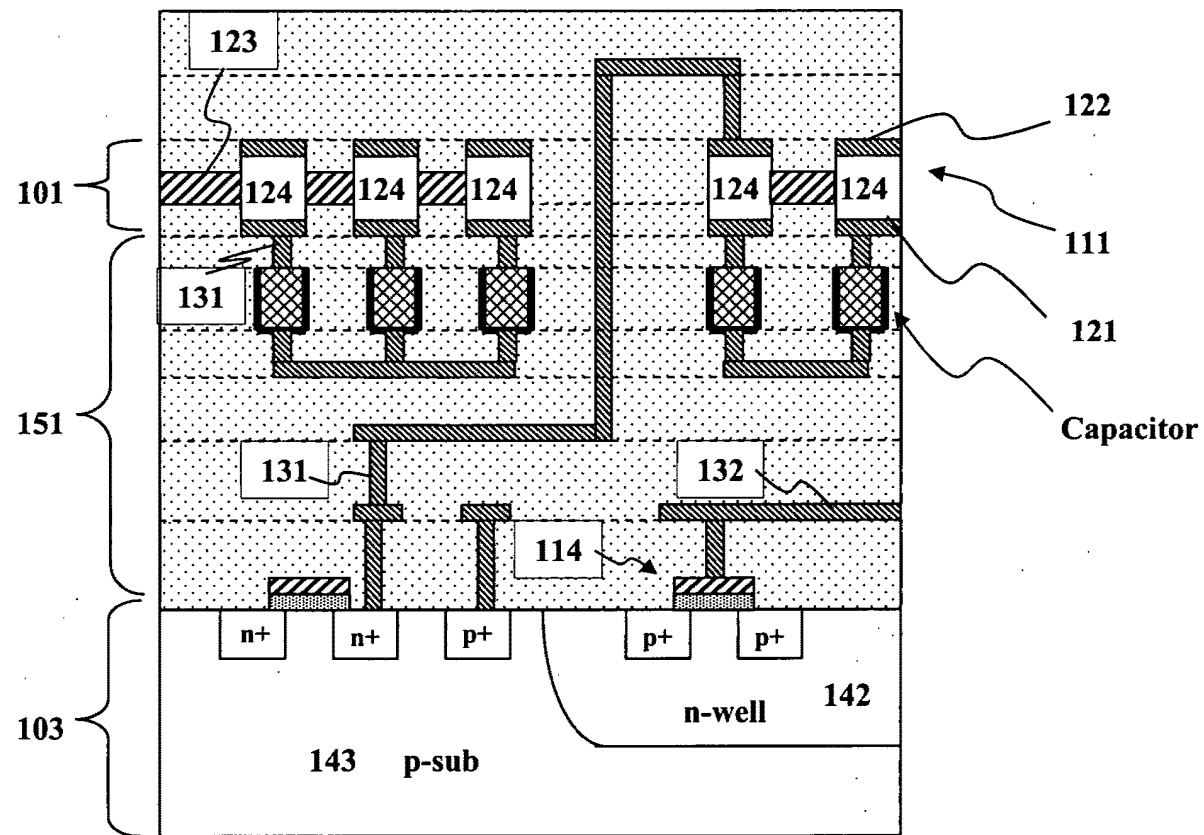


Fig. 10

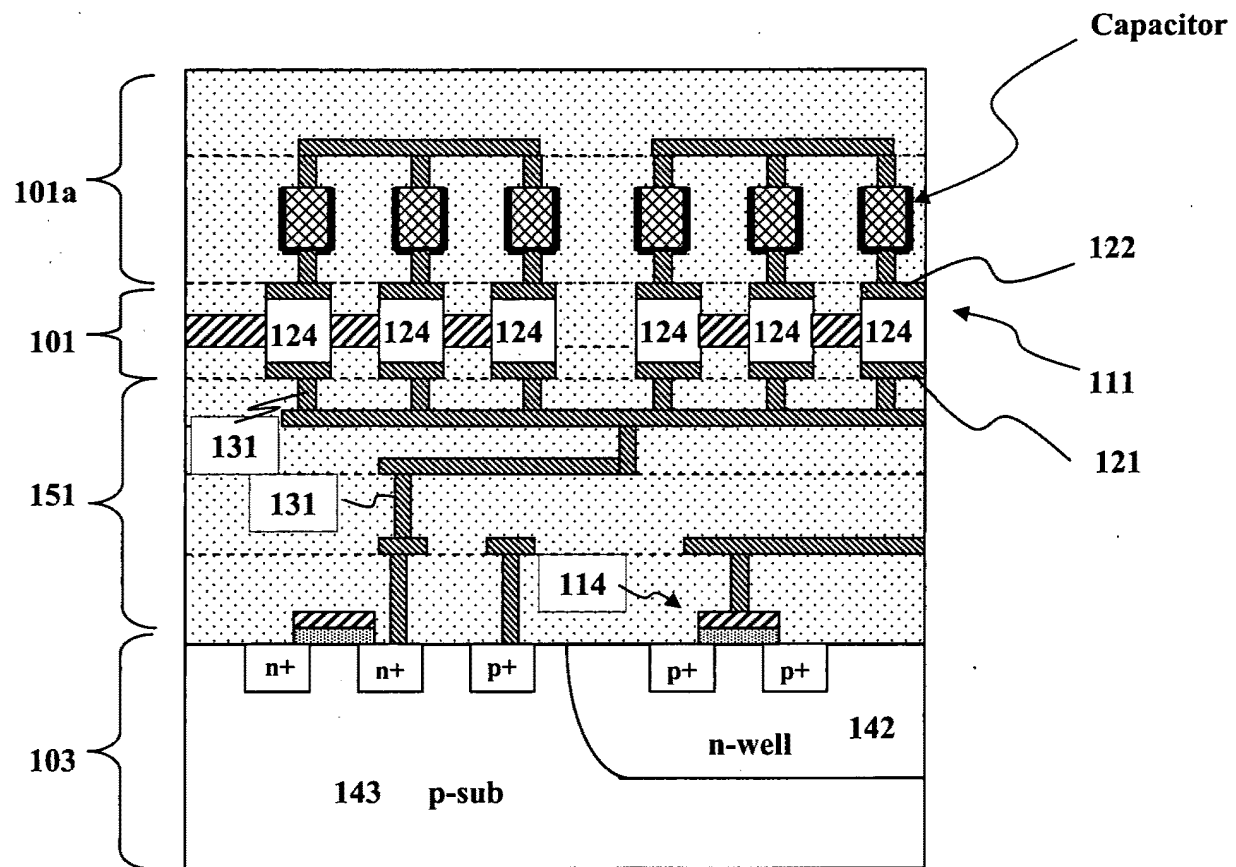


Fig. 11

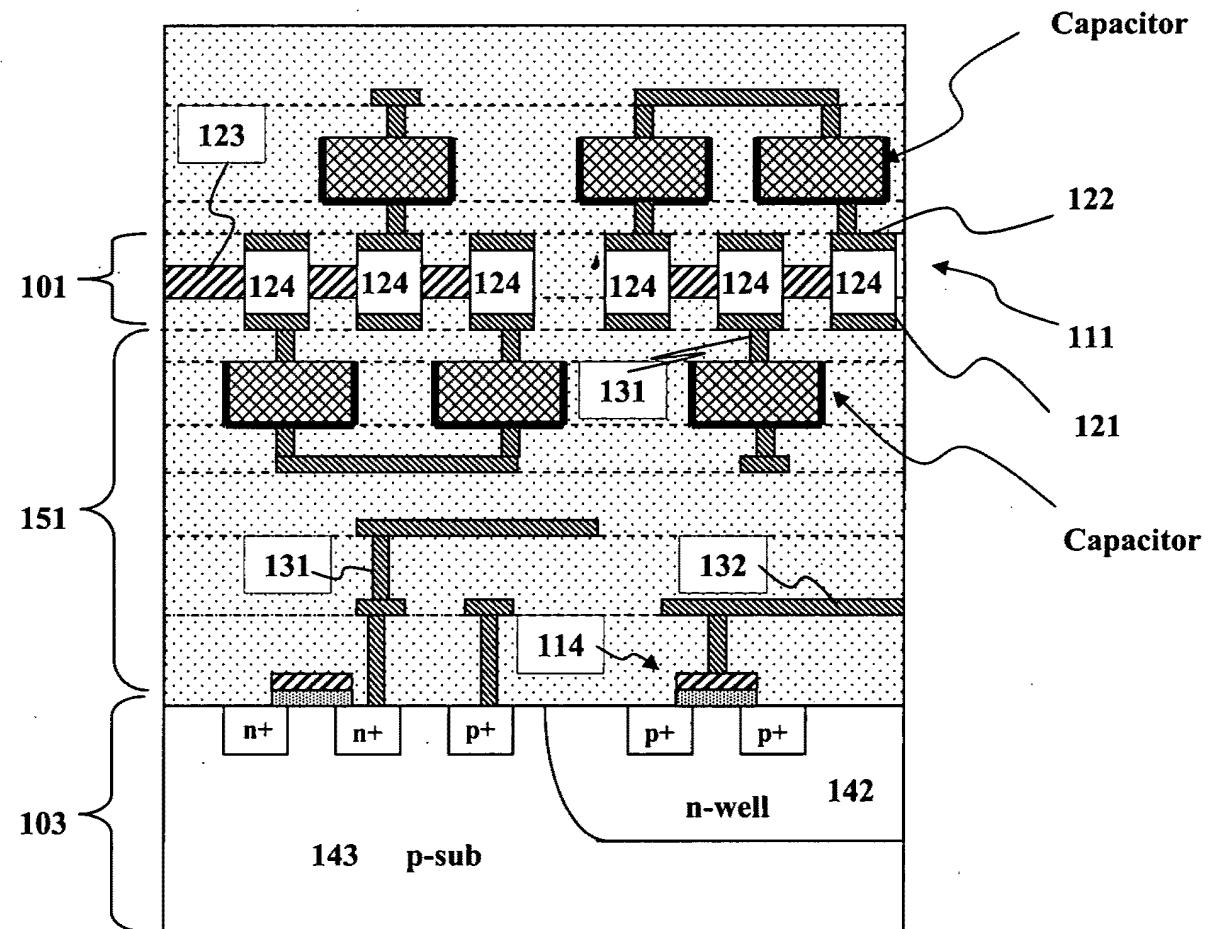


Fig. 12

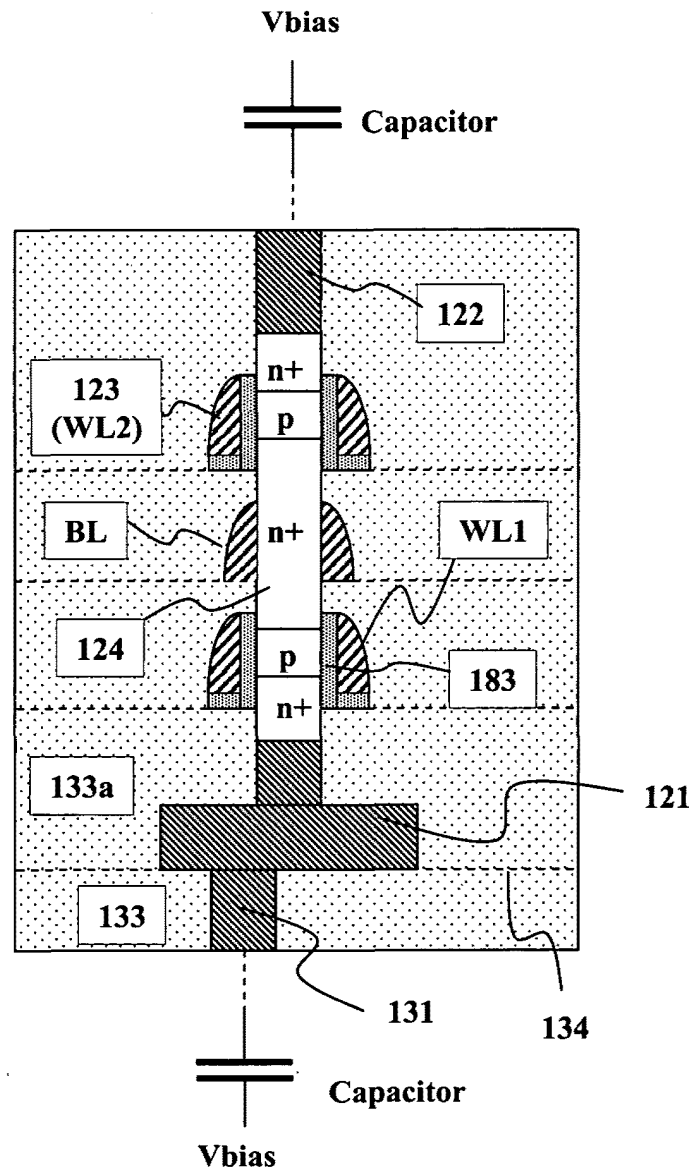


Fig. 13

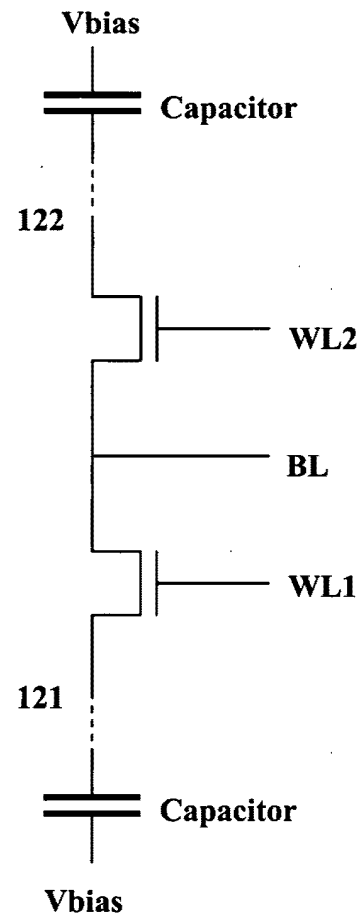


Fig. 14

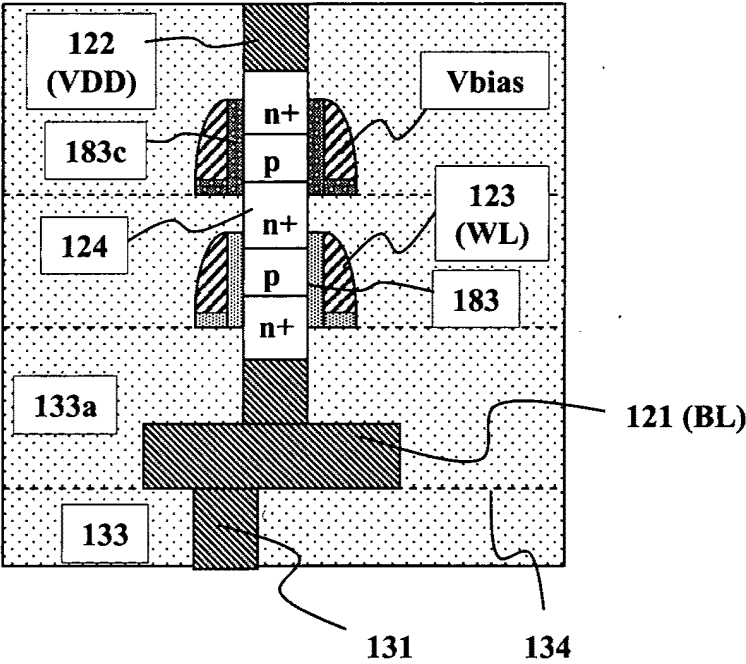


Fig. 15

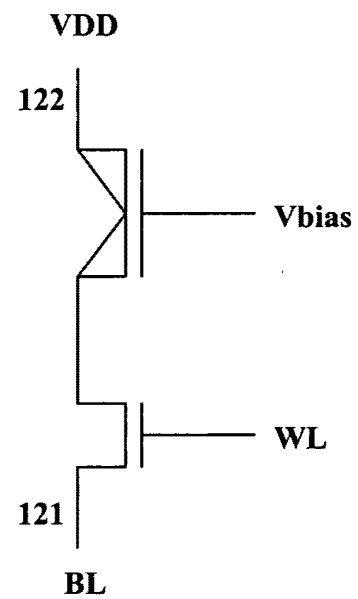


Fig. 16

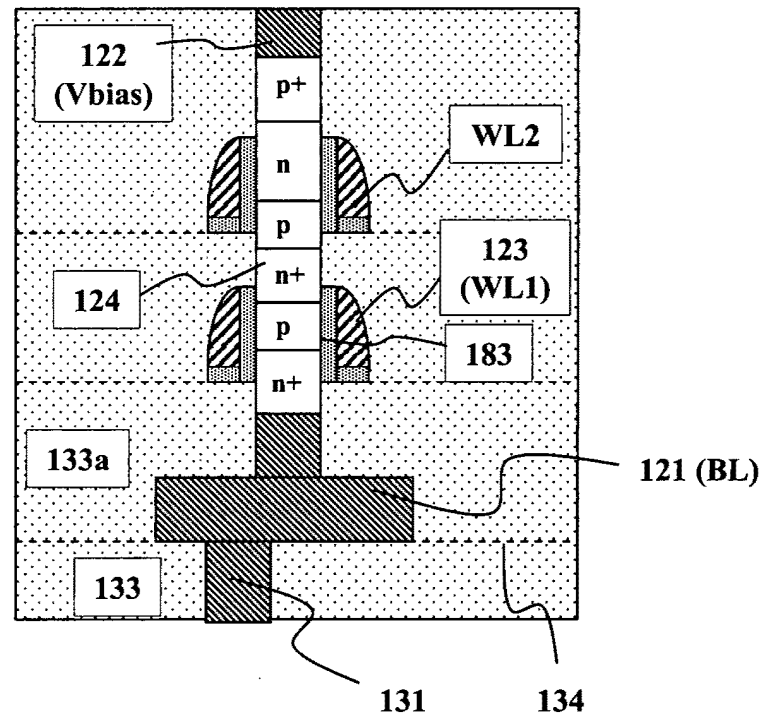


Fig. 17

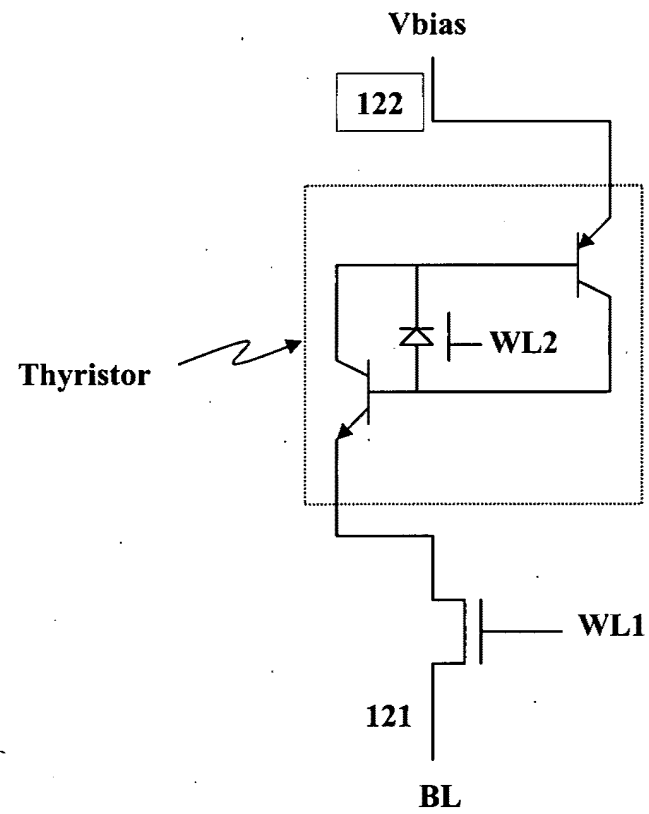


Fig. 18

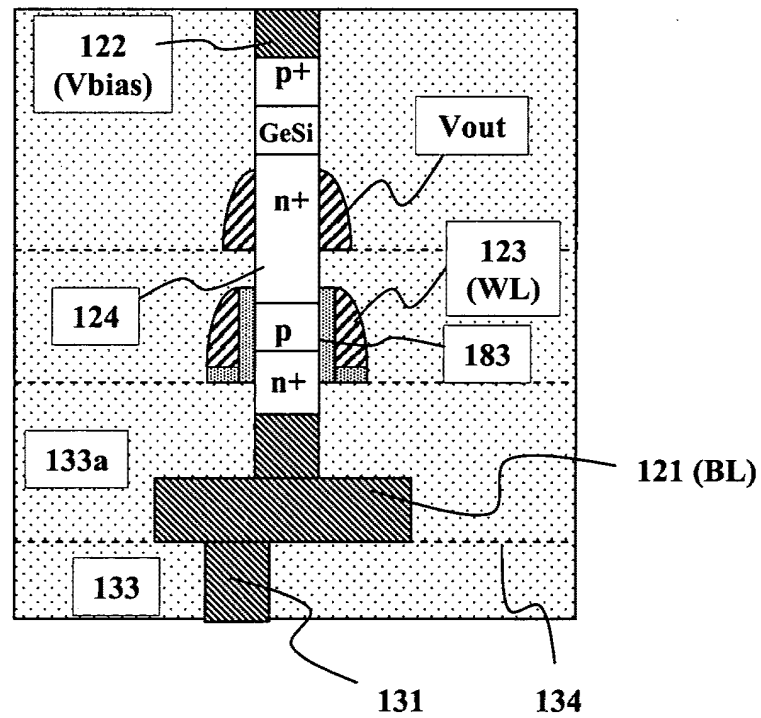


Fig. 19

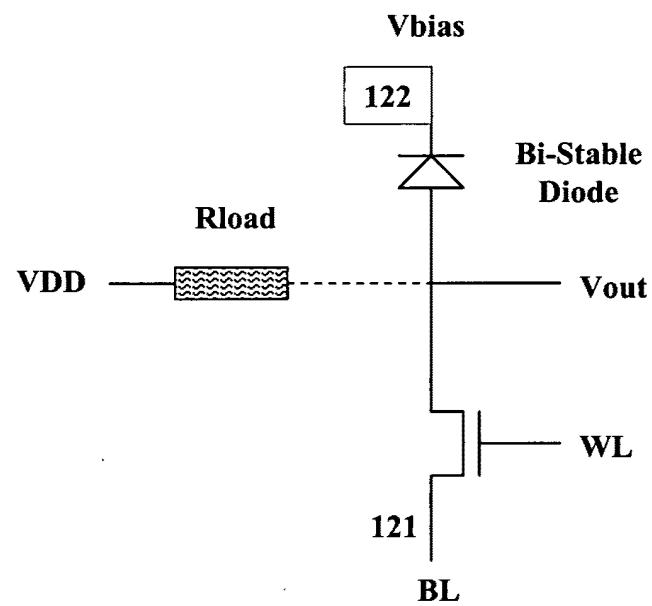


Fig. 20

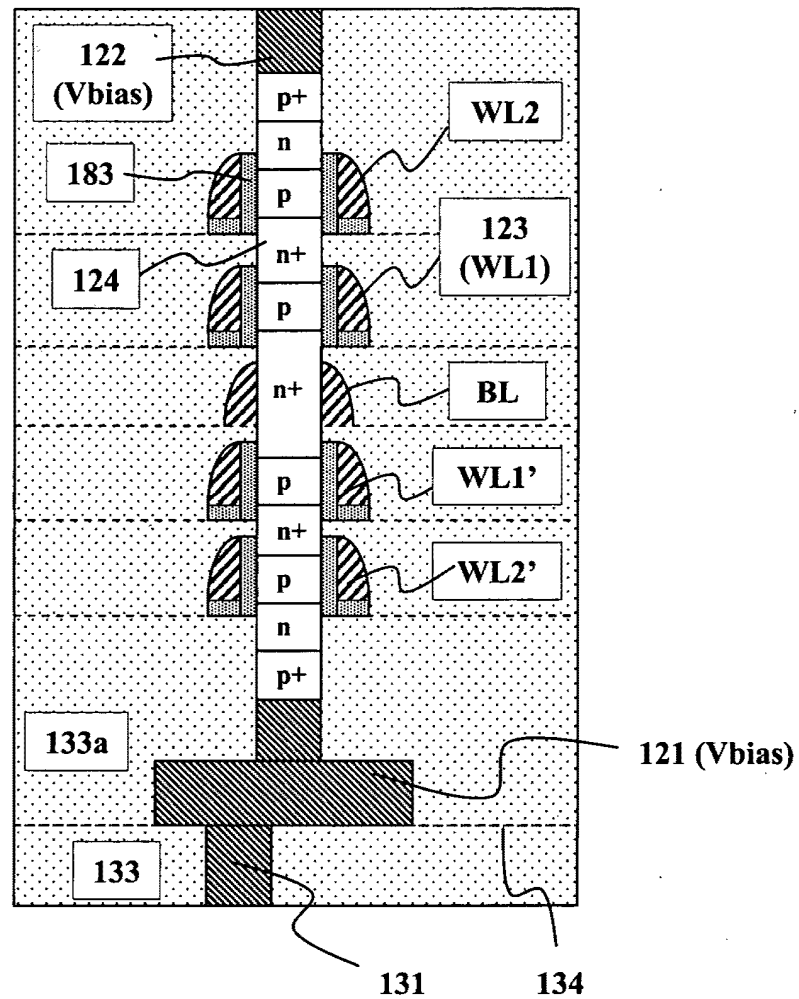


Fig. 21

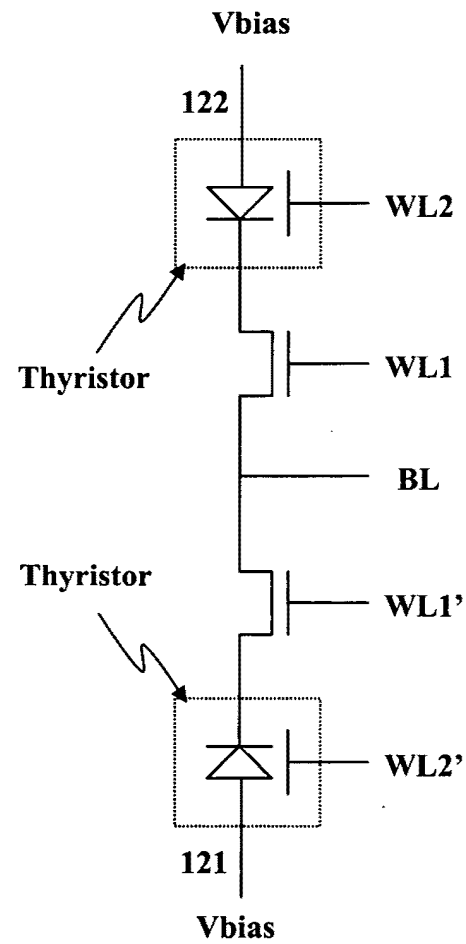


Fig. 22

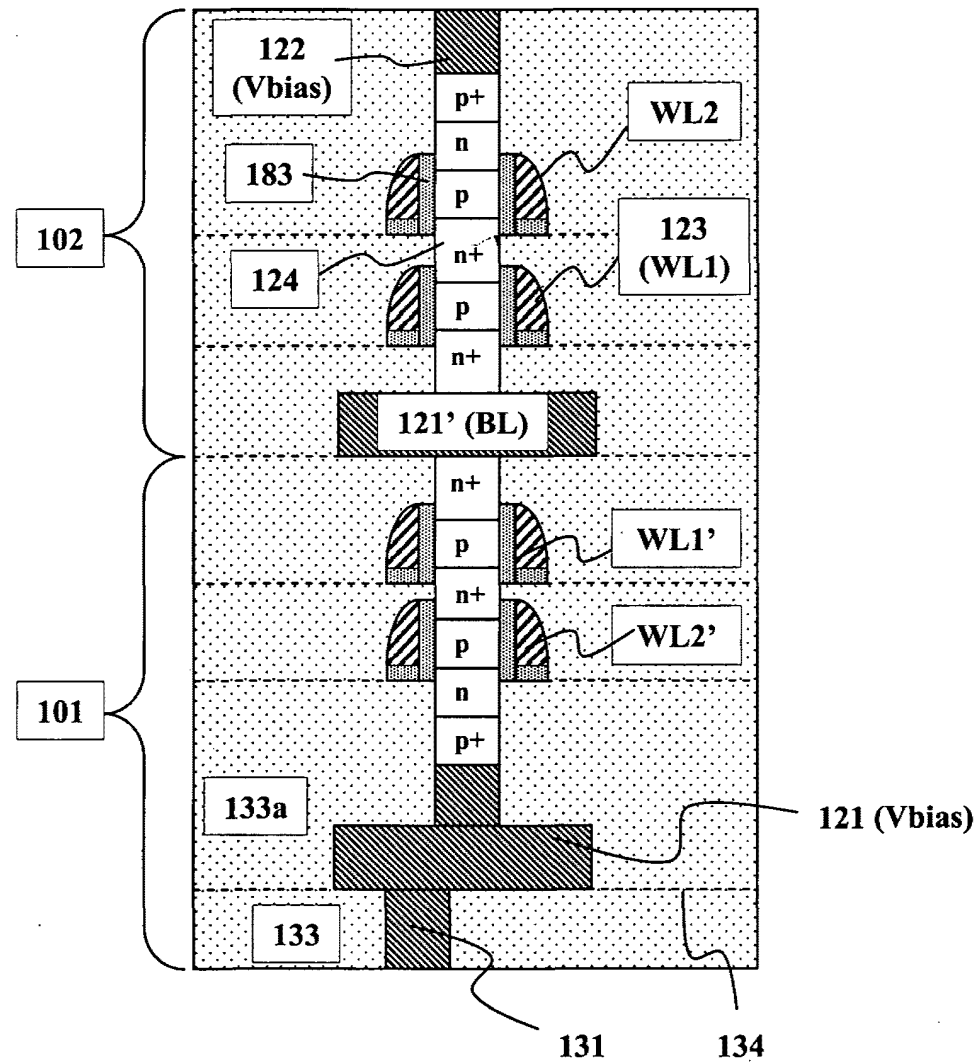


Fig. 23

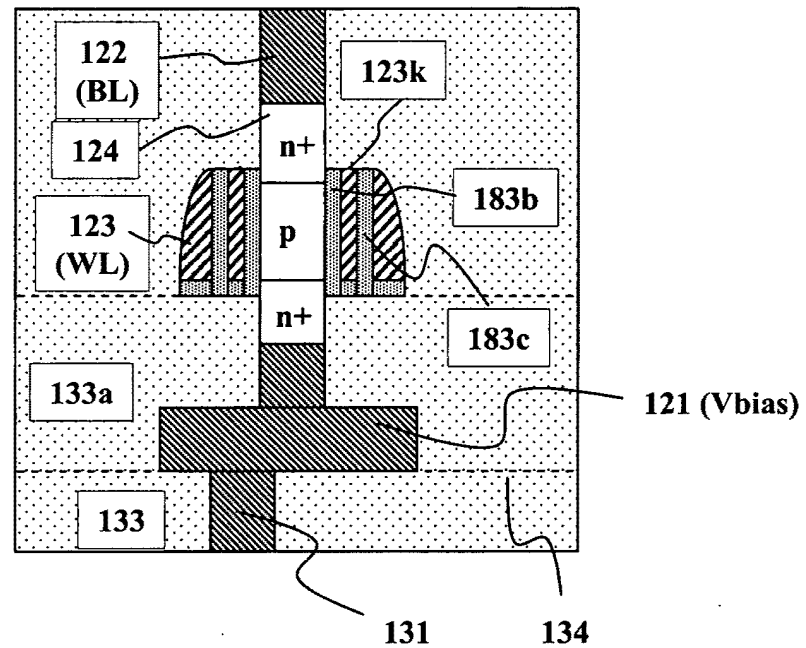


Fig. 24

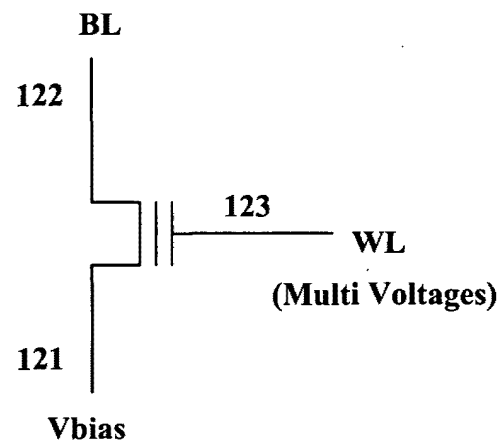


Fig. 25

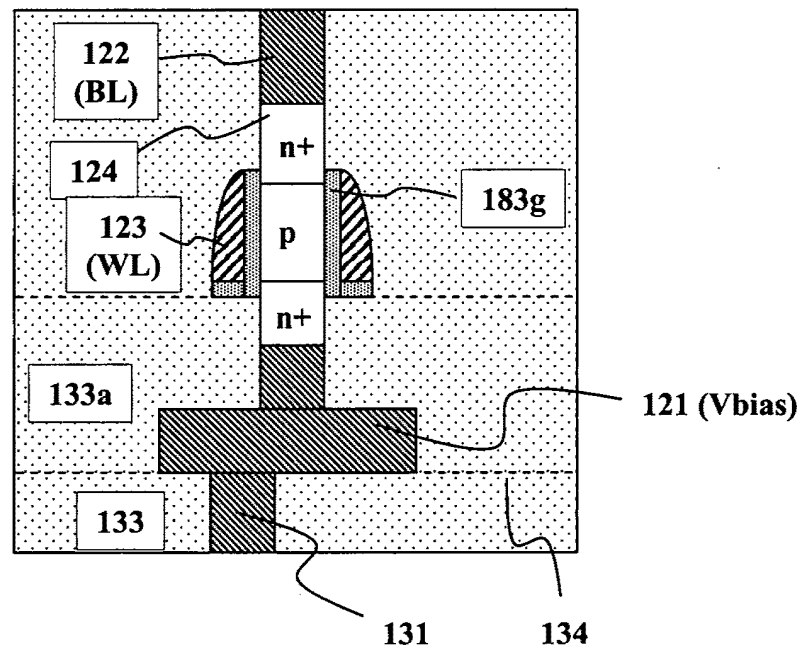


Fig. 26

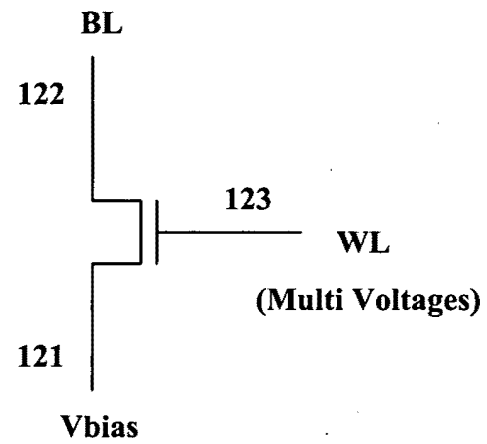


Fig. 27

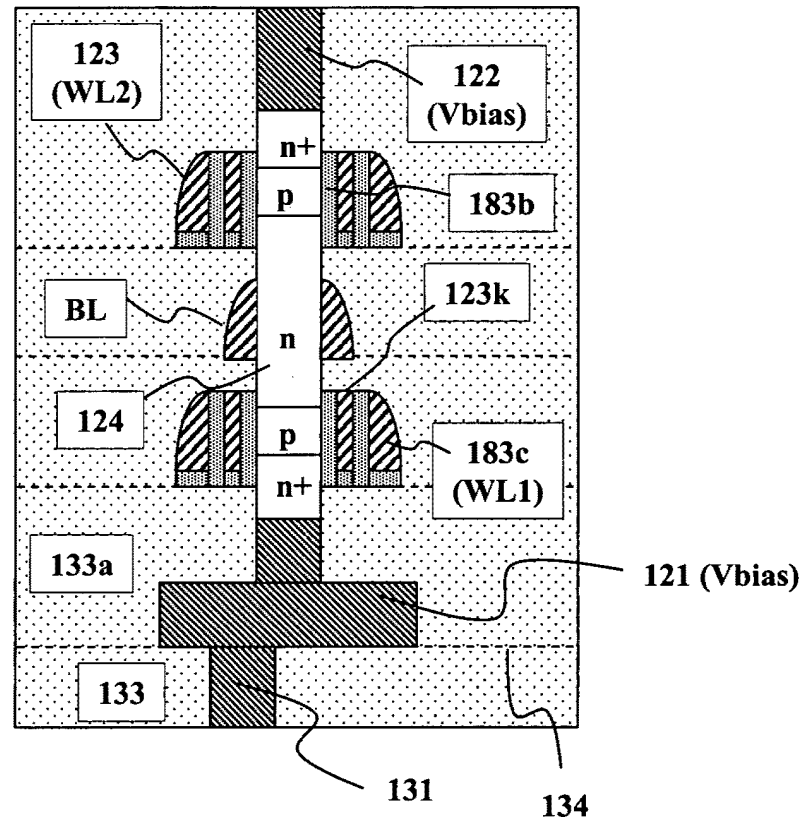


Fig. 28

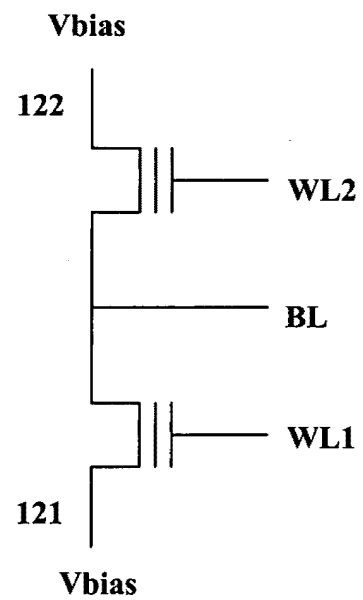


Fig. 29

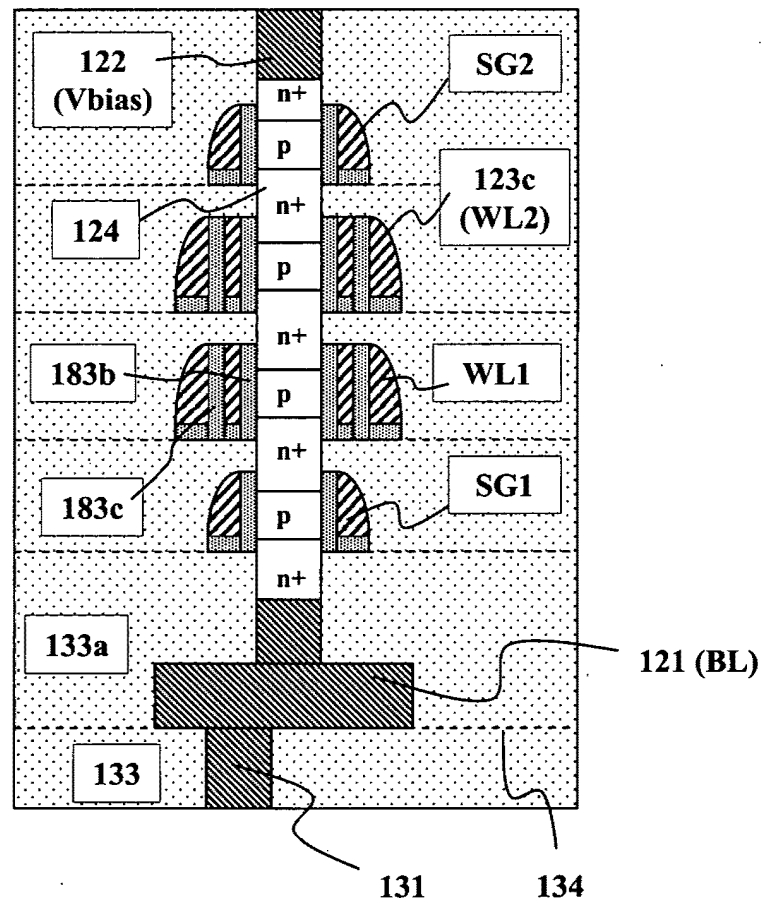


Fig. 30

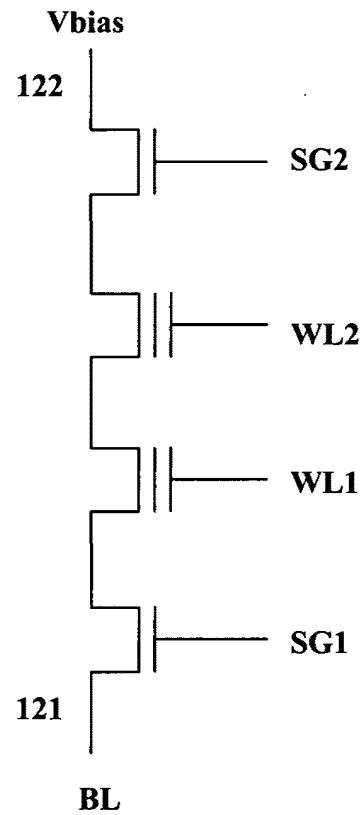


Fig. 31

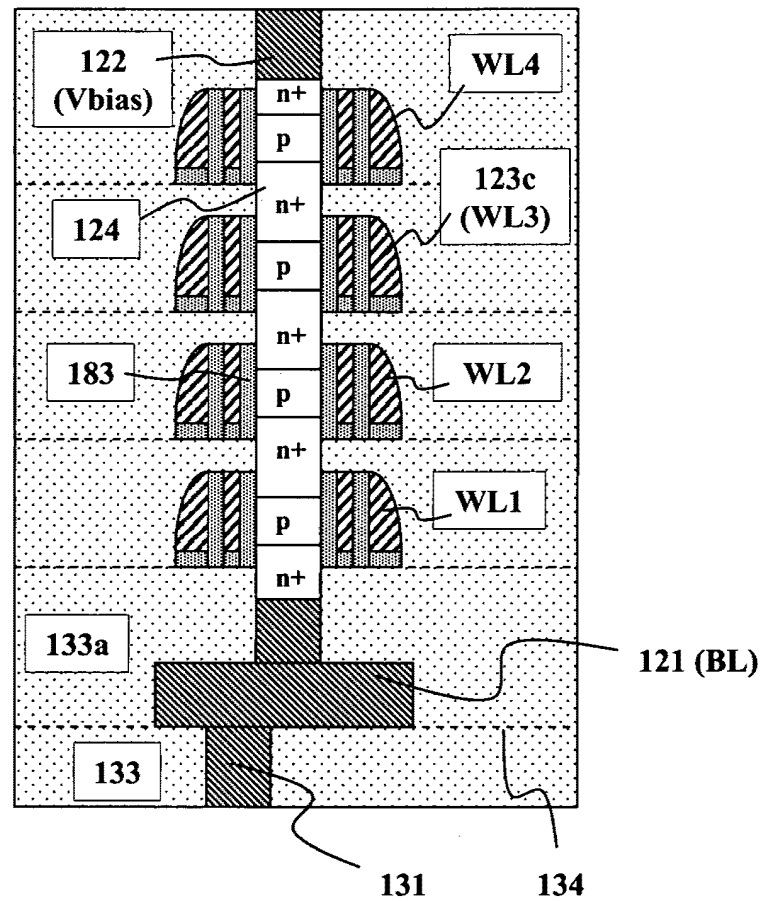


Fig. 32

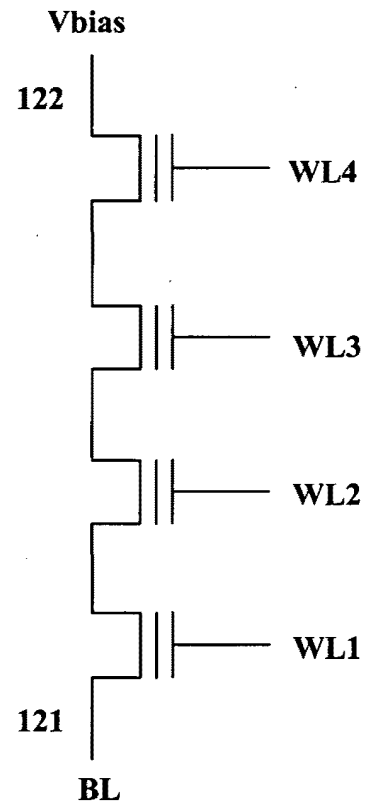


Fig. 33

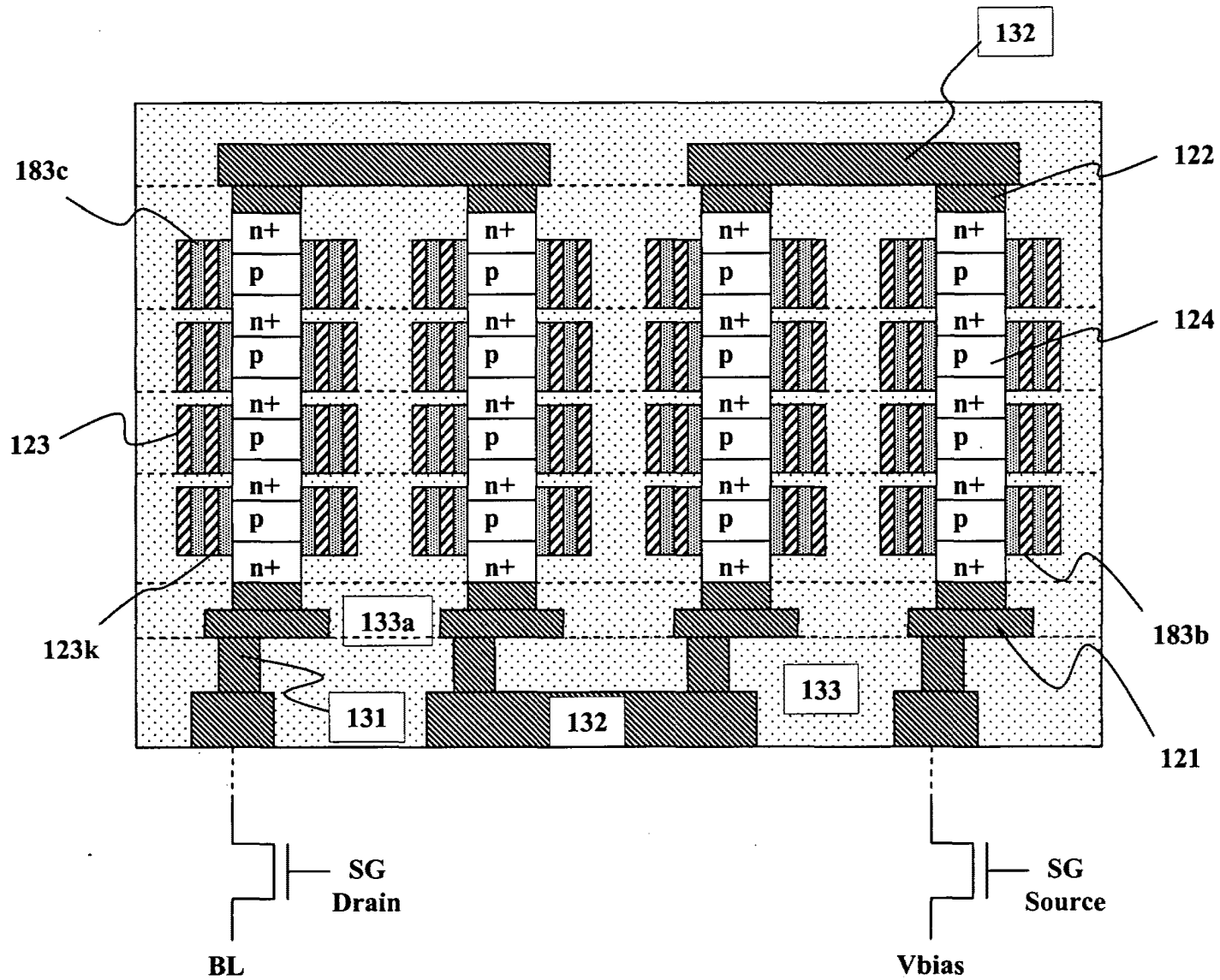
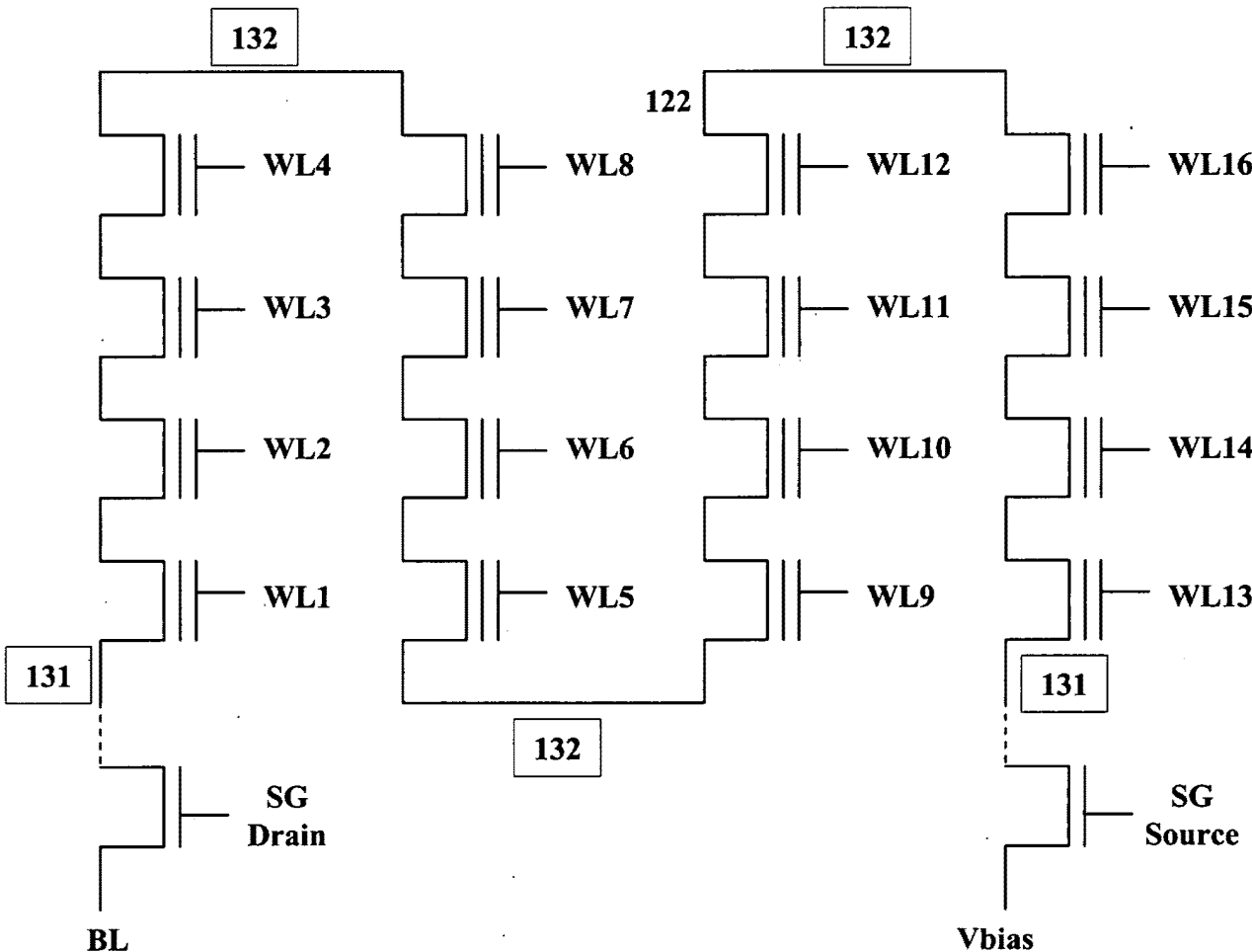


Fig. 34



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Declaration
Submitted
With Initial
Filing

OR

Declaration
Submitted after Initial
Filing (surcharge
(37 CFR 1.16 (e))
required)

Attorney Docket Number

BeSang, P001X1

First Named Inventor

Sang-Yun Lee

COMPLETE IF KNOWN

Application Number

N/A

Filing Date

03 September 2004

Art Unit

N/A

Examiner Name

N/A

I hereby declare that:

Each inventor's residence, mailing address, and citizenship are as stated below next to their name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Vertical Memory Device Structures

(Title of the Invention)

the specification of which



is attached hereto

OR



was filed on (MM/DD/YYYY)

as United States Application Number or PCT International

Application Number

and was amended on (MM/DD/YYYY)

(if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

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Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				Yes	No
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

[Page 1 of 2]

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or Surname **Lee**Inventor's
Signature **Sangyun Lee**Date **9/3/04**Residence: City **Beaverton**State **OR**Country **USA**

Citizenship

Mailing Address **17082 N.W. Elk Run Drive**City **Beaverton,**State **OR**ZIP **97006**Country **USA**NAME OF SECOND INVENTOR: ☐ A petition has been filed for this unsigned inventorGiven Name
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Application Number	N/A
Filing Date	03 SEPTEMBER 2004
First Named Inventor	Sang-Yun Lee
Title	Vertical Memory Device...
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	BeSang-P001X1

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☐ Practitioner(s) named below:

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as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.

Please recognize or change the correspondence address for the above-identified application to:

☐ The address associated with the above-mentioned Customer Number:

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
Address					
City		State		Zip	
Country					
Telephone		Fax			

I am the:

☒ Applicant/Inventor.

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

SIGNATURE of Applicant or Assignee of Record

Signature	<i>Sang-Yun Lee</i>	Date	03 SEPT 2004
Name	Sang-Yun Lee	Telephone	
Title and Company			

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

09/08/2004 FHETEKI1 00000049 10934270

01 FC:2001

385.00 OP

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-257/59033

PATENT APPLICATION FEE DETERMINATION RECORD

Effective October 1, 2003

Application or Docket Number

1093 6270

CLAIMS AS FILED - PART I

(Column 1) (Column 2)

TOTAL CLAIMS	17	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	17 minus 20 =	0
INDEPENDENT CLAIMS	3 minus 3 =	0
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
XS 9=	
X43=	
+145=	
TOTAL	385

RATE	FEE
BASIC FEE	770.00
XS18=	
X86=	
+290=	
TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

(Column 1) (Column 2) (Column 3)

AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

(Column 1) (Column 2) (Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

(Column 1) (Column 2) (Column 3)

AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total	*	Minus	**	=
	Independent	*	Minus	***	=
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐				

RATE	ADDITIONAL FEE
XS 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
XS18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

What is Claimed is:

- 126
Bule
1. A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and
a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;
wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate; and wherein the memory cell is a DRAM having at least one transistor.
 2. The semiconductor structure of Claim 1, wherein the vertically oriented memory cell comprises a vertical transistor and a serially connected capacitor in a SOI pillar.
 3. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises a vertical transistor in an SOI pillar and a capacitor connected in series therewith, the capacitor disposed external to the first stackable add-on layer.
 4. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises a first capacitor, a first access

transistor serially connected to the first capacitor, a second access transistor serially connected to the first access transistor, and a second capacitor serially connected to the second access device; wherein the first capacitor, the first access transistor, the second access transistor, and the second capacitor are all formed in a single vertically oriented SOI pillar.

5. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically oriented, serially connected transistors formed on a SOI pillar, the serially connected transistors further connected to a capacitor disposed external to the stackable add-on layer.

6. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically and serially connected transistors and a shared serially connected capacitor in a SOI pillar.

7. The semiconductor memory structure of Claim 1, wherein the vertically oriented semiconductor memory cell comprises:

a first diode;

a first access transistor connected in series to the first diode;

a second access transistor connected in series to the first access transistor;

a third access transistor connected in series to the second access transistor;

a fourth access transistor connected in series to the third access transistor;

and

a second diode connected in series to the fourth access transistor;

wherein the first diode, the first, second, third, and fourth transistors, and the second diode are formed on the same SOI pillar.

8. A semiconductor memory structure, comprising:

a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate;

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material; and

the stackable add-on layer to a layer of the substrate that is the greatest distance from the substrate;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate; and wherein the memory cell is an SRAM having at least one Negative Differential Resistance device.

9. The semiconductor memory structure of Claim 8, wherein the vertically oriented semiconductor memory cell comprises a vertically oriented transistor and a vertically oriented NDR-type Thyristor serially connected to each other.

10. The semiconductor memory structure of Claim 9, wherein the vertically oriented transistor is formed on an SOI pillar and the vertically NDR-type Thyristor is formed on an SOI pillar.

11. The semiconductor memory structure of Claim 9, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on two separated SOI pillars.

12
13. The semiconductor memory structure of Claim 8, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on the same SOI pillar.

13
14. A semiconductor memory structure, comprising:

• a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate;

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material; and

the stackable add-on layer to a layer of the substrate that is the greatest distance from the substrate;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate; and wherein the memory cell is a nonvolatile memory having at least one transistor.

14
15. The semiconductor memory structure of Claim 14, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

13

¹⁵
~~16.~~ The semiconductor memory structure of Claim ¹³~~14~~, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

¹⁶
~~17.~~ The semiconductor memory structure of Claim ¹³~~14~~, wherein at least two nonvolatile memory cells are vertically and serially connected on a first SOI pillar.

¹⁷
~~18.~~ The semiconductor memory structure of Claim ¹⁶~~17~~, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected by an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell on a second SOI pillar.



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 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
10/934,270	09/03/2004	Sang-Yun Lee	BeSang.P001X1

000041536
 RAYMOND J. WERNER
 2056 NW ALOCLEK DRIVE, SUITE 314
 HILLSBORO, OR 97124

CONFIRMATION NO. 5732

FORMALITIES LETTER



OC000000014242557

Date Mailed: 10/29/2004

NOTICE OF INFORMAL APPLICATION

This application is considered to be informal since it does not comply with the regulations for the reason(s) indicated below. The period within to correct the informalities noted below and avoid abandonment is set in the accompanying Office action.

Items Required To Avoid Processing Delays:

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A new oath or declaration, identifying this application number is required. The oath or declaration does not comply with 37 CFR 1.63 in that it:
- does not identify the citizenship of each inventor.

Replies should be mailed to: Mail Stop Missing Parts
 Commissioner for Patents
 P.O. Box 1450
 Alexandria VA 22313-1450

*A copy of this notice **MUST** be returned with the reply.*

Customer Service Center
 Initial Patent Examination Division (703) 308-1202

PART 1 - ATTORNEY/APPLICANT COPY

CLAIMS ONLY							Application Number 10/934270		Filing Date		
							Applicant(s)				
							* May be used for additional claims or amendments				
CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT						
	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend	Indep	Depend	
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Total Depend		←		←		←		←		←	
Total Claims											

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2763	(3-D near integrated near circuit (three adj dimensional and integrated adj circuit)) and stack\$3 and vertical\$2 and memory and stack\$4	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2006/02/11 09:58
L2	2210	(3-D near integrated near circuit (three adj dimensional and integrated adj circuit)) and stack\$3 and vertical\$2 and memory and stack\$4 and semiconductor	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2006/02/11 09:59



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BeSang.P001X1	5732
41536	7590	03/01/2006	EXAMINER	
RAYMOND J. WERNER 2056 NW ALOCLEK DRIVE, SUITE 314 HILLSBORO, OR 97124			TRAN, MAI HUONG C	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

87✓

Office Action Summary	Application No.		Applicant(s)	
	10/934,270		LEE, SANG-YUN	
	Examiner		Art Unit	
	Mai-Huong Tran		2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Claim Objections

Claim 1, 8, and 14 are objected to for the unclear recitation: "...that is the greatest distance from the substrate..." which can make it to become indefinite.

It is unclear what distance that the applicant refers to.

Applicant is required to amend the claim so that the claim will be in acceptable form to clearly define the meter and bound of the invention that the Applicant wishes to have patent protection from the Office. The examiner suggests the applicant amends the last recitation of claims 1, 8, and 14 to "...that is the greatest distance from the substrate **measuring from the bottom surface of the substrate...**".

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1–18 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-20 of U.S. Application No. 10/873,969. Although the conflicting claims are not identical, they are not patentably distinct from each other because the subject matter claimed in the instant application is fully disclosed in the application 10/873,969 and is covered by the application 10/873,969 since both applications are claiming common subject matter, as follows:

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material; wherein the stackable add-on layer is bonded to layer of the substrate that is the greatest distance from the substrate, and wherein the memory cell is a DRAM having at least one transistor; and wherein the memory cell is an

SRAM having at least one Negative Differential Resistance device; and wherein the memory cell is a nonvolatile memory having at least one transistor.

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mai-Huong Tran

Notice of References Cited	Application/Control No. 10/934,270	Applicant(s)/Patent Under Reexamination LEE, SANG-YUN	
	Examiner Mai-Huong Tran	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,943,067	09-2005	Greenlaw, David	438/152
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims



Application/Control No.

10/934,270

Examiner

Mai-Huong Tran

Applicant(s)/Patent under Reexamination

LEE, SANG-YUN

Art Unit

2818

✓	Rejected
≡	Allowed

—	(Through numeral) Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date									
Final	Original	2/11/06									
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Bib Data Sheet

CONFIRMATION NO. 5732

SERIAL NUMBER 10/934,270	FILING DATE 09/03/2004 RULE	CLASS 257	GROUP ART UNIT 2818	ATTORNEY DOCKET NO. BeSang.P001X1
-----------------------------	---------------------------------------	--------------	------------------------	---

APPLICANTS

Sang-Yun Lee, Beaverton, OR;

** CONTINUING DATA *****
 This application is a CIP of 10/873,969 06/21/2004 *yes*

** FOREIGN APPLICATIONS ***** *none*

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **
 ** 10/29/2004

Foreign Priority claimed ☐ yes ☒ no	STATE OR COUNTRY OR	SHEETS DRAWING 34	TOTAL CLAIMS 17	INDEPENDENT CLAIMS 3
35 USC 119 (a-d) conditions met ☐ yes ☒ no ☐ Met after Allowance				
Verified and Acknowledged	Examiner's Signature <i>[Signature]</i> Initials			

ADDRESS
 000041536
 RAYMOND J. WERNER
 2056 NW ALOCLEK DRIVE, SUITE 314
 HILLSBORO , OR
 97124

TITLE
 Vertical memory device structures

FILING FEE RECEIVED 385	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____
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Search Notes

Application/Control No.

10/934,270

Examiner

Mai-Huong Tran

Applicant(s)/Patent under
Reexamination

LEE, SANG-YUN

Art Unit

2818

SEARCHED

Class	Subclass	Date	Examiner
438	152, 153	2/11/2006	MT
257	118, 199		

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
EAST	2/11/2006	MT

07-31-06

IFW
#



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

Confirmation No.: 5732

Serial No.: 10/934,270

Examiner: Tran, Mai Huong C

Filed: September 3, 2004

Docket No.: BeSang.P001X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT TRANSMITTAL

Sir:

Transmitted herewith is an amendment for this application along with a Petition for a two-month extension of time and a Terminal Disclaimer. Applicant is a small entity.

Enclosed is Check No. 1066 in the amount of \$225.00 for the two-month extension of time and Check No. 1067 in the amount of \$65.00 for the terminal disclaimer. A duplicate copy of this transmittal is attached.

Respectfully submitted,

Dated: July 27, 2006

Sangyun Lee
Sang-Yun Lee
Applicant and Inventor

BeSang, Inc.
15188 NW Central Dr. Ste. #213
Portland, OR 97229
Phone) 503-533-5150
Fax) 503-533-5150



Express Mail Mailing Label: EQ 749731910 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

Confirmation No.: 5732

Serial No.: 10/934,270

Examiner: Tran, Mai Huong C

Filed: September 3, 2004

Docket No.: BeSang.P001X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action mailed March 1, 2006, please amend and reconsider the above-identified application as follows:

Amendments to the Specification there are no amendments to the specification.

Amendments to the Claims begin on Page 2 of this paper.

Amendments to the Drawings- there are no amendments to the drawings.

Remarks/Arguments begin on Page 7 of this paper.

AMENDMENTS TO THE CLAIMS

Please amend Claims 1-18 as shown. A listing of the claims is provided below and will replace all prior versions and listings of the claims in the application.

Listing of the Claims:

1. (amended) A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and
a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;
wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and
wherein the memory cell is a DRAM having at least one transistor.
2. (amended) The semiconductor memory structure of claim 1, wherein the vertically oriented memory cell comprises a vertical transistor and a serially connected capacitor in a SOI pillar.
3. The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises a vertical transistor in an SOI pillar and a capacitor connected in series therewith, the capacitor disposed external to the first stackable add-on layer.

4. (amended) The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises:

- a first capacitor,
- a first access transistor serially connected to the first capacitor,
- a second access transistor serial connected to the first access transistor, and
- a second capacitor serially connected to the second access transistor [device];

wherein the first capacitor, the first access transistor, the second access transistor, and the second capacitor are all formed in a single vertically oriented SOI pillar.

5. The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically oriented, serially connected transistors formed on a SOI pillar, the serially connected transistors further connected to a capacitor disposed external to the stackable add-on layer.

6. The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically and serially connected transistors and a shared serially connected capacitor in a SOI pillar.

7. The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises:

- a first diode;
- a first access transistor connected in series to the first diode;
- a second access transistor connected in series to the first access transistor;
- a third access transistor connected in series to the second

access transistor; a fourth access transistor connected in series to the third access transistor; and

a second diode connected in series to the fourth access transistor;

wherein the first diode, the first, second, third, and fourth transistors, and the second diode are formed on the same SOI pillar.

8. (amended) A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate;

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material; and

~~the stackable add-on layer to a layer of the substrate that is the greatest distance from the substrate;~~

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and

wherein the memory cell is an SRAM having at least one Negative Differential Resistance device.

9. The semiconductor memory structure of claim 8, wherein the vertically oriented semiconductor memory cell comprises a vertically oriented transistor and a vertically oriented NDR-type Thyristor serially connected to each other.

10. The semiconductor memory structure of claim 9, wherein the vertically oriented transistor is formed on an SOI pillar and the vertically NDR-type Thyristor is formed on an SOI pillar.

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11. The semiconductor memory structure of claim 9, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on two separated SOI pillars.

13. The semiconductor memory structure of claim 8, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on the same SOI pillar.

14. (amended) A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having ~~at least one~~ a dielectric layer ~~and at least one interconnect layer~~ disposed above the substrate electrical devices;
a [first] stackable add-on layer, ~~the first stackable add-on layer including~~ having a plurality of vertically oriented semiconductor memory cells ~~disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material~~; and
the stackable add-on layer being bonded to a ~~layer of the substrate that is the greatest distance from the substrate~~ the dielectric layer;
~~wherein the stackable add-on layer [is] being bonded to a layer of the substrate that is the greatest distance from the substrate~~; and
wherein the memory cells [is] are [a] nonvolatile memory cells having at least one transistor.

15. (amended) The semiconductor memory structure of claim 14, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

16. (amended) The semiconductor memory structure of claim 14, wherein the vertically oriented semiconductor nonvolatile memory

Express Mail Mailing Label: EQ 749731910 US

cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

17. (amended) The semiconductor memory structure of claim 14, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with [on] a first SOI pillar.

18. (amended) The semiconductor memory structure of claim 17, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected [by] with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with [on] a second SOI pillar.

Remarks/Arguments

Entry of the foregoing amendments and reconsideration of this application is respectfully requested. By this amendment, Claims 1, 2, 4, 8 and 14-18 have been amended to more clearly set forth the present invention and to rectify certain informalities pointed out by the Examiner. These amendments do not introduce any new matter into the application and are not being made for reasons related to patentability.

The applicant believes that Claims 1-11 and 13-18 are in condition for allowance and notice to that effect is respectfully requested. The applicant points out that the claim numbering in the originally filed application inadvertently left out Claim 12.

Respectfully submitted,

Dated: July 27, 2006

Sang-Yun Lee
Sang-Yun Lee
Applicant and Inventor

BeSang, Inc.
15188 NW Central Dr. Ste. #213
Portland, OR 97229
Phone) 503-533-5150
Fax) 503-533-5150



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

Confirmation No.: 5732

Serial No.: 10/934,270

Examiner: Tran, Mai Huong C

Filed: September 3, 2004

Docket No.: BeSang.P001X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TERMINAL DISCLAIMER

Sir:

The owner and inventor, Sang-Yun Lee of one-hundred per cent interest in the above-identified patent (the "instant patent") hereby disclaims, except as provided below, the terminal part of the patent term that extends beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 to 156 and 173, as presently shortened by any terminal disclaimer, of prior Patent Application 10/873,969, now U.S. Patent No. 7,052,941 (the "prior patent"), which is also owned by Sang-Yun Lee. The owner hereby agrees that the instant patent shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with the instant patent and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the instant patent that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 to 156 and 173 of the prior patent, as presently shortened by any terminal disclaimer, in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally

08/02/2006 WADDELRI 00000048 10934270 65.00 DP
01 FC:2814

disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

FEE PAYMENT

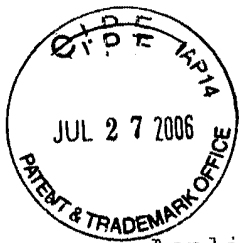
Please find enclosed Check No. 1067 in the sum of \$65.00 for a small-entity. A duplicate of this disclaimer is included.

Respectfully submitted,

Dated: July 27, 2006

Sangyun Lee
Sang-Yun Lee
Applicant and Inventor

BeSang, Inc.
15188 NW Central Dr. Ste. #213
Portland, OR 97229
Phone) 503-533-5150
Fax) 503-533-5150



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

Confirmation No.: 5732

Serial No.: 10/934,270

Examiner: Tran, Mai Huong

Filed: September 3, 2004

Docket No.: BeSang.P001.X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR EXTENSION

Sir:

In accordance with 37 CFR 1.136(a), it is requested that the due date for response to the March 1, 2006 Office Action in the above application be extended by two months, from June 1, 2006 to August 1, 2006.

Enclosed is our Check No. 1066 in the amount of \$225.00 to cover the required fee for the two-month extension under 37 CFR 1.17. A duplicate of this Petition is enclosed for the convenience of the Patent and Trademark Office.

08/02/2006 WABDELRI 00000047 10934270

01 FC:2252

225.00 OP

Respectfully submitted,

Dated: July 27, 2006

Sangyun Lee
Sang-Yun Lee
Applicant and Inventor

BeSang, Inc.
15188 NW Central Dr. Ste. #213
Portland, OR 97229
Phone) 503-533-5150
Fax) 503-533-5150

Application Number 	Application No. 10/934,270	Applicant(s) LEE, SANG-YUN	
	Terminal Disclaimer Filed: 07/27/06		

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Document Code - DISQ	This patent is subject to a Terminal Disclaimer	Reasons:
INTERNAL DOCUMENT – DO NOT MAIL		

U.S. Patent and Trademark Office

NOTE DISCLAIMER:

The term of this patent shall not extend
beyond the expiration date of Pat. No. 7,052,941, , , .

☒ **SHARON S. HOPPE**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **RENEE M. PRESTON**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **TREDELLE D. JACKSON**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **NOVA M. CHAPMAN**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **CASSANDRA B. PARIS**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BeSang.P001X1	5732
41536	7590	08/09/2006	EXAMINER	
RAYMOND J. WERNER 2056 NW ALOCLEK DRIVE, SUITE 314 HILLSBORO, OR 97124			HUYNH, ANDY	
			ART UNIT	PAPER NUMBER

2818

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Notice of Non-Compliant
Amendment (37 CFR 1.121)**

Application No.
10/934270

Applicant(s)

Examiner
Huynh, Andy

Art Unit
2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The amendment document filed on **7/27/04** is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121 or 1.4. In order for the amendment document to be compliant, correction of the following item(s) is required.

THE FOLLOWING MARKED (X) ITEM(S) CAUSE THE AMENDMENT DOCUMENT TO BE NON-COMPLIANT:

- ☐ 1. Amendments to the specification:
- ☐ A. Amended paragraph(s) do not include markings.
 - ☐ B. New paragraph(s) should not be underlined.
 - ☐ C. Other _____.
- ☐ 2. Abstract:
- ☐ A. Not presented on a separate sheet. 37 CFR 1.72.
 - ☐ B. Other _____.
- ☐ 3. Amendments to the drawings:
- ☐ A. The drawings are not properly identified in the top margin as "Replacement Sheet," "New Sheet," or "Annotated Sheet" as required by 37 CFR 1.121(d).
 - ☐ B. The practice of submitting proposed drawing correction has been eliminated. Replacement drawings showing amended figures, without markings, in compliance with 37 CFR 1.84 are required.
 - ☐ C. Other _____.
- ☒ 4. Amendments to the claims:
- ☐ A. A complete listing of all of the claims is not present.
 - ☐ B. The listing of claims does not include the text of all pending claims (including withdrawn claims)
 - ☒ C. Each claim has not been provided with the proper status identifier, and as such, the individual status of each claim cannot be identified. Note: the status of every claim must be indicated after its claim number by using one of the following status identifiers: (Original), (Currently amended), (Canceled), (Previously presented), (New), (Not entered), (Withdrawn) and (Withdrawn-currently amended).
 - ☐ D. The claims of this amendment paper have not been presented in ascending numerical order.
 - ☒ E. Other: **Claims 13-18 is Renumber As 12-17.**
- ☐ 5. Other (e.g., the amendment is unsigned or not signed in accordance with 37 CFR 1.4):

For further explanation of the amendment format required by 37 CFR 1.121, see MPEP § 714.

TIME PERIODS FOR FILING A REPLY TO THIS NOTICE:

1. Applicant is given **no new time period** if the non-compliant amendment is an after-final amendment, an amendment filed after allowance, or a drawing submission (only). If applicant wishes to resubmit the non-compliant after-final amendment with corrections, the **entire corrected amendment** must be resubmitted.
2. Applicant is given **one month**, or thirty (30) days, whichever is longer, from the mail date of this notice to supply the correction, if the non-compliant amendment is one of the following: a preliminary amendment, a non-final amendment (including a submission for a request for continued examination (RCE) under 37 CFR 1.114), a supplemental amendment filed within a suspension period under 37 CFR 1.103(a) or (c), and an amendment filed in response to a *Quayle* action. If any of above boxes 1. to 4. are checked, the correction required is only the **corrected section** of the non-compliant amendment in compliance with 37 CFR 1.121.

Extensions of time are available under 37 CFR 1.136(a) only if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action.

Failure to timely respond to this notice will result in:

Abandonment of the application if the non-compliant amendment is a non-final amendment or an amendment filed in response to a *Quayle* action; or

Non-entry of the amendment if the non-compliant amendment is a preliminary amendment or supplemental amendment.

Smith Smith
Legal Instruments Examiner (LIE), if applicable

(571) 272-1622
Telephone No.

PATENT APPLICATION FEE DETERMINATION RECORD
Effective December 8, 2004

Application or Docket Number

10/934270

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS		
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	minus 20 =	*
INDEPENDENT CLAIMS	minus 3 =	*
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

SMALL ENTITY
TYPE ☐

OR OTHER THAN
SMALL ENTITY

RATE	FEE
BASIC FEE	
X\$ 25=	
X100=	
+180=	
TOTAL	

RATE	FEE
BASIC FEE	
X\$50=	
X200=	
+360=	
TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	7/27/06	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR
Total	*	17	Minus ** 20 =
Independent	*	3	Minus *** 3 =
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

SMALL ENTITY

OR OTHER THAN
SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 25=	
X100=	
+180=	
TOTAL	

RATE	ADDITIONAL FEE
X\$50=	
X200=	
+360=	
TOTAL	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR
Total	*	Minus	** =
Independent	*	Minus	*** =
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X\$ 25=	
X100=	
+180=	
TOTAL	

RATE	ADDITIONAL FEE
X\$50=	
X200=	
+360=	
TOTAL	

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR
Total	*	Minus	** =
Independent	*	Minus	*** =
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

RATE	ADDITIONAL FEE
X\$ 25=	
X100=	
+180=	
TOTAL	

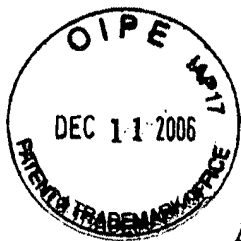
RATE	ADDITIONAL FEE
X\$50=	
X200=	
+360=	
TOTAL	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20"

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Lee; Sang-Yun
Appl. No.: 10/934,270
Title: VERTICAL MEMORY DEVICE STRUCTURES
Attorney Docket No.: BeSang.P001X1
Filed: September 3, 2004

Examiner: TRAN, MAI HUONG C

Mail Stop Assignment Recordation Services
Director of the US Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

SUBSTITUTE POWER OF ATTORNEY

Sir:

The undersigned owner and applicant of the above-identified patent application hereby revokes all prior powers of attorney, and appoints the practitioner, Greg L. Martinez, associated with Customer Number 51493, USPTO Reg. No. 53,276, located at 3116 South Mill Avenue, Suite 408 Tempe, Arizona 85282, Telephone No. (480)-785-6325 as his agent with full powers of attorney, to prosecute said patent application, and to transact all business in the United States Patent and Trademark Office in connection therewith.

Please address all communications relating to the present patent application to the attention of GREG L. MARTINEZ at the above address.

Dated: 12/5/2006

Sangyun Lee
Sang-Yun Lee, Applicant and Inventor

BeSang, Inc.
15188 NW Central Dr. Ste. #213
Portland, OR 97229
Phone) 503-533-5150
Fax) 503-533-5150

CERTIFICATE OF MAILING UNDER 37 CFR 1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope with sufficient postage addressed to: Mail Stop Assignment Recordation Services, Director of the US Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on the date shown below:

12/5/2006
Date

Sangyun Lee

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

Confirmation No.: 5732

Serial No.: 10/934,270

Examiner: Tran, Mai Huong

Filed: September 3, 2004

Docket No.: BeSang.P001X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUBSTITUTE POWER OF ATTORNEY

Sir:

Transmitted herewith is a substitute power of attorney for the above identified application. Please send all correspondence to the address below.

Respectfully submitted,

Dated: December 5, 2006

Greg L. Martinez
Agent for Applicant
Registration No. 53,276

3116 South Mill Avenue #408
Tempe, Az 85282
Phone: 480 785-6933

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 United States Patent and Trademark Office
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 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/934,270	09/03/2004	Sang-Yun Lee	BeSang.P001X1

Attention: GREG L. MARTINEZ
 Suite 408
 3116 South Mill Avenue
 Tempe, AZ 85282

CONFIRMATION NO. 5732



OC000000021710024

Date Mailed: 12/21/2006

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/11/2006.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

HN
 MY-HOA NGUYEN
 PTOSS (703) 305-0677 EXT 146

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
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 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/934,270	09/03/2004	Sang-Yun Lee	BeSang.P001X1

41536
 RAYMOND J. WERNER
 2056 NW ALOCLEK DRIVE, SUITE 314
 HILLSBORO, OR 97124

CONFIRMATION NO. 5732

OC000000021710012

Date Mailed: 12/21/2006

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/11/2006.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

JIN
 MY-HOA NGUYEN
 PTOSS (703) 305-0677 EXT 146

OFFICE COPY



Express Mail Mailing Label EQ037192272

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

Confirmation No.: 5732

Serial No.: 10/934,270

Examiner: Tran, Mai Huong C

Filed: September 3, 2004

Docket No.: BeSang.P001X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NON-COMPLIANT AMENDMENT

Sir:

In response to the Notice of Non-compliant Amendment mailed on August 9, 2006, please amend and reconsider the above-identified application as follows:

Amendments to the Claims begin on Page 2 of this paper.

12/27/2006 BABRAHA1 00000123 10934270

01 FC:2254

795.00 0P

AMENDMENTS TO THE CLAIMS

Please amend Claims 1-2, 4, 8, and 13-17 as shown below. A listing of the claims is provided below and will replace all prior versions and listings of the claims in the application.

Applicant points out that the claim numbering in the originally filed application inadvertently left out Claim 12. This change is reflected in the listing provided herein.

Listing of the Claims:

1. (amended) A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and

wherein the memory cell is a DRAM having at least one transistor.

2. (amended) The semiconductor memory structure of claim 1, wherein the vertically oriented memory cell comprises a vertical transistor and a serially connected capacitor in a SOI pillar.

3. (original) The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises a vertical transistor in an SOI pillar and a capacitor

connected in series therewith, the capacitor disposed external to the first stackable add-on layer.

4. (amended) The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises:

- a first capacitor,
- a first access transistor serially connected to the first capacitor,

- a second access transistor serial connected to the first access transistor, and

- a second capacitor serially connected to the second access transistor [device];

wherein the first capacitor, the first access transistor, the second access transistor, and the second capacitor are all formed in a single vertically oriented SOI pillar.

5. (original) The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically oriented, serially connected transistors formed on a SOI pillar, the serially connected transistors further connected to a capacitor disposed external to the stackable add-on layer.

6. (original) The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises two vertically and serially connected transistors and a shared serially connected capacitor in a SOI pillar.

7. (original) The semiconductor memory structure of claim 1, wherein the vertically oriented semiconductor memory cell comprises:

a first diode;
a first access transistor connected in series to the first diode;
a second access transistor connected in series to the first access transistor;
a third access transistor connected in series to the second access transistor; a fourth access transistor connected in series to the third access transistor; and
a second diode connected in series to the fourth access transistor;
wherein the first diode, the first, second, third, and fourth transistors, and the second diode are formed on the same SOI pillar.

8. (amended) A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate;
a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material; and
~~the stackable add-on layer to a layer of the substrate that is the greatest distance from the substrate;~~
wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and
wherein the memory cell is an SRAM having at least one Negative Differential Resistance device.

9. (original) The semiconductor memory structure of claim 8, wherein the vertically oriented semiconductor memory cell

comprises a vertically oriented transistor and a vertically oriented NDR-type Thyristor serially connected to each other.

10. (original) The semiconductor memory structure of claim 9, wherein the vertically oriented transistor is formed on an SOI pillar and the vertically NDR-type Thyristor is formed on an SOI pillar.

11. (original) The semiconductor memory structure of claim 9, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on two separated SOI pillars.

12. (original) The semiconductor memory structure of claim 8, wherein the vertically oriented transistor and the vertically NDR-type Thyristor are formed on the same SOI pillar.

13. (amended) A semiconductor memory structure, comprising:
a substrate having electrical devices formed therein, and further having ~~at least one~~ a dielectric layer ~~and at least one interconnect layer~~ disposed above the ~~substrate~~ electrical devices;

a [first] stackable add-on layer, ~~the first stackable add-on layer including~~ having a plurality of vertically oriented semiconductor memory cells ~~disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material~~; and

the stackable add-on layer being bonded to ~~a layer of the substrate that is the greatest distance from the substrate~~ the dielectric layer;

~~wherein the stackable add-on layer [is] being bonded to a layer of the substrate that is the greatest distance from the substrate~~; and

wherein the memory cells [is] are [a] nonvolatile memory cells having at least one transistor.

14. (original) The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

15. (original) The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

16. (amended) The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with [on] a first SOI pillar.

17. (amended) The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected [by] with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with [on] a second SOI pillar.

Remarks/Arguments

Entry of the foregoing amendments and reconsideration of this application is respectfully requested. By this amendment, Claims 1-2, 4, 8, 13-14 and 16-17 have been amended to more clearly set forth the present invention and to rectify certain informalities pointed out by the Examiner. These amendments do not introduce any new matter into the application and are not being made for reasons related to patentability. Applicant believes that Claims 1-17 are in condition for allowance and notice to that effect is respectfully requested.

Respectfully submitted,



Dated: Dec. 13, 2006

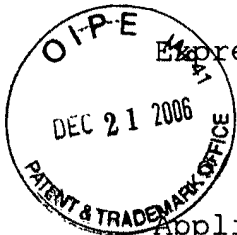
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

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Docket No.: BeSang.P001X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

NON-COMPLIANT AMENDMENT TRANSMITTAL

Sir:

Transmitted herewith is an amendment for this application along with a Petition for a four-month extension of time. Applicant is a small entity.

Enclosed is Check No. 1021 in the amount of \$795.00 for the four-month extension of time. A duplicate copy of this transmittal is attached.

Respectfully submitted,

Dated: Dec. 13, 2006

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PATENT APPLICATION FEE DETERMINATION RECORD						Application & Docket Number 10/934270			
Substitute for Form PTO-875									
CLAIMS AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA		RATE	FEE				
BASIC FEE (37 CFR 1.16(a))					\$	OR			
TOTAL CLAIMS (37 CFR 1.16(c))		minus 20 =		X \$	=	OR	X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(b))		minus 3 =		X \$	=	OR	X \$ =		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(d))				\$	=	OR	+ \$ =		
				TOTAL		OR	TOTAL		
* If the difference in column 1 is less than zero, enter "0" in column 2									
CLAIMS AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE	RATE	ADDITIONAL FEE
	Total (37 CFR 1.16(c))	17	Minus	20	=	X \$		X \$	
	Independent (37 CFR 1.16(b))	3	Minus	3	=	X \$		X \$	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(d))					\$		\$	
						TOTAL ADDITIONAL FEE		TOTAL ADDITIONAL FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. * If the "Highest Number Previously Paid For" in THIS SPACE is less than 20, enter "20". * If the "Highest Number Previously Paid For" in THIS SPACE is less than 3, enter "3". * The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.15. The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22304-1450. 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PLUS Search Results for S/N 10934270, Searched Wed Jan 31 14:36:04 EST 2007

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	6086	vertical with memory with cell	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:02
L2	2578	1 and stack\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:03
L3	1894	1 and stacked	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:03
L4	627	1 and bond\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:05
L5	60832	bond\$4 near pad	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:05
L6	416	4 and (not 5)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:07
L7	464223	(second 2nd) with (substrate wafer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:08
L8	277	6 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:11
L9	1529	2 and 7	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:08

EAST Search History

L10	1156146	bonded bonding	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:31
L11	219	8 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:16
L12	215	vertical near memory near cell	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:17
L13	9	11 and 12	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:17
L14	226750	10 same (substrate wafer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 11:32
L15	590	(438/152,153).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 11:33
L16	209	(257/118,199).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 11:33
L17	799	15 16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 11:33
L18	21	1 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 11:39
L19	5	"6849871"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 11:44

EAST Search History

L20	0	11/934270	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 11:44
L21	1	10/934270	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 11:49
L22	9022	substrate with electrical with device	US-PGPUB	OR	ON	2007/03/15 11:53
L23	4	stackable with add-on with (layer film)	US-PGPUB	OR	ON	2007/03/15 11:52
L24	2177	22.clm.	US-PGPUB	OR	ON	2007/03/15 11:53
L25	3	23.clm.	US-PGPUB	OR	ON	2007/03/15 11:53
L26	2	24 and 25	US-PGPUB	OR	ON	2007/03/15 11:53

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	10717	(257/295,296,314,315,316).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/03/15 20:55
L2	2575652	substrate wafer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 20:55
L3	1564923	(active passive electrical electronic) with (device component)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 20:57
L4	416962	2 and 3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 20:57
L5	165280	DRAM SRAM	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 20:58
L6	2053476	(non adj volatile nonvolatile) memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 20:59
L7	153046	(non adj volatile nonvolatile) near memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 20:59
L8	73156	dynamic adj random adj access adj memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:00
L9	40792	static with random with access with memory	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:01

EAST Search History

L10	93473	8 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:01
L11	28532	4 and 5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:01
L12	17397	4 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:02
L13	0	stack\$4 same add adj on with (layer wafer substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:03
L14	22	stack\$4 same add-on with (layer wafer substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:06
L15	50	stack\$4 same add-on same (layer wafer substrate)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:07
L16	464223	(second 2nd) with (substrate wafer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:08
L17	1729	1 and 11	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:09
L18	2428	1 and 10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:09
L19	1190	16 and 17	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:09

EAST Search History

L20	1574	16 and 18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:09
L21	1646664	bond\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:10
L22	210	19 and 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:10
L23	225	20 and 21	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:11
L24	549297	vertical with (Oriented direction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:12
L25	73	22 and 24	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:14
L26	65	23 and 24	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/03/15 21:12



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NOTICE OF ALLOWANCE AND FEE(S) DUE

7590

03/21/2007

Attention: GREG L. MARTINEZ
Suite 408
3116 South Mill Avenue
Tempe, AZ 85282

EXAMINER

NGUYEN, THINH T

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 03/21/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1	5732
TITLE OF INVENTION: VERTICAL MEMORY DEVICE STRUCTURES				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$0	\$1000	06/21/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
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P.O. Box 1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590

03/21/2007

Attention: GREG L. MARTINEZ
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 3116 South Mill Avenue
 Tempe, AZ 85282

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1	5732

TITLE OF INVENTION: VERTICAL MEMORY DEVICE STRUCTURES

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$0	\$1000	06/21/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, THINH T	2818	257-296000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

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- ☐ Publication Fee (No small entity discount permitted)
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- ☐ A check is enclosed.
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- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1	5732
7590	03/21/2007		EXAMINER	
Attention: GREG L. MARTINEZ Suite 408 3116 South Mill Avenue Tempe, AZ 85282			NGUYEN, THINH T	
			ART UNIT	PAPER NUMBER
			2818	
DATE MAILED: 03/21/2007				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability

Application No.

10/934,270

Examiner

Thinh T. Nguyen

Applicant(s)

LEE, SANG-YUN

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 12/21/2006.
2. ☒ The allowed claim(s) is/are 1-17.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some* c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
- (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
- 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
- (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Notice of Informal Patent Application |
| 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. |
| 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 7. ☐ Examiner's Amendment/Comment |
| 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 8. ☒ Examiner's Statement of Reasons for Allowance |
| | 9. ☐ Other _____. |

DETAILED ACTION

1. Claims 1-17 are pending in the Application

Reason for allowance

2. Claims 1-17 are allowed.

The following is an examiner's statement of reason for allowance:

A/ I/ Group I: Claims 1-7:

None of the references of record teaches or suggests the claimed SEMICONDUCTOR STRUCTURE having the limitations:

' a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate and

wherein the memory cell is a DRAM having at least one transistor. "--

In combination with all other limitations as recited in claim 1.

II/ Group II: Claims 8-12:

None of the references of record teaches or suggests the claimed SEMICONDUCTOR STRUCTURE having the limitations:

‘ a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate ; and

wherein the memory cell is an SRAM having at least one Negative Differential Resistance device. “--

In combination with all other limitations as recited in claim 8.

III/ Group III: Claims 13-17:

None of the references of record teaches or suggests the claimed SEMICONDUCTOR STRUCTURE having the limitations:

‘ a first stackable add-on layer, the first stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

the stackable add-on layer being bonded to the dielectric layer wherein the memory cells are nonvolatile memory cells having at least one transistor. . “--

In combination with all other limitations as recited in claim 13.

Art Unit: 2818

B/ Applicant filing of the terminal disclaimer has overcome the double patenting rejection of claim 1-17.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached at 571-272-1907.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2818

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system.

Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T Nguyen



Art unit 2818

Andy Hays
Andy Hays
Primary Examiner

Issue Classification 	Application/Control No. 10/934,270	Applicant(s)/Patent under Reexamination LEE, SANG-YUN
	Examiner Thinh T. Nguyen	Art Unit 2818

ISSUE CLASSIFICATION													
ORIGINAL					INTERNATIONAL CLASSIFICATION								
CLASS		SUBCLASS			CLAIMED				NON-CLAIMED				
257		296			H	01	L	27	/108				/
CROSS REFERENCES									/				/
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)								/				/
257	296	295	315						/				/
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Thinh T. Nguyen 3/2007 (Assistant Examiner) (Date)	Andy H. Hupel 03/07 (Primary Examiner) (Date)	Total Claims Allowed: 17
G. Stanley 3-20-07 (Legal Instruments Examiner) (Date)	O.G. Print Claim(s)	O.G. Print Fig. fig 1

☒ Claims renumbered in the same order as presented by applicant												☐ CPA		☒ T.D.		☐ R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		31		61		91		121		151		181				
2	2		32		62		92		122		152		182				
3	3		33		63		93		123		153		183				
4	4		34		64		94		124		154		184				
5	5		35		65		95		125		155		185				
6	6		36		66		96		126		156		186				
7	7		37		67		97		127		157		187				
8	8		38		68		98		128		158		188				
9	9		39		69		99		129		159		189				
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11	11		41		71		101		131		161		191				
12	12		42		72		102		132		162		192				
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	25		55		85		115		145		175		205				
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	27		57		87		117		147		177		207				
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	30		60		90		120		150		180		210				



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov



Bib Data Sheet

CONFIRMATION NO. 5732

SERIAL NUMBER 10/934,270	FILING DATE 09/03/2004 RULE	CLASS 257	GROUP ART UNIT 2818	ATTORNEY DOCKET NO. BeSang.P001X1
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APPLICANTS

Sang-Yun Lee, Beaverton, OR;

** CONTINUING DATA ***** *yes*

This application is a CIP of 10/873,969 06/21/2004

** FOREIGN APPLICATIONS ***** *none*

IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** SMALL ENTITY **

** 10/29/2004

Foreign Priority claimed ☐ yes ☒ no	STATE OR COUNTRY OR	SHEETS DRAWING 34	TOTAL CLAIMS 17	INDEPENDENT CLAIMS 3
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35 USC 119 (a-d) conditions met
☐ yes ☒ no ☐ Met after
 Allowance

Verified and Acknowledged
 Examiner's Signature: *[Signature]* Initials: *[Initials]*

ADDRESS
 000041536
 RAYMOND J. WERNER
 2056 NW ALOCLEK DRIVE, SUITE 314
 HILLSBORO , OR
 97124

TITLE
 Vertical memory device structures

FILING FEE RECEIVED 385	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____
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Index of Claims



Application/Control No.

10/934,270

Examiner

Thinh T. Nguyen

Applicant(s)/Patent under Reexamination

LEE, SANG-YUN

Art Unit

2818

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date											
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Search Notes 	Application/Control No.		Applicant(s)/Patent under Reexamination	
	10/934,270		LEE, SANG-YUN	
	Examiner		Art Unit	
	Mai-Huong Tran		2818	

SEARCHED			
Class	Subclass	Date	Examiner
438	152, 153	2/11/2006	MT
257	118, 199		
257	314, 315	3/14/07	TTN
257	298, 299	3/14/07	TTN

INTERFERENCE SEARCHED			
Class	Subclass	Date	Examiner
EAST	PUB	3/15/07	TTN

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	DATE	EXMR
EAST	2/11/2006	MT
EAST	3/15/07	TTN



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1	5732

EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
07/18/2007	PAPER

7590 07/18/2007
Attention: GREG L. MARTINEZ
Suite 408
3116 South Mill Avenue
Tempe, AZ 85282

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Abandonment	Application No.	Applicant(s)	
	10/934,270	Sang-Yum Lee	
	Examiner	Art Unit	
	NGUYEN, THINH T	2818	

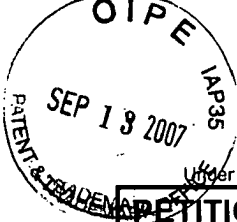
-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

This application is abandoned in view of:

1. ☐ Applicant's failure to timely file a proper reply to the Office letter mailed on _____.
 - (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
 - (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CFR 1.113 (a) to the final rejection.
(A proper reply under 37 CFR 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
 - (c) ☐ A reply was received on _____ but it does not constitute a proper reply, or a bona fide attempt at a proper reply, to the non-final rejection. See 37 CFR 1.85(a) and 1.111. (See explanation in box 7 below).
 - (d) ☐ No reply has been received.
2. ☒ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
 - (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance (PTOL-85).
 - (b) ☐ The submitted fee of \$_____ is insufficient. A balance of \$_____ is due.
The issue fee required by 37 CFR 1.18 is \$_____. The publication fee, if required by 37 CFR 1.18(d), is \$_____.
 - (c) ☒ The issue fee and publication fee, if applicable, has not been received.
3. ☐ Applicant's failure to timely file corrected drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
 - (a) ☐ Proposed corrected drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
 - (b) ☐ No corrected drawings have been received.
4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.
5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.
6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.
7. ☐ The reason(s) below:

/AG/

Petitions to revive under 37 CFR 1.137(a) or (b), or requests to withdraw the holding of abandonment under 37 CFR 1.181, should be promptly filed to minimize any negative effects on patent term.



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT
ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)**Docket Number (Optional)
BESANG.P001X1

First named inventor: Sang-Yun Lee

Application No.: 10/934,270

Art Unit: 2818

Filed: 09/03/2004

Examiner: Nguyen, Thinh T.

Title: VERTICAL MEMORY DEVICE STRUCTURES

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX (571) 273-8300NOTE: If information or assistance is needed in completing this form, please contact Petitions
Information at (571) 272-3282.The above-identified application became abandoned for failure to file a timely and proper reply to a notice or
action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration
date of the period set for reply in the office notice or action plus an extensions of time actually obtained.**APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION**

NOTE: A grantable petition requires the following items:

- (1) Petition fee;
- (2) Reply and/or issue fee;
- (3) Terminal disclaimer with disclaimer fee - required for all utility and plant applications
filed before June 8, 1995; and for all design applications; and
- (4) Statement that the entire delay was unintentional.

1. Petition fee☒ Small entity-fee \$ 750.00 (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.☐ Other than small entity - fee \$ _____ (37 CFR 1.17(m)) **The PTO did not receive the following
listed item(s) CK. 1750.00 we
received ck. 1150.00****2. Reply and/or fee**A. The reply and/or fee to the above-noted Office action in
the form of _____ (identify type of reply):

- ☐ has been filed previously on 09/14/2007 NNGUYEN2 00000101 10934270
☐ is enclosed herewith.

02 FC:2453

750.00 OP

B. The issue fee and publication fee (if applicable) of \$ 1,000.00.

- ☐ has been paid previously on _____
☒ is enclosed herewith.

[Page 1 of 2]

This collection of information is required by 37 CFR 1.137(b). The information is required to obtain or retain a benefit by the public which is to file (and by the
USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1.0 hour to
complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any
comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer,
U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED
FORMS TO THIS ADDRESS. **SEND TO: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

3. Terminal disclaimer with disclaimer fee

☒ Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.☐ A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of \$ _____ for a small entity or \$ _____ for other than a small entity) disclaiming the required period of time is enclosed herewith (see PTO/SB/63).

4. STATEMENT: The entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE: The United States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D)).]

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

_____ Signature	August 24, 2007 Date
_____ Greg L. Martinez Typed or printed name	53,276 Registration Number, if applicable
_____ Address	_____ Telephone Number
_____ Address	

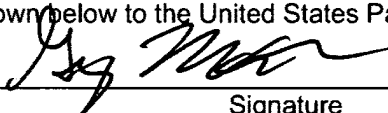
Enclosures: ☒ Fee Payment☐ Reply☐ Terminal Disclaimer Form☐ Additional sheets containing statements establishing unintentional delay☐ Other: _____**CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]**

I hereby certify that this correspondence is being:

☒ Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.☐ Transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (571) 273-8300.

August 24, 2007

Date



Signature

Greg L. Martinez

Typed or printed name of person signing certificate

Privacy Act Statement

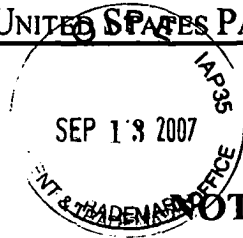
The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES PATENT AND TRADEMARK OFFICE



UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590

03/21/2007

Attention: GREG L. MARTINEZ
Suite 408
3116 South Mill Avenue
Tempe, AZ 85282

EXAMINER

NGUYEN, THINH T

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 03/21/2007

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1	5732
TITLE OF INVENTION: VERTICAL MEMORY DEVICE STRUCTURES				

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$700	\$300	\$0	\$1000	06/21/2007

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

09/14/2007 NHGUYEN2 00000101 10934270

I. Review the SMALL ENTITY status shown above.

01 FC:2501

700.00 0P

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

If the SMALL ENTITY is shown as NO:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

A. Pay TOTAL FEE(S) DUE shown above, or

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

DATE 10/1/2007

APPLICATION NUMBER 10/934,270

DOC CODE PETDEC

DOC DATE 10/11/07

DELIVER THE ATTACHED FILE/DOCUMENT TO THE TC
SCANNING CENTER

CONTRACTOR: THE ATTACHED FILE/DOCUMENT MUST BE
INDEXED AND SCANNED INTO IFW WITHIN 8 WORK HOURS;
UPLOADING OF THE SCANNED IMAGES SHOULD OCCUR NO
LATER THAN 16 WORK HOURS
FOLLOWING RECEIPT OF THIS REQUEST

AFTER SCANNING, ORIGINAL DOCUMENTS SHOULD BE BOXED IN
ACCORDANCE WITH INSTRUCTIONS



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Attention: GREG L. MARTINEZ
Suite 408
3116 South Mill Avenue
Tempe AZ 85282

COPY MAILED

OCT 11 2007

OFFICE OF PETITIONS

In re Application of	:	
Sang-Yun LEE	:	
Application No. 10/934,270	:	DECISION ON PETITION
Filed: September 3, 2004	:	
Attorney Docket No. BESANG.P001X1	:	

This is a decision on the petition under 37 CFR 1.137(b), filed September 13, 2007, to revive the above-identified application.

The petition is **DISMISSED**.

Any request for reconsideration of this decision must be submitted within TWO (2) MONTHS from the mail date of this decision. Extensions of time under 37 CFR 1.136(a) are permitted. The reconsideration request should include a cover letter entitled "Renewed Petition under 37 CFR 1.137(b)." This is **not** a final agency action within the meaning of 5 U.S.C. § 704.

The above-identified application became abandoned for failure to reply to the Notice of Allowance and Fee(s) Due ("Notice"), mailed March 21, 2007, which set a shortened statutory period for reply of three (3) months. Accordingly, the above-identified application became abandoned on June 22, 2007.

A grantable petition under 37 CFR 1.137(b) must be accompanied by: (1) the required reply, unless previously filed; (2) the petition fee as set forth in 37 CFR 1.17(m); (3) a statement that the entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition pursuant to 37 CFR 1.137(b) was unintentional; and (4) any terminal disclaimer (and fee as set forth in 37 CFR 1.20(d)) required by 37 CFR 1.137(d). Where there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137 was unintentional, the Commissioner may require additional information. See MPEP 711.03(c)(III)(C) and (D). The instant petition lacks item(s) (1) and (3). The petitioner has not submitted the required publication fee of \$300 set forth in 37 CFR 1.18(d).

The statement of delay is not acceptable. In this regard, petitioner's attention is directed to 37 CFR 1.33(b), which states:

(b) Amendments and other papers. Amendments and other papers, except for written assertions pursuant to § 1.27(c)(2)(ii) of this part, filed in the application must be signed by:

- (1) A registered patent attorney or patent agent of record appointed in compliance with § 1.32(b);
- (2) A registered patent attorney or patent agent not of record who acts in a representative capacity under the provisions of § 1.34;
- (3) An assignee as provided for under § 3.71(b) of this chapter; or
- (4) All of the applicants (§ 1.41(b)) for patent, unless there is an assignee of the entire interest and such assignee has taken action in the application in accordance with § 3.71 of this chapter.

An unsigned amendment (or other paper) or one not properly signed by a person having authority to prosecute the application is not entered. In this instance, Greg L. Martinez did not sign the petition.

Further correspondence with respect to this matter should be addressed as follows:

By Mail: Mail Stop PETITION
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

By hand: U. S. Patent and Trademark Office
Customer Service Window, Mail Stop Petitions
Randolph Building
401 Dulany Street
Alexandria, VA 22314

The centralized facsimile number is (571) 273-8300.

Telephone inquiries concerning this decision should be directed to Brian Sines at (571) 272-6051 or in his absence, the undersigned at (571) 272-7099.



David Bucci
Petitions Examiner
Office of Petitions

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Sang-Yun Lee

Appl. No.: 10/934,270

Examiner: Nguyen, Thinh T

Title: VERTICAL MEMORY DEVICE STRUCTURES

Attorney Docket No.: BESANG.P001X1

Filed: September 3, 2004

Director of the US Patent and Trademark Office

P.O. Box 1450

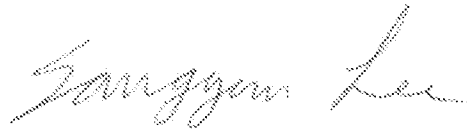
Alexandria, VA 22313-1450

SUBSTITUTE POWER OF ATTORNEY

Sir:

The undersigned owner and applicant of the above-identified patent application hereby revokes all prior powers of attorney, and appoint all Attorneys/Agents associated with Customer No. 23123, as his Attorney/Agent with full powers of attorney, to prosecute said patent application, and to transact all business in the United States Patent and Trademark Office in connection therewith.

Please address all communications relating to the present patent application to the attention of Albert L. Schmeiser at the below address.



Dated: October, 12, 2007

Sang-Yun Lee

Schmeiser, Olsen & Watts LLP

18 E. University Dr., Ste. 101

Mesa, AZ 85201-5946

Tel.: 480.655.0073

Fax: 480.655.9536

Electronic Patent Application Fee Transmittal

Application Number:	10934270			
Filing Date:	03-Sep-2004			
Title of Invention:	VERTICAL MEMORY DEVICE STRUCTURES			
First Named Inventor/Applicant Name:	Sang-Yun Lee			
Filer:	Greg L. Martinez/Joyce Brown			
Attorney Docket Number:	BESANG.P001X1			
Filed as Small Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Publ. Fee- early, voluntary, or normal	1504	1	300	300
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				300

Electronic Acknowledgement Receipt

EFS ID:	2343017
Application Number:	10934270
International Application Number:	
Confirmation Number:	5732
Title of Invention:	VERTICAL MEMORY DEVICE STRUCTURES
First Named Inventor/Applicant Name:	Sang-Yun Lee
Correspondence Address:	Attention: GREG L. MARTINEZ - Suite 408 3116 South Mill Avenue Tempe AZ 85282 US 4807856325 -
Filer:	Greg L. Martinez/Joyce Brown
Filer Authorized By:	Greg L. Martinez
Attorney Docket Number:	BESANG.P001X1
Receipt Date:	19-OCT-2007
Filing Date:	03-SEP-2004
Time Stamp:	12:30:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 300
RAM confirmation Number	7905

Deposit Account	190513
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 and 1.17	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	VERTICAL_MEMORY_DEVICE_STRUCTURES_Reasons_for_Allowance.pdf	14505 3e3d2781d7e4129bab0548d9bef04e93fd891aa	no	1

Warnings:

Information:

2	Power of Attorney	VERTICAL_MEMORY_DEVICE_STRUCTURES_POA.pdf	29296 29bfad14bc9fd1134db396bfb70d89b119ac1883	no	1
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Warnings:

Information:

3	Fee Worksheet (PTO-06)	fee-info.pdf	8156 78867468de3b8403a656b6bf9501017049dc6efb	no	2
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Warnings:

Information:

Total Files Size (in bytes):			51957
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Sang-Yun Lee

Appl. No.: 10/934,270

Examiner: Nguyen, Thinh T

Title: VERTICAL MEMORY DEVICE STRUCTURES

Attorney Docket No.: BESANG.P001X1

Filed: September 3, 2004

Director of the US Patent and Trademark Office

P.O. Box 1450

Alexandria, VA 22313-1450

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Sir:

Applicant agrees that Examiner has accurately stated one reason for allowance of the claims. However, the claims include other patentable aspects that were not identified by Examiner. This response is submitted to avoid the possibility of any unnecessary limitation on the scope of the claims which might result from the stated reason for allowance. It is being submitted concurrently with the rest of the issue fee payment (\$300.00), which was unintentionally not submitted earlier.

Dated: October 12, 2007

By: /Greg L. Martinez/
Greg L. Martinez
Agent for Applicant
Reg. No. 53,276

Schmeiser, Olsen & Watts LLP
18 E. University Dr., Ste. 101
Mesa, AZ 85201-5946
Tel.: 480.655.0073
Fax: 480.655.9536

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Sang-Yun Lee

Appl. No.: 10/934,270

Examiner: Nguyen, Thinh T

Title: VERTICAL MEMORY DEVICE STRUCTURES

Attorney Docket No.: BESANG.P001X1

Filed: September 3, 2004

Director of the US Patent and Trademark Office

P.O. Box 1450

Alexandria, VA 22313-1450

RENEWED PETITION UNDER 37 CFR 1.137(B)

Sir:

Applicant respectfully requests reconsideration of his petition filed September 13, 2007. Applicant unintentionally did not submit the required publication fee of \$300 and failed to sign the Petition. Applicant hereby submits the \$300.00 publication fee and the signed petition. Applicant believes that the Petition is now grantable under 37 CFR 1.137(b).

Dated: October 22, 2007

By: /Greg L. Martinez/
Greg L. Martinez
Agent for Applicant
Reg. No. 53,276

Schmeiser, Olsen & Watts LLP
18 E. University Dr., Ste. 101
Mesa, AZ 85201-5946
Tel.: 480.655.0073
Fax: 480.655.9536



**PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT
ABANDONED UNINTENTIONALLY UNDER 37 CFR 1.137(b)**

Docket Number (Optional)
BESANG.P001X1

First named inventor: Sang-Yun Lee

Application No.: 10/934,270

Art Unit: 2818

Filed: 09/03/2004

Examiner: Nguyen, Thinh T.

Title: VERTICAL MEMORY DEVICE STRUCTURES

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX (571) 273-8300

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (571) 272-3282.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the office notice or action plus an extensions of time actually obtained.

APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION

NOTE: A grantable petition requires the following items:

- (1) Petition fee;
- (2) Reply and/or issue fee;
- (3) Terminal disclaimer with disclaimer fee - required for all utility and plant applications filed before June 8, 1995; and for all design applications; and
- (4) Statement that the entire delay was unintentional.

1. Petition fee

☒ Small entity-fee \$ 750.00 (37 CFR 1.17(m)). Applicant claims small entity status. See 37 CFR 1.27.

☐ Other than small entity - fee \$ _____ (37 CFR 1.17(m)) The PTO did not receive the following listed item(s) EX-1750-00 WR
received ex. 1450-00

2. Reply and/or fee

A. The reply and/or fee to the above-noted Office action in the form of _____ (identify type of reply):

☐ has been filed previously on 09/14/2007 NNGUYN2 00000101 10934270
☐ is enclosed herewith.

02 FC:2453

750.00 OP

B. The issue fee and publication fee (if applicable) of \$ 1,000.00

☐ has been paid previously on _____
☒ is enclosed herewith.

[Page 1 of 2]

This collection of information is required by 37 CFR 1.137(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

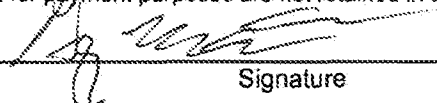
3. Terminal disclaimer with disclaimer fee

- ☒ Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.
- ☐ A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of \$ _____ for a small entity or \$ _____ for other than a small entity) disclaiming the required period of time is enclosed herewith (see PTO/SB/63).

4. STATEMENT: The entire delay in filing the required reply from the due date for the required reply until the filing of a grantable petition under 37 CFR 1.137(b) was unintentional. [NOTE: The United States Patent and Trademark Office may require additional information if there is a question as to whether either the abandonment or the delay in filing a petition under 37 CFR 1.137(b) was unintentional (MPEP 711.03(c), subsections (III)(C) and (D)).]

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.



 Signature

August 24, 2007

Date

Greg L. Martinez

Typed or printed name

53,276

Registration Number, if applicable

Address

Telephone Number

Address

Enclosures: ☒ Fee Payment☐ Reply☐ Terminal Disclaimer Form☐ Additional sheets containing statements establishing unintentional delay☐ Other: _____**CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]**

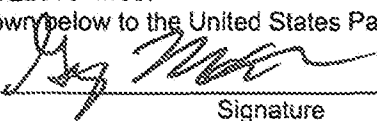
I hereby certify that this correspondence is being:

☒ Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

☐ Transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (571) 273-8300.

August 24, 2007

Date



 Signature

Greg L. Martinez

Typed or printed name of person signing certificate

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	2352883
Application Number:	10934270
International Application Number:	
Confirmation Number:	5732
Title of Invention:	VERTICAL MEMORY DEVICE STRUCTURES
First Named Inventor/Applicant Name:	Sang-Yun Lee
Correspondence Address:	Attention: GREG L. MARTINEZ - Suite 408 3116 South Mill Avenue Tempe AZ 85282 US 4807856325 -
Filer:	Greg L. Martinez/Joyce Brown
Filer Authorized By:	Greg L. Martinez
Attorney Docket Number:	BESANG.P001X1
Receipt Date:	22-OCT-2007
Filing Date:	03-SEP-2004
Time Stamp:	17:52:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	VERTICAL_MEMORY_DEVICE_STRUCTURES_Petition_Request_for_Reconsideration.pdf	14735	no	1
			6804e43df33738736c6d6130019749f4239abc85		
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	VERTICAL_MEMORY_DEVICE_STRUCTURES_Petition_Revive_Signed.pdf	2516808	no	3
			7a0b38b78ddc51b2049e7d13e76e128476ab6392		
Warnings:					
Information:					
Total Files Size (in bytes):			2531543		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1

CONFIRMATION NO. 5732

POA ACCEPTANCE LETTER



Albert L. Schmeiser
Schmeiser, Olsen & Watts LLP
Suite 101
18 E. University Dr.
Mesa, AZ 85201-5946

Date Mailed: 10/29/2007

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/19/2007.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/atesfai/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1

CONFIRMATION NO. 5732

POWER OF ATTORNEY NOTICE



OC000000026443564

Attention: GREG L. MARTINEZ
Suite 408
3116 South Mill Avenue
Tempe, AZ 85282

Date Mailed: 10/29/2007

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/19/2007.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/atesfai/

Office of Initial Patent Examination (571) 272-4000 or 1-800-PTO-9199



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Albert L. Schmeiser
Schmeiser, Olsen & Watts LLP
18 E. University Drive, Suite 101
Mesa, AZ 85201-5946

COPY MAILED

APR 03 2008

OFFICE OF PETITIONS

In re Application of :
Sang-Yun Lee :
Application No. 10/934,270 : DECISION ON PETITION
Filed: September 03, 2004 :
Attorney Docket No. BESANG.P001X1 :

This is a decision on a renewed petition under the unintentional provisions of 37 CFR 1.137(b), filed 22 October 2007, to revive the above-identified application.

The petition is **GRANTED**.

This application became abandoned for failure to timely pay the issue and publication fees on or before 21 June 2007, as required by the Notice of Allowance and Fee(s) Due, mailed 21 March 2007. Accordingly, the date of abandonment of this application is 22 June 2007.

The petition satisfies the requirements of 37 CFR 1.137(b) in that petitioner has supplied (1) the reply in the form of payment of the issue fee of \$700.00 and the publication fee of \$300.00, (2) the petition fee of \$750.00; and (3) a proper statement of unintentional delay.

Telephone inquiries concerning this decision should be directed to Allen C. Ho at (571) 272-6052.

This application is being referred to Publishing Division for processing into a patent.

for David Bucci
Petitions Examiner
Office of Petitions

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590

03/21/2007

Attention: GREG L. MARTINEZ

~~Suite 408~~ Schmeiser, Olsen & Watts LLP
~~3116 South Mill Avenue~~ 18 E. University Drive, Ste.101
~~Tempe, AZ 85282~~ Mesa, AZ 85201

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Joyce D. Brown	(Depositor's name)
<i>Joyce D. Brown</i>	(Signature)
April 9, 2008	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	09/03/2004	Sang-Yun Lee	BESANG.P001X1	5732
TITLE OF INVENTION: VERTICAL MEMORY DEVICE STRUCTURES			BESA-11983	

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	~~\$700~~ \$720	\$300	\$0	~~\$X000~~ \$1020	06/21/2007
EXAMINER		ART UNIT	CLASS-SUBCLASS			
NGUYEN, THINH T		2818	257-296000			

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1. Schmeiser, Olsen & Watts LLP
 2. *(Signature)*
 00 00 000

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-0513 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Greg L. Martinez/

Date April 9, 2008

Typed or printed name Greg L. Martinez

Registration No. 53,276

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Bib Data Sheet

CONFIRMATION NO. 5732

SERIAL NUMBER 10/934,270	FILING OR 371(c) DATE 09/03/2004 RULE	CLASS 257	GROUP ART UNIT 2818	ATTORNEY DOCKET NO. BESANG.P001X1
APPLICANTS Sang-Yun Lee, Beaverton, OR;				
** CONTINUING DATA ***** This application is a CIP of 10/873,969 06/21/2004 PAT 7,052,941 ** FOREIGN APPLICATIONS *****				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED** SMALL ENTITY ** ** 10/29/2004				
Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions met ☐ yes ☐ no ☐ Met after Allowance Verified and Acknowledged _____ Examiner's Signature _____ Initials _____	STATE OR COUNTRY OR	SHEETS DRAWING 34	TOTAL CLAIMS 17	INDEPENDENT CLAIMS 3
ADDRESS GREG L. MARTINEZ Schmeiser, Olsen & Watts LLP 18 E. University Dr. Suite 101 Mesa, AZ85201				
TITLE VERTICAL MEMORY DEVICE STRUCTURES				
FILING FEE RECEIVED 685	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit	



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/934,270	05/27/2008	7378702	BESANG.P001X1	5732

7590 05/07/2008

GREG L. MARTINEZ
Schmeiser, Olsen & Watts LLP
18 E. University Dr.
Suite 101
Mesa, AZ 85201

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Sang-Yun Lee, Beaverton, OR;

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sang-Yun Lee

Confirmation No.: 5732

Serial No.: 10/934,270

Filed: 09/03/2004

Patent No.: 7,378,702 B2

Issued: 05/27/2008

Examiner: Andy Huynh

Docket No.: BESANG.P001X1

Title: VERTICAL MEMORY DEVICE STRUCTURES

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

REQUEST TO UPDATE ATTORNEY DOCKET NUMBER

Sir:

Applicant respectfully requests that the attorney docket number be changed in the above matter from BESANG.P001X1 to:

BESA.11983

It was not possible to make this change on PAIR.

Respectfully submitted,

Dated: September 9, 2010

/Greg L. Martinez/

Agent for Applicant
Reg. No. 53,276

Customer No. 23123
SCHMEISER, OLSEN & WATTS LLP
18 East University Drive, #101
Mesa, AZ 85201
(480) 655-0073

Electronic Acknowledgement Receipt

EFS ID:	8382451
Application Number:	10934270
International Application Number:	
Confirmation Number:	5732
Title of Invention:	VERTICAL MEMORY DEVICE STRUCTURES
First Named Inventor/Applicant Name:	Sang-Yun Lee
Correspondence Address:	GREG L. MARTINEZ Schmeiser, Olsen & Watts LLP 18 E. University Dr. Suite 101 Mesa AZ 85201 US 4806550073 -
Filer:	Greg L. Martinez/Joyce Brown
Filer Authorized By:	Greg L. Martinez
Attorney Docket Number:	BESANG.P001X1
Receipt Date:	09-SEP-2010
Filing Date:	03-SEP-2004
Time Stamp:	13:16:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	VERTICAL_MEMORY_DEVICE_STRUCTURES_Request_Update_Dkt_Number11983.pdf	14371 7055b55a115c382b1487c8ba948d675e51d8f59f	no	1

Warnings:

Information:

Total Files Size (in bytes):	14371
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Application Number	10/534,220
	Filing Date	September 3, 2004
	First Named Inventor	Sang-Yun Lee
	Title	Vertical Memory Device Structures
	Art Unit	2618
	Examiner Name	Nguyen, Thinh T
	Attorney Docket Number	BESA.11983

I hereby revoke all previous powers of attorney given in the above-identified application.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

102591

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified application to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the:

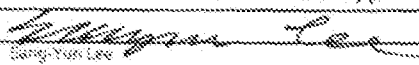
☐ Applicant/inventor.

OR

☒ Assignee of record of the entire interest. See 37 CFR 3.71.

Statement under 37 CFR 3.73(b) (Form PTO/SB/96) submitted herewith or filed on _____

SIGNATURE of Applicant or Assignee of Record

Signature		Date	Mar 18 2012
Name	Sang-Yun Lee	Telephone	+1 (503) 601-2025
Title and Company	CEO of Bering, Inc.		

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.21, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1480, Alexandria, VA 22313-1480. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1480, Alexandria, VA 22313-1480.

If you need assistance in completing the form, call 1-800-PTO-5199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Sang-Yun Lee

Application No./Patent No.: 10/934,270

Filed/Issue Date: September 3, 2004

Titled: VERTICAL MEMORY DEVICE STRUCTURES

BaSang, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 325696, Frame 0106, or for which a copy therefore is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

(NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08)

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Sang-Yun Lee
Signature

March 19, 2012

Date

Sang-Yun Lee

CEO

Printed or Typed Name

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	12492415
Application Number:	10934270
International Application Number:	
Confirmation Number:	5732
Title of Invention:	VERTICAL MEMORY DEVICE STRUCTURES
First Named Inventor/Applicant Name:	Sang-Yun Lee
Correspondence Address:	GREG L. MARTINEZ Schmeiser, Olsen & Watts LLP 18 E. University Dr. Suite 101 Mesa AZ 85201 US 4806550073 -
Filer:	Greg L. Martinez
Filer Authorized By:	
Attorney Docket Number:	BESA.11983
Receipt Date:	07-APR-2012
Filing Date:	03-SEP-2004
Time Stamp:	00:49:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	sb0081_fill_BESA_11983_Signeda.pdf	225711 8d8c6a894c7ac1142026aec2fa98584c66d5b78a	no	1
Warnings:					
Information:					
2	Power of Attorney	sb0096_11983_Signeda.pdf	205055 339a5466227baac15bb4f55ba1c26e31d3a88dab	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			430766		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/934,270	09/03/2004	Sang-Yun Lee	BESA.11983

102591
GREG L. MARTINEZ
3116 SOUTH MILL AVENUE #408
TEMPE, AZ 85282

CONFIRMATION NO. 5732
POA ACCEPTANCE LETTER



Date Mailed: 04/16/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/07/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/zabraha/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/934,270	09/03/2004	Sang-Yun Lee	BESA.11983

GREG L. MARTINEZ
Schmeiser, Olsen & Watts LLP
18 E. University Dr.
Suite 101
Mesa, AZ 85201

CONFIRMATION NO. 5732
POWER OF ATTORNEY NOTICE



OC000000053701293

Date Mailed: 04/16/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 04/07/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/zabaha/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101