

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner

v.

BESANG INC.,

Patent Owner

Case IPR2023-00991

U.S. Patent No. 7,378,702

DECLARATION OF DR. CARL SECHEN

IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW

OF U.S. PATENT NO. 7,378,702

Intel v. BeSang IPR2023-00991 Exhibit 1003
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I, **Dr. Carl Sechen**, declare as follows:

I. INTRODUCTION AND COMPENSATION

1. I have been retained by Intel Corporation as an independent expert consultant in this *inter partes* review (“IPR”) proceeding before the United States Patent and Trademark Office (“PTO”).

2. I have been asked by Counsel for Petitioner (“Counsel”) to consider whether certain references teach or suggest the features recited in claims 1 and 13–17 of U.S. Patent No. 7,378,702 (the “’702 Patent”) (Exhibit 1001). My opinions, and the bases for those opinions, are set forth below.

3. I am being paid at my ordinary and customary consulting rate of \$425 per hour. My compensation in no way depends on the outcome of this matter. I have no other financial interest in this proceeding.

II. QUALIFICATIONS

4. All of my opinions stated herein are based on my own personal knowledge, professional judgment, and analysis of the materials and information I considered in preparing this Declaration. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching the technology referenced in this Declaration.

5. I am over the age of 18 and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my

current curriculum vitae, which details my education and professional and academic experience, is being submitted as Exhibit 1004. The following provides a brief overview of some of my experience that is relevant to the matters set forth in this Declaration.

6. I have over 35 years of experience in semiconductor memories and integrated circuits, including experience designing, implementing, fabricating, and securing integrated circuits and memory devices in addition to optimizing integrated circuits. My areas of research include design of digital and analog memory devices and integrated circuits, simulation-based analysis of integrated circuits, reverse engineering prevention of integrated circuits, and salvaging damaged or discarded printed circuit boards.

7. I received a Bachelor of Electrical Engineering from the University of Minnesota in 1975. I received a Master of Science in Electrical Engineering from Massachusetts Institute of Technology in 1977. I received a Ph.D. in Electrical Engineering from the University of California in Berkeley, California in 1986 where I wrote my thesis on memory devices and integrated circuits.

8. I am currently a professor at the University of Texas at Dallas. I have held this position since August 2005. Previously, I held the position of Associate Professor from July 1992 to June 1999 and Professor from July 1999 to August 2005 at the University of Washington. Prior to that role, I began my professional career at

Yale University as an Assistant Professor from July 1986 to June 1990 before I was elevated to Associate Professor. I remained at Yale University until June 1992.

9. I have authored or co-authored numerous journal publications concerning memory devices, integrated circuits, and related topics including:

- S. Senturia, C. Sechen, and J. Wishneusky, "The Charge-Flow Transistor: A New MOS Device," *Applied Physics Letters*, Vol. 30, No. 2, Jan. 1977, p. 106-108;
- S. Senturia and C. Sechen, "The Use of the Charge-Flow Transistor to Distinguish Surface and Bulk Components of Thin-Film Sheet Resistance," *IEEE Transactions on Electron Devices*, vol.24, no.9, p.1207, September 1977;
- C. Sechen, "Chip-Planning, Placement, and Global Routing of Macro Cell Integrated Circuits Using Simulated Annealing," *Int. J. Computer-Aided VLSI Design*, vol. 2, no. 2, 1990, pp. 127-158;
- J. J. Hsu and C. Sechen, "DC Small Signal Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I*, Vol. 41, No. 12, pp. 817-828, December 1994;
- W. Sun and C. Sechen, "Efficient and Effective Placement for Very Large Circuits," *IEEE Transactions on Computer-Aided Design*, Vol. 14, No. 3, pp. 349-359, March 1995;
- K. Roy, D. Guan and C. Sechen, "A Sea-of-Gates Style FPGA Placement Algorithm," *Int. Journal of VLSI Design*, Vol. 4, No. 4, pp. 293-307, 1996;
- Q. Yu and C. Sechen, "A Unified Approach to the Approximate Symbolic Analysis of Large Analog Integrated Circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, Vol. 43, No. 8, pp. 656-669, August 1996;

- L. Liu and C. Sechen, “Multi-layer Pin Assignment for Macro Cell Circuits”, *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 10, October 1999; and
- T. Thorp and C. Sechen, “Design and Synthesis of Dynamic Circuits,” *IEEE Transactions on VLSI Systems*, Vol. 11, No. 1, February 2003, pp. 141-149.

10. I authored the book *Placement and Global Routing of Integrated Circuits Using Simulated Annealing* in 1988. This book covered topics related to memory devices, integrated circuit design, development, and fabrication.

11. I am listed as the lead inventor on four total patents. These four patents (U.S. Patent Nos. 11,362,662; 10,855,285; 10,511,308; 6,549,038) are all related to integrated circuits.

12. I have graduated 34 Ph.D. students whose research was also related to memory devices and integrated circuits including:

- Kai-Win Lee (Yale May 1990) “Global Routing of Row-Based Integrated Circuits;”
- William Swartz (Yale May 1993) “Automatic Layout of Analog and Digital Mixed Macro/Standard Cell Integrated Circuits;”
- Kalapi Roy (University of Washington June 1994) “A Timing-Driven Multi-Way Partitioning System for Integrated Circuits and Multi-Chip Systems;”
- Jer-Jaw Hsu (University of Washington December 1994) “Fully Symbolic Analysis of Large Analog Integrated Circuits;”
- Wern-Jieh Sun (University of Washington December 1994) “Effective and Efficient Placement for Very Large Integrated Circuits;”

- Qicheng Yu (University of Washington March 1995) “Approximate Symbolic Analysis of Large Analog Integrated Circuits;”
- Bingzhong David Guan (University of Washington August 1996) “Automatic Layout Generation of Static CMOS Combinational Cells and Blocks;”
- Hsiao-Ping Tseng (University of Washington, December 1997) “Detailed Routing Algorithms for VLSI Circuits;”
- Yi Han (University of Washington, December 2004), “A High-Performance CMOS Programmable Logic Core for System-on-Chip Applications;”
- Mohammad Rahman (UT-Dallas, December 2011), “Power and Leakage Minimization for Digital ICs;”
- Anitha Yella (UT-Dallas, January 2016), “Power Optimization in ICs;” and
- Lubaba Nahar, (UT-Dallas, July 2022), “CAD Tools for PCB Reverse Engineering and IC Interconnect.”

13. I have taught classes on memory devices, analog and digital integrated circuits, and very large scale integration (“VLSI”) from 1992 until present day. I have also won teaching awards including:

- Department of Electrical Engineering at the University of Washington | Outstanding Research Advisor Award (2002);
- Department of Electrical Engineering, Erik Jonsson School of Engineering and Computer Science at the University of Texas at Dallas | Distinguished Teacher of the Year (2008); and
- Department of Electrical Engineering, Erik Jonsson School of Engineering and Computer Science at the University of Texas at Dallas | Distinguished Teaching Award (2014).

14. Throughout my career I have been recognized for various honors and awards outside of those including:

- Semiconductor Research Corporation | SRC Inventor's Recognition Award (1988, 2001) and SRC Technical excellence Award (1994);
- NSF Center for the Design of Digital and Analog ICs | Best Project Award (July 2002);
- IEEE Fellow (2002); and
- IEEE Ph.D. Research in Microelectronics and Electronics Conference | Best Paper Award (February 2017).

15. I have also been awarded funding for various research endeavors related to memory devices and integrated circuit design, development, and fabrication including:

- "Three-Transistor Memory Cell Research", Carl Sechen, Texas Instruments, Jan. – Dec., 2007;
- "DRAM-Density SRAM", Carl Sechen, Honeywell, January 2006 – April 2007;
- "Low Power Digital IC Design," NSF Center for the Design of Analog and Digital ICs (CDADIC), PI (Sep 03 – Aug 04);
- "Reconfigurable RF, Analog, and Digital Array for Radiation-Hardened Communication Circuits," Air Force Research Lab, PI (Sep 02 – Aug 03);

- “Ultra High Speed Digital Circuit Synthesis and Layout”, Semiconductor Research Corporation, PI (Mar 99-Mar 00);
- “Synthesis of Ultra High Speed Random Logic Blocks”, Semiconductor Research Corporation, PI (Mar 98-Feb 99);
- “Symbolic Analysis of Large Analog Circuits”, National Science Foundation, PI (Sep 94-Aug 97);
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), PI (Sep. 94-Aug. 95);
- “Automatic Layout Research”, Semiconductor Research Corporation, PI (Mar 93-Feb 94); and
- “High Speed Circuit Design and Mixed Signal Layout”, NSF Center for the Design of Analog and Digital ICs (CDADIC), PI (Sep. 92-Aug. 93).

III. SUMMARY OF OPINIONS

16. It is my opinion that claims 1 and 13–17 of the ’702 Patent are unpatentable under 35 U.S.C. § 103 on the following grounds:

- **Ground 1A:** Claims 13–17 are rendered obvious by U.S. Patent Application Publication No. 2002/0028541 (“Lee”) (Exhibit 1007);

- **Ground 1B:** Claims 16–17 are rendered obvious by Lee and U.S. Patent Application Publication No. 2002/054556 (“Endoh”) (Exhibit 1012);
- **Ground 1C:** Claims 13–17 are rendered obvious by Lee and U.S. Patent Application Publication No. 2003/0157748 (“Kim”) (Exhibit 1008);
- **Ground 1D:** Claims 16-17 are rendered obvious by Lee, Kim, and Endoh;
- **Ground 1E:** Claims 13–17 are rendered obvious by Lee and Aspar et al, The Generic Nature of the Smart-Cut® Process for Thin Film Transfer, 30 J. Elec. Materials 834 (2001) (“Aspar”) (Exhibit 1009);
- **Ground 1F:** Claims 16–17 are rendered obvious by Lee, Aspar, and Endoh;
- **Ground 2A:** Claim 13 is rendered obvious by U.S. Patent No. 6,034,882 (“Johnson”) (Exhibit 1010);
- **Ground 2B:** Claim 13 is rendered obvious by Johnson and Kim;
- **Ground 2C:** Claim 13 is rendered obvious by Johnson and Aspar;
and

- **Ground 3:** Claim 1 is rendered obvious by U.S. Patent No. 5,571,730 (“Park”) (Exhibit 1011) and Kim.

IV. MATERIALS REVIEWED

17. My opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge of the field.

18. In forming my opinions expressed in this Declaration, I have reviewed and considered the following materials:

- the ’702 Patent (“’702 Patent”) (Exhibit 1001);
- the prosecution history for the ’702 Patent (“’702FH”) (Exhibit 1002);
- U.S. Patent No. 7,052,941 (“’941 Patent”) (Exhibit 1005);
- the prosecution history for the ’941 Patent (“’941FH”) (Exhibit 1006);
- U.S. Patent Application Publication No. 2002/0028541 (“Lee”) (Exhibit 1007);
- U.S. Patent Application Publication No. 2003/0157748 (“Kim”) (Exhibit 1008);
- Aspar, The Generic Nature of the Smart-Cut® Process for Thin Film Transfer, 30 J. Elec. Materials 834 (2001) (“Aspar”) (Exhibit 1009);

- U.S. Patent No. 6,034,882 (“Johnson”) (Exhibit 1010);
- U.S. Patent No. 5,571,730 (“Park”) (Exhibit 1011);
- U.S. Patent Application Publication No. 2002/0154556 (“Endoh”) (Exhibit 1012)
- Silicon Processing, Vol. 1 by Stanley Wolf (2000) (Exhibit 1014);
- Silicon Processing, Vol. 4 by Stanley Wolf (2002) (Exhibit 1015);
- U.S. Patent No. 6,355,501 (“Fung”) (Exhibit 1016);
- U.S. Patent No. 5,414,288 (“Fitch”) (Exhibit 1017);
- U.S. Patent No. 6,027,975 (“Hergenrother”) (Exhibit 1018);
- U.S. Patent No. 6,337,247 (“Schulz”) (Exhibit 1019);
- U.S. Patent No. 6,449,186 (“Noble”) (Exhibit 1020);
- U.S. Patent No. 6,943,067 (“Greenlaw”) (Exhibit 1021);
- IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition (2000) (Exhibit 1022);
- U.S. Patent No. 5,882,987 (“Srikrishnan”) (Exhibit 1023);
- Maleville et al., Multiple SOI layers by multiple Smart-Cut® transfers, 2000 IEEE International SOI Conference (Oct. 2000) (“Maleville”) (Exhibit 1024);
- U.S. Patent No. 5,615,148 (“Yamamura”) (Exhibit 1025);

- U.S. Patent No. 5,544,103 (“Lambertson”) (Exhibit 1026);
- U.S. Patent No. 6,381,173 (“Zatelli”) (Exhibit 1027); and
- Any other materials cited in this declaration.

19. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '702 Patent, and the '941 Patent incorporated-by-reference in its entirety, at the time of the alleged invention, which I have been asked to initially consider no earlier than September 3, 2004 (the filing date of U.S. Patent Application No. 10/934,270). My opinions reflect how one of ordinary skill in the art would have understood the '702 Patent, the prior art to the patent, and the state of the art at the time of the alleged invention. My opinions would remain the same even if the '702 Patent were entitled to priority to U.S. Patent Application No. 10/873,969, such that the priority date would be June 21, 2004.

V. LEGAL PRINCIPLES

20. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person of ordinary skill in the art.

21. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my analysis, as summarized below.

A. PRIORITY DATE

22. I understand that, to gain benefit of the filing date of an earlier patent application, each application in the chain leading back to the earlier application must comply with the statutory written description requirement.

23. I understand that, to satisfy the written description requirement, a patent's specification must reasonably convey to a person of ordinary skill in the art ("POSITA") that the inventor had possession of the claimed subject matter when the patent application was filed. I understand that, to show "possession" of the invention, the disclosure must describe the invention, including all its claimed limitations. It is not enough that a claimed invention is an obvious variant of that which is disclosed in the specification. While the meaning of terms, phrases, or diagrams in a disclosure is to be explained or interpreted from the vantage point of a person of ordinary skill in the art, all the limitations must appear in the specification.

24. I further understand that entitlement to a filing date extends only to subject matter that is disclosed and not to subject matter that is not disclosed but would be obvious over what is expressly disclosed. Thus, a prior application itself must describe an invention, and do so in sufficient detail that a person of ordinary skill in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought.

25. I also understand that a patent's priority date is a legal determination based on underlying factual issues. For that reason, I am not rendering a legal opinion on the ultimate legal question of priority date. Rather, my testimony addresses the underlying facts and factual analysis that would support a legal determination of the priority date.

B. CLAIM INTERPRETATION

26. I understand from Counsel that during an IPR proceeding, claims are to be construed in light of the specification as would be read by a person of ordinary skill in the relevant art at the time the application was filed. I understand that claim terms are given their ordinary and customary meaning as would be understood by a person of ordinary skill in the relevant art in the context of the entire disclosure. A claim term, however, will not receive its ordinary meaning if the patentee acted as his or her own lexicographer and clearly set forth a definition of the claim term in the specification. In that case, the claim term will receive the definition set forth in the patent.

C. PRIOR ART

27. I understand from Counsel that certain patents and printed publications can be considered prior art in an IPR proceeding. I understand that prior art must predate the effective filing date of the claims of the patent-at-issue.

D. OBVIOUSNESS

28. I understand that a claim is unpatentable if the claim limitations, as arranged in a claim, would have been obvious to a person of ordinary skill in the art as of the date of invention. For example, a combination of familiar elements according to known methods is likely to be obvious if the combination does no more than produce predictable results.

29. In determining obviousness, I understand that the analysis may take into account multiple prior art references as well as the common knowledge possessed by a person of ordinary skill in the art (as discussed below). I further understand that the person of ordinary skill in the art is not an automaton but one having common sense and ordinary creativity. I also understand that a claim is not obvious simply because a combination of prior art references discloses each claim element collectively.

30. In determining obviousness, I understand that one should consider the following:

- The scope and content of the prior art;
- The differences between the claimed invention and the prior art;
- The level of ordinary skill in the pertinent art; and
- Secondary considerations of non-obviousness.

31. I understand that a person of ordinary skill in the art is assumed to have knowledge of all prior art references. I also understand that when considering the obviousness of a patent claim, one should consider whether a teaching, suggestion, or motivation to combine the references exists so as to avoid impermissibly applying hindsight when considering the prior art. I understand this test should not be rigidly applied, but that the test can be important to avoiding such hindsight.

32. I understand that a person of ordinary skill in the art can combine various prior art references based on the teachings of those prior art references, the general knowledge present in the art, or common sense. I understand that a motivation to combine the references may be implicit in the prior art, and there is no requirement that there be an actual or explicit teaching to combine two references. Thus, one may take into account the inferences and creative steps that a person of ordinary skill in the art would employ to combine the known elements in the prior art in the manner claimed by the patent-at-issue. I understand that one should avoid “hindsight bias” and ex post reasoning in performing an obviousness analysis. This does not mean, however, that a person of ordinary skill in the art for purposes of the obviousness inquiry does not have recourse to common sense.

33. I understand that the following are examples of approaches and rationales that may be considered in determining whether a prior art reference could

have been combined with other prior art or with other information within the knowledge of a person of ordinary skill in the art:

- Combining prior art elements according to known methods to yield predictable results;
- Simple substitution of one known element for another to obtain predictable results;
- Use of known techniques to improve similar devices, methods, or products in the same way;
- Applying a known technique to a known device, method, or product ready for improvement to yield predictable results;
- That it was “obvious to try”—i.e., that it was one choice from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- Known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; and
- Some teaching, suggestion, or motivation in the prior art that would have led a person of ordinary skill in the art to modify the prior art

reference or to combine multiple prior art reference teachings to arrive at the claimed invention.

34. I also understand that “obviousness” is a legal conclusion based on the underlying factual issues of the scope and content of the prior art, the differences between the claimed invention and the prior art, the level of ordinary skill in the art, and any objective indicia of non-obviousness. For that reason, I am not rendering a legal opinion on the ultimate legal question of obviousness. Rather, my testimony addresses the underlying facts and factual analysis that would support a legal conclusion of obviousness, and when I use the term obvious, I am referring to the perspective of a person of ordinary skill in the art at the time of invention.

VI. LEVEL OF ORDINARY SKILL IN THE ART

35. I understand that a POSITA is a hypothetical person who is presumed to have known the relevant art at the time of the invention. To determine the level of skill held by a person of ordinary skill in the art, I understand that a number of factors may be considered, including the following:

- The type of problems encountered in the art;
- Prior art solutions to those problems;
- Rapidity with which innovations are made;
- Sophistication of the technology; and
- Educational level of active workers in the field.

36. I understand that not all of the above factors will be present in every case and one or more factors may predominate.

37. In view of the above factors, it is my opinion that a person of ordinary skill in the art as of either June 21, 2004 or September 3, 2004 would have had at least a bachelor's degree in electrical engineering, computer engineering, materials science, or a related field and at least three years of experience in the research, design, or development of semiconductor memory device structures, integrated circuits, or the equivalent, with additional education substituting for experience and vice versa.

38. I understand that the '702 Patent is currently challenged by Micron Technology Inc., et al. in IPR2023-00900, where Petitioners propose a slightly different articulation of the level of ordinary skill in the art. My opinions would not change under the articulation of ordinary skill in the art proposed by Petitioners in IPR2023-00900.

39. As of the effective filing date of the '702 Patent, I met, and in fact exceeded, the qualifications of a person of ordinary skill in the art. My opinions are offered from this perspective, even if they do not specifically refer to the perspective of a person of ordinary skill in the art.

VII. TECHNOLOGICAL BACKGROUND

40. The technology at issue, at the time of the alleged priority date of June 21, 2004 or September 3, 2004, was well known. In particular, each of the technologies involved were well known, including (1) wafer bonding, and (2) vertically-oriented transistors.

A. Wafer Bonding and SOI Technology

41. Forming semiconductor layers on separate wafers and then bonding them together to create stacked semiconductor structures, i.e., wafer bonding, was well-known by 2004. *See e.g.*, Exhibit 1015, 54. Specifically, wafer bonding can be used to bond two wafers together (e.g., if devices are fabricated on separate substrates and then stacked). *Id.*

42. Known techniques for wafer bonding included Bond and Etch-Back, Smart-Cut®, Nanocleave™ (by Silicon Genesis, Inc., aka “SiGen”), and ELTRAN®. Exhibit 1014, 92–93; Exhibit 1015, 58–67. Each is cited in U.S. Patent Application No. 10/873,969 (issued as U.S. Patent No. 7,052,941 (Exhibit 1005, “the ’941 Patent”)), which has the same inventor and is incorporated by reference in its entirety into the ’702 patent. ’941 Patent, 9:40–47, 9:63–10:1; ’702 patent, 1:7–10. Thus, the ’702 Patent expressly discloses known prior art wafer bonding techniques. ’941 Patent, 9:40–47, 9:63–10:1; ’702 patent 1:7–10.

43. In well-known wafer bonding techniques, two wafers are brought into contact, attracted to each other by van der Waals forces, and adhere together. Exhibit 1015, 54. One example of a wafer bonding process is pictured in the figure below.

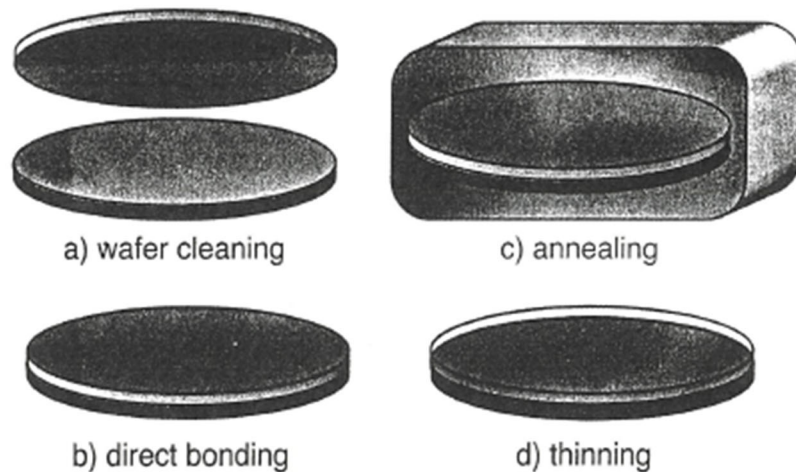


Fig. 11-21 Generic direct-wafer-bonding process flow.

Exhibit 1015, Fig. 11-21 (p.56)

In this process, pressure is first applied to the two wafers at room temperature, and heat is subsequently applied in a furnace anneal. Exhibit 1015, 54–56; Exhibit 1014, 91. Thereafter, one of the wafers is typically thinned (e.g., silicon is removed). Exhibit 1015, 56–58; Exhibit 1014, 91.

44. Several ways to bond two wafers were well-known at the relevant time including, for example: (1) applying external pressure and an oxidizing-ambient at high heat to two wafers positioned face-to-face, thus converting trapped oxygen between the wafers into silicon dioxide; (2) applying moderate voltage at high temperatures across two wafers positioned face-to-face; and (3) treating the wafers

with an acid solution, drying the wafers, positioning the wafers face-to-face at room temperature in clean air, and annealing the wafers in a nitrogen-ambient at high temperatures. Exhibit 1014, 91–92; Exhibit 1015, 57. Removal of most of the silicon from one of the wafers after bonding is important to produce the SOI structure. Exhibit 1014, 92; Exhibit 1015, 58.

45. The Bond and Etch-Back method (pictured below) includes removing the heavily doped substrate of one wafer by mechanical methods (e.g., grinding). Exhibit 1014, 92; Exhibit 1015, 58–59.

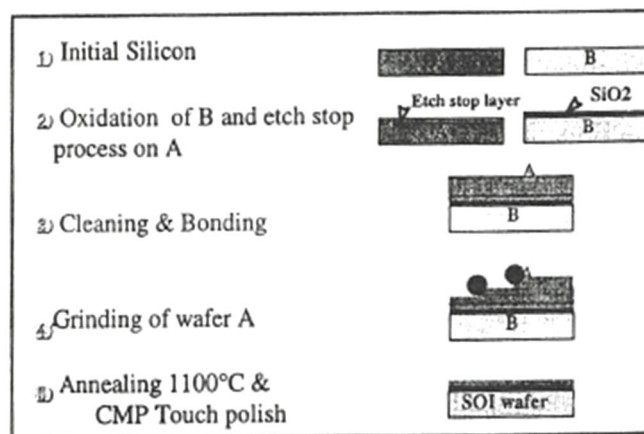


Fig. 11-23 Schematic of the Bonded-and-Etched-Back SOI technology (*BESOI*).

Exhibit 1015, Fig. 11-23 (p. 59)

46. The Smart-Cut® method (shown below) starts by oxidization and ion-implantation of wafer A. Exhibit 1014, 92–93; Exhibit 1015, 59–61.

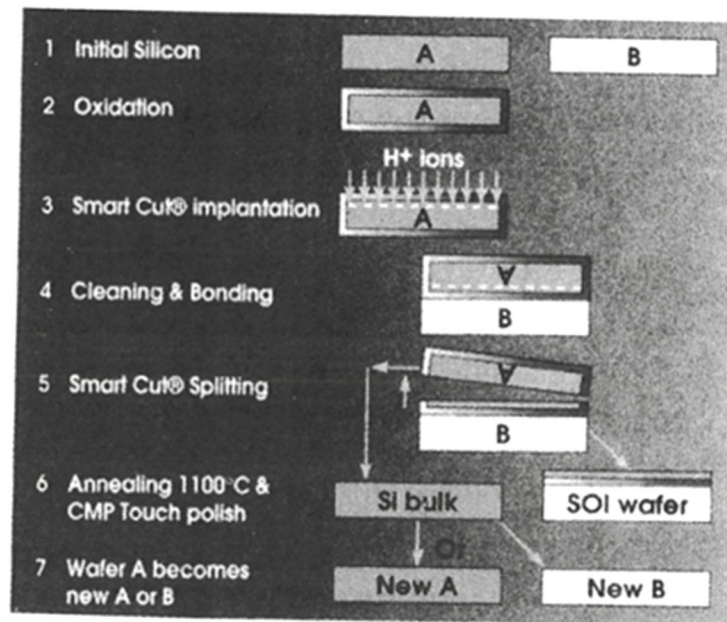


Fig. 11-24 Process flow for fabricating Smart-Cut® wafers.

Exhibit 1015, Fig. 11-24 (pg. 60); *see also* Exhibit 1014, Fig. 7-29 (pg. 92).

47. Next, wafers A and B are cleaned and bonded face-to-face at a low temperature. Exhibit 1014, 92–93; Exhibit 1015, 59–61. Wafer A is then split leaving the remaining structure to serve as the SOI wafer. Exhibit 1014, 92–93; Exhibit 1015, 59–61.

48. The Nanocleave™ method (shown below) begins with the formation of a donor wafer. Exhibit 1015, 61–62.

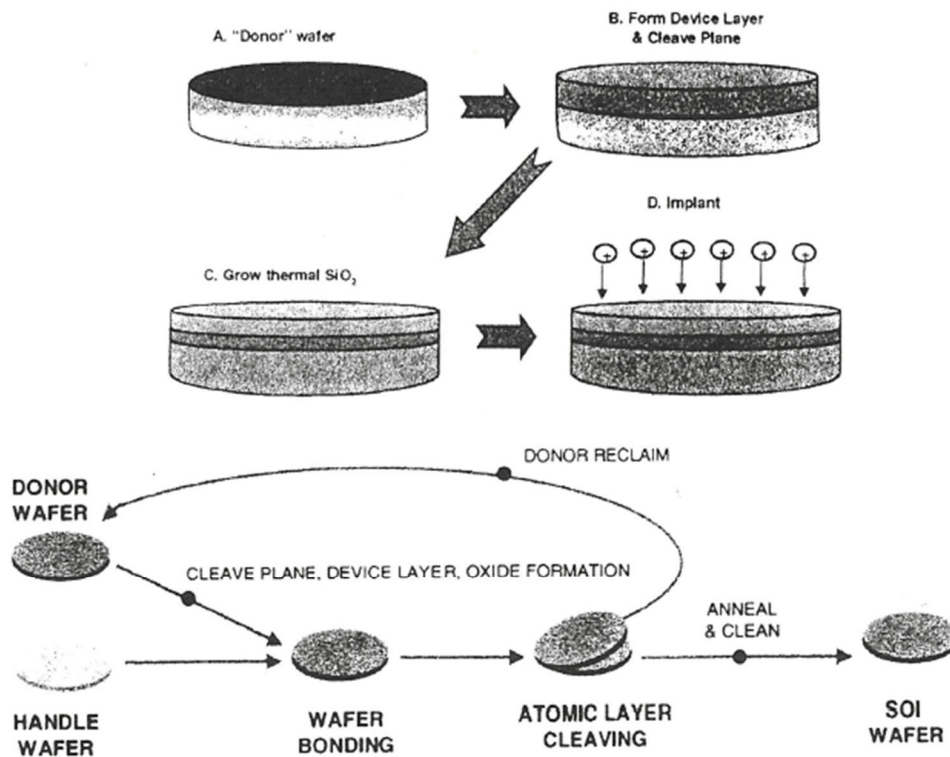


Fig. 11-25 Process flow of the Nanocleave® SOI technology.

Exhibit 1015, Fig. 11–25 (p.62)

49. The cleave-plane is created by epitaxially growing a layer of Si-Ge on a donor wafer and continuing to grow the layer with an epitaxial silicon-device layer. Exhibit 1015, 62. The donor wafer is then bonded to the handle wafer on which the device layer will ultimately reside. *Id.*, 62–63. The bond strength is significantly greater than the interface-strength along the cleave plane, allowing for a different cleaving process to separate the Si device layer from the donor wafer. *Id.*, 63. Unlike the Smart-Cut method, donor wafer cleaving in the Nanocleave™ method occurs by applying a high-pressure nitrogen gas along the Si-Ge layer at room temperature.

Id., 62–63. Any residual Ge-rich layer can be removed through a selective etch step.

Id., 64.

50. The ELTRAN® process (shown below) begins by growing a double porous silicon layer on a donor wafer, with each porous layer having a different porosity. Exhibit 1015, 64–66. An epitaxial layer is grown on top of the porous silicon, and then the surface of the epitaxial layer is thermally oxidized. *Id.*, 64. The donor wafer is bonded to a handle wafer, and then the donor wafer is split off between the porous silicon sublayers using water-jet technology. *Id.*, 64–66. The device layer over a buried oxide layer is then formed by etchback of the porous silicon and hydrogen-annealing. *Id.*, 66.

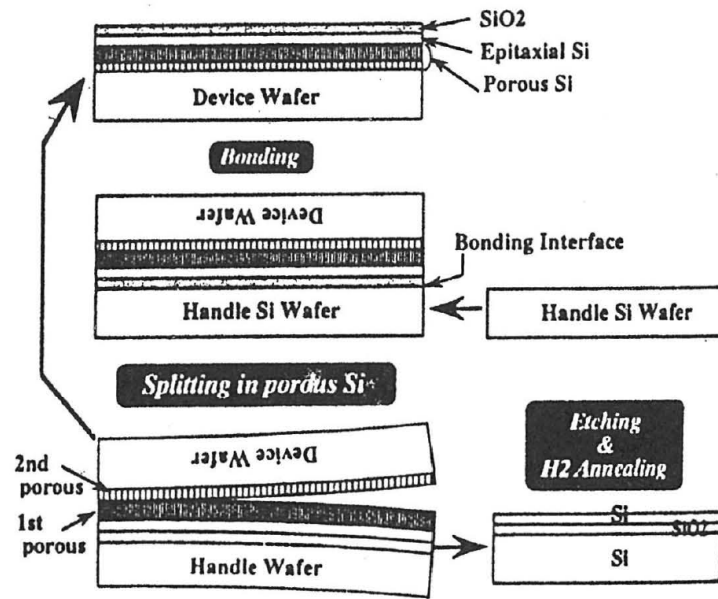


Fig. 11-29 The ELTRAN process flow for device wafer re-usage. Bonded pairs are split within the porous-Si layer. The device wafer sides are used as a starting device wafer. The handle sides result in ELTRAN wafers after etching the porous-Si and H₂-annealing.

Exhibit 1015, Fig. 11-29 (p. 66)

B. Vertically-oriented transistors

51. Vertically-oriented transistors were well-known years, maybe even a decade, prior to the effective filing date of the '702 Patent. The '941 Patent even identifies that vertical devices were known at the time. For example, the '941 Patent features Figure 1 (annotated below) showing prior art that has a vertical device 212.

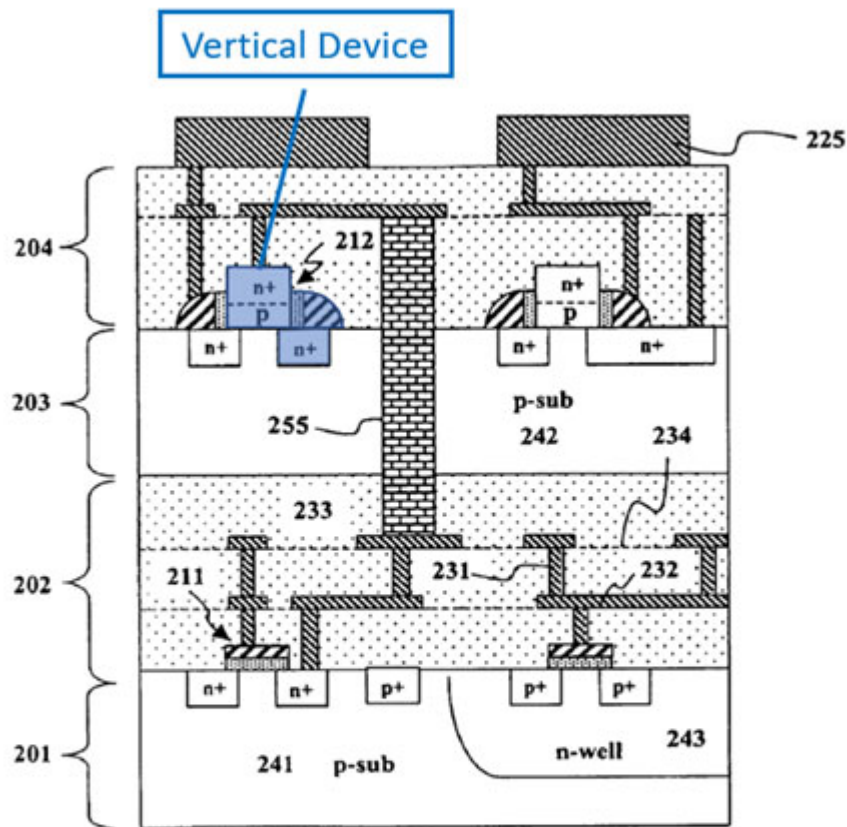


Fig. 1 (Prior Art)

'941 Patent, Fig. 1

The '941 Patent also states that U.S. Patent Nos. 5,414,288; 6,027,975; 6,337,247; and 6,449,186 have “vertical devices.” Exhibit 1005, 12:34–38.

52. U.S. Patent No. 5,414,288 (“Fitch”) was filed on February 16, 1994 and issued on May 9, 1995. Exhibit 1017. Fitch states:

A planar transistor has a diffused source electrode and a diffused drain electrode separated by a channel region. Overlying the channel region is a gate electrode that is separated from the channel region by a gate

oxide. Planar transistors, although used and useful in many integrated circuit applications, are substrate area intensive.

Exhibit 1017, 1:15–22. “Planar transistors” are parallel to a substrate surface, that is, horizontally-oriented. Fitch then states that “vertical transistors are known in the art,” and is directed to improving upon these known transistors. *Id.*, 1:66–2:6.

53. U.S. Patent No. 6,027,975 (“Hergenrother”) was filed on August 28, 1998 and issued on February 22, 2000. Exhibit 1018. Hergenrother is directed to a process for fabricating vertical transistors, specifically MOSFETs. *Id.*, Abstract. Hergenrother states: “[t]he device is called a vertical transistor because the length of the channel is perpendicular to the substrate surface.” *Id.*, 1:36–38. Vertical transistors are perpendicular to the substrate and not parallel like planar or horizontal transistors.

54. U.S. Patent No. 6,337,247 (“Schulz”) was filed January 18, 2000 and issued January 8, 2002. Exhibit 1019. Schulz is directed to a “[m]ethod of producing a vertical MOS transistor” that overcomes “deficiencies and disadvantages of the prior art devices and methods.” *Id.*, Title, 2:11–18. Schulz states: “[s]ince the channel length extends vertically in relation to a surface of a substrate, the surface area of a vertical transistor can be smaller than that of conventional planar transistors.” *Id.*, 1:42–45. The transistors in Schulz are vertical (i.e., perpendicular) in relation to a substrate surface.

55. U.S. Patent No. 6,449,186 (“Noble”) was filed August 8, 2001 and issued September 10, 2002. Exhibit 1020. Noble is directed to “circuits and methods for a static random access memory using vertical transistors.” *Id.*, 1:10–12. Noble states a “method includes forming vertical bars of semiconductor material on a surface of a semiconductor wafer.” *Id.*, 2:34–37. Noble also defines vertical as “a direction perpendicular to the horizontal” where horizontal is defined as “a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate.” *Id.*, 3:44–48.

56. The ’941 Patent cites several patents dating as far back as 1994 that disclose vertically-oriented transistors. Vertically-oriented transistors were well known at the relevant time. It was also well-understood that vertically-oriented transistors were beneficial for increasing the density of devices on an integrated chip. For example, U.S. Pat. Appl. Publ. No. US 2002/0028541 (“Lee”) describes conventional horizontal memory cells as “expensive because their density is not optimized,” while the vertical memory cells reduce cost because of increased density. *See* Ex. 1007 at [0017], [0106]; *see also*, Ex. 1010 at Abstract (describing memory cell array including “vertically fabricated memory cells” as “very high density”); Ex. 1019 at 1:13-25, 2:10-18 (discussing increasing integration density by using vertical MOS transistor).

VIII. OVERVIEW OF THE '702 PATENT

A. The Challenged Claims

57. Petitioner's Petition challenges (and in this Declaration I address) claims 1 and 13–17 of the '702 Patent. Of these, claims 1 and 13 are independent. For reference, I have reproduced the challenged claims below:

1. A semiconductor memory structure, comprising:

a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and

a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;

wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and

wherein the memory cell is a DRAM having at least one transistor.

13. A semiconductor memory structure, comprising:

a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

the stackable add-on layer being bonded to the dielectric layer; and

wherein the memory cells are nonvolatile memory cells having at least one transistor.

14. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

15. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

58. As an example, claim 13 recites a structure with the following components: (A) a substrate with (i) electrical devices formed therein and (ii) a dielectric layer above the electrical devices; (B) a stackable add-on layer with a plurality of non-volatile vertically oriented memory cells having at least one transistor; and (C) the stackable add-on layer bonded to the dielectric layer. As I discuss in the Technological Background section and in the unpatentability grounds below, these components were not new.

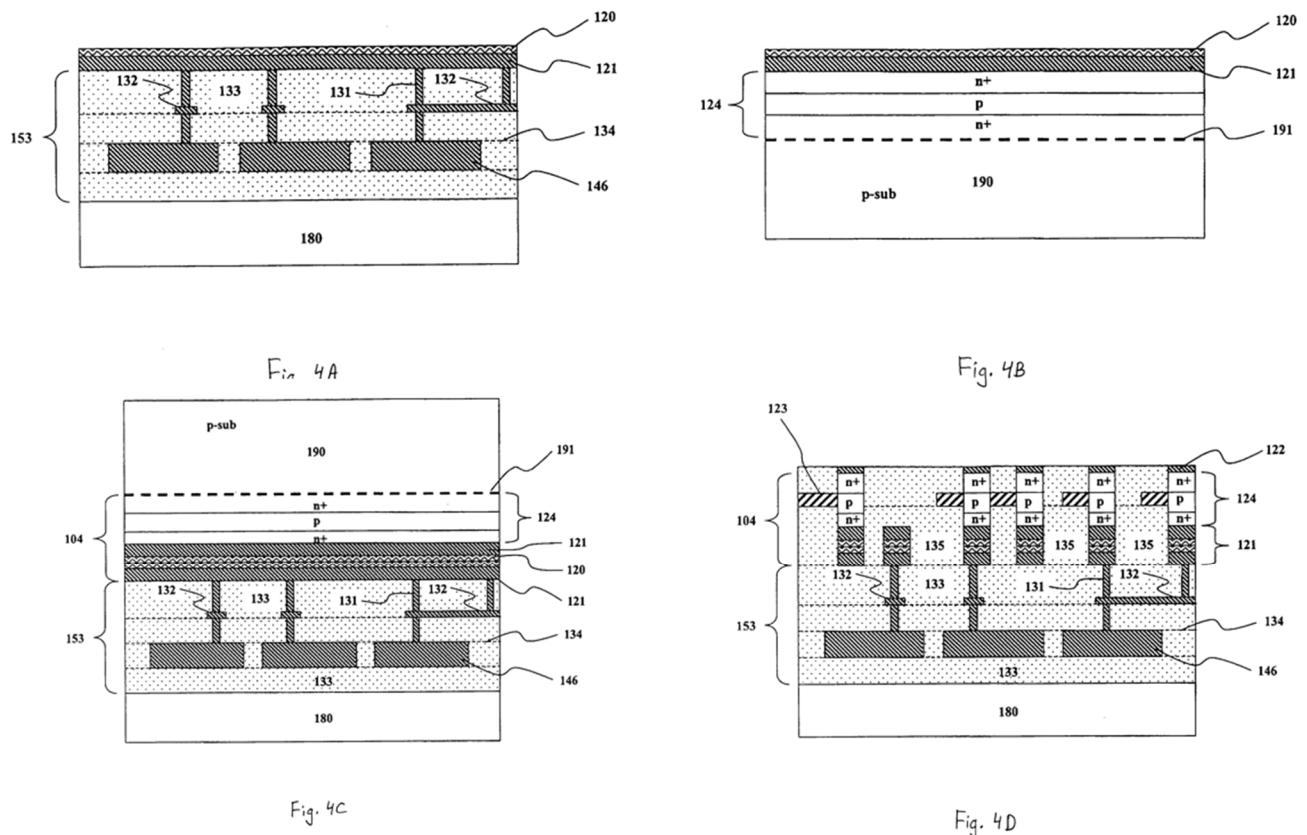
B. The '941 Patent (Parent to '702 Patent)

1. '941 Specification

59. The '702 Patent is a continuation-in-part of application No. 10/873,969, filed on Jun. 21, 2004, that issued as US Patent No. 7,052,941 ("the '941 Patent").

'702 Patent, (63). The disclosure of the '941 Patent is incorporated by reference in its entirety into the '702 Patent. *Id.*, 1:7–10.

60. The '941 Patent provides detail about “bonding” of the stackable add-on layer. '941 Patent, Abstract. In particular, the '941 Patent explains a process for making three-dimensional integrated circuit (“3-D IC”) structures in its Figures 4A–D. *Id.*, 2:46–48, 8:53–54; 9:19–10:25.



'941 Patent, Figs. 4A–4D.

61. Figures 4A and 4B show the two wafers used in the process described by the '941 Patent. Figure 4A shows (i) base substrate 180, (ii) dielectric layer 153 with single or multiple inter-layer dielectric layers 133, (iii) metal layer 121 used as

a bottom electrode, and (iv) metal layer 120 used as an intermediate bonding layer with a lower melting point than the metal layer 121 on dielectric layer 153. '941 Patent, 8:54–9:18.

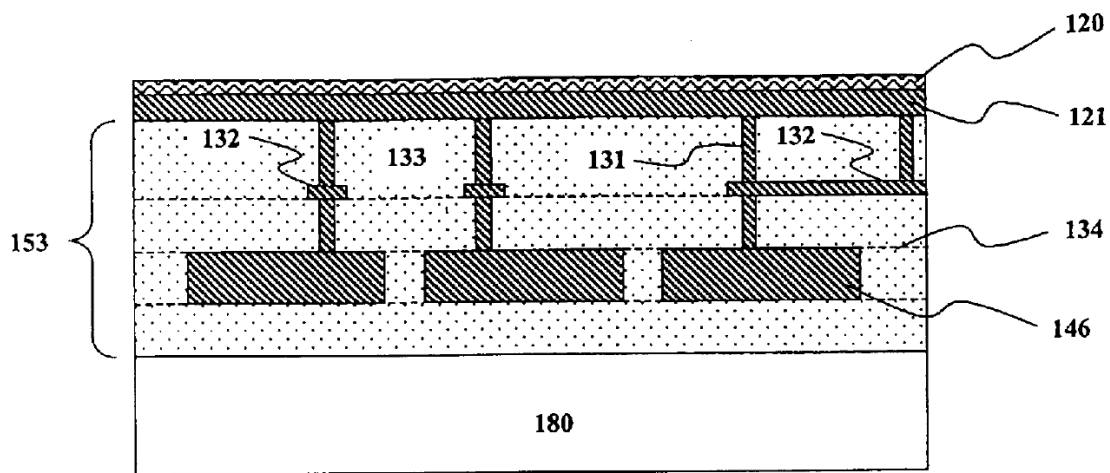


Fig. 4A

'941Pat, Fig. 4A.

62. Figure 4B shows an entirely separate wafer with (i) SOI substrate 190 with an optional detach layer 191 implemented “using, for example, SmartCut ... ELTRAN ... or SiGen technologies” ('941 Patent, 9:40–43) (ii) single crystal semiconductor layer 124 where doped regions can be formed using known methods like ion implantation or epitaxial layer growth, (iii) metal layer 121, and (iv) bonding layer 120 formed on metal layer 121 ('941 Patent, 9:19–39).

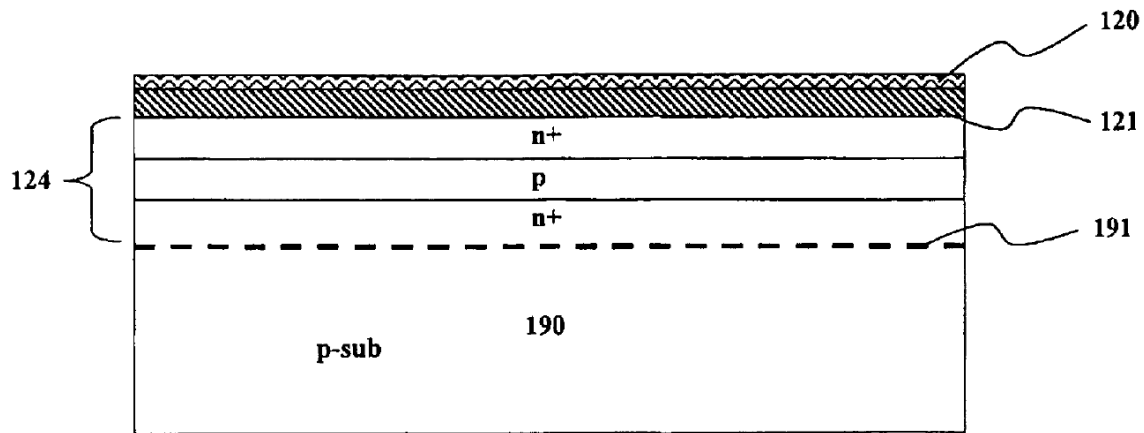
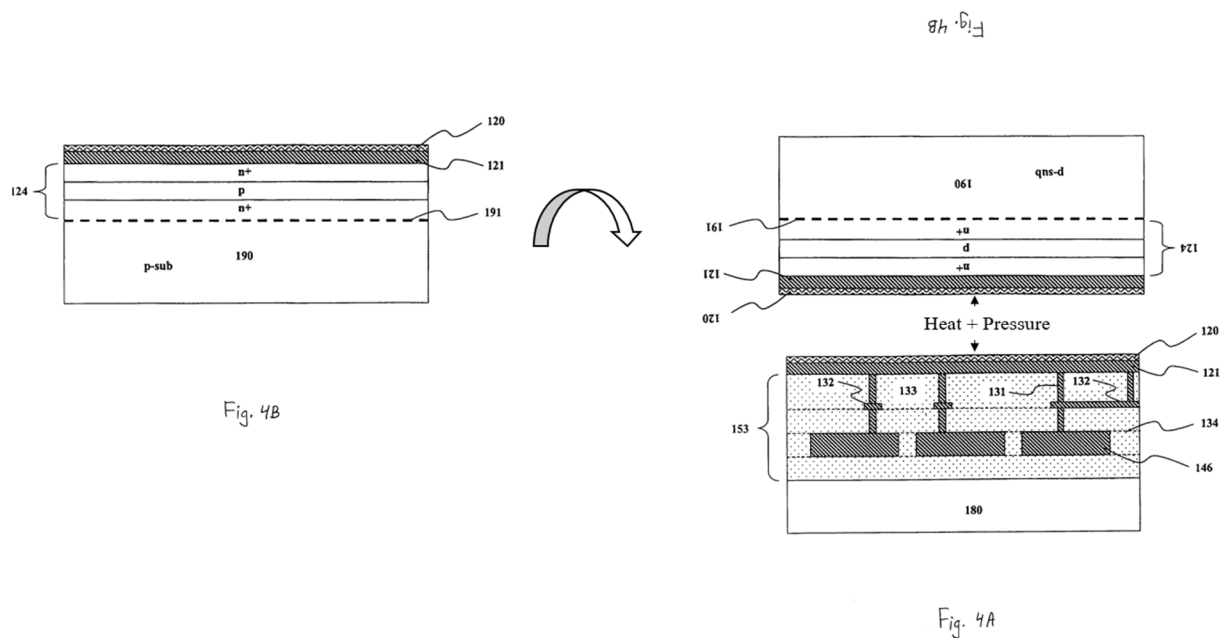


Fig. 4B

'941Pat, Fig. 4B.

63. The '941 Patent explains that the wafer shown in its Figure 4B is flipped upside-down and bonded to the top of the wafer shown in its Figure 4A by applying heat and pressure. '941 Patent, 9:48–59. I have modified Figures 4A and 4B below to depict this process:



'941 Patent, FIGS. 4A–B (annotated and combined).

64. Figure 4C shows the result of this bonding:

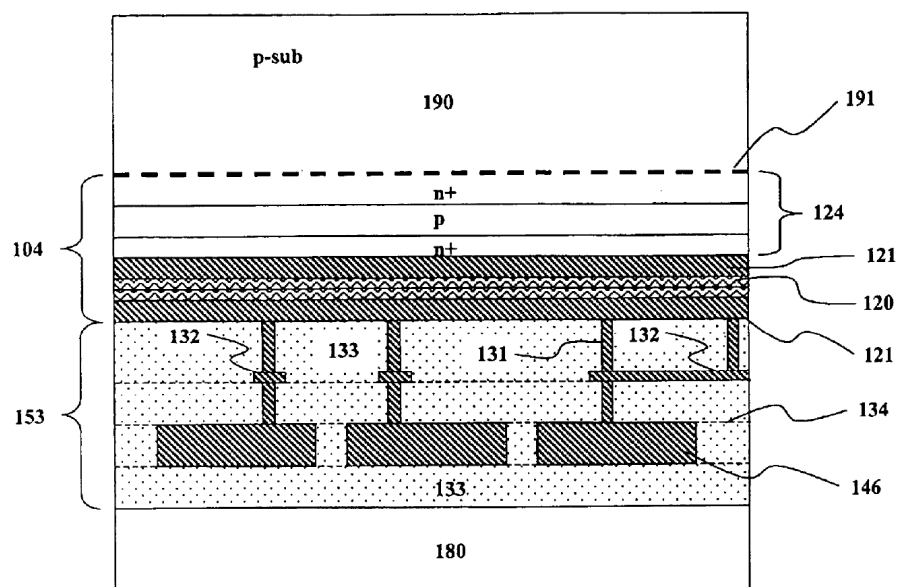


Fig. 4C

'941 Patent, Fig. 4C.

65. Figure 4D shows the final result of the '941 Patent's 3D-IC fabrication process. SOI layer 124, also referred to alternatively as "an SOI" ('941 Patent, 6:44-46) and a stackable add-on layer (*id.*, 6:44-46), is exposed by detaching the SOI substrate 190 using detach layer 191 and a wafer jet or by either etching or polishing away SOI substrate 190. '941 Patent, 9:60–10:21. Alternatively, SOI substrate 190 can be bonded to a handling or temporary substrate that uses a vacuum so that SOI layer 124 can easily be transferred to a dielectric layer without damage by releasing the vacuum. *Id.* Once the SOI substrate has been detached and the SOI layer transferred to a dielectric layer, floating devices are made using isolation. *Id.*, 10:22–25. "As shown in Fig. 1, vertical memory devices 656 in accordance with the present invention are separated by isolation 135 and have floating structures in the filled dielectric materials 133a. Vertical memory devices 656 are referred herein to as floating devices (FLD)." '702 Patent, 5:18–22; *see also* '941 Patent, 9:60–63. Such SOI devices are referred to as "floating" insofar as they are not tethered to an underlying semiconductor wafer, and rather are surrounded by an insulator or dielectric. *See, e.g.*, '702 Patent, 5:18–22, Fig. 1.

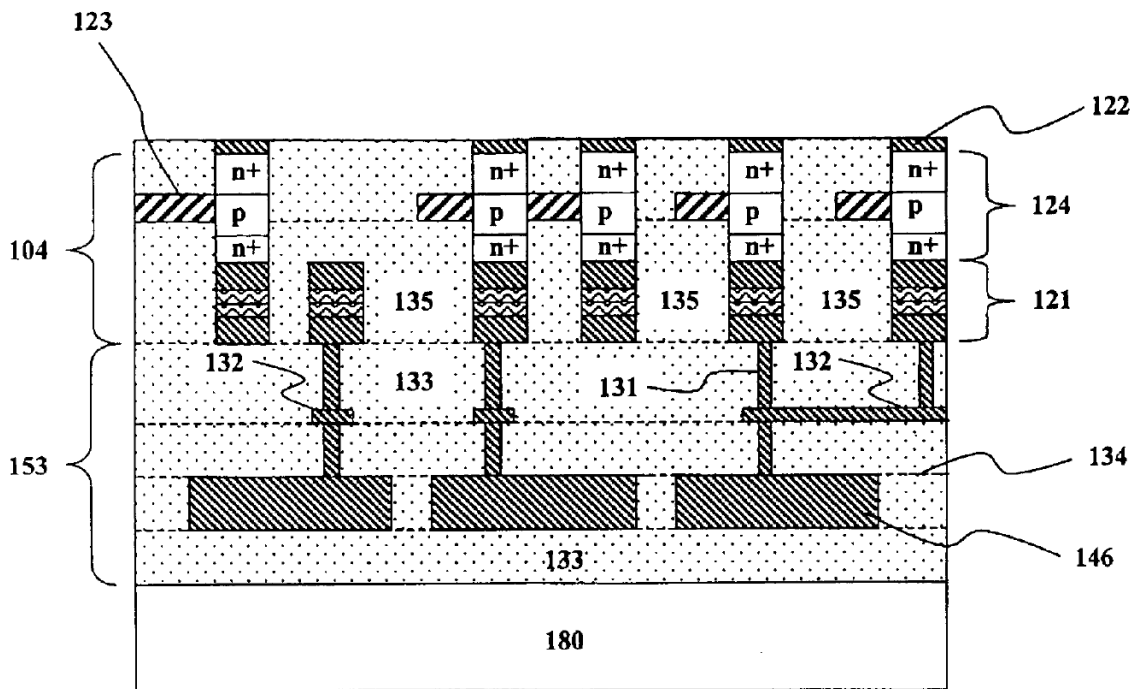


Fig. 4D

'941 Patent, Fig. 4D.

2. '941 Prosecution History

66. During the prosecution of the '941 Patent, the Examiner did not make any prior art based rejections, and did not consider any of the references on which I based my unpatentability opinions.¹ In a Non-Final Office Action dated September

¹ In a Non-Final Office Action dated November 28, 2005, the Examiner listed U.S. Patent Number 6,943,067 ("Greenlaw") as "prior arts made of record but not relied upon." Exhibit 1006, 46.

13, 2005, I understand that the Examiner required the applicant to elect between two species of claims. Exhibit 1006, 64–70. After the applicant made that election, the Examiner later objected to claim 1 because “[t]hat is the greatest distance from the substrate” was indefinite, recommending the applicant amend the claim to include “measuring from the bottom surface of the substrate.” *Id.*, 43–48. After the applicant amended claim 1,² the Examiner allowed the ’941 claims. *Id.*, 23–29.

C. The ’702 Patent

1. The Specification

67. The ’702 Patent is directed to “[v]ertically oriented semiconductor memory cells” that are “added to a separately fabricated substrate that includes electrical devices and/or interconnect.” ’702 Patent, Abstract. The memory cells can include SRAM, DRAM, or nonvolatile memory, and are added to the separately fabricated substrate as either a thin layer of doped and etched semiconductor regions or by attaching pre-fabricated memory cells. *Id.*, Abstract, 1:56–2:9. The memory cells are described as being “vertically oriented with respect to a major surface of a wafer” or substrate. *Id.*, 3:50–61; *see also id.*, 4:7–9. Consistent with well-known

² Applicant added “as measured from the bottom surface of the substrate” to pending independent claim 1 to address the examiner’s indefiniteness objection. Exhibit 1006, 39.

vertically oriented transistors, the '702 Patent states that the benefit of utilizing this vertical device orientation is to increase the density of devices, and thus functionality, for a “chip of given surface area.” *Id.*

68. The '702 Patent further describes the process of adding the vertical memory cells as a “stackable add-on layer” to a separately fabricated substrate. '702 Patent, Abstract, 1:47–50, 1:57–62, 1:67–2:9. This process includes a series of doping and etching steps which produce individual pillar-shaped structures that form the transistor components of the memory cells. *See id.*, Abstract, 1:56–2:3. The “stackable add-on layer” is described as a Silicon-on-Insulator (“SOI”) layer that “can be formed a variety of ways” known to those skilled in the art. *Id.*, 4:45–5:7. The '702 Patent states that “SOI layer” “is used herein to refer to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate.” *Id.*, 4:47–53. “In this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections. As a stackable add-on layer, the single-crystal layer may have been doped so as to have one or more doped regions vertically adjacent each other.” *Id.*, 4:53–60.

2. The Prosecution History

69. The application leading to the '702 Patent was filed on September 3, 2004, and as I discuss above, is a continuation-in-part of the application leading to the '941 Patent, filed on June 21, 2004. '702 Patent, (21), (22), (63).

70. During the prosecution of the '702 Patent, the Examiner did not make any prior art based rejections, and did not consider any of the references on which I base my unpatentability opinions. In a Non-Final Office Action dated March 1, 2006, I understand that the Examiner (i) objected to the pending claims because "...that is the greatest distance from the substrate..." recited in the pending independent claims could be indefinite and (ii) rejected the pending claims for obviousness-type double patenting over the claims of the application that led to the '941 Patent. Exhibit 1002, 72–75. The Examiner cited only one reference, Greenlaw (Exhibit 1021), in the Non-Final Office Action but did not rely on the reference in rejecting the claims. *Id.*, 77. That reference is the only reference cited on the face of the '702 Patent. '702 Patent, (56). After the applicant amended the claims³ to address

³ Applicant added "as measured from the bottom surface of the substrate" to independent claims 1 and 8 to address the examiner's indefiniteness objection. Exhibit 1002, 83, 85. Applicant amended pending independent claim 14 (issued as

the examiner's objection and submitted a terminal disclaimer, the Examiner allowed the claims. Exhibit 1002, 83–88, 117–119.

IX. CLAIM CONSTRUCTION

A. “Stackable add-on layer ... the stackable add-on layer [is]/[being] bonded” (Claims 1 and 13)

71. Independent claim 1 recites “wherein the stackable add-on layer *is bonded to* a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate,” and independent claim 13 recites “the stackable add-on layer *being bonded* to the dielectric layer.” In my opinion, in the context of the intrinsic record of the '702 Patent, a person of ordinary skill in the art would have understood these limitations to require that the “stackable add-on layer” is wafer bonded to the recited layer of the substrate.

independent claim 13) by removing the limitation the examiner objected to and replacing it with “the stackable add-on layer *being bonded to the dielectric layer.*” Exhibit 1002, 87 (emphasis added). Applicant further amended the limitation in pending claim 14 reciting “[a plurality of vertically oriented semiconductor memory cells] *disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor devices separated from each other by dielectric material.*” *Id.* (emphasis showing deleted portion).

72. Based on the plain language, in my opinion, a person of ordinary skill in the art would have understood “stackable add-on layer” to be its own structure capable of being stacked and added on to the other recited structure. This concept can be analogized to creating a layer cake: each layer is baked individually and then the layers are stacked on top of one another. Similarly for the “stackable add-on layer” recited in claims 1 and 13, the stackable add-on layer is its own layer (one cake layer) capable of being stacked on another (the bottom cake layer). Based on my experience in the relevant art, a POSITA would have understood such stacking to be performed by wafer bonding of those layers.

73. This understanding is in line with the intrinsic record. The ’702 Patent describes its “SOI layer” as a stackable add-on layer. ’702 Patent, 4:53–57 (“[T]he SOI layer may be thought of as ... [a] stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.”). “[T]he ‘SOI layer’ is used herein to refer to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate.” *Id.*, 4:48–53.

74. In my opinion, a POSITA would have understood the ’702 Patent’s description of its “SOI layer” requires wafer bonding. As I discuss above in Section

VIII.B.1, the incorporated '941 Patent ('702 Patent, 1:7–10) describes a process for creating a structure containing an SOI layer⁴ in its Figures 4A–D. '941 Patent, 8:53–10:56. The '941 Patent also describes existing technologies that allow for its SOI substrate to have a detach layer, so that after bonding, the SOI substrate can be removed other than the desired portion (i.e., including the stackable add-on layer). *Id.*, 6:61, 9:40–47 (“SOI substrate 190 may have a detach layer 191...using, for example, SmartCut (U.S. Pat. No. 5,882,987).”). A POSITA would have understood that those wafer bonding processes cited in the intrinsic record were known to allow for a thin monocrystalline film formed on one wafer to be bonded to another previously fabricated wafer and then cleaved, like the description of the “SOI layer” in the '702 Patent. '702 Patent, 4:46–60; Exhibit 1023, Abstract, 1:17–61, 4:8–16.

75. I note that the statement in the '702 Patent that “the substrate bonded to lower dielectric layer 151 is called base substrate 103” ('702 Patent, 5:37–38; '941 Patent, 7:14–15 (same)) does not affect my opinion on the proper construction of “stackable add-on layer [is]/[being] bonded” because that statement refers to bonding a dielectric layer, not a “*stackable add-on*” layer, to the substrate. A POSITA would have understood bonding of a dielectric layer to be different, for

⁴ The '941 Patent also describes its “SOI layer” as a stackable add-on layer. '941 Patent, 6:12–17, 10:1–2.

example, than bonding of an SOI layer which the '702 Patent describes as a "stackable add-on layer." '702 Patent, 4:45–5:7; '941 Patent, 6:4–28.

76. The '702 Patent's description of its "SOI layer" (i.e., stackable add-on layer) is further consistent with known techniques for separately forming layers and then bonding them. As I explain above in Section VIII.B.1, the '941 Patent is incorporated by reference into the '702 Patent, and like the '702 Patent, the '941 Patent describes its "SOI layer" as a stackable add-on layer. '941Pat., 10:1–2 ("This SOI layer 124 may also be referred to as a stackable add-on layer.").

77. The '941 Patent describes a process for creating a structure containing an SOI layer in its Figures 4A-D. In Figure 4B, "doped layers are formed in single crystal semiconductor layer 124, where the doped layers may be formed by any suitable method including, but not limited to, ion implantation, or impurity mixing during epitaxial layer growth for single crystalline semiconductor layer 124 formation." *Id.*, 9:19–24. These doped layers are formed on SOI substrate 190 (*id.*, 9:19, Fig. 4B), and then, the SOI substrate with doped layers (Figure 4B) is flipped upside-down and bonded to dielectric layer 153 as shown in Figure 4C. *Id.*, 9:48–51. The SOI substrate is then detached. *Id.*, 9:40–47, 9:60–10:2.

78. The '941 Patent identifies known technologies that allow for SOI substrate 190 in Figure 4B to have detach layer 191, so that after bonding, SOI substrate 190 can be removed while retaining the desired portion (i.e., the stackable

add-on layer). *Id.*, 9:40–47 (“SOI substrate 190 may have a detach layer 191, which may be a porous or strained layer at a certain desired depth using, for example, Smart-Cut® (U.S. Pat. No. 5,882,987), ELTRAN® (U.S. Pat. No. 5,371,037), or SiGen technologies”). Indeed, these are the very same technologies I discuss above in Section VII.A. After bonding with dielectric layer 153, SOI substrate 190 will be removed except for single crystal layer 124 which forms the FLD [floating device].”). This can be seen in Figures 4C and 4D of the ’941 Patent:

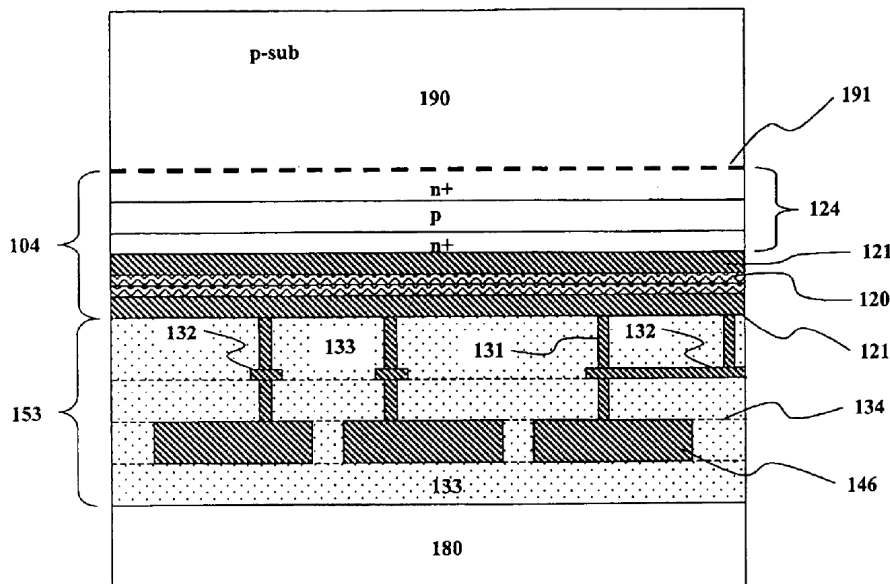


Fig. 4C

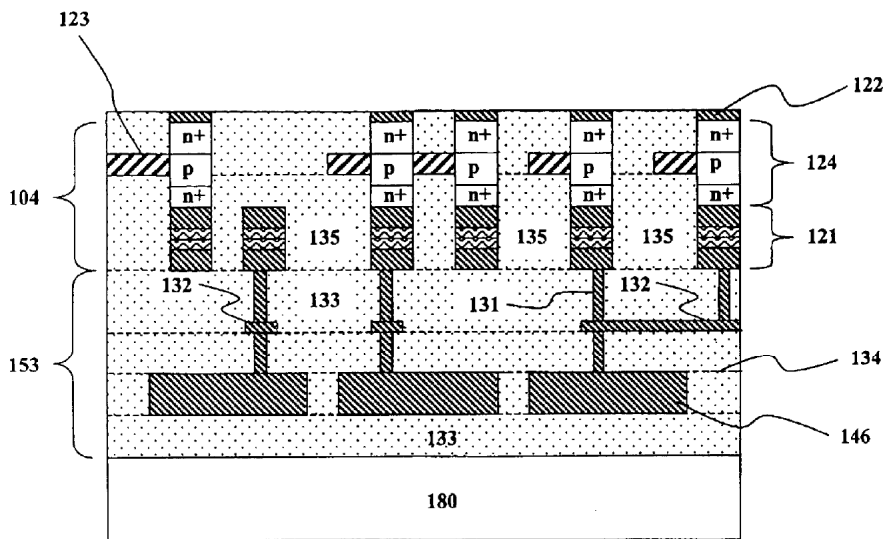


Fig. 4D

79. As noted above, one of the examples identified in the '941 Patent specification is Srikrishnan (U.S. Pat. No. 5,882,987), issued on March 6, 1999, over five years before the earliest possible priority date of the '702 Patent (Exhibit 1023, "Srikrishnan"). *Id.*

80. Srikrishnan describes "[a] process applicable to the production of monocrystalline films [that] improves on the Smart-Cut® process by using an etch stop layer in conjunction with the Smart-Cut® process." Exhibit 1023, Abstract. In its Background of the Invention section, Srikrishnan states: "Among the methods used for producing monocrystalline films are those used for producing silicon on insulator (SOI) substrates, where the aim is to produce a monocrystalline silicon film on a substrate that is electrically insulated from the film." *Id.*, 1:17–22.

81. Srikrishnan states: “The Smart-Cut® process has the following steps: 1) a device wafer is processed to have a device quality surface layer, an oxide layer is provided over the device layer, and a buried hydrogen-rich layer is implanted at a certain depth; 2) a ‘handle wafer’ with an oxide surface is provided; 3) the device wafer is flipped and the oxide surfaces are bonded; 4) the structure is annealed to form connecting voids from hydride formation; 5) the structure is fractured; and 6) the transferred device layer is CMP polished [chemical-mechanical polished] and cleaned.” *Id.*, 1:53–61; *see also* Exhibit 1014, 92–93; Exhibit 1015, 59–61; Exhibit 1009.

82. The Smart-Cut® process, and other similar processes like ELTRAN® and SiGen technologies, are consistent with the ’702 and ’941 Patents’ descriptions of the SOI layer, and stackable add-on layer. Specifically, in such processes, “a relatively thin, single crystal portion of a semiconductor wafer [is] cleaved and bonded to another previously fabricated wafer, or similar type of substrate.” ’702 Patent, 4:48–52; Exhibit 1023, 1:53–61.

83. Thus, in my opinion, a person of ordinary skill in the art would have understood that the terms “the stackable add-on layer [is]/[being] bonded” as recited in claims 1 and 13 require that the “stackable add-on layer” is wafer bonded to the recited layer of the substrate.

84. I have been asked to assume that the patent owner may argue that “the stackable add-on layer [is]/[being] bonded” encompasses any layer that is directly or indirectly adhered to the recited layer of the substrate. I have reviewed the intrinsic record of the ’702 patent, and it does not support such a construction. In my opinion, such a construction would be incorrect because it reads out the words “stackable” and “add-on” from the claim. Such a construction further is not supported by the intrinsic evidence I discuss above, including the ’702 and ’941 Patents’ discussion of “stackable add-on layer” and the ’941 Patent’s discussion of bonding the “stackable add-on layer” (formed on a separate wafer) to a base substrate. Regardless, as I explain below and in my opinion, the challenged claims of the ’702 patent would have been obvious in view of the prior art under either construction.

B. “SOI pillar” (Claims 14–17)

85. In my opinion, and based on the intrinsic record, “SOI pillar” requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology.

86. As to the term “pillar,” the ’702 Patent explains that “[i]n various embodiments of the present invention, a FLD [floating device] can be directly contacted by metal electrodes at top, bottom, and intermediate regions of the individual doped stack structures (i.e., pillar structures).” ’702 Patent, 5:21–22,

6:26–29. In my opinion, a person of ordinary skill in the art would have thus understood that a “pillar” as recited in claims 14–17 is a doped stack structure.

87. The '702 Patent and its incorporated '941 Patent each state: “The acronym ‘SOI’ generally refers to Silicon-on-Insulator.” '702 Patent, 4:45–46; '941 Patent, 6:4–5. Both patents then go on to discuss “SOI layer.” '702 Patent, 4:46–62; '941 Patent, 6:5–22. For example, the '702 Patent states:

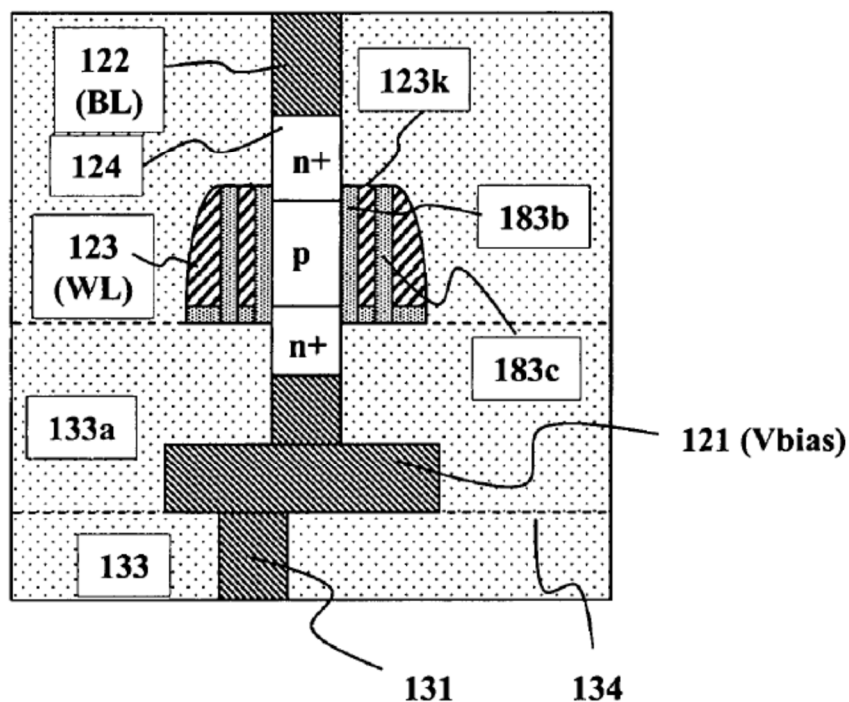
Unless otherwise noted, “SOI layer” is used herein to refer to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate. In this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.

'702 Patent, 4:46–57. Both the '702 Patent and the '941 Patent state that “[i]ndividual semiconductor structures may be formed by etching through portions of the doped stack to electrically isolate those structures,” and “[t]he spaces between such individual structures may be filled with dielectric material so as to re-form a layer without gaps or voids therein, and thereby provide for mechanical stability, and support for additional stacked layers.” '702 Patent, 4:62–5:3; '941 Patent, 6:22–28. According to the '702 Patent, “[i]n this way, the stackable add-on layer may provide a plurality of memory cells suitable for connections to an underlying substrate.” '702 Patent, 5:3–7. The '941 Patent states: “Because single crystalline

semiconductor layer 124 is formed by SOI technology, it is referred to herein simply as an SOI.” ’941 Patent, 6:44–46.

88. Further, in the embodiments, “SOI pillar” is labeled as 124. ’702 Patent, 8:9, 15, 21, 29–30, 46; 9:16–17, 55. As one example, I have reproduced Figure 23 of the ’702 Patent below:

Fig. 23



'702 Patent, Fig. 23.

89. “FIG. 23 shows a vertical memory cell with a vertical MOSFET in a stackable add-on layer, where the vertical memory has a floating gate 123k and a control gate 123.” *Id.*, 9:24–26. In Figure 23, the vertical MOSFET is made up of doped stack N+, P, N+ regions formed in SOI pillar 124.

90. In addition, as I discuss above, the '702 Patent incorporates by reference in its entirety the disclosure of the '941 Patent, and the '941 Patent provides more context as to the '702 Patent's pillar including the fabrication process for creating such pillars.

91. Thus, in my opinion, "SOI pillar," as recited in Challenged Claims 14–17 and supported by the intrinsic record, requires a pillar-shaped doped stack structure formed in a stackable add-on layer added using SOI technology.

92. I have been asked to assume that the patent owner may argue that "SOI pillar" encompasses any pillar-shaped structure with insulating material below it. I have reviewed the intrinsic record of the '702 patent, and it does not support such a construction. I have been specifically asked to consider whether the statement in the '702 and '941 Patents that "the substrate bonded to lower dielectric layer 151 is called base substrate 103" would support such a construction. '702 Patent, 5:37–38; '941 Patent, 7:14–15. It does not. This statement refers to bonding a dielectric layer to a base substrate in Figure 1, not bonding a "stackable add-on layer" to the substrate. In my opinion, such a construction would be incomplete because it would not provide meaning to "SOI" in "SOI pillar." Such a construction further is not supported by the intrinsic evidence I discuss above. Regardless, as I explain below and in my opinion, Challenged Claims 14–17 of the '702 patent would have been obvious in view of the prior art under either construction.

X. DETAILED EXPLANATION OF GROUNDS

A. Ground 1A: Obviousness over Lee (Claims 13–17)

93. As I discuss above, I have been asked to assume that Patent Owner may argue “the stackable add-on layer being bonded” encompasses any type of layer, so long as that layer is directly or indirectly adhered to the “dielectric layer.” For claims 14–17, I have similarly been asked to assume that Patent Owner may argue that “SOI pillar” encompasses any pillar-shaped structure with insulating material below it. In my opinion, such constructions are not supported by the intrinsic evidence, and are not consistent with how a person of ordinary skill in the art would have understood “the stackable add-on layer being bonded” and “SOI pillar” in the context of the Challenged Claims. Nevertheless, under these constructions, claims 13–17 would have been obvious over Lee for the reasons I discuss below.

1. Lee

94. Lee is directed to a “three dimensional array of charge storage devices which includes a plurality of device levels.” Exhibit 1007, Abstract. Lee’s three-dimensional array is disposed above a “monocrystalline semiconductor substrate” having “driver (i.e., peripheral) circuitry [] formed in the substrate under the array.” *Id.*, ¶110. Such an embodiment is depicted in Lee’s Figure 35, which I have annotated and reproduced below:

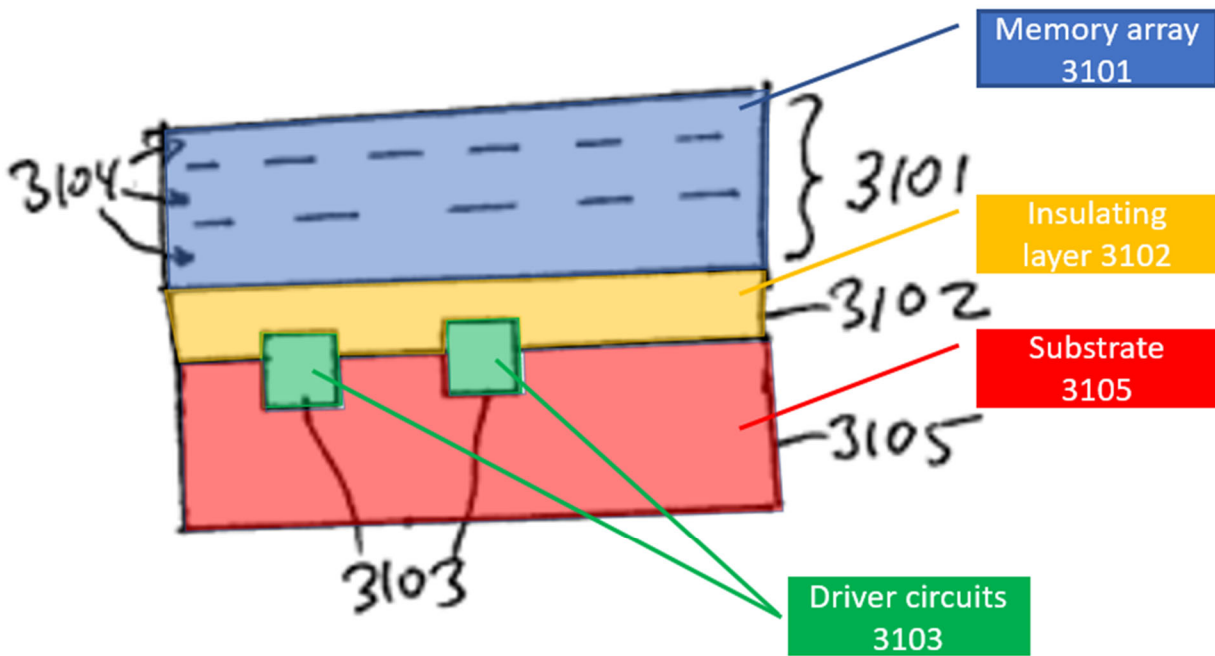


FIGURE 35

95. Figure 35 depicts substrate 3105 (red) having driver circuits 3103 (green) therein, insulator layer 3102 (yellow) above substrate 3105, and array 3101 of device levels 3104 (blue) of “charge storage logic or memory devices” (not shown) above insulator layer 3102. *Id.*, ¶111. Figure 35 is agnostic as to the particular type or structure of the memory devices in the levels 3104 of array 3101, which it depicts as a rectangular box (i.e., a cross-section showing levels in the array but not any of the details of the devices in each level).

96. Lee explains that the “charge storage devices of the array may be any type of semiconductor devices which store charge,” and provides specific embodiments which disclose charge storage devices “formed in various

configurations, such as a pillar TFT EEPROM [thin film transistor electrically erasable programmable read only memory].” Exhibit 1007, ¶¶13, 113. Lee further explains that “[i]n the preferred embodiments of the present invention described in detail below, the charge storage devices are formed in various configurations, such as a pillar TFT EEPROM ... and various other configurations,” and then discusses a “first set of embodiments describ[ing] various pillar devices,” including those in Figures 1A, 1B, 2, 7, and 25A. *Id.*, ¶¶113, 117–169 (describing the “Pillar Devices” as a first set of embodiments with Figure 1A described in paragraphs 122–124, Figure 1B described in paragraph 125, Figure 2 described in paragraphs 126–131, Figure 7 described in paragraph 138, and Figure 25A described in paragraphs 165–166).

97. I have reproduced Lee’s Figure 1A below:

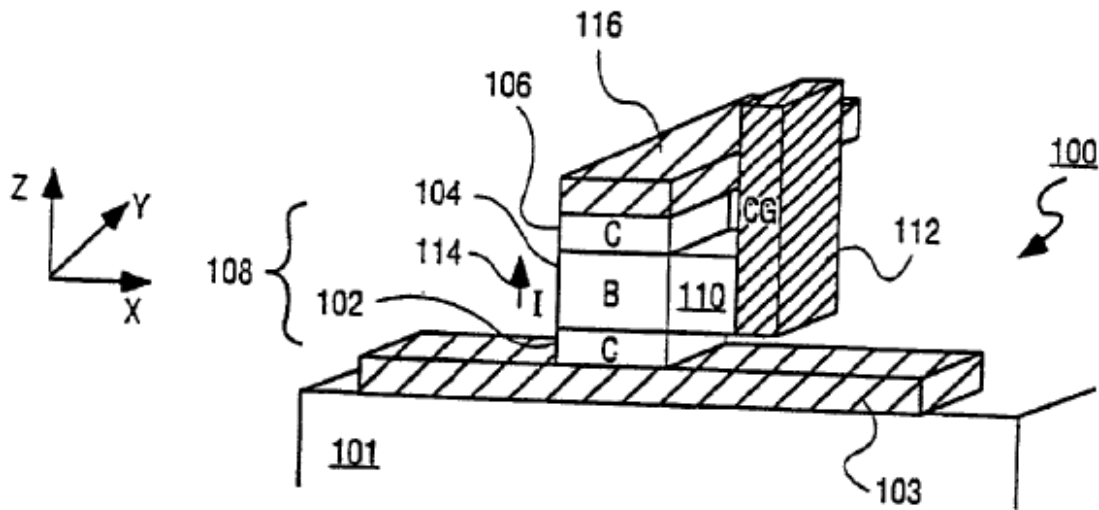


FIG. 1A

98. Figure 1A shows “[p]illar memory device 100” having “a first contact region 102,” a “semiconductor body 104 [] formed directly on the first contact region 102,” and “a second contact region 106 [] formed directly on the body 104,” wherein “[t]he first contact region 102, the body 104, and the second contact (source/drain) region 106 are each vertically aligned with one another to form a pillar 108.” *Id.*, ¶122. Lee further explains “current 114 flows vertically (z) (or perpendicular) with respect to the plane (x-y) of the substrate 101 above which pillar memory device is formed.” *Id.*, ¶124.

99. I have reproduced Lee’s Figure 1B below:

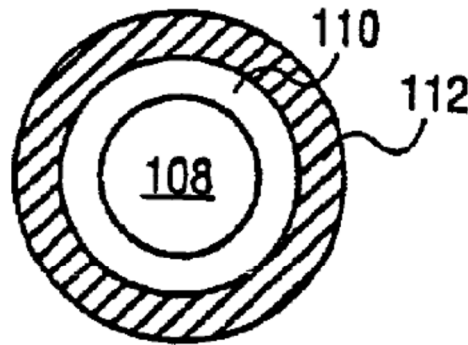


FIG. 1B

100. Figure 1B (which is a top view) shows a variation of the structure in Figure 1A (which is a side view), where instead of charge storage medium 110 and control gate 112 “formed on only one side or surface of pillar 108,” “pillar 108 is surrounded by a single charge storage member 110 and a single control gate 112.” *Id.*, ¶125.

101. I have reproduced Lee’s Figures 2 and 7 below:

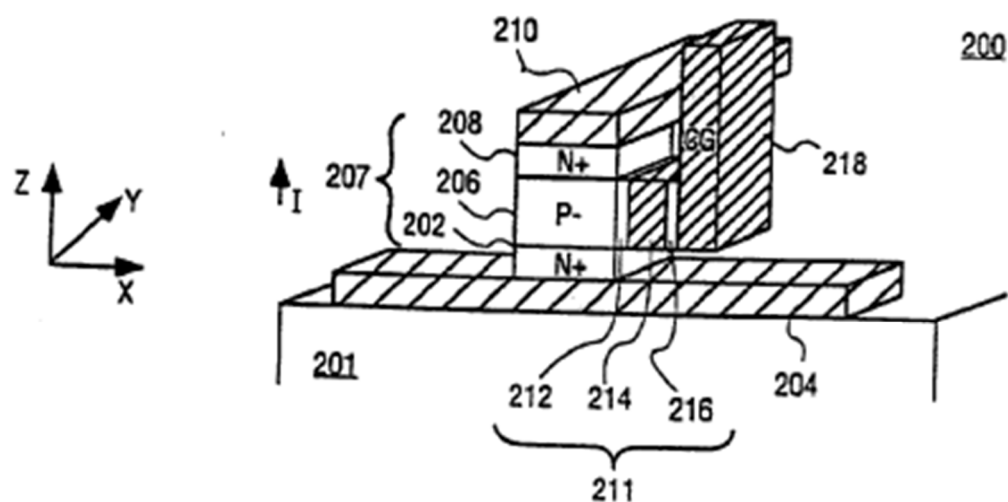


FIG. 2

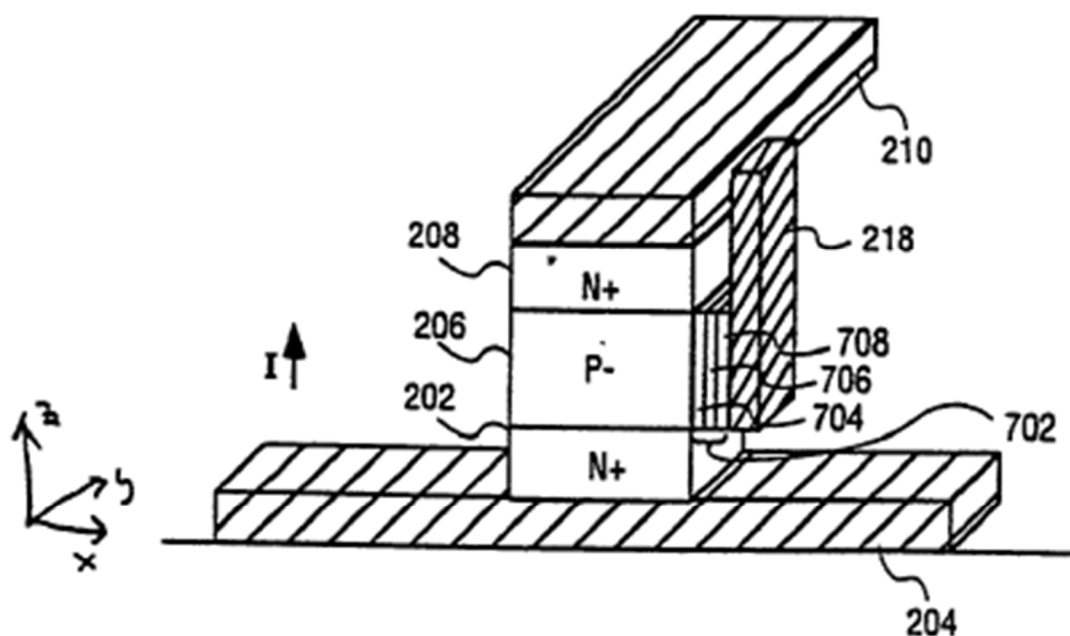


FIG. 7

102. Similar to Figure 1A, each of Figures 2 and 7 show memory devices in which channel 206 is stacked above source 202 and below drain 208, such that

current from drain to source runs perpendicularly with respect to the surface of the substrate. See Exhibit 1007, ¶¶126, 138.

103. Lee additionally discloses a method of integrating its pillar memory device into “a multilevel array of storage cells,” i.e., array 3101 of Figure 35. *Id.*, ¶147. As Lee describes with reference to Figure 13A, the process begins by providing a “substrate [] on which the multilevel array of storage devices is to be formed,” the substrate being topped with a planarized insulating layer or passivation layer. *Id.* Lee then describes that “a first conductor layer 1308” and “stack 1310 of films from which a first level of pillars is to be fabricated is blanket deposited” as shown in Figure 13A, which I have annotated and reproduced below.

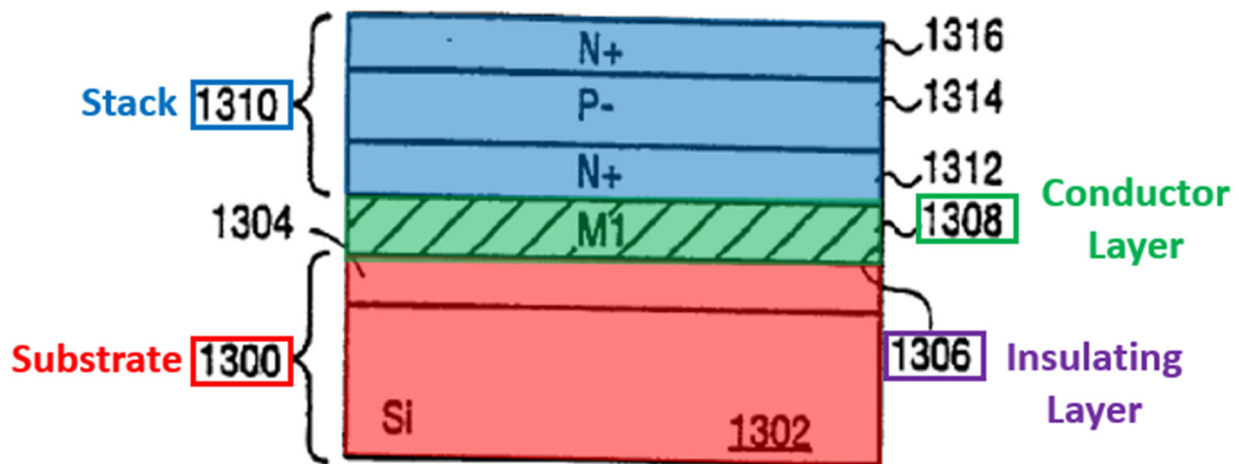


FIG. 13A

104. The conductor layer 1308 and stack 1310 are then “patterned utilizing well-known photolithography and etching techniques to form a plurality of pillar strips 1318” as shown in Figure 14A (cross section view) and Figure 14B (top view), which I have annotated and reproduced below. *Id.*, ¶149.

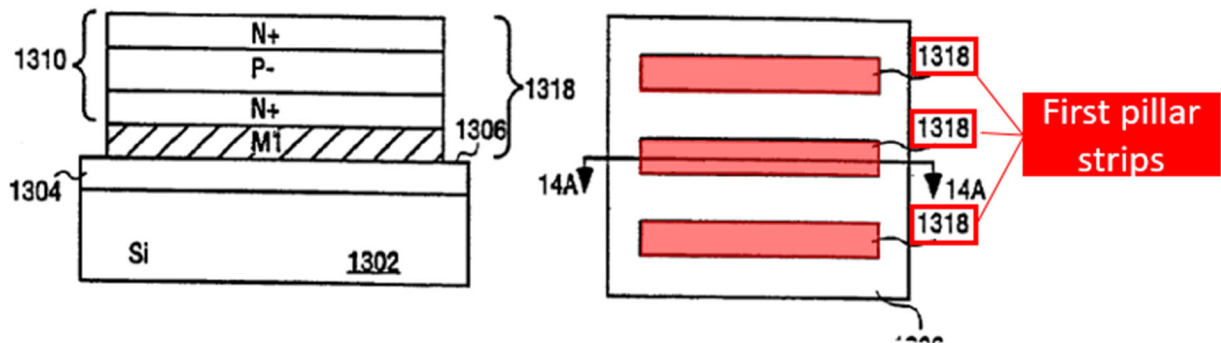


FIG. 14A

FIG. 14B

105. Lee then describes depositing various layers to form a floating gate and control gate surrounding the pillar strips 1318. *Id.*, ¶151. Afterwards, to form a second level of memory devices, Lee discloses blanket depositing a second conductor layer 1336 and film stack 1338 over and in contact with the N+ region of the first memory device layer as well as over and on ILD 1334, as shown in annotated Figure 20A below. *Id.*, ¶157–158.

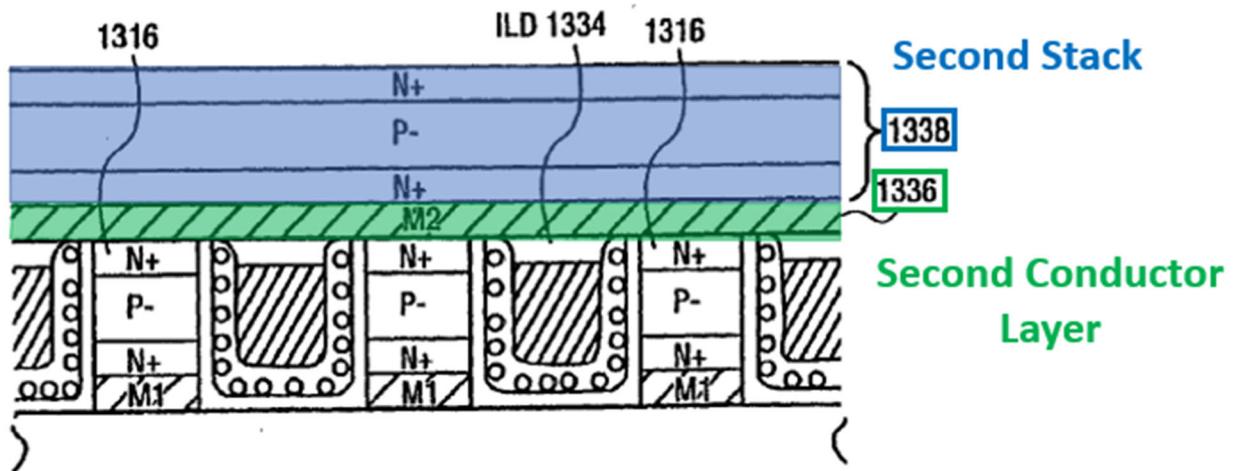


FIG. 20A

106. Similar to the first level of memory devices, the second level of memory devices is then patterned to form a plurality of second pillar strips 1340 as shown in Figures 21A (cross section view) and 21B (top view), which I have annotated and reproduced below. *Id.*, ¶159.

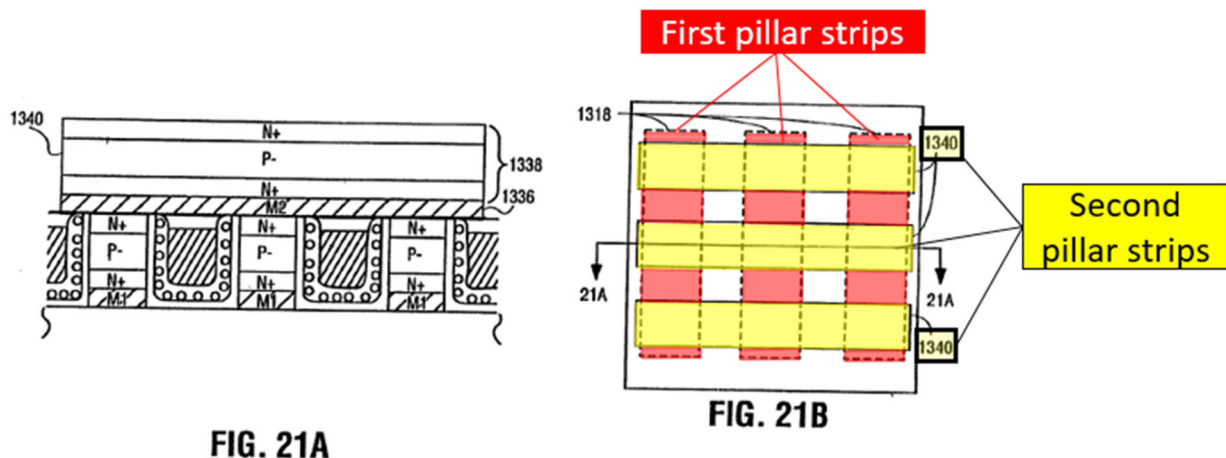
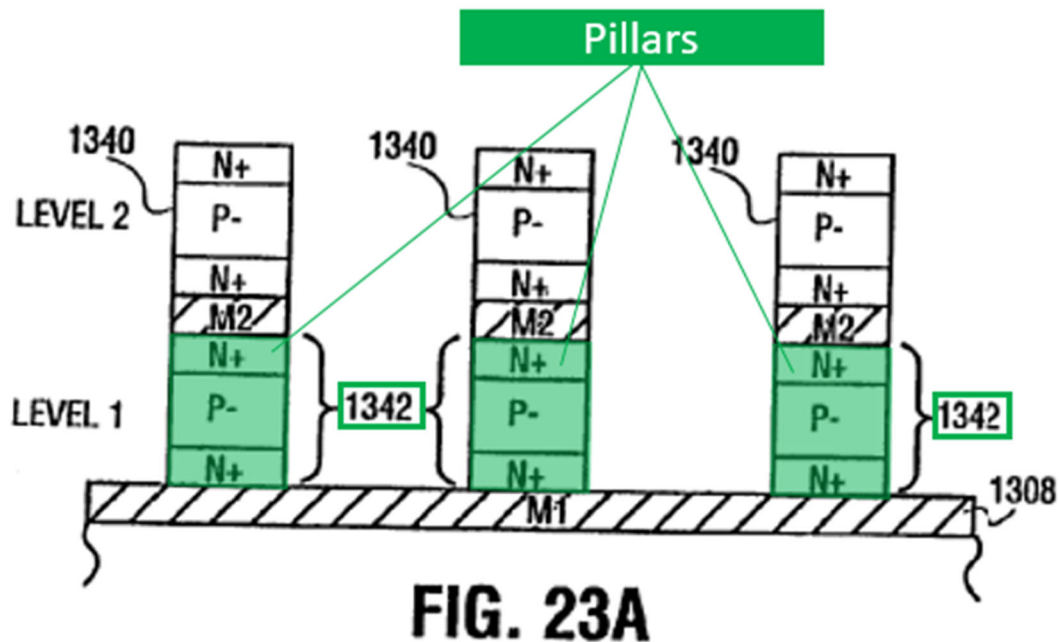


FIG. 21A

FIG. 21B

107. Lee then describes conducting further etching to remove the portions of the first pillar strips 1318 not covered or masked by second pillar strips 1340 such

that “a first level of square or rectangular pillars 1342 have been formed,” as shown in Fig. 23A, which I have annotated and reproduced below. *Id.*, ¶161.



108. Next, as shown in FIG. 24, which I have annotated and reproduced below, “a tunnel dielectric 1344, a nanocrystal floating gate material 1346, and a control gate dielectric 1348 are each successively blanket deposited over substrate 1300 to form a tunnel dielectric/floating gate/control gate on the sidewalls of pillar devices 1342 as well as along the sidewalls of the second pillar strip 1340.” *Id.*, ¶163.

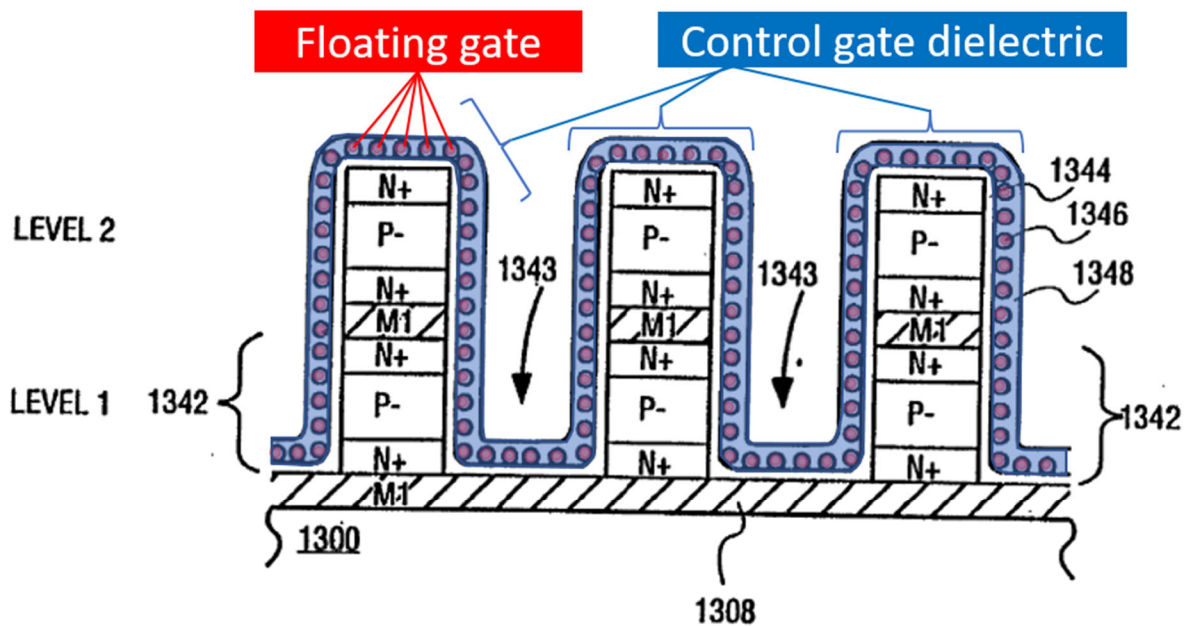


FIG. 24

109. Then, “as shown in FIG. 25A, a control gate 1350 is formed between second pillar strip 1340 as well as in the gaps 1343 between pillars 1342.” *Id.*, ¶165.

I have annotated and reproduced Figure 25A below.

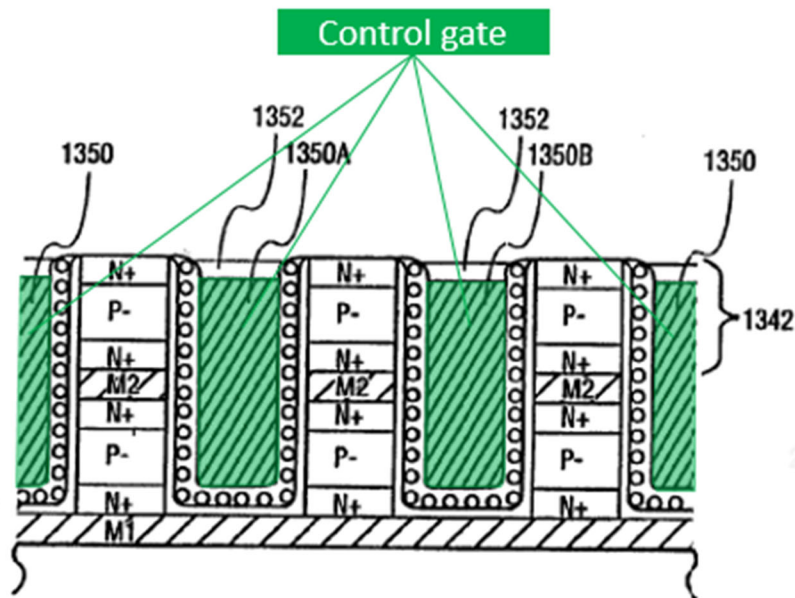


FIG. 25A

110. Although Lee discloses that, in the step shown in Figure 25A, only the memory cells in Level 1 have been etched to form “square or rectangular pillars” and deposited with the appropriate gate and gate insulator materials on all sides, while Level 2 continues to include pillar strips, Lee continues on to explain the iterative process through which subsequent levels (including Level 2) are similarly etched from pillar strips to create fully-formed pillars. *Id.*, ¶166–167 (explaining that this process may be “repeated again to complete the fabrication of memory devices on the second level,” i.e., “to pattern the second pillar strips 1340 into a plurality of second pillars [] on a second level and to form a second pair of control gates [] adjacent to the second pillars”). In this respect, “[e]ach control gate 1350 will be

shared with the subsequently formed pillar memory device position[ed] vertically above, in Level 2.” *Id.*, ¶166.

2. Claim 13

111. As I discuss in detail below, Lee renders obvious claim 13 under PO’s apparent constructions because Lee’s Figure 35 in combination with any of Figures 1A, 1B, 2, 7, or 25A⁵ teaches the limitations of independent claim 13 and a POSITA would have been motivated to combine the relied upon teachings.

a. 13[pre]: “A semiconductor memory structure, comprising:”

112. In my opinion, Lee discloses or suggests a “semiconductor memory structure.” Specifically, Lee discloses a three-dimensional memory array formed on a semiconductor substrate, as shown in Fig. 35 below. Exhibit 1007, ¶111 (“an array of charge storage logic or *memory* devices 3101”), ¶113 (“charge storage devices of the array may be any type of *semiconductor* devices which store charge”); *see also*

⁵ Any one of the following combinations renders claim 13 obvious: Figure 35 in combination with (1) Figure 1A, (2) Figure 1B, (3) Figure 2, (4) Figure 7, or (5) Figure 25A. I address all five combinations for claim 13 because dependent claims 14–17 depend from claim 13 and further recite specific memory cell structures, as taught in Figures 1A, 1B, 2, 7 and/or 25A.

¶3 (“The present invention relates to semiconductor devices in general and to a three dimensional TFT array in particular.”), ¶18 (“According to one preferred embodiment of the present invention, a semiconductor device comprises a monolithic three dimensional array of charge storage devices comprising a plurality of device levels.”); ¶24 (“Another preferred embodiment of the present invention provides a nonvolatile stackable pillar memory device and its method of fabrication.”).

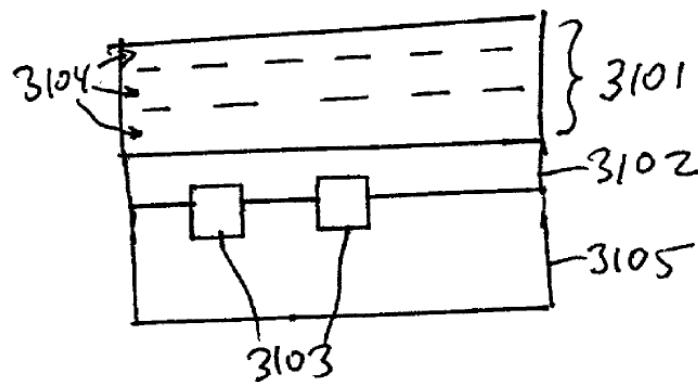


FIGURE 35

113. For the reasons I discuss above, and to the extent it is limiting, in my opinion, Lee discloses or suggests 13[pre].

b. 13[a]: “a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices”

114. In my opinion, Lee discloses or suggests 13[a], which recites (1) “a substrate having electrical devices formed therein,” and (2) “a dielectric layer disposed above the electrical devices.”

115. I note that the '702 Patent defines the term “device” as “active and passive circuit elements,” including, but not limited to “FETs (n-channel and p-channel), Thyristor[s], capacitors, varactors, floating gates, charge trap layers, diodes, and resistors.” '702 Patent, 4:28–34. In addition, the incorporated '941 Patent defines “device” as “one or more circuit elements that have characteristics that are voltage variant,” including, but not limited to, “FETs (n-channel and p-channel), diodes, and varactors.” '941Pat, 5:51–54, 59–60.

116. Regarding (1) “a substrate having electrical devices formed therein,” Lee’s Figure 35, which I have annotated below, shows “driver circuits 3103” (green) “disposed in” substrate 3105 (red). Exhibit 1007, ¶111; *see also id.*, ¶110 (“[A]t least part, and preferably all, the driver (i.e., peripheral) circuitry is formed in the substrate under the array.”). Lee further discloses that the driver circuitry can include “sense amps and charge pumps” in the form of “CMOS [complementary metal oxide semiconductor] or other transistors.” *Id.*, ¶¶110–111, 208.

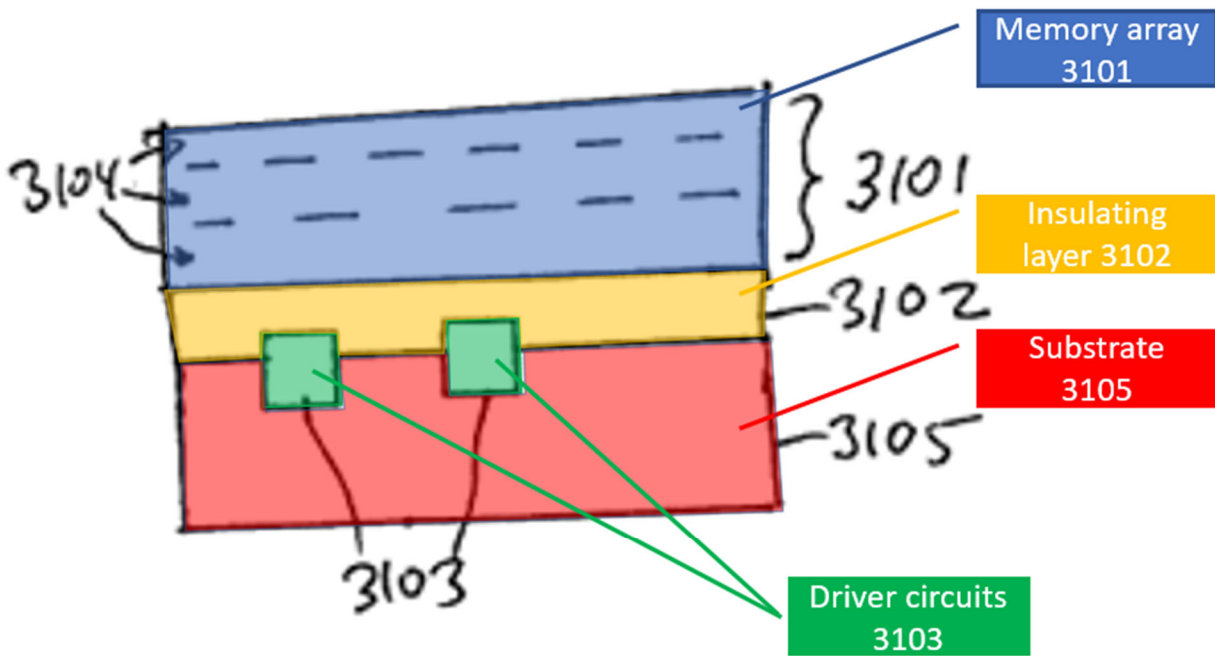


FIGURE 35

117. In my opinion, a person of ordinary skill in the art would have understood that the “sense amps” or “charge pumps,” formed of “CMOS and other transistors,” are “devices” as described in the ’702 Patent. Specifically, in my opinion, a person of ordinary skill in the art would have understood that these circuit elements (transistors) described by Lee are “active circuit elements,” i.e., having power gain. In contrast, passive circuit elements such as resistors, capacitors, and inductors do not have power gain. Further, a POSITA would have known that “CMOS or other transistors” include types of “FETs,” or MOSFETs, which the ’702 Patent and the ’941 Patent provide as an example of a “device.” ’702 Patent, 4:28–

34; '941 Patent, 5:51–54, 59–60. As such, Lee teaches “a substrate having electrical devices formed therein.”

118. Regarding (2) “a dielectric layer disposed above the electrical devices,” in Figure 35 (above), Lee discloses “an interlayer insulating layer 3102” (yellow) sandwiched between memory array 3101 (blue) and substrate 3105 (red). Exhibit 1007, ¶111. Thus, insulating layer 3102 is “disposed above the electrical devices.” A POSITA would have understood that an insulating layer, in the context of semiconductor structures and electrical circuits, does not conduct electricity and thus an insulating layer is a “dielectric layer.” For example, the 2000 IEEE Dictionary defines “insulator” as “a device intended to ... insulate ... conductors or equipment from ground or from other conductors or equipment” or “[a] device made of a material in which electrons or ions cannot be moved easily, hence preventing the flow of electric current.” (Exhibit 1022, 568).

119. As such, Lee discloses or suggests its insulating layer 3102 (“a dielectric layer”) is above (“disposed above”) driver circuits 3103, such as CMOS or other transistors, disposed in substrate 3105 (“the electrical devices”).

120. In my opinion, Lee discloses or suggests limitation 13[a].

c. 13[b]: “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells”

121. In my opinion, Lee discloses or suggests limitation 13[b] to the extent that a “stackable add-on layer” encompasses any type of layer that is directly or indirectly adhered to the “dielectric layer.” Specifically, bottom level 3104 of Lee’s array 3101 as shown in Figure 35 (“stackable add-on layer”) containing two or more of Lee’s pillar memory devices as shown in any one of Figures 1A, 1B, 2, 7, or 25A (“having a plurality of vertically oriented semiconductor memory cells”) teaches limitation 13[b].

122. As an initial matter, I note that “stackable add-on layer” is not so broad, and further discuss in my opinions below how 13[b] is taught by the prior art under the proper construction.

123. Lee’s Figure 35, which I have annotated and reproduced below, shows device levels 3104 above insulator layer 3102. Exhibit 1007, ¶111. In my opinion, the bottom-most level 3104 of array 3101 teaches a “stackable add-on layer” under PO’s apparent construction.

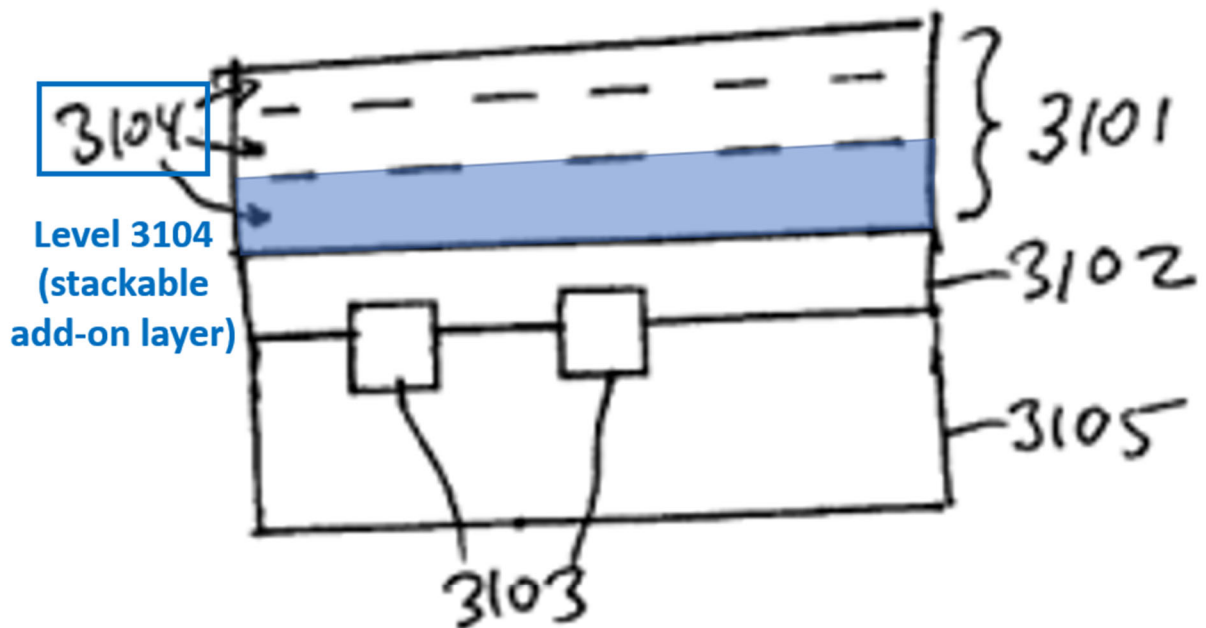


FIGURE 35

124. Figure 35 depicts level 3104 as a rectangular box (as shown above), and is agnostic as to the particular type or structure of the memory cells in it. Lee, however, explains that the “charge storage devices of the array may be any type of semiconductor devices which store charge, such as EPROMs or EEPROMs.” *Id.*, ¶113.⁶ In my opinion, a person of ordinary skill in the art would have understood

⁶ See, e.g., Exhibit 1025, U.S. Pat. No. 5,615,148, 1:6–8 (“The present invention relates to an electrically erasable and reprogrammable nonvolatile semiconductor memory (EEPROM).”); Exhibit 1026, U.S. Pat. No. 5,544,103, 1:17–20 (“In general,

each level 3104 contains two or more memory cells. For example, Exhibit 1007, ¶¶26 (“each level comprising an array of TFT EEPROMs”), 107, Fig. 25A.

125. Lee further explains that “[i]n the preferred embodiments of the present invention described in detail below, the charge storage devices are formed in various configurations, such as a pillar TFT EEPROM ... and various other configurations,” and then proceeds to discuss a “first set of embodiments describ[ing] various pillar devices,” including those in Figures 1A, 2, 7, and 25A. *Id.*, ¶¶113, 117–169 (describing the “Pillar Devices” as a first set of embodiments with Figure 1A described in paragraphs 122–124, Figure 1B in paragraph 125, Figure 2 described in paragraphs 126–131, Figure 7 described in paragraph 138, and Figure 25A described in paragraphs 165–166). I have annotated and reproduced figures 1A, 2, 7, and 25A below:

nonvolatile semiconductor memory devices can be classified into two groups: electrically programmable read-only memories (EPROMs) and electrically erasable and programmable read-only memories (EEPROMs).”); Exhibit 1027, U.S. Pat. No. 6,381,173, 2:50–52 (“an EEPROM memory array 25 that belongs to a nonvolatile memory 100”)

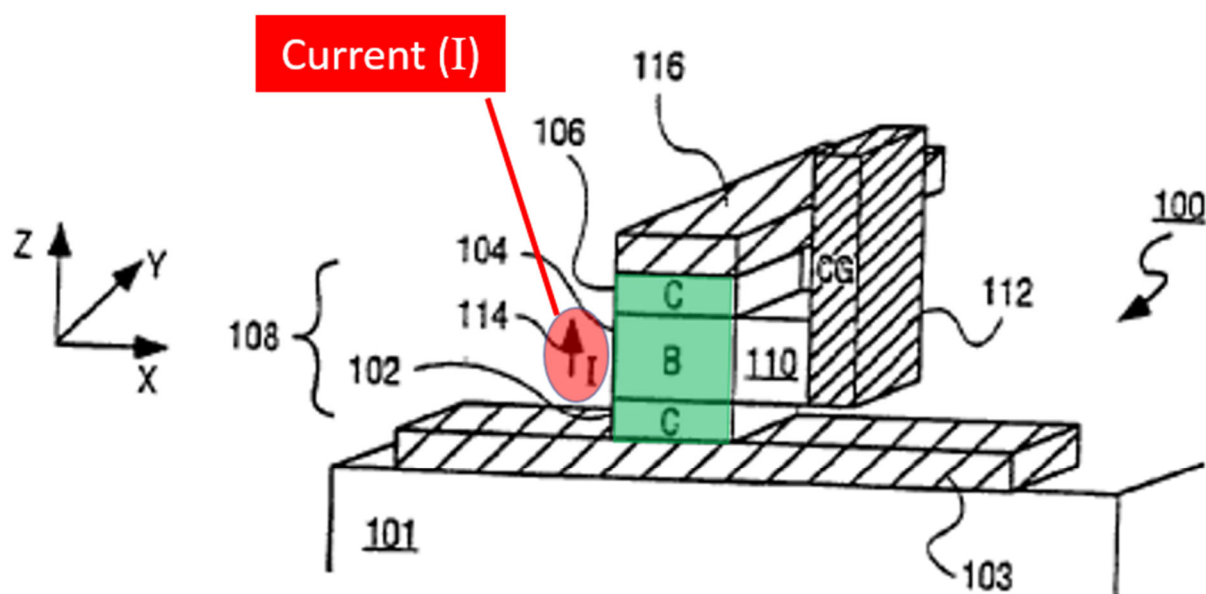


FIG. 1A

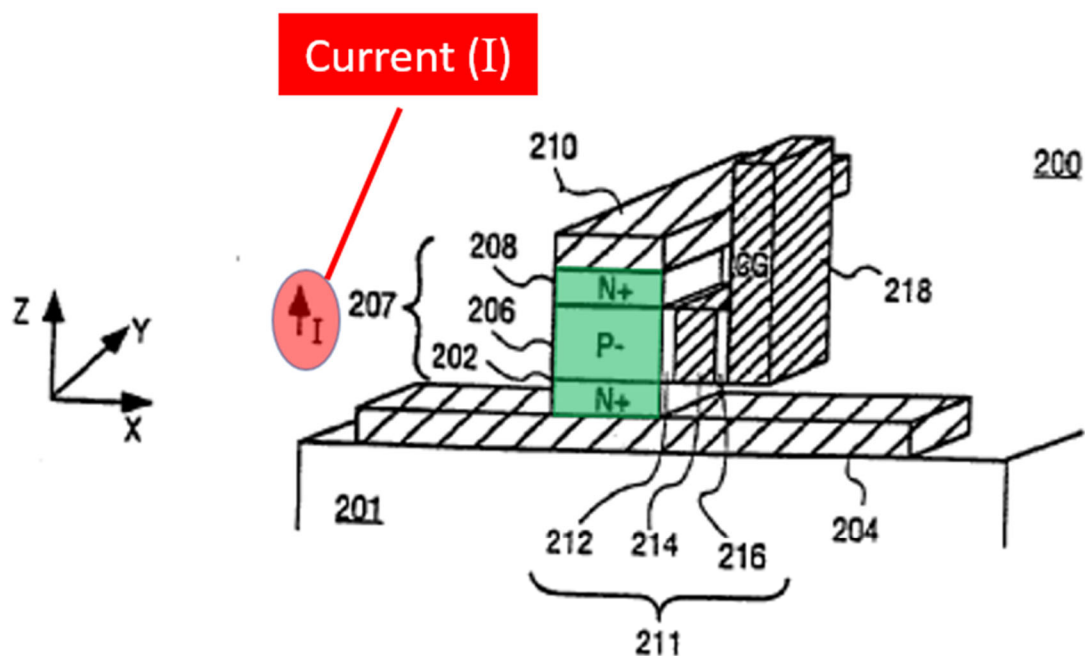


FIG. 2

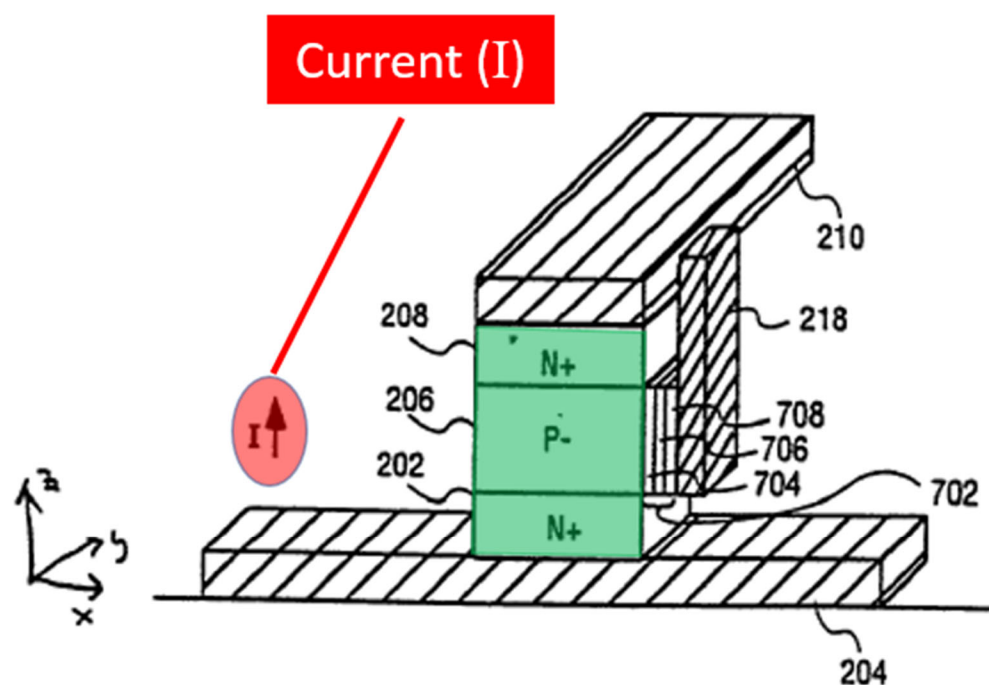


FIG. 7

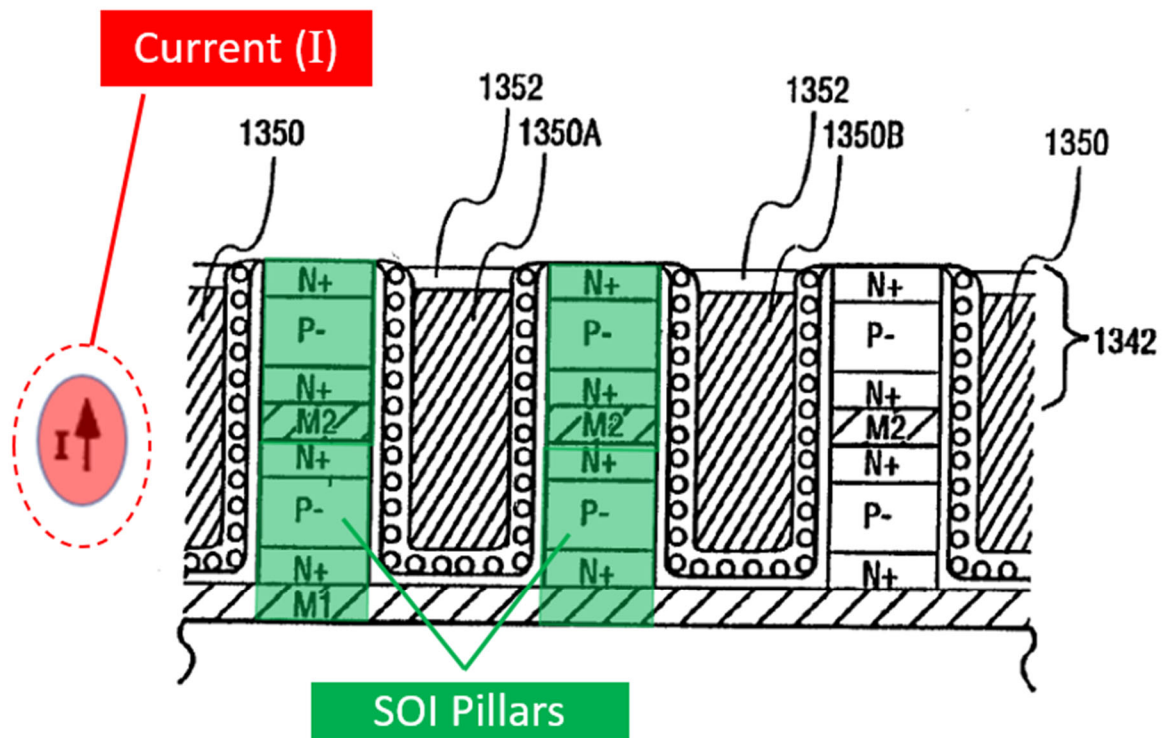


FIG. 25A

126. As I show in the annotated figures above, each of Figures 1A, 2, 7, and 25A depicts a memory cell with a transistor in which the source, channel, and drain (green in each figure) are arranged perpendicular with respect to the substrate. *Id.*, ¶¶24, 26, 119, 122–124 (Fig. 1A has the drain (106), channel (104), and source (102) stacked vertically and perpendicularly to the substrate), 126 (each of Figures 2 and 7 has channel 206 stacked above source 202 and below drain 208), 165 (Figure 25A's pillar 1342 comprises N+/P-/N+ stack as in Figure 2, i.e., drain/channel/source). In addition, Figs. 1A, 2, and 7 show current (I) (red) running vertically through the transistor and perpendicular to the substrate, and I have

annotated Fig. 25A in a consistent manner. *Id.*, Figs. 1A, 2, 7, 25A, ¶119, 124 (in Fig. 1A, “current 114 flows vertically (z) (or perpendicular) with respect to the plane (x-y) of the substrate 101 above which pillar memory device is formed”), 131.

127. I have also annotated and reproduced Figure 1B below, which is a top view implementation of Figure 1A which is shown in side view:

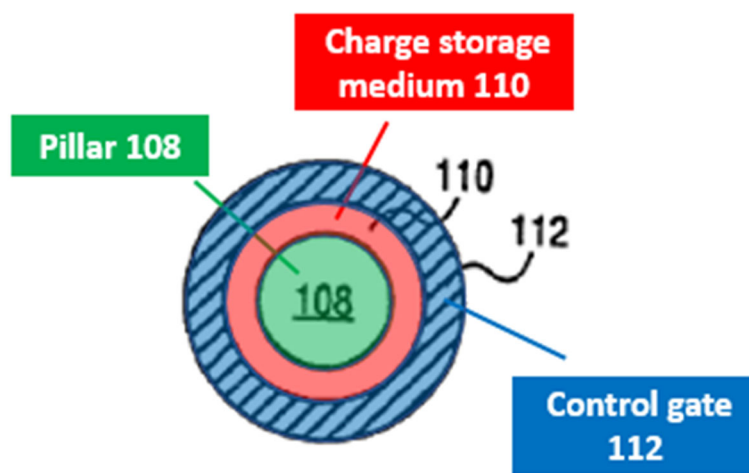


FIG. 1B

128. Figure 1B shows a variation of the structure in Figure 1A, where instead of charge storage medium 110 and control gate 112 “formed on only one side or surface of pillar 108,” “pillar 108 is surrounded by a single charge storage member 110 and a single control gate 112.” Exhibit 1007, ¶125. Based on this description, in my opinion, a POSITA would have understood that Figure 1B shows a top view of an implementation of Figure 1A, and that in vertical cross-section, pillar 108 in

Figure 1B would have the same drain (106), channel (104), and source (102) as shown in Figure 1A, stacked vertically and perpendicularly to the substrate.

129. The '702 Patent states: “The term ‘vertical,’ as used herein, means substantially perpendicular to a major surface of a substrate, such as, for example, a semiconductor wafer.” '702 Patent, 4:6–8. As described above, each of Lee’s Figure 1A, 1B, 2, 7, and 25A teach a memory cell with a transistor in which the source, drain, and channel regions are arranged perpendicular to the substrate (as shown in green with the current flow in red in the annotated figures above), and thus each of Lee’s Figure 1A, 1B, 2, 7, and 25A teaches a “vertically-oriented memory cell.” I note that the memory cells in each of Lee’s Figure 1A, 1B, 2, 7, and 25A are “vertically-oriented” in the same way as the memory cells of the '702 Patent’s Figures 23 and 25. '702 Patent, 9:24–50.

130. In my opinion, a person of ordinary skill in the art would have been motivated to use any of Lee’s memory cell structures in Figures 1A, 1B, 2, 7, or 25A as the memory cells in Figure 35’s bottom level 3104, with multiples of each such cell included in that level. Exhibit 1007, ¶111. Lee states that “[i]n the preferred embodiments of the present invention described in detail below, the charge storage devices are formed in various configurations, such as a pillar TFT EEPROM ... and various other configurations”; Figures 1A, 1B, 2, 7, and 25A are then described in detail. EX1007, ¶¶113, 118–169. From this express disclosure in Lee, in my opinion,

a person of ordinary skill in the art would have understood that the memory cells shown in Figures 1A, 1B, 2, 7, or 25A of Lee are “type[s] of semiconductor devices which store charge” as Lee describes its array’s memory cells, and so would have been motivated to use them in the array of Figure 35. *Id.*, ¶¶113, 123, 125, 127, 138, 166.

131. As described in Lee’s paragraph 122, the memory device of Figure 1A stores charge in the charge storage medium 110. *Id.*, ¶122–123. Lee makes clear that Figure 1B is merely an alternative arrangement of the components described in Figure 1A. *Id.*, ¶125. Also, as described in paragraph 127, the memory device of Figure 2 stores charge in floating gate 214. *Id.*, ¶127. As described in paragraph 138, the memory device of Figure 7 stores charge in the oxide-nitride-oxide layers 704, 706, and 708. *Id.*, ¶138. And finally, as described in paragraph 166, pillars 1342 in Figure 25A have charge storage regions. *Id.*, ¶166. In these combinations, Lee’s level 3104 with such memory cells would be “stackable.” *Id.*, ¶¶24, 108–109, 122, 124.

132. In addition, in my opinion, a person of ordinary skill in the art would have been motivated to use the memory cell of any of Figures 1A, 1B, 2, 7, or 25A with Figure 35 because using one in place of another would have amounted to nothing more than simple substitution of a known memory cell, as contemplated by Lee’s teachings. Exhibit 1007, ¶¶113, 114, 117. In my opinion, a person of ordinary

skill in the art would have further recognized using the memory cells in any of Figures 1A, 1B, 2, 7, or 25A in Figure 35's level 3104 would allow for each memory cell to take up less lateral surface area (because of the vertical orientation of the transistor in each), furthering Lee's stated goal of increasing density of memory devices. *Id.*, ¶¶17, 106, 107, 110, 113.

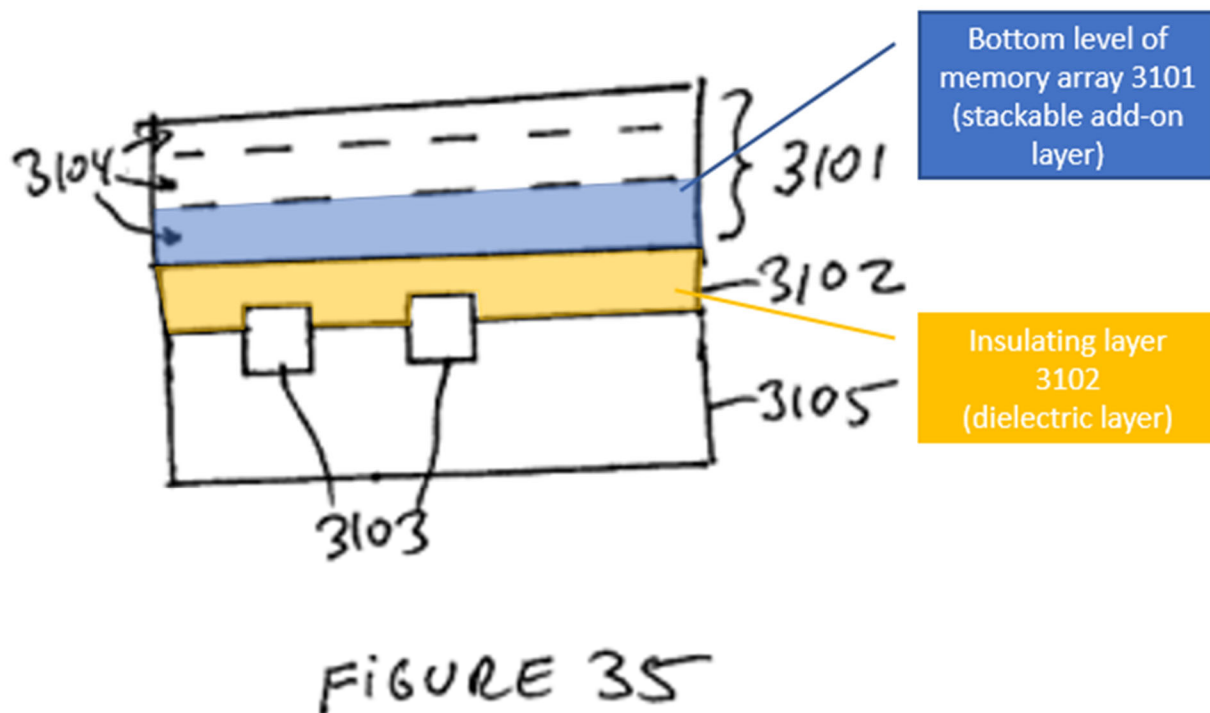
133. Lee gives an express motivation for the proposed combinations when Lee explains that “by creating a memory device with a ‘vertical’ read current path, the pillar memory cell of the present invention can be easily stacked in a three dimensional array with source/drain conductors 103 and 116 running parallel or perpendicular to each other and parallel to the plane of the substrate 101 without requiring the use of vertical interconnect strategies for the source and drain connection.” Exhibit 1007, ¶124. Although this passage refers to Figure 1A, the same principle applies equally to Figures 1B, 2, 7, or 25A with predictable results based on the foregoing discussion. *Id.*, ¶¶119, 131.

134. Further, in my opinion, a person of ordinary skill in the art would have had a reasonable expectation of success in making this combination because Lee expressly contemplates using the memory devices of Figures 1A, 1B, 2, 7, or 25A in the array of Figure 35 and doing so would have obtained predictable results. Exhibit 1007, ¶¶113, 114.

d. 13[c]: “the stackable add-on layer being bonded to the dielectric layer”

135. As I discuss above, Patent Owner may argue that “the stackable add-on layer being bonded” encompasses any type of layer that is directly or indirectly adhered to the “dielectric layer.” In my opinion, such a construction is incorrect because it is inconsistent with the intrinsic evidence. Nevertheless, Lee discloses or suggests this limitation under such a construction.

136. As I discuss above in Section X.A.2.c, bottom-most level 3104 (as shown in Figure 35, which I have annotated and reproduced below) teaches a “stackable add-on layer,” and under PO’s apparent construction, that layer is adhered to insulating layer 3102 (“the dielectric layer”).



137. This figure shows that bottom level 3104 of array 3101 (“stackable add-on layer”) is adhered to interlayer insulating layer 3102 (“dielectric layer”).

e. 13[d]: “wherein the memory cells are nonvolatile memory cells having at least one transistor”

138. In my opinion, Lee discloses or suggests limitation 13[d]. As I explained above in Section X.A.2.c, Figures 1A, 1B, 2, 7, and 25A each disclose a memory cell with a transistor, and my opinion is that a person of ordinary skill in the art would have been motivated to include any of those memory cells as the memory cells of level 3104 in Figure 35. For the same reasons, in my opinion, Lee teaches “the memory cells...having at least one transistor.”

139. Each of Figures 1A, 1B, 2, 7, and 25A also disclose nonvolatile memory cells. Exhibit 1007, ¶¶6 (“electrically erasable *nonvolatile* memories such as...EEPROMs”) (emphasis added), 113 (“pillar TFT EEPROM” “described in detail below”). Lee specifically describes Figure 1A as “a three terminal *nonvolatile* stackable pillar memory device,” and Figure 1B as a modification of Figure 1A. Exhibit 1007, ¶¶122, 125 (emphasis added). Although the text associated with Figures 2, 7, and 25A does not explicitly call those structures “nonvolatile,” in my opinion, a POSITA would have understood them to be nonvolatile because they each comprise a floating gate (Figures 2 and 25A) or a charge-trapping dielectric film (Figure 7) (Exhibit 1007, ¶¶127, 138, 165), which ensure that stored information is

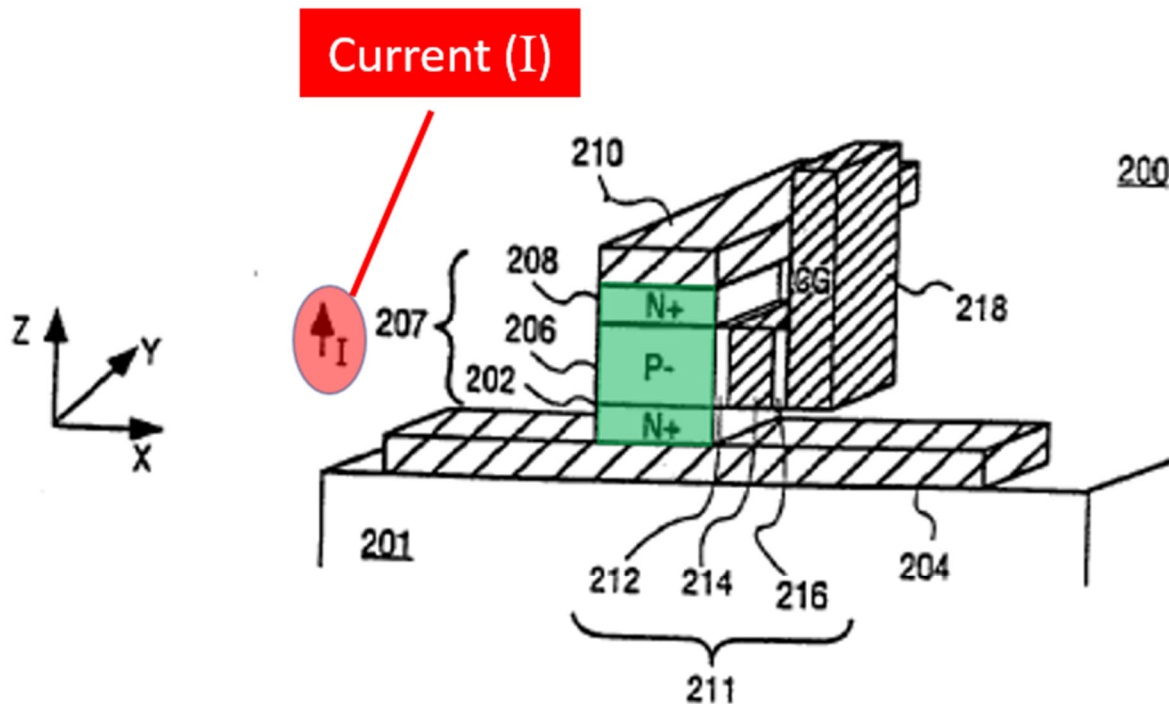
retained even when power is removed (each is designed to store charge as described in Section X.A.2.c above).

3. Claim 14: “The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.”

140. As I discuss above, Patent Owner may argue “SOI pillar” encompasses any pillar-shaped structure with insulating material below it. In my opinion, such a construction is incorrect because it is inconsistent with the intrinsic evidence. Nevertheless, Lee discloses or suggests this limitation under such a construction.

141. In my opinion, Lee discloses or suggests claim 14’s additional limitations, which recite (1) “a vertical transistor,” (2) the vertical transistor has “a floating gate and a control gate,” and (3) the floating gate and control gate are “on a SOI pillar.”

142. As to (1), for a “vertical transistor,” in Section X.A.2.c, I describe how Lee’s Figure 2 (as I have reproduced and annotated below) depicts a “vertical transistor” (channel 206 stacked above source 202 and below drain 208 and direction of current flow I).



143. As to (2), the vertical transistor in Lee's Figure 2 also has "a floating gate and a control gate," namely, floating gate 214 ("floating gate") and control gate 218 ("control gate"). *Id.*, ¶¶126–127.

144. As to (3), the floating gate and control gate are on pillar 207 ("on a SOI pillar" under PO's apparent construction). More specifically, Figure 2 shows "a charge storage medium 211 comprising a tunnel dielectric 212, a floating gate 214, and a control gate dielectric 216." Exhibit 1007, ¶127. Lee explains that tunnel dielectric 212 "is formed adjacent to and in direct contact with P type silicon body 206 [of pillar 207]," "floating gate 214 is formed adjacent to and in direct contact

with tunnel dielectric 212,” “control gate dielectric 216 is formed adjacent to and in direct contact with floating gate 214,” and “control gate 218 is formed adjacent to and in direct contact with control gate dielectric 216.” *Id.*, ¶¶126, 127. In my opinion, Lee’s Figure 2 teaches floating gate 214 and control gate 218 “on” pillar 207 in the same way that the ’702 Patent teaches floating gate 123k and control gate 123 are “on” SOI pillar 124 in Figure 23. As I discuss in Section X.A.2.d, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (Figure 2 pillars) have insulating material below them (insulating layer 3102). In addition, Lee discusses that pillar 207 and conductive input/output 204 can be formed of silicon. Exhibit 1007, ¶126.

145. Thus, the combination of Lee’s Figure 35 with Figure 2 teaches the limitations of claim 13 and a POSITA would have been motivated to combine those figures for the reasons I discuss above in Section X.A.2.c. Lee’s Figure 2 teaches the additional limitations of claim 14. Accordingly, in my opinion, the combination of Lee’s Figure 35 with Figure 2 renders claim 14 obvious.

4. Claim 15: “The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.”

146. As I discuss above, Patent Owner may argue “SOI pillar” encompasses any pillar-shaped structure with insulating material below it. In my opinion, such a

construction is incorrect because it is inconsistent with the intrinsic evidence. Nevertheless, Lee discloses or suggests this limitation under such a construction.

147. In my opinion, Lee discloses or suggests claim 15's additional limitations, which recite (1) "a vertical transistor," (2) the vertical transistor has "a charge-trapping gate insulator and a gate," and (3) the charge-trapping gate insulator and gate are "on a SOI pillar."

148. As to (1) "vertical transistor," in Section X.A.2.c I describe how Lee's Figures 1A, 1B, and 7 (as I have annotated and reproduced below) depict a "vertical transistor" (channel stacked above source and below drain and direction of current flow I).

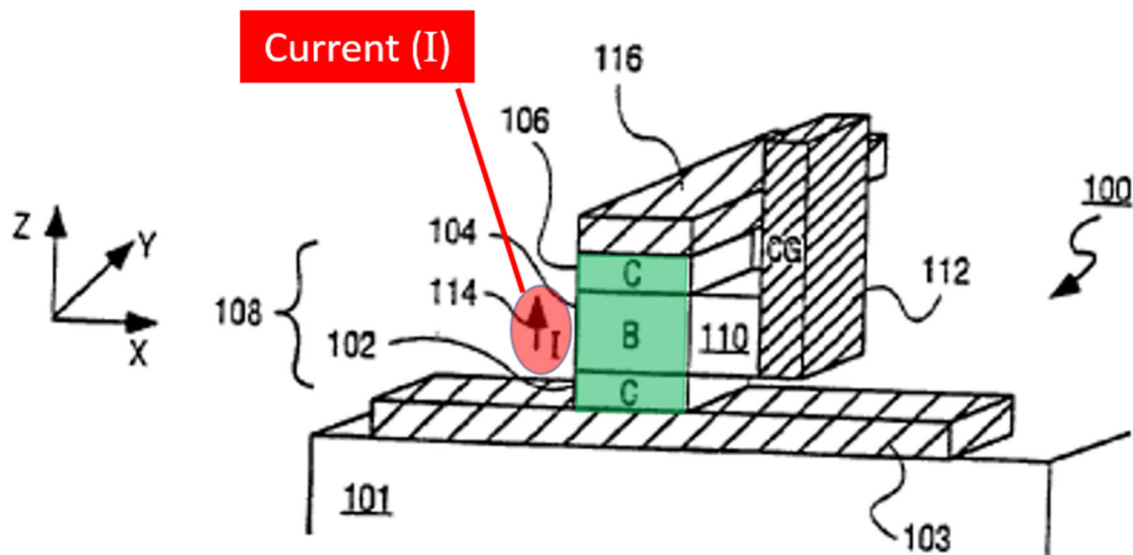


FIG. 1A

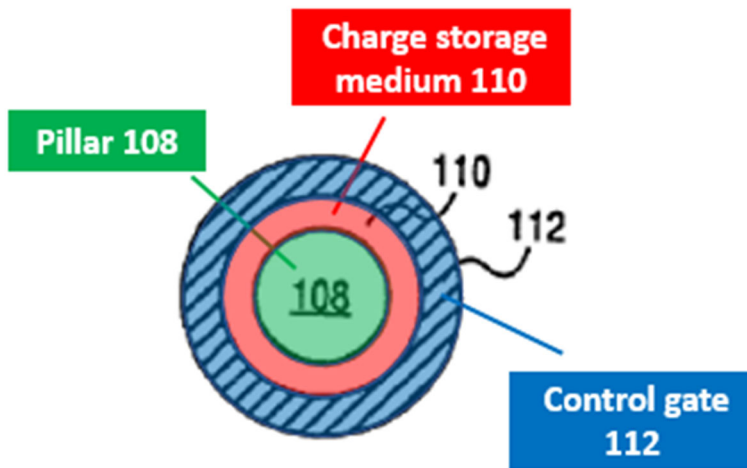


FIG. 1B

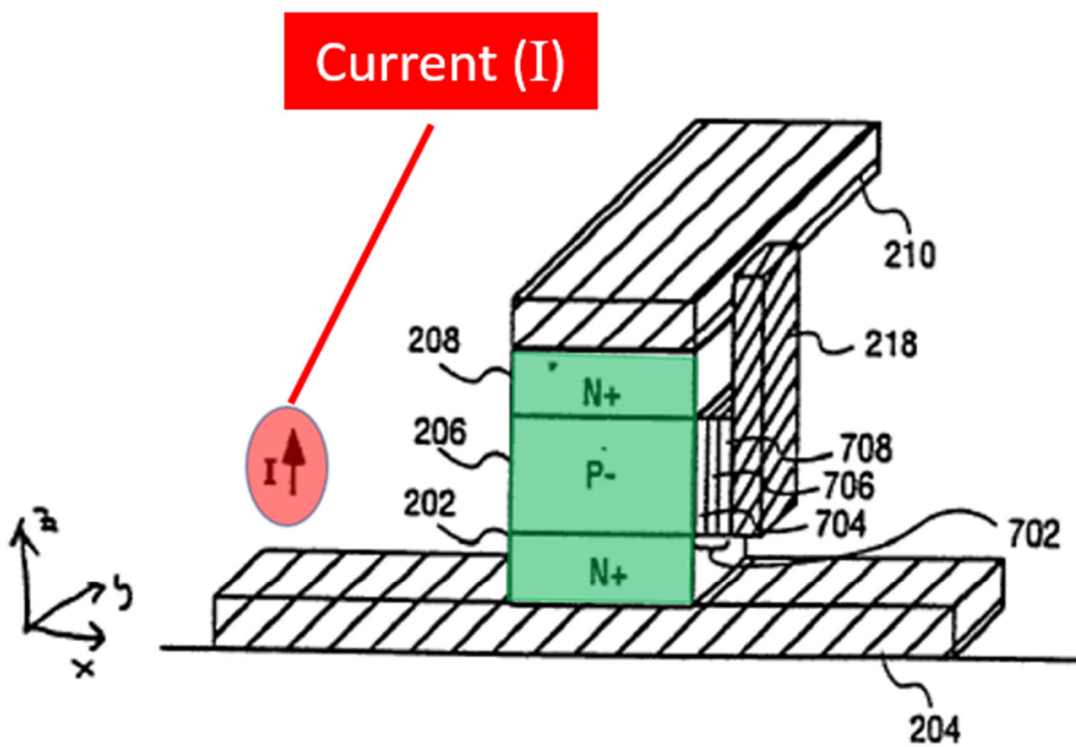


FIG. 7

149. As to (2) the vertical transistor has “a charge-trapping gate insulator and a gate,” in each of Figures 1A, 1B, and 7, the vertical transistor has “a charge-trapping gate insulator and a gate.” In Lee’s Figure 1A, the drain (106), channel (104), and source (102) stacked vertically and perpendicularly to the substrate (“vertical transistor”) has charge storage medium 110 (“charge-trapping gate insulator”) and control gate 112 (“gate”). *Id.*, ¶¶119, 122–125. In Lee’s Figure 7, channel 206 stacked above source 202 and below drain 208 (“vertical transistor”) has dielectric stack 702 (“charge-trapping gate insulator”) and control gate 218 (“gate”). *Id.*, ¶138.

150. As to (3) the charge-trapping gate insulator and gate are “on a SOI pillar,” in each of Figures 1A, 1B, and 7, under PO’s apparent construction. In Lee’s Figure 1A, charge storage medium 110 (“charge-trapping gate insulator”) and control gate 112 (“gate”) are on pillar 108 (“SOI pillar” under PO’s apparent construction). In Figure 1A, “[a]dherent to and in contact with body 104 is a charge storage medium 110,” and “a control gate 112 is formed adjacent to and in direct contact with the charge storage medium 110.” *Id.*, ¶¶122, 125. In Lee’s Figure 1B, “the pillar 108 is surrounded by a single charge storage member 110 and a single control gate 112.” *Id.*, ¶125, Fig. 1B. In Lee’s Figure 7, “the charge storage medium can be a dielectric stack 702 comprising a first oxide layer 704 adjacent to the silicon body or channel, a nitride layer 706 adjacent to the first oxide layer and a second

oxide layer 708 adjacent to the nitride layer and adjacent to the control gate 218.” *Id.*, ¶138. In my opinion, each of Lee’s Figures 1A, 1B, and 7 teaches its charge storage medium and control gate “on” the pillar in the same way that charge-trapping gate insulating layer 183g and gate 123 are “on” SOI pillar 124 in ’702 Patent Figure 25. ’702 Patent, 9:26, 36–50.

151. As I discuss in Section X.A.2.d, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (pillars of Figures 1A, 1B, and 7) have insulating material below them (insulating layer 3102). In addition, Lee discusses that in Figures 1A, 1B, and 7, the pillar and conductive input/outputs can be formed of silicon. Exhibit 1007, ¶¶119, 126.

152. Thus, the combination of Lee’s Figure 35 with either Figure 1A, 1B, or 7 teaches the limitations of claim 13 and a POSITA would have been motivated to combine those figures for the reasons I discuss above in Section X.A.2.c. For the reasons I discuss above, Lee’s Figure 1A, 1B, or 7 teaches the additional limitations of claim 15. Accordingly, in my opinion, the combination of Lee’s Figure 35 with Figure 1A, 1B, or 7 renders claim 15 obvious.

5. Claim 16: “The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.”

153. As I discuss above, Patent Owner may argue “SOI pillar” encompasses any pillar-shaped structure with insulating material below it. In my opinion, such a construction is incorrect because it is inconsistent with the intrinsic evidence. Nevertheless, Lee discloses or suggests this limitation under such a construction.

154. In my opinion, Lee discloses or suggests claim 16’s additional limitations, which recite: (1) two nonvolatile memory cells which are (2) vertically oriented, (3) serially connected together, and (4) formed with a first SOI pillar.

155. As I discuss above in Section X.A.1, Lee discloses a fabrication process through a progression of Figures. Exhibit 1007, Figs. 13–28. I have reproduced and annotated below Lee’s Figure 25A, showing a multi-level pillar memory structure made with that fabrication process.

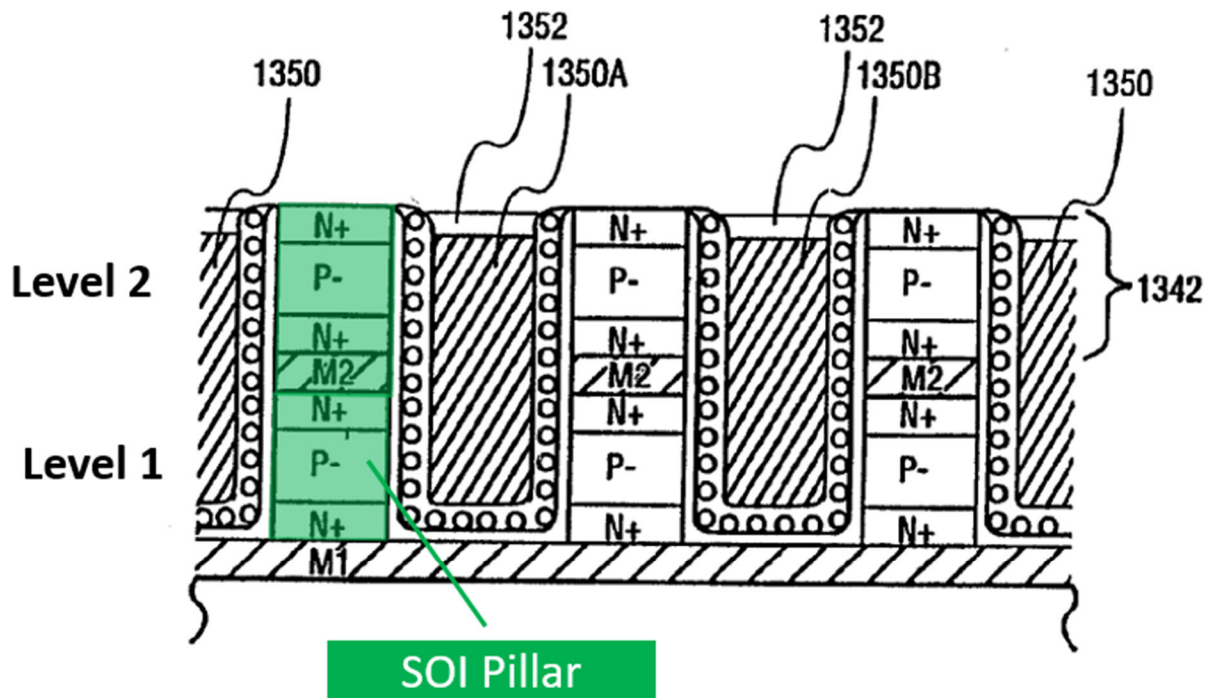


FIG. 25A

156. Figure 25A shows (1) two nonvolatile memory cells which are (2) vertically oriented, (3) serially connected together, and (4) formed with a first SOI pillar. I note that, as I explain in Section X.A.1, although Level 2 of Lee's Figure 25A remains in pillar strip form, Lee discloses an iterative process for fully fabricating its levels, including Level 2. Exhibit 1007, Figs. 13–28. Based on the disclosed fabrication process, in my opinion, a POSITA would have understood after the subsequent etch step I discuss above, Level 2 would be pillars (not pillar strips) and have the same cross-section depicted in Figure 25A (as I have reproduced and annotated above).

157. As to (1) two nonvolatile memory cells, Figure 25A discloses “two nonvolatile memory cells” (green) because, similar to the discussion of Lee’s Figures 2 and 7 above, the structures of the memory cells shown in Figure 25A, i.e., floating gate, control gate dielectric, and control gate, ensure that stored information is retained even when power is removed. *See* Exhibit 1007, ¶¶6, 113, 147–148, 154–155, 163–167.

158. As to (2) two nonvolatile memory cells which are vertically oriented, the two memory cells in Figure 25A are “vertically oriented” for the same reasons explained in Section X.A.2.c, i.e., that the source, channel, drain are arranged perpendicular to the substrate, such that current flows perpendicular to the substrate. *See, e.g.*, Exhibit 1007, ¶¶148, 158, 165 (Figure 25A pillar 1342 comprises an N+/P-/N+ stack as in Figure 2, i.e., drain/channel/source).

159. As to (3) two nonvolatile memory cells which are serially connected together, Figure 25A’s two memory cells are “serially connected together.” Specifically, the two memory cells (green) are separated from one another only by conductor layer M2. As such, those two memory cells are electrically connected to one another, with the source of the top memory cell connected to the drain of the bottom cell, and therefore, the two memory cells are serially connected. Exhibit 1007, Fig. 23A, ¶¶119, 161.

160. As to (4) two nonvolatile memory cells which are formed with a first SOI pillar, Figure 25A's two memory cells are "formed with a first SOI pillar," to the extent that "SOI pillar" encompasses any pillar-shaped structure with an insulating material below it. In Figure 25A, the two memory cells are formed within Levels 1 and 2 on a common pillar (green). Exhibit 1007, ¶147. Lee's Figure 25A teaches two memory cells "formed with a first SOI pillar" in the same way that the two memory cells in Figure 27 of the '702 Patent are "formed with" SOI pillar 124. '702 Patent, 9:51–58. In addition, in Figure 25A, the pillar and conductive input/outputs can be formed of silicon. Exhibit 1007, ¶¶119, 126, 147, 148.

161. As I discuss in Section X.A.2.d, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (Figure 25A pillars) have insulating material below them (insulating layer 3102).

162. The combination of Lee's Figure 35 with Figure 25A teaches the limitations of claim 13, and a POSITA would have been motivated to combine those figures for the reasons I discuss above in Section X.A.2.c. For the reasons discussed above, Lee's Figure 25A teaches the additional limitations of claim 16 under PO's apparent construction. Accordingly, in my opinion, the combination of Lee's Figure 35 with Figure 25A renders claim 16 obvious.

6. **Claim 17: “The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.**

163. As I discuss above, Patent Owner may argue “SOI pillar” encompasses any pillar-shaped structure with insulating material below it. In my opinion, such a construction is incorrect because it is inconsistent with the intrinsic evidence. Nevertheless, Lee discloses or suggests claim 17’s additional limitations under such a construction.

164. Section X.A.5 explains that Lee’s Figure 25A discloses or suggests “at least two nonvolatile memory cells on the first SOI pillar.” Figure 25A further shows that those memory cells are serially connected to a conductive bitline or wordline M1 1308 (“interconnect line”) and M1 connects the first pillar to an adjacent pillar having a nonvolatile memory cell. Exhibit 1007, ¶¶148, 161, Fig. 25A. Further still, M1 1308 is disposed on interlayer dielectric layer 1304, as explicitly shown in Figs. 13A, 14A, 15A, 16A, 17A, and 18A describing earlier stages in the fabrication process that leads to and includes Fig. 25A. Exhibit 1007, ¶¶147–165. In my opinion, in the combination with Lee’s Figure 35, that interconnect line would similarly be disposed on interlayer insulating layer 3102 (“dielectric layer”).

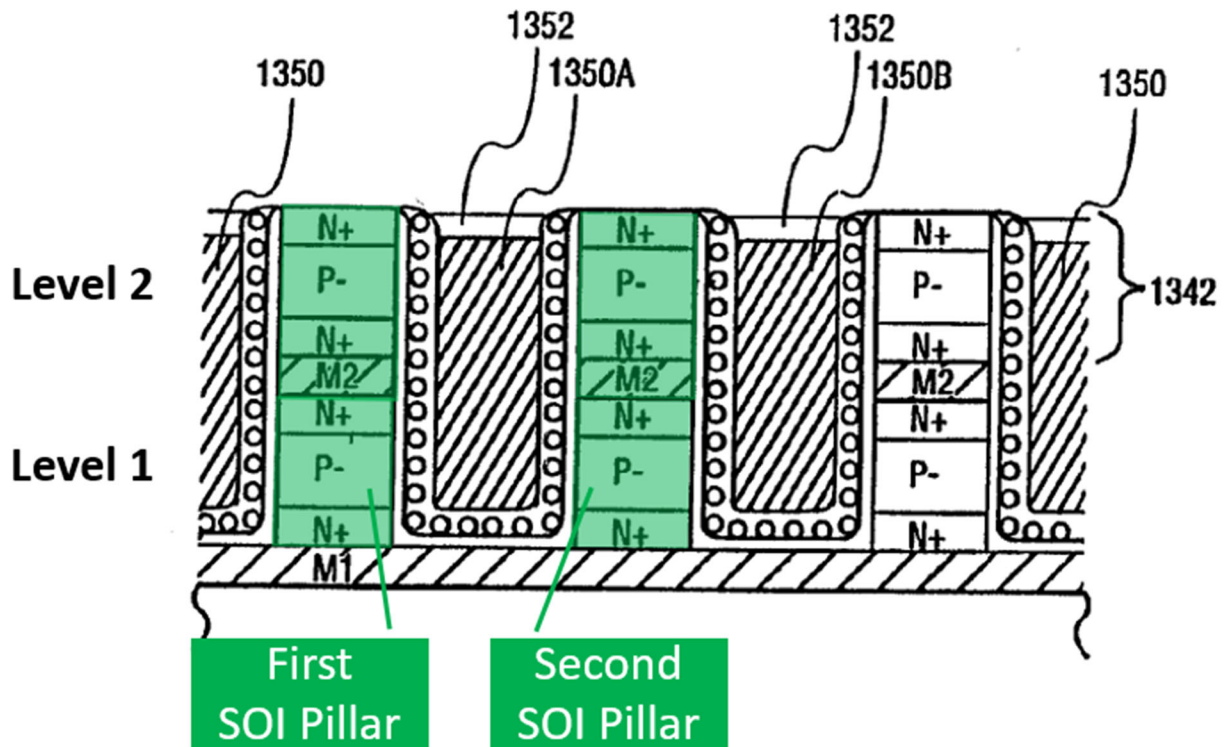


FIG. 25A

165. The memory cell in the adjacent pillar in Figure 25A is nonvolatile because it has the same structure as the “two nonvolatile memory cells” discussed in Section X.A.5 for claim 16 and thus ensures that stored information is retained even when power is removed. Exhibit 1007, ¶¶6, 113, 147–148, 154–155, 163–167.

166. Thus, in my opinion, in view of the above, Lee discloses the “first SOI pillar” serially connected by M1 (i.e., “interconnect line”), to a nonvolatile memory cell within the “second SOI pillar.”

167. In my opinion, Lee’s Figure 25A teaches a memory cell “formed with a second SOI pillar” in the same way that two memory cells in ’702 Patent Figure

27 are “formed with” SOI pillar 124. ’702 Patent, 9:51–58. As I discuss in Section X.A.2.c, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (Figure 25A pillars) have insulating material below them (insulating layer 3102). In addition, in Figure 25A, the pillar and conductive input/outputs can be formed of silicon. Exhibit 1007, ¶¶119, 126, 147–148.

168. For the reasons I discuss above, in my opinion, the combination of Lee’s Figure 35 with Figure 25A renders claim 17 obvious.

B. Ground 1B: Obviousness over Lee and Endoh (Claims 16-17)

169. As I discuss above in Section X.A.2, Lee teaches all of the limitations of independent claim 13 under PO’s apparent interpretation of “stackable add-on layer being bonded,” and Lee further teaches the additional limitations of dependent claims 14 and 15 under PO’s apparent interpretation of “SOI pillar.” In my opinion, Lee in combination with Endoh teaches the additional limitations of claims 16 and 17 under PO’s apparent interpretation of “SOI pillar.”

1. Claim 16: “The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.”

170. Claim 16 depends from independent claim 13. For the reasons I discuss above in Section X.A.2, Lee teaches or renders obvious all of the limitations of claim 13 under PO’s apparent constructions. Claim 16 further recites (1) “at least two

nonvolatile memory cells are vertically oriented,” (2) those two memory cells are “serially connected together,” and (3) those two memory cells are “formed with a first SOI pillar.” In my opinion, Lee in combination with Endoh teaches claim 16’s additional limitations under PO’s apparent constructions.

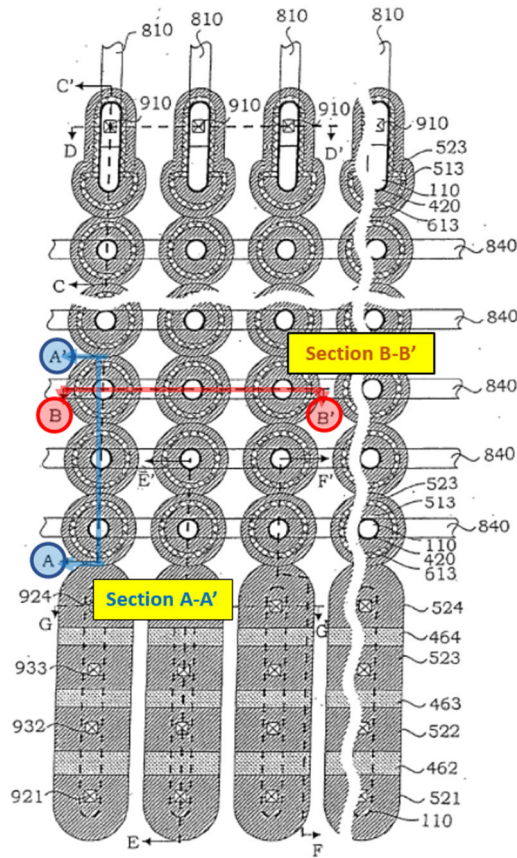
171. Endoh discloses “a semiconductor memory provided with a memory transistor having a charge storage layer and a control gate, and its production process.” Exhibit 1012, [0003]. Endoh’s Figures 1-11 “are plan views illustrating various memory cell arrays of EEPROMs [electrically erasable programmable read-only memories] having floating gates as charge storage layers in semiconductor memory devices in accordance with the present invention.” *Id.*, [0153]. Further, Endoh’s Figures 132-1650 “are sectional views (taken on line A-A' and line B-B' in FIG. 1, FIG. 5, FIG. 10 or FIG. 13) illustrating various production steps for producing semiconductor memory devices in accordance with the present invention.” *Id.*, [0165]. In particular, Endoh’s “Production Example 52” discloses that Figures 1171 and 1172 “are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.” *Id.*,

[1206]. In my opinion, a POSITA would have understood that EEPROM memory cells are non-volatile memory cells. Exhibit 1007, ¶6.⁷

172. I have reproduced and annotated Endoh's Figure 1 below:

⁷ See also, for example, Exhibit 1025, U.S. Pat. No. 5,615,148, 1:6-8 ("The present invention relates to an electrically erasable and reprogrammable nonvolatile semiconductor memory (EEPROM)."); Exhibit 1026, U.S. Pat. No. 5,544,103, 1:17-20 ("In general, nonvolatile semiconductor memory devices can be classified into two groups: electrically programmable read-only memories (EPROMs) and electrically erasable and programmable read-only memories (EEPROMs)."); Exhibit 1027, U.S. Pat. No. 6,381,173, 2:50-52 ("an EEPROM memory array 25 that belongs to a nonvolatile memory 100").

Fig. 1



173. Figure 1171, which I have reproduced and annotated below, shows a cross sectional view at A-A', and Figure 1172, which I have also reproduced and annotated below, shows a cross-sectional view at B-B':

Fig. 1171

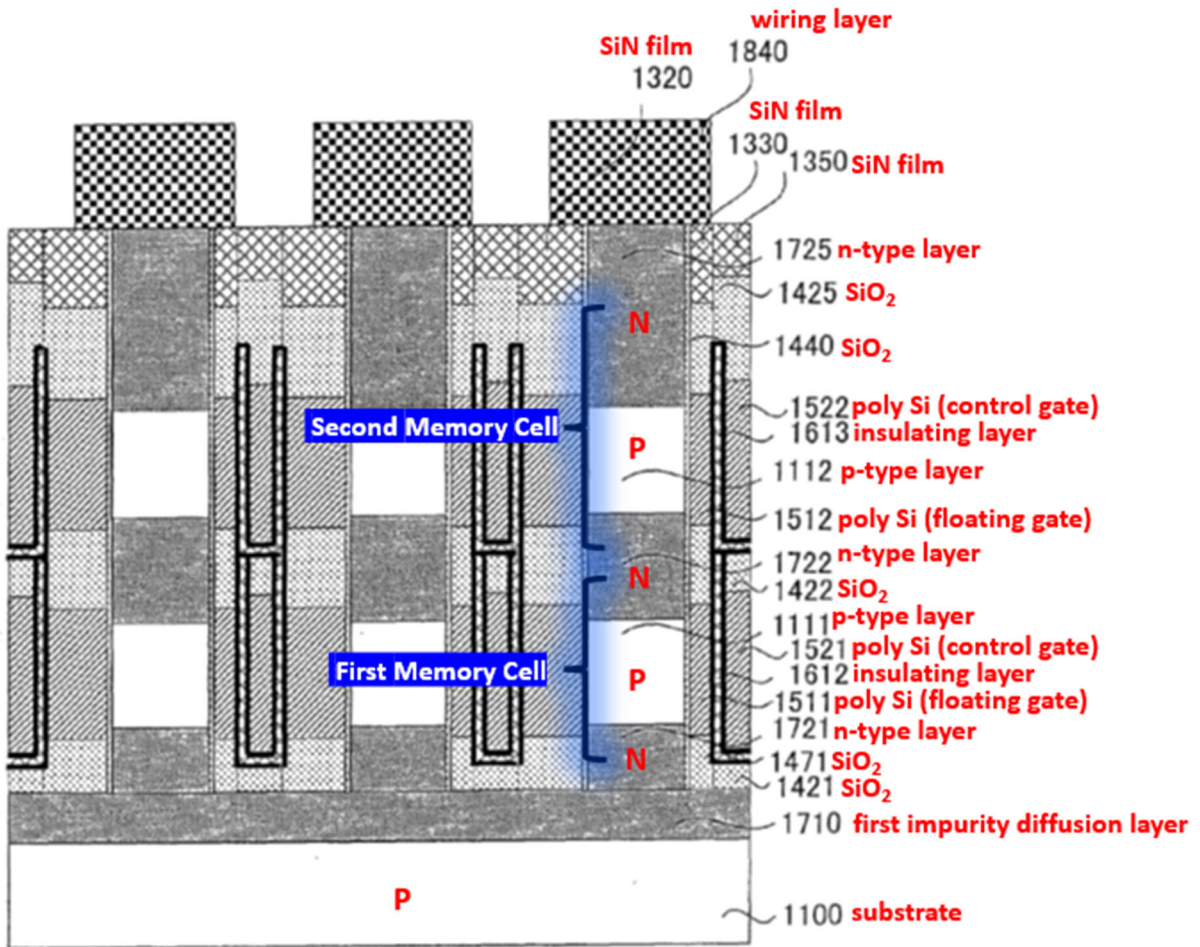


Fig. 1172

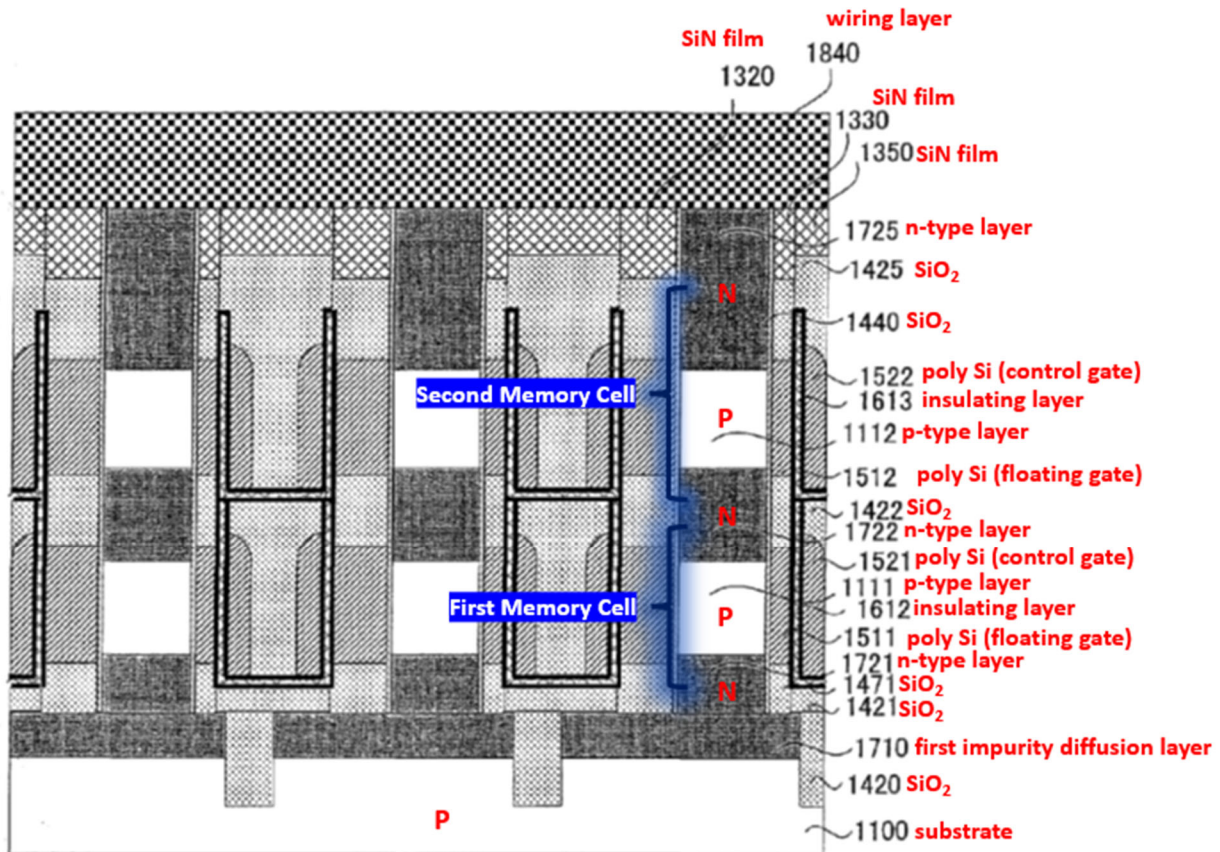


Exhibit 1012, [1206], [1207]. Endoh discloses that in the embodiment with respect to these figures, “island-like semiconductor layers are formed in the form of pillars,” “two memory cells are arranged on each island-like semiconductor layer,” “two memory transistors are arranged on the island-like semiconductor layer,” and “the transistors are connected in series along the island-like semiconductor layer.” *Id.* Further, Endoh’s configuration is shown in annotated Figures 1171 and 1172 above (n-type layer 1725, p-type layer 1112, n-type layer 1722, p-type layer 1111, and n-type layer 1721, all in the same pillar, form two transistors for two memory cells).

Id., [1206], [1207] (stating that “[i]n this example, production step[s] are the same as Production Example 45” with limited exceptions), [1050]-[1081] (describing Production Example 45, with paragraph [1074] identifying the p-type and n-type semiconductor layers used in the two transistors with the same reference numbers in Figures 1171 and 1172).

174. For (1) “at least two nonvolatile memory cells are vertically oriented,” Endoh’s Production Example 52 discloses two EEPROM memory cells (“at least two nonvolatile memory cells”), each with transistors in which the source (e.g., n-type layers 1721-22 in Figures 1171-72), drain, and channel regions (e.g., p-type layers 1111-12 in Figures 1171-72) are arranged perpendicular to the substrate (e.g., substrate 1100 in Figures 1171-72) (each of those memory cells “are vertically oriented”). *Id.*, [1050]-[1081], [1206], [1207], Figs. 1171-72. As with ’702 Patent Figure 27, in my opinion, a POSITA would have understood that current flows through the source, channel, and drain of the two memory cells perpendicular to the base substrate. *Id.*, [1205]-[1207], Figures 1171-72.

175. For (2) “at least two nonvolatile memory cells” are “serially connected together,” Endoh’s nonvolatile memory cells are “serially connected together.” Endoh’s Production Example 52 discloses that the “island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate” and that the

“transistors [of the two EEPROM memory cells] are connected in series along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172.” *Id.*, [1205]-[1207], Figures 1171-72.

176. For (3) “at least two nonvolatile memory cells” are “formed with a first SOI pillar,” Endoh’s nonvolatile memory cells are “formed with a first SOI pillar,” under PO’s apparent construction, because the transistors of the two EEPROM memory cells “are arranged on the island-like semiconductor layer” (“formed with a first SOI pillar”). *Id.*, [1205]-[1207], Figures 1171-72. In my opinion, this is consistent with the ’702 Patent’s Figure 27. As I discuss in Section X.A.2.c, the stackable add-on layer is bottom level 3104 in Lee Figure 35, and thus pillars formed in it (the pillars of the Lee-Endoh combination as I discuss below) have insulating material below them (insulating layer 3102). In addition, the pillars and conductors can be formed of silicon. EX1007, ¶¶119, 126, 147-148; EX1012, ¶1206.

177. In my opinion, a POSITA would have been motivated to modify Lee’s device level 3104 in the array of memory devices 3101 to implement two memory cells on each pillar as taught in Endoh’s Production Examples. In particular, both Lee and Endoh disclose cylindrical pillar nonvolatile memory structures. *Compare* Exhibit 1007, Fig. 1B, *with* Exhibit 1012, Fig. 1. Further, Lee discloses a nonvolatile memory structure with two memory cells on each pillar (*see* Section X.A.5 (discussing Fig. 25A)). In my opinion, Lee’s Figure 25A provides motivation for a

POSITA to implement Endoh's two memory cells on each pillar in Lee's device level 3104.

178. In my opinion, a POSITA would have recognized that applying two memory cells in each pillar as taught in Endoh to Lee's level 3104 would further Lee's objective of increasing device density. Exhibit 1007, ¶¶106, 107. For example, Lee states "[t]he present inventors have realized that the cost of memory and logic devices would be decreased if the device density was increased." *Id.*, [0106]. Based on the need for increased device density, Lee discloses providing "an ultra dense matrix array of charge storage semiconductor devices which has an increased density and a lower cost." *Id.* Lee explains "[o]ne method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels." *Id.*, [0107]. Endoh, as I discuss above, discloses a structure with two memory cells arranged on each pillar (e.g., island-like semiconductor layers in the form of pillars in Endoh's Production Example 52). Exhibit 1012, [1206], [1207], Figs. 1171–1172.

179. Further, in my opinion, a POSITA would also have recognized that this combination merely amounts to using a known technique (implementing serial memory cells in a pillar as taught by Endoh) to improve a similar known device (Lee's memory array 3101) in the same way (serial memory cells in the same pillar to increase density). In addition, in my opinion, the combination would have

amounted to applying a known technique (two memory cells on each pillar) to address the same known problem recognized by both Lee and Endoh (fabricating memory arrays using pillar structures) using prior art elements according to their established functions (pillar structures with two memory cells per pillar in Lee's Figure 35 structure).

180. Further, in view of the above, in my opinion, a POSITA would have had a reasonable expectation of success in making such a modification to Lee in light of Endoh's teachings. In particular, both Lee and Endoh disclose embodiments with two memory cells per pillar showing that such structures were within the skill of a POSITA. Exhibit 1007, Fig. 25A; Exhibit 1012, Figs. 1171-1172.

181. Accordingly, in my opinion, Lee in combination with Endoh renders claim 16 obvious under PO's apparent constructions.

2. Claim 17: "The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar."

182. Dependent claim 17 further depends from dependent claim 16. As I discuss above in Section X.B.1, Lee and Endoh render claim 16 obvious under PO's apparent constructions. Claim 17 additionally recites (1) the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line

disposed on a dielectric layer and (2) those two memory cells are connected to another nonvolatile memory cell formed with a second SOI pillar.

183. As to (1), Endoh teaches “the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer.” As I discuss above in Section X.B.1, Endoh’s Figures 1171-72 disclose two EEPROM memory cells arranged on each pillar-shaped semiconductor layer (“the at least two nonvolatile memory cells on the first SOI pillar”). Further, as shown in annotated Figures 1171-72 (which I have reproduced and annotated below), those two nonvolatile memory cells in each pillar are serially connected to wiring layer 1840 (“interconnect line”) disposed on SiN films 1320, 1330 and 1350 (“dielectric layer”). Exhibit 1012, Figs. 1171-72.

Fig. 1171

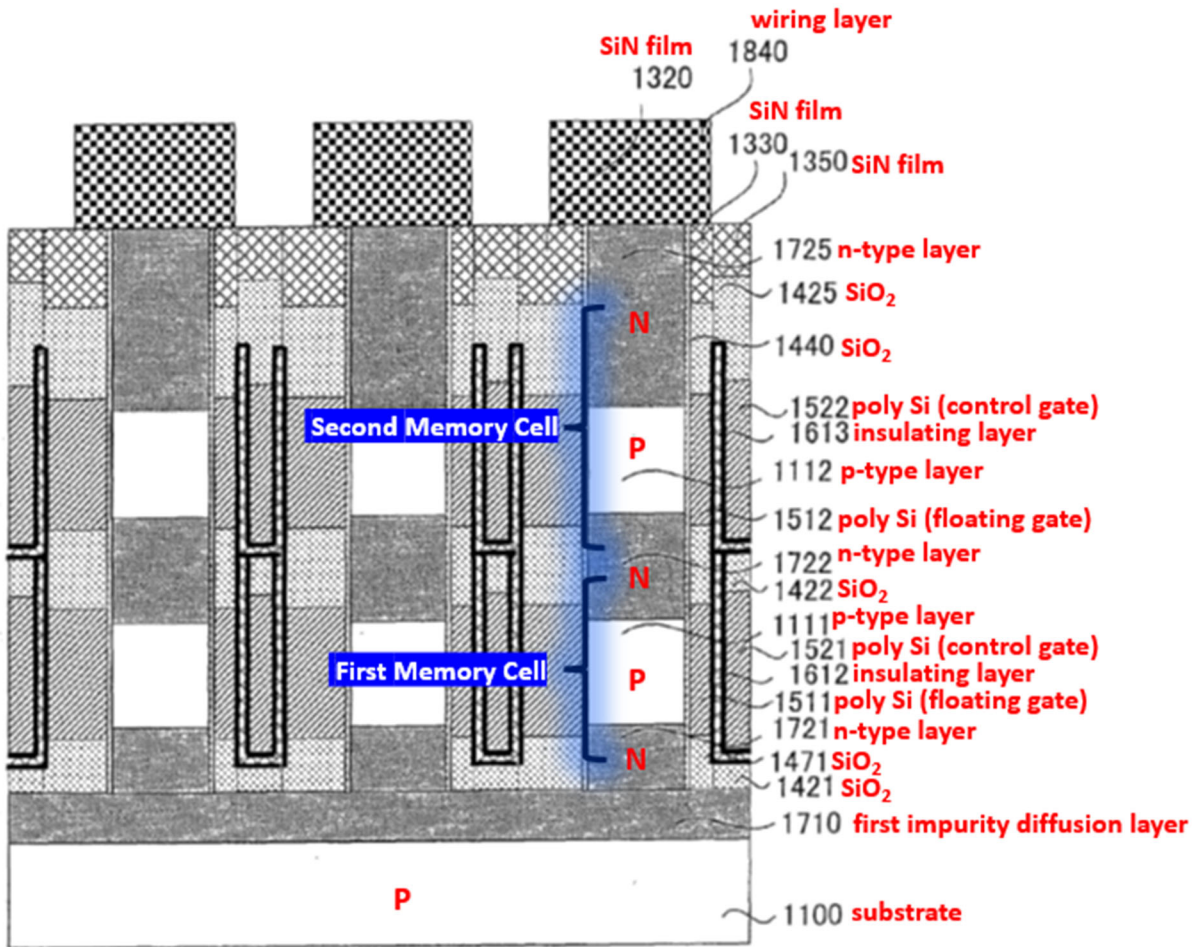
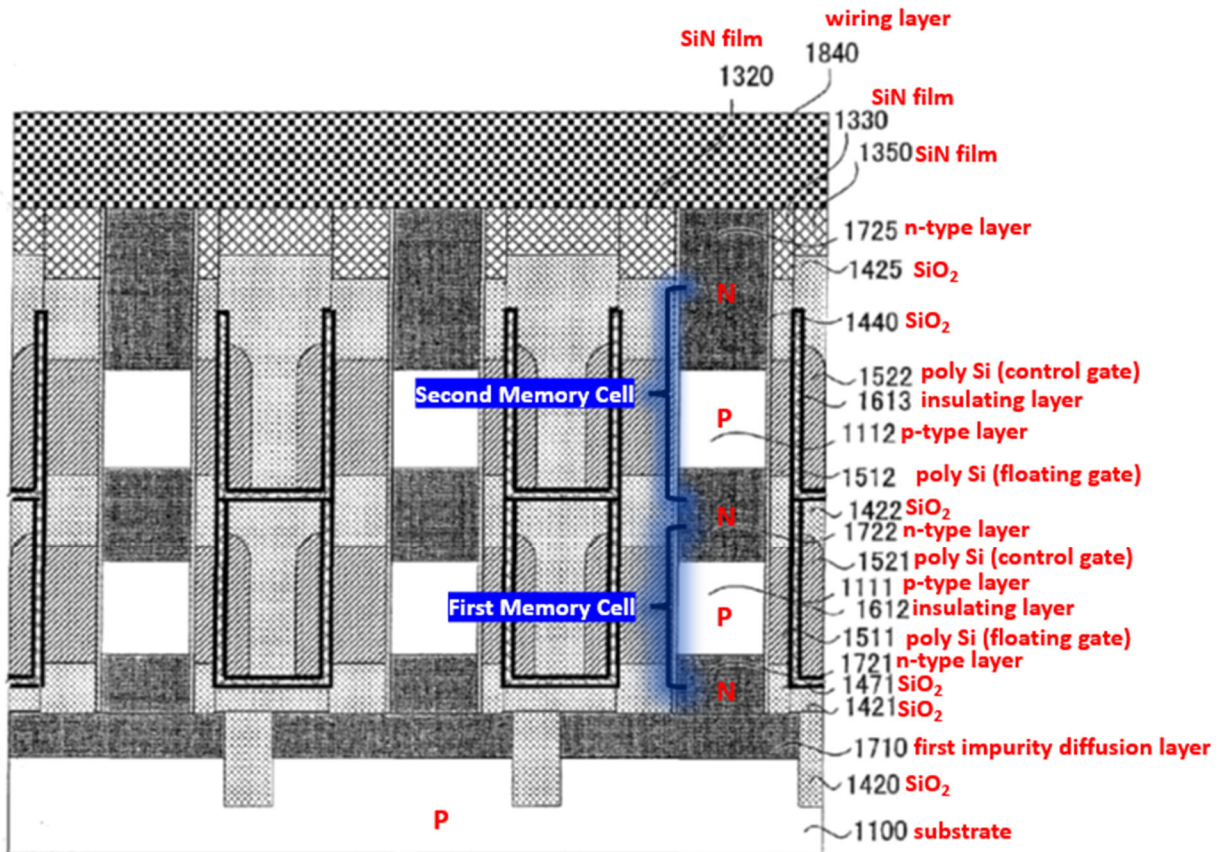


Fig. 1172

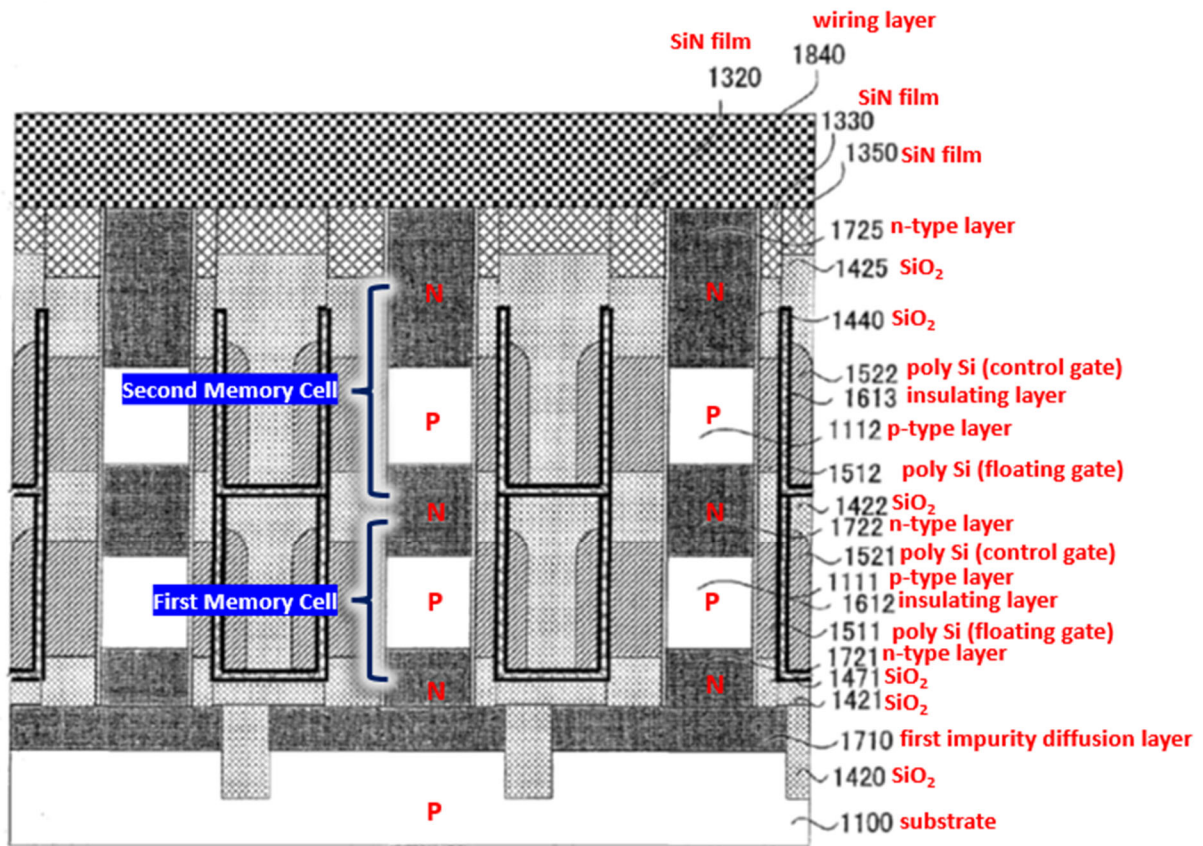


Further, Endoh's Production Example 52 teaches arranging wiring layer 1840 on SiN films 1320, 1330 and 1350. Exhibit 1012, [1207] (stating that "[i]n this example, production step[s] are the same as Production Example 45" with limited exceptions), [1050]-[1081] (describing Production Example 45, with paragraph [1076] identifying wiring layer 1840 connected to n-type layer 1725 and paragraphs [1056], [1069] identifying silicon nitride films 1320, 1330 and 1350 as insulating films). Therefore, Endoh's two EEPROM memory cells arranged on each pillar-shaped semiconductor layer ("the at least two nonvolatile memory cells on the first SOI

pillar”) are serially connected with wiring layer 1840 (“interconnect line”) disposed on SiN films 1320, 1330 and 1350 (“dielectric layer”).

184. Those two memory cells are also connected to another “nonvolatile memory cell formed with a second SOI pillar,” under PO’s apparent construction. As shown in annotated Figure 1172 (above), Endoh’s wiring layer 1840 connects two “island-like semiconductor layers [that] are formed in the form of pillars” (i.e., the “first SOI pillar” to the “second SOI pillar”). *Id.*, [1206], Figure 1172. Endoh also discloses two nonvolatile memory cells formed with a neighboring pillar having island-like semiconductor layers (i.e., “second SOI pillar”). *Id.*, [1206], Figure 1172 (reproduced below).

Fig. 1172



Thus, those memory cells in the “first SOI pillar” are connected to another nonvolatile memory cell formed with the “second SOI pillar” through wiring layer 1840, as shown in Figure 1172. As I discuss in Section X.A.2.c, the stackable add-on layer is bottom level 3104 in Lee Figure 35, and thus pillars formed in it (the pillars of the Lee-Endoh combination as I discuss below) have insulating material below them (insulating layer 3102). In addition, in both Lee and Endoh, the pillars and conductors can be formed of silicon. Exhibit 1007, ¶¶119, 126, 147-148; Exhibit 1012, ¶1206.

185. The modification to Lee based on Endoh's teachings, reasoning for that modification, and reasonable expectation of success analyses for claim 16 (as I discuss in Section X.B.1) apply equally to claim 17. *Id.* In addition, in the combination, Lee's Figure 1A and 1B pillars are serially connected to conductive layer 103 ("serially connected with an interconnect line") which in the combination with Lee's Figure 35 is disposed on insulating layer 3102 ("disposed on a dielectric layer"). Exhibit 1007, Figs. 1A, 1B, 35, ¶¶111, 122, 125. In my opinion, Lee's teachings thus support that a POSITA would have been motivated to modify Lee to include two memory cells per pillar as taught in Endoh and in this modification, those two memory cells would be serially connected with an interconnect line disposed on a dielectric layer. In my opinion, Lee's and Endoh's teachings also support a reasonable expectation of success for the modification because they show this configuration was within the skill of a POSITA.

186. Thus, in my opinion, Lee in combination with Endoh renders claim 17 obvious under PO's apparent constructions.

C. Ground 1C: Obviousness over Lee and Kim (Claims 13–17)

187. As I discuss above, in my opinion, in the context of the intrinsic record of the '702 Patent, a person of ordinary skill in the art would have understood "the stackable add-on layer being bonded" as recited in claim 13 to require that the stackable add-on layer is wafer bonded to the dielectric. Under the proper

construction of “the stackable add-on layer being bonded” for claim 13 and PO’s apparent construction of “SOI pillar” for claims 14–17, in my opinion, claims 13–17 would have been obvious over Lee and Kim for the reasons I discuss below.

1. Claim 13

a. 13[pre]-13[b]

188. For the same reasons I discuss in Sections X.A.2.a, X.A.2.b, and X.A.2.c above, in my opinion, Lee discloses or suggests limitations 13[pre]–13[b].

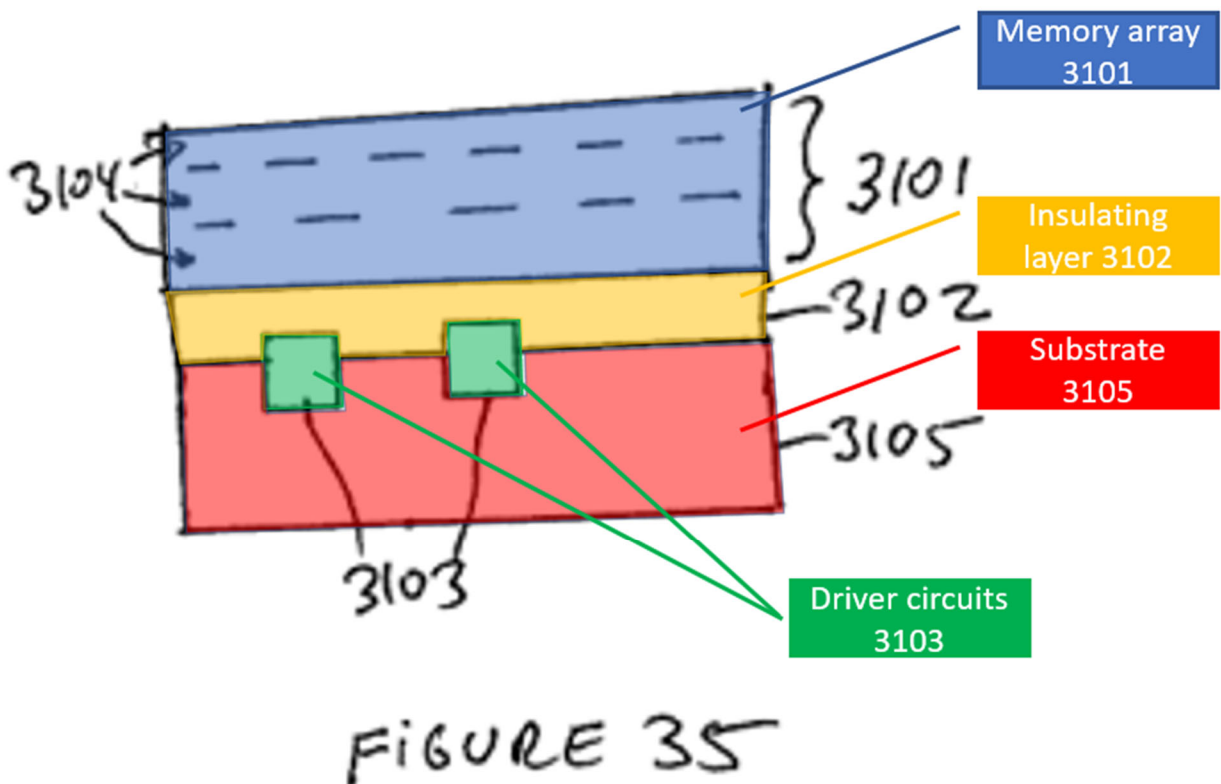
b. 13[c]: “the stackable add-on layer being bonded to the dielectric layer; and”

189. In my opinion, under the proper construction of “the stackable add-on layer being bonded” as requiring wafer bonding, as I discuss above in Section IX.A, the combination of Lee and Kim teaches this limitation.

190. Kim discloses bonding active device wafers together via a dielectric layer to form “a three-dimensional (3-D) wafer-to-wafer vertical stack.” Exhibit 1008, ¶¶19–20, Fig. 1. Kim’s describes its invention as being “applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, ... CMOS devices, MOSFETs, and new memory devices.” *Id.*, ¶19. Kim also discloses that its 3D vertical wafer stack may include “any number” of wafers, and provides an example bonding wafer 110 having one or more microprocessors and wafer 120 including one or more memory devices using a

dielectric layer 102. *Id.*, ¶20, Fig. 1; *see also id.*, ¶22 (discussing “logic/memory stacking”).

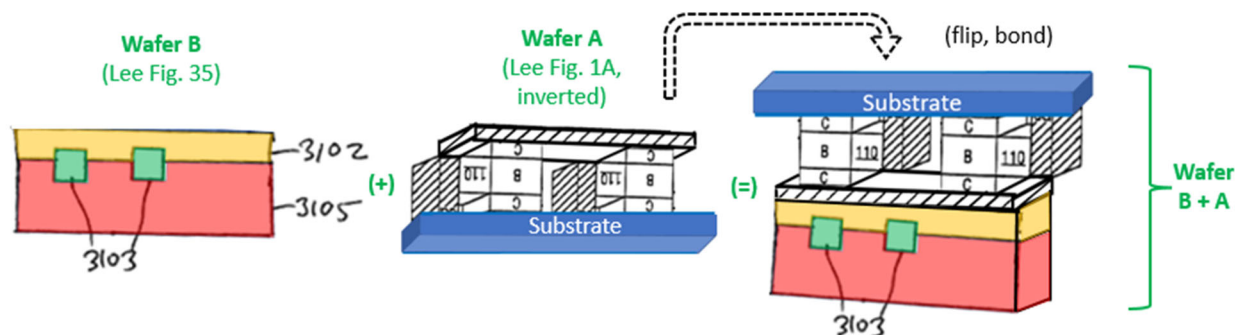
191. In Lee, each level 3104 of array 3101 is deposited on the underlying levels of array 3101. Exhibit 1007, ¶107, Fig. 35 (reproduced below).



192. Lee does not explicitly describe the process by which bottom level 3104 of array 3101 is formed on interlayer insulating layer 3102. *See id.*, ¶¶107-113. Thus, in my opinion, a POSITA would have looked to other art, such as Kim, for details about attaching bottom level 3104 to insulating layer 3102. For example, a POSITA looking to separately form Lee’s memory device and “package [it] together” with Lee’s substrate 3105 having driver circuits 3103 formed therein and insulating layer

3102 on top “to form a non-monolithic memory device” would have looked to the teachings of Kim. Exhibit 1007, ¶107. Kim contemplates bonding a wafer having CMOS devices, like Lee’s substrate 3105 having CMOS transistors forming driver circuits 3103, with a wafer having memory devices, like Lee’s level 3104. Exhibit 1008, ¶¶19–20; Exhibit 1007, ¶111. In my opinion, a POSITA would have been motivated to apply Kim’s wafer bonding teachings to implement Lee’s Figure 35 memory device as a non-monolithic one.

193. I have created the figures below to illustrate one way a POSITA would have found it obvious to apply Kim’s teachings in Lee to wafer bond level 3104 as shown in Lee’s Figure 1A to layer 3102. (I note that a POSITA would have found it obvious to use any of the memory structures in Figures 1A, 1B, 2, 7, or 25A in such a process).



194. As shown above, Lee’s separately fabricated memory cells (e.g., from Lee’s Figure 1A) would be formed on their own substrate (“Wafer A”). Wafer A (having Lee’s separately fabricated memory devices) would be flipped and bonded,

per Kim's teachings, to Wafer B having Lee's driver circuits 3103 ("electrical devices") and insulating layer 3102 ("dielectric layer"). Exhibit 1008, ¶20 ("a dielectric layer is used to bond active device wafers"). In the combination, as in Kim Figure 1 with wafer 120 bonded to wafer 110 using dielectric layer 102, Lee's bottom level 3104 ("stackable add-on layer," having, e.g., Lee's Figure 1A memory cells) would be wafer bonded to interlayer insulating layer 3102 ("dielectric layer"), resulting in the structure shown in Lee's Figure 35.

195. In my opinion, a POSITA would have recognized that using wafer-bonding to bond level 3104 ("stackable add-on layer") to interlayer insulating layer 3102 ("dielectric layer") of Lee's Figure 35 would have been a predictable way to non-monolithically build the Figure 35 structure. In my opinion, a POSITA would have found this modification to be nothing more than using a known technique (Kim's wafer bonding) to improve a similar known device (the structure in Lee's Figure 35) in the same way (logic/memory stacking using a wafer bonding process). In addition, in my opinion, the combination would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Lee and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Lee's memory cell structures in Figures 1A, 1B, 2, 7, or 25A in Lee's Figure 35 structure).

196. In my opinion, a POSITA would have also recognized that wafer-bonding Lee's level 3104 to insulating layer 3102, as compared to monolithic deposition, allows for more efficient quality control with less potential waste. Specifically, when separately forming the memory devices in layer 3104, a POSITA would have recognized that quality control can be performed on the memory cells (e.g., testing for shorts) prior to bonding. If a quality issue is detected, then only that level 3104 would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited layer stacks, etc.) would need to be discarded. Testing layers of devices prior to stacking has well-known benefits. For example, Fung explains that, while "stacking chips is definitely the preferred approach for attaining 3d-IC," yield loss could be "very large" because reduced yield on stacked wafers multiplies yield loss. Exhibit 1016 ("Fung"), 1:33–47 ("Assuming a 70% yield for each finished wafer, by stacking two wafers, the maximum yield achievable is 49% (i.e., 0.7×0.7)"). Fung explains the solution to this problem is to test each wafer before stacking "to screen out defective ones." *Id.*, 1:48–52. Thus, Kim's wafer-bonding process minimizes waste resulting from defects detected in quality control. In addition, a POSITA would have recognized that forming electrical devices on one substrate separately from the memory devices on another substrate would have allowed optimization of the respective processes rather than forcing the memory devices to be formed with

a sub-optimal process tailored to preserving the electrical devices formed on the single wafer in the monolithic process.

197. In my opinion, a POSITA would have had a reasonable expectation of success with predictable results in using wafer bonding to attach Lee’s separately fabricated memory devices in layer 3104 to insulating layer 3102 because Kim shows that using such a technique to bond one wafer with electrical devices to another wafer with memory cells was within the skill of a POSITA. Exhibit 1008, ¶¶19, 20.

c. 13[d]: “wherein the memory cells are nonvolatile memory cells having at least one transistor.”

198. For the same reasons I discuss above in Section X.A.2.e, in my opinion, Lee discloses or suggests this limitation.

2. Claims 14–17

199. For the same reasons I discuss above in Sections X.A.3–X.A.6, in my opinion, Lee combined with Kim discloses or suggests each limitation in claims 14–17.

D. Ground 1D: Obviousness over Lee, Kim, and Endoh (claims 16–17)

200. In my opinion, Lee and Kim render obvious claims 16 and 17 under the proper construction of “the stackable add-on layer being bonded” and the construction I have been asked to assume PO will argue for with regard to that term.

See Section IX.A. In my opinion, claims 16 and 17 would have also been obvious over Lee, Kim, and Endoh under those constructions. The description of the Lee-Kim combination (*see* Section X.C), the description of the Lee-Endoh combination (*see* Section X.B), and the motivation to combine and reasonable expectation of success discussion for the Lee-Kim (*see* Section X.C) and Lee-Endoh (*see* Section X.B) combinations apply equally to this ground.

E. Ground 1E: Obviousness over Lee in view of Aspar (Claim 13–17)

201. As I discuss in Section IX.A, a POSITA would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the “stackable add-on layer” is wafer bonded to “the dielectric layer.” Additionally, as I discuss in Section IX.B, a POSITA would have understood that “SOI pillar” means a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology. Under these proper constructions, claims 13–17 would have been obvious over Lee in view of Aspar for the reasons I discuss below.

1. Claim 13

a. 13[pre]-13[b]

202. For the same reasons discussed in Sections X.A.2.a–X.A.2.c above, in my opinion, Lee discloses or suggests limitations 13[pre]–13[b]. In limitation 13[b], “a” stackable add-on layer encompasses one or more stackable add-on layers.

b. 13[c]

203. Under the proper construction of “the stackable add-on layer being bonded” as requiring the “stackable add-on layer” to be wafer bonded to “the dielectric layer,” in my opinion, the combination of Lee with Aspar teaches limitation 13[c].

204. In Lee, each level 3104 of array 3101 is deposited on the underlying levels of array 3101. Exhibit 1007, ¶107. Lee does not explicitly describe the process by which bottom level 3104 of array 3101 is formed on insulating layer 3102. See *id.*, ¶¶107–113. Consequently, a POSITA would have looked to and been motivated to apply other art, such as known wafer bonding techniques, for details about attaching bottom level 3104 to insulating layer 3102.⁸

205. One such known wafer bonding technique was the Smart-Cut® process described in Aspar. Exhibit 1009, 834. Aspar states “[w]afer bonding and layer transfer enable different materials to be associated to form multilayer substrates,” and the Smart-Cut® process was “an industrial process which provides high quality materials in large quantities.” *Id.* Specifically, Aspar espouses the Smart-Cut®

⁸ Wafer bonding processes were well known prior to the earliest alleged priority date of the '702 Patent (June 21, 2004). See, e.g., Section VII.A; Exhibit 1015, 54–67 (discussing various well known wafer bonding techniques).

process' ability to transfer a thin monocrystalline layer of "very good thickness homogeneity and with a high crystalline quality." *Id.*

206. The Smart-Cut® process is depicted in Aspar's Figure 1, which I have reproduced below:

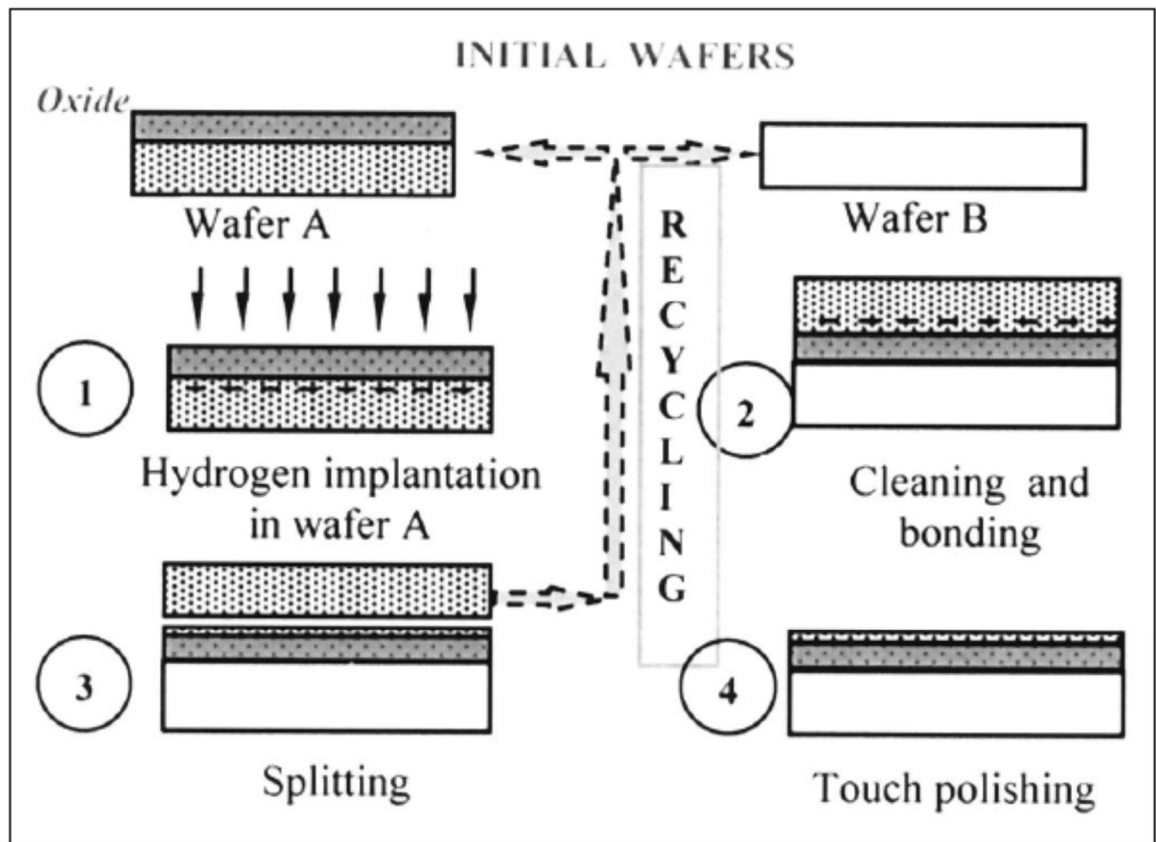


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

207. Figure 1 shows the following steps:

1. Hydrogen is implanted in a substrate A. This step induces formation of an in-depth weakened layer.
2. Substrate A is bonded to a support B by wafer bonding.

3. A splitting step, which takes place along the in-depth weakened layer, gives rise to transfer of a thin layer from the substrate A onto the support B.

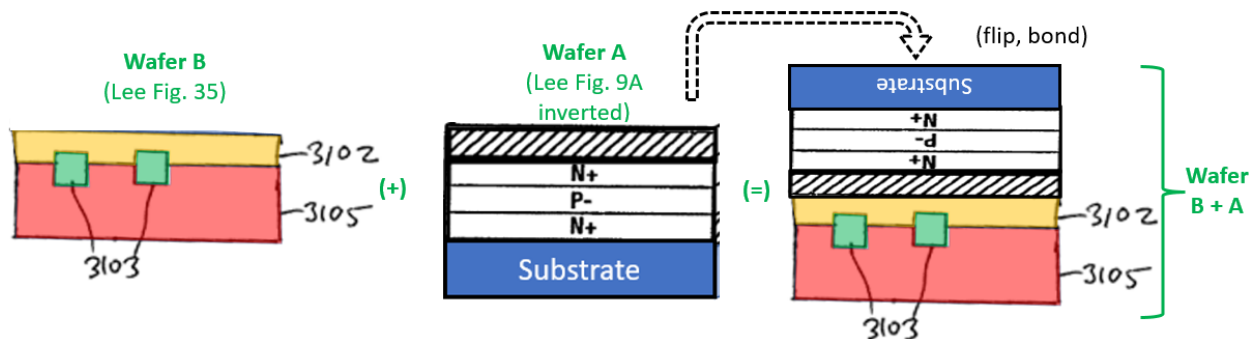
4. A final treatment can be performed to remove the rough surface left after splitting.

Id., 834–835. Aspar’s description of using Smart-Cut® to transfer a thin layer is consistent with the ’702 Patent’s description of its “SOI layer”: “a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate.” ’702 Patent, 4:48–51.

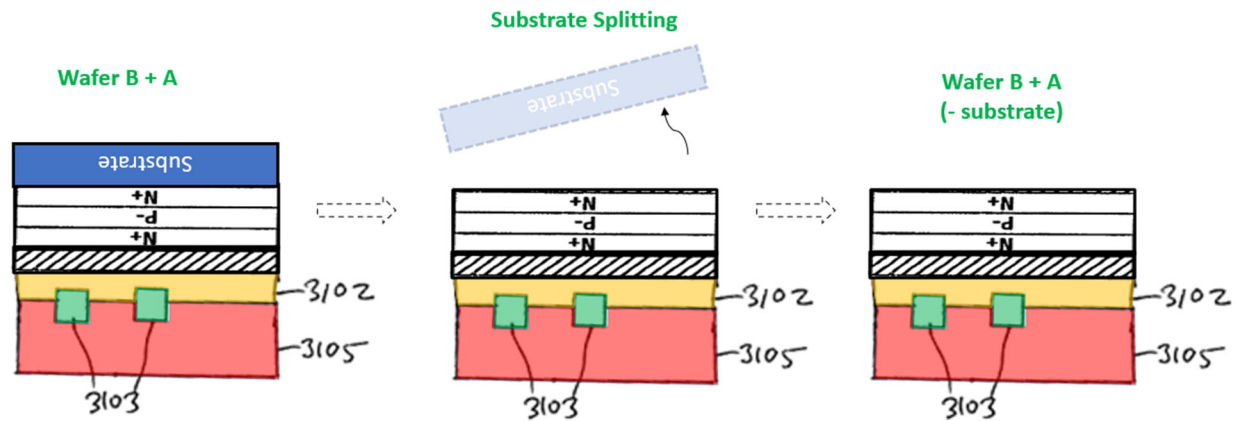
208. In addition, Aspar states “we can conclude that the Smart-Cut process really is a generic process. It allows a great deal of combinations (material and bonding layer) which open up new scope for developments.” Exhibit 1009, 839. Among these combinations, Aspar states that the Smart-Cut® process is compatible with conductive (metallic) bonding layers and can be used “to realize complex structures,” including by “transferring SOI layers stacks already formed onto a single substrate or a SOI wafer.” *Id.*, 838–839.

209. In the combination, Aspar’s Smart-Cut® process would be used to wafer bond bottom level 3104 (“stackable add-on layer”) in Lee’s Figure 35 to interlayer insulating layer 3102 (“dielectric layer”). Wafer B would consist of Lee’s

substrate 3105 with driver circuits 3103 formed therein and insulating layer 3102 disposed above the substrate. Wafer A would be separately fabricated with a single crystal surface layer with a doped stack, similar to the stack depicted in Lee's Figure 9A to form the pillars for the memory cell structures of Figs. 1A, 1B, 2, 7, and 25A. Exhibit 1007, ¶¶119, 122, 125, 138–141; *see also id.*, Fig. 13A, ¶¶147–148; Section X.A.2, ¶111, footnote 5. A conductive layer would then be deposited over the doped stack, as taught in Lee's Figure 9A, which includes input/output conductor layer 900 to form the first input/output conductors for the memory cell structures of Figs. 1A, 1B, 2, 7, and 25A. *Id.*; footnote 5 above. After the levels on Wafer A were formed, Wafer A would be flipped upside down and bonded to Wafer B. This process is depicted in the annotated series of figures I have created below:



210. After bonding, a splitting (i.e., cleaving) step would be performed, resulting in the transfer of the desired thin layer (e.g., the doped stack) and conductive layer from Wafer A onto Wafer B. This process is depicted in the annotated series of figures I have created below:



211. After bonding, the individual memory cells in level 3104 would be fabricated from the transferred thin layer in the same way they are fabricated in Lee. *E.g.*, Exhibit 1007, ¶141.

212. In my opinion, a POSITA would have been motivated to use Aspar's Smart-Cut® process to wafer bond bottom level 3104 ("stackable add-on layer") to insulating layer 3102 ("dielectric layer") of Lee's Figure 35. Exhibit 1008, ¶20, Fig. 1. Aspar teaches that Smart-Cut® "[r]ealiz[es] multiple SOI layers based on a layer transfer process ... [such as] transferring SOI layers stacks already formed onto a single substrate or a SOI wafer. So multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology." Exhibit 1009, 839. In addition, the Smart-Cut® process had several well-known advantages including "transferring thin layers of very good thickness homogeneity and with a high crystalline quality." Exhibit 1009, 834. In addition, in my opinion, a POSITA would have recognized this combination merely amounts to using a known technique (Aspar's Smart-Cut®

process) to improve a similar known device (the structure in Lee's Figure 35) in the same way (vertically stacking memory devices using SOI technology). In addition, in my opinion, the combination would have amounted to applying a known technique (Aspar's Smart-Cut® process) to address the same known problem recognized by both Lee and Aspar (fabricating 3D structures) using prior art elements according to their established functions (Aspar's Smart-Cut® process and Lee's Figure 35 memory device using the memory cell structures of Figure 1A, 1B, 2, 7, or 25A).

213. In my opinion, a POSITA would have also recognized that Aspar's Smart-Cut® process as compared to monolithic deposition allows for more efficient quality control at the layer formation stage. Specifically, when using Smart-Cut®, quality control can be performed on the stack prior to bonding (e.g., layer thickness, uniformity, etc.). If a quality issue is detected, then only that stack would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded. Testing layers of devices prior to stacking has well-known benefits. For example, Fung explains that, while "stacking chips is definitely the preferred approach for attaining 3d-IC," yield loss could be "very large" because reduced yield on stacked wafers multiplies yield loss. Exhibit 1016, 1:33–47 ("Assuming a 70% yield for each finished wafer, by stacking two wafers, the maximum yield achievable

is 49% (i.e., 0.7×0.7)”). Fung explains the solution to this problem is to test each wafer before stacking “to screen out defective ones.” *Id.*, 1:48–52. Thus, Aspar’s Smart-Cut® process minimizes waste resulting from defects detected in quality control. In addition, a POSITA would have recognized that forming electrical devices on one substrate separately from the memory devices on another substrate would have allowed optimization of the respective processes rather than forcing the memory devices to be formed with a sub-optimal process tailored to preserving the electrical devices formed on the single wafer in the monolithic process.

214. In my opinion, a POSITA would have had a reasonable expectation of success in using Aspar’s Smart-Cut® process to wafer bond bottom level 3104 (“stackable add-on layer”) to interlayer insulating layer 3102 (“dielectric layer”) of Lee’s Figure 35. Lee’s substrate 3105 with driver circuits 3103 therein and insulating layer 3102 on top is suitable for use with SOI technology such as Aspar’s Smart-Cut® process to add a stackable add-on layer. *Compare* Exhibit 1007, ¶¶111–208, *with* Exhibit 1009, 834, 837 (“major application of this process is...fabrication SOI wafers”), 839. In addition, the Smart-Cut® process was understood as a predictable process at the relevant time, and had been used, for example, to transfer SOI stacks and with metallic bonding layers. *Id.* (citing Exhibit 1009, 838–839) (demonstrating applicability of Smart-Cut® to various structures and materials). Further, a POSITA would have recognized Aspar’s process for transferring thin monocrystalline layers

as compatible with Lee, which discusses using single crystal silicon for the thin film transistor (TFT) pillars of its memory cells. *Id.* (citing Exhibit 1009, 834); Exhibit 1007, ¶¶119, 139.

215. Alternatively, Aspar teaches repeated transfers of single layers (each a stackable add-on layer of the one or more stackable add-on layers encompassed by 13[b]). Exhibit 1009, 838–839. Those single layers would be transferred to a holding wafer and then wafer bonded as a stack to the dielectric, or each individual layer would be bonded to Wafer B in a series of wafer bonding steps. *E.g.*, Exhibit 1024, 134 (discussing the Smart-Cut® SOI process) (“Realizing multiple SOI layers based on a layer transfer process can be achieved in many different ways: repeating a single layer transfer several times onto a SOI wafer initially obtaining, transferring onto a single substrate or a SOI wafer whole SOI layers stacks already formed.”). The conductive layer, including silicon (*see* Exhibit 1007, ¶126) or other conductive material, would be transferred as a single layer to the holding wafer or bonded to Wafer B, deposited on the stack of the holding wafer prior to bonding, or deposited on another single layer for bonding with that layer to Wafer B. The motivation to combine and reasonable expectation of success analyses I discuss above would apply equally for these combinations.

c. 13[d]

216. For the same reasons I discuss in Section X.A.2.e above, in my opinion, Lee discloses or suggests 13[d].

2. Claims 14–17

217. Lee discloses the elements of claims 14-17 as I discuss above in Sections X.A.3–X.A.6. Additionally, Section X.E.1.b describes that the stackable add-on layer is added using Aspar’s Smart-Cut® process which is SOI technology. Exhibit 1009, 834, 837 (“major application of this process is...fabrication SOI wafers”), 839. As described in that Section, the doped stack of the stackable add-on layer bonded to Wafer B is used to form pillars (“SOI pillars”) for the memory cell structures of Lee’s Figure 1A, 1B, 2, 7, or 25A.

F. Ground 1F: Obviousness over Lee, Aspar, and Endoh (claims 16–17)

218. In my opinion, Lee and Endoh render obvious claims 16 and 17 under PO’s apparent constructions as I discuss above in Section X.B. Under the proper constructions of “stackable add-on layer” and “SOI pillar,” in my opinion, claims 16 and 17 would have been obvious over Lee, Aspar, and Endoh. The description of the Lee-Aspar combination (see Section X.E), the description of the Lee-Endoh combination (see Section X.B), and the motivation to combine and reasonable expectation of success discussion for the Lee-Aspar (see Section X.E.1.b) and Lee-Endoh (see Section X.B.1) combinations apply equally to this ground.

219. Additionally, in Section X.E.1.b, I describe that the stackable add-on layer is added using Aspar's Smart-Cut® process which is SOI technology. Aspar, 834, 837 (“major application of this process is... fabrication SOI wafers”), 839. As I discuss in Section X.E.1.b, the doped stack of the stackable add-on layer bonded to Wafer B is used to form the pillars (“SOI pillars”) for the memory cell structures of Lee's Figure 1A, 1B, 2, 7, or 25A. In my opinion, a POSITA would have also found it obvious to form a suitable doped stack of the stackable add-on layer added using SOI technology to form SOI pillars with two memory cells as taught in Endoh for the same reasons described in Sections X.B.1 and X.B.2.

G. Ground 2A: Obviousness over Johnson (Claim 13)

220. As discussed above in Section IX.A, I have been asked to assume that Patent Owner may argue that “the stackable add-on layer being bonded” encompasses any type of layer that is directly or indirectly adhered to the “dielectric layer.” Such a construction is not supported by the intrinsic evidence, and is not consistent with how a POSITA would have understood “the stackable add-on layer being bonded” in the context of claim 13. Nevertheless, under such a construction, in my opinion, claim 13 would have been obvious over Johnson for the reasons discussed below.

1. Claim 13

a. 13[pre]: “A semiconductor memory structure, comprising:”

221. To the extent the preamble is limiting, in my opinion, Johnson discloses or suggests a “semiconductor memory structure.” Specifically, Johnson discloses a “low cost, high density semiconductor memor[y].” Exhibit 1010, 1:7–12, 5:41–45, 6:52–56, 7:49–61, Fig. 4(a).

b. 13[a]: “a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices”

222. In my opinion, Johnson discloses or suggests 13[a], which recites (1) “a substrate having electrical devices formed therein,” and (2) “a dielectric layer disposed above the electrical devices.”

223. I note that the '702 Patent defines the term “device” as “active and passive circuit elements,” including, but not limited to “FETs (n-channel and p-channel), Thyristor[s], capacitors, varactors, floating gates, charge trap layers, diodes, and resistors.” '702 Patent, 4:28–34. In addition, the incorporated '941 Patent defines “device” as “one or more circuit elements that have characteristics that are voltage variant,” including, but not limited to, “FETs (n-channel and p-channel), diodes, and varactors.” '941 Patent, 5:51–54, 59–60.

224. Regarding “a substrate having electrical devices formed therein,” Johnson teaches an array of memory cells that “may be fabricated above a silicon

substrate, with decoders and I/O circuitry formed [] in the substrate.” Exhibit 1010, 4:17–22. Johnson further teaches that the “substrate beneath the memory cell array ... may be used to ... lay[] out substantial portions of the row decoders, column decoders, I/O multiplexors, and read/write circuits.” *Id.*, 7:11–18. Johnson also teaches “a wafer that may have received prior processing steps, for example, CMOS transistors may be fabricated in the monocrystalline substrate for the peripheral circuitry.” *Id.*, 13:26–35.

225. In my opinion, “CMOS transistors” are “electrical devices” as the ’702 Patent defines them (i.e., “active circuit elements,” namely, those having power gain). This is in contrast to passive circuit elements such as resistors, capacitors and inductors which do not have power gain. Further, a POSITA would have known that “CMOS transistors” are types of “FETs” or MOSFETs, which the ’702 Patent and incorporated ’941 Patent each provide as an example of a “device” (’702 Patent, 4:28–34; ’941 Patent, 5:51-54, 59-60). A POSITA would have understood that Johnson’s “decoders,” “I/O multiplexors,” and “read/write circuits” are formed from CMOS transistors and hence are formed from electrical devices. Accordingly, Johnson teaches “a substrate having electrical devices formed therein.”

226. Regarding “a dielectric layer disposed above the electrical devices,” Johnson discloses fabrication starting with a wafer having devices in the substrate and “[a]n insulator then is deposited, and preferably, planarized (using chemical-

mechanical polishing ('CMP'), resist etchback planarization, or any of a number of other technologies for planarization)." Exhibit 1010, 13:26–35. Johnson further teaches the "fabrication sequence for the memory cell" depicted in Figures 6(b)-6(g) involves "deposition and planarization of an interlevel dielectric." *Id.*, 12:42–54. In my opinion, these disclosures when read together teach a dielectric layer deposited onto a substrate containing electrical devices. Accordingly, Johnson teaches "a dielectric layer disposed above the electrical devices" in a substrate.

227. In my opinion, Johnson discloses or suggests 13[a].

c. 13[b]: "a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells"

228. In my opinion, under PO's apparent construction of "stackable add-on layer," Johnson discloses or suggests 13[b].

229. First, Johnson discloses "vertically oriented semiconductor memory cells." The '702 Patent states: "The term 'vertical,' as used herein, means substantially perpendicular to a major surface of a substrate, such as, for example, a semiconductor wafer." '702 Patent, 4:6–8. Figure 4(a) (which I have reproduced and annotated below) depicts one embodiment where elements of the memory cell "are stacked vertically in a 'pillar' shaped arrangement" with current also flowing vertically. Exhibit 1010, Fig. 4(a), 1:7-12, 2:33-37, 4:30-51, 5:30-42, 5:66–6:7

(“[T]he steering element 22 and the state change element 23 are stacked vertically in a ‘pillar’ shaped arrangement...The pillar is vertical and so is the current flow.”).

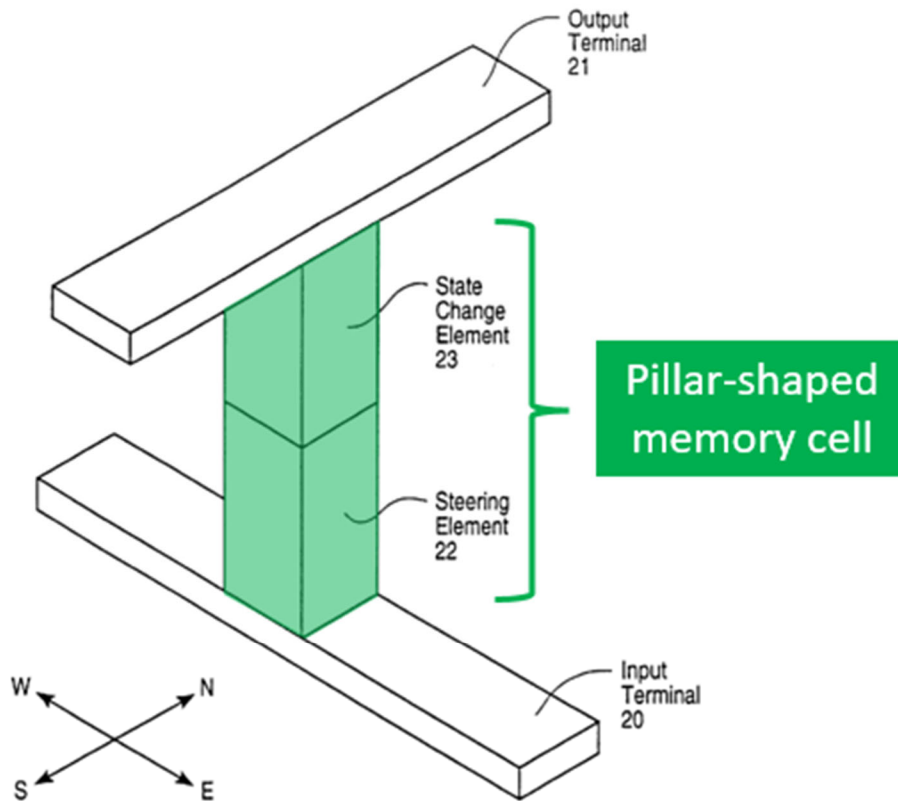


FIG. 4(a)

230. Additionally, Johnson discloses “[a] unique organization of these cells in a three dimensional memory array disposed above a substrate.” Exhibit 1010, 5:38–40. The memory cells “can be stacked vertically in numerous layers to form a three dimensional array.” *Id.*, 5:30–37. The invention described in Johnson “stacks multiple levels of memory cells above one another.” *Id.*, 11:10–11. Figure 5 (which

I have reproduced and annotated below) shows an exemplary three dimensional memory array with each layer having two memory cell pillars (27 in Layer 1). *Id.*, 6:63–7:10, 11:10-25, Fig. 5.

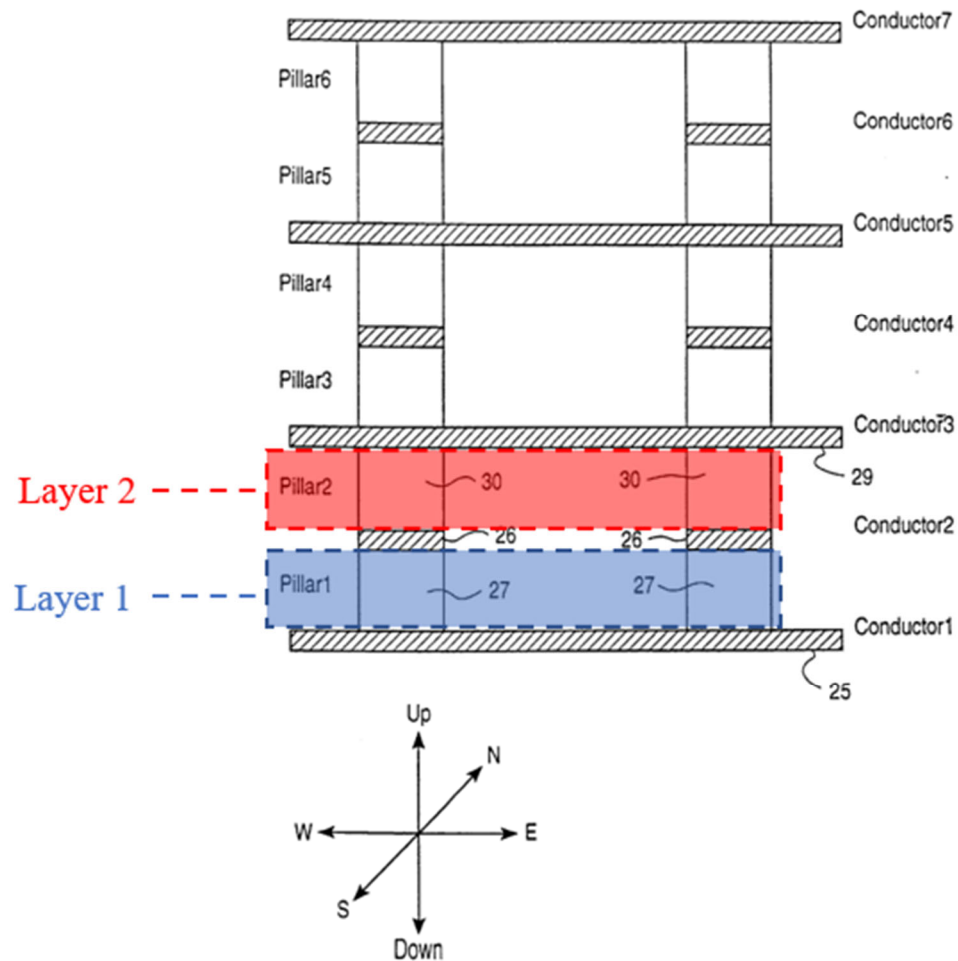


FIG. 5

In my opinion, bottom layer 1 shown in Johnson’s Figure 5 (with or without Conductor1) teaches a “stackable add-on layer” having a plurality of vertically-oriented semiconductor memory cells under PO’s apparent construction.

231. For the foregoing reasons, in my opinion, Johnson discloses or suggests 13[b].

d. 13[c]: “the stackable add-on layer being bonded to the dielectric layer”

232. Under PO’s apparent construction of this limitation (with which I disagree as discussed above), Johnson discloses or suggests this limitation.

233. Johnson teaches a fabrication method comprising a series of deposition and etching steps in Figures 6(b)-6(g). Exhibit 1010, 12:42–65. The fabrication process starts with an insulator deposited and planarized on a wafer. *Id.*, 13:26–35. As I discuss in Section X.A.2.b, a POSITA would have understood that an insulating layer is a “dielectric layer.” Next, a conductor layer followed by the materials to create the memory cell, referred to as the “layer stack” (*id.*, 12:8–10), are deposited as illustrated in Figure 6(b), which I have reproduced and annotated below (*id.*, 13:26–35).

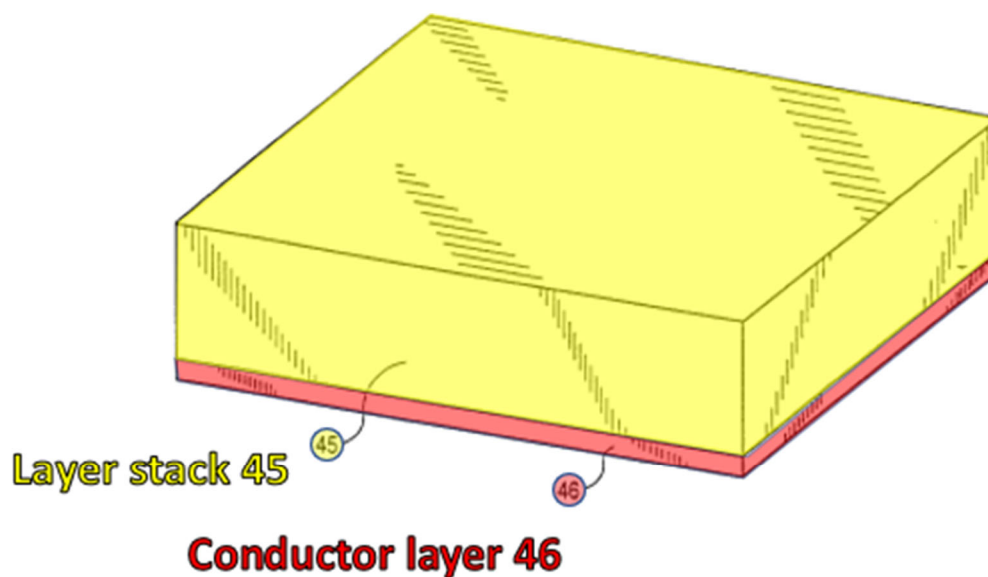


FIG. 6(b)

234. Next, Figure 6(c) below illustrates the result of an etching step applied to the layer stack. *Id.*, 13:36–41.

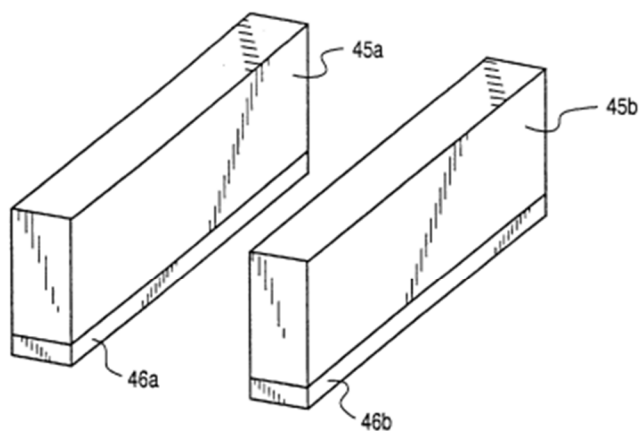


FIG. 6(c)

235. Following the etch step, another conductor layer 50 and layer stack 51 are deposited as illustrated in Figure 6(d) below. *Id.*, 13:58–60.

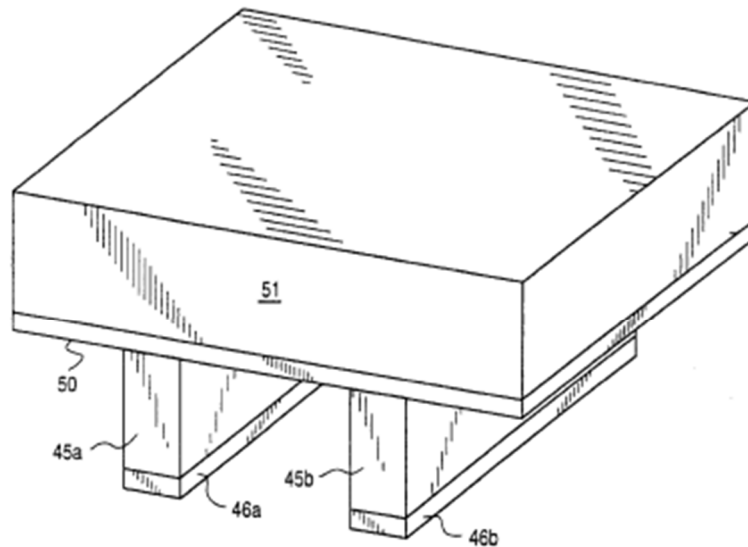


FIG. 6(d)

236. Next, Figure 6(e) (which I have reproduced below) illustrates the result of another etching step that forms four pillars in the bottom layer (45a1, 45a2, 45b1, 45b2). *Id.*, 13:64–14:4. In my opinion, a POSITA would have understood that this bottom layer (with or without conductors 46a, 46b) corresponds to the bottom layer shown in Figure 5 (above) (“stackable add-on layer”).

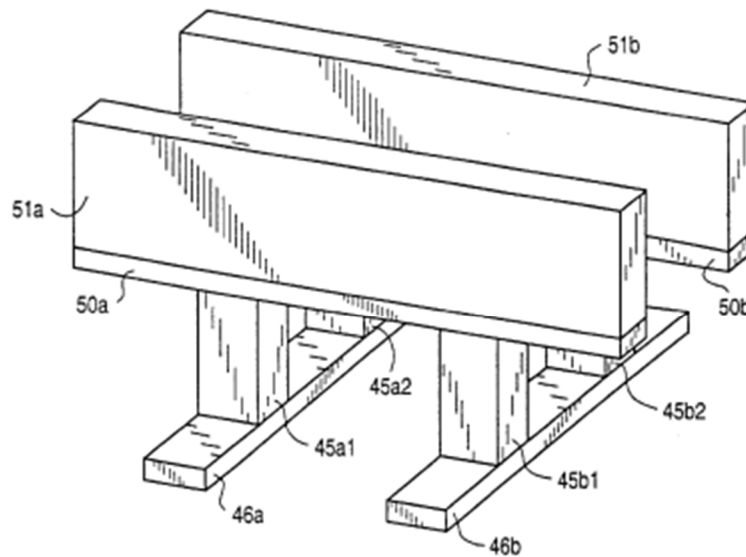


FIG. 6(e)

237. Thus, Johnson teaches a stackable add-on layer monolithically grown from the insulator or “dielectric layer” via a series of deposition and etching steps. As such, in my opinion, Johnson discloses or suggests that the stackable add-on layer (bottom layer 1 shown in Johnson’s Figure 5 (with or without Conductor1)) is directly or indirectly adhered to the dielectric layer (PO’s apparent construction).

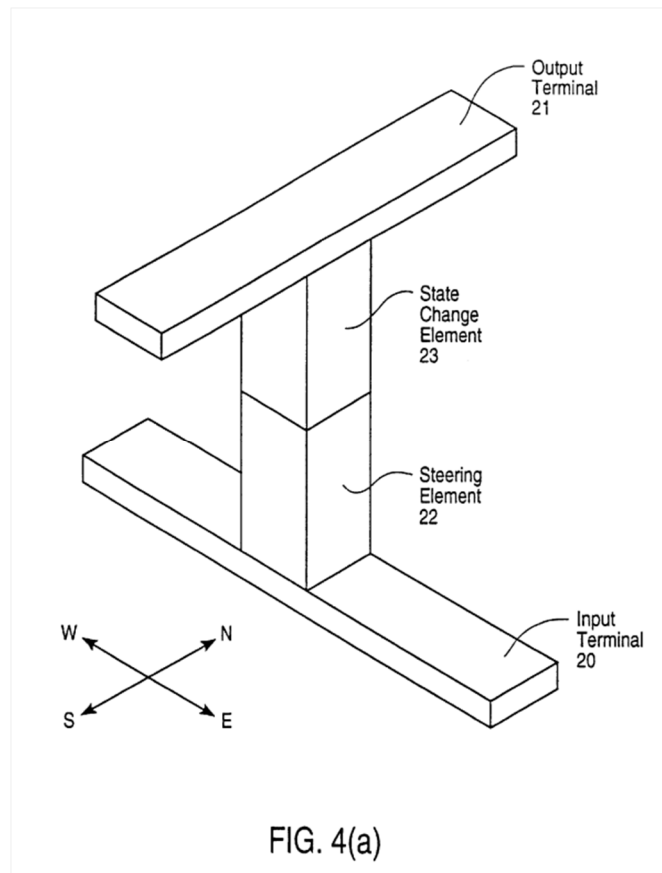
238. For the reasons discussed above, in my opinion, under PO’s apparent construction, Johnson discloses or suggests 13[c].

e. 13[d]: “wherein the memory cells are nonvolatile memory cells having at least one transistor”

239. In my opinion, Johnson discloses or suggests 13[d], which recites “wherein the memory cells are nonvolatile memory cells having at least one

transistor.” First, Johnson discloses nonvolatile memory cells. *See, e.g.*, Exhibit 1010, Title (“Vertically stacked field programmable nonvolatile memory and method of fabrication”); *id.*, 1:7–12 (“This invention relates to low cost, high density semiconductor memories and, in particular, to semiconductor memories whose contents are ‘nonvolatile’”); *Id.*, 9:59–62 (“The invented memory cell can be embodied either as a one-time programmable nonvolatile memory, or as a write/erase/rewrite nonvolatile memory”).

240. Johnson also discloses that each nonvolatile memory cell has at least one transistor. Figure 4(a) (below) illustrates one embodiment of the memory cell. Exhibit 1010, 5:41–49, Fig. 4(a).



241. Steering element 22 can be implemented using: “(i) a PN junction diode, in amorphous, microcrystalline, polycrystalline or single crystal semiconductor (e.g. Si, Ge, SiGe, GaAs, InP, etc.); (ii) a metal-semiconductor Schottky diode; (iii) *a junction field-effect transistor with gate connected to source (or to drain)*; (iv) *a MOSFET with gate either floating, or connected to source or connected to drain*; (v) a Zener diode, avalanche diode, or tunnel diode; (vi) a four-layer diode (SCR); (vii) a P-I-N diode in amorphous, microcrystalline, polycrystalline or single crystal semiconductor; and others that will be readily apparent to those skilled in the art.” *Id.*, 7:61–8:5 (emphases added).

242. In my opinion, a person of ordinary skill in the art would have understood the steering element 22 of the nonvolatile memory cell disclosed in Johnson to have at least one transistor because Johnson expressly discloses such implementations. Exhibit 1010, 7:61–8:5.

243. In my opinion, Johnson discloses or suggests 13[d].

H. Ground 2B: Obviousness over Johnson and Kim (Claim 13)

244. As discussed above, in the context of the intrinsic record of the '702 Patent, a person of ordinary skill in the art would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the “stackable add-on layer” is wafer bonded to “the dielectric layer.” Under this proper construction, in my opinion, claim 13 would have been obvious over Johnson and Kim for the reasons discussed below.

1. Claim 13

a. 13[pre]-13[b]

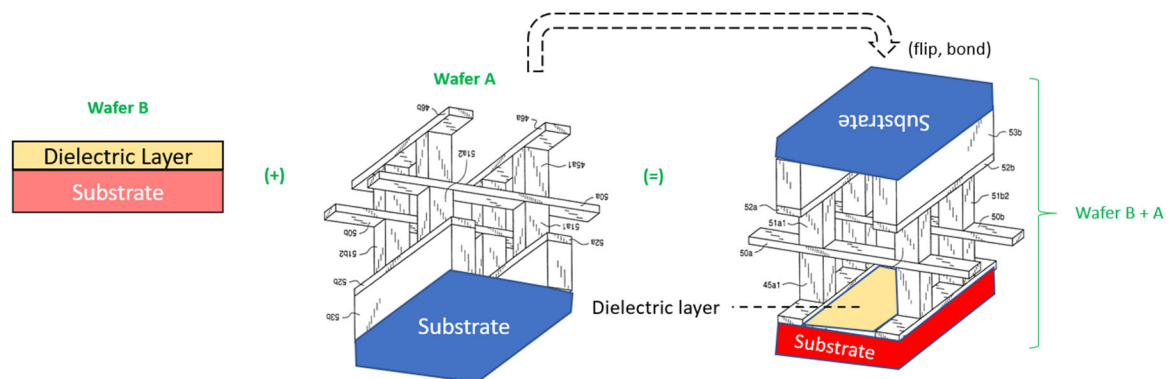
245. For the same reasons I discussed above, in my opinion, Johnson discloses or suggests 13[pre]-13[b].

b. 13[c]: “the stackable add-on layer being bonded to the dielectric layer”

246. Under the proper construction of “the stackable add-on layer being bonded,” in my opinion, the combination of Johnson and Kim teaches this limitation. Although Johnson discloses a series of deposition and etching steps as discussed

above in Section X.G.1.d, in my opinion, a POSITA would have been motivated to use Kim's wafer bonding techniques when fabricating Johnson's structure for the reasons explained below. Kim's wafer stacking and bonding technique is discussed above in Section X.C.1.b.

247. The figures I have created below illustrate one way a POSITA would have found it obvious to apply Kim's teachings in Johnson.



248. As shown above, Johnson's separately fabricated memory cells (e.g., from Johnson's Figure 6(e)) would be formed on their own substrate ("Wafer A"). Wafer A would be flipped and bonded to Wafer B having Johnson's "decoders," "I/O multiplexors," "read/write circuits," and/or "CMOS transistors" ("electrical devices") and insulating layer ("dielectric layer"). Exhibit 1008, ¶20. In the combination, as in Kim Figure 1 where wafer 120 is bonded to wafer 110 using a dielectric layer 102, Johnson's level of memory cells ("stackable add-on layer") would be wafer bonded to Johnson's insulating layer ("dielectric layer").

249. In my opinion, a POSITA would have been motivated to wafer bond Johnson's layer of memory cells ("stackable add-on layer") to its insulating layer ("dielectric layer") based on Kim's teachings. In my opinion, a POSITA would have recognized that using wafer-bonding to bond Johnson's level of memory cells ("stackable add-on layer") to its insulating layer ("dielectric layer") would have been a predictable way to non-monolithically build Johnson's 3D structure. Specifically, in my opinion, a POSITA would have viewed this modification as consisting of nothing more than using a known technique (Kim's wafer bonding) to improve a similar known device (Johnson's structure) in the same way (logic/memory stacking using a wafer bonding process). In addition, in my opinion, the combination would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Johnson and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Johnson's structure).

250. In my opinion, a POSITA would have also recognized that wafer-bonding Johnson's level of memory cells to its insulating layer, as compared to monolithic deposition, allows for more efficient quality control with less potential waste. Specifically, a POSITA would have recognized that quality control can be performed on the memory cells (e.g., testing for shorts). If a quality issue is detected,

then only that level would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited layer stacks, etc.) would need to be discarded. Testing layers of devices prior to stacking has well-known benefits. For example, Fung explains that, while “stacking chips is definitely the preferred approach for attaining 3d-IC,” yield loss could be “very large” because reduced yield on stacked wafers multiplies yield loss. Exhibit 1016, 1:33-47 (“Assuming a 70% yield for each finished wafer, by stacking two wafers, the maximum yield achievable is 49% (i.e., 0.7×0.7)”). Fung explains the solution to this problem is to test each wafer before stacking “to screen out defective ones.” *Id.*, 1:48-52. Thus, Kim’s wafer-bonding process minimizes waste resulting from defects detected in quality control. In addition, a POSITA would have recognized that forming electrical devices on one substrate separately from the memory devices on another substrate would have allowed optimization of the respective processes rather than forcing the memory devices to be formed with a sub-optimal process tailored to preserving the electrical devices formed on the single wafer in the monolithic process.

251. In my opinion, a POSITA would have had a reasonable expectation of success in using wafer bonding to attach Johnson’s layer of memory cells to its insulating layer because Kim shows that using such a technique to bond one wafer

with electrical devices to another wafer with memory cells was within the skill of a POSITA. Exhibit 1008, ¶¶19, 20.

c. 13[d]: “wherein the memory cells are nonvolatile memory cells having at least one transistor”

252. For the same reasons discussed above in Section X.G.1.e, in my opinion, Johnson discloses or suggests this limitation.

I. Ground 2C: Obviousness over Johnson and Aspar (Claim 13)

253. As discussed in Section IX.A, a POSITA would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the “stackable add-on layer” is wafer bonded to “the dielectric layer.” Under this proper construction, in my opinion, claim 13 would have been obvious over Johnson in view of Aspar for the reasons discussed below.

1. Claim 13

a. Claim[pre]-13[b]

254. For the same reasons discussed in Sections X.G.1.a–X.G.1.c above, in my opinion, Johnson discloses or suggests 13[pre]–13[b].

b. Claim 13[c]

255. Under the proper construction of “the stackable add-on layer being bonded” as requiring that the “stackable add-on layer” is wafer bonded to “the

dielectric layer,” as discussed above in Section IX.A, in my opinion, the combination of Johnson with Aspar teaches this limitation.

256. As discussed above in Section X.E.1.b, Aspar discloses a wafer bonding technique called the Smart-Cut® process that transfers a thin monocrystalline layer of “very good thickness homogeneity and with a high crystalline quality.” Exhibit 1009, 834. The Smart-Cut® process is a generic process that is compatible with conductive (metallic) bonding layers and can be used “to realize complex structures,” including by “transferring SOI layer stacks already formed onto a single substrate or a SOI wafer.” *Id.*, 838–839.

257. In the combination, Aspar’s Smart-Cut® wafer bonding process would be used to bond Johnson’s layer of memory cells to its insulating layer. Wafer B would consist of Johnson’s “silicon substrate, with decoders and I/O circuitry formed either in the substrate or in thin film transistors above the substrate” and a dielectric layer deposited on top of the substrate. Exhibit 1010, 4:19–22, 12:42–54, 13:26–35. Wafer A would have a thin single crystal film with a doped stack, similar to the layer stack depicted in Johnson Figures 6(a) and 6(b) which I have annotated and created below.

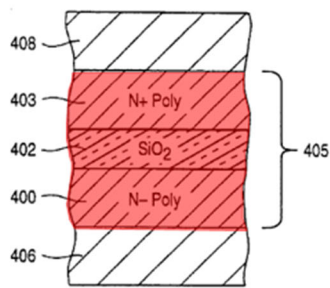


FIG. 6(a)

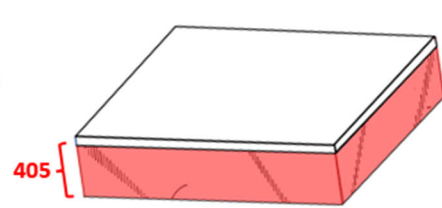
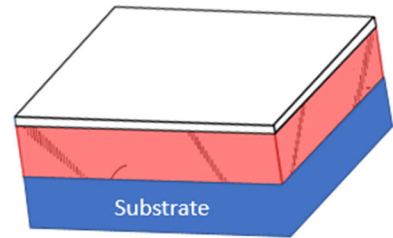
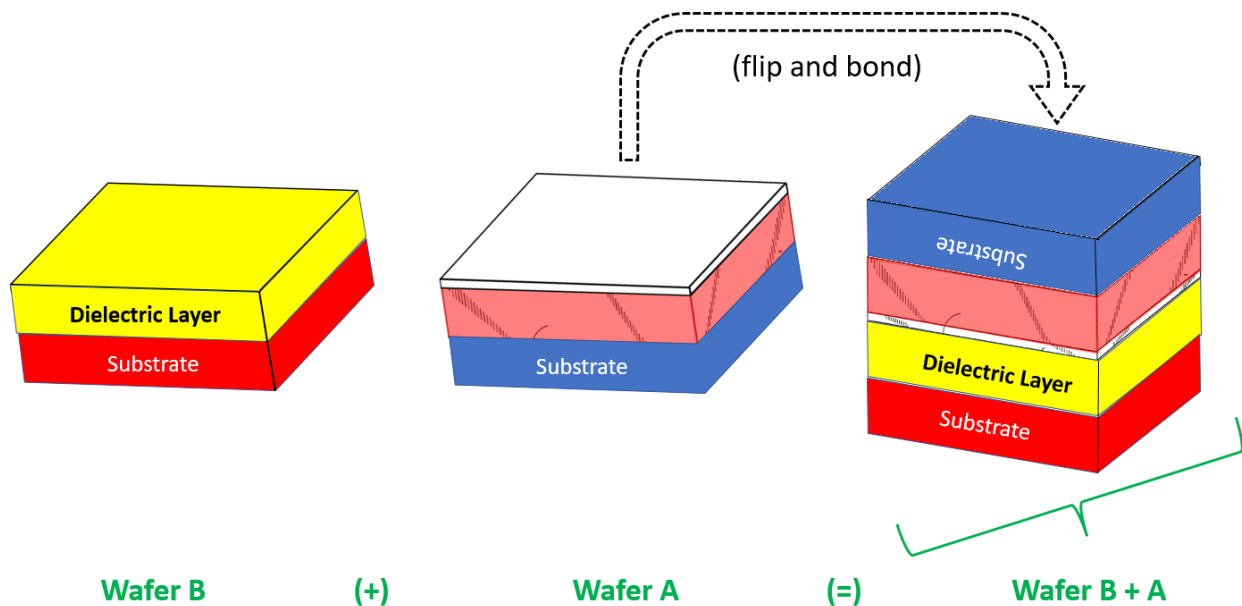


FIG. 6(b)
(inverted)



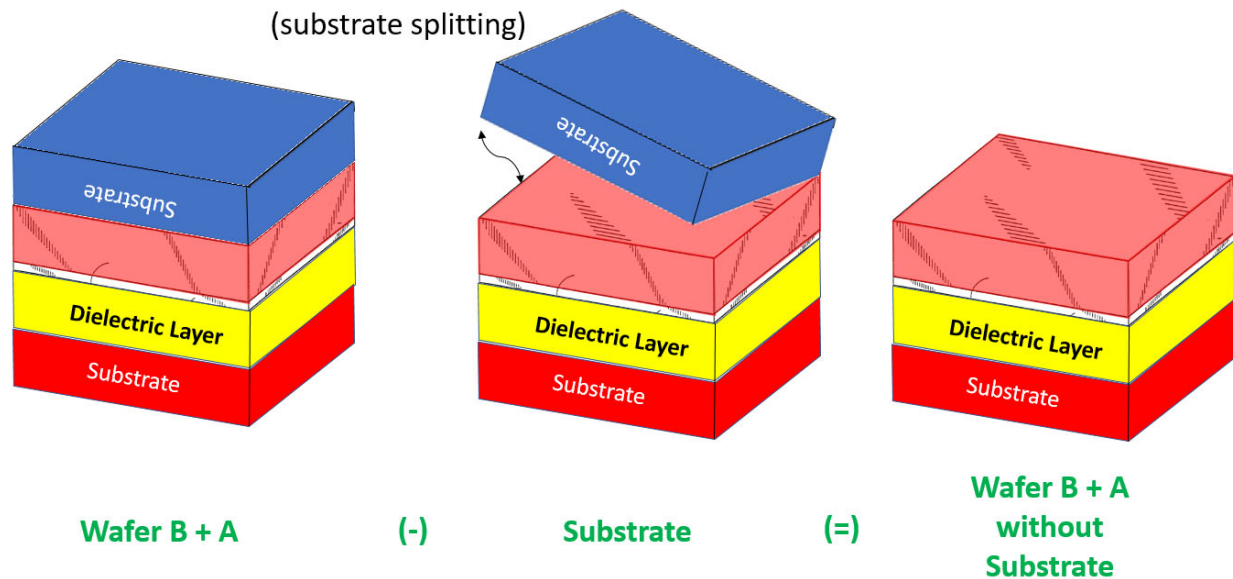
Wafer A

258. After the layers on Wafer A were formed, Wafer A would be flipped upside down and bonded to Wafer B. This process is depicted in the annotated series of figures I have created below:



259. After bonding, a splitting (i.e., cleaving) step would be performed, resulting in the transfer of the desired thin layer (e.g., the doped stack) and

conductive layer from Wafer A onto Wafer B. This process is depicted in the annotated series of figures below:



260. In my opinion, a POSITA would have been motivated to use Aspar’s Smart-Cut® process to wafer bond a layer of semiconductor pillars as depicted in Johnson’s Figures 6(a)-6(b) (“stackable add-on layer”) to the insulating layer above the substrate (“dielectric layer”). Aspar itself teaches that Smart-Cut® “[r]ealiz[es] multiple SOI layers based on a layer transfer process ... [such as] transferring SOI layers stacks already formed onto a single substrate or a SOI wafer. So multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology.” EX1009, 839. In addition, the Smart-Cut® process was known to have several advantages including “transferring thin layers of very good thickness homogeneity and with a high crystalline quality.” *Id.*, 834. In my opinion, this combination merely amounts

to using a known technique (Aspar's Smart-Cut® process) to improve a similar known device (Johnson's structure) in the same way (vertically stacking memory devices using SOI technology). In addition, in my opinion, the combination would have amounted to applying a known technique (Aspar's Smart-Cut® process) to address the same known problem recognized by both Johnson and Aspar (fabricating 3D structures) using prior art elements according to their established functions (Aspar's Smart-Cut® process and Johnson's structure).

261. In my opinion, a POSITA would have also recognized that Aspar's Smart-Cut® process as compared to monolithic deposition allows for more efficient quality control at the layer formation stage. Specifically, when using Smart-Cut®, quality control can be performed on the layer stack prior to bonding (e.g., layer thickness, uniformity, etc.). If a quality issue is detected, then only that layer stack would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited layer stacks, etc.) would need to be discarded. Testing layer of devices prior to stacking has well-known benefits. For example, Fung explains that, while "stacking chips is definitely the preferred approach for attaining 3d-IC," yield loss could be "very large" because reduced yield on stacked wafers multiplies yield loss. Exhibit 1016, 1:33-47 ("Assuming a 70% yield for each finished wafer, by stacking two wafers, the maximum yield achievable is 49% (i.e., 0.7×0.7)"). Fung explains the solution to

this problem is to test each wafer before stacking “to screen out defective ones.” *Id.*, 1:48-52. Thus, Aspar’s Smart-Cut® process minimizes waste resulting from defects detected in quality control. In addition, a POSITA would have recognized that forming electrical devices on one substrate separately from the memory devices on another substrate would have allowed optimization of the respective processes rather than forcing the memory devices to be formed with a sub-optimal process tailored to preserving the electrical devices formed on the single wafer in the monolithic process.

262. In my opinion, a POSITA would have had a reasonable expectation of success in using Aspar’s Smart-Cut® process to wafer bond a layer of semiconductor pillars as depicted in Figures 6(a)-6(b) (“stackable add-on layer”) to the insulating layer above the substrate (“dielectric layer”). In addition, the Smart-Cut® process was understood as a predictable process at the relevant time, and had been used, for example, to transfer SOI layer stacks and with metallic bonding layers. Exhibit 1009, 838-839 (“The flexibility of this process can be used to realize complex structures...Realizing multiple SOI layers based on a layer transfer process can be achieved in many different ways: repeating a single layer transfer several times onto a same wafer, transferring SOI layers stacks already formed onto a single substrate or a SOI wafer.”), 839 (“[T]he Smart-Cut process really is a generic process. It allows a great deal of combinations (material and bonding layer) which

open up new scope for development.”)). Further, in my opinion, a POSITA would have recognized Aspar’s process for transferring thin monocrystalline layers as compatible with the types of memory cells in Johnson (e.g., a MOSFET with gate either floating, or connected to source or connected to drain (steering element) with, e.g., polysilicon resistor-fuse (state change element)). Exhibit 1010, 7:49–51, 7:67–8:1, 8:46–55; Exhibit 1009, 834; Exhibit 1007, ¶¶127, 139.

c. Claim 13[d]

263. For the same reasons discussed in Section X.G.1.e above, in my opinion, Johnson discloses or suggests this limitation.

J. Ground 3: Obviousness over Park and Kim (Claim 1)

264. Under either construction of “the stackable add-on layer is bonded” as discussed in Section IX.A, in my opinion, claim 1 would have been obvious over Park and Kim for the reasons discussed below.

1. Park

265. Park teaches a “vertically structured transistor” that is “especially suitable for manufacturing a semiconductor memory device.” Exhibit 1011, Abstract, 2:11–14. More specifically, Park’s vertically structured transistor “comprises a silicon pillar serving as a channel region. The silicon pillar is extended in a perpendicular (vertical) direction with respect to a semiconductor substrate and is surrounded by an insulating film.” *Id.*, 2:16–21. Park further teaches “vertically

forming the transistor on the capacitor and [] vertically forming the bitline contact hole on the transistor.” *Id.*, 2:51–56. Park’s vertically structured memory cell occupies a “remarkably reduced” area, which enables “increased integration” of semiconductor devices. *Id.*, 2:7–10, 2:46–56. Park further teaches that its vertically structured memory cell may be a DRAM cell. *Id.*, 5:20–24.

2. Claim 1

a. 1[pre]: “A semiconductor memory structure”

266. To the extent the preamble is limiting, in my opinion, the combination of Park and Kim discloses or suggests this limitation. Park discloses “a semiconductor memory device,” Exhibit 1011, 2:11–14, and more specifically a DRAM cell, *id.*, 5:20–24. A POSITA would understand a DRAM cell alone to be a “semiconductor memory structure.” Kim further discloses integrating memory devices with “one or more microprocessors.” Exhibit 1008, ¶20. In my opinion, a person of ordinary skill in the art would have understood Kim’s wafer stack including one or more microprocessors in combination with Park’s DRAM cells to also be “a semiconductor memory structure.” Further, in my opinion, a person of ordinary skill in the art would have been motivated to combine those teachings for the reasons discussed herein.

267. In my opinion, a POSITA would have been motivated to make this combination. Park discloses vertically structured DRAM cells that enable “increased

integration.” Exhibit 1011, 2:7–10. Kim’s teachings are discussed in Section X.C.1.b. Kim further explains that an advantage of “vertically stacking many layers of active IC devices such as processors, programmable devices and memory devices inside a single chip [is] to shorten average wire lengths, thereby reducing interconnect RC delay and increasing system performance.” Exhibit 1008, ¶¶7, 22. In my opinion, a POSITA would have been motivated to vertically stack, through wafer bonding, Park’s DRAM memory cells on top of logic devices, e.g., one or more microprocessors, based on Kim’s teachings because the combination would have furthered Park’s and Kim’s express goal of increasing integration, and resulted in Kim’s advantage of reducing interconnect RC delay and increasing system performance. *Id.*

268. In my opinion, integrating Park’s DRAM memory cells with logic per Kim’s teachings would have been no more than applying a known technique (Kim’s 3D wafer stacking of logic and memory cells) to a known device ready for improvement (Park’s vertically structured DRAM cells) to yield predictable results (increased performance through logic/memory stacking). In my opinion, it would have further been a simple substitution of one known element (Park’s DRAM) for another (Kim’s memory cells) to yield predictable results (increased integration of memory devices wafer bonded to logic). In addition, in my opinion, the combination would have amounted to applying a known technique (Kim’s wafer bonding) to

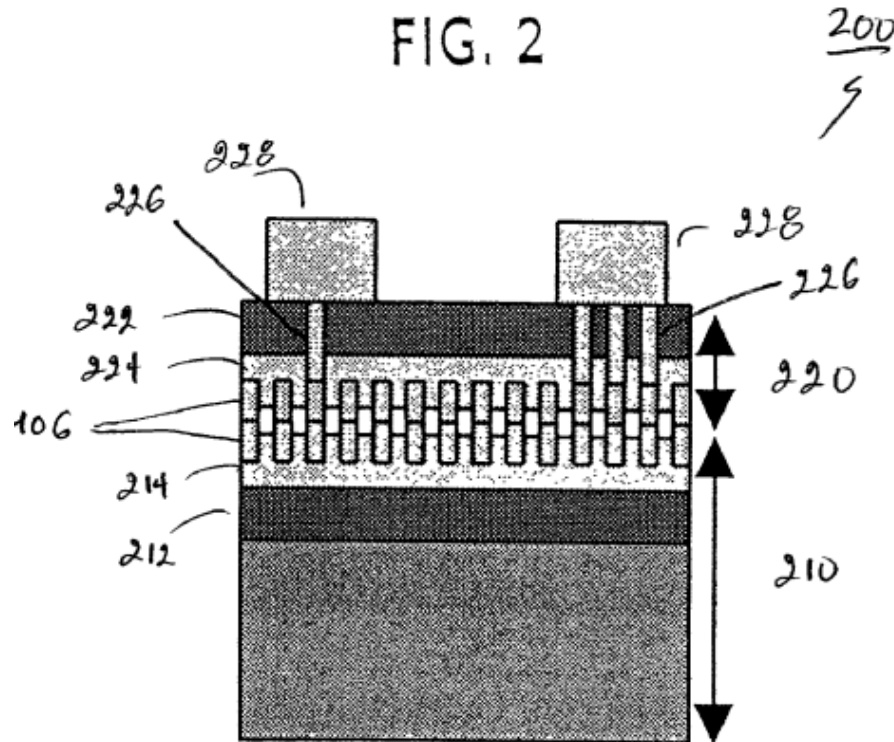
address the same known problem recognized by both Park and Kim (fabricating 3D memory arrays) using prior art elements according to their established functions (Park's and Kim's structures).

269. In my opinion, a POSITA would have further had a reasonable expectation of success in employing Kim's 3D wafer stacking with Park's vertically-oriented DRAM cells because the teachings of both Park and Kim would have been employed for their intended purposes. Further, Kim shows that the combination was within the skill of a POSITA because Kim wafer bonds one wafer with electrical devices to another wafer with memory cells. Exhibit 1008, ¶¶19, 20.

b. 1[a]: “a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate”

270. In my opinion, the combination of Park and Kim discloses or suggests this limitation. Kim discloses a “3D wafer-to-wafer vertical stack,” where, for example, the bottom wafer of a stack may include “one or more microprocessors” and the second wafer includes “one or more memory devices” Exhibit 1008, ¶20. Kim then provides a more detailed description of an exemplary two-wafer vertical stack wherein “bottom silicon (Si) wafer 210 may include an active silicon (Si) layer 212 supporting one or more active IC devices (not shown) and an interlayer dielectric (ILD) layer 214.” *Id.*, ¶23. In my opinion, a POSITA would have thus understood

that Figure 2 merely provides a more detailed view of a two-wafer stacks per Kim's teachings. Kim's two-wafer vertical stack is illustrated in its Figure 2:



271. In my opinion, a person of ordinary skill in the art would have understood Kim's first wafer 210 including "active silicon (Si) layer 212 supporting one or more active IC devices (not shown)" to be "a substrate having electrical devices formed therein."

272. Kim further explains that the wafers are "bonded via a metal bonding layer 106 deposited on opposing surfaces of the bottom wafer 210 and the top wafer 220 at designated bonding areas to establish electrical connections between active IC devices on vertically stacked wafers 210 and 220 and to bond adjacent wafers 210 and 220, while maintaining electrical isolation between bonding areas via ILD

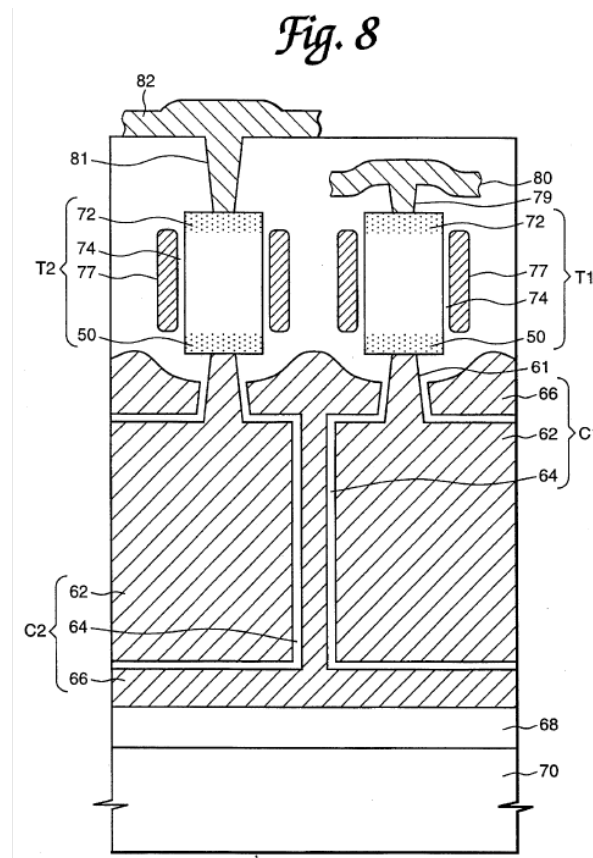
[interlayer dielectric] layers 214 and 224.” Exhibit 1008, ¶23. In my opinion, a person of ordinary skill in the art would have understood Kim’s ILD layer 214 to be the claimed “at least one dielectric layer” and Kim’s metal bonding layer 106 to teach “at least one interconnect layer,” both of which are disposed above the substrate (i.e., Kim’s active silicon layer 212). In my opinion, a person of ordinary skill in the art would have been motivated to combine Kim’s teachings discussed above with Park for the reasons discussed above.

- c. **1[b]: “a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material”**

273. In my opinion, the combination of Park and Kim discloses or suggests this limitation. Kim discloses wafer bonding a second wafer including an active silicon layer 222 with one or more memory devices on top of the first wafer having one or more active IC devices. Exhibit 1008, ¶¶20, 22-23, 25. In my opinion, a person of ordinary skill in the art would have recognized Kim’s active silicon layer 222 including memory devices on the second wafer, with or without interlayer dielectric layer 224, teach a “first stackable add-on layer” because the second wafer is stacked on top of the first wafer.

274. Further, Park's semiconductor memory cells include vertical transistors formed from silicon pillars, which are perpendicular with respect to the semiconductor substrate. Exhibit 1011, 2:16-25 ("The silicon pillar is extended in a perpendicular (vertical) direction with respect to a semiconductor substrate"), 2:46-56, 1:11-21, Abstract. In my opinion, a POSITA would have understood that because Park's pillar-shaped transistor stacks the source, drain, and channel regions perpendicular to the substrate, the current flowing through the transistor (i.e., "one or more circuit elements that have characteristics that are voltage variant") would also be substantially perpendicular to the substrate. Park further explains that its transistors are incorporated into its DRAM memory cells, which further comprise a capacitor vertically formed with respect to the transistor. *Id.*, 5:33-37, 8:5-23, Figs. 7-9. Thus, in my opinion, a POSITA would have understood Park's DRAM memory cells to be "vertically oriented"

275. In the combination, the stackable add-on layer (Kim's top wafer 220) would have a plurality of vertically oriented semiconductor memory cells, as depicted in Park's Figure 8 which I have reproduced below. Exhibit 1011, Fig. 8; Exhibit 1008, ¶¶19-20

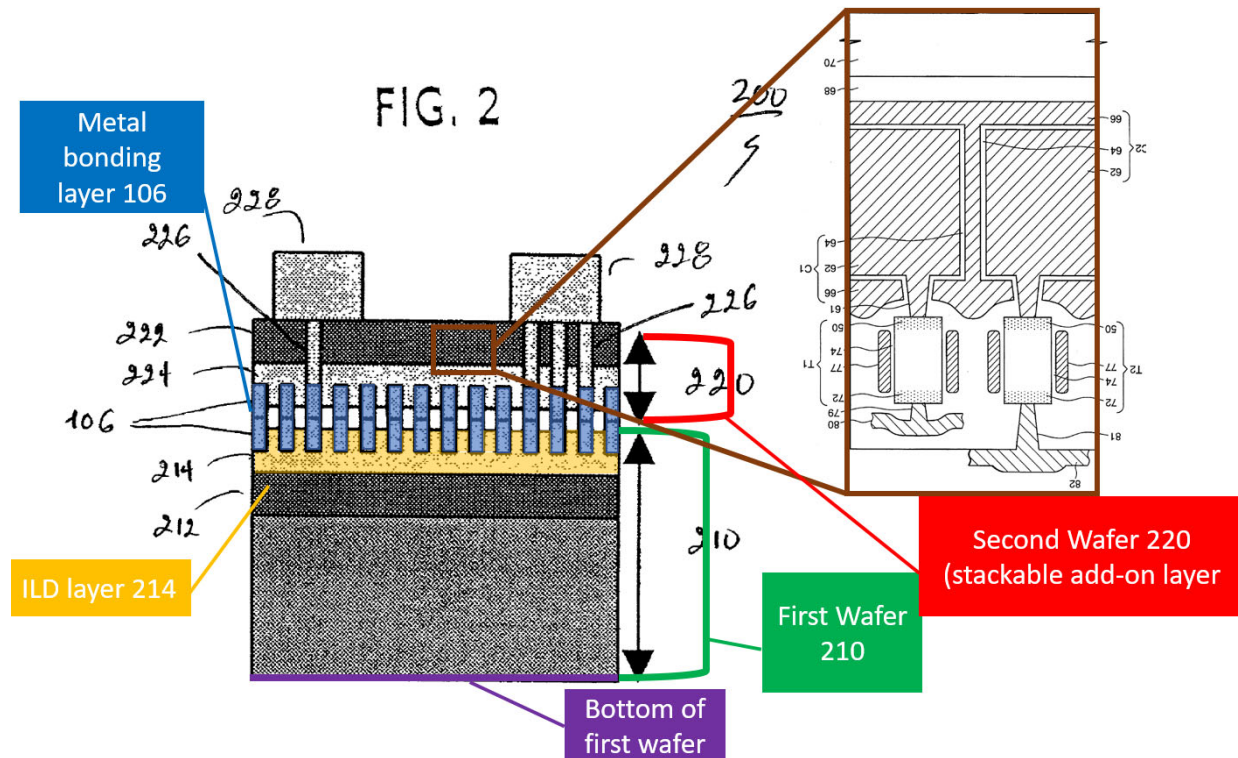


276. Finally, Park discloses that each of its vertically structured transistors are “surrounded [] with an insulating film.” Exhibit 1011, 2:16-21 (The silicon pillar is ... surrounded [] with an insulating film”), 4:9-27 (showing fabrication of vertically structured transistor surrounded by insulating films 16, 18, and 20), Figs. 3, 4:6-8, 5:21-22. Park further discloses that a dielectric film 64 is interposed between the plate and storage electrodes of the capacitors C1 and C2. Exhibit 1011, 5:37-43. Thus, each of Park’s DRAM memory cells is “separated from each other by dielectric material” because both the transistors and capacitors of each memory cell are surrounded by insulating (i.e., dielectric) material. In my opinion, a POSITA

would have understood the need to separate the memory cells with dielectric material for proper operation (e.g., avoiding shorts between them).

- d. **1[c]: “wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate”**

277. In my opinion, the combination of Park and Kim discloses or suggests this limitation. Kim discloses bonding the bottom wafer (i.e., Kim’s wafer 210 containing one or more microprocessors) and the top wafer (i.e., Kim’s wafer 220 containing Park’s vertically oriented DRAM cells) via wafer bonding using a metal bonding layer 106. Exhibit 1008, ¶¶23-25 (“After the wafer bonding process is completed...”). The below annotated figure is a schematic representation illustrating how Park’s DRAM cells (brown, schematically represented by Park’s Figure 8), would have been bonded to logic devices on a first wafer (green) using Kim’s teachings (represented by Kim’s Figure 2):



278. The annotated figure above shows the “stackable add-on layer” (active silicon layer 222 with dielectric 224 (red) in Kim’s Figure 2) containing Park’s vertically-oriented DRAM cells (inserted, brown), is bonded to the ILD layer 214 (orange) of the first wafer via the metal bonding layer 106 (blue). Exhibit 1008, ¶¶23-24 In other words, in the combination, metal bonding layer 106, or alternatively, ILD layer 214 is “a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate.”

279. In my opinion, a POSITA would have understood that the recited “at least one dielectric layer and at least one interconnect layer disposed above the

substrate” in 1[a] are both layers “of the substrate,” as recited in 1[c] because 1[a] characterizes the substrate as “having” those layers. ’702 Patent, 5:37-38. Thus, ILD layer 214 and metal bonding layer 106 are each layers “of the substrate.” Accordingly, in my opinion, a POSITA would have understood that second wafer 220 with active silicon layer 222 and dielectric 224 (“stackable add-on layer”) is bonded, through its own metal bonding layer 106, to metal bonding layer 106 of the first wafer 210 (“a layer of the substrate that is the greatest distance from the substrate as measured from bottom of the substrate” (purple)).

280. In my opinion, a POSITA would have further understood that in the Park-Kim combination schematically represented above, Park’s DRAM cells would have been flipped upside down relative to their depiction in Park’s Figure 8 in order to place Park’s interconnect lines close to the metal bonding layer 106 and accomplish Kim’s stated goal of “shortened [interconnect structure] resulting [in] a faster signal and minimal RC delays.” Exhibit 1008, ¶22. The motivation to combine and reasonable expectation of success for the Park-Kim combination are discussed in Section X.J.2.a.

e. 1[d]: “wherein the memory cell is a DRAM having at least one transistor.”

281. In my opinion, the combination of Park and Kim discloses or suggests this limitation. Park discloses DRAM memory cells, each with one transistor, e.g.,

Exhibit 1011, 5:20-22, which in the combination would be contained in Kim's second wafer 220, for the reasons explained above. Park also discloses a DRAM cell having a vertically oriented transistor. Exhibit 1011, 5:20-21; 2:16-25 ("the silicon pillar is extended in a perpendicular (vertical) direction with respect to a semiconductor substrate"), Fig. 8. The motivation to combine and reasonable expectation of success for the Park-Kim combination are discussed in Section X.J.2.a.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 1st day of June, 2023 in Dallas, Texas.

By: Carl Sechen
Dr. Carl Sechen