

[1090] Subsequently, a silicon oxide film 1440, for example, is formed as a third insulating film to be a tunnel oxide film of about 10 nm on the inner wall of the first trench 1210, for example, using CVD (FIG. 1000 and FIG. 1010). Here, the third insulating film 1440 is not particularly limited to a CVD oxide film, but may be a thermally oxidized film or a nitrogen oxide film.

[1091] Subsequently, the silicon oxide film 1440 located on the first impurity diffusion layer 1710 or on the P-type silicon substrate 1100 is selectively removed, for example, by anisotropic etching so that the silicon oxide film 1440 remains in the form of a sidewall only on the sidewall of the first trench 1210 (FIG. 1001 and FIG. 1011).

[1092] Thereafter, the silicon oxide film 1440 is treated, for example, by thermal treatment. This treatment can be conducted in the same manner as in Production Example 45.

[1093] Thereafter, the oxide film formed on the surface of the first impurity diffusion layer 1710 or on the P-type silicon substrate 1100 is optionally removed, for example, with diluted HF, and the first trench is filled with island-like semiconductor layers 1721 to 1725 and 1111 to 1114. For example, the semiconductor layers are selectively grown epitaxially from the first impurity diffusion layer 1710 or the P-type silicon substrate 1100 positioned at the bottom of the first trench 1210. At this time, from the bottom, an N-type semiconductor layer 1721, a P-type semiconductor layer 1111, an N-type semiconductor layer 1722, a P-type semiconductor layer 1112, an N-type semiconductor layer 1723, a P-type semiconductor layer 1113, an N-type semiconductor layer 1724, a P-type semiconductor layer 1114 and an N-type semiconductor layer 1725 are sequentially formed (FIG. 1002 and FIG. 1012). The concentration of the N-type semiconductor layers 1721 to 1725 is formed at an arsenic dose of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$, and the concentration of the P-type semiconductor layers 1111 to 1114 is formed at a boron dose of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Preferably, the N-type semiconductor layers 1721 and 1722 overlap each other with intervention of the polysilicon layer 1511 and the silicon oxide film 1440; the N-type semiconductor layers 1722 and 1723 overlap each other with intervention of the polysilicon layer 1512 and the silicon oxide film 1440; the N-type semiconductor layers 1723 and 1724 overlap each other with intervention of the polysilicon layer 1513 and the silicon oxide film 1440; and the N-type semiconductor layers 1724 and 1725 overlap each other with intervention of the polysilicon layer 1514 and the silicon oxide film 1440.

[1094] Thereafter, the N-type semiconductor layer 1725 is reduced, for example, by etch back or by CMP to expose the silicon nitride film 1360 and divide the N-type semiconductor layer. Thereafter, a fourth wiring layer is connected to the top of the N-type semiconductor layer 1725 so as to cross the direction of the second and third wiring layers.

[1095] Thereafter, an interlayer insulating film is formed by a known technique, and contact holes and metal wiring are formed. Thereby a semiconductor memory device is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive film.

[1096] In this production example, films formed on the surface of the polysilicon film such as the silicon nitride film

(the second insulating film) 1342 may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. The impurity introduction into the polysilicon films 1511 to 1514 as the first conductive films and the polysilicon films 1521 to 1524 as the second conductive films may be performed when the polysilicon films are formed, after the polysilicon films are formed or after the sidewalls are formed. The timing of introducing the impurity is not limited so long as the conductive film is formed.

[1097] In this production example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only in the case where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1098] By providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1099] Production Example 47

[1100] In a semiconductor memory device to be formed in this example, after regions where charge storage layers and selection gates are formed are to be pre-defined by laminated films including floating gates as charge storage layer, tunnel oxide films are formed in hole-form trenches opened using a photoresist mask. Island-like semiconductor layer are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to a semiconductor substrate. Active regions of memory cells are electrically floated. In this semiconductor memory device, selection gate transistors are disposed at the top and at the bottom of each island-like semiconductor layer. A plurality of, for example, two memory cells are disposed between the selection gate transistors. The tunnel oxide films and interlayer insulating films of the memory cells are formed at the same time. The memory cells are connected in series along the island-like semiconductor layer. The gate insulating films of the selection gate transistors have the same thickness of the gate insulating films of the memory transistors.

[1101] This semiconductor memory device can be formed by the following production process. FIGS. 1015 to 1037 and FIGS. 1038 to 1060 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1102] First, a first impurity diffusion layer 1710 is introduced into the P-type silicon substrate 1100 using ion implantation. For example, the ion implantation is performed at an implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{14} to $1 \times 10^{16}/\text{cm}^2$ in a direction inclined about 0 to 7°. Alternatively, instead of ion implantation, an oxide film containing arsenic may be deposited by CVD and diffusion of arsenic from the oxide film may be utilized. Also the first impurity diffusion layer 1710 need not necessarily be introduced in the topmost surface of the P-type silicon substrate 1100.

[1103] Subsequently, using as a mask a resist film R4 patterned by a known photolithography technique (FIG. 1015 and FIG. 1038), the P-type silicon substrate 1100 are

etched 200 to 2000 nm, for example, by RIE so as to divide the first impurity diffusion layer **1710** to form a second trench **1220**.

[**1104**] After the resist film **R4** is removed, a silicon oxide film **1420**, for example, is deposited to 100 to 300 nm as a fifth insulating film in the second trench **1220** and etched back to be buried (**FIG. 1016** and **FIG. 1039**). Means for burying the silicon oxide film **1420** is not particularly limited, and the silicon oxide film **1420** may be etched back using isotropic etching, etched back using anisotropic etching, buried by flattening using CMP or by a combination of these means. The silicon oxide film **1420** may be a silicon nitride film.

[**1105**] Subsequently, on the P-type silicon substrate **1100** or on the first impurity diffusion layer **1710**, are sequentially formed a silicon nitride film **1381** as an eighteenth insulating film, a polysilicon film **1511** as a first conductive film, a silicon nitride film **1382** as an eighteenth insulating film, a polysilicon film **1512** as a first conductive film, a silicon nitride film **1383** as an eighteenth insulating film, a polysilicon film **1513** as a first conductive film, a silicon nitride film **1384** as an eighteenth insulating film, a polysilicon film **1514** as a first conductive film, and a silicon nitride film **1385** as an eighteenth insulating film, for example.

[**1106**] Subsequently, using as a mask a resist film **R2** patterned by a known photolithography technique (**FIG. 1017** and **FIG. 1040**), etching is performed, for example, by RIE until the silicon nitride film **1381** is reached, so as to form a third trench (**FIG. 1018** and **FIG. 1041**).

[**1107**] Thereafter, the polysilicon films **1511** to **1514** are isotropically etched (**FIG. 1019** and **FIG. 1042**) to reduce the diameter of the polysilicon films **1511** to **1514** as compared with the diameter of the silicon nitride films **1382** to **1385**.

[**1108**] Subsequently, a silicon oxide film **1421** is deposited to 50 to 500 nm as a fifth insulating film by CVD in the third trench **1230**. Thereafter, the silicon oxide film **1421** is buried almost to the height of the top of the polysilicon film **1511**, for example, by isotropic etching (**FIG. 1020** and **FIG. 1043**). A silicon nitride film **1390**, for example, is deposited to about 10 to 200 nm as a nineteenth insulating film on the surface of the polysilicon films **1512** to **1514** and the silicon nitride films **1382** to **1385**.

[**1109**] The silicon nitride film **1390** is anisotropically etched to form a sidewall (**FIG. 1021** and **FIG. 1004**), and then, the silicon oxide film **1421** is removed by isotropic etching (**FIG. 1022** and **FIG. 1045**).

[**1110**] Subsequently, a polysilicon film **1521**, for example, is deposited to 100 to 500 nm as a second conductive film and is etched back to form a sidewall on the sidewall of the polysilicon film **1511** (**FIG. 1023** and **FIG. 1046**). At this time, by setting the intervals between the third trenches **1230** to a predetermined value or smaller in the A-A' direction in **FIG. 1**, the polysilicon film **1521** is formed as a second wiring layer to be a selection gate line continuous in the direction without using a masking process.

[**1111**] Subsequently, a silicon oxide film **1421** is deposited 50 to 500 nm as a fifth insulating film in the third trench. The silicon oxide film **1421** is buried almost to the height of the top of the silicon nitride film **1382**, for example, by isotropic

etching (**FIG. 1024** and **FIG. 1047**), and then, an interlayer insulating film **1612** is formed on the surface of the polysilicon films **1512** to **1514** and the silicon nitride films **1383** to **1385** (**FIG. 1025** and **FIG. 1048**). This interlayer insulating film is formed of an ONO film, for example. The ONO film can be formed in the same manner as in Production Example 1.

[**1112**] Subsequently, a polysilicon film **1522** is deposited to about 100 to 500 nm as a second conductive film and is buried almost to the height of the top of the silicon nitride film **1384**, for example, by isotropic etching (**FIG. 1026** and **FIG. 1049**). Thereafter, the interlayer insulating film **1612** deposited on the surface of the polysilicon film **1514** and on the surface of the silicon nitride film **1385** is removed, for example, by isotropic etching (**FIG. 1027** and **FIG. 1050**). Next, a polysilicon film **1524**, for example, is deposited to about 100 to 500 nm as a second conductive film (**FIG. 1028** and **FIG. 1051**).

[**1113**] Thereafter, the polysilicon films **1524** and **1522** are anisotropically etched in self-alignment with the interlayer insulating film **1612** deposited on the sidewalls of the silicon nitride film **1385** and the silicon nitride film **1384** (**FIG. 1029** and **FIG. 1052**) so that the polysilicon film **1522** is buried in the recesses of the polysilicon films **1512** to **1513** sandwiched between the silicon nitride films **1382** to **1384**, with intervention of the interlayer insulating film **1612**.

[**1114**] Thereby, the polysilicon film **1522** is arranged on the side of the polysilicon film **1512** with intervention of the interlayer insulating film **1612**, and the polysilicon film **1523** is arranged on the side of the polysilicon film **1513** with intervention of the interlayer insulating film **1612**. The polysilicon film **1524** as the second conductive film need not necessarily be formed.

[**1115**] Subsequently, a polysilicon film **1532**, for example, is deposited to about 50 to 200 nm as third conductive film and is etched back to form a sidewall on the side of the polysilicon film **1512** with intervention of the interlayer insulating film **1612** (**FIG. 1030** and **FIG. 1053**). At this time, by setting the intervals between the third trenches **1230** to a predetermined value or smaller in the A-A' direction in **FIG. 1**, the polysilicon film **1532** is formed as a second wiring layer to be a selection gate line continuous in the direction without using a masking process.

[**1116**] Thereafter, a silicon oxide film **1422**, for example, is deposited to 50 to 500 nm as a fifth insulating film, and then, is buried almost to the height of the top of the silicon nitride film **1383**, for example, by isotropic etching. Thereafter, by repeating the above-described steps, a sidewall is formed of a polysilicon film **1533** as a third conductive film on the side of the polysilicon film **1513** with intervention of the interlayer insulating film **1513** (**FIG. 1031** and **FIG. 1054**).

[**1117**] Next, a silicon oxide film **1423**, for example, is deposited to 50 to 500 nm as a fifth insulating film. Subsequently, the silicon oxide film **1423** is buried almost to the height of the top of the silicon nitride film **1384**, for example, by isotropic etching. Then a polysilicon film **1534**, for example, is deposited to about 50 to 200 nm as a third conductive film, and then etched back to form a sidewall of the polysilicon film **1534** on the side of the polysilicon film **1513** (**FIG. 1032** and **FIG. 1055**).

[**1118**] Thereafter, the silicon nitride film **1385** is removed by isotropic etching. A silicon oxide film **1491**, for example,

is deposited to about 50 to 500 nm as a twentieth insulating film. Using as a mask a resist film R1 patterned by a known photolithography technique (FIG. 1033 and FIG. 1056), etching is performed by RIE until reached the first impurity diffusion layer 1710, thereby to form a first trench 1210 (FIG. 1034 and FIG. 1057).

[1119] Subsequently, a silicon oxide film 1440, for example, is formed as a third insulating film to be a tunnel oxide film of about 10 nm in the inner wall of the first trench, for example, using CVD. Here, the third insulating film is not particularly limited to a CVD oxide film, but may be a thermally oxidized film or a nitrogen oxide film.

[1120] Thereafter, the silicon oxide film 1440 positioned on the first impurity diffusion layer 1710 is selectively removed, for example, by anisotropic etching so that the silicon oxide film 1440 remains in the form of a sidewall only on the sidewall of the first trench 1210 (FIG. 1035 and FIG. 1058).

[1121] Thereafter, the silicon oxide film 1440 is treated, for example, by thermal treatment. This treatment can be conducted in the same manner as in Production Example 45.

[1122] Thereafter, the oxide film formed on the surface of the first impurity diffusion layer 1710 is optionally removed, for example, with diluted HF, and the first trench 1210 is filled with island-like semiconductor layers 1721 to 1725 and 1111 to 1114. For example, the semiconductor layers are selectively grown epitaxially from the first impurity diffusion layer 1710 positioned at the bottom of the first trench 1210. At this time, from the bottom, an N-type semiconductor layer 1721, a P-type semiconductor layer 1111, an N-type semiconductor layer 1722, a P-type semiconductor layer 1112, an N-type semiconductor layer 1723, a P-type semiconductor layer 1113, an N-type semiconductor layer 1724, a P-type semiconductor layer 1114 and an N-type semiconductor layer 1725 are sequentially formed. The concentration of the N-type semiconductor layers 1721 to 1725 is formed at an arsenic dose of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$, and the concentration of the P-type semiconductor layers 1111 to 1114 is formed at a boron dose of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Preferably, the N-type semiconductor layers 1721 and 1722 overlap each other with intervention of the polysilicon layer 1511 and the silicon oxide film 1440; the N-type semiconductor layers 1722 and 1723 overlap each other with intervention of the polysilicon layer 1512 and the silicon oxide film 1440; the N-type semiconductor layers 1723 and 1724 overlap each other with intervention of the polysilicon layer 1513 and the silicon oxide film 1440; and the N-type semiconductor layers 1724 and 1725 overlap each other with intervention of the polysilicon layer 1514 and the silicon oxide film 1440.

[1123] Thereafter, the N-type semiconductor layer 1725 is reduced, for example, by etch back or by CMP to expose the silicon oxide film 1425 and divide the N-type semiconductor layer (FIG. 1036 and FIG. 1059).

[1124] Subsequently, a fourth wiring layer is connected to the top of the N-type semiconductor layer 1725 so as to cross the direction of the second and third wiring layers.

[1125] Thereafter, an interlayer insulating film is formed by a known technique, and contact holes and metal wiring are formed (FIG. 1037 and FIG. 1060).

[1126] Thereby a semiconductor memory device is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive film.

[1127] The impurity introduction into the polysilicon films 1511 to 1514 as the first conductive films, the polysilicon films 1521 to 1524 as the second conductive films and the polysilicon films 1532 to 1534 as the third conductive films may be performed when the polysilicon films are formed, after the polysilicon films are formed or after the sidewalls are formed. The timing of introducing the impurity is not limited so long as the conductive film is formed.

[1128] In this production example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only in the case where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1129] By providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1130] Production Example 48

[1131] In a semiconductor memory device to be formed in this example, after regions where charge storage layers and selection gates are formed are to be pre-defined by laminated films including floating gates as charge storage layer, tunnel oxide films are formed in hole-form trenches opened using a photoresist mask. Island-like semiconductor layer are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to a semiconductor substrate. Active regions of memory cells are electrically in common. In this semiconductor memory device, selection gate transistors are disposed at the top and at the bottom of each island-like semiconductor layer. A plurality of, for example, two memory cells are disposed between the selection gate transistors. The tunnel oxide films of the memory cells are formed at the same time. The memory cells are connected in series along the island-like semiconductor layer. The gate insulating films of the selection gate transistors have the same thickness of the gate insulating films of the memory transistors. Transfer gates are formed between the transistors for transferring potential to the active regions of the memory transistors.

[1132] This semiconductor memory device can be formed by the following production process. FIGS. 1061 to 1063 and FIGS. 1064 to 1066 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1133] In this example, production steps are the same as those in Production Example 45 until the silicon nitride film 1320 as the tenth insulating film, the silicon nitride film 1330 as the eleventh insulating film, the silicon nitride film 1342 as the twelfth insulating film and the silicon nitride film 1350 as the fourteenth insulating film are exposed to divide the N-type semiconductor layer 1725 (FIG. 1061 and FIG. 1064).

[1134] Thereafter, isotropically etched are the silicon nitride film 1320 as the tenth insulating film, the silicon

nitride film 1330 as the eleventh insulating film, the silicon nitride film 1342 as the twelfth insulating film, the silicon nitride film 1350 as the fourteenth insulating film, the silicon nitride films 1422, 1423, 1424 and 1425 as the fifth insulating films, and the silicon oxide films 1472, 1473, 1474 and 1475 as the ninth insulating film. At this time, the silicon oxide films 1472, 1473, 1474 and 1475 are removed, and further, the silicon oxide film 1440 as the third insulating film between the silicon oxide films 1472, 1473, 1474, 1475 and the island-like semiconductor layer 111 or the impurity diffusion layer 1721 or 1725 as the N-type semiconductor layer is removed (FIG. 1062 and FIG. 1065). Or the silicon oxide film 1440 as the third insulating film between the silicon oxide films 1472, 1473, 1474, 1475 and the island-like semiconductor layer 111 or the impurity diffusion layer 1721 or 1725 as the N-type semiconductor layer is removed. After the silicon oxide films 1472, 1473, 1474, 1475 are removed, and further, portions of the interlayer insulating film 1612 and 1613 exposed by the etching of the silicon oxide films 1472, 1473, 1474, 1475 are etched.

[1135] Subsequently, a silicon oxide film 1400, for example, is deposited to about 5 to 50 nm as a twenty-first insulating film, and then, a polysilicon film 1530, for example, is deposited to about 30 to 300 nm as a third conductive film. Thereafter, the polysilicon film 1530 is etched back to a degree such that at least the top surface of the impurity diffusion layer 1725 is exposed.

[1136] Next, a silicon oxide film 1426, for example, is deposited to about 50 to 500 nm as a twenty-second insulating film. Thereafter, the silicon oxide film 1426 is reduced by etch back or by CMP to expose the N-type semiconductor layer 1725.

[1137] Thereafter, a semiconductor memory device can be realized in accordance with Production Example 45 (FIG. 1063 and FIG. 1066).

[1138] Production Example 49

[1139] In this production example, a layered insulating film is used as the charge storage layer to realize charge storage by trapping in the layered insulating film, as shown in FIGS. 1067 to 1093 and FIGS. 1094 to 1120. FIGS. 1067 to 1093 and FIGS. 1094 to 1120 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 12 which illustrates a memory cell array of an EEPROM.

[1140] First, on the surface of a P-type silicon substrate 1100, a silicon oxide film 1410, for example, is deposited to 2 to 20 nm as a first insulating film to be an implantation protection film, and a first impurity diffusion layer 1710 is introduced into the p-type silicon substrate 1100 using ion implantation (FIG. 1067 and FIG. 1094). For example, the ion implantation may be performed at an implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{14} to $1 \times 10^{16}/\text{cm}^2$ in a direction inclined about 0 to 7°. Instead of the ion implantation, an oxide film containing arsenic may be deposited by CVD, and arsenic diffusion from the oxide film may be utilized. The first impurity diffusion layer 1710 need not necessarily be introduced on the topmost surface of the P-type silicon substrate 1100.

[1141] Subsequently, using as a mask a resist film R5 patterned by a known photolithography technique, the P-type silicon substrate 1100 are etched 200 to 2000 nm, for

example, by RIE so as to divide the first impurity diffusion layer 1710 to form a second trench 1220 (FIG. 1068 and FIG. 1095).

[1142] After the resist film R5 is removed, a silicon oxide film 1420, for example, is deposited to 100 to 300 nm as a fifth insulating film in the second trench 1220 and etched back to be buried. Means for burying the silicon oxide film 1420 is not particularly limited, and the silicon oxide film 1420 may be etched back using isotropic etching, etched back using anisotropic etching, buried by flattening using CMP or by a combination of these means. The silicon oxide film 1420 may be a silicon nitride film. The silicon oxide film 1410 may be removed or may be retained. For example, in the case where the silicon oxide film 1410 is removed, a silicon oxide film 1471 is formed as a ninth insulating film on the P-type silicon substrate 1100 or on the first impurity diffusion layer 1710 (FIG. 1069 and FIG. 1096).

[1143] Thereafter, sequentially deposited are a polysilicon film 1511 as a first conductive film, a silicon oxide film 1472 as a ninth insulating film, a polysilicon film 1512 as a first conductive film, a silicon oxide film 1473 as a ninth insulating film, a polysilicon film 1513 as a first conductive film, a silicon oxide film 1474 as a ninth insulating film, a polysilicon film 1514 as a first conductive film, a silicon oxide film 1475 as a ninth insulating film, and a silicon nitride film 1320 as a tenth insulating film, for example (FIG. 1070 and FIG. 1097). At this time, the silicon oxide films 1471 to 1475 may have different thicknesses or may have the same thickness. The first conductive films 1511 to 1514 may have different thicknesses or may have the same thickness.

[1144] Thereafter, using as a mask a resist film R6 patterned by a known photolithography technique (FIG. 1071 and FIG. 1098), etching is performed to a degree such that the silicon oxide film 1475 is exposed, for example, by RIE (FIG. 1072 and FIG. 1099).

[1145] Next, a silicon nitride film 1330, for example, is formed in the form of a sidewall as an eleventh insulating film on the sidewall of the patterned silicon nitride film 1320 as the tenth insulating film (FIG. 1073 and FIG. 1100). Using the silicon nitride film 1320 and the silicon nitride film 1330 as a mask, the silicon oxide films 1472 to 1475 and the polysilicon films 1511 to 1514 are anisotropically etched sequentially (FIG. 1074 and FIG. 1101) until the time when the first conductive film 1511 is removed, i.e., until the silicon oxide film 1471 is exposed, to form a third trench 1230.

[1146] Subsequently, a polysilicon film 1521, for example, is deposited to 20 to 200 nm as a second conductive film (FIG. 1075 and FIG. 1102).

[1147] Next, the polysilicon film 1521 is etched back to form a sidewall on the sidewall of the polysilicon film 1511 (FIG. 1076 and FIG. 1103). At this time, by setting the intervals between the third trenches 1230 to a predetermined value or smaller in the A-A' direction in FIG. 12, the polysilicon film 1521 is formed as a second wiring layer to be a selection gate line continuous in the direction without using a masking process.

[1148] Thereafter, a silicon nitride film 1342, for example, is deposited to 10 to 100 nm as a twelfth insulating film (FIG. 1077 and FIG. 1104), and a silicon oxide film 1422,

for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD. Thereafter, the silicon oxide film 1422 is buried almost to the height of the sidewall of the silicon oxide film 1472, for example, by isotropic etching (FIG. 0178 and FIG. 1105). The exposed silicon nitride film 1342 as the twelfth insulating film is removed, and then, a polysilicon film 1522, for example, is deposited 20 to 200 nm as a second conductive film.

[1149] Subsequently, the polysilicon film 1522 is etched back to form a sidewall on the sidewall of the polysilicon film 1512 (FIG. 1079 and FIG. 1106). At this time, by setting the intervals between the third trenches 1230 to a predetermined value or smaller in the A-A' direction in FIG. 10, the polysilicon film 1522 is formed as a third wiring layer to be a control gate line continuous in the direction without using a masking process.

[1150] Thereafter, a silicon nitride film 1343, for example, is deposited to 10 to 100 nm as a twelfth insulating film, and a silicon oxide film 1423, for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD. Subsequently, the silicon oxide film 1423 is buried almost to the height of the sidewall of the silicon oxide film 1473, for example, by isotropic etching. The exposed silicon nitride film 1343 as the twelfth insulating film is removed (FIG. 1080 and FIG. 1107).

[1151] Subsequently, in the same manner, a polysilicon film 1523, for example, is deposited to 20 to 200 nm as a second conductive film and is etched back to form a sidewall on the sidewall of the polysilicon film 1513.

[1152] Further, a silicon nitride film 1344, for example, is deposited to 10 to 100 nm as a twelfth insulating film, and a silicon oxide film 1424, for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD.

[1153] Thereafter, the silicon oxide film 1424 is buried almost to the height of the sidewall of the silicon oxide film 1474, for example, by isotropic etching. The exposed silicon nitride film 1344 as the twelfth insulating film is removed. A polysilicon film 1524, for example, is deposited to 20 to 200 nm as a second conductive film and is etched back to form a sidewall on the sidewall of the polysilicon film 1514.

[1154] Next, a silicon nitride film 1345, for example, is deposited to 10 to 100 nm as a twelfth insulating film, and a silicon oxide film 1425, for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD. Thereafter, the oxide film 1425 is buried almost to the height of the sidewall of the silicon oxide film 1475, for example, by isotropic etching. The exposed silicon nitride film 1345 as the twelfth insulating film is removed (FIG. 1081 and FIG. 1108).

[1155] Subsequently, a silicon nitride film 1350, for example, is deposited to 50 to 500 nm as a fourteenth insulating film. Thereafter, the surface of the silicon nitride film 1350 is flattened by CMP (FIG. 1082 and FIG. 1109). Using as a mask a resist film R7 patterned by a known photolithography (FIG. 1083 and FIG. 1110), the silicon nitride film 1350, the silicon nitride film 1330 or the silicon nitride film 1310 is patterned by etching, for example, by RIE.

[1156] Further, the silicon oxide films 1471 to 1475 and the polysilicon films 1511 to 1514 are sequentially etched, for example, by anisotropic etching until the silicon oxide

film 1471 is removed, i.e., until the surface of the P-type silicon substrate 1100 is exposed, to form a first trench 1210 (FIG. 1084 and FIG. 1111).

[1157] Subsequently, a silicon oxide film 1441, for example, is formed as a third insulting film to be a tunnel oxide film of about 10 nm on the inner wall of the first trench 1210, for example, using CVD (FIG. 1085 and FIG. 1112). Here, the third insulating film 1441 is not particularly limited to a CVD oxide film, but may be a thermally oxidized film or a nitrogen oxide film.

[1158] Next, the silicon oxide film 1441 positioned on the first impurity diffusion layer 1710 or the P-type silicon substrate 1100 is selectively removed, for example, by anisotropic etching, so that the silicon oxide film 1441 remains in the form of a sidewall only on the sidewall of the first trench 1210 (FIG. 1086 and FIG. 1113).

[1159] Subsequently, the silicon oxide film 1441 is treated, for example, by thermal treatment. This treatment can be conducted in the same manner as in Production Example 45.

[1160] Thereafter, the oxide film formed on the surface of the first impurity diffusion layer 1710 or on the P-type silicon substrate 1100 is optionally removed, for example, with diluted HF, and the first trench 1210 is filled with island-like semiconductor layers 1721, 1722-1 and 1111. For example, the semiconductor layers are selectively grown epitaxially from the first impurity diffusion layer 1710 or the P-type silicon substrate 1100 positioned at the bottom of the first trench 1210. At this time, from the bottom, an N-type silicon layer 1721, a P-type silicon layer 1111 and an N-type silicon layer 1722-1 are sequentially formed (FIG. 1087 and FIG. 1114). The concentration of the N-type silicon layers 1721 to 1722-1 is formed at an arsenic dose of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$, and the concentration of the P-type silicon layer 1111 is formed at a boron dose of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Preferably, the N-type silicon layers 1721 and 1722-1 overlap the polysilicon layer 1511 as the first conductive film with intervention of the silicon oxide film 1441 as the third insulating film.

[1161] Subsequently, using the N-type semiconductor layer 1722-1 as a mask, the exposed silicon oxide film 1441 is removed, for example, by isotropic etching (FIG. 1088 and FIG. 1115), and then, a layered insulating film 1620 to be a charge storage layer is formed on the inner wall of the first trench 1210 (FIG. 229 and FIG. 256). Here, in the case where the layered insulating film is of MNOS structure, a silicon nitride film of 4 to 10 nm and a silicon oxide film of 2 to 5 nm may be sequentially formed on the surface of the polysilicon film by CVD, for example. Alternatively, a silicon nitride film of 4 to 10 nm may be deposited on the surface of the polysilicon film by CVD, and then the surface of the silicon nitride film may be oxidized to form a silicon oxide film of 2 to 5 nm. In the case where the layered insulating film is of MONOS structure, a silicon oxide film of 2 to 5 nm by CVD, a silicon nitride film of 4 to 8 nm by CVD and a silicon oxide film of 2 to 5 nm may be sequentially formed on the surface of the polysilicon film. Or a silicon oxide film of 2 to 5 nm and a silicon nitride film of 4 to 8 nm by CVD may be sequentially formed on the surface of the polysilicon film, and then the surface of the silicon nitride film may be oxidized to form a silicon oxide film of 2 to 5 nm. Or the surface of the polysilicon film may

be oxidized to form a silicon oxide film of 2 to 5 nm. The above-described techniques may be combined in various way.

[1162] Subsequently, the layered insulating film 1620 positioned on the N-type semiconductor layer is selectively removed, for example, by isotropic etching so that the layered insulating film 1620 remains in the form of a sidewall only on the sidewall of the first trench 1210 (FIG. 1090 and FIG. 1117). Thereafter, the layered insulating film 1620 may be treated, for example, by thermal treatment.

[1163] Subsequently, in the same manner as described above, the first trench 1210 is filled with island-like semiconductor layers 1722-2 to 1724-1 and 1112 to 1113. For example, the semiconductor layers are selectively grown epitaxially from the island-like semiconductor layer 1722-1 positioned at the bottom of the first trench 1210. At this time, from the bottom, an N-type semiconductor layer 1722-1, a P-type semiconductor layer 1112, an N-type semiconductor layer 1723, a P-type semiconductor layer 1113 and an N-type semiconductor layer 1724-1 are sequentially formed. As previously described, the concentration of the N-type semiconductor layers 1722-2 to 1724-1 is formed at an arsenic dose of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$, and the concentration of the P-type semiconductor layers 1112 to 1113 is formed at a boron dose of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Preferably, the N-type semiconductor layers 1722-2 and 1723 overlap the polysilicon layer 1512 as the first conductive film with intervention of the layered insulating film 1620. Likewise the N-type semiconductor layers 1723 and 1724-1 preferably overlap the polysilicon layer 1513 as the first conductive film with intervention of the layered insulating film 1620. Further, preferably the N-type semiconductor layer 1724-1 is so formed not to overlap the polysilicon film 1514 as the first conductive layer. Thereafter, the layered insulating film 1620 is partially removed using the N-type semiconductor film 1724-1 as a mask.

[1164] Subsequently, a silicon oxide film 1444, for example, is formed as a third insulating film to be a gate oxide film of about 10 nm on the inner wall of the first trench 1210, for example, using CVD. Here, the third insulating film 1444 is not particularly limited to a CVD oxide film, but may be a thermally oxidized film or a nitrogen oxide film.

[1165] Subsequently, the silicon oxide film 1444 positioned on the island-like semiconductor layer 1724-1 is selectively removed, for example, by anisotropic etching so that the silicon oxide film 1444 remains in the form of a sidewall on the sidewall of the first trench 1210. Thereafter, the silicon oxide film 1444 is treated, for example, by thermal treatment.

[1166] Subsequently, in the same manner as described above, the first trench 1210 is filled with island-like semiconductor layers 1724-2 to 1725 and 1114. For example, the semiconductor layers are selectively grown epitaxially from the island-like semiconductor layer 1724-1 positioned at the bottom of the first trench 1210. At this time, from the bottom, an N-type semiconductor layer 1724-2, a P-type semiconductor layer 1114 and an N-type semiconductor layer 1725 are sequentially formed (FIG. 1091 and FIG. 1118). As previously described, the concentration of the N-type semiconductor layers 1724-2 to 1725 is formed at an arsenic dose of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$, and the concentration of the P-type semiconductor layer 1114 is formed

at a boron dose of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Preferably, the N-type semiconductor layers 1724-2 and 1725 overlap the polysilicon layer 1514 as the first conductive film with intervention of the silicon oxide film 1444 as the third insulating film.

[1167] Subsequently, the N-type semiconductor layer 1725 is reduced, for example, by etch back or by CMP to expose the silicon oxide film 1425 as the fifth insulating film and divide the N-type semiconductor layer 1725.

[1168] Thereafter, a fourth wiring layer is connected to the top of the N-type semiconductor layer 1725 so that the fourth wiring layer crosses the direction of the second wiring layer or the third wiring layer.

[1169] Further, by a known technique, an interlayer insulating film is formed, and contact holes and metal wiring are formed.

[1170] Thereby, a semiconductor memory device is realized which has a memory function according to the state of a charge in the charge storage layer which is formed of the layered insulating film.

[1171] The impurity introduction into the polysilicon films 1511 to 1514 as the first conductive films and the polysilicon films 1522 to 1523 as the second conductive films may be performed when the polysilicon films are formed, after the polysilicon films are formed or after the sidewalls are formed. The timing of introducing the impurity is not limited so long as the conductive film is formed.

[1172] In this production example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only in the case where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1173] By providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1174] Production Example 50

[1175] In this production example, a semiconductor memory device has a plurality of memory cells using MIS capacitors as the charge storage layers, as shown in FIGS. 1121 to 1143 and FIGS. 1144 to 1166. FIGS. 1121 to 1143 and FIGS. 1144 to 1166 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 13 which illustrates a memory cell array of an EEPROM.

[1176] First, on the surface of a P-type silicon substrate 1100, a silicon oxide film 1410, for example, is deposited to 2 to 20 nm as a first insulating film to be an implantation protection film, and a first impurity diffusion layer 1710 is introduced into the p-type silicon substrate 1100 using ion implantation (FIG. 1121 and FIG. 1144). For example, the ion implantation may be performed at an implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{14} to $1 \times 10^{16}/\text{cm}^2$ in a direction inclined about 0 to 7°. Instead of the ion implantation, an oxide film containing arsenic may be deposited by CVD, and arsenic diffusion from the oxide film may be utilized. The first impurity diffusion layer 1710

need not necessarily be introduced on the topmost surface of the P-type silicon substrate **1100**.

[1177] Subsequently, using as a mask a resist film **R5** patterned by a known photolithography technique, the P-type silicon substrate **1100** are etched 200 to 2000 nm, for example, by RIE so as to divide the first impurity diffusion layer **1710** to form a second trench **1220** (FIG. 1122 and FIG. 1145).

[1178] After the resist film **R5** is removed, a silicon oxide film **1420**, for example, is deposited to 100 to 300 nm as a fifth insulating film in the second trench **1220** and etched back to be buried. Means for burying the silicon oxide film **1420** is not particularly limited, and the silicon oxide film **1420** may be etched back using isotropic etching, etched back using anisotropic etching, buried by flattening using CMP or by a combination of these means. The silicon oxide film **1420** may be a silicon nitride film. The silicon oxide film **1410** may be removed or may be retained. For example, in the case where the silicon oxide film **1410** is removed, a silicon oxide film **1471** is formed as a ninth insulating film on the P-type silicon substrate **1100** or on the first impurity diffusion layer **1710** (FIG. 1123 and FIG. 1146).

[1179] Thereafter, sequentially deposited are a polysilicon film **1511** as a first conductive film, a silicon oxide film **1472** as a ninth insulating film, a polysilicon film **1512** as a first conductive film, a silicon oxide film **1473** as a ninth insulating film, a polysilicon film **1513** as a first conductive film, a silicon oxide film **1474** as a ninth insulating film, a polysilicon film **1514** as a first conductive film, a silicon oxide film **1475** as a ninth insulating film, and a silicon nitride film **1320** as a tenth insulating film, for example (FIG. 1124 and FIG. 1147). At this time, the silicon oxide films **1471** to **1475** may have different thicknesses or may have the same thickness. The first conductive films **1511** to **1514** may have different thicknesses or may have the same thickness.

[1180] Thereafter, using as a mask a resist film **R6** patterned by a known photolithography technique (FIG. 1125 and FIG. 1148), etching is performed to a degree such that the silicon oxide film **1475** is exposed, for example, by RIE (FIG. 1126 and FIG. 1149).

[1181] Next, a silicon nitride film **1330**, for example, is formed in the form of a sidewall as an eleventh insulating film on the sidewall of the patterned silicon nitride film **1320** as the tenth insulating film (FIG. 1127 and FIG. 1150). Using the silicon nitride film **1320** and the silicon nitride film **1330** as a mask, the silicon oxide films **1472** to **1475** and the polysilicon films **1511** to **1514** are anisotropically etched sequentially (FIG. 1128 and FIG. 1151) until the first conductive film **1511** is removed, i.e., until the silicon oxide film **1472** is exposed, to form a third trench **1230**.

[1182] Subsequently, a polysilicon film **1521**, for example, is deposited to 20 to 200 nm as a second conductive film (FIG. 1129 and FIG. 1152).

[1183] Next, the polysilicon film **1521** is etched back to form a sidewall on the sidewall of the polysilicon film **1511** (FIG. 1130 and FIG. 1153). At this time, by setting the intervals between the third trenches **1230** to a predetermined value or smaller in the A-A' direction in FIG. 13, the polysilicon film **1521** is formed as a second wiring layer to be a selection gate line continuous in the direction without using a masking process.

[1184] Thereafter, a silicon nitride film **1342**, for example, is deposited to 10 to 100 nm as a twelfth insulating film (FIG. 1131 and FIG. 1154), and a silicon oxide film **1422**, for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD. Thereafter, the silicon oxide film **1422** is buried almost to the height of the sidewall of the silicon oxide film **1472**, for example, by isotropic etching (FIG. 1132 and FIG. 1155). The exposed silicon nitride film **1342** as the twelfth insulating film is removed, and then, a polysilicon film **1522**, for example, is deposited 20 to 200 nm as a second conductive film.

[1185] Subsequently, the polysilicon film **1522** is etched back to form a sidewall on the sidewall of the polysilicon film **1512** (FIG. 1133 and FIG. 1156). At this time, by setting the intervals between the third trenches **1230** to a predetermined value or smaller in the A-A' direction in FIG. 13, the polysilicon film **1522** is formed as a third wiring layer to be a control gate line continuous in the direction without using a masking process.

[1186] Thereafter, a silicon nitride film **1343**, for example, is deposited to 10 to 100 nm as a twelfth insulating film, and a silicon oxide film **1423**, for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD. Subsequently, the silicon oxide film **1423** is buried almost to the height of the sidewall of the silicon oxide film **1473**, for example, by isotropic etching. The exposed silicon nitride film **1343** as the twelfth insulating film is removed (FIG. 1134 and FIG. 1157).

[1187] Further, in the same manner, a polysilicon film **1523**, for example, is deposited to 20 to 200 nm as a second conductive film and is etched back to form a sidewall on the sidewall of the polysilicon film **1513**. Next, a silicon nitride film **1344**, for example, is deposited to 10 to 100 nm as a twelfth insulating film, and a silicon oxide film **1424**, for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD. Thereafter, the silicon oxide film **1424** is buried almost to the height of the sidewall of the silicon oxide film **1474**, for example, by isotropic etching. The exposed silicon nitride film **1344** as the twelfth insulating film is removed.

[1188] A polysilicon film **1524**, for example, is deposited to 20 to 200 nm as a second conductive film and is etched back to form a sidewall on the sidewall of the polysilicon film **1514**. Next, a silicon nitride film **1345**, for example, is deposited to 10 to 100 nm as a twelfth insulating film, and a silicon oxide film **1425**, for example, is deposited to 50 to 500 nm as a fifth insulating film by CVD. Thereafter, the oxide film **1425** is buried almost to the height of the sidewall of the silicon oxide film **1475**, for example, by isotropic etching. The exposed silicon nitride film **1345** as the twelfth insulating film is removed (FIG. 1135 and FIG. 1158).

[1189] Subsequently, a silicon nitride film **1350**, for example, is deposited to 50 to 500 nm as a fourteenth insulating film. Thereafter, the surface of the silicon nitride film **1350** is flattened by CMP (FIG. 1136 and FIG. 1159). Using as a mask a resist film **R7** patterned by a known photolithography technique (FIG. 1137 and FIG. 1160), the silicon nitride film **1350**, the silicon nitride film **1330** or the silicon nitride film **1310** is patterned by etching, for example, by RIE.

[1190] Further, the silicon oxide films **1471** to **1475** and the polysilicon films **1511** to **1514** are sequentially etched,

for example, by anisotropic etching until the silicon oxide film 1471 is removed, i.e., until the surface of the P-type silicon substrate 1100 is exposed, to form a first trench 1210 (FIG. 1138 and FIG. 1161).

[1191] Subsequently, a silicon oxide film 1440, for example, is formed as a third insulating film to be a tunnel oxide film of about 10 nm on the inner wall of the first trench 1210, for example, using CVD (FIG. 1139 and FIG. 1162). Here, the third insulating film 1440 is not particularly limited to a CVD oxide film, but may be a thermally oxidized film or a nitrogen oxide film.

[1192] Next, the silicon oxide film 1440 positioned on the first impurity diffusion layer 1710 or the P-type silicon substrate 1100 is selectively removed, for example, by anisotropic etching, so that the silicon oxide film 1440 remains in the form of a sidewall only on the sidewall of the first trench 1210 (FIG. 1140 and FIG. 1163).

[1193] Thereafter, the silicon oxide film 1440 is treated, for example, by thermal treatment. This treatment can be conducted in the same manner as in Production Example 1.

[1194] Subsequently, the oxide film formed on the surface of the first impurity diffusion layer 1710 or on the P-type silicon substrate 1100 is optionally removed, for example, with diluted HF, and the first trench 1210 is filled with island-like semiconductor layers 1721, 1725, 1726, 1727 and 1111 to 1113. For example, the semiconductor layers are selectively grown epitaxially from the first impurity diffusion layer 1710 or the P-type silicon substrate 1100 positioned at the bottom of the first trench 1210. At this time, from the bottom, an N-type silicon layer 1721, a P-type silicon layer 1111, an N-type silicon layer 1726, a P-type silicon layer 1112, an N-type silicon layer 1727, a P-type silicon layer 1113 and an N-type silicon layer 1725 are sequentially formed (FIG. 1141 and FIG. 1164). The concentration of the N-type silicon layers 1721, 1725, 1726 and 1727 is formed at an arsenic dose of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$, and the concentration of the P-type silicon layers 1111 to 1113 is formed at a boron dose of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Preferably, the N-type silicon layers 1721 and 1726 overlap the polysilicon layer 1511 as the first conductive film with intervention of the silicon oxide film 1440 as the third insulating film, and the N-type silicon layers 1725 and 1727 overlap the polysilicon layer 1514 as the first conductive film with intervention of the silicon oxide film 1440 as the third insulating film. Preferably the P-type silicon layer 1112 does not overlap either the polysilicon film 1512 as the first conductive film or the polysilicon film 1513 as the first conductive film.

[1195] Thereafter, the N-type semiconductor layer 1725 is reduced, for example, by etch back or by CMP to expose the silicon oxide film 1425 as the fifth insulating film and divide the N-type semiconductor layer 1725 (FIG. 1142 and FIG. 1165).

[1196] Further, a fourth wiring layer is connected to the top of the N-type semiconductor layer 1725 so that the fourth wiring layer crosses the direction of the second wiring layer or the third wiring layer.

[1197] Thereafter, by a known technique, an interlayer insulating film is formed, and contact holes and metal wiring are formed (FIG. 1143 and FIG. 1166).

[1198] Thereby, two pairs of DRAM elements can be formed in the island-like semiconductor layer, the DRAM element having a one-transistor/one-capacitor structure using an MIS capacitor as the charge storage layer.

[1199] The impurity introduction into the polysilicon films 1511 to 1514 as the first conductive films and the polysilicon films 1522 to 1523 as the second conductive films may be performed when the polysilicon films are formed, after the polysilicon films are formed or after the sidewalls are formed. The timing of introducing the impurity is not limited so long as the conductive film is formed.

[1200] In this production example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only in the case where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1201] Production Example 51

[1202] In this production example, a semiconductor memory device has a structure in which a plurality of memory cells uses floating gates as the charge storage layers; selection gate transistors arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistor; tunnel oxide films of memory transistors are formed at the same time and are connected along the island-like semiconductor layer; gate insulating films of the selection gate transistors have the same thickness as gate insulation films of the memory transistors, as shown in FIGS. 1167 to 1168 and FIGS. 1169 to 1170. FIGS. 1167 to 1168 and FIGS. 1169 to 1170 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1203] In this production example, production steps are the same as those in Production Example 45 (FIGS. 939 to 966 and FIGS. 967 to 994) until the N-type semiconductor layer 1721, the P-type semiconductor 1111 and the N-type semiconductor 1722 are arranged from the first trench 1210. However, the silicon oxide film 1473 as the ninth insulating film is controlled to have a thickness of about 20 to 40 nm when deposited, or after a polysilicon film 1512 is deposited as the first conductive film, a thermally oxidized film is formed in a thickness of about 20 to 40 nm. At this time, by setting, at 20 to 30 nm, the interval between the polysilicon films 1512 and 1513 as the first conductive films which are the floating gates of the memory cells, it becomes unnecessary to form, among the island-like semiconductor layers 1721 to 1725 to be formed in the first trench 1210 in a later step, an N-type semiconductor layer 1723 between the memory cells (FIG. 1167 and FIG. 1169).

[1204] As another production example, production steps are conducted in the same manner as in Production Example 45 until the N-type semiconductor layer 1721 is arranged from the first trench 1210, but the silicon oxide films 1472 to 1474 are controlled to have a thickness of about 20 to 40 nm when deposited, or every time after the polysilicon films 1511 to 1513 are deposited, thermally oxidized films are

formed in a thickness of about 20 to 40 nm. At this time, by setting, at 20 to 30 nm, the intervals between the polysilicon films **1511** and **1512**, **1512** and **1513**, and **1513** and **1514** as the first conductive films which are the floating gates of the memory cells, it becomes unnecessary to form, among the island-like semiconductor layers **1721** to **1725** to be formed in the first trench **1210** in a later step, impurity diffusion layers **1722**, **1723**, **1724** between the selection gates and the memory cells (**FIG. 1168** and **FIG. 1170**).

[1205] Production Example 52

[1206] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers; selection gate transistors are formed, and then tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; two memory cells are arranged on each island-like semiconductor layer; the tunnel oxide films of the memory transistors are formed at the same time; and the transistors are connected in series along the island-like semiconductor layer, as shown in **FIG. 1171** and **FIG. 1172**. **FIG. 1171** and **FIG. 1172** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** which illustrates a memory cell array of an EEPROM.

[1207] In this example, production step are the same as those of Production Example 45, except that, after the silicon oxide film **1473** is deposited as the ninth insulating film, without depositing the silicon oxide films **1474** and **1475** as the ninth insulating films and the polysilicon films **1513** and **1514** as the first conductive films, the silicon nitride film **1320** is deposited as the tenth insulating film and the polysilicon films **1521** and **1522** are arranged as the second conductive films on the sidewalls of the polysilicon films **1511** and **1522** as the first conductive films with intervention of interlayer insulating films **1612** and **1613**. Thereby two memory transistors are arranged on the island-like semiconductor layer. A semiconductor memory device is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive film (**FIG. 1171** and **FIG. 117**).

[1208] Production Example 53

[1209] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers on a semiconductor of a semiconductor substrate into which an oxide film is inserted, e.g., a SOI substrate; selection gates and control gates are formed, and then, tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; selection gate transistors are arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistors; the tunnel oxide films of the transistors are formed at the same time; the transistors are connected in series along the island-like semiconductor layer; and the gate insulating films of the selection gate transistors have the same thickness as the gate insulating

films of the memory transistors, as shown in **FIG. 1173** and **FIG. 1174**. **FIG. 1173** and **FIG. 1174** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** which illustrates a memory cell array of an EEPROM.

[1210] This production example is substantially the same as Production Example 45 except that the SOI substrate is used.

[1211] Also by this production example, the same effect as of Production Example 45 can be obtained. Further the junction capacity of the impurity diffusion layer **1710** and the first wiring layer is suppressed or eliminated. The use of a SOI substrate as the substrate is applicable to all the examples of the present invention.

[1212] Production Example 54

[1213] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers; selection gates and control gates are formed, and then, tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; selection gate transistors are arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistors; the tunnel oxide films of the transistors are formed at the same film; the transistors are connected in series along the island-like semiconductor layer; and the gate insulating films of the selection gate transistors have larger than the thickness as the gate insulating films of the memory transistors, as shown in **FIG. 1175** and **FIG. 1176**. **FIG. 1175** and **FIG. 1176** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** which illustrates a memory cell array of an EEPROM.

[1214] This production example is substantially the same as Production Example 1 except that the tunnel oxide film as the third insulating film, which is formed on the inner wall of the first trench **1210**, is arranged to contact the polysilicon films **1512** and **1513** as the first conductive films as shown in **FIG. 1175** and **FIG. 1176**, except that the silicon oxide film **1451** as the thirteenth insulating is arranged to contact the polysilicon film **1511** as the first conductive film, and except that the silicon oxide film **1454** as the thirteenth insulating film is arranged to contact the polysilicon film **1514** as the first conductive film.

[1215] Thereby, a structure is realized in which the gate insulating films of the selection gate transistors have a larger thickness than the gate insulating films of the memory transistors, and the same effect as of the Production Example 45 is obtained.

[1216] Production Example 55

[1217] **FIGS. 1177** to **1179** and **FIGS. 1180** to **1182** show a production example for obtained a structure in which the direction of the first wiring layer is parallel to the direction of the fourth wiring layer. **FIGS. 1177** to **1179** and **FIGS. 1180** to **1182** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** which illustrates a memory cell array of an EEPROM.

[1218] This production example is substantially the same as Production Example 45 except that first, using as a mask a resist film R5 patterned by a known photolithography technique (FIG. 1177 and FIG. 1180), the first insulating film 1410 and the P-type silicon substrate 1100 is etched by 200 to 2000 nm, for example, by RIE so that the first impurity diffusion layer 1710 is divided and the second trench 1220 is formed in a direction crossing the second wiring layer which is to be a continuous gate line later (FIGS. 1178 to 1179 and FIGS. 1181 to 1182).

[1219] Thereby, a semiconductor memory device is realized in which the first wiring layer is parallel to the fourth wiring layer and which has memory function according to the state of a charge accumulated in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive layer.

[1220] Films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film (the second insulating film) 1310 may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. The impurity introduction into the polysilicon films 1511 to 1514 as the first conductive films and the polysilicon films 1522 and 1523 as the second conductive films may be performed when the polysilicon films are formed, after the polysilicon films are formed or after the sidewalls are formed. The timing of introducing the impurity is not limited so long as the conductive film is formed.

[1221] In this production example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only in the case where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1222] By providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1223] Production Example 56

[1224] FIG. 1183 and FIG. 1184 show a production example for obtaining a structure in which the first wiring is electrically common to a memory array. FIG. 1183 and FIG. 1184 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1225] The second trench 1220 is not formed in the semiconductor substrate 1100. This production example is substantially the same as Production Example 45 except that the step of forming the second trench 1220 is omitted (FIG. 1183 and FIG. 1184).

[1226] Thereby, the first wiring layer is not divided and is common at least in an array. A semiconductor memory device is realized which has a memory function according to the state of a charge accumulated in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive film.

[1227] Production Example 57

[1228] Production Example 49 (FIGS. 1067 to 1087 and FIGS. 1094 to 1114) shows a production process for using

a layered insulating film as the charge storage layer and realizing charge storage by trapping into the layered insulating film in contrast to Production Example 45. This production example shows another production process for obtaining an equivalent effect to the effect of Production Example 49, as shown in FIGS. 1185 to 1195 and FIGS. 1196 to 1206. FIGS. 1185 to 1195 and FIGS. 1196 to 1206 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 12 which illustrates a memory cell array of an EEPROM.

[1229] In this example, production steps are the same as those of Production Example 49 until the silicon nitride film 1320 is deposited as the tenth insulating film (FIGS. 1185 to 1188 and FIGS. 1196 to 1199).

[1230] Subsequently, using as a mask a resist film R6 patterned by a known photolithography technique (FIG. 1189 and FIG. 1200), etching is performed to a degree such that the silicon oxide film 1475 as the ninth insulating film, for example, by RIE. At this time, the silicon oxide film 1475 is not divided in the A-A' direction (FIG. 1190 and FIG. 1201).

[1231] Next, a silicon nitride film 1330 is formed as an eleventh insulating film in the form of a sidewall on the sidewall of the patterned silicon nitride film 1320 as the tenth insulating film (FIG. 1191 and FIG. 1202). Using the silicon nitride film 1320 and the silicon nitride film 1330 as a mask, the silicon oxide films 1472 to 1475 as the ninth insulating films and the polysilicon films 1511 to 1514 as the first conductive films are sequentially etched (FIG. 1192 and FIG. 1203, for example, by anisotropic etching until the first conductive film 1511 is etched, i.e., until the ninth insulating film 1471 is exposed, to form a third trench 1230).

[1232] Subsequently, a silicon oxide film 1421 is deposited as a fifth insulating film and buried in the third trench 1230 (FIG. 1193 and FIG. 1204). Using as a mask a resist film R7 patterned by a known photolithography technique, the silicon nitride film 1330 and the silicon nitride film 1320 are patterned, for example, by RIE.

[1233] Further, the silicon oxide films 1471 to 1475 and the polysilicon films 1511 to 1514 are sequentially etched, for example, by anisotropic etching until the silicon oxide film 1471 is removed, i.e., until the P-type silicon substrate 1100 is exposed, thereby to form the first trench 1210 (FIG. 1194 and FIG. 1205).

[1234] Thereafter, production steps are in accordance with Production Example 49 (FIGS. 1067 to 1087 and FIGS. 1094 to 1114). Thereby, a semiconductor memory device is realized which has a memory function according to the state of a charge accumulated in the charge storage layer made of the layered insulating film (FIG. 1195 and FIG. 1206).

[1235] In this production example, the impurity introduction into the polysilicon films 1511 to 1514 as the first conductive films may be performed when the polysilicon films are formed or after the polysilicon films are formed. The timing of introducing the impurity is not limited so long as the conductive film is formed.

[1236] By providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1237] Production Example 58

[1238] FIG. 1207 and FIG. 1208 show a production example for a semiconductor memory device in which the transistor, the capacitor, the transistor and the capacitor are disposed in this order in contrast to the semiconductor memory device formed in Production Example 50. FIG. 1207 and FIG. 1208 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 13 which illustrates a memory cell array of a DRAM.

[1239] This production example is in accordance with Production Example 50 (FIGS. 1121 to 1143 and FIGS. 1144 to 1166) except that the impurity diffusion layer 1710 is not formed and the step of dividing the impurity layer is not introduced. The structure shown in FIG. 1207 and FIG. 1208 is obtained.

[1240] Thereby, a plurality of capacitors formed on the semiconductor layer disposed in the first trench can be divided. Since the impurity diffusion layer 1710 is not used as a wiring layer, the wiring capacity decreases.

[1241] Production Example 59

[1242] FIGS. 1209 to FIG. 1210 and FIG. 1211 to FIG. 1212 show a production example for a semiconductor memory device in which a region where charge storage layers and selection gates are formed is pre-defined by a layered film including the floating gates as the charge storage layers; the tunnel oxide films are formed in a hole-form trench opened using a photoresist mask; island-like semiconductor layers are formed in the pillar form by selective epitaxial silicon growth; the island-like semiconductor layers are electrically floated with respect to the semiconductor substrate; the active regions of memory cells are electrically in common; selection gate transistors are arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistors; the tunnel oxide films of the memory transistors are formed at the same time; the transistors are connected in series along the island-like semiconductor layer; the gate insulating films of the selection gate transistors have the same thickness as the gate insulating films of the memory transistors; and the surface area of the floating gate is increased. FIGS. 1209 to FIG. 1210 and FIG. 1211 to FIG. 1212 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1243] This production example is carried out in accordance with Production Example 45 (FIGS. 939 to 966 and FIGS. 967 to 994) until the polysilicon film 1521 as the second conductive film is etched back to form a sidewall on the sidewall of the polysilicon film 1511 as the first conductive film.

[1244] Subsequently, the silicon oxide films 1471 to 1475 as the ninth insulating films are etched in a horizontal direction with respect to the semiconductor substrate 1100, for example, by isotropic etching (FIG. 1209 and FIG. 1211).

[1245] Thereafter, a silicon nitride film 1342, for example, is deposited to 2 to 20 nm as a twelfth insulating film on the sidewall of the third trench 1230. Thereafter the semicon-

ductor memory device is formed in accordance with Production Example 1 (FIG. 1210 and FIG. 1212).

[1246] Thereby, the area of the second conductive films 1512 and 1513 which are to be floating gates connecting the third conductive film to be control gates with intervention of the interlayer insulating films 1612 and 1613 increases, and thereby the capacitance between the floating gates and the control gates increases.

[1247] Production Example 60

[1248] FIGS. 1213 and 1215 and FIGS. 1214 and 1216 show a production example for obtaining a structure in which the gates of the transistors have different lengths in the vertical direction. FIGS. 1213 to 1214 and FIGS. 1215 to FIG. 1216 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1249] In this production example, as to the lengths of the polysilicon layers 1511 to 1514 to be the gates of the memory cells and the selection gate in the direction perpendicular to the semiconductor substrate 1110, the selection gate lengths of the polysilicon layers 1511 and 1514 are different as shown in FIG. 1213 and FIG. 1215.

[1250] The gate lengths of the memory cells of the polysilicon films 1512 and 1513 as the first conductive films may be different as shown in FIGS. 1214 and 1216.

[1251] Further the polysilicon films 1512 and 1513 may also have different lengths in the vertical direction.

[1252] Production Example 61

[1253] FIG. 1217 and FIG. 1218 show a production example for obtaining a structure in which the activated regions of the transistors have different lengths in the vertical direction. FIG. 1217 and FIG. 1218 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1254] In this production example, as to the lengths of the semiconductor layers 1111 to 1114 to be the channels of the memory cells and the channels of the selection transistors in the direction perpendicular to the semiconductor substrate 1110, the channel lengths of the selection transistors of the semiconductor layers 1111 and 1114 are different as shown in FIG. 1217 and FIG. 1218.

[1255] The channel lengths of the memory cells of the semiconductor layers 1112 and 1113 may also be different.

[1256] Production Example 62

[1257] FIG. 359 and FIG. 360 show a production example for obtaining a structure in which a large height is given to the impurity diffusion layer 1725 which is positioned on the top of the semiconductor layer 1110 and connected to the fourth wiring layer 1840. FIG. 1219 and FIG. 1220 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1258] In this production example, the semiconductor layer 1725 connected to the fourth wiring layer 1840 is high as shown in FIG. 1219 and FIG. 1220. The thickness of the silicon oxide film 1425 can be set large to improve insulation between the polysilicon film 1514 as the first conductive film and the fourth wiring layer 1840. Or when the impurity diffusion layer 1725 is exposed, exposed area can be set

large, and thereby, the connection between the impurity diffusion layer **1725** and the fourth wiring layer **1840** is improved.

[1259] Production Example 63

[1260] This production example shows a modification of the shape of the island-like semiconductor layers as shown in FIGS. **1221** to **1222** and FIGS. **1223** to **1224**. FIGS. **1221** to **1222** and FIGS. **1223** to **1224** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** which illustrates a memory cell array of an EEPROM.

[1261] FIG. **1221** and FIG. **1223** show the case where, when the first trench **1210** is formed by RIE, the first trench **1210** has different outside shapes at its top and at its bottom. For example, if the first trench **1210** has a circular plan view from the top, the trench has a conic shape.

[1262] FIG. **1222** and FIG. **1224** show the case where the top and the bottom of the first trench **1210** are shifted in the horizontal direction. For example, if the first trench **1210** has a circular plan view from the top, the trench has an inclined conic shape.

[1263] The shape of the first trench **1210** is not particularly limited so long as the memory cells can be arranged in series in the direction perpendicular to the semiconductor substrate **1110**.

[1264] Production Example 64

[1265] This production example shows further modification of the shape of the island-like semiconductor layers as shown in FIGS. **1225** to **1228** and FIGS. **1229** to **1232**. FIGS. **1225** to **1228** and FIGS. **1229** to **1232** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** which illustrates a memory cell array of an EEPROM.

[1266] FIGS. **1225** to **1226** and FIGS. **1229** to **1230** show the case where, when the first trench **1210** is formed by RIE, the outside shape of the first trench **1210** in the silicon oxide films **1422** to **1425** as the fifth insulating films and the silicon oxide film **1471** as the ninth insulating film is larger than the outside shape of the first trench **1210** in the polysilicon films **1511** to **1514** as the first conductive films.

[1267] On the other hand, FIGS. **1227** to **1228** and FIGS. **1231** to **1232** show the case where the outside shape of the first trench **1210** in the silicon oxide films **1422** to **1425** as the fifth insulating films and the silicon oxide film **1471** as the ninth insulating film is smaller than the outside shape of the first trench **1210** in the polysilicon films **1511** to **1514** as the first conductive films.

[1268] As to the size relationship between the outside shape of the first trench **1210** in the above-mentioned insulating films and the outside shape of the first trench **1210** in the silicon nitride film **1330** as the eleventh insulating film, it does not matter, and the shape of the first trench **1210** is not particularly limited so long as the memory cells can be arranged in series in the direction perpendicular to the semiconductor substrate **1100**.

[1269] Production Example 65

[1270] This production example shows a modified shape at the bottom of the island-like semiconductor layers as shown in FIGS. **1233** to **1236** and FIGS. **1237** to **1240**. FIGS. **1233** to **1236** and FIGS. **1237** to **1240** are sectional

views taken on line A-A' and line B-B', respectively, in FIG. **1** which illustrates a memory cell array of an EEPROM.

[1271] The bottom shape of the first trench **1210** in the lattice form has a linearly inclined structure as shown in FIGS. **1233** to **1234** and FIGS. **1237** to **1238**.

[1272] Alternatively, the bottom shape of the first trench **1210** in the lattice form has a roundedly inclined structure as shown in FIGS. **1235** to **1236** and FIGS. **1239** to **1240**.

[1273] The bottom end of the polysilicon film **1511** as the first conductive film may reach or may not reach the inclined bottom of the first trench **1210**.

[1274] Production Example 66

[1275] This production example shows a modified shape for a polysilicon film deposited on an underlying step as shown in FIG. **1241** and FIG. **1242**. FIG. **1241** and FIG. **1242** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** which illustrates a memory cell array of an EEPROM.

[1276] The second polysilicon films **1521** to **1524** covering the silicon oxide films **1471** to **1475** as the ninth insulating films, the silicon nitride film **1320** as the tenth insulating film, the silicon nitride film **1330** as the eleventh insulating film and the polysilicon films **1511** to **1514** as the first conductive films has a uniformly deposited structure according to the bottom shape of the first trench **1210**.

[1277] However, the second polysilicon films **1521** to **1524** may have a non-uniformly deposited structure in part depending upon the bottom shape as shown in Production Example 45.

[1278] Production Example 67

[1279] This production example shows the formation of fourth wiring layer **1840** by patterning the impurity diffusion layer **1725** positioned on the top end of the semiconductor layers **1110** as shown in FIGS. **1243** to **1244** and FIGS. **1245** to **1246**. FIGS. **1243** to **1244** and FIGS. **1245** to **1246** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** which illustrates a memory cell array of an EEPROM.

[1280] The semiconductor layer **1725** is patterned by RIE using as a mask a resist film **R8** patterned by a known photolithography (FIG. **1243** and FIG. **1245**) to form the fourth wiring layer which crosses the direction of the second or third wiring layer (FIG. **1244** and FIG. **1246**).

[1281] Production Example 68

[1282] This production example shows the formation of terminals for electrically connecting the first, second and third wiring layers and peripheral circuits as shown in FIGS. **1247** to **1242** and FIGS. **1253** to **1258**. FIGS. **1247** to **1252** and FIGS. **1253** to **1258** are sectional views taken on line H-H', I1-I1', I2-I2', I3-I3', I4-I4' and line I5-I5' in FIGS. **11** and **10** which illustrate a memory cell array of an EEPROM. These sectional views are taken at locations showing sites **1921**, **1932**, **1933**, **1924** and **1910** where terminals mounted on the top face of the semiconductor memory device are electrically connected to the buried wiring layers **1521**, **1522**, **1523**, **1524** and **1710** for the application of voltage to the buried wiring layers from outside.

[1283] The first, second and third wiring layers buried in wiring layer lead-out portions are stepwise arranged. First, second and third contacts **1921**, **1932**, **1933**, **1924** and **1910** are formed from end portions of the wiring layers so that the contacts are contacted only with desired wiring layers, and thereby the first, second and third wiring layers are lead out onto the top of the semiconductor memory device (FIGS. **1247** to **1252**).

[1284] Alternatively, conductive films may be taken out onto the semiconductor memory device instead of forming the first, second and third contacts **1921**, **1932**, **1933**, **1924** and **1910**. With this construction, the same effect as described above can be obtained.

[1285] Further the first, second and third wiring layers buried in the wiring layer lead-out portions may be lead out onto the top of the semiconductor memory device in the following process. The wiring layers are arranged as shown in FIG. **1247** to FIG. **1252**. The first, second and third contacts **1921**, **1932**, **1933**, **1934** and **1910** are opened, and then, a silicon oxide film **1499**, for example, is deposited to 10 to 100 nm as a twenty-third insulating film and etched back by a deposited thickness. Thereby sidewalls are formed of the silicon oxide film **1499** on the inner walls of the contacts formed in the wiring layer lead-out portions. At this time, the twenty-third insulating film is not particularly limited to a silicon oxide film, but may be an insulating film such as a silicon nitride film. Thereafter, a metallic or conductive film is filled in the contacts, and thereby, the first, second and third wiring layers are lead out onto the top of the semiconductor memory device (FIG. **1253** and FIG. **1258**).

[1286] The contacts for leading out the wiring layers may be formed in common to wiring layers of adjacent memory cells that are continuous in the A-A' direction as shown in FIGS. **1253** to **1258** or may be formed in each wiring layer lead-out portion as shown in FIGS. **1247** to **1252**.

[1287] Leading the first, second and third wiring layers out onto the top of the semiconductor memory device is applicable to all the examples of the present invention.

[1288] In the above-described production examples, after a plurality of charge storage layers are formed, island-like semiconductor layers **1110** are formed in the form of pillars by selective epitaxial silicon growth; before the active regions are formed of the semiconductor substrate or semiconductor layers, regions to be the charge storage layers are defined by multi-layered film and the charge storage layers are formed in these regions; a plurality of memory cells having charge storage layers and control gates are connected in series in the direction perpendicular to the surface of the semiconductor substrate and these memory cells are formed on the semiconductor substrate and the sidewalls of the island-like semiconductor layers which are arranged in matrix and separated in the lattice form on the semiconductor substrate; impurity diffusion layers disposed on the island-like semiconductor layers form sources or drains of the memory cells and the impurity diffusion layers electrically separate the substrate from the island-like semiconductor layers; control gates have control gate lines which are formed continuously with respect to a plurality of island-like semiconductor layers in one direction and horizontally with respect to the surface of the semiconductor substrate; and bit lines are electrically connected with the impurity diffusion

layers in a direction crossing the control gate lines and are arranged horizontally with respect to the surface of the semiconductor substrate. However the production steps and the constructions of the semiconductor memory device shown in the examples may be optionally combined.

[1289] Hereinafter, described is a production process for producing a semiconductor memory in which, charge storage layers or control gates are formed, insulating films are formed between the charge storage layers and a semiconductor substrate or a semiconductor layer at the same time, and then semiconductor layers in the form of pillars to be active regions are formed on the sides of the insulating films. For forming gate electrodes in the form of sidewall spacers, an insulating film is buried in advance in an adjacent trench and etching is carried out in a horizontal direction using the insulating film as a mask. Thereby the gate electrodes are formed accurately by etching to a depth corresponding to the deposit thickness of a material for the gate electrodes.

[1290] Production Example 69

[1291] In a semiconductor memory to be produced in this example, a plurality of floating gates are formed as charge storage layers and selection gates and control gates are formed. Then, tunnel oxide films are formed and island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors. Tunnel oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer. Further, the thickness of gate insulating films of the selection gate transistors is equal to the thickness of gate insulating films of the memory transistors.

[1292] Such a semiconductor memory may be produced by the following process. FIGS. **1259** to **1283** and FIGS. **1284** to **1308** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating an EEPROM memory cell array.

[1293] First, on a surface of a p-type silicon substrate **1100**, a silicon oxide film **1410** is deposited as a first insulating film to be an implantation protective film to a thickness of **2** to **20** nm and a first impurity layer **1710** is formed on the p-type silicon substrate **1100** by ion implantation (FIGS. **1259** and **1284**). For example, the ion implantation may be performed at an implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{14} to $1 \times 10^{16}/\text{cm}^2$ in a direction inclined by about 0 to 7° with respect to the normal line of the surface of the substrate. Alternatively, instead of the channel ion implantation, an oxide film containing arsenic may be deposited by CVD with a view to utilizing diffusion of arsenic from the oxide film. The first impurity layer **1710** may not be formed on the topmost surface of the p-type silicon substrate **1100**.

[1294] Using a resist film **R5** patterned by a known photolithographic technique as a mask (FIGS. **1260** and **1285**), the first insulating film **1410** and the p-type silicon substrate **1100** are etched by 200 to 2,000 nm by reactive ion

etching so that the first impurity layer 1710 is separated, thereby forming a second trench 1220.

[1295] After the resist film R5 is removed (FIGS. 1261 and 1286), a silicon oxide film 1420, for example, is deposited as a fifth insulating film to a thickness of 100 to 300 nm and buried in the second trench 1220 by etch-back. The silicon oxide film 1420 may be buried by isotropic or anisotropic etch-back, CMP, or a combination in various ways. At this time, the silicon oxide film 1420 may be a silicon nitride film. The silicon oxide film 1410 may be removed or may remain.

[1296] For example, if the silicon oxide film 1410 is removed, a silicon nitride film 1310, for example, is formed as a second insulating film to a thickness of 2,000 to 20,000 nm on the p-type silicon substrate 1100 or the first impurity layer 1710 (FIGS. 1262 and 1287).

[1297] Subsequently, using a resist film R6 patterned by a known photolithographic technique as a mask (FIGS. 1263 and 1288), the silicon nitride film 1310 is etched by reactive ion etching, for example, to form a fourth trench 1240 in a lattice form. Then, a silicon oxide film 1421, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD in the lattice-form fourth trench 1240.

[1298] Thereafter, the silicon oxide film 1421 is buried in the fourth trench 1240 to a desired depth, for example, by isotropic etching (FIGS. 1264 and 1289). On the surface of the silicon nitride film 1310, a silicon oxide film 1431, for example, is deposited as a fourth insulating film to a thickness of 1 to 10 nm and a polysilicon film 1511, for example, is deposited as a first conductive film to a thickness of about 100 to 500 nm (FIGS. 1265 and 1290).

[1299] The polysilicon film 1511 is then etched back into the form of a sidewall spacer of a desired height (FIGS. 1266 and 1291). At this time, by setting the intervals between the fourth trenches 1240 in a direction of A-A' in FIG. 1 to a predetermined value or smaller, the polysilicon film 1511 is formed into a second wiring layer to be a selection gate line continuous in the direction without need to use a masking process.

[1300] Thereafter, a silicon oxide film 1422, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm in the fourth trench 1240 and buried in the fourth trench 1240 to a desired depth by isotropic etching. Then, on the surface of the silicon nitride film 1310, a silicon oxide film 1432, for example, is deposited as a fourth insulating film to a thickness of 1 to 10 nm (FIGS. 1267 and 1292) and a polysilicon film 1512, for example, is deposited as a first conductive film to a thickness of about 50 to 200 nm (FIGS. 1268 and 1293).

[1301] In the same manner, the polysilicon film 1512 is etched back into the form of a sidewall spacer of a desired height (FIGS. 1269 and 1294). At this time, the polysilicon films 1512 (the first conductive films) are formed to surround the silicon nitride film 1310, respectively, and isolated from each other.

[1302] Subsequently, an interlayer insulating film 1612 is formed on the surface of the polysilicon film 1512 (FIG. 1270 and FIG. 1295). This interlayer insulating film 1612 may be formed of an ONO film. The ONO film can be formed in the same manner as Production example 1.

[1303] Then, in the same manner, a polysilicon film 1522, for example, is deposited as a second conductive film to a thickness of 15 to 150 nm (FIGS. 1271 and 1296) and etched back to a depth corresponding to the deposit thickness, thereby the interlayer insulating film 1612 on the silicon oxide film 1422 is exposed and the polysilicon film 1522 is disposed on the side of the polysilicon film 1512 (the first conductive film) with intervention of the interlayer insulating film 1612. At this time, a polysilicon film 1526 (a second conductive film) remains around the silicon nitride film 1310. Preferably the polysilicon film 1522 and the polysilicon film 1526 are separated (FIGS. 1272 and 1297). At this time, by setting the intervals between the fourth trenches 1240 in a direction of A-A' in FIG. 1 to a predetermined value or smaller, the polysilicon film 1522 is formed into a third wiring layer to be a control gate line continuous in the direction without need to use a masking process.

[1304] Thereafter, a silicon oxide film 1423, for example, is deposited as a fifth insulating film in the fourth trench 1240 to a thickness of 50 to 500 nm, and then buried in the fourth trench 1240 to a desired depth by isotropic etching (FIGS. 1273 and 1298). Using the silicon oxide film 1423 as a mask, the exposed polysilicon film 1526 is removed by isotropic etching (FIGS. 1274 and 1299). At this time, the etching is performed in an etching amount corresponding to the thickness of the polysilicon film 1526. Thereby, variations in the production process can be reduced.

[1305] Subsequently, the polysilicon film 1526 remaining between the silicon nitride film 1310 and the silicon oxide film 1423 is removed by isotropic or anisotropic etching (FIGS. 1275 and 1300).

[1306] Then, a silicon oxide film 1483, for example, is deposited as a sixth insulating film to a thickness of 8 to 80 nm such that it is buried in a space between the silicon nitride film 1310 and the silicon oxide film 1423. At this time, it is preferred that the thickness of the silicon oxide film 1483 is about half or more of the thickness of the polysilicon film 1522 (FIGS. 1276 and 1301).

[1307] Then, isotropic etching is performed to a depth corresponding to the deposit thickness of the silicon oxide film 1483, thereby the interlayer insulating film 1612 present on the side of the silicon nitride film 1310 is exposed and the silicon oxide film 1483 is buried in the fourth trench 1240.

[1308] Here, explanation is given of the formation of the polysilicon film 1522 as the second conductive film. However, the polysilicon film 1522 may be formed into the form of a sidewall spacer merely by a combination of deposition and anisotropic etching. Thereafter, using the silicon oxide film 1423 as a mask, the interlayer insulating film 1612 is partially removed by isotropic etching (FIGS. 1277 and 1302).

[1309] By repeating likewise, a polysilicon film 1523 is disposed as a second conductive film on the side of a polysilicon film 1513 with intervention of an interlayer insulating film 1613, and then the polysilicon film 1523 is buried by forming thereon a silicon oxide film 1424 (a fifth insulating film) and a silicon oxide film 1484 (a sixth insulating film) (FIGS. 1278 and 1303). With regard to a polysilicon film 1514 which is the topmost first conductive film, the polysilicon film 1514 is etched back in the same manner as the polysilicon film 1511 which is the bottommost first conductive film.

[1310] Thereafter, a silicon oxide film 1425, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm and the top of the silicon nitride film 1310 is exposed by etch-back or by CMP (FIGS. 1279 and 1304). At this time, the silicon oxide film 1425 may be a silicon nitride film.

[1311] Then, the silicon nitride film 1310 is selectively removed by isotropic etching to form a first trench 1210. Then, a silicon oxide film 1440 is formed as a third insulating film to be a tunnel oxide film to a thickness of about 10 nm by CVD on the inner wall of the first trench 1210 (FIGS. 1280 and 1305). The silicon oxide film 1440, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[1312] Subsequently, the silicon oxide film 1440 formed on the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 is selectively removed. For example, the silicon oxide film 1440 is anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench 1210 (FIGS. 1281 and 1306).

[1313] Thereafter, the silicon oxide film 1440 is subjected to thermal treatment or the like in a nitrogen atmosphere at 800 to 1,000° C. for 10 to 100 minutes. At this time, gases other than nitrogen, e.g., oxygen, may be added. After the thermal treatment, the thickness of the silicon oxide film 1440 is preferably about 10 nm.

[1314] Then, an oxide film generated on the surface of the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 is optionally removed by using diluted HF, for example, and island-like semiconductor layers 1721 to 1725 and 1111 to 1114 are buried in the first trench 1210. For example, from the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 located at the bottom of the first trench 1210, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer 1721, a P-type semiconductor layer 1111, an N-type semiconductor layer 1722, a P-type semiconductor layer 1112, an N-type semiconductor layer 1723, a P-type semiconductor layer 1113, an N-type semiconductor layer 1724, a P-type semiconductor layer 1114, and an N-type semiconductor layer 1725 are formed sequentially (FIGS. 1282 and 1307). The N-type semiconductor layers 1721 to 1725 are formed at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layers 1111 to 1114 are formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Further, it is preferable that the N-type semiconductor layers 1721 and 1722 are overlapped with the polysilicon film 1511 (the first conductive film) with intervention of the silicon oxide film 1440 (the third insulating film), respectively. In the same manner, it is preferred that the N-type semiconductor layers 1722 and 1723 are overlapped with the polysilicon film 1512, the N-type semiconductor layers 1723 and 1724 are overlapped with the polysilicon film 1513, and the N-type semiconductor layers 1724 and 1725 are overlapped with the polysilicon film 1514, with intervention of the silicon oxide film 1440, respectively.

[1315] Thereafter, the N-type semiconductor layer 1725 is reduced by etch-back or CMP, for example, to expose the silicon oxide film 1425 (the fifth insulating film). Thereby the N-type semiconductor layer 1725 is separated. Then, a fourth wiring layer is formed so that its direction crosses the

direction of the second or third wiring layer and is connected to the top portion of the N-type semiconductor layer 1725.

[1316] Thereafter, by known techniques, an interlayer insulating film is formed, and a contact hole and metal wiring are formed. Thereby, a semiconductor memory is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film).

[1317] In this example, films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film (the second insulating film) 1310 may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. With regard to the polysilicon films 1511 to 1514 (the first conductive films) and the polysilicon films 1522 and 1523 (the second conductive films), impurity introduction may be carried out during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the impurity introduction to the polysilicon films is not particularly limited so long as these films become conductive films.

[1318] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1319] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1320] The charge storage layer may be formed of not only the floating gate structure but also a laminated insulating film. This example is also applicable even if MNOS or MONOS structure is employed. The laminated insulating film mentioned herein signifies a laminated structure of a tunnel oxide film and a silicon nitride film, or a structure including a tunnel oxide film, a silicon nitride film and a silicon oxide film.

[1321] Production Example 70

[1322] In a semiconductor memory to be produced in this example, selection gates and control gates are formed, and laminated insulating films are formed as charge storage layers. Then, island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors. Tunnel oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer. Further, the thickness of gate insulating films of the selection gate transistors is equal to the thickness of gate insulating films of the memory transistors.

[1323] Such a semiconductor memory may be produced by the following process. FIGS. 1309 to 1326 and FIGS.

1327 to **1344** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 12** illustrating an NMOS or MONOS memory cell array.

[**1324**] This example is same as Production example 69 (FIGS. **1259** to **1283** and **1284** to **1308**) until the silicon nitride film **1310** is etched by reactive ion etching by using the resist film **R6** as a mask to form the lattice-form fourth trench **1240** (FIGS. **1309** to **1313** and **1327** to **1331**).

[**1325**] Then, a silicon oxide film **1421**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD in the lattice-form fourth trench **1240**.

[**1326**] Thereafter, the silicon oxide film **1421** is buried in the fourth trench **1240** to a desired depth, for example, by isotropic etching (FIGS. **1314** and **1332**). On the surface of the silicon nitride film **1310**, a silicon oxide film **1431**, for example, is deposited as a fourth insulating film to a thickness of 1 to 10 nm and a polysilicon film **1511**, for example, is deposited as a first conductive film to a thickness of about 100 to 500 nm (FIGS. **1315** and **1333**).

[**1327**] The polysilicon film **1511** is etched back in the form of a sidewall spacer of a desired height (FIGS. **1316** and **1334**). At this time, by setting the intervals between the fourth trenches **1240** in a direction of A-A' in **FIG. 12** to a predetermined value or smaller, the polysilicon film **1511** is formed into a second wiring layer to be a selection gate line continuous in the direction without need to use a masking process.

[**1328**] Thereafter, a silicon oxide film **1422**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm in the fourth trench **1240** and buried in the fourth trench **1240** to a desired depth by isotropic etching (FIGS. **1317** and **1335**).

[**1329**] By repeating likewise, a polysilicon film (a first conductive film) **1512**, a silicon oxide film (a fifth insulating film) **1423**, a polysilicon film (a first conductive film) **1513**, a silicon oxide film (a fifth insulating film) **1424**, a polysilicon film (a first conductive film) **1514** and a silicon oxide film (a fifth insulating film) **1425** are formed sequentially (FIGS. **1318** and **1336**).

[**1330**] Thereafter, the top of the silicon nitride film **1310** is exposed by etch-back or CMP (FIGS. **1319** and **1337**). At this time, the silicon oxide film **1425** may be a silicon nitride film.

[**1331**] Then, the silicon nitride film **1310** is selectively removed by isotropic etching to form a first trench **1210**.

[**1332**] Then, a silicon oxide film **1440** is formed as a third insulating film to be a gate oxide film to a thickness of about 10 nm by CVD on the inner wall of the first trench **1210**. The silicon oxide film **1440**, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[**1333**] Subsequently, the silicon oxide film **1440** formed on the first impurity diffusion layer **1710** or the p-type silicon substrate **1100** is selectively removed. For example, the silicon oxide film **1440** anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench **1210** (FIGS. **1320** and **1338**).

[**1334**] Thereafter, the silicon oxide film **1440** is subjected to thermal treatment or the like in a nitrogen atmosphere at

800 to 1,000° C. for 10 to 100 minutes. At this time, gases other than nitrogen, e.g., oxygen, may be added. After the thermal treatment, the thickness of the silicon oxide film **1440** is preferably about 10 nm.

[**1335**] An oxide film generated on the surface of the first impurity diffusion layer **1710** or the p-type silicon substrate **1100** is optionally removed by using diluted HF, for example, and island-like semiconductor layers **1721**, **1722-1** and **1111** are buried in the first trench **1210**. For example, from the first impurity diffusion layer **1710** or the p-type silicon substrate **1100** located at the bottom of the first trench **1210**, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer **1721**, a P-type semiconductor layer **1111** and an N-type semiconductor layer **1722-1** are formed sequentially (FIGS. **1321** and **1339**). The N-type semiconductor layers **1721** and **1722-1** are formed at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layer **1111** is formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Further, it is preferable that the N-type semiconductor layers **1721** and **1722-1** are overlapped with the polysilicon film **1511** (the first conductive film) with intervention of the silicon oxide film **1440** (the third insulating film), respectively. Further, it is preferred that the N-type semiconductor layer **1722-1** is formed such that it is not overlapped with the polysilicon film **1512** (the first conductive film).

[**1336**] Then, using the N-type semiconductor layer **1722-1** as a mask, the silicon oxide film **1440** is partially removed.

[**1337**] Subsequently, a laminated insulating film **1620** to be charge storage layer is formed on the inner wall of the first trench **1210** (FIGS. **1322** and **1340**). In the case of forming a laminated insulating film of MNOS structure, a silicon nitride film of 4 to 10 nm thickness and a silicon oxide film of 2 to 5 nm thickness may be formed sequentially on the surface of the polysilicon film by CVD. Alternatively, a silicon nitride film of 4 to 10 nm thickness is deposited on the surface of the polysilicon film by CVD and the surface of the silicon nitride film is oxidized to form a silicon oxide film of 2 to 5 nm thickness. In order to form a laminated insulating film of MONOS structure, a silicon oxide film of 2 to 5 nm thickness, a silicon nitride film of 4 to 8 nm thickness and a silicon oxide film of 2 to 5 nm thickness are deposited sequentially on the surface of the polysilicon film by CVD. Alternatively, a silicon oxide film of 2 to 5 nm thickness and a silicon nitride film of 4 to 10 nm thickness are sequentially deposited on the surface of the polysilicon film by CVD, and then the surface of the silicon nitride film is oxidized to form a silicon oxide film of 2 to 5 nm thickness, or alternatively, the surface of the polysilicon film may be oxidized to form a silicon oxide film of 2 to 5 nm thickness. These processes may be combined in any way.

[**1338**] Then, the laminated insulating film **1620** formed on the N-type semiconductor layer **1722-1** is selectively removed. For example, the laminated insulating film **1620** is anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench **1210** (FIGS. **1323** and **1341**). Thereafter, the laminated insulating film **1620** may be subjected to thermal treatment or the like.

[**1339**] In the same manner as the above, island-like semiconductor layers **1722-2** to **1724-1**, **1112** and **1113** are buried

in the first trench **1210**. For example, from the island-like semiconductor layer **1722-1** located at the bottom of the first trench **1210**, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer **1722-2**, a P-type semiconductor layer **1112**, an N-type semiconductor layer **1723**, a P-type semiconductor layer **1113** and an N-type semiconductor layer **1724-1** are formed sequentially. The N-type semiconductor layers **1722-2** to **1724-1** are formed in the same manner as the above, i.e., at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layers **1112** and **1113** are formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. It is preferable that the N-type semiconductor layers **1722-2** and **1723** are overlapped with the polysilicon film **1512** (the first conductive film) with intervention of the laminated insulating film **1620**, respectively. It is also preferable that the N-type semiconductor layers **1723** and **1724-1** are overlapped with the polysilicon film **1513** (the first conductive film) with intervention of the laminated insulating film **1620**, respectively. Further, it is preferred that the N-type semiconductor layer **1724-1** is formed such that it is not overlapped with the polysilicon film **1514** (the first conductive film).

[1340] Then, using the N-type semiconductor layer **1724-1** as a mask, the laminated insulating film **1620** is partially removed. A silicon oxide film **1444** is formed as a third insulating film to be a gate oxide film to a thickness of about 10 nm by CVD on the inner wall of the first trench **1210**. The silicon oxide film **1444**, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[1341] Subsequently, the silicon oxide film **1444** formed on the island-like semiconductor layer **1724-1** is selectively removed. For example, the silicon oxide film **1444** is anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench **1210** (FIGS. 1324 and 1342).

[1342] Thereafter, the silicon oxide film **1444** is subjected to thermal treatment or the like. Further, in the same manner as the above, island-like semiconductor layers **1724-2**, **1725** and **1114** are buried in the first trench **1210**. For example, from the island-like semiconductor layer **1724-1** located at the bottom of the first trench **1210**, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer **1724-2**, a P-type semiconductor layer **1114** and an N-type semiconductor layer **1725** are formed sequentially (FIGS. 1325 and 1343). The N-type semiconductor layers **1724-2** and **1725** are formed in the same manner as the above, i.e., at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layer **1114** is formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. It is preferable that the N-type semiconductor layers **1724-2** and **1725** are overlapped with the polysilicon film **1514** (the first conductive film) with intervention of the silicon oxide film **1444** (the third insulating film), respectively. Thereafter, the N-type semiconductor layer **1725** is reduced by etch-back or CMP, for example, to expose the silicon oxide film **1425** (the fifth insulating film). Thereby the N-type semiconductor layer **1725** is separated. Then, a fourth wiring layer is formed so that its direction crosses the direction of the second or third wiring layer and is connected to the top portion of the N-type semiconductor layer **1725**.

[1343] Thereafter, by known techniques, an interlayer insulating film is formed, and a contact hole and metal wiring are formed. Thereby, a semiconductor memory is realized which has a memory function according to the state of a charge in the charge storage layer formed of the laminated insulating film.

[1344] In this example, the silicon nitride film (the second insulating film) **1310** formed on the surface of the semiconductor substrate or the polysilicon film may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. With regard to the polysilicon films **1511** to **1514** (the first conductive films) and the polysilicon films **1522** and **1523** (the second conductive films), impurity introduction may be carried out during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the impurity introduction to the polysilicon films is not particularly limited so long as these films become conductive films.

[1345] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1346] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1347] Production Example 71

[1348] In a semiconductor memory to be produced in this example, gates to be MIS capacitors as charge storage layers and selection gates are formed, and then gate oxide films are formed. Then, island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors. The gate oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer. Further, the thickness of gate insulating films of the selection gate transistors is equal to the thickness of gate insulating films of the memory transistors.

[1349] Such a semiconductor memory may be produced by the following process. FIGS. 1345 to 1358 and FIGS. 1359 to 1372 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 13 illustrating a DRAM memory cell array.

[1350] This example is the same as Production example 70 (FIGS. 1309 to 1320 and 1327 to 1338) except that the first insulating film **1410** and the p-type silicon substrate **1100** are etched by reactive ion etching to a depth of 200 to 2,000 nm by using a resist film **R5** patterned by a known photolithographic technique as a mask (FIGS. 1260 and 1285) such that the first impurity layer **1710** is separated, thereby

forming a second trench **1220** in a direction crossing the second wiring layer to be a continuous gate line (FIGS. **1345** to **1356** and **1359** to **1370**).

[**1351**] Thereafter, an oxide film generated on the surface of the first impurity diffusion layer **1710** or the p-type silicon substrate **1100** is optionally removed by using diluted HF, for example, and island-like semiconductor layers **1721**, **1726**, **1727**, **1725**, **1111**, **1120** and **1114** are buried in the first trench **1210**. For example, from the first impurity diffusion layer **1710** or the p-type silicon substrate **1100** located at the bottom of the first trench **1210**, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer **1721**, a P-type semiconductor layer **1111**, an N-type semiconductor layer **1726**, a P-type semiconductor layer **1120**, an N-type semiconductor layer **1727**, a P-type semiconductor layer **1114** and an N-type semiconductor layer **1725** are formed sequentially (FIGS. **1357** and **1371**). The N-type semiconductor layers **1721**, **1726**, **1727** and **1725** are formed at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layers **1111**, **1120** and **1114** are formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. It is preferable that the N-type semiconductor layers **1721** and **1726** are overlapped with the polysilicon film **1511** (the first conductive film) with intervention of the silicon oxide film **1440** (the third insulating film), respectively. The N-type semiconductor layer **1726** is preferably overlapped with the polysilicon film **1512** (the first conductive film) with intervention of the silicon oxide film **1440** and in the same manner, the N-type semiconductor layer **1727** is preferably overlapped with the polysilicon film **1513** with intervention of the silicon oxide film **1440**. Further, the N-type semiconductor layers **1727** and **1725** are preferably overlapped with the polysilicon film **1514** (the first conductive film) with intervention of the silicon oxide film **1444** (the third insulating film), respectively.

[**1352**] Subsequently, the N-type semiconductor layer **1725** is reduced by etch-back or CMP, for example, to expose the silicon oxide film **1425** (the fifth insulating film). Thereby the N-type semiconductor layer **1725** is separated.

[**1353**] Then, a fourth wiring layer is formed so that its direction crosses the direction of the second or third wiring layer and is connected to the top portion of the N-type semiconductor layer **1725**.

[**1354**] Further, by known techniques, an interlayer insulating film is formed, and a contact hole and metal wiring are formed.

[**1355**] Thereby, a semiconductor memory is realized which has a memory function according to the state of a charge in the charge storage layer formed of the MIS capacitors.

[**1356**] In this example, films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film (the second insulating film) **1310** may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. With regard to the polysilicon films **1511** to **1514** (the first conductive films) and the polysilicon films **1522** and **1523** (the second conductive films), impurity introduction may be carried out during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the

impurity introduction to the polysilicon films is not particularly limited so long as these films become conductive films.

[**1357**] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[**1358**] Production Example 72

[**1359**] In a semiconductor memory to be produced in this example, a plurality of floating gates are formed as charge storage layers and selection gates and control gates are formed. Then, tunnel oxide films are formed and island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors. The tunnel oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer. Further, the thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors.

[**1360**] Such a semiconductor memory may be produced by the following process. FIGS. **1373** to **1382** and FIGS. **1383** to **1392** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating an EEPROM memory cell array.

[**1361**] In this example, production steps are the same as those of Production example 69 (FIGS. **1259** to **1279** and **1284** to **1304**) before the polysilicon films **1511** to **1514** are formed as the first insulating films, the polysilicon films **1522** and **1523** are formed as the second conductive films with intervention of the interlayer insulating films **1612** and **1613**, the silicon oxide film **1425** is deposited as the fifth insulating film to a thickness of 50 to 500 nm, and the top of the silicon nitride film **1310** is exposed by etch-back or CMP (FIGS. **1373** and **1383**).

[**1362**] Thereafter, the silicon nitride film **1310** is selectively removed by isotropic etching, for example, to form a first trench **1210**.

[**1363**] Then, a silicon oxide film **1451** is formed as a thirteenth insulating film to be a gate oxide film to a thickness of about 20 nm by CVD on the inner wall of the first trench **1210** (FIGS. **1374** and **1384**). The silicon oxide film **1451**, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[**1364**] Subsequently, the silicon oxide film **1451** formed on the first impurity diffusion layer **1710** or the p-type semiconductor layer **1100** is removed selectively. For example, the silicon oxide film **1451** is anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench **1210** (FIGS. **1325** and **1385**).

[1365] Thereafter, the silicon oxide film 1451 is subjected to a thermal treatment or the like in the same manner as in Production example 69.

[1366] Then, if required, an oxide film generated on the surface of the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 is optionally removed by using diluted HF, for example, and island-like semiconductor layers 1721, 1722-1 and 1111 are buried in the first trench 1210. For example, from the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 located at the bottom of the first trench 1210, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer 1721, a P-type semiconductor layer 1111 and an N-type semiconductor layer 1722-1 are formed sequentially (FIGS. 1376 and 1386). The N-type semiconductor layers 1721 to 1722-1 are formed at an arsenic concentration of about 1×10^{18} to $1 \times 10^{19}/\text{cm}^3$ and the P-type semiconductor layer 1111 is formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. It is preferable that the N-type semiconductor layers 1721 and 1722-1 are overlapped with the polysilicon film 1511 (the first conductive film) with intervention of the silicon oxide film 1451 (the thirteenth insulating film), respectively. Further, it is preferred that the N-type semiconductor layer 1722-1 is formed such that it is not overlapped with the polysilicon film 1512 (the first conductive film).

[1367] Then, using the N-type semiconductor layer 1722-1 as a mask, the silicon oxide film 1451 is partially removed (FIGS. 1377 and 1387). A silicon oxide film 1440, for example, is formed as a third insulating film to be a tunnel oxide film to a thickness of about 10 nm by CVD on the inner wall of the first trench 1210 (FIGS. 1378 and 1388).

[1368] Subsequently, the silicon oxide film 1440 formed on the N-type semiconductor layer 1722-1 is selectively removed. For example, the silicon oxide film 1440 is anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench 1210 (FIGS. 1379 and 1389).

[1369] Thereafter, the silicon oxide film 1440 may be subjected to thermal treatment or the like.

[1370] In the same manner as the above, island-like semiconductor layers 1722-2 to 1724-1, 1112 and 1113 are buried in the first trench 1210. For example, from the island-like semiconductor layer 1722-1 located at the bottom of the first trench 1210, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer 1722-2, a P-type semiconductor layer 1112, an N-type semiconductor layer 1723, a P-type semiconductor layer 1113 and an N-type semiconductor layer 1724-1 are formed sequentially (FIGS. 1380 and 1390). The N-type semiconductor layers 1722-2 to 1724-1 are formed in the same manner as the above, i.e., at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layers 1112 and 1113 are formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Further, it is preferable that the N-type semiconductor layers 1722-2 and 1723 are overlapped with the polysilicon film 1512 (the first conductive film) with intervention of the silicon oxide film 1440 (the third insulating film), respectively. In the same manner, the N-type semiconductor layers 1723 and

1724-1 are preferably overlapped with the polysilicon film 1513 (the first conductive film) with intervention of the silicon oxide film 1440, respectively. Further, it is preferred that the N-type semiconductor layer 1724-1 is formed such that it is not overlapped with the polysilicon film 1514 (the first conductive film).

[1371] Using the N-type semiconductor layer 1724-1 as a mask, the silicon oxide film 1440 is partially removed.

[1372] Then, a silicon oxide film 1454 is formed as a thirteenth insulating film to be a gate oxide film to a thickness of about 20 nm by CVD on the inner wall of the first trench 1210. The silicon oxide film 1454, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[1373] Subsequently, the silicon oxide film 1454 formed on the island-like semiconductor layer 1724-1 is selectively removed. For example, the silicon oxide film 1454 is anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench 1210.

[1374] Thereafter, the silicon oxide film 1454 is subjected to a thermal treatment or the like.

[1375] In the same manner as the above, island-like semiconductor layers 1724-2, 1725 and 1114 are buried in the first trench 1210. For example, from the island-like semiconductor layer 1724-1 located at the bottom of the first trench 1210, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer 1724-2, a P-type semiconductor layer 1114 and an N-type semiconductor layer 1725 are formed sequentially (FIGS. 1381 and 1391). The N-type semiconductor layers 1724-2 and 1725 are formed in the same manner as the above at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layer 1114 is formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. It is preferable that the N-type semiconductor layers 1724-2 and 1725 are overlapped with the polysilicon film 1514 (the first conductive film) with intervention of the silicon oxide film 1454 (the third insulating film), respectively.

[1376] Thereafter, the N-type semiconductor layer 1725 is reduced by etch-back or CMP, for example, to expose the silicon oxide film 1425 (the fifth insulating film). Thereby the N-type semiconductor layer 1725 is separated.

[1377] Then, a fourth wiring layer is formed so that its direction crosses the direction of the second or third wiring layer and is connected to the top portion of the N-type semiconductor layer 1725.

[1378] Thereafter, by known techniques, an interlayer insulating film is formed, and a contact hole and metal wiring are formed.

[1379] According to this example, the same effect as obtained by Production Example 69 can be obtained (FIGS. 1259 to 1283 and 1284 to 1308).

[1380] Production Example 73

[1381] In a semiconductor memory to be produced in this example, a plurality of floating gates are formed as charge storage layers on a semiconductor substrate to which an oxide film is inserted, for example, a semiconductor portion on an oxide film of an SOI substrate, selection gates and

control gates are formed, and then tunnel oxide films are formed. Then, island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors. The tunnel oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer. Further, the thickness of gate insulating films of the selection gate transistors is equal to the thickness of gate insulating films of the memory transistors.

[1382] Such a semiconductor memory may be produced by the following process. FIGS. 1393 and 1394 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array.

[1383] In this example, production steps are substantially the same as those of Production example 1 except that the SOI substrate is used as a semiconductor substrate (FIGS. 1393 and 1394) and the same effect as obtained by Production Example 69 can be obtained. Further, the junction capacitance of the impurity diffusion layer 1710 which functions as the first wiring layer is suppressed or removed. The use of the SOI substrate as the semiconductor substrate is applicable to all the examples of the present invention.

[1384] Production Example 74

[1385] In a semiconductor memory to be produced in this example, a plurality of floating gates are formed as charge storage layers and control gates are formed. Then, tunnel oxide films are formed and island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Two memory transistors are placed in the island-like semiconductor layer. The tunnel oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer.

[1386] Such a semiconductor memory may be produced by the following process. FIGS. 1395 to 1415 and 1416 to 1436 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 5 illustrating an EEPROM memory cell array.

[1387] In this example, a silicon oxide film 1410, for example, is deposited as a first insulating film to be an injection protective film to a thickness of 2 to 20 nm on a surface of a p-type silicon substrate 1100, and a first impurity layer 1710 is formed on the p-type silicon substrate 1100 by ion implantation (FIGS. 1395 and 1416). For example, the ion implantation may be performed at implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{14} to $1 \times 10^{16}/\text{cm}^2$ in a direction inclined by about 0 to 7° with respect to the normal line of the surface of the substrate. Alternatively, instead of the channel ion implantation, an oxide film containing arsenic may be deposited by CVD with a view to utilizing diffusion of arsenic from the oxide

film. The first impurity layer 1710 may not be formed on the topmost surface of the p-type silicon substrate 1100.

[1388] Using a resist film R5 patterned by a known photolithographic technique as a mask, the first insulating film 1410 and the P-type silicon substrate 1100 are etched by 200 to 2,000 nm by reactive ion etching so that the first impurity layer 1710 is separated, thereby forming a second trench 1220 (FIGS. 1396 and 1417).

[1389] After the resist film R5 is removed, a silicon oxide film 1420, for example, is deposited as a fifth insulating film to a thickness of 100 to 300 nm and buried in the second trench 1220 by etch-back (FIGS. 1397 and 1418). The silicon oxide film 1420 may be buried by isotropic or anisotropic etch-back, CMP, or a combination in various ways. At this time, the silicon oxide film 1420 may be a silicon nitride film. The silicon oxide film 1410 may be removed or may remain. For example, if the silicon oxide film 1410 is removed, a silicon nitride film 1310, for example, is formed as a second insulating film to a thickness of 1,000 to 10,000 nm on the p-type silicon substrate 1100 or the first impurity layer 1710 (FIGS. 1398 and 1419).

[1390] Subsequently, using a resist film R6 patterned by a known photolithographic technique as a mask, the silicon nitride film 1310 is etched by reactive ion etching, for example, to form a fourth trench 1240 in a lattice form (FIGS. 1399 and 1420).

[1391] Then, a silicon oxide film 1421, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD in the lattice-form fourth trench 1240.

[1392] The silicon oxide film 1421 is buried in the fourth trench 1240 to a desired depth, for example, by isotropic etching (FIGS. 1400 and 1421). Then, on the surface of the silicon nitride film 1310, a silicon oxide film 1431, for example, is deposited as a fourth insulating film to a thickness of 1 to 10 nm and a polysilicon film 1511, for example, is deposited as a first conductive film to a thickness of about 50 to 200 nm (FIGS. 1401 and 1422).

[1393] In the same manner, the polysilicon film 1511 is etched back in the form of a sidewall spacer of a desired height (FIGS. 1402 and 1422). At this time, the polysilicon films 1511 (the first conductive films) are formed to surround the silicon nitride films 1310, respectively, and isolated from each other.

[1394] Subsequently, an interlayer insulating film 1611 is formed on the surface of the polysilicon film 1511 (FIG. 1403 and FIG. 1424). This interlayer insulating film 1611 may be formed of an ONO film. The ONO film may be formed in the same manner as in Production example 1.

[1395] Then, in the same manner, a polysilicon film 1521, for example, is deposited as a second conductive film to a thickness of 15 to 150 nm (FIGS. 1404 and 1425) and etched back to a depth corresponding to the deposit thickness, thereby the interlayer insulating film 1611 on the silicon oxide film 1421 is exposed and the polysilicon film 1521 is disposed on the side of the polysilicon film 1511 (the first conductive film) with intervention of the interlayer insulating film 1611. At this time, a polysilicon film 1525 (a second conductive film) remains around the silicon nitride film 1310. It is preferable that the polysilicon film 1521 and the polysilicon film 1525 are separated (FIGS. 1405 and

1426). At this time, by setting the intervals between the fourth trenches 1240 in a direction of A-A' in FIG. 5 to a predetermined value or smaller, the polysilicon film 1521 is formed into a third wiring layer to be a control gate line continuous in the direction without need to use a masking process.

[1396] Thereafter, a silicon oxide film 1422, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm.

[1397] Then, a silicon oxide film 1422, for example, is buried as a fifth insulating film in the fourth trench 1240 to a desired depth by isotropic etching (FIGS. 1406 and 1427). Using the silicon oxide film 1422 as a mask, the exposed polysilicon film 1525 is removed by isotropic etching (FIGS. 1407 and 1428). At this time, the etching is performed in an etching amount corresponding to the thickness of the polysilicon film 1525. Thereby, variations in the production process can be reduced.

[1398] Subsequently, the polysilicon film 1525 remaining between the silicon nitride film 1310 and the silicon oxide film 1422 is removed by isotropic or anisotropic etching (FIGS. 1408 and 1429).

[1399] Then, a silicon oxide film 1482, for example, is deposited as a sixth insulating film to a thickness of 8 to 80 nm such that it is buried in a space between the silicon nitride film 1310 and the silicon oxide film 1422. At this time, it is preferred that the thickness of the silicon oxide film 1482 is about half or more of the thickness of the polysilicon film 1521 (FIGS. 1409 and 1430).

[1400] Then, isotropic etching is performed to a depth corresponding to the deposit thickness of the silicon oxide film 1482, thereby the interlayer insulating film 1611 present on the side of the silicon nitride film 1310 is exposed and the silicon oxide film 1482 is buried in the fourth trench 1240 (FIGS. 1410 and 1431). Here, explanation is given of the formation of the polysilicon film 1521 as the second conductive film. However, the polysilicon film 1521 may be formed into the form of a sidewall spacer merely by a combination of deposition and anisotropic etching.

[1401] Thereafter, using the silicon oxide film 1422 as a mask, the interlayer insulating film 1611 is partially removed by isotropic etching, for example (FIGS. 1411 and 1423).

[1402] By repeating likewise, a polysilicon film 1522 is disposed as a second conductive film on the side of a polysilicon film 1512 with intervention of an interlayer insulating film 1612, and then the polysilicon film 1522 is buried by forming thereon a silicon oxide film 1423 (a fifth insulating film) and a silicon oxide film 1483 (a sixth insulating film).

[1403] The top of the silicon nitride film 1310 is exposed by etch-back or by CMP (FIGS. 1412 and 1433). At this time, the silicon oxide film 1423 may be a silicon nitride film.

[1404] The silicon nitride film 1310 is selectively removed by isotropic etching to form a first trench 1210.

[1405] Then, a silicon oxide film 1440 is formed as a third insulating film to be a tunnel oxide film to a thickness of about 10 nm by CVD on the inner wall of the first trench

1210 (FIGS. 1413 and 1434). The silicon oxide film 1440, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[1406] Subsequently, the silicon oxide film 1440 formed on the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 is selectively removed. For example, the silicon oxide film 1440 is anisotropically etched to remain in the form of a sidewall spacer only on the sidewall of the first trench 1210.

[1407] The silicon oxide film 1440 is subjected to thermal treatment or the like in the same manner as in Production example 69.

[1408] Then, if required, an oxide film generated on the surface of the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 is optionally removed by using diluted HF, for example, and island-like semiconductor layers 1721 to 1723, 1111 and 1112 are buried in the first trench 1210. For example, from the first impurity diffusion layer 1710 or the p-type silicon substrate 1100 located at the bottom of the first trench 1210, the semiconductor layers are formed selectively by epitaxial growth. At this time, from the bottom, an N-type semiconductor layer 1721, a P-type semiconductor layer 1111, an N-type semiconductor layer 1722, a P-type semiconductor layer 1112 and an N-type semiconductor layer 1723 are sequentially formed (FIGS. 1414 and 1435). The N-type semiconductor layers 1721 to 1723 are formed at an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ and the P-type semiconductor layers 1111 and 1112 are formed at a boron concentration of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. It is preferable that the N-type semiconductor layers 1721 and 1722 are overlapped with the polysilicon film 1511 (the first conductive film) with intervention of the silicon oxide film 1440 (the third insulating film), respectively. It is also preferred that the N-type semiconductor layers 1722 and 1723 are overlapped with the polysilicon film 1512 (the first conductive film) with intervention of the silicon oxide film 1440 (the third insulating film), respectively.

[1409] Thereafter, the N-type semiconductor layer 1723 is reduced by etch-back or CMP, for example, to expose the silicon oxide film 1423 (the fifth insulating film). Thereby the N-type semiconductor layer 1723 is separated.

[1410] Then, a fourth wiring layer is formed so that its direction crosses the direction of the second or third wiring layer and is connected to the top portion of the N-type semiconductor layer 1723.

[1411] Thereafter, by known techniques, an interlayer insulating film is formed, and a contact hole and metal wiring are formed. Thereby, a semiconductor memory is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film) (FIGS. 1415 and 1436).

[1412] In this example, films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film (the second insulating film) 1310 may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. With regard to the polysilicon films 1511 and 1512 (the first conductive films) and the polysilicon films 1521 and 1522 (the second conductive films), impurity introduction may be carried out

during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the impurity introduction to the polysilicon films is not particularly limited so long as these films become conductive films.

[1413] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1414] Production Example 75

[1415] In a semiconductor memory to be produced in this example, a plurality of floating gates are formed as charge storage layers and selection gates and control gates are formed. Then, tunnel oxide films are formed and island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active regions of memory cells are electrically in common. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors. The tunnel oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer. Further, the thickness of gate insulating films of the selection gate transistors is equal to the thickness of gate insulating films of the memory transistors.

[1416] Such a semiconductor memory may be produced by the following process. FIGS. 1437 to 1439 and FIGS. 1440 to 1442 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array. FIGS. 1443 to 1445 and FIGS. 1446 to 1448 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array.

[1417] In this example, production steps are the same as those of Production example 69 (FIGS. 1259 to 1277 and 1284 to 1302) until the polysilicon film 1522 (the second conductive film) is disposed on the side of the polysilicon film 1512 (the first conductive film) with intervention of the interlayer insulating film 1612. However, in the step of burying the silicon oxide film 1423 (the fifth insulating film) in the fourth trench 1240, the silicon oxide film 1423 is formed on the polysilicon film 1522 to a controlled thickness of about 20 to 40 nm. Alternatively, the polysilicon film 1522 is exposed to form a thermally oxidized film of about 20 to 40 nm thick (FIGS. 1437 and 1440). At this time, by setting the interval between the polysilicon films 1512 and 1513 which are formed as first conductive films to be floating gates of memory cells to 20 to 30 nm (FIGS. 1438 and 1441), an impurity diffusion layer 1723, which is one of the island-like semiconductor layers 1721 to 1725 to be formed in the first trench 1210 in a later step, need not to be formed between the memory cells (FIGS. 1439 and 1442).

[1418] In another example, production steps are the same as those of Production example 69 (FIGS. 1259 to 1266 and 1284 to 1291) until the polysilicon film (the first conductive

film) 1511 is formed. However, between the selection gate and the memory cell, the silicon oxide film 1422 (the fifth insulating film) to be buried in the fourth trench 1240 is formed on the polysilicon film 1521 (the first conductive film) to a controlled thickness of about 20 to 40 nm. Alternatively, the polysilicon film 1521 is exposed to form a thermally oxidized film of about 20 to 40 nm thick (FIGS. 1443 and 1446).

[1419] Further, between the memory cells, the silicon oxide film 1423 (the fifth insulating film) to be buried in the fourth trench 1240 is formed on the polysilicon film 1522 (the second conductive film) to a controlled thickness of about 20 to 40 nm. Alternatively, the polysilicon film 1522 is exposed to form a thermally oxidized film of about 20 to 40 nm thick (FIGS. 1444 and 1447). At this time, by setting the interval between the polysilicon films 1512 and 1513 which are formed as first conductive films to be floating gates of memory cells to 20 to 30 nm, impurity diffusion layers 1722, 1723 and 1724, which are the island-like semiconductor layers to be formed in the first trench 1210 in a later step, need not to be formed between the selection gate and the memory cell (FIGS. 1445 and 1448).

[1420] Production Example 76

[1421] In a semiconductor memory to be produced in this example, a plurality of floating gates are formed as charge storage layers and selection gates and control gates are formed. Then, tunnel oxide films are formed and island-like semiconductor layers in a pillar form are formed by selective epitaxial silicon growth. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active regions of memory cells are electrically in common. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors. The tunnel oxide films of the transistors are formed at the same time. The transistors are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is equal to the thickness of gate insulating films of the memory transistors. Transmission gates are disposed between the transistors for transmitting potentials to the active regions of the memory cell transistors.

[1422] Such a semiconductor memory may be produced by the following process. FIGS. 1449 and 1450 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array.

[1423] In this example, production steps are the same as those of Production example 69 except that the step of forming gate electrodes of the polysilicon film 1530 (the third conductive film) is added after the polysilicon films 1521, 1522, 1523 and 1524 are formed.

[1424] That is, after the formation of the polysilicon films 1521, 1522, 1523 and 1524, the silicon oxide films 1424 to 1422 (the fifth insulating films) and the interlayer insulating films 1612 and 1613 are removed by isotropic etching such that the island-like semiconductor layer 1110 is exposed between the polysilicon films 1521 and 1522 (the first conductive films).

[1425] Then, an oxide film 1400 is formed as a twenty-first insulating film on the surface of the island-like semiconduc-

tor layer **1110** between the selection gate and the memory cell and exposed surfaces of the polysilicon films **1511**, **1512**, **1513**, **1514**, **1521**, **1522**, **1523** and **1524** (the second conductive films), for example, by thermal oxidization, and then a polysilicon film **1530** is deposited as a third conductive film on the entire surface.

[1426] The polysilicon film **1530** is anisotropically etched back to such a degree that a space between the polysilicon films **1523** and **1524** is not exposed.

[1427] Then, a semiconductor memory is completed in the same manner as in Production example 69 (FIGS. **1449** and **1450**).

[1428] Production Example 77

[1429] In this example, explanation is given of an example of production process for obtaining a structure in which the direction of the first wiring layer is parallel to the direction of the fourth wiring layer. FIGS. **1451** to **1453** and **1454** to **1456** are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array.

[1430] In this example, production steps are the same as those of Production example 69 except that the first insulating film **1410** and the p-type silicon substrate **1100** are etched by 200 to 2,000 nm by reactive ion etching using a resist film **R5** patterned by a known photolithographic technique as a mask (FIGS. **1260** and **1285**) such that the first impurity layer **1710** is separated, thereby forming a second trench **1220** in a direction crossing a second wiring layer to be a continuous gate line (FIGS. **1451** to **1453** and **1454** to **1456**).

[1431] Thereby, a semiconductor memory is realized in which the first wiring layer is parallel to the fourth wiring layer and which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film).

[1432] In this example, films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film (the second insulating film) **1310** may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. With regard to the polysilicon films **1511** to **1514** (the first conductive films) and the polysilicon films **1522** and **1523** (the second conductive films), impurity introduction may be carried out during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the impurity introduction to the polysilicon films is not particularly limited so long as these films become conductive films.

[1433] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1434] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1435] Production Example 78

[1436] In this example, explanation is given of an example of production process for obtaining a structure in which the first wiring layer is electrically common to the memory array. FIGS. **1457** to **1458** and FIGS. **1459** to **1460** are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array.

[1437] In this example, the second trench **1220** is not formed in the semiconductor substrate **1100**. This example is the same as Production Example 69 from which the steps regarding the formation of the second trench **1220** is omitted.

[1438] Thereby, a semiconductor memory is realized in which at least the first wiring layer in the array is not divided but is common and which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film) (the first conductive film) (FIGS. **1457** to **1458** and FIGS. **1459** to **1460**).

[1439] Production Example 79

[1440] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of an example of production process for forming rectangular floating gates. FIGS. **1461** to **1466** and FIGS. **1467** to **1472** are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array.

[1441] In this example, for forming polysilicon films **1511** to **1514** as first conductive films, a polysilicon film **1512** (a first conductive film) covering a silicon nitride film **1310** (a second insulating film) is anisotropically etched in the form of a sidewall spacer. Then, a silicon oxide film **1462** is buried as an eighth insulating film in a space formed by the polysilicon film **1512** to a desired depth. Using the silicon oxide film **1462** as a mask, the polysilicon film **1512** is partially removed by isotropic or anisotropic etching (FIGS. **1461** to **1464** and **1467** to **1470**).

[1442] Then, the silicon oxide film **1462** is removed and the polysilicon film **1512** is arranged in the form of a rectangle. A polysilicon film **1522** (a second conductive film) may be arranged in the same manner. Further, the polysilicon films **1511** to **1514** which are selection gates may be arranged in the same manner (FIGS. **1465** to **1466** and **1471** to **1472**).

[1443] Production Example 80

[1444] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of an example of production process of forming a structure in which the side and the top of the floating gate are covered with the control gate with intervention of an inter-layer insulating film. FIGS. **1473** to **1476** and FIGS. **1477** to **1480** are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating an EEPROM memory cell array.

[1445] In this example, production steps are the same as those of Production example 69 until the polysilicon film

1522, for example, is deposited as the second conductive film to a thickness of 15 to 150 nm.

[**1446**] Then, the polysilicon film **1522** is etched back to a depth corresponding to the deposit thickness, thereby the interlayer insulating film **1612** present on the silicon oxide film **1422** (the fifth insulating film) is exposed and the polysilicon film **1522** is disposed on the side of the polysilicon film **1512** (the first conductive film) with intervention of the interlayer insulating film **1612**. At this time, a polysilicon film **1522** (a second conductive film) remains around the silicon nitride film **1310** (FIGS. **1473** and **1477**).

[**1447**] Subsequently, a silicon oxide film **1423**, for example, is deposited as a fifth insulating film in the fourth trench **1240** to a thickness of 50 to 500 nm.

[**1448**] The silicon oxide film **1423** is buried in the fourth trench **1240** to a desired depth, for example, by isotropic etching (FIGS. **1474** and **1478**). Using the silicon oxide film **1423** as a mask, the exposed polysilicon film **1522** is removed by isotropic or anisotropic etching (FIGS. **1475** and **1479**). At this time, the etching is performed in an etching amount corresponding to the thickness of the polysilicon film **1522**. Thereby, variations in the production process can be reduced.

[**1449**] Subsequently, the polysilicon film **1522** is arranged such that it remains between the silicon nitride film **1310** and the silicon oxide film **1423** (FIGS. **1476** and **1480**). Thereby, an area increases in which the polysilicon film **1512** contacts the polysilicon film **1522** with intervention of the interlayer insulating film **1612**, which improves the coupling ratio.

[**1450**] Production Example 81

[**1451**] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of an example of production process in which the transistor gates have different lengths in a vertical direction. FIGS. **1481** to **1482** and FIGS. **1483** to **1484** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating an EEPROM memory cell array.

[**1452**] In this example, regarding the polysilicon films (the first conductive films) **1511** to **1514** to be the memory cell gates or the selection gates, the selection gates of the polysilicon films **1511** and **1514** may have different lengths in a direction vertical to the semiconductor substrate **1100** as shown in FIGS. **1481** and **1483**.

[**1453**] Further, as shown in FIGS. **1482** and **1484**, the memory cell gates of the polysilicon films **1512** and **1513** may have different lengths in a direction vertical to the semiconductor substrate **1100**, and the polysilicon films **1511** to **1514** may have different vertical lengths.

[**1454**] Production Example 82

[**1455**] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of an example of production process in which the active regions of the transistors have different lengths in a vertical direction. FIGS. **1485** and **1486** are sectional views

taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating an EEPROM memory cell array.

[**1456**] In this example, regarding the semiconductor layers **1111** to **1114** to be channel regions of the memory cells or the selection transistors, the selection gates of the semiconductor layers **1111** and **1114** may have different channel lengths in a direction vertical to the semiconductor substrate **1100**, or alternatively, the memory cells of the semiconductor layers **1112** and **1113** may have different channel lengths in a direction vertical to the semiconductor substrate **1100** as shown in FIGS. **1485** and **1486**.

[**1457**] Production Example 83

[**1458**] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of an example of production process in which the impurity diffusion layer **1725** formed on the top of the island-like semiconductor layer **1110** and connected to the fourth wiring layer **1840** has a large height. FIGS. **1487** and **1488** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating an EEPROM memory cell array.

[**1459**] In this example, the impurity diffusion layer **1725** connected to the fourth wiring layer **1840** may have a large height. (FIGS. **1487** and **1488**). At this time, a silicon oxide film **1425** (a fifth insulating film) may be designed to have a large thickness and the insulating properties improve between the polysilicon film (the first conductive film) **1514** and the fourth wiring layer **1840**. Or, since an increased area of the impurity diffusion layer **1725** can be exposed, better connection is obtained between the impurity diffusion layer **1725** and the fourth wiring layer **1840**.

[**1460**] Production Example 84

[**1461**] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of an example of production process in which the impurity diffusion layer **1725** located on the top of the semiconductor layer **1110** is arranged to form the fourth wiring layer **1840**. FIGS. **1489** to **1490** and **1491** to **1492** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating an EEPROM memory cell array.

[**1462**] In this example, the semiconductor layer **1725** is arranged by reactive ion etching by using a resist film **R8** patterned by a known photolithographic technique as a mask (FIGS. **1489** and **1491**) to form a fourth wiring layer so that its direction crosses the direction of the second or third wiring layer (FIGS. **1490** and **1492**).

[**1463**] Production Example 85

[**1464**] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. FIGS. **1493** to **1494** and **1495** to **1496** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating an EEPROM memory cell array.

[**1465**] In this example, the silicon nitride film **1310** may have the top and the bottom having different outward shape

as shown in **FIGS. 1493 and 1495** through the formation of the first trench **1210** by reactive ion etching.

[1466] Also the top and the bottom of the island-like semiconductor layer **110** may be shifted in a horizontal direction as shown in **FIG. 1494** and **FIG. 1495**.

[1467] For example, in the case where the silicon nitride film **1310** is circular in plan view, the former silicon nitride film **1310** shows a truncated cone shape and the latter silicon nitride film **1310** shows an inclined column shape. The shape of the silicon nitride film **1310** is not particularly limited so long as the memory cells can be disposed in series in the direction vertical to the semiconductor substrate **1100**.

[1468] Production Example 86

[1469] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of an example of production process in which the island-like semiconductor layer **1100** has an altered shape at its bottom. **FIGS. 1497 to 1500 and 1501 to 1504** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating an EEPROM memory cell array.

[1470] In this example, the first lattice-form trench **1210** may have a linear slant shape at its bottom as shown in **FIGS. 1497 and 1501 and FIGS. 1498 and 1502**.

[1471] Alternatively, the first lattice-form trench **1210** may have a rounded slant shape at its bottom as shown in **FIGS. 1499 and 1503 and FIGS. 1500 and 1504**.

[1472] Here, the bottom of the polysilicon film (the first conductive film) **1511** may or may not reach the slant bottom of the first trench **1210**.

[1473] Production Example 87

[1474] This example shows an example of production process for producing a semiconductor memory in which floating gates are formed as charge storage layers and then island-like semiconductor layers are formed. Explanation is given of the shape of the deposited polysilicon film. **FIGS. 1505 to 1510 and 1511 to 1516** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating an EEPROM memory cell array.

[1475] The first polysilicon films **1511 to 1514** and the second polysilicon films **1521 to 1524** covering the silicon nitride film **1310** (the second insulating film) may have a shape such that it is uniformly deposited along the bottom shape of the first trench **1210** as shown in **FIGS. 1505 to 1510 and 1511 to 1516**. Alternatively, the polysilicon films may have a shape such that it is deposited partially ununiformly according to the bottom shape of the first trench **1210** as in the same manner as in Production example 69.

[1476] Production Example 88

[1477] This example shows an example of production process for producing a semiconductor memory in which the selection gates and the floating gates of the transistors are formed at the same time. Explanation is given of a production process for forming terminals which electrically connect first, second and third wiring layers to a peripheral circuit, respectively. **FIGS. 1517 to 1522** are sectional views taken on line H-H', line I1-I1', line I2-I2', line I3-I3', line

I4-I4', and line I5-I5', respectively, of **FIGS. 10 and 11** illustrating a memory cell array of EEPROM. **FIGS. 336 to 341** are also the same. These sectional views are taken at locations showing sites **1921, 1932, 1933, 1934** and **1910** where terminals mounted on the top face of the semiconductor device are electrically connected to the wiring layers **1511, 1522, 1523, 1514** and **1710** for the application of voltage to the buried wiring layers from outside.

[1478] In this example, the buried first, second and third wiring layers in a region of a lead-out portion may be arranged into steps as shown in **FIGS. 1517 to 1522** and first, second and third contact portions **1921, 1932, 1933, 1934** and **1910** are formed to reach the edges of the wiring layers, respectively, so that they do not contact other wiring layers than the intended one. Thereby, the first, second and third wiring layers may be lead out to the top face of the semiconductor memory.

[1479] Instead of forming the first, second and third contact portions **1921, 1932, 1933, 1934** and **1910**, the conductive films may be arranged such that they are lead out to the top face of the semiconductor memory to obtain the same effect as the above.

[1480] Alternatively, the buried first, second and third wiring layers in a region of a lead-out portion may be arranged as shown in **FIGS. 1523 to 1528** and first, second and third contact portions **1921, 1932, 1933, 1934** and **1910** are opened. Then, a silicon oxide film **1499**, for example, is deposited as a twenty-third insulating film to a thickness of 10 to 100 nm and etched back to a depth corresponding to the deposit thickness in the form of a sidewall spacer on the inner wall of each contact portion formed in the leading out portion. Thereafter, the first, second and third wiring layers may be lead out to the top face of the semiconductor memory by burying metal or a conductive film in the contact portions (**FIGS. 1523 to 1528**). At this time, the twenty-third insulating film may be made of not only a silicon oxide film but also a silicon nitride film as long as it is an insulating film.

[1481] For leading out the wiring layers, a common contact portion may be formed in the region of the lead-out portion of the memory cells continuous in a direction of A-A' as shown in **FIGS. 1526 to 1528**, or alternatively, the contact portions may be formed in the lead out portions of the memory cells, respectively as shown in **FIGS. 1517 to 1522**.

[1482] The lead-out of the first, second and third wiring layers to the top face of the semiconductor by the above-described process is applicable to all examples of the present invention.

[1483] Production Example 89

[1484] This example shows an example of production process for producing a semiconductor memory in which the transistor, the capacitor, the capacitor and the transistor are arranged in this order from the top of the island-like semiconductor layer **1110** to form a DRAM. **FIGS. 1529 and 1530** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 13** illustrating an EEPROM memory cell array.

[1485] In this example, production steps are according to those of Production example 71 except that the impurity diffusion layer **1710** is not formed and thus the step of

separating the impurity diffusion layer **1710** is not carried out. FIGS. **1529** and **1530** show a structure of the semiconductor memory of this example.

[**1486**] Thereby, a plurality of capacitors formed on the island-like semiconductor layers **1110** are separated by the transistors. Further, since the impurity diffusion layer **1710** is not used as a wiring layer, wiring capacitance is reduced.

[**1487**] The above-described examples in which the island-like semiconductor layers **1110** are formed in a pillar-form by selective epitaxial silicon growth after a plurality of charge storage layers are formed may be combined in any way.

[**1488**] Production Example 90

[**1489**] In a semiconductor memory to be produced in this example, a semiconductor substrate is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers are formed on the active regions. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors. The transistors are formed from the bottom to the top.

[**1490**] Such a semiconductor memory may be produced by the following process. FIGS. **1531** to **1540** and FIGS. **1541** to **1550** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating a memory cell array of an EEPROM.

[**1491**] First, a silicon nitride film **310**, for example, is deposited to a thickness of 200 to 2,000 nm as a first insulating film to be a mask layer on a surface of a P-type silicon substrate **100**. Using a resist film **R11** patterned by a known photolithographic technique as a mask (FIG. **1531** and FIG. **1541**), the silicon nitride film **310** is etched by reactive ion etching.

[**1492**] The P-type silicon substrate **100** is etched to a depth of about 2,000 to 20,000 nm by reactive ion etching using the silicon nitride film **310** as a mask to form a first trench **210** in a lattice form. Thereby the P-type silicon substrate **100** is separated into a plurality of island-like pillar-form semiconductor layers **110**.

[**1493**] The surface of the island-like semiconductor layer **110** is oxidized to form a second insulating film, for example, a thermally oxidized film **410**, to a thickness of 10 nm to 100 nm (FIGS. **1532** and **1542**). At this time, if the island-like semiconductor layer **110** has been formed in the minimum photoetching dimension, the dimension of the island-like semiconductor layer **110** is decreased by the formation of the thermally oxidized film **410**, that is, the island-like semiconductor layer **110** is formed to have a dimension not larger than the minimum photoetching dimension.

[**1494**] Next, the thermally oxidized film **410** is etched away from the periphery of each island-like semiconductor layer **110**, for example, by isotropic etching (FIGS. **1533** and **1543**). Then, as required, channel ion implantation is carried out into the sidewall of the island semiconductor layers **110** by slant ion implantation. For example, the ion implantation may be performed at an implantation energy of 5 to 100 keV at a boron dose of about 1×10^{11} to $1 \times 10^{13}/\text{cm}^2$ at an angle of 5 to 45° with respect to the normal line of the surface of the substrate. Preferably the channel ion implantation is performed from various directions to the island-like semiconductor layers **110** because a surface impurity concentration becomes more uniform. Alternatively, instead of the channel ion implantation, an oxide film containing boron may be deposited by CVD with a view to utilizing diffusion of boron from the oxide film. The impurity implantation from the surface of the island-like semiconductor layers **110** may be carried out before the island-like semiconductor layers **110** are covered with the thermally oxidized film **410**, or the impurity implantation may be finished before the island-like semiconductor layers **110** are formed. Means for the implantation are not particularly limited so long as an impurity concentration distribution is almost equal over the island-like semiconductor layers **110**.

[**1495**] Subsequently, a silicon oxide film **431**, for example, is deposited as a fifth insulating film in the lattice-form first trench **210** to a thickness of 50 to 500 nm by CVD and etched back to a desired depth so that the silicon oxide film **431** is buried in the first trench **210**. The deposition and the etch-back of the silicon oxide film **431** may be carried out without removing the thermally oxidized film **410** by etching.

[**1496**] Then, a silicon oxide film **481**, for example, is formed as a thirteenth insulating film to be a tunnel oxide film to a thickness of about 10 nm around each island-like semiconductor layer **110**, for example, by CVD. The tunnel oxide film, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[**1497**] Subsequently, a polysilicon film **511**, for example, is deposited as a first conductive film to a thickness of about 50 to 200 nm. The polysilicon film **511** is then etched by reactive ion etching, for example, to remain in the form of a sidewall spacer of a desired height (FIGS. **1534** and **1544**).

[**1498**] Then, a silicon oxide film **432**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD. The silicon oxide film **432** is then etched back by isotropic etching, for example, such that the polysilicon film **511** remaining in the form of the sidewall spacer is completely buried.

[**1499**] Thereafter, a silicon oxide film **422**, for example, is formed as a third insulating film to be a tunnel oxide film to a thickness of about 10 nm, for example, by thermal oxidation. The silicon oxide film **422**, similar to the silicon oxide film **481** (the thirteenth insulating film), may be formed of not only a thermally oxidized film but also a CVD oxide film or a nitrogen oxide film. The silicon oxide film **422** may not be formed of the same material as that of the silicon oxide film **481**. The silicon oxide films **422** and **481** may be formed to have an optionally determined thickness,

and the thickness of the silicon oxide film 422 may be smaller or larger than or equal to the thickness of the silicon oxide film 481.

[1500] Subsequently, a polysilicon film 512, for example, is deposited as a first conductive film to a thickness of about 50 to 200 nm. The polysilicon film 512 is then etched by reactive ion etching, for example, to remain in the form of a sidewall spacer of a desired height (FIGS. 1535 and 1545). By repeating likewise, a silicon oxide film 433 (a fifth insulating film) is embedded such that the polysilicon film 512 is buried, a silicon oxide film 423 is formed as a third insulating film to be a tunnel oxide film to a thickness of about 10 nm around each island-like semiconductor layer 110, and then a polysilicon film 513 is disposed as a first conductive film on the side of the silicon oxide film 423. In the same manner, a silicon oxide film 434 (a fifth insulating film) is embedded such that the polysilicon film 513 is buried, a silicon oxide film 484 is formed as a thirteenth insulating film to be a tunnel oxide film to a thickness of about 10 nm around each island-like semiconductor layer 110, and then a polysilicon film 514 is disposed as a first conductive film on the side of the silicon oxide film 484 (FIGS. 1536 and 1546).

[1501] Next, the silicon oxide films 434, 433, 432 and 431 (the fifth insulating films) are removed by isotropic etching, and then impurity introduction is carried out into the island-like semiconductor layers 110 and the semiconductor substrate 100 in self-alignment with the polysilicon films 511 to 514, which are separated first conductive films, and the silicon nitride film 310. For example, N-type impurity diffusion layers 710 to 724 are formed in an arsenic concentration of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$ by, for example, solid or vapor phase diffusion process. At this time, the impurity diffusion layer 710 to be a first wiring layer may be adjusted about its impurity concentration by ion implantation (FIG. 1537 and FIG. 1547). For example, the ion implantation may be performed at an implantation energy of 5 to 100 keV at a phosphorus dose of about 1×10^{13} to $1 \times 10^{15}/\text{cm}^2$ in a direction inclined by about 0 to 7°. Thereafter, thermal treatment is carried out to form the impurity diffusion layers 710 to 724, thereby bringing P-type regions of the island-like semiconductor layers 110 to an electrically floating state (FIGS. 1538 and 1548). Preferably the impurity concentration distribution in the impurity diffusion layer 710 to be a first wiring layer keeps a gentle gradient towards the P-type silicon substrate 110. The impurity introduction to the polysilicon films 511 to 514 may be performed during the formation of the polysilicon film 510 or during the impurity introduction into the island-like semiconductor layers 110. The timing of the impurity introduction is not particularly limited so long as these films become conductive films.

[1502] Then, a silicon oxide film 471, for example, is deposited as an eleventh insulating film to a thickness of 50 to 500 nm by CVD and embedded by anisotropic or isotropic etching to bury the side of the polysilicon film 511.

[1503] Then, a silicon nitride film 340, for example, is deposited as a twelfth insulating film to a thickness of 5 to 50 nm to form a sidewall spacer (FIGS. 1539 and 1549).

[1504] Subsequently, the silicon oxide film 471 is etched back to such a degree that the side of the polysilicon film 511

is exposed, and a polysilicon film 521, for example, is deposited as a second conductive film to a thickness of 15 to 150 nm.

[1505] Then, the polysilicon film 521 is etched back, and the silicon oxide film 471 and the P-type silicon substrate 100 are etched by anisotropic etching, for example, to form a second trench 220 in self-alignment with the polysilicon film 521, thereby separating the impurity diffusion layer 710. That is, a separation portion of the first wiring layer is formed in self-alignment with a separation portion of the second conductive film.

[1506] Subsequently, the polysilicon film 521 is etched back to such a degree that the polysilicon film 521 is able to contact the polysilicon film 511 to form a selection gate. At this time, by setting the intervals between the island-like semiconductor layers 110 in a direction of A-A' in FIG. 1 to a predetermined value or smaller, the polysilicon film 521 is formed into a second wiring layer to be a selection gate line continuous in the direction without need to use a masking process.

[1507] Thereafter, a silicon oxide film 462, for example, is deposited as an eighth insulating film to a thickness of 50 to 500 nm by CVD and anisotropically or isotropically etched so that the silicon oxide film 462 is embedded at least to bury the polysilicon film (the second conductive film) 521. Then the sidewall spacer of the silicon nitride film (the twelfth insulating film) 340 is removed by isotropic etching and an interlayer insulating film 612 is formed on exposed surfaces of the polysilicon films 512 to 514. This interlayer insulating film 612 may be formed of an ONO film, for example. The ONO film can be formed in the same manner as Production example 1.

[1508] Subsequently, in the same manner, a polysilicon film 522 is deposited as a second conductive film to a thickness of 15 to 150 nm and etched back so that the polysilicon film 522 is disposed on the side of the polysilicon film (the first conductive film) 512 with intervention of the interlayer insulating film 612. At this time, by setting the intervals between the island-like semiconductor layers 110 in the direction of A-A' in FIG. 1 to a predetermined value or smaller, the polysilicon film 522 is formed into a third wiring layer to be a control gate line continuous in the direction of A-A' without need to use a masking process.

[1509] Thereafter, a silicon oxide film 463, for example, is deposited as an eighth insulating film to a thickness of 50 to 500 nm by CVD and anisotropically or isotropically etched so that the silicon oxide film 463 is embedded at least to bury the polysilicon film (the second conductive film) 522. By repeating likewise, a polysilicon film (a second conductive film) 523 is disposed on the side of the polysilicon film (the first conductive film) 513 with intervention of an interlayer insulating film 613. With regard to the polysilicon film 514 which is the topmost first conductive film, a polysilicon film (a second conductive film) 524 is etched back to such a degree that the polysilicon film 524 is able to contact the polysilicon film (the first conductive film) 514, in the same manner as the polysilicon film 511 which is the bottommost first conductive film. A silicon oxide film 465, for example, is deposited as a tenth insulating film to a thickness of 100 to 500 nm on the top of the polysilicon film 524. The top portion of the island-like semiconductor layer 110 provided with the impurity diffusion layer 724 is exposed by etch-

back or by CMP. A fourth wiring layer is then formed so that its direction crosses the direction of the second or third wiring layer and is connected to the top portion of the island-like semiconductor layer **110**.

[1510] Thereafter, by known techniques, an interlayer insulating film is formed, and a contact hole and metal wiring are formed (FIGS. 1540 and 1550).

[1511] Thereby, a semiconductor memory is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film).

[1512] By bringing an active region of each memory cell into a floating state with respect to the semiconductor substrate, the back-bias effect from the substrate is eliminated and variations in threshold between the memory cells located at the top and the bottom of a set of memory cells connected in series are avoided at reading data.

[1513] In this example, the side of the island-like semiconductor layer **110**, which makes an active region, is oxidized and the oxide film **410** is removed to form the pillar-form island-like semiconductor layer **110** having a dimension smaller than the minimum photoetching dimension. This allows increase in the ratio of the capacity between the floating gates and the control gates to the capacity between the floating gates and the pillar-form semiconductor layers without increasing the area occupied by the memory cells. Thereby, data writing and erasing in and from the memory cells can be carried out without difficulty.

[1514] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1515] In this example, films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film **310** and the silicon nitride film **340** may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface.

[1516] The insulating films used in the present invention are not limited to an oxide film and a nitride film. Similar to the insulating film to be buried in the second trench **220**, the oxide film may be replaced with the nitride film and vice versa as long as it causes no inconvenience.

[1517] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. That is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1518] Production Example 91

[1519] In a semiconductor memory to be produced in this example, a semiconductor substrate is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers are formed on the active regions. The island-like semiconductor layers are each in an electrically floating

state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. The active regions of the memory cells are electrically common. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors. The transistors are formed from the bottom to the top.

[1520] Such a semiconductor memory may be produced by the following process. FIGS. 1551 to 1564 and FIGS. 1565 to 1578 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating a memory cell array of an EEPROM.

[1521] First, a silicon nitride film **310**, for example, is deposited to a thickness of 200 to 2,000 nm as a first insulating film to be a mask layer on a surface of a P-type silicon substrate **100**. Using a resist film **R11** patterned by a known photolithographic technique as a mask, the silicon nitride film **310** is etched by reactive ion etching. The P-type silicon substrate **100** is then etched to a depth of about 100 to 5,000 nm by reactive ion etching to form a first trench **210** in a lattice form in a direction of B-B' (FIGS. 1551 and 1565). At the etching of the P-type silicon substrate **100**, the resist film **R11** may be removed and the silicon nitride film **310** may be used as a mask.

[1522] Then, using a resist film **R12** patterned by a known photolithographic technique as a mask, the silicon nitride film **310** is etched by reactive ion etching to form a trench **211** in a lattice form in a direction of A-A' (FIGS. 1552 and 1566).

[1523] The P-type silicon substrate **100** is etched by reactive ion etching to a depth of about 2,000 to 20,000 nm to form a trench **212** in a lattice form (FIGS. 1553 and 1567). Thereby the P-type silicon substrate **100** is separated into a plurality of island-like pillar-form semiconductor layers **110**. At this time, the lattice-form trench **212** in the direction of B-B' is formed to have a larger depth than that of the trench **212** in the direction of A-A'.

[1524] Subsequently, in the same manner as Production example 90, channel ion implantation is carried out into the sidewall of the island semiconductor layers **110**. Means and timing for the implantation are not particularly limited as in the same manner as Production example 90.

[1525] The surface of the island-like semiconductor layer **110** is oxidized to form a second insulating film, for example, a thermally oxidized film **410**, to a thickness of 10 nm to 100 nm. If the island-like semiconductor layer **110** has been formed in the minimum photoetching dimension, the dimension of the island-like semiconductor layer **110** is decreased by the formation of the thermally oxidized film **410**, that is, the island-like semiconductor layer **110** is formed to have a dimension not larger than the minimum photoetching dimension. Thereafter, a silicon oxide film **431**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD in the lattice-form trench **212**. The silicon oxide film **431** is buried in the lattice-form trench **212** in the direction of B-B' to a depth equal to or

lower than the bottom of the lattice-form trench **212** in the direction of A-A', and then impurity introduction is carried out into the bottom of the separation portions between the island-like semiconductor layers **110** (FIGS. **1554** and **1568**). For example, ion implantation may be performed at an implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{13} to $1 \times 10^{16}/\text{cm}^2$ in a direction inclined by about 0 to 7°. Then, thermal treatment is carried out to diffuse impurities that have been introduced in advance to form an impurity diffusion layer **710**. The impurity diffusion layer **710** does not require any additional separation process and is ready to be formed as a first wiring layer.

[**1526**] Then, a silicon oxide film **481**, for example, is formed as a thirteenth insulating film to be a tunnel oxide film to a thickness of about 10 nm around each island-like semiconductor layer **110**, for example, by thermal oxidation (FIGS. **1555** and **1569**). The tunnel oxide film, however, may be formed of not only a thermally oxidized film but also a CVD oxide film or a nitrogen oxide film.

[**1527**] Subsequently, a polysilicon film **511**, for example, is deposited as a first conductive film to a thickness of about 50 to 200 nm. The polysilicon film **511** is then etched by reactive ion etching, for example, to remain in the form of a sidewall spacer of a desired height (FIGS. **1556** and **1570**). At this time, by setting the intervals between the island-like semiconductor layers **110** in a direction of A-A' in FIG. **1** to a predetermined value or smaller, the polysilicon film **511** is formed into a second wiring layer to be a selection gate line continuous in the direction without need to use a masking process.

[**1528**] Then, a silicon oxide film **451**, for example, is deposited as a seventh insulating film to a thickness of about 10 to 30 nm around each island-like semiconductor layer **110** and the polysilicon film **511**, for example, by thermal oxidation. Thereafter, a silicon oxide film **432**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD (FIGS. **1557** and **1571**) and embedded such that the polysilicon film **511** remaining in the form of the sidewall spacer is completely buried (FIGS. **1558** and **1572**). At this time, the thickness of the silicon oxide film **432** is set to be 20 to 30 nm or smaller on the top portion of the polysilicon film **511**.

[**1529**] Thereafter, a silicon oxide film **422**, for example, is formed as a third insulating film to be a tunnel oxide film to a thickness of about 10 nm, for example, by thermal oxidation. The silicon oxide film **422**, similar to the silicon oxide film **481** (the thirteenth insulating film), may be formed of not only a thermally oxidized film but also a CVD oxide film or a nitrogen oxide film. The silicon oxide film **422** may not be formed of the same material as that of the silicon oxide film **481**. The silicon oxide films **422** and **481** may be formed to have an optionally determined thickness, and the thickness of the silicon oxide film **422** may be smaller or larger than or equal to the thickness of the silicon oxide film **481**. The silicon oxide film **451** may not necessarily be formed. However, in that case, the thickness of the silicon oxide film (the third insulating film) **422** might possibly be uneven at a portion contacting the silicon nitride film (the fourth insulating film) **432**. Therefore it is preferred to form the silicon oxide film **451** in advance.

[**1530**] Subsequently, a polysilicon film **512**, for example, is deposited as a first conductive film to a thickness of about

50 to 200 nm. The polysilicon film **512** is then etched by reactive ion etching, for example, to remain in the form of a sidewall spacer of a desired height.

[**1531**] Then, an interlayer insulating film **612** is formed (FIGS. **1559** and **1573**). This interlayer insulating film **612** may be formed of an ONO film, for example. The ONO film may be formed in the same manner as described in Production example 1.

[**1532**] Subsequently, a polysilicon film **522**, for example, is deposited as a second conductive film to a thickness of 15 to 150 nm and etched back so that the polysilicon film **522** is disposed on the side of the polysilicon film (the first conductive film) **512** with intervention of the interlayer insulating film **612** (FIGS. **1560** and **1574**). At this time, by setting the intervals between the island-like semiconductor layers **110** in the direction of A-A' in FIG. **1** to a predetermined value or smaller, the polysilicon film **522** is formed into a third wiring layer to be a control gate line continuous in the direction of A-A' without need to use a masking process.

[**1533**] Then, a silicon oxide film **452**, for example, is deposited as a seventh insulating film to a thickness of about 10 to 30 nm around each island-like semiconductor layer **110** and the polysilicon film **522**, for example, by thermal oxidation. Thereafter, a silicon oxide film **433**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD (FIGS. **1561** and **1575**). By repeating likewise, a position within 20 to 30 nm or smaller above the third wiring layer, a silicon oxide film **423** is formed as a third insulating film to be a tunnel oxide film on the surface of the island-like semiconductor layer **110**. A polysilicon film **513** is disposed as a first conductive film on the side of the silicon oxide film **423** and a polysilicon film **523** is disposed as a second conductive film on the side of the polysilicon film **513** with intervention of an interlayer insulating film **613**.

[**1534**] Then, a silicon oxide film **453**, for example, is deposited as a seventh insulating film to a thickness of about 10 to 30 nm around each island-like semiconductor layer **110** and the polysilicon film **523**, for example, by thermal oxidation. Thereafter, a silicon oxide film **434**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD (FIGS. **1562** and **1576**) and etched back. At this time, the thickness of the silicon oxide film **434** is set to be 20 to 30 nm or smaller on the top portion of the polysilicon film **523**.

[**1535**] Thereafter, a silicon oxide film **484** is formed as a thirteenth insulating film to be a tunnel oxide film on the surface of the island-like semiconductor layer **110**. A polysilicon film **514** (a first conductive film) is formed on the side of the silicon oxide film **484**. On the polysilicon film **514**, a silicon oxide film **435**, for example, is deposited as a fifth insulating film to a thickness of 50 to 500 nm by CVD (FIGS. **1563** and **1577**). The top portion of the island-like semiconductor layer **110** is exposed by etch-back or CMP and impurities are introduced therein. Thermal treatment is carried out to form an impurity diffusion layer **724**. The impurity introduction may be realized by doping arsenic by ion implantation, or an oxide film containing arsenic may be deposited by CVD with a view to utilizing diffusion of arsenic from the oxide film.

[**1536**] Then, a fourth wiring layer is formed so that its direction crosses the direction of the second or third wiring

layer and is connected to the top portion of the island-like semiconductor layer **110** (FIGS. **1564** and **1578**).

[**1537**] Thereafter, by known techniques, an interlayer insulating film is formed, and a contact hole and metal wiring are formed.

[**1538**] The same effect as obtained by Production Example 90 can be obtained in this example. According to this example, the number of production steps is decreased, the necessary height of the island-like semiconductor layers can be reduced and variations in the production process can be reduced. Thereby, a semiconductor memory is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film).

[**1539**] By bringing an active region of each memory cell into a floating state with respect to the semiconductor substrate, the back-bias effect from the substrate is eliminated and variations in threshold between the memory cells located at the top and the bottom of a set of memory cells connected in series are avoided at reading data.

[**1540**] In this example, the side of the island-like semiconductor layer **110**, which makes an active region, is oxidized and the oxide film **410** is removed to form the pillar-form island-like semiconductor layer **110** having a dimension smaller than the minimum photoetching dimension. This allows increase in the ratio of the capacity between the floating gates and the control gates to the capacity between the floating gates and the pillar-form semiconductor layers without increasing the area occupied by the memory cells. Thereby, data writing and erasing in and from the memory cells can be carried out without difficulty.

[**1541**] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[**1542**] In this example, films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film **310** and the silicon nitride film **340** may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface.

[**1543**] The insulating films used in the present invention are not limited to an oxide film and a nitride film. Similar to the insulating film to be buried in the second trench **220**, the oxide film may be replaced with the nitride film and vice versa as long as it causes no inconvenience.

[**1544**] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[**1545**] The silicon oxide films **452** and **453** (the seventh insulating films) may not be formed for the same reason mentioned above with respect to the silicon oxide film **451**. However, it is preferred to form the silicon oxide films **452** and **453** with a view to improving uniformity in thickness of the silicon oxide films **423** and **484**.

[**1546**] In this example, memory cells or control gates are formed stage by stage, i.e., until a memory cell or a control gate at a certain stage is completed, a memory cell or a control gate at a stage thereabove is not formed. However, in the same manner as in Production example 90, the tunnel oxide films and the floating gates of every stage may be formed in advance and then a second wiring layer or an interlayer insulating film and a third wiring layer may be formed stage by stage. More particularly, this example is the same as Production example 90 except the step of forming the polysilicon films **511** to **514** (FIGS. **1534** to **1536** and **1544** to **1546**), in which the polysilicon films **511** to **514** are arranged such that intervals therebetween are set to 20 to 30 nm or smaller and the impurity diffusion layers **721**, **722**, **723** and **724** are not formed (FIGS. **1537** and **1547**).

[**1547**] The first wiring layer may also be formed in the same manner as in Production example 90, that is, a second trench **220** is formed in the P-type silicon substrate **110** in self-alignment with a polysilicon film **521** (FIG. **1550**) and then a separation portion of the first wiring layer is formed.

[**1548**] Production Example 92

[**1549**] In a semiconductor memory to be produced in this example, a semiconductor substrate to which an oxide film is inserted, for example, a semiconductor portion on an oxide film of an SOI substrate, is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers are formed on the active regions. The island-like semiconductor layers are each electrically common to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors. The transistors are formed from the bottom to the top.

[**1550**] Such a semiconductor memory may be produced by the following process. FIGS. **1579** to **1585** and FIGS. **1586** to **1592** are sectional views taken on line A-A' and line B-B', respectively, in FIG. **1** illustrating a memory cell array of an EEPROM.

[**1551**] First, a silicon nitride film **310**, for example, is deposited to a thickness of 200 to 2,000 nm as a first insulating film to be a mask layer on a surface of a SOI substrate **101** which is used as a substrate. Using a resist film **R11** patterned by a known photolithographic technique as a mask, the silicon nitride film **310** is etched by reactive ion etching. The SOI substrate **101** is then etched to a depth of about 10 to 5,000 nm by reactive ion etching to form a first trench **210** in a lattice form in a direction of B-B' (FIGS. **1579** and **1586**). At the etching of the SOI substrate **101**, the resist film **R11** may be removed and the silicon nitride film **310** may be used as a mask.

[**1552**] Then, using a resist film **R12** patterned by a known photolithographic technique as a mask, the silicon nitride film **310** is etched by reactive ion etching to form a trench **211** in a lattice form in a direction of A-A' (FIGS. **1580** and **1587**).

[1553] The SOI substrate **101** is etched by reactive ion etching to a depth of about 2,000 to 20,000 nm to form a trench **212** in a lattice form (FIGS. 1581 and 1588). Thereby the P-type silicon portion on the surface of the SOI substrate **101** is separated into a plurality of island-like pillar-form semiconductor layers **110**. At this time, an insulating layer portion of the SOI substrate **101** is exposed in a separation portion extending in the direction of B-B' between the island-like semiconductor layers **110** and the P-type silicon portion on the surface of the SOI substrate **101** is left in a separation portion extending in the direction of A-A' between the island-like semiconductor layers **110**.

[1554] Subsequently, in the same manner as Production example 90, channel ion implantation is carried out into the sidewall of the island semiconductor layers **110**. Means and timing for the implantation are not particularly limited as in the same manner as Production example 90.

[1555] The surface of the island-like semiconductor layer **110** is oxidized to form a second insulating film, for example, a thermally oxidized film **410**, to a thickness of 10 nm to 100 nm. If the island-like semiconductor layer **110** has been formed in the minimum photoetching dimension, the dimension of the island-like semiconductor layer **110** is decreased by the formation of the thermally oxidized film **410**, that is, the island-like semiconductor layer **110** is formed to have a dimension not larger than the minimum photoetching dimension. After the thermally oxidized film **410** is thus formed, impurity introduction is carried out through the thermally oxidized film **410** into the P-type silicon portion of the surface of the SOI substrate **101** remaining in the separation portion extending in the direction of A-A' between the island-like semiconductor layers **110** (FIGS. 1582 and 1589). For example, ion implantation may be performed at an implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{13} to $1 \times 10^{16}/\text{cm}^2$ in a direction inclined by about 0° to 7° . Then, thermal treatment is carried out to diffuse impurities that have been introduced in advance to form an impurity diffusion layer **710** (FIGS. 1583 and 1590). The impurity diffusion layer **710** does not require any additional separation process and is ready to be formed as a first wiring layer.

[1556] Subsequently, a silicon oxide film **431**, for example, is deposited as a fifth insulating film in the lattice-form trench **212** to a thickness of 50 to 500 nm by CVD and buried in the lattice-form trench **212** to a desired depth. Then, a silicon oxide film **481**, for example, is formed as a thirteenth insulating film to be a tunnel oxide film to a thickness of about 10 nm around each island-like semiconductor layer **110**, for example, by CVD (FIGS. 1584 and 1591). The tunnel oxide film, however, may be formed of not only a CVD oxide film but also a thermally oxidized film or a nitrogen oxide film.

[1557] Production steps thereafter follow Production example 91 (FIGS. 1556 to 1564 and 1570 to 1578).

[1558] According to this example, the same effect as obtained by Production Example 91 can be obtained, and furthermore, the junction capacitance of the impurity diffusion layer **710** which functions as the first wiring layer is suppressed or removed. Thereby, a semiconductor memory is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film).

[1559] By bringing an active region of each memory cell into a floating state with respect to the semiconductor substrate, the back-bias effect from the substrate is eliminated and variations in threshold between the memory cells located at the top and the bottom of a set of memory cells connected in series are avoided at reading data.

[1560] In this example, the side of the island-like semiconductor layer **110**, which makes an active region, is oxidized and the oxide film **410** is removed to form the pillar-form island-like semiconductor layer **110** having a dimension smaller than the minimum photoetching dimension. This allows increase in the ratio of the capacity between the floating gates and the control gates to the capacity between the floating gates and the pillar-form semiconductor layers without increasing the area occupied by the memory cells. Thereby, data writing and erasing in and from the memory cells can be carried out without difficulty.

[1561] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1562] In this example, films formed on the surface of the semiconductor substrate or the polysilicon film such as the silicon nitride film **310** and the silicon nitride film **340** may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface.

[1563] The insulating films used in the present invention are not limited to an oxide film and a nitride film. Similar to the insulating film to be buried in the second trench **220**, the oxide film may be replaced with the nitride film and vice versa as long as it causes no inconvenience.

[1564] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. That is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1565] Production Example 93

[1566] In a semiconductor memory to be produced in this example, gate oxide films **481** and **484** and tunnel oxide films **422** and **423** are formed by thermal oxidation of the island-like semiconductor layer **110** in the same manner as Production example 90. However, as shown in FIGS. 1594 and 1596, a diameter of the island-like semiconductor layer **110** decreases stage by stage from the bottom to the top.

[1567] For example, if the gate oxide film (the thirteenth insulating film) **481** is formed through thermal oxidation of the island-like semiconductor layer **110**, the side of the island-like semiconductor layer **110** is consumed to form the silicon oxide film **481**. Then, at the removal of the silicon oxide film (the fifth insulating film), the silicon oxide film **481** is removed together from a portion where the polysilicon film (the first conductive film) **511** is not formed to cover the silicon oxide film **481**. Thereby, as shown in FIGS. 1593 and 1595, the diameter of the island-like semiconductor layer **110** is reduced. A memory cell and a selection gate to be formed at an upper stage are formed on the island-like

semiconductor layer **110** whose diameter has been reduced. Therefore, in the memory cells and the selection gates at every stage, the diameter of the island-like semiconductor layer **110** decreases with height.

[1568] The shape of the island-like semiconductor layer **110** is not particularly limited as long as the memory cells are arranged in series in a direction perpendicular to the semiconductor substrate **100** as shown in **FIGS. 1594 and 1596**.

[1569] Production Example 94

[1570] In a semiconductor memory to be produced in this example, a semiconductor substrate is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and laminated insulating films as charge storage layers are formed on the active regions. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors. The transistors are formed from the bottom to the top.

[1571] Such a semiconductor memory may be produced by the following process. **FIGS. 1597 and 1598** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 11** illustrating a memory cell array of an EEPROM.

[1572] In this example, in contrast to Production example 90, interlayer insulating films **622** and **623** are formed instead of forming the silicon oxide films (the third insulating films) **422** and **423**, respectively. Further, instead of forming the polysilicon films (the second conductive films) **521** to **524**, the polysilicon films (the first conductive films) **511** to **514** are formed to be continuous in a direction of line A-A' in **FIG. 11** by controlling the deposit thickness and the etching amount, and the second trench **220** for separating the first wiring layer is formed by anisotropic etching in self-alignment with the polysilicon film **511** (**FIGS. 1597 and 1598**).

[1573] The impurity introduction to the polysilicon films **511** to **514** may be performed during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the impurity introduction is not particularly limited so long as these films become conductive films.

[1574] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. That is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1575] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1576] Production Example 95

[1577] In a semiconductor memory to be produced in this example, a semiconductor substrate is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. On the active regions, a plurality of gate oxide films are formed and gates to be MIS capacitors as charge storage layers and selection gates are formed. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. The transistors and the MIS capacitors are arranged alternately from the top of the island-like semiconductor layer. The thickness of gate insulating films of the transistors is equal to the thickness of gate insulating films of the MIS capacitors.

[1578] Such a semiconductor memory may be produced by the following process. **FIGS. 1599 to 1600** and **FIGS. 1601 to 1602** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 12** illustrating a memory cell array of a DRAM.

[1579] In this example, in contrast to Production example 90, the impurity diffusion layer **710** is not formed. Further, instead of forming the polysilicon films (the second conductive films) **521** to **524**, the polysilicon films (the first conductive films) **511** to **514** are formed to be continuous in a direction of line A-A' in **FIG. 12** and impurity diffusion layers **726** and **727** formed in the island-like semiconductor layer **110** are distributed as shown in **FIGS. 1599 and 1601**.

[1580] In contrast to the structure shown in **FIGS. 1599 and 1601**, in the case of arranging the transistor, the MIS capacitor, the MIS capacitor and the transistor in this order from the top of the island-like semiconductor layer **110**, the impurity diffusion layer **710** is formed. Further, a second trench **220** is formed in a direction of line B-B' in **FIG. 12** to separate the impurity diffusion layer, and the impurity diffusion layers **726** and **727** formed in the island-like semiconductor layer **110** are distributed as shown in **FIGS. 1600 and 1602**.

[1581] In this example, explanation is given of a semiconductor memory in which two memory cells, each comprising one transistor and one MIS capacitor, are arranged in the island-like semiconductor layer **110**. However, one memory cell, or three or more memory cells may be arranged in the island-like semiconductor layer **110**. The impurity introduction to the polysilicon films **511** to **514** may be performed during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the impurity introduction is not particularly limited so long as these films become conductive films.

[1582] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. That is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1583] Production Example 96

[1584] In a semiconductor memory to be produced in this example, a semiconductor substrate is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers are formed on the active regions. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is equal to the thickness of gate insulating films of the memory transistors. The transistors are formed from the bottom to the top.

[1585] Such a semiconductor memory may be produced by the following process. **FIGS. 1603 and 1604** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1586] In this example, in contrast to Production example 90, the silicon oxide films (the thirteenth insulating films) **481** and **484** are not formed. Instead of them, the silicon oxide films (the third insulating films) **421** and **424** are formed to have an equal thickness to that of the silicon oxide films (the third insulating films) **422** and **423** (**FIGS. 1603 and 1604**).

[1587] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. That is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1588] Production Example 97

[1589] In a semiconductor memory to be produced in this example, island-like semiconductor layers are formed on a semiconductor substrate to which an oxide film is inserted, for example, a semiconductor portion on an oxide film of an SOI substrate. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers are formed on the active regions. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors. The transistors are formed from the bottom to the top.

[1590] Such a semiconductor memory may be produced by the following process. **FIGS. 1605 and 1606** are sec-

tional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1591] In this example, in contrast to Production example 90, a semiconductor substrate to which an oxide film is inserted, e.g., a SOI substrate, is used instead of the semiconductor substrate **100** (**FIGS. 1605 and 1606**).

[1592] According to this example, the same effect as obtained by Production Example 90 can be obtained, and furthermore, the junction capacitance of the impurity diffusion layer **710** which functions as the first wiring layer is suppressed or removed.

[1593] The use of the SOI substrate as the substrate is applicable to all examples of the present invention.

[1594] Production Example 98

[1595] Explanation is given of a production process of a semiconductor memory in which the semiconductor substrate **100** is electrically insulated from the island-like semiconductor layers **110** not by the impurity diffusion layer but by a depletion layer existing at junction of the impurity diffusion layer with the semiconductor substrate **100** or the island-like semiconductor layer **110**. **FIG. 1607** and **FIG. 1608** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1596] In **FIG. 1607** and **FIG. 1608**, the island-like semiconductor layer **110** and the semiconductor substrate **100** are structurally connected. In this example, the island-like semiconductor layer **110** and the semiconductor substrate **100** are electrically insulated by a depletion layer formed on an island-like semiconductor layer **110** side or a semiconductor substrate **100** side of a PN junction between the impurity diffusion layer **710** as the first wiring layer and the island-like semiconductor layer **110** or the semiconductor substrate **100** owing to a potential difference between a potential given to the impurity diffusion layer **710** and a potential given to the island-like semiconductor layer **110** or the semiconductor substrate **100** at reading or at erasing.

[1597] More particularly, supposing that the depletion layer formed on the island-like semiconductor layer **110** side or the semiconductor substrate **100** side has a width **W**, the electrical insulation can be produced if at least either a space **Sa1** or **Sb1** of the impurity diffusion layer **710** shown in **FIG. 1607** and **FIG. 1608** is two or less times as large as **W**. Also, as regards the N-type impurity diffusion layers **721** to **723**, like the impurity diffusion layer **710**, the active region of each transistor is electrically insulated if at least either one of **Sa2** and **Sb2**, **Sa3** and **Sb3**, or **Sa4** and **Sb4** is two or less times as large as **W**.

[1598] The above described state may be produced both at reading and at erasing, only at erasing or only at reading. The above dimensional relationships may be combined in any way so long as the electrical insulation can be obtained.

[1599] This example may apply to any example of the semiconductor memory of the present invention.

[1600] Production Example 99

[1601] In a semiconductor memory to be produced in this example, a semiconductor substrate is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers are formed on the active regions. The island-

like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. A plurality of memory transistors, for example, two memory transistors, are placed and the transistors are connected in series along the island-like semiconductor layer. The transistors are formed from the bottom to the top.

[1602] Such a semiconductor memory may be produced by the following process. FIGS. 1609 and 1610 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating a memory cell array of an EEPROM.

[1603] In this example, production steps are the same as those of Production example 90 except that the polysilicon films 513 and 514 (the first conductive films), the silicon oxide film 423 (the third insulating film) and the silicon oxide film 484 (the thirteenth insulating film) are not formed, and that the polysilicon film 521 is disposed on the side of the polysilicon film 511 with intervention of the interlayer insulating film 612 after the separation of the impurity diffusion layer 710 and in the same manner, the polysilicon film 522 is disposed on the side of the polysilicon film 512 with intervention of the interlayer insulating film 613. Thereby, a semiconductor memory is realized which has two memory transistors in the island-like semiconductor layer and which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film) (FIGS. 1609 and 1610).

[1604] Production Example 100

[1605] In a semiconductor memory to be produced in this example, a semiconductor substrate is patterned in the form of pillars to form island-like semiconductor layers. Sides of the island-like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers are formed on the active regions. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors. Transmission gates are disposed between the transistors for transmitting potentials to the active regions of the memory cell transistors.

[1606] Such a semiconductor memory may be produced by the following process. FIGS. 1611 and 1612 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating a memory cell array of an EEPROM.

[1607] This example is the same as Production Example 90 except that the step of forming gate electrodes of a polysilicon film 530 (a third conductive film) is added after the polysilicon films (second conductive films) 521, 522, 523 and 524 are formed.

[1608] That is, after the formation of the polysilicon films 521, 522, 523 and 524, the silicon oxide films (the fifth insulating films) 424 to 422 and the interlayer insulating films 612 and 613 are removed by isotropic etching to such

an extent that the island-like semiconductor layer 110 is exposed between the polysilicon films 521 and 522. A silicon oxide film 400 is formed as a sixteenth insulating film by thermal oxidization on the surface of island-like semiconductor layer 110 between the selection gates and the memory cells and in exposed portions of polysilicon films 511, 512, 513, 514, 521, 522, 523 and 524. A polysilicon film 530 which is a third conductive film is deposited on the entire surface.

[1609] The polysilicon film 530 is anisotropically etched back to such an extent that a space between the polysilicon films 523 and 524 is not exposed.

[1610] Production steps thereafter follow Production Example 90 (FIGS. 1611 and 1612). Thereby the semiconductor memory is completed.

[1611] Production Example 101

[1612] Explanation is given of an example of production process for obtaining a structure in which the direction of the first wiring layer is parallel to the direction of the fourth wiring layer. FIGS. 1613 and 1614 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 illustrating a memory cell array of an EEPROM.

[1613] This example is the same as Production Example 90 except that, instead of forming the second trench 220 for separating the impurity diffusion layer 710 in self-alignment with the polysilicon film 511, the second trench 220 is formed in a direction of line A-A' in FIG. 1 by reactive ion etching using a resist film patterned by a known photolithographic technique such that the impurity diffusion layer 710 is separated. Thereby, a semiconductor memory is realized in which the first wiring layer is parallel to the fourth wiring layer and which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film) (FIGS. 1613 and 1614).

[1614] The impurity introduction to the polysilicon films 511 to 514 (the first conductive films) and the polysilicon films 521 to 524 (the second conductive films) may be performed during or after the formation of the polysilicon films or after the formation of the sidewall spacer. The timing of the impurity introduction is not particularly limited so long as these films become conductive films.

[1615] In this example, the control gates of the memory cells are formed continuously in one direction without using a mask. That is possible only where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1616] Further, by providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1617] Production Example 102

[1618] Explanation is given of an example of production process for obtaining a structure in which the first wiring layer is electrically common to the memory array. FIG. 1615

and **FIG. 1616** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1619] In this example, the second trench **220** is not formed in the semiconductor substrate **100**. This example is the same as Production Example 90 from which the steps regarding the formation of the second trench **220** is omitted.

[1620] Thereby, a semiconductor memory is realized in which at least the first wiring layer in the array is not divided but is common and which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film (the first conductive film) (**FIGS. 1615 and 1616**).

[1621] Production Example 103

[1622] This example shows an example of production process for producing a semiconductor memory in which the impurity diffusion layer **724** formed in the top of the island-like semiconductor layer **110** and connected to the fourth wiring layer **840** is distributed greater in a direction perpendicular to the semiconductor substrate while avoiding reduction in gate length of the selection gate transistor disposed on the top of the island-like semiconductor layer **110**. **FIG. 1617** and **FIG. 1618** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1623] In this example, in contrast to Production example 90, the impurity diffusion layer **724** which is connected to the fourth wiring layer **840** is formed to have a large height (**FIGS. 1617 and 1618**). At this time, the silicon oxide film (the tenth insulating film) **465** may be designed to have a large thickness and the insulating properties improve between the polysilicon film (the second conductive film) **524** and the fourth wiring layer **840**. Or, since an increased area of the impurity diffusion layer **724** can be exposed, contact resistance is reduced between the impurity diffusion layer **724** and the fourth wiring layer **840**.

[1624] Production Example 104

[1625] This example shows an example of production process for producing a semiconductor memory in which the transistor gates have different lengths in a vertical direction. **FIGS. 1619 and 1620** and **FIGS. 1621 and 1622** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1626] As shown in **FIGS. 1619 and 1621**, the polysilicon films (the first conductive films) **511** to **514** to be the memory cell gates or the selection gates may have different lengths in a direction vertical to the semiconductor substrate **100**.

[1627] Further, as shown in **FIGS. 1620 and 1622**, the memory cell gates of the polysilicon films **512** and **513** may have different lengths, and the polysilicon films **511** to **514** may have different vertical lengths.

[1628] Production Example 105

[1629] In a semiconductor memory to be produced in this example, island-like semiconductor layers are formed by patterning a semiconductor substrate. Sides of the island like semiconductor layers make active regions. A plurality of tunnel oxide films and floating gates as charge storage layers

are formed on the active regions. The island-like semiconductor layers are each in an electrically floating state with respect to the semiconductor substrate. The active region of each memory cell is in the electrically floating state. Selection gate transistors are disposed at the top and the bottom of the island-like semiconductor layer. A plurality of memory transistors, for example, two memory transistors, are placed between the selection gate transistors and are connected in series along the island-like semiconductor layer. The thickness of gate insulating films of the selection gate transistors is larger than the thickness of gate insulating films of the memory transistors. The island-like semiconductor layers are not cylindrical. The transistors are formed from the bottom to the top.

[1630] Such a semiconductor memory may be produced by the following process. **FIGS. 1623** to **1624** and **FIGS. 1625** to **1626** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1631] The island-like semiconductor layer **110** formed by reactive ion etching may have the top and the bottom having different outward shape as shown in **FIGS. 1623 and 1625**.

[1632] Also the top and the bottom of the island-like semiconductor layer **110** may be shifted in a horizontal direction as shown in **FIG. 1624** and **FIG. 1625**.

[1633] For example, in the case where the island-like semiconductor layer **110** is circular in plan view, the former island-like semiconductor layer **110** shows a truncated cone shape and the latter island-like semiconductor layer **110** shows an inclined column shape. The shape of the island-like semiconductor layer **110** is not particularly limited so long as the memory cells can be disposed in series in the direction vertical to the semiconductor substrate **100**.

[1634] Production Example 106

[1635] This example shows an example of production process for producing a semiconductor memory in which the island-like semiconductor layer **100** has an altered shape at its bottom. **FIGS. 1627** to **1630** and **FIGS. 1631** to **1634** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[1636] As shown in **FIGS. 1629 and 1633** and **FIGS. 1630 and 1634**, the first lattice-form trench **210** may have a linear slant shape at its bottom.

[1637] Alternatively, the first lattice-form trench **210** may have a rounded slant shape at its bottom as shown in **FIGS. 1627 and 1631** and **FIGS. 1628 and 1632**.

[1638] Here, the bottom of the polysilicon film (the first conductive film) **511** may or may not reach the slant bottom of the first trench **210**.

[1639] Production Example 107

[1640] This example shows an example of production process for producing a semiconductor memory in which the transistors are formed from the bottom to the top after the formation of the island-like semiconductor layers. Explanation is given of an example of production process for obtaining a structure in which the side and the top of the floating gate are covered with the control gate with intervention of an interlayer insulating film. **FIGS. 1635 and**

1636 are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating an EEPROM memory cell array.

[**1641**] In this example, in contrast to Production example 90, the polysilicon film **522** and **523** are deposited as second conductive films and then etched back to a depth of the top portion of the polysilicon films **512** and **513**, respectively, by isotropic etching (**FIGS. 1635 and 1636**).

[**1642**] Thereby, an area increases in which the polysilicon film **512** contacts the polysilicon film **522** with intervention of the interlayer insulating film **612**, and an area increases in which the polysilicon film **513** contacts the polysilicon film **523** with intervention of the interlayer insulating film **613**. Thereby, the memory cells improve the coupling ratio, respectively.

[**1643**] Production Example 108

[**1644**] This example shows an example of production process for producing a semiconductor memory in which the transistors are formed from the bottom to the top after the formation of the island-like semiconductor layers. Explanation is given of a production process for forming terminals which electrically connect first, second and third wiring layers to a peripheral circuit, respectively. **FIGS. 1637 to 1642** are sectional views taken on line H-H', line I1-I1', line I2-I2', line I3-I3', line I4-I4', and line I5-I5', respectively, of **FIG. 8** illustrating a memory cell array of EEPROM. These sectional views are taken at locations showing sites **921**, **932**, **933**, **934** and **910** where terminals mounted on the top face of the semiconductor device are electrically connected to the wiring layers **521**, **522**, **523**, **524** and **710** for the application of voltage to the buried wiring layers from outside.

[**1645**] The buried first, second and third wiring layers in a region of a lead-out portion are arranged into steps as shown in **FIGS. 1637 to 1642** and first, second and third contact portions **921**, **932**, **933**, **934** and **910** are opened to reach the edges of the wiring layers, respectively, so that they do not contact other wiring layers than the intended one. Then, a silicon oxide film **492**, for example, is deposited as a fifteenth insulating film to a thickness of 10 to 100 nm and etched back to a depth corresponding to the deposit thickness to form a sidewall spacer on the inner wall of each contact portion formed in the leading out portion. Thereafter, the first, second and third wiring layers may be lead out to the top face of the semiconductor memory by burying metal or a conductive film in the contact portions.

[**1646**] Instead of forming the first, second and third contact portions **921**, **932**, **933**, **934** and **910**, the conductive films may be arranged such that they are lead out to the top face of the semiconductor memory to obtain the same effect as the above.

[**1647**] Alternatively, the sidewall spacer of the silicon oxide film **492** may not be formed in the inner wall of each contact portion formed in the lead-out portion. In the case of forming the sidewall spacer of the silicon oxide film **492** (the fifteenth insulating film), the fifteenth insulating film may be formed of not only a silicon oxide film but also a silicon nitride film as long as it is an insulating film.

[**1648**] For leading out the wiring layers, a common contact portion may be formed in the region of the lead-out

portion of the memory cells continuous in a direction of A-A' as shown in **FIGS. 1637 to 1642**, or alternatively, the contact portions may be formed in the lead out portions of the memory cells, respectively.

[**1649**] The lead-out of the first, second and third wiring layers to the top face of the semiconductor by the above-described process is applicable to all examples of the present invention.

[**1650**] Production Example 109

[**1651**] This example shows an example of production process for producing a semiconductor memory in which the transistors are formed from the bottom to the top after the formation of the island-like semiconductor layers. Explanation is given of a production process in which the polysilicon film covering the island-like semiconductor layer **110** has an altered shape. **FIGS. 1643 and 1644** and **FIGS. 1645 and 1646** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[**1652**] As shown in **FIGS. 1643 and 1645** and **FIGS. 1644 and 1646**, the polysilicon film (the first conductive film) **510** covering the island-like semiconductor layer **110** may have a shape such that it is uniformly deposited along the bottom shape of the first trench **210**. Alternatively, the polysilicon film **510** may have a shape such that it is deposited partially ununiformly according to the bottom shape of the first trench **210**.

[**1653**] Production Example 110

[**1654**] This example shows an example of production process for producing a semiconductor memory in which the transistors are formed from the bottom to the top after the formation of the island-like semiconductor layer. Explanation is given of a production process in which the silicon nitride film **310** has an altered shape. **FIGS. 1647 and 1648** and **FIGS. 1649 and 1650** are sectional views taken on line A-A' and line B-B', respectively, in **FIG. 1** illustrating a memory cell array of an EEPROM.

[**1655**] According Production example 90 (**FIGS. 1531 and 1541**), the mask layer **310** is etched by reactive ion etching using a resist film **R1** patterned by a known photolithographic technique as a mask, and then the P-type semiconductor substrate **100** is etched to a depth of 2,000 to 20,000 nm by reactive ion etching by using the mask layer **310** as a mask to form a first trench **210**. At this time, the mask layer **310** may be smaller (**FIGS. 1647 and 1649**) or larger (**FIGS. 1648 and 1650**) than the outward shape of the island-like semiconductor layer **110**. The shape of the mask layer **310** is not particularly limited.

[**1656**] The above-described examples are formed may be combined in any way.

[**1657**] According to the present invention, it is possible to avoid the back-bias effect of the substrate in the direction vertical to the island semiconductor layer or prevent variations of the back-bias effect, and it is also possible to avoid increase of drive voltage. Thus a plurality of memory cells can be formed which are connected in series between bit lines and source lines. Thereby, it is possible to prevent variations in the characteristics of the memory cells which are caused by decline of the threshold in the memory cells at reading, the decline resulting from the back-bias effect from the substrate.

[1658] In the case where the island-like semiconductor layers are formed by epitaxial growth, it is possible to avoid damage caused by etching process since the island-like semiconductor layers can be formed without etching the semiconductor layer.

[1659] Further, in the case where semiconductor substrate pillars provided with memory transistors are formed in the minimum etching dimension and the smallest distance between the semiconductor substrate pillars is the minimum etching dimension, double the capacity of the prior-art memory device can be obtained if memory transistors in two tiers are formed per semiconductor substrate pillar. That is, the capacity of the device can be multiplied by the number of tiers of transistors per semiconductor substrate pillar. Generally, the larger the number of tiers, the more capacity can be obtained. Thereby, the cell area per bit decreases, the size of chips can be decreased and the production costs can be reduced.

[1660] Furthermore, since the vertical direction which determines the device performance does not depend upon the minimum etching dimension, the device performance can be maintained.

[1661] Further, since the memory cells are arranged to surround the respective island-like semiconductor layers, the drive current can be improved and the S value can be increased.

[1662] According to the production method for the semiconductor memory device of the present invention, the semiconductor substrate is patterned into the pillar form using a circular pattern, and then the side of the semiconductor substrate is sacrificially oxidized for eliminating damage, defects and unevenness on the surface of the substrate. Thus the surface of the substrate can be used as good active regions. The diameter of the pillar can be controlled by controlling the thickness of the oxide film formed by this sacrificial oxidization, and therefore, it is possible to easily increase the capacity between the floating gate and the control gate. This capacity depends upon the surface area of the tunnel oxide film and the surface area of the interlayer capacity film between the floating gate and the control gate.

[1663] Further, by using a circular pattern, it is possible to avoid local concentration of the electric field in the active region, and therefore, electric control can be easily done. The arrangement of the gate electrodes around the pillar-form semiconductor substrate improves the drive current and increase the S value. The formation of impurity diffusion layers such that the active regions of the memory cells are in the floating state with respect to the substrate eliminates the back-bias effect and variations in the characteristics of the memory cells caused by the decline of the threshold of the memory cells at reading.

[1664] By forming a plurality of sidewalls of an insulating film in the vertical direction on the sidewalls of floating gates after the tunnel oxide films and the floating gates are deposited, the floating gate can be patterned at the same time. That is, the tunnel oxide films of the same nature can be obtained with the respective memory cells. Or, by forming the tunnel oxide film after the floating gates and the control gates are formed, the tunnel oxide films of the same nature can be obtained with the respective memory cells.

The region where the floating gates and the control gates are formed is pre-defined by the thickness of the deposited films, and then, the floating gates or the control gates are formed. Therefore, it is possible to reduce patterning variations in the gate length of the memory cell transistors to process variations in the thickness of the deposited film. By using these techniques, the variations in the characteristics of the memory cells are suppressed and the variations in the device performance are suppressed. Thus the memory device can be more easily controlled and produced at low costs.

What is claimed is:

1. A semiconductor memory comprising:

a substrate; and

one or more memory cells constituted of at least one island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein at least one of said one or more memory cells is electrically insulated from the semiconductor substrate and has an insulating film allowing an electric charge to pass at least in a part of a region between the charge storage layer and the island-like semiconductor layer.

2. A semiconductor memory comprising:

a substrate; and

one or more memory cells constituted of at least one island-like semiconductor layer formed by epitaxial growth, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein at least one of said one or more memory cells is electrically insulated from the semiconductor substrate.

3. A semiconductor memory comprising:

a substrate; and

one or more memory cells constituted of at least one island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein at least one of said one or more memory cells is electrically insulated from the semiconductor substrate and a part of the charge storage layer and a part of the control gate electrode are formed of different materials.

4. A semiconductor memory according to claim 2, wherein the charge storage layer and the control gate electrode are arranged entirely or partially in alignment.

5. A semiconductor memory according to claim 1 or 2, wherein a part of the charge storage layer and a part of the control gate electrode are formed of different materials.

6. A semiconductor memory according to any one of claims 1 to 3, wherein said one or more memory cells are electrically insulated from the semiconductor substrate by an impurity diffusion layer of a conductivity type opposite to the conductivity type of the semiconductor substrate, the impurity diffusion layer being formed in the semiconductor substrate or in the island-like semiconductor, or by a first

impurity diffusion layer of a conductivity type opposite to the conductivity type of the semiconductor substrate, the first impurity diffusion layer being formed in the island-like semiconductor, and a second impurity diffusion layer of the same conductivity type as that of the semiconductor substrate, the second impurity diffusion layer being formed in the first diffusion layer.

7. A semiconductor memory according to any one of claims 1 to 3, wherein at least one of the memory cells is electrically insulated from the semiconductor substrate by a depletion layer formed at a junction between an impurity diffusion layer and the semiconductor or the island-like semiconductor.

8. A semiconductor memory according to claim 6 or 7, wherein a plurality of memory cells are formed and at least one of the memory cells is electrically insulated from another memory cell by an impurity diffusion layer of a conductivity type opposite to the conductivity type of the semiconductor substrate, the impurity diffusion layer being formed in the island-like semiconductor layer, or by a first impurity diffusion layer of a conductivity type opposite to the conductivity type of the semiconductor substrate, the first impurity diffusion layer being formed in the island-like semiconductor, and a second impurity diffusion layer of the same conductivity type as that of the semiconductor substrate, the second impurity diffusion layer being formed in the first diffusion layer.

9. A semiconductor memory according to claim 6 or 7, wherein a plurality of memory cells are formed and at least one of the memory cells is electrically insulated from another memory cell by an impurity diffusion layer of a conductivity type opposite to the conductivity type of the semiconductor substrate, the impurity diffusion layer being formed in the island-like semiconductor and a depletion layer formed at a junction between the impurity diffusion layer and the semiconductor substrate or the island-like semiconductor layer.

10. A semiconductor memory according to claim 1, wherein the insulating film is formed as a tunnel insulating film immediately under the charge storage layer.

11. A semiconductor memory according to any one of claims 1 to 3, wherein an impurity diffusion layer is formed on the semiconductor substrate, the impurity diffusion layer functions as common wiring for at least one memory cell.

12. A semiconductor memory according to any one of claims 1 to 3, wherein a plurality of memory cells are formed with regard to one island-like semiconductor layer and the memory cells are arranged in series.

13. A semiconductor memory according to any one of claims 1 to 3,

wherein a plurality of island-like semiconductor layers are formed in matrix,

wiring layers for reading a state of a charge stored in the memory cells are formed in the island-like semiconductor layers,

a plurality of control gates are arranged continuously in a direction to form a control gate line, and

a plurality of the wiring layers are connected in a direction crossing the control gate line to form a bit line.

14. A semiconductor memory according to any one of claims 1 to 3, wherein a gate electrode for selecting a memory cell is formed at least at an end of the memory cell

formed on the island-like semiconductor layer so as to partially or entirely encircle the sidewall of the island-like semiconductor layer and the gate electrode is arranged in series with the memory cell.

15. A semiconductor memory according to claim 14, wherein a part of the island-like semiconductor layer opposed to the gate electrode is electrically insulated from the semiconductor substrate or the memory cell by an impurity diffusion layer of a conductivity type opposite to the conductivity type of the semiconductor substrate, the impurity diffusion layer being formed in the semiconductor substrate or in the island-like semiconductor layer.

16. A semiconductor memory according to any one of claims 1 to 3, wherein the control gates of the memory cells are arranged adjacently so that channel layers of the memory cells are electrically connected.

17. A semiconductor memory according to claim 14, wherein the control gate and the gate electrode are adjacently arranged so that a channel layer formed in a part of the island-like semiconductor layer opposed to the gate electrode and the channel layer of the memory cell are electrically connected.

18. A semiconductor memory according to any one of claims 1 to 3, further comprising electrodes for electrically connecting channel layers of the memory cells between the control gates.

19. A semiconductor memory according to claim 14, further comprising an electrode for electrically connecting a channel layer formed in a part of the island-like semiconductor layer opposed to the gate electrode with a channel layer of the memory cell, between the control gate and the gate electrode.

20. A semiconductor memory according to claim 14, wherein all, some or one control gate(s) are formed of the same material as all, some or one gate electrode(s).

21. A semiconductor memory according to claim 14, wherein the charge storage layer and the gate electrode are formed of the same material.

22. A semiconductor memory according to any one of claims 1 to 3, wherein a plurality of island-like semiconductor layers are formed in matrix, and the width of the island-like semiconductor layers in one direction is smaller than a distance between adjacent island-like semiconductor layers in the same direction.

23. A semiconductor memory according to any one of claims 1 to 3, wherein a plurality of island-like semiconductor layers are formed in matrix, and a distance between the island-like semiconductor layers in one direction is smaller than a distance between the island-like semiconductor layers in another direction.

24. A semiconductor memory according to claim 14,

wherein (i) a lower gate electrode and the control gate,

(ii) the lower gate electrode, the control gate and an upper gate electrode or

(iii) the control gate and the upper gate electrode are arranged in an upward order in a direction vertical to the semiconductor substrate, and

(i) a lower gate electrode and the control gate,

(ii) the lower gate electrode, the control gate and an upper gate electrode or

(iii) the control gate and the upper gate electrode are sequentially led out onto a surface of the semiconductor memory at an end of a memory cell array in which island-like semiconductor layers with the memory cells formed thereon are arranged in matrix.

25. A semiconductor memory according to any one of claims 1 to 3,

wherein said at least one island-like semiconductor layer has at least two plane orientations.

26. A process for producing a semiconductor memory a substrate; and

one or more memory cells constituted of at least one island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer,

wherein at least one of said one or more memory cells is electrically insulated from the semiconductor substrate and has an insulating film allowing an electric charge to pass at least in a part of a region between the charge storage layer and the island-like semiconductor layer, the process comprising at least the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;

forming, on the island-like semiconductor layer, an insulating film which covers at least a part of a surface of the island-like semiconductor layer and a first conductive layer which covers a surface of the insulating film;

forming a sidewall spacer of an insulating film on the first conductive layer located on a sidewall of the island-like semiconductor layer, the sidewall spacer being divided in a height direction;

dividing the first conductive film using the sidewall spacer as a mask;

introducing an impurity in self-alignment with the divided first conductive film; and

forming an interlayer capacity film and a second conductive film on the first conductive film.

27. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer formed by epitaxial growth, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

forming one or more laminate films each composed of three or more different films including a first insulating film, on a semiconductor substrate;

forming a hole in the laminate film, the hole reaching the semiconductor substrate;

epitaxially growing a semiconductor in the hole to form an island-like semiconductor layer on the semiconductor substrate;

dividing the first insulating film so that the first insulating film is located only around the island-like semiconductor layer and covering the divided first insulating film with another insulating film;

partially exposing a surface of the island-like semiconductor layer so that the first insulating film and said another insulating film remain;

forming a first conductive film with intervention of the insulating films on an exposed of the island-like semiconductor layer;

forming a second conductive film on the first conductive film with intervention of an interlayer insulating film; and

introducing an impurity into the island-like semiconductor layer.

28. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer formed by epitaxial growth, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

forming one or more laminate films each composed of three or more different films including a first insulating film, on a semiconductor substrate;

forming a hole in the laminate film, the hole reaching the semiconductor substrate;

epitaxially growing a semiconductor in the hole to form an island-like semiconductor layer on the semiconductor substrate;

dividing the first insulating film so that the first insulating film is located only around the island-like semiconductor layer and covering the divided first insulating film with another insulating film;

partially exposing a surface of the island-like semiconductor layer so that the first insulating film and said another insulating film remain; and

forming a first conductive film on an exposed sidewall of the island-like semiconductor layer with intervention of a charge storage layer of an laminate insulating film; and

introducing an impurity into the island-like semiconductor layer.

29. A process for producing a semiconductor memory according to claim 27 or 28, wherein the impurity is introduced into the island-like semiconductor layer by putting the impurity into the first insulating film simultaneously when or after the first insulating film is formed and diffusing the impurity from the first insulating film.

30. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or

more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

- forming a laminate film made of first insulating films and first conductive films which are alternately laminated, on a semiconductor substrate;
- patterning the laminate film to form island-like laminate films separated from each other;
- forming a second conductive film in the form of a sidewall on sidewalls of the first conductive films in the island-like laminate films with intervention of an interlayer capacity film;
- patterning the island-like laminate films to expose a part of a surface of the semiconductor substrate and sidewalls of the first conductive films;
- forming a tunnel insulating film on the exposed sidewalls of the first conductive film;
- forming an island-like semiconductor layer by epitaxial growth so that the island-like semiconductor layer contacts the tunnel insulating film; and
- introducing an impurity into a region of the island-like semiconductor layer opposed to the first conductive film.

31. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

- forming a laminate film made of first insulating films and first conductive films which are alternately laminated, on a semiconductor substrate;
- patterning the laminate film to form island-like laminate films separated from each other;
- patterning the island-like laminate films to expose a part of a surface of the semiconductor substrate and sidewalls of the first conductive films;
- forming a charge storage layer of a laminate insulating film on the exposed sidewalls of the first conductive films;
- forming an island-like semiconductor layer by epitaxial growth so that the island-like semiconductor layer contacts the charge storage layer; and
- introducing an impurity into a region of the island-like semiconductor layer opposed to the first conductive film.

32. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

- forming a laminate film made of first insulating films and first conductive films which are alternately laminated, on a semiconductor substrate;
- patterning the laminate film to form island-like laminate films separated from each other;
- patterning the island-like laminate films to expose a part of a surface of the semiconductor substrate and sidewalls of the first conductive films;
- forming a gate insulating film on the exposed sidewalls of the first conductive films;
- forming an island-like semiconductor layer by epitaxial growth so that the island-like semiconductor layer contacts the gate insulating film; and
- introducing an impurity into a region of the island-like semiconductor layer opposed to the first conductive film.

33. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

- forming a first insulating film on a semiconductor substrate;
- patterning the first insulating film to form island-like insulating films separated from each other;
- forming a charge storage layer of a first conductive film in the form of sidewalls on sidewalls of the island-like insulating films;
- forming a control gate of a second conductive film in the form of a sidewall on a sidewall of the charge storage layer with intervention of an interlayer capacity film;
- patterning the island-like insulating films to expose a part of a surface of the semiconductor substrate and a sidewall of the first conductive film;
- forming a tunnel insulating film on the exposed sidewall of the first conductive film;
- forming an island-like semiconductor layer by epitaxial growth so that the semiconductor layer contacts the tunnel insulating film; and
- introducing an impurity into a region of the island-like semiconductor layer opposed to the first conductive film.

34. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

- forming a first insulating film on a semiconductor substrate;

patterning the first insulating film to form island-like insulating films separated from each other;

forming a control gate of a first conductive film in the form of a sidewall on sidewalls of the island-like insulating films;

patterning the island-like insulating films to expose a part of a surface of the semiconductor substrate and a sidewall of the first conductive film;

forming a charge storage layer of a laminate insulating film on the exposed sidewall of the first conductive film;

forming an island-like semiconductor layer by epitaxial growth so that the semiconductor layer contacts the charge storage layer; and

introducing an impurity into a region of the island-like semiconductor layer opposed to the first conductive film.

35. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

forming a first insulating film on a semiconductor substrate;

patterning the first insulating film to form island-like insulating films separated from each other;

forming a control gate and a capacitor electrode of first conductive films in the form of sidewalls on sidewalls of the island-like insulating films;

patterning the island-like insulating films to expose a part of a surface of the semiconductor substrate and sidewalls of the first conductive films;

forming a gate insulating film on the exposed sidewalls of the first conductive films;

forming an island-like semiconductor layer by epitaxial growth so that the semiconductor layer contacts the gate insulating film; and

introducing an impurity into a region of the island-like semiconductor layer opposed to the first conductive film.

36. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;

forming a tunnel insulating film on a surface of the island-like semiconductor layer;

forming sidewall spacers of first conductive films on the tunnel insulating film, the first conductive films being separated from each other in a height direction;

forming an impurity diffusion layer by introducing an impurity in self-alignment with the separated first conductive films; and

forming interlayer capacity film and a second conductive film on the first conductive films;

37. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;

forming a tunnel insulating film on a surface of the island-like semiconductor layer;

forming a charge storage layer of a laminate insulating film on the tunnel insulating film;

forming sidewall spacers of first conductive films on the charge storage layer, the first conductive films being separated from each other in a height direction; and

forming an impurity diffusion layer by introducing an impurity in self-alignment with the separated first conductive films.

38. A process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

forming at least one island-like semiconductor layer on a semiconductor substrate;

forming an impurity diffusion layer by introducing an impurity in a part of a surface of the island-like semiconductor layer; and

forming sidewall spacers of first conductive films on the surface of the island-like semiconductor layer with intervention of an insulating film, the first conductive films being separated from each other in a height direction.

39. A process according to any one of claims 26 to 28 and **30 to 38**, wherein the introduced impurity is so diffused that a continuous impurity diffusion layer is formed in the island-like semiconductor layer in a direction horizontal to the surface of the semiconductor substrate.

40. A process according to any one of claims 26 to 28 and **30 to 38**, wherein a plurality of island-like semiconductor layers are formed in matrix, sidewalls of the island-like

semiconductor layers are oxidized to form oxide films, and the oxide films are removed so that the width of the island-like semiconductor layers in one direction is smaller than a distance between the island-like semiconductor layers in the same direction.

41. A process according to claim 26 wherein a third conductive film is formed between separated first conductive films.

42. A process according to any one of claims 26 to 28 and **30** to **38**, wherein the first conductive film is separated into two or more separated first conductive films which are located so closely that a channel layer formed beneath a separated first conductive film along the island-like semiconductor layer is electrically connected to an adjacent channel layer.

43. A process according to any one of claims 26 to 28 and **30** to **38**, wherein a lower gate electrode, the control gate and/or an upper gate electrode are arranged in an upward order in a direction vertical to the semiconductor substrate, and

the upper gate electrode, the control gate and/or the lower gate electrode are sequentially led out to a surface of the semiconductor memory at an end of a memory cell

array in which island-like semiconductor layers with the memory cells formed thereon are arranged in matrix.

44. A process according to claim 27, wherein an insulating film is formed in a part of a surface of the island-like semiconductor layer, another insulating film is formed in another part of the surface of the island-like semiconductor layer, and the first conductive film is formed on the insulating film and on said another insulating film.

45. A process according to claims **28**, wherein the charge storage layer is formed of the laminate insulating film in a part of a surface of the island-like semiconductor layer, another insulating film is formed in another part of the surface of the island-like semiconductor layer, and the first conductive film is formed on the charge storage layer and on said another insulating film.

46. A process according to claim 32, wherein at least two first conductive films are formed, an impurity is introduced into a region of the island-like semiconductor layer opposed to the first conductive film so that one of the first conductive films functions as a control gate electrode and another of the first conductive films functions as a capacitor electrode.

* * * * *