

Multiple SOI layers by multiple Smart-Cut[®] transfers

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Silicon On Insulator (SOI) technologies are now entering into mainstream applications, with recent announcements regarding for instance microprocessors applications [1]. One condition for this to happen has been to prove that SOI material manufacturing processes exist that are compatible with such industrial developments (availability, cost, quality, ..). Among those processes, the Smart-cut[®] process is one based on layer transfer from one substrate to another [2]. Stacking monocrystalline silicon onto another silicon substrate with a silica layer in between is then possible and indeed is being used on an industrial scale to manufacture SOI wafers. Beyond simple SOI wafers that can also be high value added substrates for other applications such as photonics [3], sensors and other micromachining purposes, we will show and demonstrate in this paper how the Smart cut process can be seen as a basic step and how this process can be used to realize multiple SOI wafers, allowing different crystalline and/or amorphous layers to be stacked.

The Smart-Cut SOI process involves two basic technologies such as hydrogen implantation and wafer bonding. In this process, the Hydrogen implantation energy defines how deep the fragilized buried layer will be and thus the layer thickness transferred in the process (figure 1). As the buried insulator may simply be thermally grown in the case of silica, or even be deposited on the surface of at least one of the two surfaces to be contacted during wafer bonding, its thickness is very flexible and its nature can be changed (SiO_2 , Si_3N_4 , combinations, ...). Realizing multiple SOI layers based on a layer transfer process can be achieved in many different ways: repeating a single layer transfer several times onto a SOI wafer initially obtained, transferring onto a single substrate or a SOI wafer whole SOI layers stacks already formed, ... In any case, at least one SOI wafer has to be used again in a wafer bonding step. Wafer bonding, without any glue but based on molecular or hydrogen bonds as it is meant generally, requires pretty good substrate surface quality, especially in terms of roughness and surface defect density. Figure one shows surface roughness on a standard SOI wafer achieved with Smart-Cut (called UNIBOND[®] wafer), exhibiting same surface roughness than standard silicon substrates. Since flatness and surface defects density are also in silicon properties range, wafer bonding can be applied similarly between two SOI wafers. Then, multiple SOI layers stacks can be easily performed when using SOI wafers as top and base in Smart-Cut technology.

Figure 2 describes one process that has been chosen for a demonstration purpose. 3 hydrogen induced splitting steps have been used in this case to obtain on the whole surface of 6 inches substrates 4 buried oxide layers. The first step is simply the standard SOI Smart-Cut process adapted to obtain a 2400 Å silicon onto 2600 Å oxide structure. This SOI wafer is then used again as the wafer that will be sliced: after the formation of a new 2600 Å thick surface oxide, a second hydrogen implantation through the two oxide layers is performed. After bonding to a bare silicon base wafer, splitting and final polishing, wafer B, equivalent to a double SOI structure, is obtained. Same kind of process is then repeated but this time using SOI both for the wafer to be sliced (SOI A') and for the new handle substrate (SOI B). That way, a four SOI stack is obtained. Such process is only possible since Smart-Cut does not introduce any particular stress to the wafers. Moreover, unbonded area on the edge of the final wafer does not exceed 3 mm, enhancing UNIBOND SOI layer edge integrity. Figure 3 shows a SEM view of the final structure with sharp interfaces and perfect intra-layer insulation.

Applications for those kinds of structures can be imagined in multiple fields from 3D process integration to optical filters, micromachining, sensors, ... Intermediate additional implantation or diffusion steps can be introduced in order to adjust doping and then optical properties of the different layers. P doping of one layer has already been demonstrated without any negative impact of the whole process. This result can also be achieved by using starting silicon wafers with the right doping (as grown for instance) before using it in the for the Smart-Cut process.

As a conclusion, through this example, it has been demonstrated how powerful and flexible the Smart-Cut can be to realize complex structures. As soon as single step Smart-Cutting is demonstrated for one material, it can be integrated in the layer stack. Smart-Cut process is compatible with many materials: AsGa, SiC and InP [4] for instance have been shown as several examples of materials that can be sliced, the use of many different base wafers such as quartz, glass or even SiC bare wafer, but also various intermediate layers introduced before the bonding (buried oxides, Nitrides, ...). have been demonstrated [5].

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- [1] "IBM to release 64-bit PowerPC processor with SOI", Electronic Buyers' news, 02/19/99
- [2] M. Bruel, Nuclear instruments and methods, Phys. Res. B, 108 (1996) 313-319.
- [3] T.W. Ang et al., 9th Int. Symposium on Silicon-on-Insulator Technology and Devices, Seattle, Abs N°434.
- [4] E. Jalaguier et al., JNMO'99, (7th Int. Nat. Journ. In Micro and Optoelectronics); Egat (France), Jan. 99
- [5] B. Aspar et al., Electron. Lett., 35, (12), (1999).

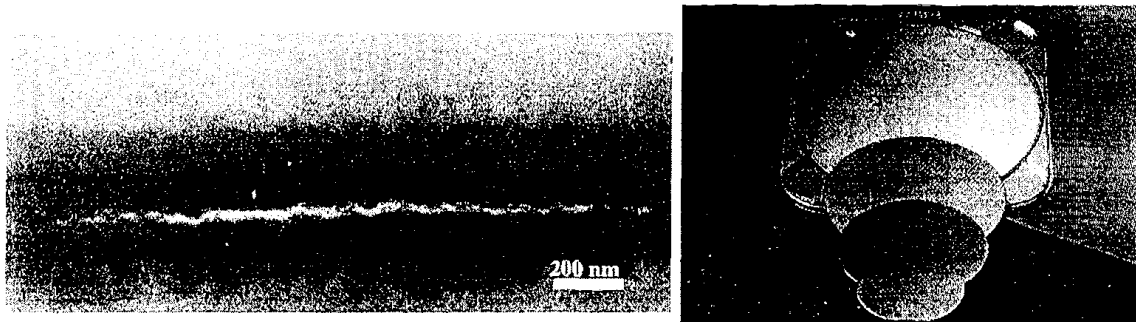


Figure 1: TEM cross section view of an hydrogen induced crack propagation in silicon, in case of an hydrogen implanted wafer bonded to a silicon bare wafer and annealed to 500°C. Right figure shows 4, 6, 8 and 12" UNIBOND wafers realized using the Smart-Cut process.

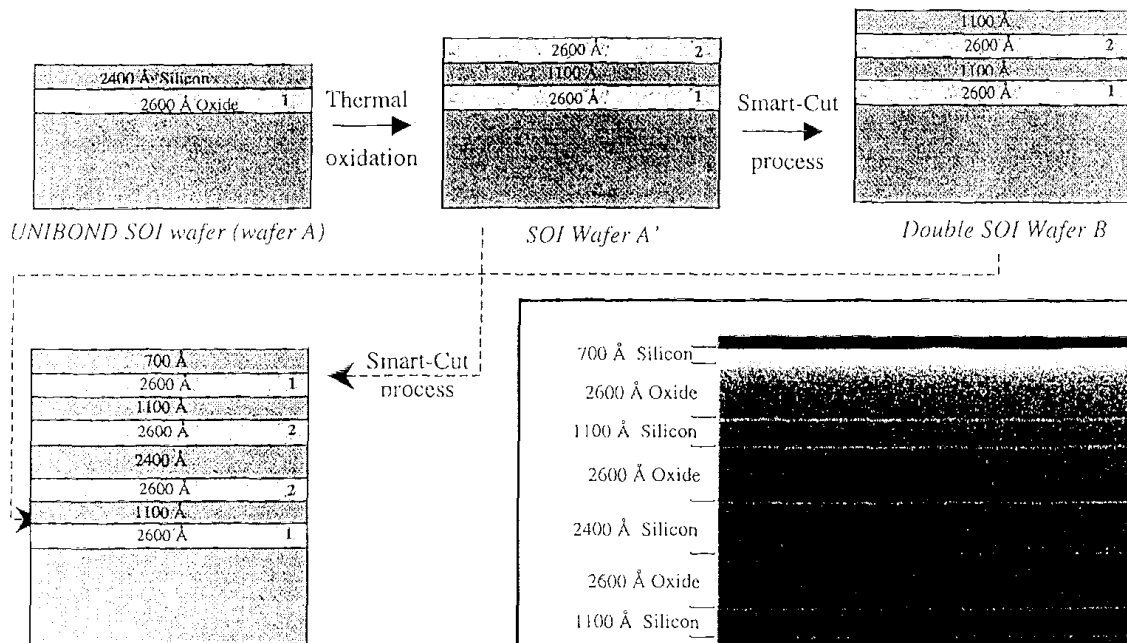


Figure 2 : Multiple Smart-Cut processes for multiple SOI stack structure realization.

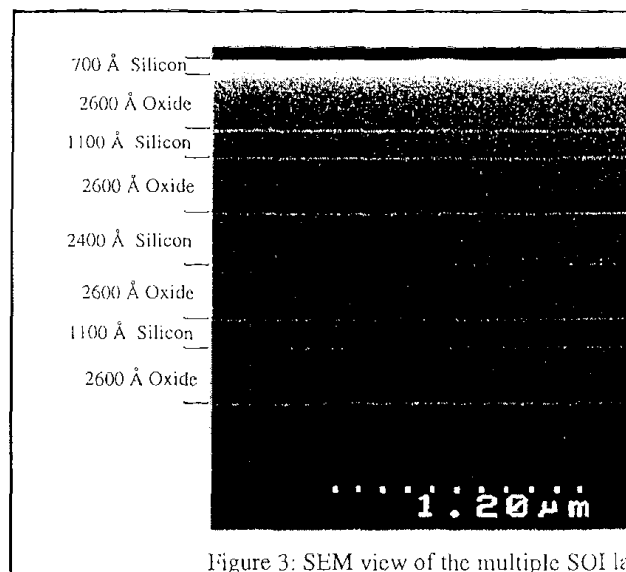


Figure 3: SEM view of the multiple SOI layers