



(19) **United States**

(12) **Patent Application Publication**

Endoh et al.

(10) **Pub. No.: US 2002/0154556 A1**

(43) **Pub. Date: Oct. 24, 2002**

(54) **SEMICONDUCTOR MEMORY AND ITS PRODUCTION PROCESS**

Jun. 23, 2001 (JP) 2001-266490
Jun. 23, 2001 (JP) 2001-264928
Jun. 23, 2001 (JP) 2001-266491

(76) Inventors: **Tetsuo Endoh**, Natori-shi (JP); **Fujio Masuoka**, Sendai-shi (JP); **Takuji Tanigami**, Fukuyama-shi (JP); **Takashi Yokoyama**, Sendai-shi (JP); **Noboru Takeuchi**, Sendai-shi (JP)

Publication Classification

(51) **Int. Cl.⁷** **G11C 29/00**
(52) **U.S. Cl.** **365/200**

Correspondence Address:
NIXON & VANDERHYE P.C.
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714 (US)

(21) Appl. No.: **10/107,380**

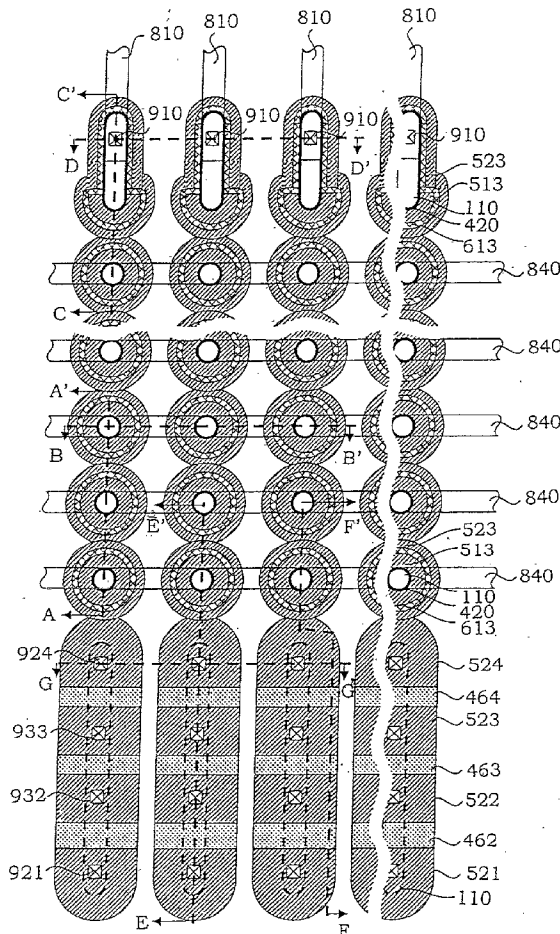
(22) Filed: **Mar. 28, 2002**

(30) **Foreign Application Priority Data**

Mar. 30, 2001 (JP) 2001-142454
Jun. 23, 2001 (JP) 2001-264927

(57) **ABSTRACT**

A semiconductor memory comprises: a substrate; and one or more memory cells constituted of at least one island-like semiconductor layer, a charge storage layer and a control gate, the charge storage layer and the control gate being formed to entirely or partially encircle a sidewall of the island-like semiconductor layer, wherein at least one of said one or more memory cells is electrically insulated from the semiconductor substrate and has an insulating film allowing an electric charge to pass at least in a part of a region between the charge storage layer and the island-like semiconductor layer.



Intel v. BeSang
IPR2023-00991
Exhibit 1031

Fig. 1

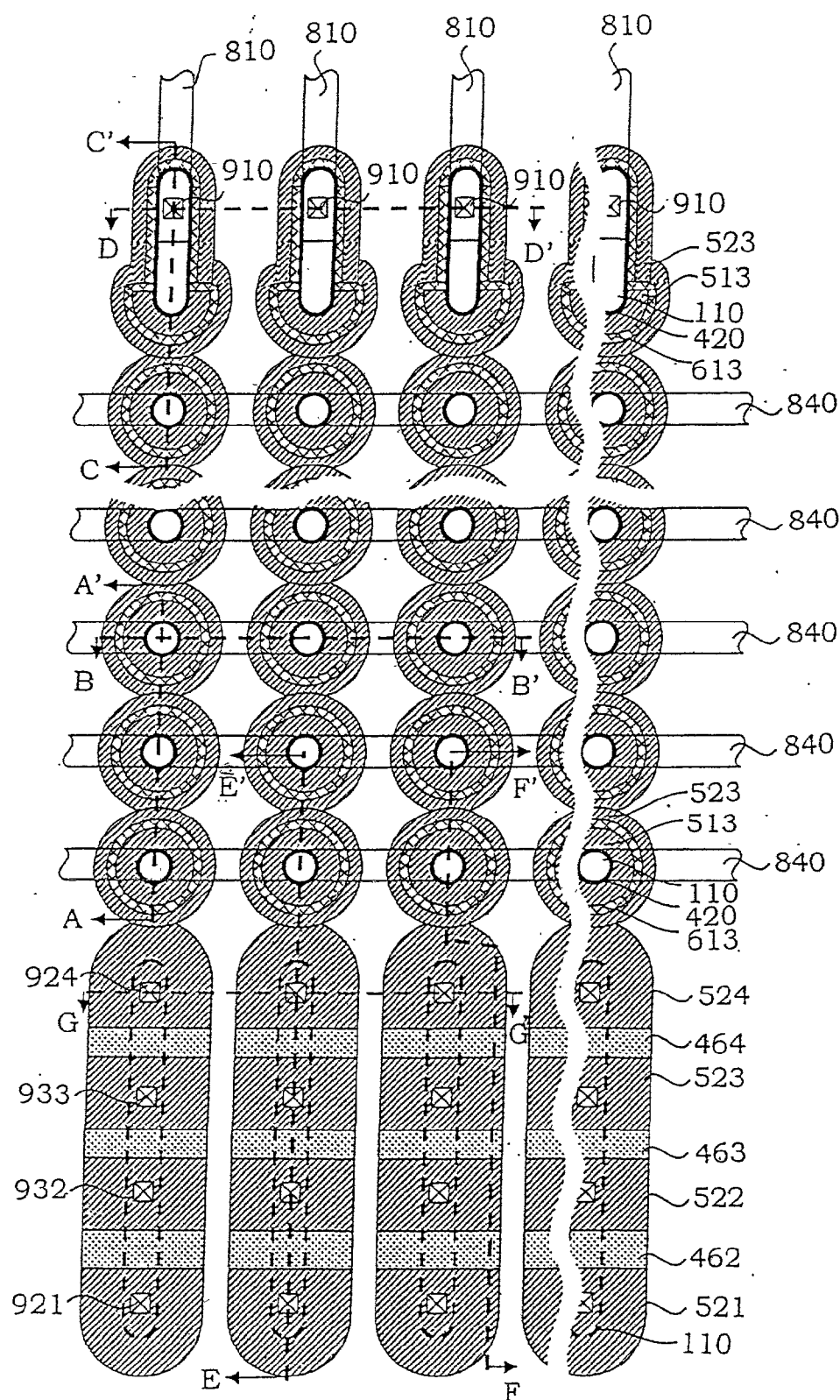


Fig. 1171

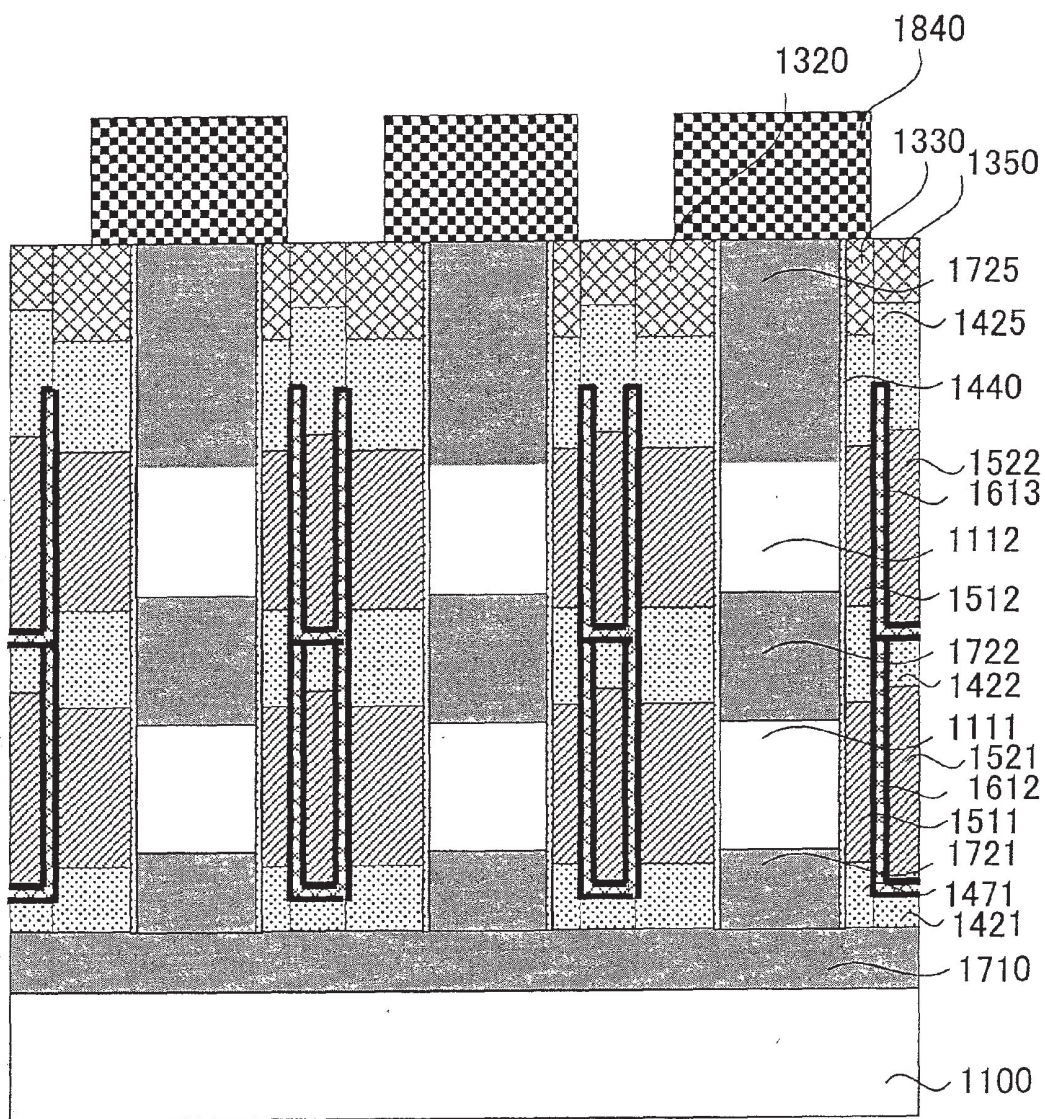
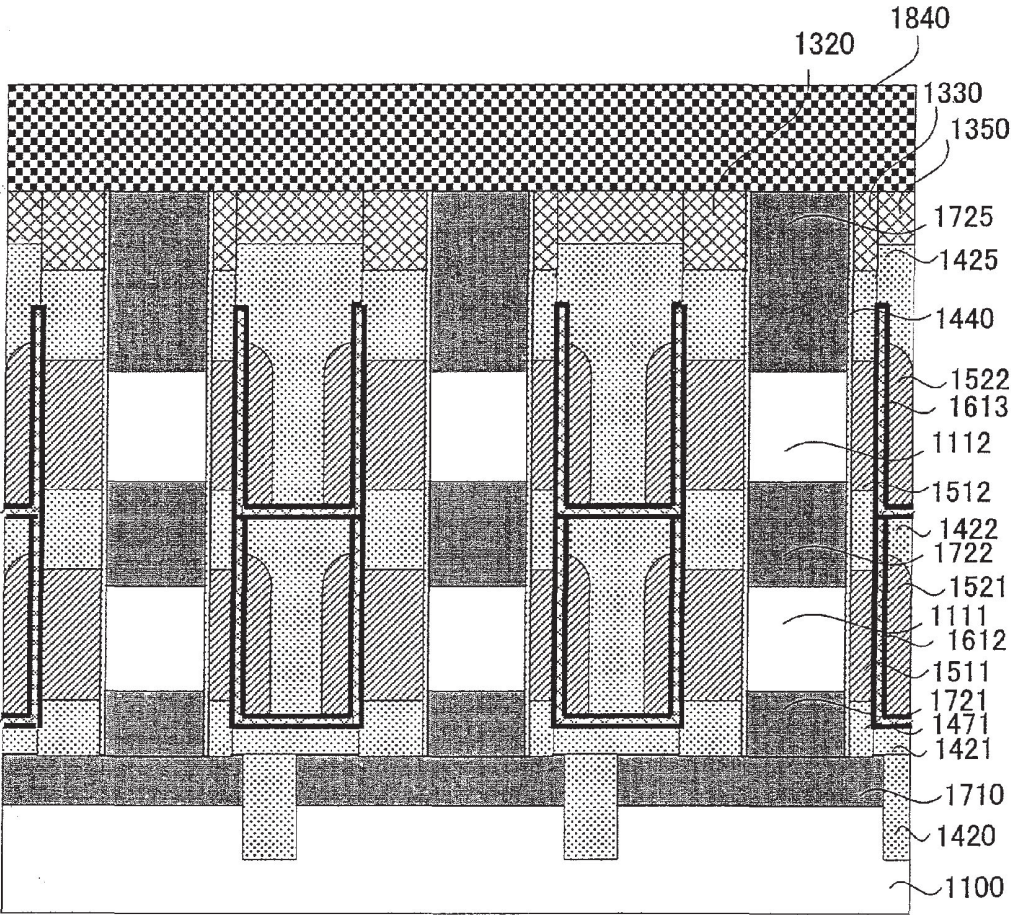


Fig. 1172



SEMICONDUCTOR MEMORY AND ITS PRODUCTION PROCESS

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is related to Japanese Patent Application No. 2001-142454 filed on Mar. 30, 2001, No. 2001-264927 filed on Jun. 23, 2001, No. 2001-264928 filed on Jun. 23, 2001, No. 2001-266490 filed on Jun. 23, 2001 and No. 2001-266491 filed on Jun. 23, 2001, whose priority is claimed under 35 USC §119, the disclosure of which is incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor memory and its production process, and more particularly, the invention relates to a semiconductor memory provided with a memory transistor having a charge storage layer and a control gate, and its production process.

[0004] 2. Description of Related Art As a memory cell of an EEPROM, is known a device of a MOS transistor structure having a charge storage layer and a control gate in a gate portion, in which an electric charge is injected into and released from the charge storage layer by use of a tunnel current. In this memory cell, data "0" and "1" are stored as changes in a threshold voltage by the state of the charge in the charge storage layer. For example, in the case of an n-channel memory cell using a floating gate as the charge storage layer, when a source/drain diffusion layer and a substrate are grounded and a high positive voltage is applied to the control gate, electrons are injected from the substrate into the floating gate by a tunnel current. This injection of electrons shifts the threshold voltage of the memory cell toward positive. When the control gate is grounded and a high positive voltage is applied to the source/drain diffusion layer or the substrate, electrons are released from the floating gate to the substrate by the tunnel current. This release of electrons shifts the threshold voltage of the memory cell toward negative.

[0005] In the above-described operation, a relationship of capacity coupling between the floating gate and the control gate with capacity coupling between the floating gate and the substrate plays an important role in effective injection and release of electrons, i.e., effective writing and erasure. That is, the larger the capacity between the floating gate and the control gate, the more effectively the potential of the control gate can be transmitted to the floating gate and the easier the writing and erasure become.

[0006] With recent development in semiconductor technology, especially, in micro-patterning techniques, the size reduction and the capacity increase of memory cells of EEPROM are rapidly progressing. Accordingly, it is important how large capacity can be ensured between the floating gate and the control gate.

[0007] For increasing the capacity between the floating gate and the control gate, it is necessary to thin a gate insulating film therebetween, to increase the dielectric constant of the gate insulating film or to enlarge an area where the floating gate opposes the control gate.

[0008] However, the thinning of the gate insulating film is limited in view of reliability of memory cells. For increasing the dielectric constant of the gate insulating film, a silicon nitride film is used as the gate insulating film instead of a silicon oxide film. This is also questionable in view of reliability and is not practical.

[0009] Therefore, in order to ensure a sufficient capacity between the floating gate and the control gate, it is necessary to set a sufficient overlap area therebetween. This is, however, contradictory to the size reduction of memory cells and the capacity increase of EEPROM.

[0010] In an EEPROM disclosed by Japanese Patent No. 2877462, memory transistors are formed by use of sidewalls of a plurality of pillar-form semiconductor layers arranged in matrix on a semiconductor substrate, the pillar-form semiconductor layers being separated by trenches in a lattice form. A memory transistor is composed of a drain diffusion layer formed on the top of each pillar-form semiconductor layer, a common source diffusion layer formed at the bottom of the trenches, and a charge storage layer and a control gate which are around all the periphery of the sidewall of the pillar-form semiconductor layer. The control gate is provided continuously for a plurality of pillar-form semiconductor layers lined in one direction so as to form a control gate line, and a bit line is connected to drain diffusion layers of a plurality of memory transistors lined in a direction crossing the control gate line. The above-described charge storage layer and the control gate are formed in a lower part of the pillar-form semiconductor layer. In a one transistor/one cell structure, if a memory transistor is over-erased, i.e., a reading potential is 0 V and the threshold is negative, a cell current flows in the memory cell even if it is not selected. To surely prevent this inconvenience, a selection gate transistor is provided above the memory transistor. The selection gate transistor has a gate electrode formed to surround at least a part of the periphery of the pillar-form island semiconductor layer in an upper part of the pillar-form semiconductor layer.

[0011] The prior-art EEPROM memory cell has the charge storage layer and the control gate which are formed by use of the sidewall of the island-like semiconductor layer to surround the pillar-form semiconductor layer. With this construction, a sufficiently large capacity can be ensured between the charge storage layer and the control gate with a small area occupied. The drain regions of the memory cells connected to the bit lines are formed on the top of the pillar-form semiconductor layers and completely insulated from each other by the trenches. A device isolation region can further be decreased and the memory cells are reduced in size. Accordingly, it is possible to obtain a mass-storage EEPROM with memory cells which provide excellent writing and erasing efficiency.

[0012] Hereinafter, explanation is given of a prior-art EEPROM with reference to figures. FIG. 1651 is a plan view of the prior-art EEPROM, and FIGS. 1652(a) and 1652(b) are sectional views taken on lines A-A' and B-B', respectively, in FIG. 1651.

[0013] In FIG. 1651, pillar-form silicon semiconductor layers 2 are columnar, that is, the top thereof is circular. However, the shape of the pillar-form silicon semiconductor layers need not be columnar. In the plan view of FIG. 1651, selection gate lines formed by continuing the gate electrodes of the selection gate transistors are not shown for avoiding complexity of the figure.

[0145] forming sidewall spacers of first conductive films on the charge storage layer, the first conductive films being separated from each other in a height direction; and

[0146] forming an impurity diffusion layer by introducing an impurity in self-alignment with the separated first conductive films.

[0147] Moreover, the present invention provides a process for producing a semiconductor memory which has a semiconductor substrate and one or more memory cells composed of at least one island-like semiconductor layer, a charge storage layer and a control gate which are formed to partially or entirely encircle a sidewall of the island-like semiconductor layer, at least one of said one or more memory cells being electrically insulated from the semiconductor substrate, the process comprising the steps of:

[0148] forming at least one island-like semiconductor layer on a semiconductor substrate;

[0149] forming an impurity diffusion layer by introducing an impurity in a part of a surface of the island-like semiconductor layer; and

[0150] forming sidewall spacers of first conductive films on the surface of the island-like semiconductor layer with intervention of an insulating film, the first conductive films being separated from each other in a height direction.

[0151] The present invention has been made in view of the above-mentioned problems. An object of the invention is to provide a semiconductor memory and a production process therefor, in which the degree of integration of the memory is improved by reducing the back-bias effect in a semiconductor memory having charge storage layers and control gates, capacity between the charge storage layers and the control gates is increased without increasing an area occupied by memory cells and variations in the characteristics of the memory cells are suppressed by minimizing the variations in gate lengths of the memory cell transistors and the difference in thermal histories of the memory cell transistors derived from the production process.

[0152] These and other objects of the present application will become more readily apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0153] FIGS. 1 to 11 are plan views illustrating various memory cell arrays of EEPROMs having floating gates as charge storage layers in semiconductor memory devices in accordance with the present invention;

[0154] FIG. 12 is a plan view illustrating a memory cell array of MONOS structure having a layered insulating film as a charge storage layer in a semiconductor memory device in accordance with the present invention;

[0155] FIG. 13 is a plan view illustrating a memory cell array of DRAM structure having a MIS capacitor as a charge

storage layer in a semiconductor memory device in accordance with the present invention;

[0156] FIG. 14 is a plan view illustrating a memory cell array of SRAM structure having a MIS transistor as a charge storage layer in a semiconductor memory device in accordance with the present invention;

[0157] FIGS. 15 to 42 are sectional views of various semiconductor memory devices having floating gates as charge storage layers in accordance with the present invention, the sectional views corresponding to those taken on line A-A' and line B-B' in FIG. 1;

[0158] FIGS. 43 to 54 are sectional views of various semiconductor memory devices having layered insulating films as charge storage layers in accordance with the present invention, the sectional views corresponding to those taken on line A-A' and line B-B' in FIG. 12;

[0159] FIGS. 55 to 60 are sectional views of various semiconductor memory devices having MIS capacitors as charge storage layers in accordance with the present invention, the sectional views corresponding to those taken on line A-A' and line B-B' in FIG. 13;

[0160] FIGS. 61 to 64 are sectional views of semiconductor memory devices having MIS transistors as charge storage layers in accordance with the present invention, the sectional views corresponding to those taken on line J1-J1', line J2-J2', line K1-K1' and line K2-K2' in FIG. 12;

[0161] FIGS. 65 to 77 are equivalent circuit diagrams of semiconductor memory devices in accordance with the present invention;

[0162] FIGS. 78 to 84 are examples of timing charts at reading, writing and erasing of a semiconductor memory device in accordance with the present invention;

[0163] FIGS. 85 to 125 are sectional views (taken on line A-A' and line B-B' in FIG. 1) illustrating production steps for producing a semiconductor memory device in accordance with the present invention;

[0164] FIGS. 126 to 131 are enlarged plan views or plan views of an island-like semiconductor layer in each production step for producing a semiconductor memory device in accordance with the present invention;

[0165] FIGS. 132 to 1650 are sectional views (taken on line A-A' and line B-B' in FIG. 1, FIG. 5, FIG. 10 or FIG. 13) illustrating various production steps for producing semiconductor memory devices in accordance with the present invention;

[0166] FIG. 1651 is a plan view illustrating a prior-art EEPROM;

[0167] FIG. 1652 is a sectional view taken on line A-A' and B-B' in FIG. 1651;

[0168] FIGS. 1653 to 1656 are sectional views illustrating production steps for producing a prior-art EEPROM;

[0169] FIG. 1657 is a plan view of a prior-art EEPROM and a corresponding equivalent circuit diagram;

[0170] FIGS. 1658 to 1659 are sectional views of various kinds of prior-art memory cells of MNOS structure; and

[0171] FIG. 1660 is a sectional view of a prior-art semiconductor device with a plurality of memory cells formed on each pillar-form silicon layer.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0172] The semiconductor memory of the present invention mainly has a first conductivity type semiconductor substrate and one or more memory cells. The memory cell is constituted of at least one island-like semiconductor layer, at least one charge storage layer and at least one control gate (a third electrode). The charge storage layer and the control gate are formed around a sidewall of the island-like semiconductor layer. At least one of said one or more memory cells is electrically insulated from the semiconductor substrate. An insulating film is provided which allows an electric charge to pass through at least a part of a region between the charge storage layer and the island-like semiconductor layer.

[0173] Alternatively, the semiconductor memory of the present invention mainly has a first conductivity type semiconductor substrate and one or more memory cells. The memory cell is constituted of at least one island-like semiconductor layer formed by epitaxial growth, at least one charge storage layer and at least one control gate (a third electrode). The charge storage layer and the control gate are formed around a sidewall of the island-like semiconductor layer. At least one of said one or more memory cells is electrically insulated from the semiconductor substrate.

[0174] That "at least one of said one or more memory cells is electrically insulated from the semiconductor substrate" means that the island-like semiconductor layer is electrically insulated from the semiconductor substrate. If two or more memory cells are formed in one island-like semiconductor layer, the memory cells are electrically insulated and thereby a memory cell/memory cells above an insulating site is/are electrically insulated from the semiconductor substrate. If a selection gate (a memory gate) is formed below the memory cell(s), a selection transistor composed of the selection gate is electrically insulated from the semiconductor substrate or the selection transistor is electrically insulated from a memory cell and thereby a memory cell/memory cells above an insulating site is/are electrically insulated from the semiconductor substrate. It is preferably in particular that the selection transistor is formed between the semiconductor substrate and the island-like semiconductor layer or below the memory cell(s) and the selection transistor is electrically insulated from the semiconductor substrate. Electric insulation may be made, for example, by forming a second conductivity type impurity diffusion layer over a region to be insulated, by forming the second conductivity type impurity diffusion layer in part of the region to be insulated and utilizing a depletion layer at a junction of the second conductivity type impurity diffusion layer, or by providing a distance not allowing electric conduction and achieving electric insulation as a result. The semiconductor substrate may be electrically insulated from the memory cell(s) or the selection transistor by an insulating film of SiO₂ or the like. In the case where a plurality of memory cells are formed in one island-like semiconductor layer and selection transistors are optionally formed above or below the memory cells, the electric insulation may be formed between optional memory cells and/or a selection transistor and a memory cell.

[0175] The charge storage layer and the control gate may be formed all around the sidewall of the island-like semiconductor layer or on a part of the sidewall.

[0176] Only one memory cell or two or more memory cells may be formed on one island-like semiconductor layer. If three or more memory cells are formed, a selection gate is preferably formed below and/or above the memory cells to form a selection transistor together with the island-like semiconductor layer.

[0177] The insulating film provided between the charge storage layer and the island-like semiconductor layer may be, for example, a film usually functions as a tunnel insulating film. Any insulating film may be used as long as it allows an electron charge to pass through at least a certain region. More particularly, the insulating film may be formed as a gate insulating film over the almost entire surface of the island-like semiconductor layer and as a tunnel gate insulating film only in an entire region or a partial region immediately below the charge storage layer. The insulating film may be formed of a silicon oxide film, a silicon nitride film, a laminated film thereof (e.g., an NO film, an ON film, an ONO film and the like). The insulating film may have a uniform thickness or partially reduced thickness as long as it allows the electric charge to pass through. The thickness may suitably be adjusted depending on the voltage to be applied to the semiconductor memory. For example, a thickness of about 7 to 15 nm is preferable for the silicon oxide film.

[0178] Hereinafter, are explained constructions in which a plurality of, for example, two memory cells are arranged in series on one island-like semiconductor layer, island-like semiconductor layers are arranged in matrix and selection transistors are disposed below and above the memory cells. A gate electrode of the selection transistor below the memory cells is represented as a second electrode and a gate electrode of the selection transistor above the memory cells is represented as a fifth electrode. A tunnel insulating film is represented as a third insulating film, a sidewall spacer is represented as a fourth insulating film, and a gate insulating film which is a part of the selection transistor is represented as a thirteenth insulating film.

[0179] In the above-mentioned semiconductor memory, an impurity diffusion layer for reading the state of a charge stored in the memory cells is formed as a source or drain (first wiring) of the memory cells in the island-like semiconductor layer. This impurity diffusion layer electrically insulates the island-like semiconductor layer from the semiconductor substrate. Control gates formed in a plurality of island-like semiconductor layers are arranged continuously in one direction to form a control gate line (third wiring). Another impurity diffusion layer is formed as a drain or source of the memory cells in the island-like semiconductor layer and a plurality of such impurity diffusion layers in a direction crossing the control gate line are electrically connected to form a bit line (fourth wiring).

[0180] Although the control gate line and the bit line orthogonal to the control gate may be in any three-dimensional directions, are explained hereinafter constructions in which the lines are formed in directions horizontal to the semiconductor substrate.

[0181] Embodiments of Memory Cell Arrays as Shown in Plan Views

[0182] The memory cell array in the semiconductor memory of the present invention is described with reference to plan views shown in FIG. 1 to FIG. 14. FIG. 1 to FIG. 11 are plan views illustrating EEPROM memory cell arrays having floating gates as charge storage layers. FIG. 12 is a plan view illustrating a memory cell array of MONOS structure having laminated insulating films as charge storage layers, FIG. 13 is a plan view illustrating a memory cell array of DRAM structure having MIS capacitors as charge storage layers, and FIG. 14 is a plan view illustrating a memory cell array of SRAM structure having MIS transistors as charge storage layers. Selection gate transistors are not shown in these figures for avoiding complexity. These figures also illustrate layouts of selection gate lines as second or fifth wiring which are gate electrodes for selecting memory cells (referred to as "selection gates" hereinafter), control gates as third wiring, bit lines as fourth wiring and source lines as first wiring.

[0183] In FIG. 1, island-like semiconductor layers in a columnar form for constituting memory cells are arranged to be located at intersections where a group of parallel lines and another group of parallel lines cross at right angles. For example, the island-like semiconductor layers are not disposed alternately but aligned in vertical and lateral directions. First, second, third and fourth wiring layers 840 for selecting and controlling the memory cells are disposed in parallel to the surface of the substrate.

[0184] By changing intervals between island-like semiconductor layers between an A-A' direction which crosses the fourth wiring layers 840 and a B-B' direction which is parallel to the fourth wiring layers 840, second conductive films which act as the control gates of the memory cells are formed continuously in one direction, in the A-A' direction in FIG. 1, to be the third wiring layers.

[0185] Likewise, second conductive films which act as the gates of the selection gate transistors are formed continuously in one direction to be the second wiring layers.

[0186] A terminal for electrically connecting with the first wiring layer disposed on a substrate side of island-like semiconductor layers is provided, for example, at an A' side end of a row of memory cells connected in the A-A' direction in FIG. 1, and terminals for electrically connecting with the second and third wiring layers are provided at an A side end of the row of memory cells connected in the A-A' direction in FIG. 1. The fourth wiring layers 840 disposed on a side of the island-like semiconductor layers opposite to the substrate are electrically connected to the island-like semiconductor layers in the columnar form for constituting memory cells. In FIG. 1, the fourth wiring layers 840 are formed in the direction crossing the second and third wiring layers.

[0187] The terminals for electrically connecting with the first wiring layers are formed of island-like semiconductor layers, and the terminals for electrically connecting with the second and third wiring layers are formed of second conductive films covering the island-like semiconductor layers, respectively.

[0188] The terminals for electrically connecting with the first, second and third wiring layers are connected to first contacts 910, second contacts 921 and 924 and third contacts 932 and 933, respectively.

[0189] In FIG. 1, the first wiring layers 810 are lead out onto the top of the semiconductor memory via the first contacts 910.

[0190] The arrangement of the island-like semiconductor layers in the columnar form is not particularly limited to that shown in FIG. 1 but may be any arrangement so long as the above-mentioned positional relationship and electric connection between the wiring layers are realized.

[0191] For example, the island-like semiconductor layers connected to the first contacts 910 are all located at the A' side ends of the memory cells connected in the A-A' direction in FIG. 1. However, they may be located entirely or partially on the A side ends or may be located at any of the island-like semiconductor layers constituting the memory cells connected in the A-A' direction.

[0192] The island-like semiconductor layers covered with the second conductive films connected to the second contacts 921 and 924 and the third contacts 932 and 933 may be located at the ends where the first contacts 910 are not disposed, may be located continuously at the ends where the first contacts 910 are disposed, and may be located at any of the island-like semiconductor layers constituting the memory cells connected in the A-A' direction which crosses the fourth wiring layers 840. The second contacts 921 and 924 and the third contacts 932 may be located at different places.

[0193] The width and shape of the first wiring layers 810 and the fourth wiring layers 840 are not particularly limited so long as a desired wiring can be obtained.

[0194] In the case where the first wiring layers, which are disposed on the substrate side of the island-like semiconductor layers, are formed in self-alignment with the second and third wiring layers formed of the second conductive films, the island-like semiconductor layers which act as the terminals for electrically connecting with the first wiring layers are electrically insulated from the second and third wiring layers but contact the second and third wiring layers with intervention of insulating films. In FIG. 1, for example, first conductive films are formed partially on the sidewalls of the island-like semiconductor layers connected to the first contacts 910 with intervention of insulating films. The first conductive films are located to face the island-like semiconductor layers for constituting the memory cells. The second conductive films are formed on the sidewalls of the first conductive films with intervention of insulating films. The second conductive films are connected to the second and third wiring layers formed continuously in the A-A' direction. At this time, the shape of the first and the second conductive films is not particularly limited.

[0195] The first conductive films on the sidewalls of the island-like semiconductor layers which act as the terminals for electrically connecting with the first wiring layers may be removed by setting the intervals between said island-like semiconductor layers to the first conductive films on the island-like semiconductor layers for constituting the memory cells, for example, to be two or less times larger than the thickness of the second conductive films.

[0196] In FIG. 1, the second and third contacts are formed on the second conductive films 521 to 524 which are formed to cover the top of the island-like semiconductor layers.

However, the shape of the second and third wiring layers is not particularly limited so long as their connection is realized.

[0197] FIG. 1 also shows lines for sectional views to be used for explaining examples of production processes, i.e., line A-A', line B-B', line C-C', line D-D', line E-E' and line F-F'.

[0198] In FIG. 2, island-like semiconductor layers in a columnar form for constituting memory cells are arranged to be located at intersections where a group of parallel lines and another group of parallel lines cross at oblique angles. First, second, third and fourth wiring layers for selecting and controlling the memory cells are disposed in parallel to the surface of the substrate.

[0199] By changing intervals between island-like semiconductor layers between an A-A' direction which crosses the fourth wiring layers 840 and a B-B' direction which is parallel to the fourth wiring layers 840, second conductive films which act as the control gates of the memory cells are formed continuously in one direction, in the A-A' direction in FIG. 2, to be the third wiring layers. Likewise, second conductive films which act as the gates of the selection gate transistors are formed continuously in one direction to be the second wiring layers.

[0200] A terminal for electrically connecting with the first wiring layer disposed on a substrate side of island-like semiconductor layers is provided, for example, at an A' side end of a row of memory cells connected in the A-A' direction in FIG. 2, and terminals for electrically connecting with the second and third wiring layers are provided at an A side end of the row of memory cells connected in the A-A' direction in FIG. 2. The fourth wiring layers 840 disposed on a side of the island-like semiconductor layers opposite to the substrate are electrically connected to the island-like semiconductor layers in the columnar form for constituting memory cells. In FIG. 2, the fourth wiring layers 840 are formed in the direction crossing the second and third wiring layers.

[0201] The terminals for electrically connecting with the first wiring layers are formed of island-like semiconductor layers, and the terminals for electrically connecting with the second and third wiring layers are formed of second conductive films covering the island-like semiconductor layers, respectively.

[0202] The terminals for electrically connecting with the first, second and third wiring layers are connected to first contacts 910, second contacts 921 and 924 and third contacts 932 and 933, respectively. In FIG. 2, the first wiring layers 810 are lead out onto the top of the semiconductor memory via the first contacts 910.

[0203] The arrangement of the island-like semiconductor layers in the columnar form is not particularly limited to that shown in FIG. 2 but may be any arrangement so long as the above-mentioned positional relationship and electric connection between the wiring layers are realized.

[0204] The island-like semiconductor layers connected to the first contacts 910 are all located at the A' side ends of the memory cells connected in the A-A' direction in FIG. 2. However, they may be located entirely or partially on the A side ends or may be located at any of the island-like

semiconductor layers constituting the memory cells connected in the A-A' direction. The island-like semiconductor layers covered with the second conductive films connected to the second contacts 921 and 924 and the third contacts 932 and 933 may be located at the ends where the first contacts 910 are not disposed, may be located continuously at the ends where the first contacts 910 are disposed, and may be located at any of the island-like semiconductor layers constituting the memory cells connected in the A-A' direction. The second contacts 921 and 924 and the third contacts 932 may be located at different places.

[0205] The width and shape of the first wiring layers 810 and the fourth wiring layers 840 are not particularly limited so long as a desired wiring can be obtained.

[0206] In the case where the first wiring layers, which are disposed on the substrate side of the island-like semiconductor layers, are formed in self-alignment with the second and third wiring layers formed of the second conductive films, the island-like semiconductor layers which act as the terminals for electrically connecting with the first wiring layers are electrically insulated from the second and third wiring layers but contact the second and third wiring layers with intervention of insulating films.

[0207] In FIG. 2, for example, first conductive films are formed partially on the sidewalls of the island-like semiconductor layers connected to the first contacts 910 with intervention of insulating films. The first conductive films are located to face the island-like semiconductor layers for constituting the memory cells. The second conductive films are formed on the sidewalls of the first conductive films with intervention of insulating films. The second conductive films are connected to the second and third wiring layers formed continuously in the A-A' direction. At this time, the shape of the first and the second conductive films is not particularly limited. The first conductive films on the sidewalls of the island-like semiconductor layers which act as the terminals for electrically connecting with the first wiring layers may be removed by setting the intervals between said island-like semiconductor layers to the first conductive films on the island-like semiconductor layers for constituting the memory cells, for example, to be two or less times larger than the thickness of the second conductive films.

[0208] In FIG. 2, the second and third contacts are formed on the second conductive films 2521 to 2524 which are formed to cover the top of the island-like semiconductor layers. However, the shape of the second and third wiring layers is not particularly limited so long as their connection is realized.

[0209] FIG. 2 also shows lines for sectional views to be used for explaining examples of production processes, i.e., line A-A' and line B-B'.

[0210] In FIG. 3 and FIG. 4, in contrast to FIG. 1 and FIG. 2, island-like semiconductor layers having a square cross section are differently oriented. The cross section of the island-like semiconductor layers is not particularly limited to circular or square but may be elliptic, hexagonal or octagonal, for example. However, if the island-like semiconductor layers have a dimension close to the minimum photoetching dimension, the island-like semiconductor layers, even if they are designed to have corners like square, hexagon or octagon, may be rounded by photolithography

surface of the substrate. Preferably the channel ion implantation is performed from various directions to the island-like semiconductor layers **2110** because a surface impurity concentration becomes more uniform. Alternatively, instead of the channel ion implantation, an oxide film containing boron may be deposited by CVD with a view to utilizing diffusion of boron from the oxide film. The impurity implantation from the surface of the island-like semiconductor layers **2110** may be carried out before the island-like semiconductor layers **2110** are covered with the thermally oxidized film **2450**, or during the formation of the island-like semiconductor layers **2110**. Alternatively, the impurities may be introduced to the silicon oxide films **2422** and **2424** in advance with a view to implanting the impurities in the island-like semiconductor layers **2110** by thermal treatment or the like before removing the silicon oxide films **2422** and **2424**. Means for the implantation are not particularly limited so long as an impurity concentration distribution is almost equal over the island-like semiconductor layers **2110**.

[1046] Subsequently, a silicon oxide film **2460**, for example, is formed as a tenth insulating film to be a tunnel oxide film to a thickness of about 10 nm around each island-like semiconductor layer **2110**, for example, by thermal oxidization. The tunnel oxide film, however, may be formed of not only a thermally oxidized film but also a CVD oxide film or a nitrogen oxide film.

[1047] Subsequently, a polysilicon film **2510**, for example, is deposited as a first conductive film to a thickness of about 50 to 200 nm. Using the silicon nitride film **2330** (the fifth insulating film) and the silicon nitride film **2340** (the sixth insulating film) as a mask, the polysilicon film **2510** is divided into polysilicon films **2511**, **2512**, **2513** and **2514**, for example, by anisotropic etching (FIGS. 929 and 933).

[1048] Production steps thereafter (FIGS. 930 and 934) follow Production example 23 (FIGS. 617 to 618 and FIGS. 619 to 620). However, the interlayer capacitance film is not formed.

[1049] Alternatively, the silicon oxide films **2411**, **2416**, **2417** and **2415** may be disposed as shown in FIGS. 935 and 937 and the polysilicon film **2510** may be divided into the polysilicon films **2511**, **2512**, **2513** and **2514**. Then, as shown in FIGS. 936 and 938, a semiconductor memory having a plurality of memory cells in which the MIS capacitors formed on the island-like semiconductor layer **2110** as the charge storage layers may be formed in accordance with Production example 1 (FIGS. 595 to 600 and FIGS. 606 to 611).

[1050] Production Example 45

[1051] In a semiconductor memory device to be formed in this example, after regions where charge storage layers and selection gates are formed are to be pre-defined by laminated films including floating gates as charge storage layer, tunnel oxide films are formed in hole-form trenches opened using a photoresist mask. Island-like semiconductor layer are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to a semiconductor substrate. Active regions of memory cells are electrically floated. In this semiconductor memory device, selection gate transistors are disposed at the top and at the bottom of each island-like semiconductor layer. A plurality of, for example, two memory cells are disposed between the

selection gate transistors. The tunnel oxide films of the memory cells are formed at the same time. The memory cells are connected in series along the island-like semiconductor layer. The gate insulating films of the selection gate transistors have the same thickness of the gate insulating films of the memory transistors.

[1052] This semiconductor memory device can be formed by the following production process. FIGS. 939 to 966 and FIGS. 967 to 994 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1053] First, on the surface of a P-type silicon substrate **1100**, a silicon oxide film **1410**, for example, is deposited to 2 to 20 nm as a first insulating film to be an implantation protection film, and a first impurity diffusion layer **1710** is introduced into the p-type silicon substrate **1100** using ion implantation (FIG. 939 and FIG. 967). For example, the ion implantation may be performed at an implantation energy of 5 to 100 keV at an arsenic dose of about 1×10^{14} to 1×10^{16} / cm² in a direction inclined about 0 to 7°. Instead of the ion implantation, an oxide film containing arsenic may be deposited by CVD, and arsenic diffusion from the oxide film may be utilized. The first impurity diffusion layer **1710** need not necessarily be introduced on the topmost surface of the P-type silicon substrate **1100**.

[1054] Subsequently, using as a mask a resist film **R5** patterned by a known photolithography technique (FIG. 940 and FIG. 968), the first insulating film **1410** and the P-type silicon substrate **1100** are etched 200 to 2000 nm, for example, by RIE so as to divide the first impurity diffusion layer **1710** to form a second trench **1220**.

[1055] After the resist film **RS** is removed (FIG. 941 and FIG. 969), a silicon oxide film **1420**, for example, is deposited to 100 to 300 nm as a fifth insulating film in the second trench **1220** and etched back to be buried. Means for burying the silicon oxide film **1420** is not particularly limited, and the silicon oxide film **1420** may be etched back using isotropic etching, etched back using anisotropic etching, buried by flattening using CMP or by a combination of these means. The silicon oxide film **1420** may be a silicon nitride film. The silicon oxide film **1410** may be removed or may be retained.

[1056] For example, in the case where the silicon oxide film **1410** is removed, a silicon oxide film **1471** is formed to 50 to 500 nm as a ninth insulating film on the P-type silicon substrate **1100** or on the first impurity diffusion layer **1710**. Subsequently, a polysilicon film **1511** is deposited to 100 to 1000 nm as a first conductive film. Thus silicon oxide films **1471** to **1475** as ninth insulating films and polysilicon films **1511** to **1514** as first conductive films are formed sequentially and alternately. On the silicon oxide film **1475**, a silicon nitride film **1320** is deposited to 100 to 1000 nm as a tenth insulating film (FIG. 942 and FIG. 970). At this time, the silicon oxide films **1471** to **1475** may have different thicknesses or may have the same thickness. The first conductive films **1511** to **1514** may have different thicknesses or may have the same thickness.

[1057] Thereafter, using as a mask a resist film **R6** patterned by a known photolithography technique (FIG. 943 and FIG. 971), the silicon nitride film **1320** is patterned, for example, by RIE (FIG. 944 and FIG. 972).

[1058] Subsequently, a silicon nitride film 1330, for example, is formed in the form of a sidewall as an eleventh insulating film on the sidewall of the silicon nitride film 1320 (FIG. 945 and FIG. 973). Using the silicon nitride film 1320 and the silicon nitride film 1330 as a mask, the silicon oxide films 1472 to 1475 and the polysilicon films 1511 to 1514 are anisotropically etched sequentially (FIG. 946 and FIG. 974) until the time when the first conductive film 1511 is removed, i.e., until the ninth insulating film 1472 is exposed, to form a third trench 1230.

[1059] Subsequently, a polysilicon film 1521, for example, is deposited to 20 to 200 nm as a second conductive film (FIG. 947 and FIG. 975).

[1060] Next, the polysilicon film 1521 is etched back to form a sidewall on the sidewall of the polysilicon film 1511 (FIG. 948 and FIG. 976). At this time, by setting the intervals between the third trenches 1230 to a predetermined value or smaller in the A-A' direction in FIG. 1, the polysilicon film 1521 is formed as a second wiring layer to be a selection gate line continuous in the direction without using a masking process.

[1061] Thereafter, a silicon nitride film 1342, for example, is deposited to 2 to 20 nm as a twelfth insulating film on the sidewall of the third trench 1230 (FIG. 949 and FIG. 977).

[1062] Subsequently, a silicon oxide film 1422, for example, is deposited to 50 to 500 nm as a fifth insulating film in the third trench 1230. Next, the silicon oxide film 1422 is buried by isotropic etching so as to remain only on the sidewall of the silicon oxide film 1472 in the third trench 1230 (FIG. 950 and FIG. 978), and then, the silicon nitride film 1342 is selectively removed, for example, by isotropic etching.

[1063] Further, an interlayer insulating film 1612 is formed on the surface of the third trench 1230 and the polysilicon films 1512 to 1514 (FIG. 951 and FIG. 979). This interlayer insulating film 1612 is formed of an ONO film. The ONO film can be formed in the same manner as Production example 1.

[1064] Subsequently, in the same manner as described above, a polysilicon film 1522 is deposited to 15 to 150 nm as a second conductive film (FIG. 952 and FIG. 980) and etched back to form a sidewall on the sidewall of the polysilicon film 1512 (FIG. 953 and FIG. 981). At this time, by setting the intervals between the third trenches 1230 to a predetermined value or smaller in the A-A' direction in FIG. 1, the polysilicon film 1522 is formed as a third wiring layer to be a control gate line continuous in the direction without using a masking process.

[1065] Thereafter, by repeating the above production steps, a silicon oxide film 1423, for example, is buried as fifth insulating film in the third trench 1230 so as to remain only on the side of a silicon oxide film 1473 as a ninth insulating film (FIG. 954 and FIG. 982), and then, the interlayer insulating film 1612 is selectively removed by isotropic etching.

[1066] Subsequently, an interlayer insulating film 1613 is formed on the surface of the third trench 1230 and the polysilicon films 1513 and 1514.

[1067] Next, a polysilicon film 1523, for example, is deposited to 15 to 150 nm as a second conductive film and

etched back to form a sidewall on the sidewall of the polysilicon film 1513. Further, by repeating in the same manner, a silicon oxide film 1424 is buried as a fifth insulating film in the third trench 1230 so as to remain only on the side of a silicon oxide film 1474 as a ninth insulating film (FIG. 955 and FIG. 983).

[1068] The interlayer insulating film 1613 is selectively removed, for example, by isotropic etching. Thereafter, in the state in which the surface of the third trench 1230 and the polysilicon film 1514 is exposed (FIG. 956 and FIG. 984), a polysilicon film 1524 is deposited to 15 to 150 nm as a second conductive film and etched back to form a sidewall on the sidewall of the polysilicon film 1514 (FIG. 957 and FIG. 985).

[1069] Further in the same manner, a silicon oxide film 1425 is buried as a fifth insulating film in the third trench 1230 on the side of a silicon oxide film 1475 as a ninth insulating film or on the side of a silicon nitride film 1330 as an eleventh insulating film (FIG. 958 and FIG. 986), and a silicon nitride film 1350, for example, is deposited as a fourteenth insulating film. Thereafter, the surface of the silicon nitride film 1350 is flattened, for example, by CMP (FIG. 959 and FIG. 987). Using as a mask a resist film R7 patterned by a known photolithography (FIG. 960 and FIG. 988), the silicon nitride film 1350, the silicon nitride film 1330 or the silicon nitride film 1320 is patterned, for example, by RIE.

[1070] Subsequently, the silicon oxide films 1471 to 1475 and the polysilicon films 1511 to 1514 are sequentially etched, for example, by anisotropic etching until the time when the silicon oxide film 1471 is removed, i.e., until the surface of the P-type silicon substrate 1100 is exposed, to form a first trench 1210 (FIG. 961 and FIG. 989).

[1071] Subsequently, a silicon oxide film 1440, for example, is formed as a third insulating film to be a tunnel oxide film of about 10 nm on the inner wall of the first trench 1210, for example, using CVD (FIG. 962 and FIG. 990). Here, the silicon oxide film 1440 is not particularly limited to a CVD oxide film, but may be a thermally oxidized film or a nitrogen oxide film.

[1072] Subsequently, the silicon oxide film 1440 on the first diffusion layer 1710 or on the P-type silicon substrate 1100 is selectively removed. For example, by anisotropic etching, the silicon oxide film 1440 is left in the form of a sidewall only on the sidewall of the first trench 1210 (FIG. 963 and FIG. 991).

[1073] Thereafter, the silicon oxide film 1440 is, for example, annealed in a nitrogen atmosphere at 800 to 1000° C. for 10 to 100 minutes. At this time, a gas other than nitrogen, for example, oxygen may be added. Preferably the silicon oxide film 1440 becomes about 10 nm thick after the thermal treatment.

[1074] Thereafter, the oxide film formed on the surface of the first impurity diffusion layer 1710 or on the P-type silicon substrate 1100 is optionally removed, for example, with diluted HF, and the first trench 1210 is filled with island-like semiconductor layers 1721 to 1725 and 1111 to 1114. For example, the semiconductor layers are selectively grown epitaxially from the first impurity diffusion layer 1710 or the P-type silicon substrate 1100 positioned at the bottom of the first trench 1210. At this time, from the

bottom, an N-type semiconductor layer 1721, a P-type semiconductor layer 1111, an N-type semiconductor layer 1722, a P-type semiconductor layer 1112, an N-type semiconductor layer 1723, a P-type semiconductor layer 1113, an N-type semiconductor layer 1724, a P-type semiconductor layer 1114 and an N-type semiconductor layer 1725 are sequentially formed (FIG. 964 and FIG. 992). The concentration of the N-type semiconductor layers 1721 to 1725 is formed at an arsenic dose of about 1×10^{18} to $1 \times 10^{21}/\text{cm}^3$, and the concentration of the P-type semiconductor layers 1111 to 1114 is formed at a boron dose of about 1×10^{15} to $1 \times 10^{17}/\text{cm}^3$. Preferably, the N-type semiconductor layers 1721 and 1722 overlap each other with intervention of the polysilicon layer 1511 and the silicon oxide film 1440; the N-type semiconductor layers 1722 and 1723 overlap each other with intervention of the polysilicon layer 1512 and the silicon oxide film 1440; the N-type semiconductor layers 1723 and 1724 overlap each other with intervention of the polysilicon layer 1513 and the silicon oxide film 1440; and the N-type semiconductor layers 1724 and 1725 overlap each other with intervention of the polysilicon layer 1514 and the silicon oxide film 1440.

[1075] Thereafter, the N-type semiconductor layer 1725 is reduced, for example, by etch back or by CMP to expose the silicon oxide film 1425 and divide the N-type semiconductor layer.

[1076] Subsequently, a fourth wiring layer 1840 is connected to the top of the N-type semiconductor layer 1725 so as to cross the direction of the second and third wiring layers.

[1077] Thereafter, an interlayer insulating film is formed by a known technique, and contact holes and metal wiring are formed. Thereby a semiconductor memory device is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive film.

[1078] For forming the buried silicon oxide films, the silicon oxide films may be formed not only by CVD but also by rotational coating.

[1079] Films formed on the surface of the polysilicon film such as the silicon nitride film (the second insulating film) 1342 may be formed of a layered film of a silicon oxide film/a silicon nitride film from the silicon surface. The impurity introduction into the polysilicon films 1511 to 1514 as the first conductive films and the polysilicon films 1521 to 1524 as the second conductive films may be performed when the polysilicon films are formed, after the polysilicon films are formed or after the sidewalls are formed. The timing of introducing the impurity is not limited so long as the conductive film is formed.

[1080] In this production example, the control gates of the memory cells are formed continuously in one direction without using a mask. However, that is possible only in the case where the island-like semiconductor layers are not disposed symmetrically to a diagonal. In contrast, if the island-like semiconductor layers are disposed symmetrically to a diagonal, for example, the wiring layers may be separated through patterning with use of resist films by photolithography.

[1081] By providing the selection gates in the top and the bottom of a set of memory cells, it is possible to prevent the phenomenon that a memory cell transistor is over-erased.

[1082] Production Example 46

[1083] In a semiconductor memory device to be formed in this example, after regions where charge storage layers and selection gates are formed are to be pre-defined by layered films including floating gates as charge storage layer, tunnel oxide films are formed in hole-form trenches opened in self-alignment with the floating gates. Island-like semiconductor layer are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to a semiconductor substrate. Active regions of memory cells are electrically floated. In this semiconductor memory device, selection gate transistors are disposed at the top and at the bottom of each island-like semiconductor layer. A plurality of, for example, two memory cells are disposed between the selection gate transistors. The tunnel oxide films of the memory cells are formed at the same time. The memory cells are connected in series along the island-like semiconductor layer. The gate insulating films of the selection gate transistors have the same thickness of the gate insulating films of the memory transistors.

[1084] This semiconductor memory device can be formed by the following production process. FIGS. 995 to 1004 and FIGS. 1005 to 1014 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1085] Production steps of this example are the same as those of Production Example 45 (FIGS. 939 to 957 and FIGS. 967 to 985) until a polysilicon film 1524, for example, is deposited to 15 to 150 nm as a second conductive film and etched back to form a sidewall on the sidewall of the polysilicon film 1514 as the first conductive film.

[1086] Thereafter, a silicon nitride film 1360, for example, is buried as a sixteenth insulating film on the side of the silicon oxide film 1475 as the ninth insulating film or on the side of the silicon nitride film 1330 as the eleventh insulating film in the third trench 1230. Thereafter, a silicon oxide film 1490, for example, is deposited 100 to 500 nm as a fifteenth insulating film. Subsequently, the surface of the silicon oxide film 1490 is flattened, for example, by CMP (FIG. 995 to FIG. 1005) to expose the silicon nitride film 1320 as the tenth insulating film (FIG. 996 to FIG. 1006).

[1087] Subsequently, the silicon nitride film 1320 is selectively removed, for example, by anisotropic etching, to form a recess formed of the silicon oxide film 1490 and the silicon oxide film 1475 or the silicon nitride film 1360 (FIG. 997 and FIG. 1007).

[1088] Next, a silicon nitride film 1370 is formed as a seventeenth insulating film in the form of a sidewall on the sidewall of the silicon oxide film 1490 (FIG. 998 and FIG. 1008). Using as a mask the silicon oxide film 1490 and the silicon nitride film 1370, the silicon oxide films 1472 to 1475 and the polysilicon films 1511 to 1514 are sequentially etched by anisotropic etching until the silicon oxide film 1471 is removed, i.e., until the surface of the P-type silicon substrate 1100 is exposed, to form a first trench 1210 (FIG. 999 and FIG. 1009).

[1089] When the silicon oxide films 1472 to 1475 are etched, the silicon oxide film 1490 is also removed. However, after the silicon nitride film 1360 is exposed, the sequential etching is performed using the silicon nitride film 1360 and the silicon nitride film 1370 as a mask.

formed in a thickness of about 20 to 40 nm. At this time, by setting, at 20 to 30 nm, the intervals between the polysilicon films 1511 and 1512, 1512 and 1513, and 1513 and 1514 as the first conductive films which are the floating gates of the memory cells, it becomes unnecessary to form, among the island-like semiconductor layers 1721 to 1725 to be formed in the first trench 1210 in a later step, impurity diffusion layers 1722, 1723, 1724 between the selection gates and the memory cells (FIG. 1168 and FIG. 1170).

[1205] Production Example 52

[1206] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers; selection gate transistors are formed, and then tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; two memory cells are arranged on each island-like semiconductor layer; the tunnel oxide films of the memory transistors are formed at the same time; and the transistors are connected in series along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172. FIG. 1171 and FIG. 1172 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1207] In this example, production step are the same as those of Production Example 45, except that, after the silicon oxide film 1473 is deposited as the ninth insulating film, without depositing the silicon oxide films 1474 and 1475 as the ninth insulating films and the polysilicon films 1513 and 1514 as the first conductive films, the silicon nitride film 1320 is deposited as the tenth insulating film and the polysilicon films 1521 and 1522 are arranged as the second conductive films on the sidewalls of the polysilicon films 1511 and 1522 as the first conductive films with intervention of interlayer insulating films 1612 and 1613. Thereby two memory transistors are arranged on the island-like semiconductor layer. A semiconductor memory device is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive film (FIG. 1171 and FIG. 117).

[1208] Production Example 53

[1209] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers on a semiconductor of a semiconductor substrate into which an oxide film is inserted, e.g., a SOI substrate; selection gates and control gates are formed, and then, tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; selection gate transistors are arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistors; the tunnel oxide films of the transistors are formed at the same time; the transistors are connected in series along the island-like semiconductor layer; and the gate insulating films of the selection gate transistors have the same thickness as the gate insulating

films of the memory transistors, as shown in FIG. 1173 and FIG. 1174. FIG. 1173 and FIG. 1174 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1210] This production example is substantially the same as Production Example 45 except that the SOI substrate is used.

[1211] Also by this production example, the same effect as of Production Example 45 can be obtained. Further the junction capacity of the impurity diffusion layer 1710 and the first wiring layer is suppressed or eliminated. The use of a SOI substrate as the substrate is applicable to all the examples of the present invention.

[1212] Production Example 54

[1213] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers; selection gates and control gates are formed, and then, tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; selection gate transistors are arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistors; the tunnel oxide films of the transistors are formed at the same film; the transistors are connected in series along the island-like semiconductor layer; and the gate insulating films of the selection gate transistors have larger than the thickness as the gate insulating films of the memory transistors, as shown in FIG. 1175 and FIG. 1176. FIG. 1175 and FIG. 1176 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1214] This production example is substantially the same as Production Example 1 except that the tunnel oxide film as the third insulating film, which is formed on the inner wall of the first trench 1210, is arranged to contact the polysilicon films 1512 and 1513 as the first conductive films as shown in FIG. 1175 and FIG. 1176, except that the silicon oxide film 1451 as the thirteenth insulating is arranged to contact the polysilicon film 1511 as the first conductive film, and except that the silicon oxide film 1454 as the thirteenth insulating film is arranged to contact the polysilicon film 1514 as the first conductive film.

[1215] Thereby, a structure is realized in which the gate insulating films of the selection gate transistors have a larger thickness than the gate insulating films of the memory transistors, and the same effect as of the Production Example 45 is obtained.

[1216] Production Example 55

[1217] FIGS. 1177 to 1179 and FIGS. 1180 to 1182 show a production example for obtained a structure in which the direction of the first wiring layer is parallel to the direction of the fourth wiring layer. FIGS. 1177 to 1179 and FIGS. 1180 to 1182 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

formed in a thickness of about 20 to 40 nm. At this time, by setting, at 20 to 30 nm, the intervals between the polysilicon films 1511 and 1512, 1512 and 1513, and 1513 and 1514 as the first conductive films which are the floating gates of the memory cells, it becomes unnecessary to form, among the island-like semiconductor layers 1721 to 1725 to be formed in the first trench 1210 in a later step, impurity diffusion layers 1722, 1723, 1724 between the selection gates and the memory cells (FIG. 1168 and FIG. 1170).

[1205] Production Example 52

[1206] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers; selection gate transistors are formed, and then tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; two memory cells are arranged on each island-like semiconductor layer; the tunnel oxide films of the memory transistors are formed at the same time; and the transistors are connected in series along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172. FIG. 1171 and FIG. 1172 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1207] In this example, production step are the same as those of Production Example 45, except that, after the silicon oxide film 1473 is deposited as the ninth insulating film, without depositing the silicon oxide films 1474 and 1475 as the ninth insulating films and the polysilicon films 1513 and 1514 as the first conductive films, the silicon nitride film 1320 is deposited as the tenth insulating film and the polysilicon films 1521 and 1522 are arranged as the second conductive films on the sidewalls of the polysilicon films 1511 and 1522 as the first conductive films with intervention of interlayer insulating films 1612 and 1613. Thereby two memory transistors are arranged on the island-like semiconductor layer. A semiconductor memory device is realized which has a memory function according to the state of a charge in the charge storage layer which is the floating gate made of the polysilicon film as the first conductive film (FIG. 1171 and FIG. 117).

[1208] Production Example 53

[1209] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers on a semiconductor of a semiconductor substrate into which an oxide film is inserted, e.g., a SOI substrate; selection gates and control gates are formed, and then, tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; selection gate transistors are arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistors; the tunnel oxide films of the transistors are formed at the same time; the transistors are connected in series along the island-like semiconductor layer; and the gate insulating films of the selection gate transistors have the same thickness as the gate insulating

films of the memory transistors, as shown in FIG. 1173 and FIG. 1174. FIG. 1173 and FIG. 1174 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1210] This production example is substantially the same as Production Example 45 except that the SOI substrate is used.

[1211] Also by this production example, the same effect as of Production Example 45 can be obtained. Further the junction capacity of the impurity diffusion layer 1710 and the first wiring layer is suppressed or eliminated. The use of a SOI substrate as the substrate is applicable to all the examples of the present invention.

[1212] Production Example 54

[1213] In this production example, a semiconductor memory device has a structure in which a plurality of floating gates are formed as the charge storage layers; selection gates and control gates are formed, and then, tunnel oxide films are formed; island-like semiconductor layers are formed in the form of pillars by selective epitaxial silicon growth and are electrically floated with respect to the semiconductor substrate; active regions of the memory cells are electrically floated; selection gate transistors are arranged at the top and the bottom of each island-like semiconductor layer; a plurality of, for example, two memory transistors are arranged between the selection gate transistors; the tunnel oxide films of the transistors are formed at the same film; the transistors are connected in series along the island-like semiconductor layer; and the gate insulating films of the selection gate transistors have larger than the thickness as the gate insulating films of the memory transistors, as shown in FIG. 1175 and FIG. 1176. FIG. 1175 and FIG. 1176 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.

[1214] This production example is substantially the same as Production Example 1 except that the tunnel oxide film as the third insulating film, which is formed on the inner wall of the first trench 1210, is arranged to contact the polysilicon films 1512 and 1513 as the first conductive films as shown in FIG. 1175 and FIG. 1176, except that the silicon oxide film 1451 as the thirteenth insulating is arranged to contact the polysilicon film 1511 as the first conductive film, and except that the silicon oxide film 1454 as the thirteenth insulating film is arranged to contact the polysilicon film 1514 as the first conductive film.

[1215] Thereby, a structure is realized in which the gate insulating films of the selection gate transistors have a larger thickness than the gate insulating films of the memory transistors, and the same effect as of the Production Example 45 is obtained.

[1216] Production Example 55

[1217] FIGS. 1177 to 1179 and FIGS. 1180 to 1182 show a production example for obtained a structure in which the direction of the first wiring layer is parallel to the direction of the fourth wiring layer. FIGS. 1177 to 1179 and FIGS. 1180 to 1182 are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM.