

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner

v.

BESANG INC.,

Patent Owner

Case IPR2023-00991

U.S. Patent No. 7,378,702

Petition for *Inter Partes* Review of

U.S. Patent No. 7,378,702

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PETITIONER'S EXHIBIT LIST

Exhibit No.	DESCRIPTION
1001	U.S. Patent 7,378,702 (“’702Pat.”)
1002	File History of U.S. Patent 7,378,702 (“’702FH”)
1003	Declaration of Dr. Carl Sechen (“Sechen”)
1004	Curriculum Vitae of Dr. Carl Sechen
1005	U.S. Patent 7,052,941 (“’941Pat.”)
1006	File History of U.S. Patent 7,052,941 (“’941FH”)
1007	U.S. Patent Appl. Publ. No. 2002/0028541 (“Lee”)
1008	U.S. Patent Appl. Publ. No. 2003/0157748 (“Kim”)
1009	Aspar, The Generic Nature of the Smart-Cut® Process for Thin Film Transfer, 30 J. Elec. Materials 834 (2001) (“Aspar”)
1010	U.S. Patent No. 6,034,882 (“Johnson”)
1011	U.S. Patent No. 5,571,730 (“Park”)
1012	U.S. Patent App. Publ. No. 2002/0154556 (“Endoh”)
1013	Complaint in <i>BeSang Inc. v. Intel Corporation</i> , 3:23-cv-00113-MAH (D. Or. January 23, 2023)
1014	Silicon Processing, Vol. 1 by Stanley Wolf (2000)
1015	Silicon Processing, Vol. 4 by Stanley Wolf (2002)
1016	U.S. Patent No. 6,355,501 (“Fung”)
1017	U.S. Patent No. 5,414,288 (“Fitch”)
1018	U.S. Patent No. 6,027,975 (“Hergenrother”)
1019	U.S. Patent No. 6,337,247 (“Schulz”)
1020	U.S. Patent No. 6,449,186 (“Noble”)
1021	U.S. Patent No. 6,943,067 (“Greenlaw”)
1022	IEEE 100: The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition (2000)
1023	U.S. Patent No. 5,882,987 (“Srikrishnan”)
1024	Maleville et al., Multiple SOI layers by multiple Smart-Cut® transfers, 2000 IEEE International SOI Conference (Oct. 2000) (“Maleville”)
1025	U.S. Patent No. 5,615,148 (“Yamamura”)
1026	U.S. Patent No. 5,544,103 (“Lambertson”)
1027	U.S. Patent No. 6,381,173 (“Zatelli”)
1028	Declaration of J. Munford

Exhibit No.	DESCRIPTION
1029	Minutes from Rule 16 Conference in <i>BeSang Inc. v. Intel Corporation</i> , 3:23-cv-00113-MAH
1030	March 2023 Average Time to Trial Statistics for the District of Oregon
1031	Excerpts of Endoh (EX1012)

LISTING OF CHALLENGED CLAIMS

Reference	Claim Limitation
Claim 1	
1[pre]	A semiconductor memory structure, comprising:
1[a]	a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and
1[b]	a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;
1[c]	wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and
1[d]	wherein the memory cell is a DRAM having at least one transistor.
Claim 13	
13[pre]	A semiconductor memory structure, comprising:
13[a]	a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
13[b]	a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
13[c]	the stackable add-on layer being bonded to the dielectric layer; and
13[d]	wherein the memory cells are nonvolatile memory cells having at least one transistor.
Claim 14	
14	The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.
Claim 15	
15	The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory

Reference	Claim Limitation
	cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.
Claim 16	
16	The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.
Claim 17	
17	The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

I. INTRODUCTION

Intel Corporation (“Petitioner”) requests *inter partes* review (“IPR”) of claims 1 and 13–17 (“Challenged Claims”) of U.S. Patent No. 7,378,702 (“the ’702 Patent”).

II. GROUNDS FOR STANDING (37 C.F.R. § 42.104(A))

Petitioner certifies that the ’702 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR to challenge the claims on the grounds herein. Petitioner files this Petition within one year of service of PO’s complaint against Petitioner in district court. *See* EX1013.

III. STATEMENT OF PRECISE RELIEF REQUESTED

Petitioner respectfully requests review and cancellation under 35 U.S.C. § 311 of the Challenged Claims in view of:

Prior Art
Lee (U.S. Pat. App. Pub. 2002/0028541), published on March 7, 2002; prior art at least under §102(b) ¹ (EX1007)
Kim (U.S. Pat. App. Pub. 2003/0157748), filed on February 20, 2002 and published on August 21, 2003; prior art at least under §§102(a), (e) (EX1008)
Aspar, The Generic Nature of the Smart-Cut® Process for Thin Film Transfer, 30 J. Elec. Materials 834 (2001); prior art at least under §102(b) (EX1009) (<i>see</i> EX1028 (J. Munford Declaration))
Johnson (U.S. Pat. 6,034,882), issued on March 7, 2000; prior art at least under §102(b) (EX1010)
Park (U.S. Pat. 5,571,730), issued on November 5, 1996; prior art at least under §102(b) (EX1011)
Endoh (U.S. Pat. App. Pub. 2002/0154556); prior art under at least §102(b) (EX1012)

¹ All references to 35 U.S.C. §§102, 103 are to the pre-AIA statutory framework.

Ground (all under 35 U.S.C. §103)	Claims	References
1A	13–17	Lee
1B	16–17	Lee, Endoh
1C	13–17	Lee, Kim
1D	16–17	Lee, Kim, Endoh
1E	13–17	Lee, Aspar
1F	16–17	Lee, Aspar, Endoh
2A	13	Johnson
2B	13	Johnson, Kim
2C	13	Johnson, Aspar
3	1	Park, Kim

IV. '702 PATENT OVERVIEW

A. Specification

The '702 Patent relates to “[v]ertically oriented semiconductor memory cells” “added to a separately fabricated substrate that includes electrical devices and/or interconnect.” ’702Pat., Abstract. The memory cells include SRAM, DRAM, or nonvolatile memory formed in a stackable add-on layer and are “vertically oriented with respect to a major surface of a wafer” or substrate. *Id.*, Abstract, 1:56–2:9, 3:50–61, 4:7–9. The benefit of utilizing this vertical orientation is to increase density in a “chip of a given surface area.” *Id.*, 3:56-61.

In the '702 Patent, “[t]he acronym ‘SOI’ generally refers to Silicon-on-Insulator,” and “SOI layer” “is used herein to refer to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate.” *Id.*, 4:45–53. “In this context, the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.” *Id.*, 4:53–60.

The '702 Patent's disclosure of bonding SOI layers to wafers or substrates is sparse. *See id.*, 4:45–5:7, 5:11–41. U.S. Patent No. 7,052,941 (“’941 Patent”), incorporated by reference in its entirety into the '702 Patent ('702Pat., 1:7–10), describes a process which forms a 3-D IC [integrated circuit] structure using an “SOI layer” in its Figures 4A–D. '941Pat., Abstract, 2:46–48, 6:29–35, 8:53–54.

Figures 4A–B show the two wafers used in that process. Figure 4A shows (i) base substrate 180, (ii) dielectric layer 153, (iii) metal layer 121, and (iv) metal layer 120. *Id.*, 8:54–9:18.

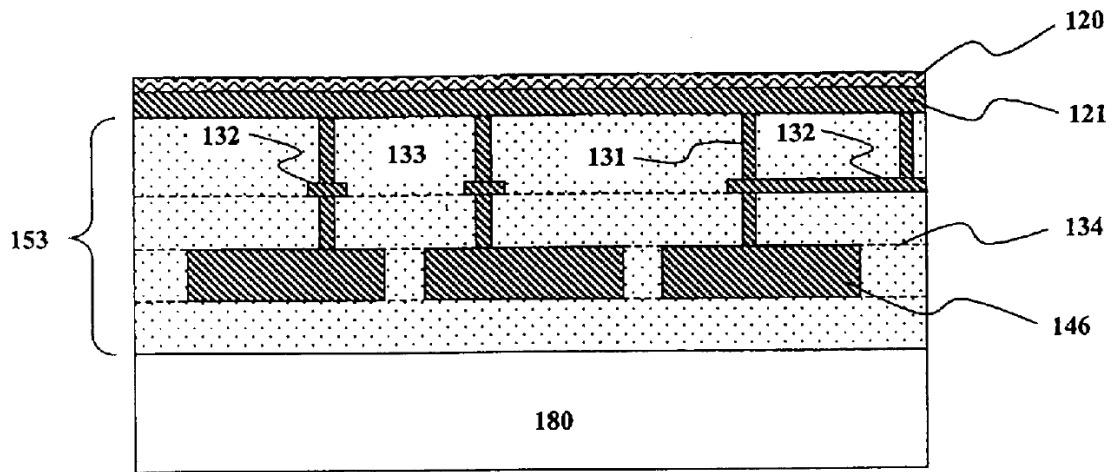


Fig. 4A

Figure 4B shows an entirely separate wafer with (i) SOI substrate 190 with optional detach layer 191, “using, for example, SmartCut technolog[y],” (ii) single crystal semiconductor layer 124, (iii) metal layer 121, and (iv) bonding layer 120 formed on metal layer 121. *Id.*, 9:19–43.

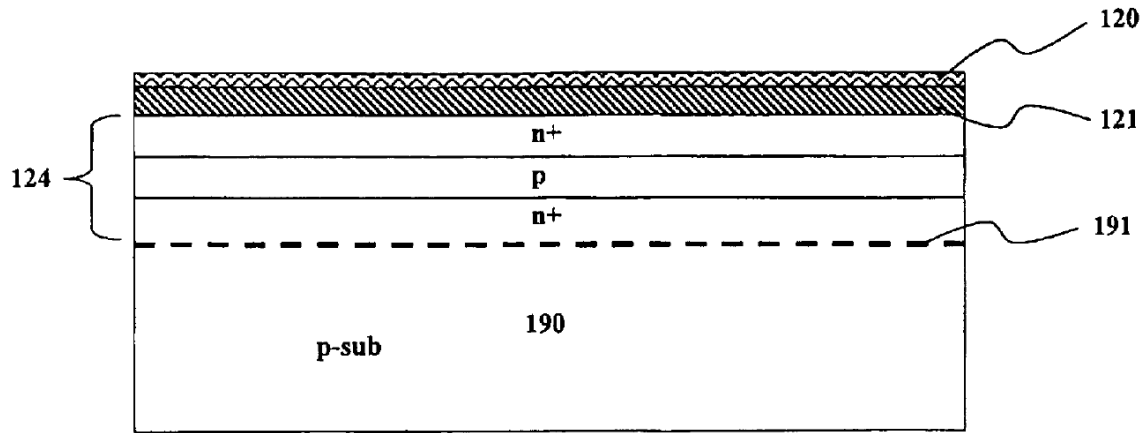
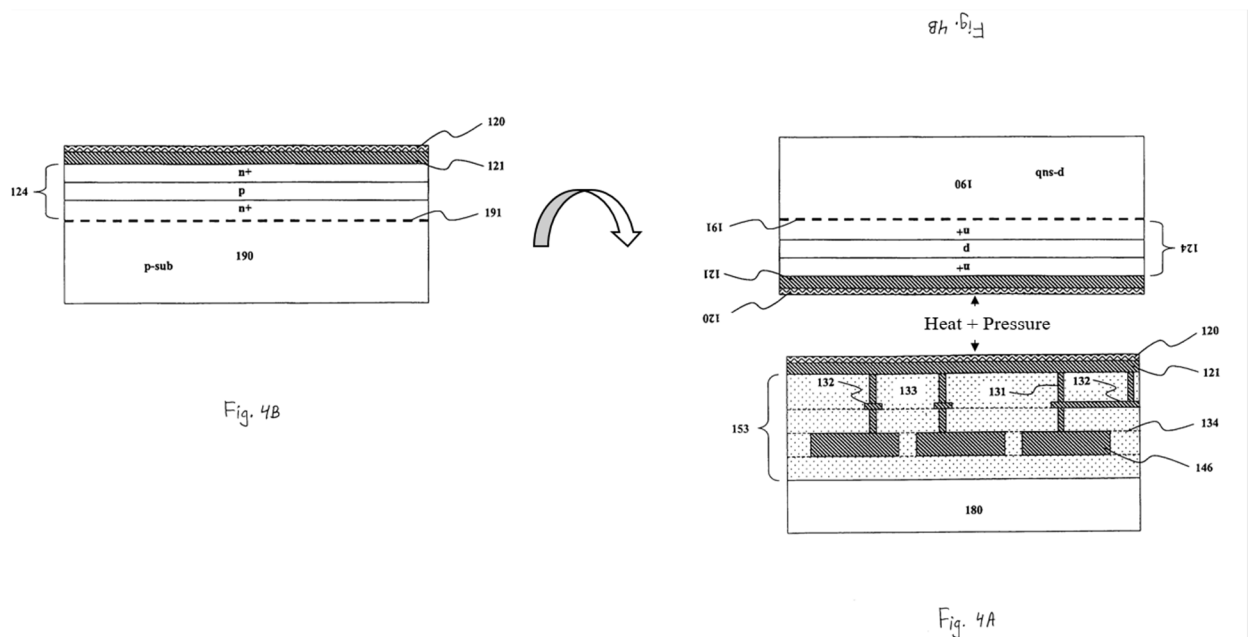


Fig. 4B

The Figure 4B wafer is flipped upside-down and bonded to the top of the Figure 4A wafer by applying heat and pressure (*id.*, 9:48–59) as depicted in modified Figures 4A–B below:



Id., Figs. 4A–B (annotated, combined); Sechen, ¶¶61-65. Figure 4C shows the result of this bonding:

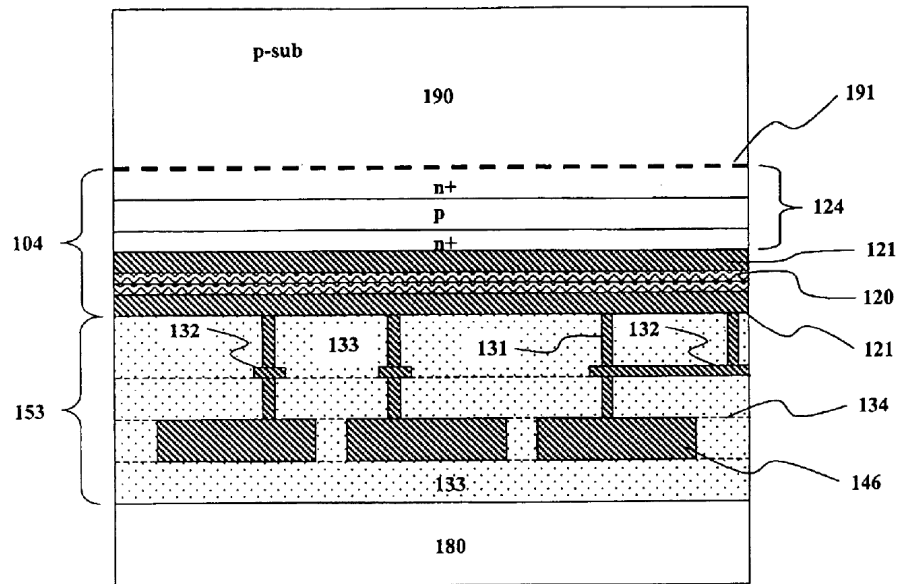


Fig. 4C

Figure 4D shows the final result of the '941 Patent's fabrication process, in which SOI layer 124 is exposed by detaching the SOI substrate 190, and then to the extent not previously fabricated, floating devices are made using isolation. '941Pat., 9:60–10:25.

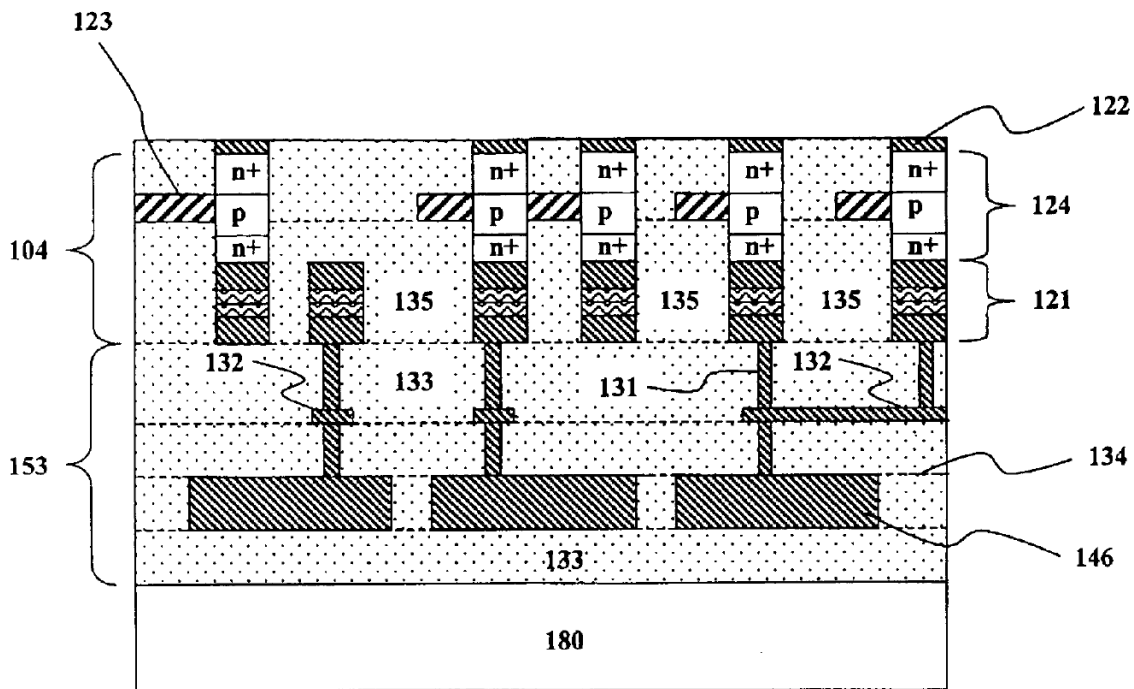


Fig. 4D

B. Prosecution History

The application leading to the '702 Patent was filed on September 3, 2004, and is a continuation-in-part of the application leading to the '941 Patent, filed on June 21, 2004. '702Pat., (21), (22), (63).² The Examiner did not make any prior art-

² June 21, 2004 is the earliest claimed priority date, and the references in this Petition qualify as prior art based on that date. Petitioner does not concede that any claims are entitled to that priority date. The '702 Patent is not entitled to foreign priority. See MPEP §214.01.

based rejections,³ and did not consider any of the references in this Petition during the prosecution of either the '702 or '941 Patents. *See* '702FH; '941FH.⁴

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) at the relevant time would have had a bachelor’s degree in electrical engineering, computer engineering, materials science, or a related field, and at least three years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa. *Sechen*, ¶37.⁵

VI. CLAIM CONSTRUCTION

Under 37 C.F.R. §42.100(b) and *Phillips v. AWH Corp.*, the “words of a claim are generally given their ordinary and customary meaning.” 415 F.3d 1303, 1312–

³ The Examiner cited only one reference, U.S. Patent Number 6,943,067 (“Greenlaw”), during prosecution but did not apply it. '702FH, 77.

⁴ The Examiner’s reasons for allowance merely indicate that no references of record taught or suggested the steps recited in each independent claim. '702FH, 121–23.

⁵ The IPR2023-00900 petitioner proposes a slightly different articulation of the level of skill. The unpatentability grounds below apply equally under that articulation. *Sechen*, ¶38.

13 (Fed. Cir. 2005) (en banc). The '702 Patent and the incorporated '941 Patent ('702Pat., 1:7–10) each contain a “Terminology” section wherein various terms are defined. '702Pat., 4:5–5:17; '941Pat., 5:25–6:35. For Challenged Claims terms defined in that section, such definitions are addressed in the grounds below. Petitioner further addresses the following terms. Because the Challenged Claims are unpatentable under any of the alternative constructions discussed below, Petitioner does not believe any terms require express construction.

A. “Stackable add-on layer ... the stackable add-on layer [is]/[being] bonded” (Claims 1, 13)

Independent claim 1 recites “wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate,” and independent claim 13 recites “the stackable add-on layer being bonded to the dielectric layer.” Based on the plain language and intrinsic record, a POSITA would have understood these limitations to require that the “stackable add-on layer” is wafer bonded to the recited layer of the substrate. Sechen, ¶71.

Based on the plain language, a POSITA would have understood that a “stackable add-on layer” must be its own structure capable of being stacked and added onto the other recited structures. *Id.* As a simplified analogy, when making a layer cake, each layer is baked individually, and then stacked one on top of each

other. So too with the “stackable add-on layer” recited in claims 1 and 13, where the stackable add-on layer is its own layer (one cake layer) capable of being stacked on another (the bottom cake layer). Sechen, ¶72. In the relevant art, a POSITA would have understood such stacking to be performed by wafer bonding of those layers. *Id.*

The intrinsic record supports this understanding. The ’702 Patent describes its “SOI layer” as a stackable add-on layer. ’702Pat., 4:53–57 (“[T]he SOI layer may be thought of as ... [a] stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.”). “[T]he ‘SOI layer’ is used herein to refer to a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate, such that a three dimensional stack is formed from the SOI layer and the previously fabricated wafer or similar type of substrate.” *Id.*, 4:48–53.

A POSITA would have understood the ’702 Patent’s description of its “SOI layer” requires wafer bonding. Sechen, ¶¶73-74. As discussed in Section IV.A, the incorporated ’941 Patent describes a process for creating a structure containing an SOI layer⁶ in its Figures 4A–D. ’941Pat., 8:53–10:56. The ’941 Patent also describes

⁶ The ’941 Patent also describes its “SOI layer” as a stackable add-on layer. ’941Pat., 6:12–17, 10:1–2.

existing technologies that allow for its SOI substrate to have a detach layer, so that after bonding, the SOI substrate can be removed other than the desired portion (i.e., including the stackable add-on layer). *Id.*, 6:61, 9:40–47 (“SOI substrate 190 may have a detach layer 191...using, for example, SmartCut (U.S. Pat. No. 5,882,987).”). Those wafer bonding processes cited in the intrinsic record were known to allow for a thin monocrystalline film formed on one wafer to be bonded to another previously fabricated wafer and then cleaved, like the “SOI layer” description in the ’702 Patent. Sechen, ¶¶74, 79-81 (citing EX1023, Abstract, 1:17–61, 4:8–16).

As discussed above, a POSITA would have understood “the stackable add-on layer [is]/[being] bonded” as recited in claims 1 and 13 requires that the “stackable add-on layer” is wafer bonded to the recited layer of the substrate. Sechen, ¶¶71-83.

PO may argue⁷ that “the stackable add-on layer [is]/[being] bonded” encompasses any layer that is directly or indirectly adhered to the recited layer of the substrate.⁸ Such a construction would not be correct, however, because it is not

⁷ E.g., based on PO’s district court complaint. EX1013.

⁸ In support, PO may point to the statement in the ’702 Patent that “the substrate bonded to lower dielectric layer 151 is called base substrate 103.” ’702Pat., 5:37–38; ’941Pat., 7:14–15 (same). That statement, however, refers to bonding a dielectric layer, not a “*stackable add-on*” layer, to the substrate. Sechen, ¶75.

consistent with the plain language of the claims or the intrinsic evidence as discussed above. Sechen, ¶84.

If the Board construes this limitation, it should adopt Petitioner’s construction. Petitioner, however, demonstrates below that the Challenged Claims are unpatentable under either construction. Thus, the Board need not explicitly construe this claim limitation to institute an IPR here.

B. “SOI pillar” (Claims 14–17)

“SOI pillar,” as recited in Challenged Claims 14–17, requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology. Sechen, ¶¶85-91. The intrinsic evidence supports this construction.

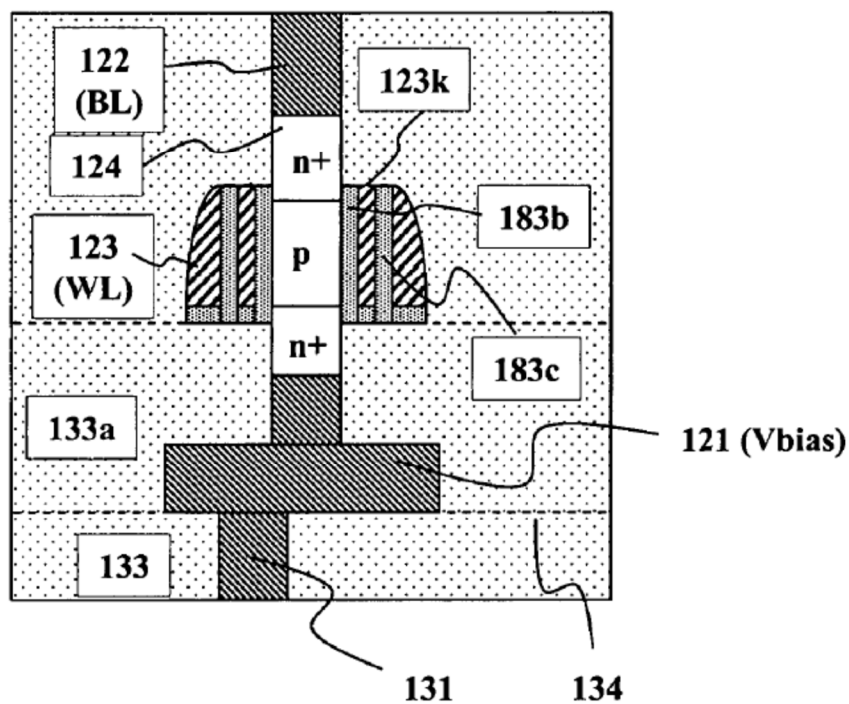
For “pillar,” the ’702 Patent states: “In various embodiments of the present invention, a FLD [floating device] can be directly contacted by metal electrodes at top, bottom, and intermediate regions of the individual doped stack structures (i.e., pillar structures).” ’702Pat., 5:21-22, 6:26–29. Thus, the intrinsic record supports that a “pillar” is a doped stack structure. Sechen, ¶86.

As to “SOI,” the ’702 Patent and its incorporated ’941 Patent each state “SOI” “generally refers to Silicon-on-Insulator.” ’702Pat., 4:45–46; ’941Pat., 6:4–5. Both patents then go on to discuss “SOI layer” (Section IV.A). ’702Pat., 4:46–62 (“a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate”);

'941Pat., 6:5–22. Both patents state “[i]ndividual semiconductor structures may be formed by etching through portions of the doped stack [in the SOI layer] to electrically isolate those structures,” and “[t]he spaces between such individual structures may be filled with dielectric material.” ’702Pat., 4:62–5:3; ’941Pat., 6:22–28. According to the ’702 Patent, “[i]n this way, the stackable add-on layer may provide a plurality of memory cells.” ’702Pat., 5:3–7. The ’941 Patent states: “Because single crystalline semiconductor layer 124 is formed by SOI technology, it is referred to herein simply as an SOI.” ’941Pat., 6:44–46.

Consistent with the description above, in the ’702 Patent embodiments, “SOI pillar” is labeled as 124. ’702Pat., 8:9, 15, 21, 29–30, 46; 9:16–17, 55. As one example, Figure 23 of the ’702 Patent is reproduced below:

Fig. 23



“FIG. 23 shows a vertical memory cell with a vertical MOSFET in a stackable add-on layer, where the vertical memory has a floating gate 123k and a control gate 123.”

Id., 9:24–26. In Figure 23, the vertical MOSFET is made up of the doped stack N+,

P, N+ regions formed in SOI pillar 124. Sechen, ¶¶88-90.

Thus, “SOI pillar,” as recited in Challenged Claims 14–17 and supported by the intrinsic record, requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology. *Sechen*, ¶¶85-91.

PO may argue that “SOI pillar” encompasses any pillar-shaped structure with insulating material below it. Such a construction, however, would be incomplete because it would read out “SOI.” *Sechen*, ¶92.

If the Board construes this limitation, it should adopt Petitioner’s construction. Nevertheless, Petitioner demonstrates below that Challenged Claims 14–17 are unpatentable under either construction. Thus, the Board need not explicitly construe this claim limitation to institute an IPR here.

VII. DETAILED GROUNDS EXPLANATION

A. Ground 1A: Obviousness over Lee (Claims 13–17)

PO may argue that “the stackable add-on layer being bonded” encompasses any type of layer, so long as that layer is directly or indirectly adhered to the “dielectric layer.” For claims 14–17, PO may argue that “SOI pillar” encompasses any pillar-shaped structure with insulating material below it. Such constructions are incorrect, but under them, claims 13–17 would have been obvious over Lee.

1. Claim 13

As discussed below, Lee renders obvious claim 13 under PO’s apparent constructions because Lee’s Figure 35 in combination with any of Figures 1A–1B,

2, 7, or 25A⁹ teaches the limitations of independent claim 13 and a POSITA would have been motivated to combine the relied-upon teachings.

a. 13[pre]

To the extent the preamble is limiting, Lee discloses or suggests it. Sechen, ¶¶112-113. Figure 35 of Lee (below) discloses a “semiconductor memory structure.” EX1007, ¶¶111 (“an array of charge storage logic or *memory* devices 3101”), 113 (“charge storage devices of the array may be any type of *semiconductor* devices which store charge”).

⁹ For clarity, any one of the following combinations renders claim 13 obvious: Figure 35 in combination with (1) Figure 1A, (2) Figure 1B, (3) Figure 2, (4) Figure 7, or (5) Figure 25A. Petitioner addresses all five combinations for claim 13 because dependent claims 14–17 (addressed in Sections VII.A.2–VII.A.5) depend from claim 13 and further recite specific memory cell structures, as taught in certain of those figures.

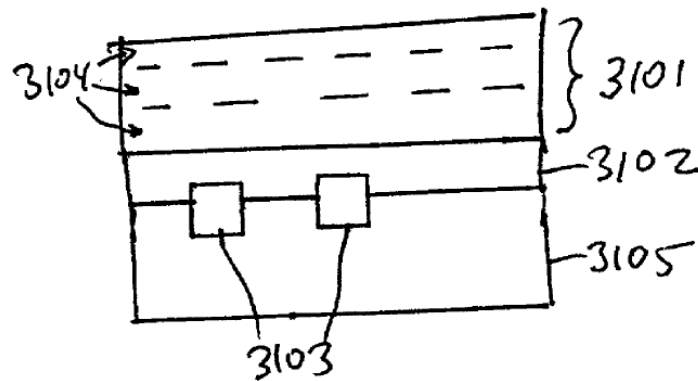


FIGURE 35

b. 13[a]

Lee discloses or suggests 13[a]. Sechen, ¶¶114-120. The '702 Patent defines “device” as “active and passive circuit elements,” including, but not limited to “FETs [field effect transistors] (n-channel and p-channel).” '702Pat., 4:28–34. The incorporated '941 Patent defines “device” as “one or more circuit elements that have characteristics that are voltage variant,” including, but not limited to, “FETs (n-channel and p-channel).” '941Pat, 5:51–54, 59–60.

Regarding “a substrate having electrical devices formed therein,” Lee’s Figure 35 (as annotated below) shows “driver circuits 3103” (green) “disposed in” substrate 3105 (red). EX1007, ¶¶110 (“[A]t least part, and preferably all, the driver (i.e., peripheral) circuitry is formed in the substrate under the array.”), 111. Lee further discloses that the driver circuitry can include “sense amps and charge pumps”

in the form of “CMOS [complementary metal oxide semiconductor] or other transistors.” *Id.*, ¶¶110–111, 208.

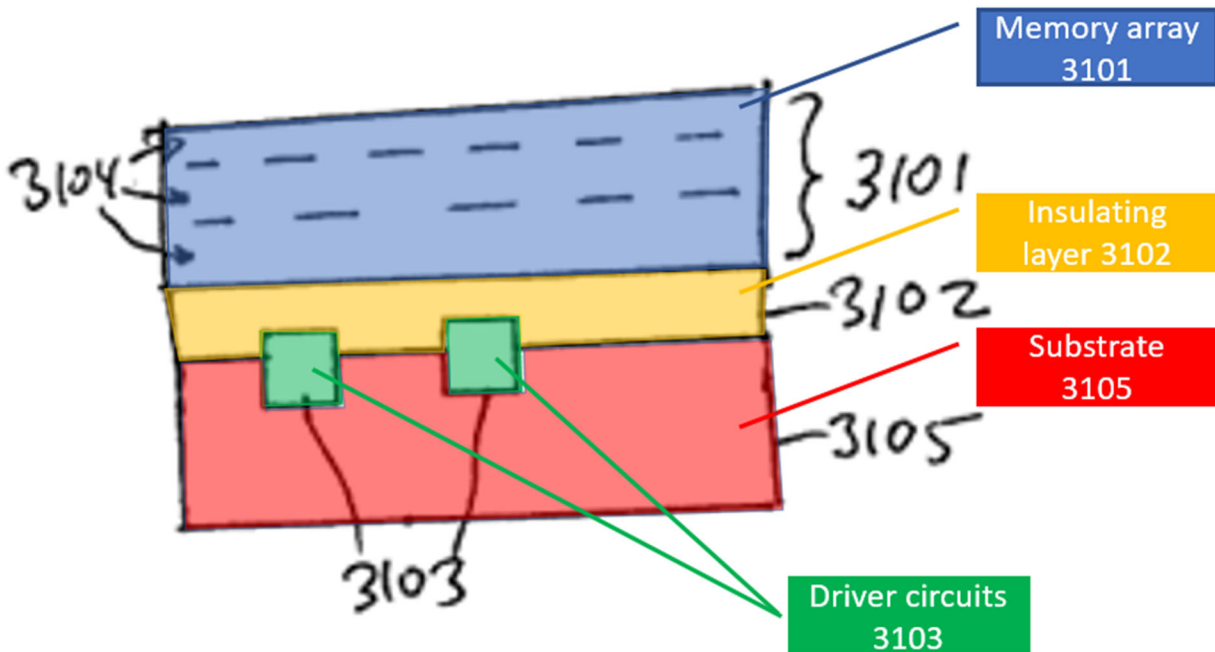


FIGURE 35

A POSITA would have understood “sense amps” or “charge pumps,” formed of “CMOS or other transistors,” are “devices” as the ’702 Patent defines them (i.e., “active circuit elements,” namely, those having power gain). Sechen, ¶117. Further, a POSITA would have known “CMOS or other transistors” are types of “FETs” or MOSFETs, which the ’702 Patent and incorporated ’941 Patent each provide as an example of a “device” (’702Pat., 4:28–34; ’941Pat, 5:51–54, 59–60). Sechen, ¶117. Accordingly, Lee’s substrate 3105 (“substrate”) has disposed therein driver circuits

3103, such as CMOS or other transistors (“having electrical devices formed therein”). *Id.*

Regarding “a dielectric layer disposed above the electrical devices,” in Figure 35 (above), Lee discloses “an interlayer insulating layer 3102” (yellow) above substrate 3105 (red) with driver circuits 3103 (green) disposed therein. EX1007, ¶111. Thus, insulating layer 3102 (“dielectric layer”) is “disposed above the electrical devices.” Sechen, ¶118 (citing EX1022, 568).

c. 13[b]

If PO argues a “stackable add-on layer” encompasses any type of layer that is directly or indirectly adhered to the “dielectric layer” (Section VI.A),¹⁰ bottom-most level 3104 as shown in Figure 35 (“stackable add-on layer”) containing two or more of Lee’s pillar memory devices as shown in any one of Figures 1A–1B, 2, 7, or 25A (“having a plurality of vertically oriented semiconductor memory cells”) teaches 13[b]. Sechen, ¶¶121-134.

Lee’s Figure 35 shows device levels 3104 above insulator layer 3102. EX1007, ¶111. Bottom-most level 3104 teaches a “stackable add-on layer” under PO’s apparent construction.

¹⁰ A “stackable add-on layer” is not so broad. Grounds 1C and 1E below discuss how 13[b] is taught by the prior art under the proper construction.

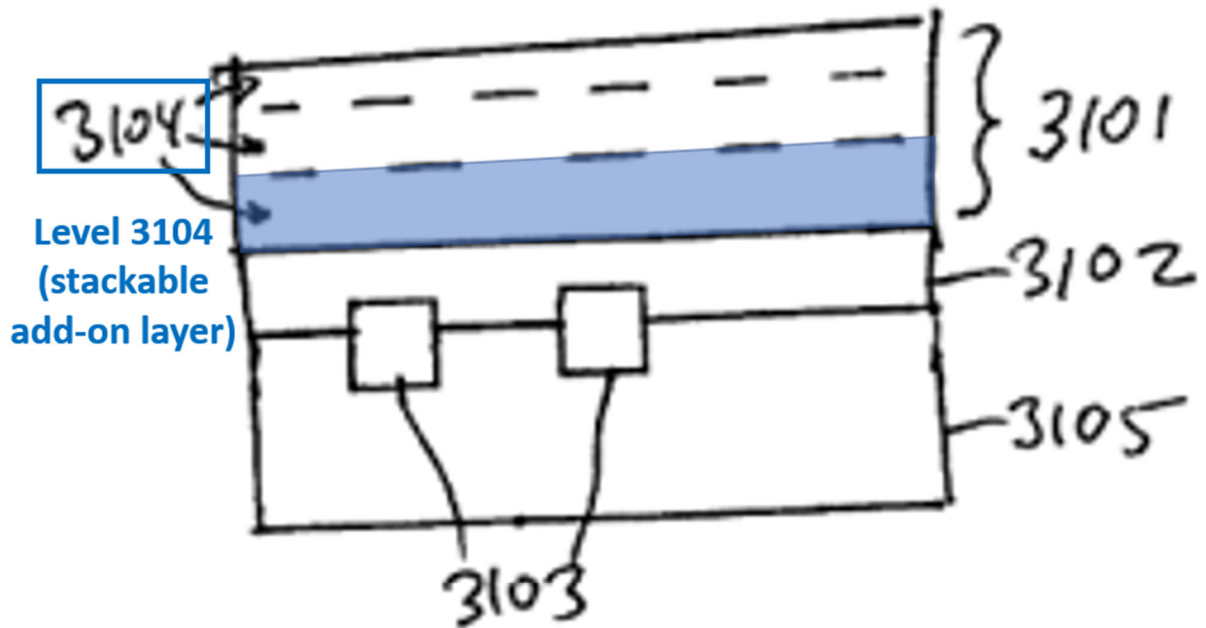


FIGURE 35

Figure 35 depicts level 3104 as a rectangular box, and is agnostic as to the particular structure of the memory cells in it. Lee, however, explains that the “charge storage devices of the array may be any type of semiconductor devices which store charge, such as EPROMs or EEPROMs.” *Id.*, ¶113; Sechen, ¶¶123-124 (citing EX1025–EX1027). A POSITA would have understood each level 3104 contains two or more memory cells. *E.g.*, EX1007, ¶¶26 (“each level comprising an array of TFT EEPROMs”), 107, Fig. 25A; Sechen, ¶124.

Lee further states “[i]n the preferred embodiments of the present invention described in detail below, the charge storage devices are formed in various

configurations, such as a pillar TFT EEPROM ... and various other configurations,” and then discusses a “first set of embodiments describ[ing] various pillar devices,” including those in Figures 1A–1B, 2, 7, and 25A. *Id.*, ¶¶113, 117–169 (describing the “Pillar Devices” as a first set of embodiments with Figure 1A described in ¶¶122–124, Figure 1B in ¶125, Figure 2 described in ¶¶126–131, Figure 7 described in ¶138, and Figure 25A described in ¶¶165–166). Figures 1A, 2, 7, and 25A are reproduced below:

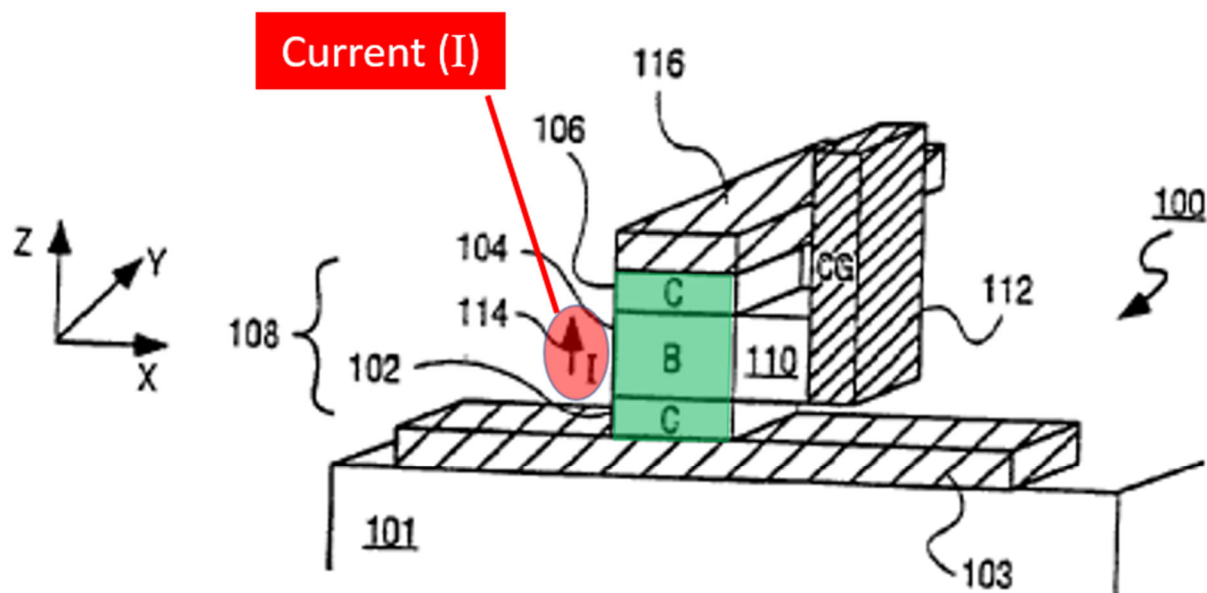


FIG. 1A

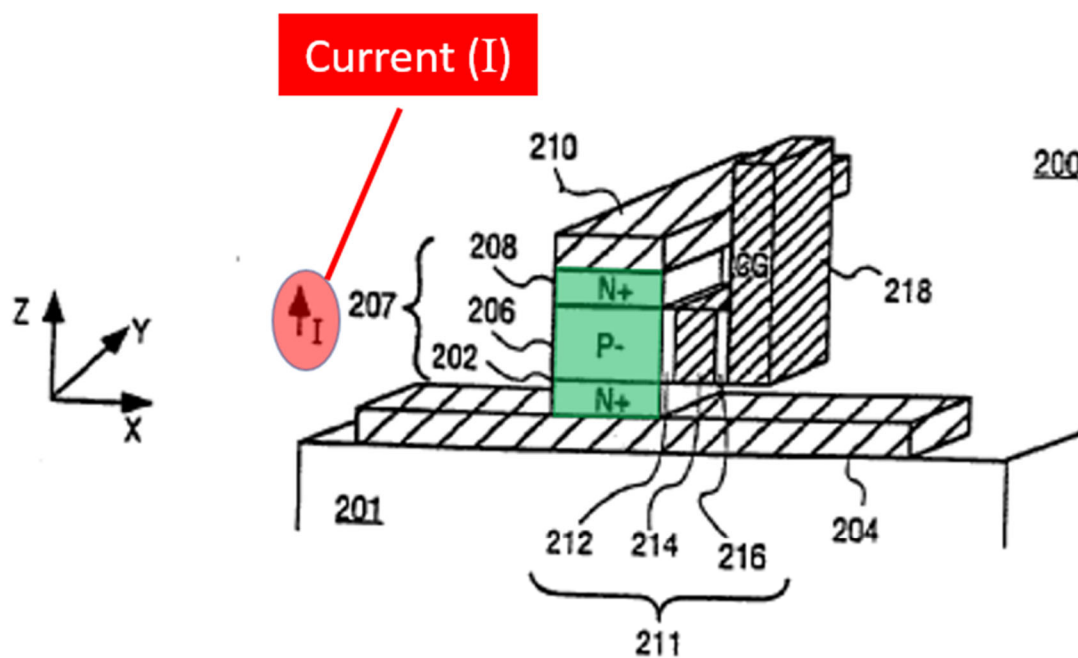


FIG. 2

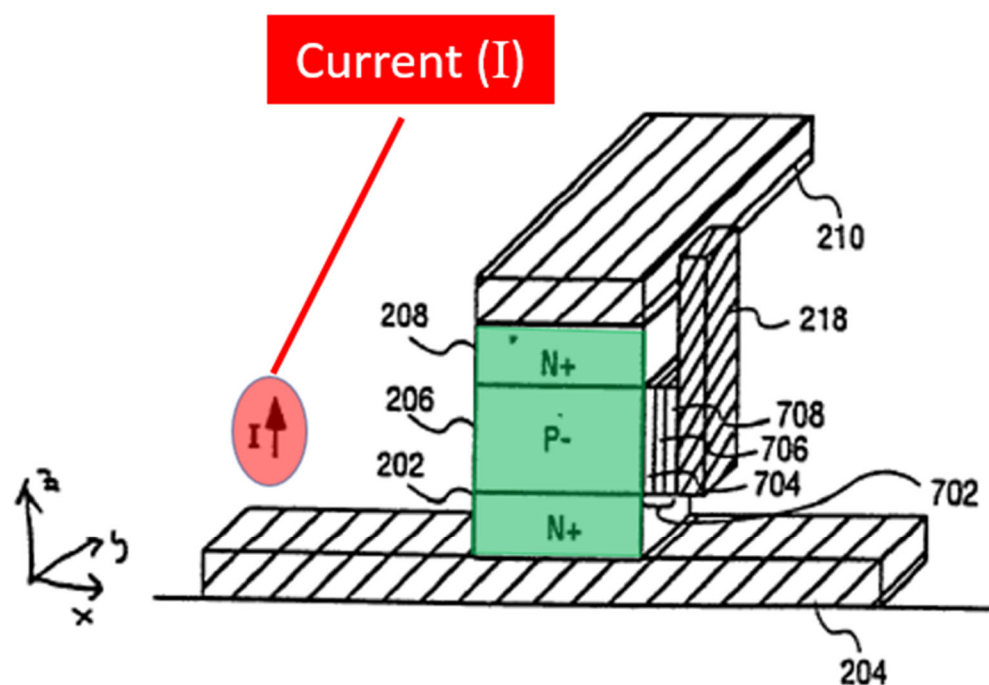


FIG. 7

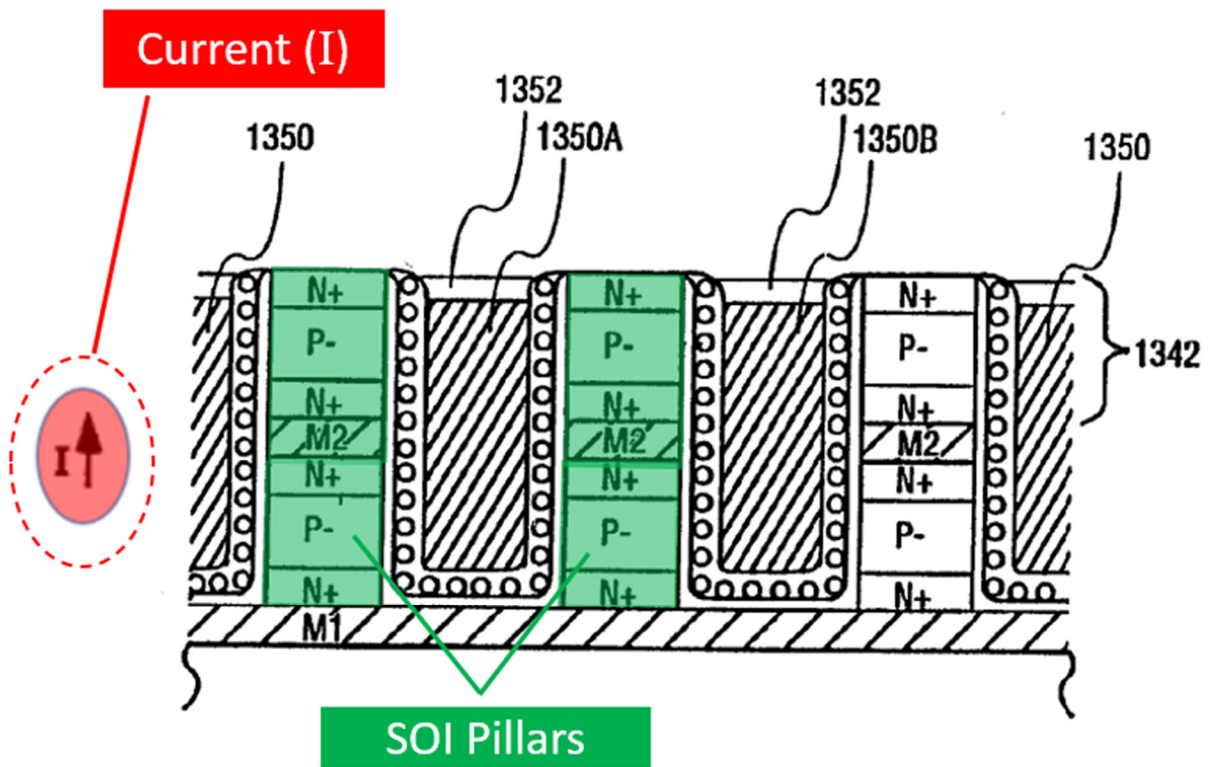


FIG. 25A

As shown in the annotated Figures 1A, 2, 7, and 25A, each depicts a memory cell with a transistor in which the source, channel, and drain (green in each figure) are arranged perpendicular to the substrate. *Id.*, ¶¶24, 26, 119, 135, 122–124 (Fig. 1A with drain (106), channel (104), source (102) stacked vertically and perpendicularly to the substrate), 126 (Figures 2 and 7 each with drain 208, channel 206, and source 202 stacked vertically and perpendicularly to the substrate), 165 (Figure 25A pillar 1342 with N+/P-/N+ stack as in Figure 2, i.e., drain/channel/source). In all four figures, current (I) (red) runs vertically through the

transistor and perpendicular to the substrate. *Id.*, Figs. 1A, 2, 7, 25A, ¶¶119, 124, 131; Sechen, ¶¶125-126.

Figure 1B is reproduced below:

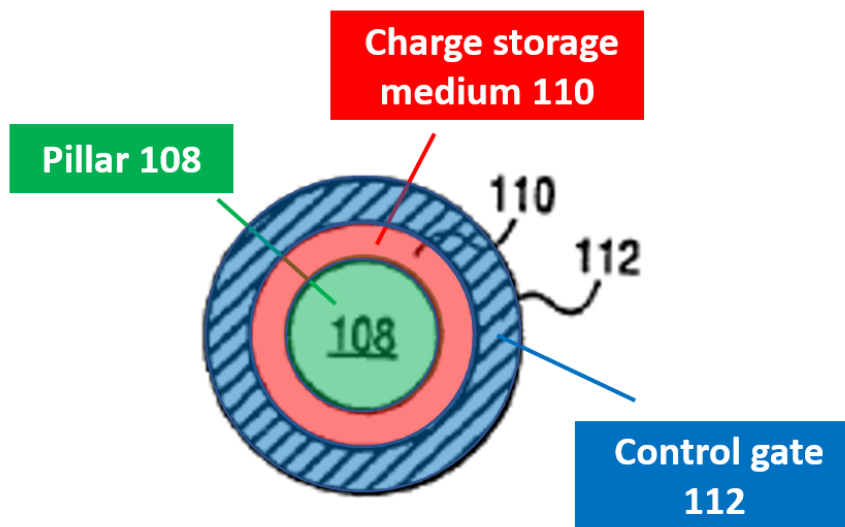


FIG. 1B

Figure 1B shows a variation of Figure 1A's structure, where "pillar 108 is surrounded by a single charge storage member 110 and a single control gate 112." EX1007, ¶125. A POSITA would have understood Figure 1B shows a top view of an implementation of Figure 1A, and that in vertical cross-section, Figure 1B's pillar 108 would have the same drain (106), channel (104), source (102) as shown in Figure 1A, stacked vertically and perpendicularly to the substrate. Sechen, ¶¶127-128.

The '702 Patent states: "The term 'vertical,' as used herein, means substantially perpendicular to a major surface of a substrate, such as, for example, a

semiconductor wafer.” ’702Pat., 4:6–8. Because each of Lee’s Figure 1A–1B, 2, 7, and 25A teach a memory cell with a transistor in which the source, drain, and channel regions are arranged perpendicular to the substrate (as shown in green with the current flow in red in the annotated figures above), these figures each teach “vertically-oriented memory cells.” Sechen, ¶129. These memory cells are “vertically-oriented” in the same way as the memory cells of the ’702 Patent’s Figures 23 and 25. *Id.*; ’702Pat., 9:24–50.

A POSITA would have been motivated to use any of Lee’s memory cell structures in Figures 1A–1B, 2, 7, or 25A as the memory cells in Figure 35’s bottom level 3104, with multiples of each such cell included in that level. EX1007, ¶111; Sechen, ¶¶130-134. Specifically, Lee states that “[i]n the preferred embodiments of the present invention *described in detail below*, the charge storage devices are formed in various configurations, such as a pillar TFT EEPROM ... and various other configurations”; Figures 1A–1B, 2, 7, and 25A are then described in detail. EX1007, ¶¶113 (emphasis added), 118–169. From this express disclosure in Lee, a POSITA would have understood the memory cells shown in Figures 1A–1B, 2, 7, or 25A of Lee are “type[s] of semiconductor devices which store charge” as Lee describes its array’s memory cells, and so would have been motivated to use them in the array of Figure 35. *Id.*, ¶¶113, 123, 125, 127, 138, 166; Sechen, ¶130. In these

combinations, Lee's level 3104 with such memory cells would be "stackable." EX1007, ¶¶24, 108–109, 122, 124; Sechen, ¶131.

In addition, a POSITA would have been motivated to use the memory cell of any of Figures 1A–1B, 2, 7, or 25A with Figure 35 because using one versus another would have amounted to nothing more than simple substitution of a known memory cell, as contemplated by Lee's teachings. EX1007, ¶¶113, 114, 117; Sechen, ¶132. A POSITA would have further recognized using the memory cells in each of Figures 1A–1B, 2, 7, or 25A in Figure 35's level 3104 would allow for each memory cell to consume less lateral surface area (because of the vertical orientation of the transistor in each), furthering Lee's stated goal of increasing density of memory devices. EX1007, ¶¶17, 106–107, 110, 113; Sechen, ¶132.

Lee expressly provides a motivation for the proposed combinations when Lee explains that "by creating a memory device with a 'vertical' read current path, the pillar memory cell of the present invention can be easily stacked in a three dimensional array with source/drain conductors 103 and 116 running parallel or perpendicular to each other and parallel to the plane of the substrate 101 without requiring the use of vertical interconnect strategies for the source and drain connection." EX1007, ¶124. Although this disclosure expressly pertains to Figure 1A, it is equally applicable to Figures 1B, 2, 7, or 25A with predictable results. *Id.*, ¶¶119, 131; Sechen, ¶133.

Further, a POSITA would have had a reasonable expectation of success in making this combination because Lee expressly contemplates using the memory devices of Figures 1A–1B, 2, 7, or 25A in the array of Figure 35 and doing so would have obtained predictable results. EX1007, ¶¶113–114; Sechen, ¶134.

d. 13[c]

If PO argues “the stackable add-on layer being bonded” encompasses any type of layer that is directly or indirectly adhered to the “dielectric layer,” Lee discloses or suggests 13[c].¹¹ As discussed in Section VII.A.1.c, bottom level 3104 (as shown in Figure 35 and reproduced below) teaches a “stackable add-on layer,” and under PO’s apparent construction, that layer is adhered to insulating layer 3102 (“the dielectric layer”). Sechen, ¶¶135-137.

¹¹ 13[c] should not be construed this broadly. Grounds 1C and 1E further discuss how 13[c] is taught by the prior art under the proper construction.

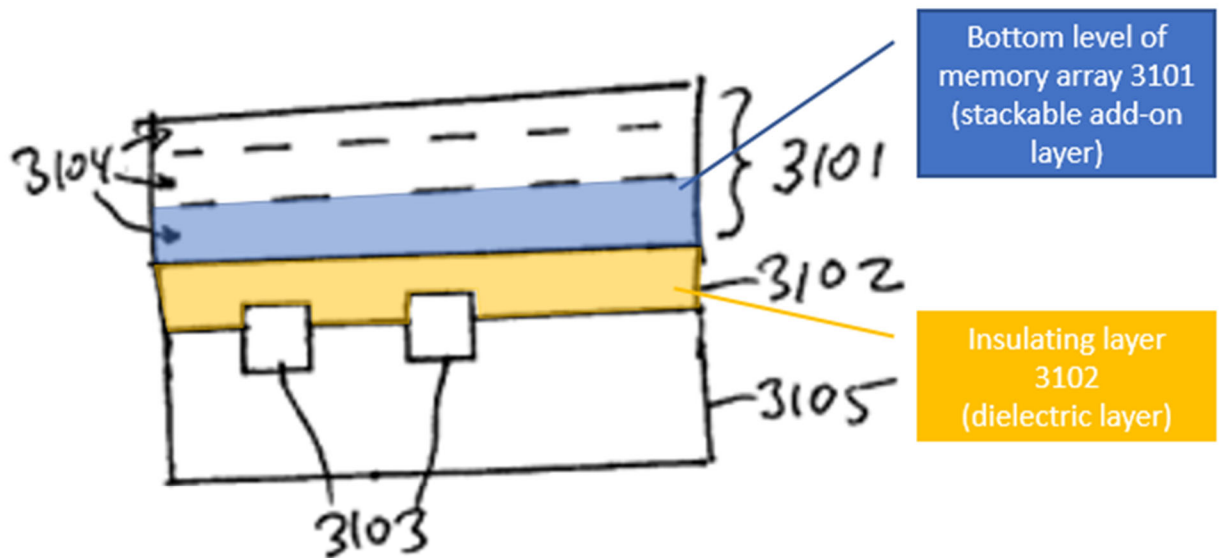


FIGURE 35

e. 13[d]

Lee discloses or suggests 13[d]. Sechen, ¶¶138-139. Section VII.A.1.c explains Figures 1A–1B, 2, 7, and 25A each disclose a memory cell with a transistor and a POSITA would have been motivated to include any of those memory cells as the memory cells of level 3104 in Figure 35. For those same reasons, Lee teaches “the memory cells...having at least one transistor.”

Each of Figures 1A–1B, 2, 7, and 25A also teach a nonvolatile memory cell. EX1007, ¶¶6 (“electrically erasable *nonvolatile* memories such as...EEPROMs”) (emphasis added), 113 (“pillar TFT EEPROM” “described in detail below”). Lee specifically describes Figure 1A as “a three terminal *nonvolatile* stackable pillar memory device,” and Figure 1B as a Figure 1A modification. EX1007, ¶¶122, 125

(emphasis added). Although the text associated with Figures 2, 7, and 25A does not explicitly refer to those structures as “nonvolatile,” a POSITA would have understood them to be nonvolatile because the structures of those figures ensure that stored information is retained even when power is removed (each is designed to store charge as described in Section VII.A.1.c). Sechen, ¶139.

2. Claim 14

If PO argues “SOI pillar” encompasses any pillar-shaped structure with insulating material below it, Lee discloses or suggests claim 14’s additional limitations. Sechen, ¶¶140-145

Section VII.A.1.c describes how Lee’s Figure 2 (below) depicts a “vertical transistor” (channel 206 stacked above source 202 and below drain 208 and direction of current flow I).

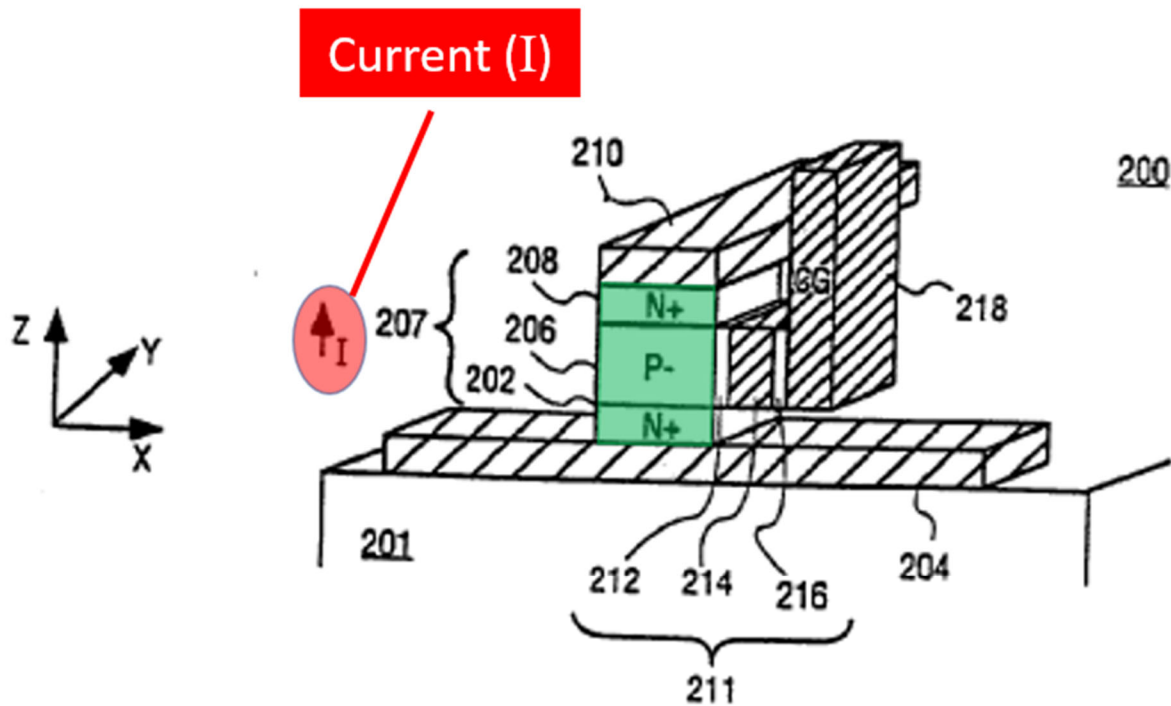


FIG. 2

The vertical transistor in Lee's Figure 2 also has "a floating gate and a control gate": floating gate 214 and control gate 218. *Id.*, ¶¶126–127. That floating gate and control gate are on pillar 207 ("on a SOI pillar" under PO's apparent construction). More specifically, Figure 2 shows "a charge storage medium 211 comprising a tunnel dielectric 212, a floating gate 214, and a control gate dielectric 216." EX1007, ¶127. Lee explains that tunnel dielectric 212 "is formed adjacent to and in direct contact with P type silicon body 206 [of pillar 207]," "floating gate 214 is formed adjacent to and in direct contact with tunnel dielectric 212," "control gate dielectric 216 is formed adjacent to and in direct contact with floating gate 214," and "control

gate 218 is formed adjacent to and in direct contact with control gate dielectric 216.” *Id.*, ¶¶126–127. Therefore, Lee’s Figure 2 teaches floating gate 214 and control gate 218 “on” pillar 207 in the same way that floating gate 123k and control gate 123 are “on” SOI pillar 124 in ’702 Patent Figure 23. ’702Pat., 9:24–35; Sechen, ¶¶142-144. As discussed in Section VII.A.1.d, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (Figure 2 pillars) have insulating material below them (insulating layer 3102). In addition, pillar 207 and conductive input/output 204 can be formed of silicon. EX1007, ¶126.

Accordingly, the combination of Lee’s Figure 35 with Figure 2 renders claim 14 obvious.

3. Claim 15

If PO argues “SOI pillar” encompasses any pillar-shaped structure with insulating material below it, Lee discloses or suggests claim 15’s additional limitations. Sechen, ¶¶146-152.

Section VII.A.1.c describes how Lee’s Figures 1A–1B and 7 (below) depict a “vertical transistor” (channel stacked above source and below drain and direction of current flow I).

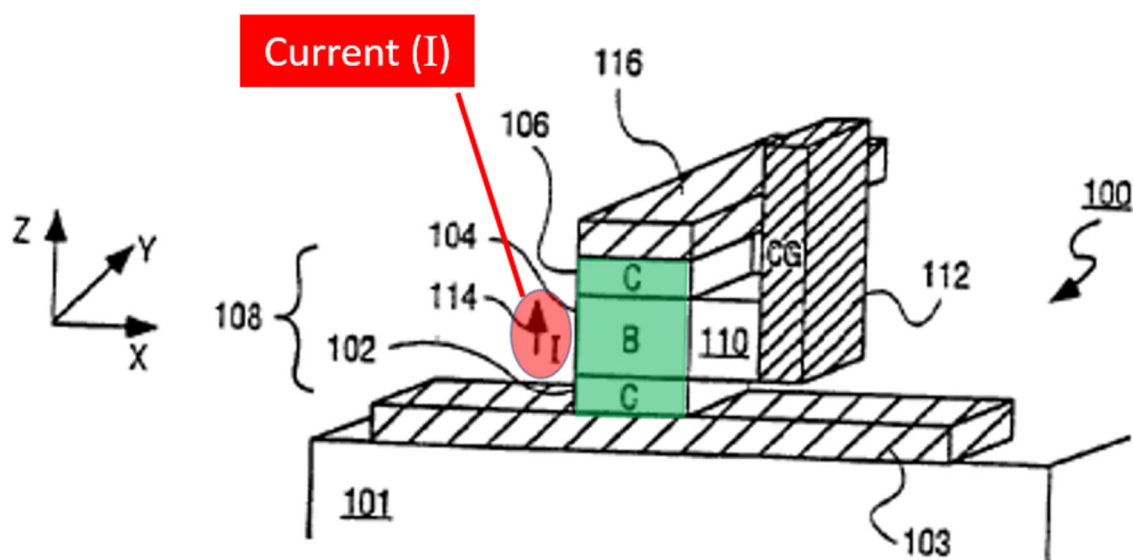


FIG. 1A

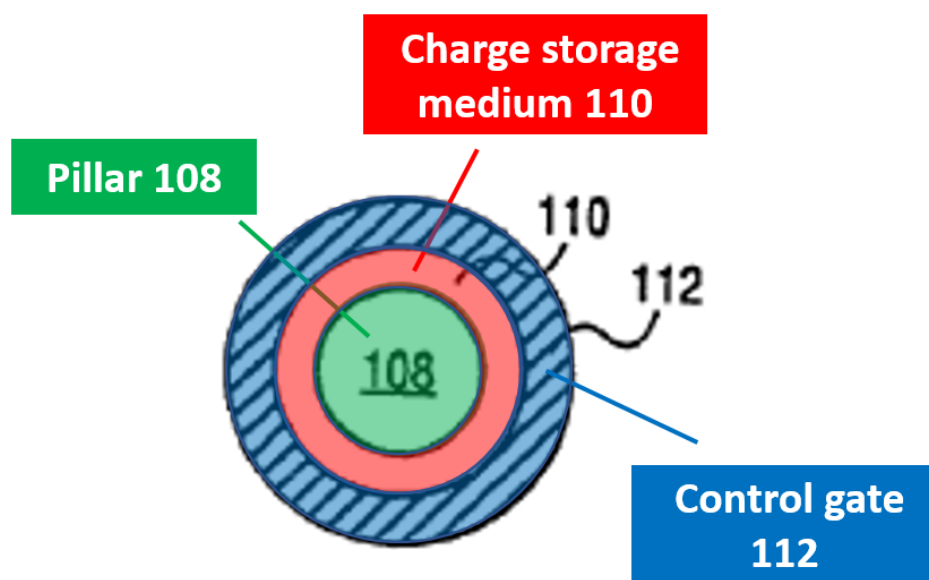


FIG. 1B

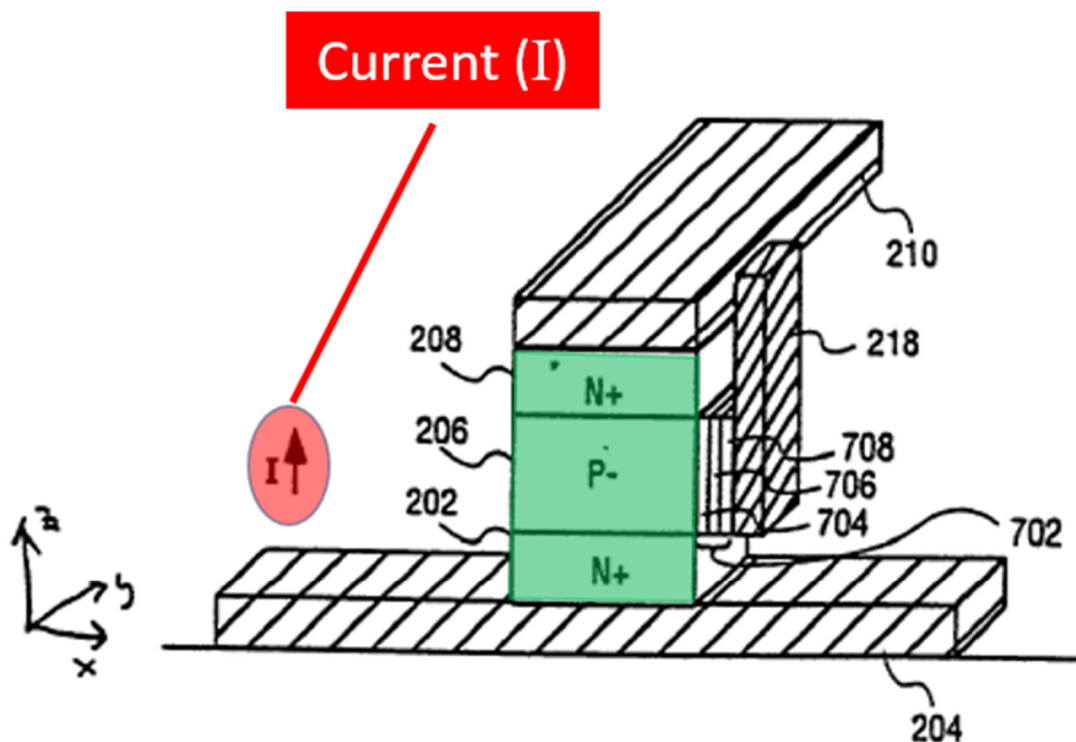


FIG. 7

In each of Figures 1A–1B, and 7, the vertical transistor has “a charge-trapping gate insulator and a gate.” In Lee’s Figure 1A and 1B, drain (106), channel (104), and source (102) stacked vertically and perpendicularly to the substrate (“vertical transistor”) has charge storage medium 110 (“charge-trapping gate insulator”) and control gate 112 (“gate”). EX1007, ¶¶119, 122–125. In Lee’s Figure 7, channel 206 stacked above source 202 and below drain 208 (“vertical transistor”) has dielectric stack 702 (“charge-trapping gate insulator”) and control gate 218 (“gate”). *Id.*, ¶138.

In each of Figures 1A–1B and 7, the charge-trapping gate insulator and gate are “on a SOI pillar” under PO’s apparent construction. In Lee’s Figure 1A, charge

storage medium 110 (“charge-trapping gate insulator”) and control gate 112 (“gate”) are on pillar 108 (“SOI pillar” under PO’s apparent construction). In Figure 1A, “[a]dherent to and in contact with body 104 [of pillar 108] is a charge storage medium 110,” and “a control gate 112 is formed adjacent to and in direct contact with the charge storage medium 110.” *Id.*, ¶¶122, 125. In Lee’s Figure 1B, “the pillar 108 is surrounded by a single charge storage member 110 and a single control gate 112.” *Id.*, ¶125, Fig. 1B. In Lee’s Figure 7, “the charge storage medium can be a dielectric stack 702 comprising a first oxide layer 704 adjacent to the silicon body or channel [206 of the pillar], a nitride layer 706 adjacent to the first oxide layer and a second oxide layer 708 adjacent to the nitride layer and adjacent to the control gate 218.” *Id.*, ¶138; Sechen, ¶¶149-150. Each of Lee’s Figures 1A–1B, and 7 teaches charge storage medium and control gate “on” the pillar in the same way that charge-trapping gate insulating layer 183g and gate 123 are “on” SOI pillar 124 in ’702 Patent Figure 25. ’702Pat., 9:26, 36–50; EX1001007, ¶138; Sechen, ¶150.

As discussed in Section VII.A.1.d, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (pillars of Figures 1A–1B, and 7) have insulating material below them (insulating layer 3102). In addition, in Figures 1A–1B and 7, the pillar and conductive input/outputs can be formed of silicon. EX1007, ¶¶119, 126.

Accordingly, the combination of Lee's Figure 35 with Figure 1A, 1B, or 7 renders claim 15 obvious.

4. Claim 16

If PO argues "SOI pillar" encompasses any pillar-shaped structure with insulating material below it, Lee discloses or suggests claim 16's additional limitations. Sechen, ¶¶153-162.

Lee's Figure 25A, showing a pillar memory structure, is below:

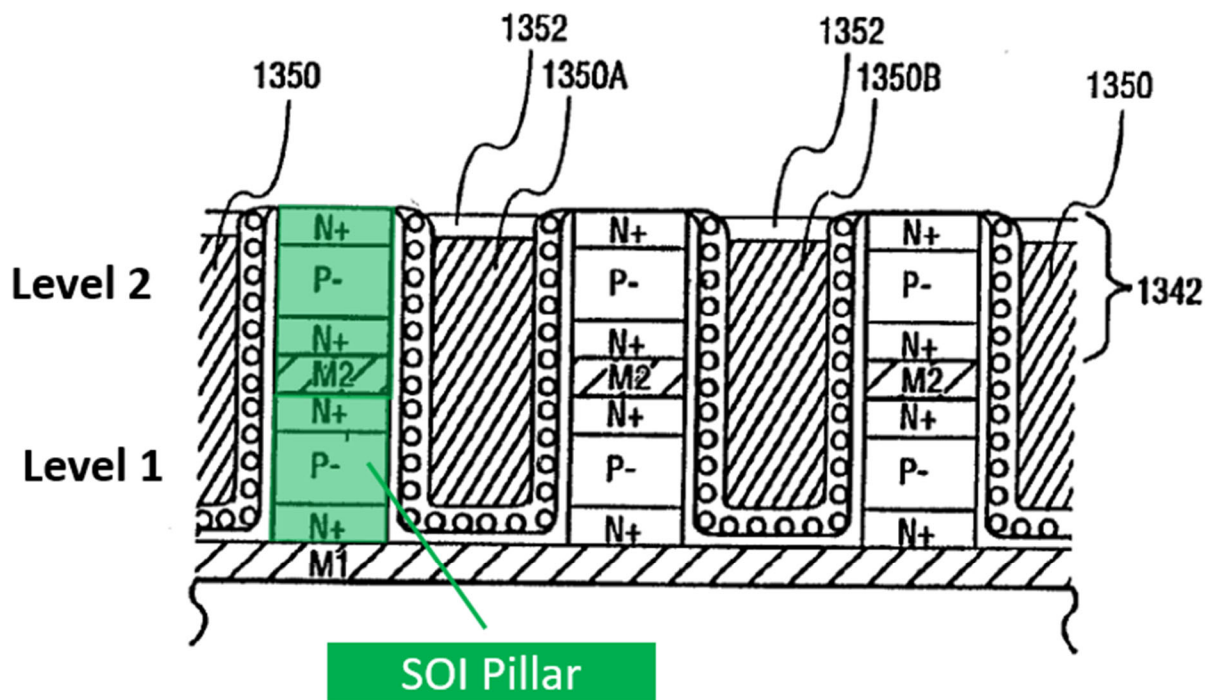


FIG. 25A

Figure 25A shows (1) two nonvolatile memory cells¹² which are (2) vertically oriented, (3) serially connected together, and (4) formed with a first SOI pillar.

First, Figure 25A discloses “two nonvolatile memory cells” (green) because, similar to Lee’s Figures 2 and 7 above (Section VII.A.1.e), the memory cell structures shown in Figure 25A, i.e., floating gate, control gate dielectric, and control gate, ensure that stored information is retained even when power is removed. *See* EX1007, ¶¶6, 113, 147–148, 154–155, 163–167; Sechen, ¶¶155-157.

Second, the two memory cells in Figure 25A are “vertically oriented” for the same reasons explained in Section VII.A.1.c (source, channel, drain are arranged perpendicular to the substrate, such that current flows perpendicular to the substrate). *See, e.g., id.*, ¶¶148, 158, 165 (Figure 25A pillar 1342 comprises an N+/P-/N+ stack as in Figure 2, i.e., drain/channel/source); Sechen, ¶158.

Third, Figure 25A’s two memory cells are “serially connected together” because the two memory cells (green) are separated from one another only by conductor layer M2 and thus are electrically connected to one another with the source of the top memory cell connected to the drain of the bottom cell, and

¹² Lee discloses an iterative process for fully fabricating the memory devices of Figure 25A. EX1007, Figs. 13–28, ¶¶147–170; Sechen, ¶¶155, 103-110.

therefore, the two memory cells are serially connected. *Id.*, Fig. 23A, ¶¶119, 161; Sechen, ¶159.

Fourth, Figure 25A's two memory cells are "formed with a first SOI pillar," under PO's apparent construction. Lee's Figure 25A teaches two memory cells "formed with a first SOI pillar" in the same way that the two memory cells in '702 Patent Figure 27 are "formed with" SOI pillar 124. '702Pat., 9:51–58; Sechen, ¶160. As discussed in Section VII.A.1.d, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (Figure 25A pillars) have insulating material below them (insulating layer 3102). In addition, in Figure 25A, the pillars and conductive input/outputs can be formed of silicon. EX1007, ¶¶119, 126, 147–148.

Accordingly, the combination of Lee's Figure 35 with Figure 25A renders claim 16 obvious.

5. Claim 17

If PO argues "SOI pillar" encompasses any pillar-shaped structure with insulating material below it, Lee discloses or suggests claim 17's additional limitations. Sechen, ¶¶163-168. Section VII.A.4 explains Lee's Figure 25A discloses or suggests "the at least two nonvolatile memory cells on the first SOI pillar." Figure 25A further shows that those memory cells are serially connected to a conductive bitline or wordline M1 1308 ("interconnect line") and M1 connects the

first pillar to an adjacent pillar having a nonvolatile memory cell. EX1007, ¶¶148, 161, Fig. 25A; Sechen, ¶164. In the combination with Lee's Figure 35, that interconnect line would similarly be disposed on interlayer insulating layer 3102 ("dielectric layer"). *Id.*

The memory cell in the adjacent pillar in Figure 25A is nonvolatile because it has the same structure as the "two nonvolatile memory cells" discussed in Section VII.A.4 for claim 16 and thus ensures that stored information is retained even when power is removed. *See* EX1007, ¶¶6, 113, 147–148, 154–155, 163–167; Sechen, ¶165.

Lee's Figure 25A teaches a memory cell "formed with a second SOI pillar" in the same way that two memory cells in '702 Patent Figure 27 are "formed with" SOI pillar 124. '702Pat., 9:51–58; Sechen, ¶167. As discussed in Section VII.A.4, the stackable add-on layer is bottom level 3104 in Figure 35, and thus pillars formed in it (Figure 25A pillars) have insulating material below them (insulating layer 3102). In addition, in Figure 25A, the pillar and conductive input/outputs can be formed of silicon. EX1007, ¶¶119, 126, 147–148.

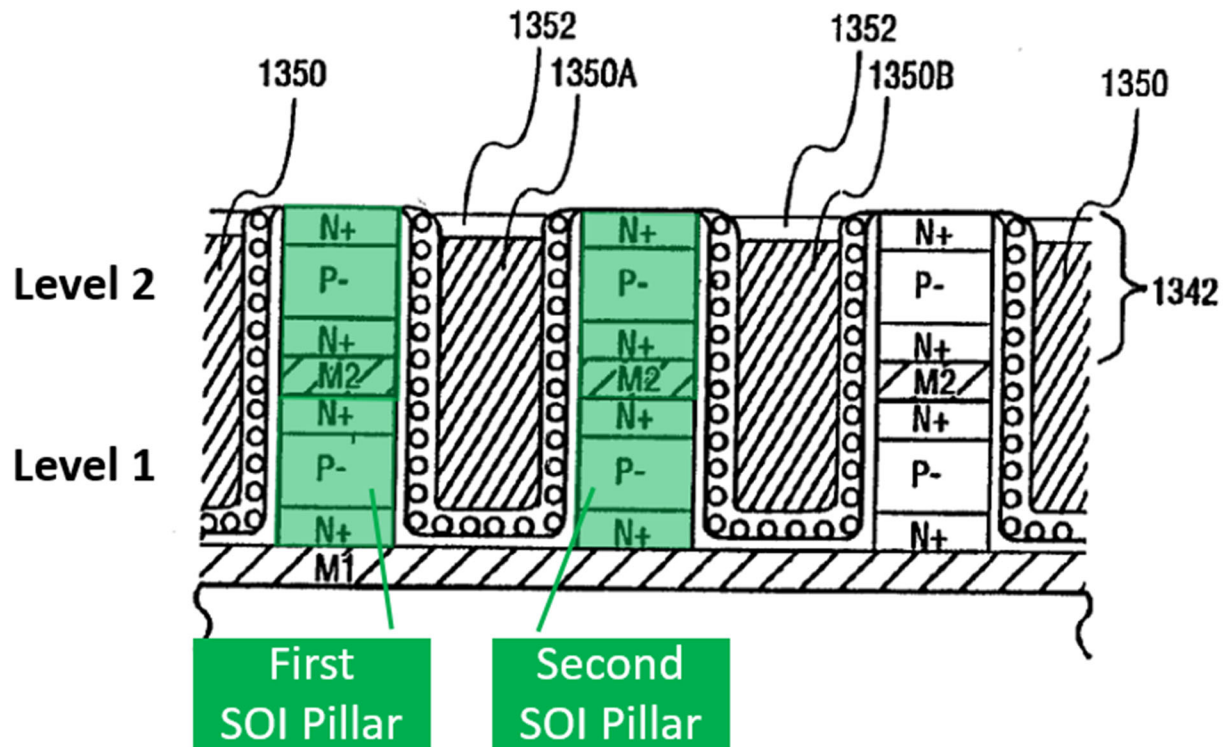


FIG. 25A

Thus, Lee discloses the “first SOI pillar” serially connected by M1 (i.e., “interconnect line”), to a nonvolatile memory cell within the “second SOI pillar.” Sechen, ¶166.

For these reasons, the combination of Lee’s Figure 35 with Figure 25A renders claim 17 obvious.

B. Ground 1B: Obviousness over Lee and Endoh (Claims 16-17)

As discussed in Section VII.A, Lee teaches claim 13’s limitations under PO’s apparent interpretation of “stackable add-on layer being bonded.” Lee and Endoh

teach claims 16 and 17's additional limitations under PO's apparent interpretation of "SOI pillar."

1. Claim 16

Lee in combination with Endoh teaches claim 16's additional limitations. Sechen, ¶¶170-181. Endoh describes "a semiconductor memory provided with a memory transistor having a charge storage layer and a control gate, and its production process." EX1012, ¶3.¹³ Endoh's Figures 1–11 "are plan views illustrating various memory cell arrays of EEPROMs [electrically erasable programmable read-only memories] having floating gates as charge storage layers in semiconductor memory devices in accordance with the present invention." *Id.*, ¶153. Endoh's Figures 132–1650 "are sectional views (taken on line A-A' and line B-B' in FIG. 1, FIG. 5, FIG. 10 or FIG. 13) illustrating various production steps for producing semiconductor memory devices in accordance with the present invention." EX1012, ¶165. Specifically, for Endoh's "Production Example 52," Figures 1171 and 1172 "are sectional views taken on line A-A' and line B-B', respectively, in FIG. 1 which illustrates a memory cell array of an EEPROM." *Id.*, ¶1206. A POSITA would have understood that EEPROM memory cells are non-volatile memory cells. Sechen, ¶171 (citing EX1025–1027; EX1007, ¶6).

¹³ For convenience, Endoh is also excerpted at EX1031.

Figure 1 of Endoh is reproduced below (annotated):

Fig. 1

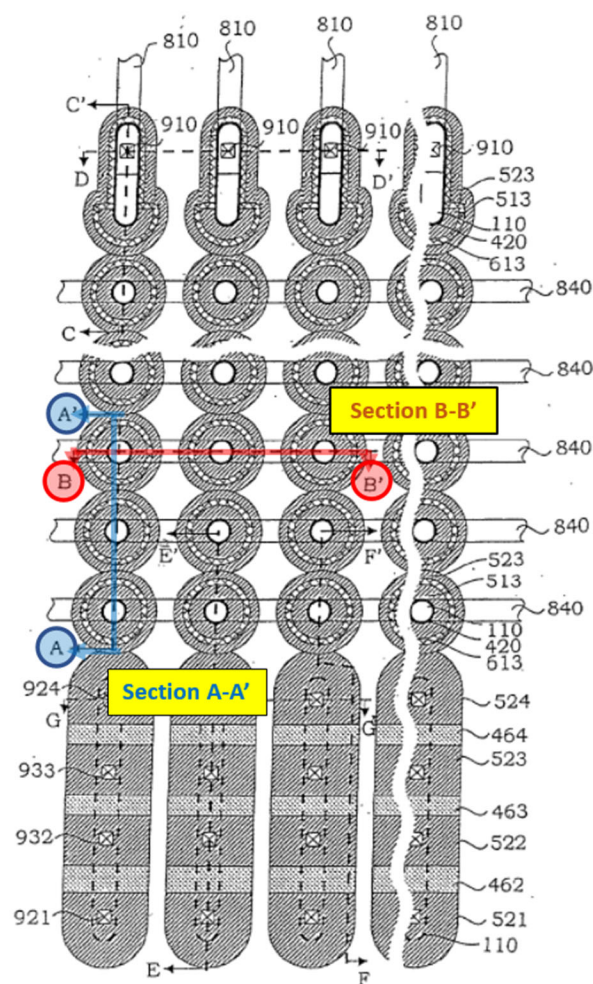


Figure 1171 shows A-A' cross-section, and Figure 1172 shows B-B' cross-section (both annotated):

Fig. 1171

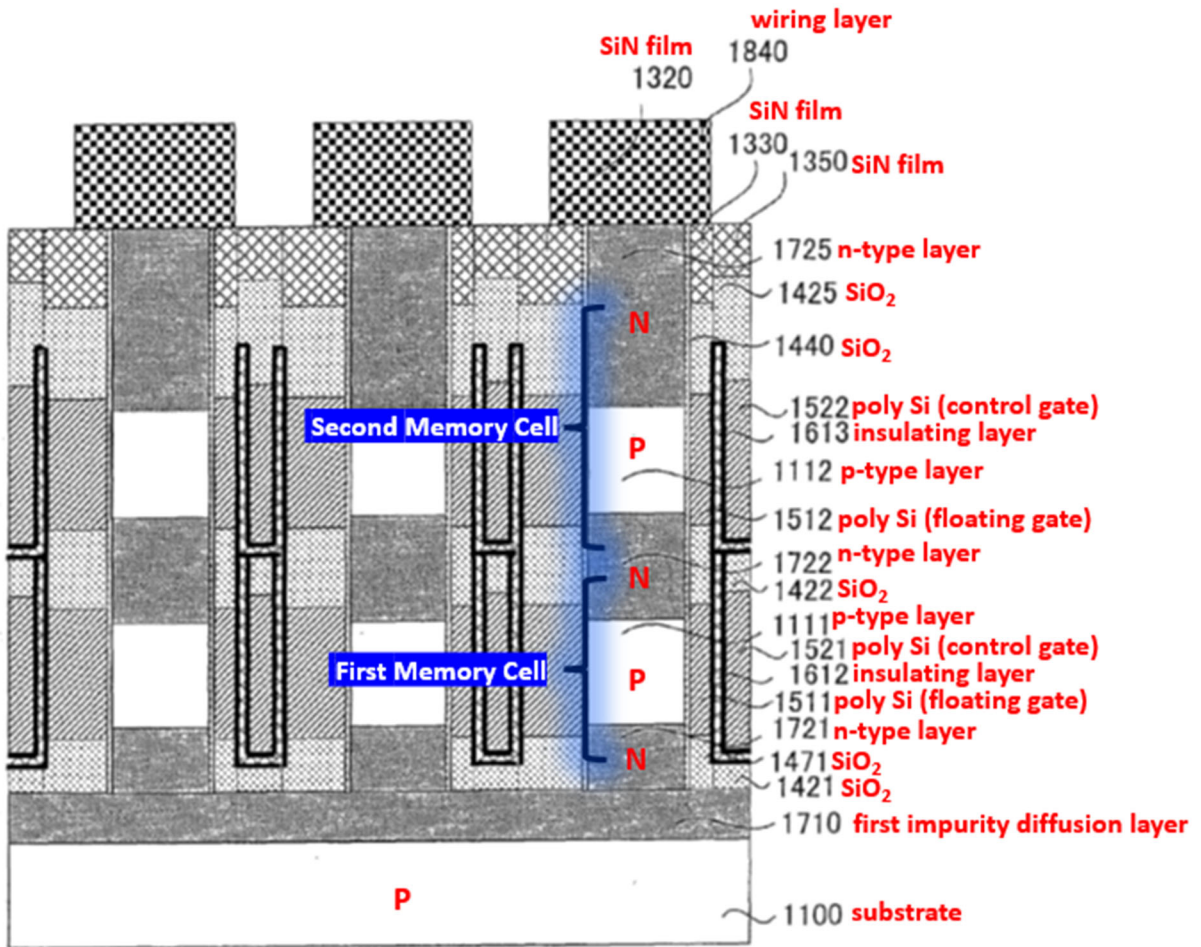
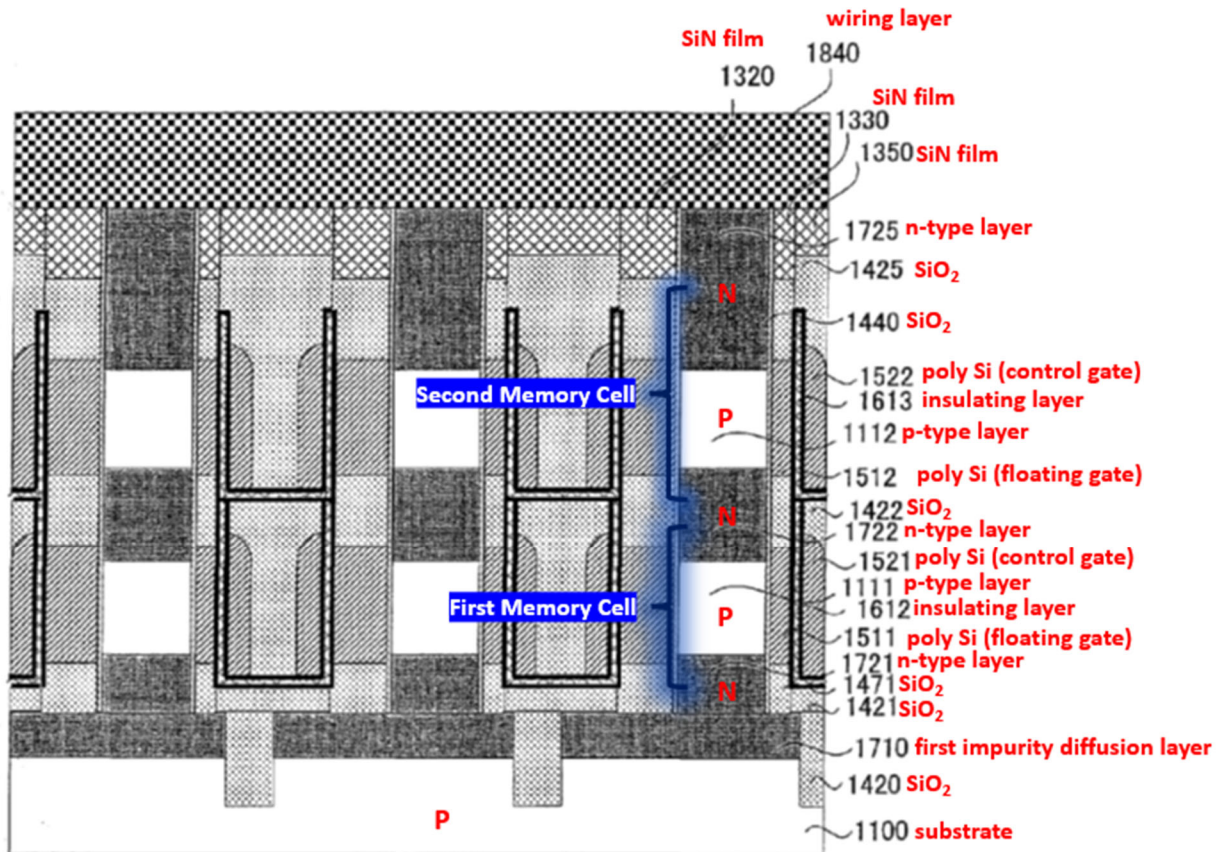


Fig. 1172



EX1012, ¶¶1206–07. Endoh explains that in these figures, “island-like semiconductor layers are formed in the form of pillars,” “two memory cells are arranged on each island-like semiconductor layer,” “two memory transistors are arranged on the island-like semiconductor layer,” and “the transistors are connected in series along the island-like semiconductor layer.” *Id.* This configuration is shown in annotated Figures 1171 and 1172 above (n-type layer 1725, p-type layer 1112, n-type layer 1722, p-type layer 1111, and n-type layer 1721, all in the same pillar, form two transistors for two memory cells). *Id.*, ¶¶1206–07 (“[i]n this example,

production step[s] are the same as Production Example 45” with limited exceptions), 1050–81 (describing Production Example 45, with ¶1074 identifying the p-type and n-type semiconductor layers used in the two transistors with the same reference numbers in Figures 1171 and 1172); Sechen, ¶173.

First, for “at least two nonvolatile memory cells are vertically oriented,” Endoh’s Production Example 52 teaches two EEPROM memory cells (“at least two nonvolatile memory cells”), each with transistors in which the source, channel, and drain (layers 1721, 1111, 1722 and 1722, 1112, and 1725 for each memory cell respectively) are arranged perpendicular to substrate 1100 (each of those memory cells “are vertically oriented”). EX1012, ¶¶1050–81, 1206–07, Figs. 1171–72; Sechen, ¶174 (citing EX1007, ¶6). As with ’702 Patent Figure 27, a POSITA would have understood that current flows through the source, channel, and drain of the two memory cells perpendicular to the base substrate. EX1012, ¶¶1205–07, Figs. 1171–72; Sechen, ¶174.

Second, Endoh’s “at least two nonvolatile memory cells” are “serially connected together.” In Endoh’s Production Example 52, “transistors [of the two EEPROM memory cells] are connected in series along the island-like semiconductor layer, as shown in FIG. 1171 and FIG. 1172.” *Id.*; Sechen, ¶175.

Third, Endoh’s “at least two nonvolatile memory cells” are “formed with a first SOI pillar,” under PO’s apparent construction, because the transistors of the two

EEPROM memory cells “are arranged on the island-like semiconductor layer” (“formed with a first SOI pillar”). *Id.*; Sechen, ¶176 (citing ’702Pat., Fig. 27). As discussed in Section VII.A.1.c, the stackable add-on layer is bottom level 3104 in Lee Figure 35, and thus pillars formed in it (the pillars of the Lee-Endoh combination as discussed below) have insulating material below them (insulating layer 3102). In addition, the pillars and conductors can be formed of silicon. EX1007, ¶¶119, 126, 147–148; EX1012, ¶1206.

A POSITA would have been motivated to modify Lee’s device level 3104 in array 3101 to incorporate two memory cells on each pillar as taught in Endoh. Sechen, ¶177. Notably, both Lee and Endoh teach cylindrical pillar nonvolatile memory structures. *Compare* EX1007, Fig. 1B, *with* EX1012, Fig. 1. In addition, Lee itself teaches a nonvolatile memory structure with two memory cells on each pillar (Section VII.A.4 (discussing Fig. 25A)), providing motivation to incorporate two memory cells on each pillar. A POSITA would have recognized that applying two memory cells in each pillar as taught in Endoh to Lee’s level 3104 would further Lee’s stated goals of increasing device density. EX1007, ¶¶106–107; Sechen, ¶178. This combination merely amounts to using a known technique (implementing serial memory cells in a pillar as taught by Endoh) to improve a similar known device (Lee’s memory array 3101) in the same way (serial memory cells in the same pillar to increase density). Sechen, ¶179. In addition, the combination would have

amounted to applying a known technique (two memory cells on each pillar) to address the same known problem recognized by both Lee and Endoh (fabricating memory arrays using pillar structures) using prior art elements according to their established functions (pillar structures with two memory cells per pillar in Lee’s Figure 35 structure). *Id.*; see *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); see also *KSR Int’l v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

Further, a POSITA would have had a reasonable expectation of success because both Lee and Endoh disclose embodiments with two memory cells per pillar showing that such structures were within the skill of a POSITA. Sechen, ¶180 (citing EX1007, Fig. 25A; EX1012, Figs. 1171–1172).

2. Claim 17

As discussed in Section VII.B.1, Lee and Endoh render claim 16 obvious under PO’s apparent constructions. Lee and Endoh also teach claim 17’s additional limitations under those constructions. Sechen, ¶¶182-186.

Section VII.B.1 explains Endoh’s Figures 1171–72 teach two EEPROM memory cells arranged on each island-like (pillar-shaped) semiconductor layer (“the at least two nonvolatile memory cells on the first SOI pillar” and “a nonvolatile memory cell formed with a second SOI pillar”). EX1012, ¶¶1206–07. As shown in annotated Figures 1171–72 (above), the nonvolatile memory cells in each pillar are serially connected to wiring layer 1840 (“interconnect line”) disposed on silicon

nitride films 1320, 1330 and 1350 (“dielectric layer”). EX1012, Figures 1171–72, ¶¶1206–07 (stating that “[i]n this example, production step[s] are the same as Production Example 45” with limited exceptions), ¶¶1050–81 (describing Production Example 45, with ¶1076 identifying wiring layer 1840 connected to n-type layer 1725 and ¶¶1056, 1069 identifying silicon nitride films 1320, 1330 and 1350 as insulating films). Therefore, Endoh’s two EEPROM memory cells arranged on one pillar-shaped semiconductor layer (“the at least two nonvolatile memory cells on the first SOI pillar”) are serially connected with wiring layer 1840 (“interconnect line”) disposed on silicon nitride films 1320, 1330 and 1350 (“dielectric layer”) to an EEPROM memory cell arranged on another pillar-shaped semiconductor layer (“a nonvolatile memory cell formed with a second SOI pillar”). Sechen, ¶¶183-184. As discussed in Section VII.A.1.c, the stackable add-on layer is bottom level 3104 in Lee Figure 35, and thus pillars formed in it (the pillars of the Lee-Endoh combination as discussed below) have insulating material below them (insulating layer 3102). In addition, in both Lee and Endoh, the pillars and conductors can be formed of silicon. EX1007, ¶¶119, 126, 147–148; EX1012, ¶1206.

The modification to Lee based on Endoh’s teachings, reasoning for that modification, and reasonable expectation of success analyses for claim 16 (Section VII.B.1) apply equally to claim 17. *Id.* In addition, in the combination, Lee’s Figure 1A and 1B pillars are serially connected to conductive layer 103 (“serially connected

with an interconnect line”) which in the combination with Lee’s Figure 35 is disposed on insulating layer 3102 (“disposed on a dielectric layer”). Sechen ¶185 (citing EX1007, Figs. 1A–1B, 35, ¶¶111, 122, 125). Lee’s teachings thus support that a POSITA would have been motivated to modify Lee to include two memory cells per pillar as taught in Endoh, and in this modification, those two memory cells would be serially connected with an interconnect line disposed on a dielectric layer to a memory cell of another pillar. *Id.* Lee’s and Endoh’s teachings also support a reasonable expectation of success for the modification because they show this configuration was within the skill of a POSITA. *Id.*

C. Ground 1C: Obviousness over Lee and Kim (Claims 13–17)

As discussed in Section VI.A, a POSITA would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the stackable add-on layer is wafer bonded to the dielectric. Under the proper construction of “the stackable add-on layer being bonded” for claim 13 and PO’s apparent construction of “SOI pillar” for claims 14–17, claims 13–17 would have been obvious over Lee and Kim for the reasons discussed below.

1. Claim 13

a. 13[pre]-13[b]

For the same reasons discussed in Sections VII.A.1.a–VII.A.1.c, Lee discloses or suggests 13[pre]–13[b].

b. 13[c]

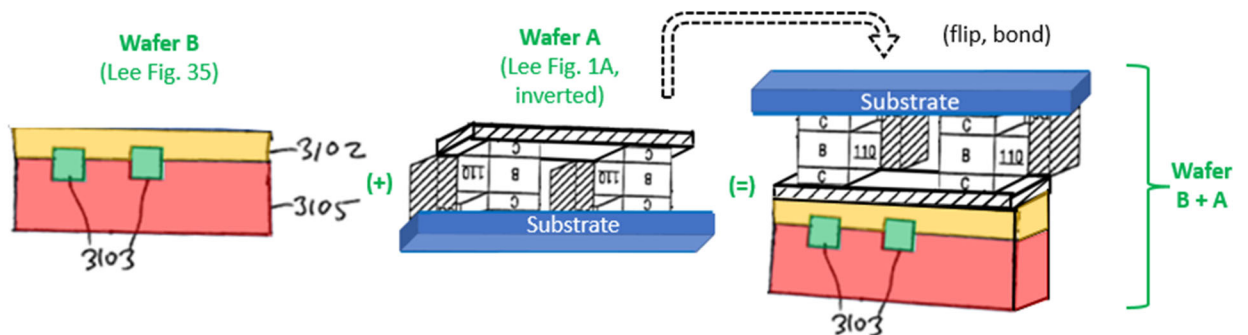
Under the proper construction of “the stackable add-on layer being bonded” as requiring wafer bonding (Section VI.A), the combination of Lee and Kim teaches 13[c]. Sechen, ¶¶189-197.

Kim describes bonding active device wafers together using a dielectric layer to form “a three-dimensional (3-D) wafer-to-wafer vertical stack.” EX1008, ¶¶19–20, Fig. 1. Kim’s invention “is applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, ... CMOS devices, MOSFETs, and new memory devices.” *Id.*, ¶19. Kim also discloses that its 3D vertical wafer stack may comprise “any number” of wafers, and provides an example bonding wafer 110 having one or more microprocessors and wafer 120 including one or more memory devices using a dielectric layer 102. *Id.*, ¶20, Fig. 1; *see also id.*, ¶22 (contemplating “logic/memory stacking”).

In Lee, each level 3104 is deposited on the underlying level of array 3101. EX1007, ¶107. Lee does not clearly describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102. *See id.*, ¶¶107–113. Consequently, a POSITA would have looked to other art, such as Kim, for details about attaching bottom level 3104 to insulating layer 3102. This is especially so where a POSITA, at the suggestion of Lee, was looking to separately form a two-dimensional array of memory devices and “package [it] together” with Lee’s substrate 3105 having driver

circuits 3103 formed therein and insulating layer 3102 on top “to form a non-monolithic memory device.” Sechen, ¶¶190-192 (citing EX1007, ¶107). Indeed, Kim contemplates bonding a wafer having CMOS devices, like Lee’s substrate 3105 having CMOS transistors forming driver circuits 3103, with a wafer having memory devices, like Lee’s level 3104. EX1008, ¶¶19–20; EX1007, ¶111. A POSITA therefore would have been motivated to apply Kim’s wafer bonding teachings to implement Lee’s Figure 35 memory device as a non-monolithic one. Sechen, ¶192.

The figures below illustrate one way a POSITA would have found it obvious to apply Kim’s teachings in Lee to wafer bond level 3104 to layer 3102 (a POSITA would have found it obvious to use any of the memory structures in Figures 1A–1B, 2, 7, or 25A in such a process). Section VII.A.1.c; Sechen, ¶193.



Lee’s separately fabricated memory cells (e.g., from Lee’s Figure 1A) would be formed on their own substrate (“Wafer A”). Wafer A would be flipped and bonded to Wafer B having Lee’s driver circuits 3103 (“electrical devices”) and insulating layer 3102 (“dielectric layer”). Sechen, ¶194; EX1008, ¶20. In the

combination, as in Kim Figure 1 with wafer 120 bonded to wafer 110 using dielectric layer 102, Lee's bottom level 3104 ("stackable add-on layer," having, e.g., Lee's Figure 1A memory cells) would be wafer bonded to insulating layer 3102 ("dielectric layer"), resulting in Lee's Figure 35 structure. Sechen, ¶194.

A POSITA would have recognized that using wafer-bonding to bond level 3104 ("stackable add-on layer") to insulating layer 3102 ("dielectric layer") of Lee's Figure 35 would have been a predictable way to non-monolithically build Figure 35's structure. Sechen, ¶195. This modification consists of nothing more than using a known technique (Kim's wafer bonding) to improve a similar known device (the structure in Lee's Figure 35) in the same way (logic/memory stacking using a wafer bonding process). *Id.* In addition, the combination would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Lee and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Lee's memory cell structures in Figures 1A–1B, 2, 7, or 25A in Lee's Figure 35 structure). *Id.*; see *Intel*, 61 F.4th at 1380; *KSR*, 550 U.S. at 417.

A POSITA would have also recognized that wafer-bonding Lee's bottom level 3104 to insulating layer 3102, as compared to monolithic deposition, allows for more efficient quality control with less potential waste. Sechen, ¶196 (citing

EX1016). Specifically, a POSITA would have recognized that quality control can be performed on the memory cells (e.g., testing for shorts). *Id.* If a quality issue is detected, then only that level 3104 would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded. *Id.* Thus, Kim's wafer-bonding process minimizes waste resulting from defects detected in quality control. *Id.*

A POSITA would have had a reasonable expectation of success in using wafer bonding to attach Lee's separately fabricated memory devices in layer 3104 to insulating layer 3102 because Kim shows that using such a technique to bond one wafer with electrical devices to another wafer with memory cells was within the skill of a POSITA. *Id.*, ¶197 (citing EX1008, ¶¶19, 20).

c. 13[d]

For the same reasons discussed in Section VII.A.1.e, Lee discloses or suggests 13[d].

2. Claims 14–17

Lee discloses or suggests the elements of claims 14–17 as discussed in Sections VII.A.2–VII.A.5.

D. Ground 1D: Obviousness over Lee, Kim, and Endoh (claims 16–17)

Lee and Kim render obvious claims 16 and 17 under the proper construction of “the stackable add-on layer being bonded” and PO’s apparent construction of “SOI pillar.” Claims 16 and 17 would have also been obvious over Lee, Kim, and Endoh under those constructions. The description of the Lee-Kim combination (Section VII.C), the description of the Lee-Endoh combination (Section VII.B), and the motivation to combine and reasonable expectation of success discussion for the Lee-Kim (Section VII.C.1.b) and Lee-Endoh (Section VII.B.1) combinations apply equally to this ground. Sechen, ¶200.

E. Ground 1E: Obviousness over Lee and Aspar (Claims 13–17)

As discussed in Section VI.A, a POSITA would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the “stackable add-on layer” is wafer bonded to “the dielectric layer.” Additionally, as discussed in Section VI.B, a POSITA would have understood that “SOI pillar” means a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology. Under these proper constructions, claims 13–17 would have been obvious over Lee and Aspar for the reasons discussed below.

1. Claim 13

a. 13[pre]-13[b]

For the same reasons discussed in Sections VII.A.1.a–VII.A.1.c, Lee discloses or suggests 13[pre]–13[b]. In 13[b], “a” stackable add-on layer encompasses one or more stackable add-on layers. Sechen, ¶202.

b. 13[c]

Under the proper construction of “the stackable add-on layer being bonded” as requiring the “stackable add-on layer” to be wafer bonded to “the dielectric layer,” the combination of Lee with Aspar teaches 13[c]. Sechen, ¶¶203-215.

In Lee, each level 3104 is deposited on the underlying levels of array 3101. EX1007, ¶107. Lee does not clearly describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102. *See id.*, ¶¶107–113. Consequently, a POSITA would have looked to and been motivated to apply other art, such as known wafer bonding techniques, for details about attaching bottom level 3104 to insulating layer 3102. Sechen, ¶204.

One such known wafer bonding technique was the Smart-Cut® process described in Aspar. EX1009, 834. Aspar states “[w]afer bonding and layer transfer enable different materials to be associated to form multilayer substrates,” and the Smart-Cut® process was “an industrial process which provides high quality materials in large quantities.” *Id.* Specifically, Aspar touts the Smart-Cut® process’

ability to transfer a thin monocrystalline layer of “very good thickness homogeneity and with a high crystalline quality.” *Id.*

The Smart-Cut® process is depicted in Aspar’s Figure 1 (below):

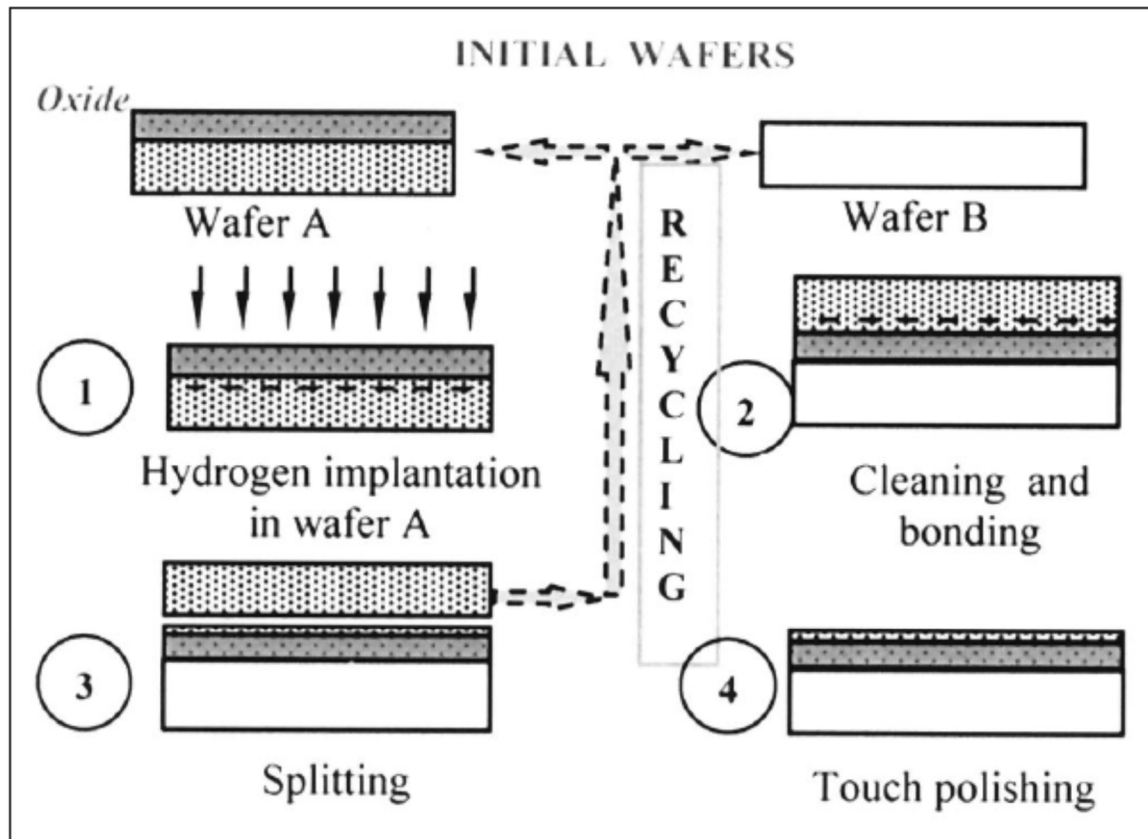


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

Figure 1 shows the following steps:

1. Hydrogen is implanted in a substrate A. This step induces formation of an in-depth weakened layer.
2. Substrate A is bonded to a support B by wafer bonding.

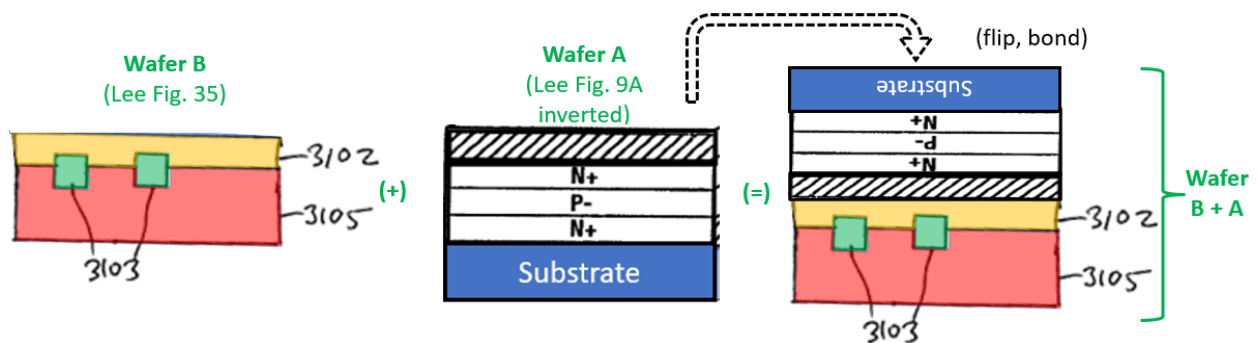
3. A splitting step, which takes place along the in-depth weakened layer, gives rise to transfer of a thin layer from the substrate A onto the support B.
4. A final treatment can be performed to remove the rough surface left after splitting.

Id., 834–835. Aspar’s description of using Smart-Cut® to transfer a thin layer is consistent with the ’702 Patent’s description of its “SOI layer,” namely, “a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate.” ’702Pat., 4:48–51; Sechen, ¶207.

Aspar states “we can conclude that the Smart-Cut process really is a generic process. It allows a great deal of combinations (material and bonding layer) which open up new scope for developments.” EX1009, 839. Among these combinations, Aspar states that the Smart-Cut® process is compatible with conductive (metallic) bonding layers and can be used “to realize complex structures,” including by “transferring SOI layer stacks already formed onto a single substrate or a SOI wafer.” *Id.*, 838–839.

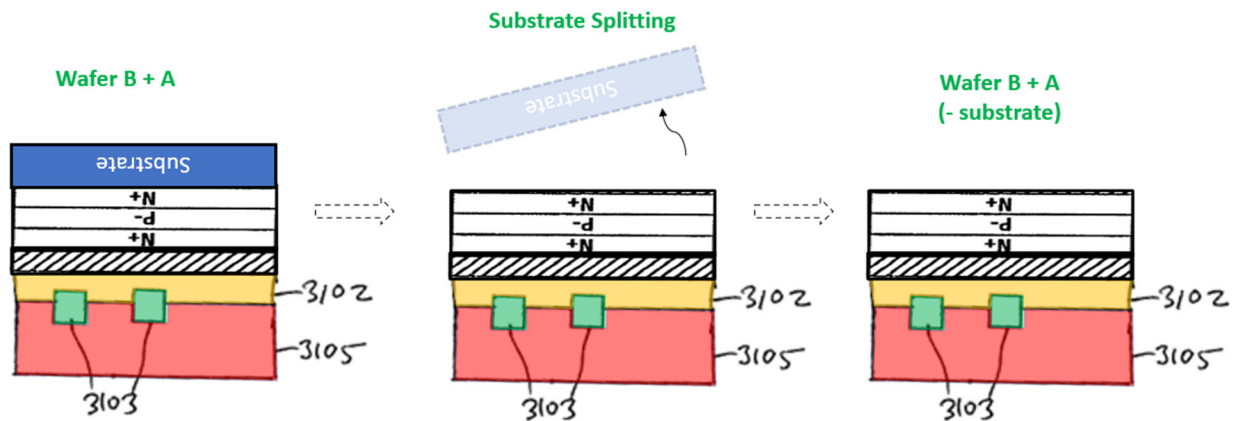
In the combination, Aspar’s Smart-Cut® process would be used to wafer bond bottom level 3104 (“stackable add-on layer”) in Lee’s Figure 35 to insulating layer 3102 (“dielectric layer”). Sechen, ¶209. Wafer B would consist of Lee’s substrate

3105 with driver circuits 3103 formed therein and insulating layer 3102 disposed above the substrate. *Id.* Wafer A would be separately fabricated with a single crystal surface layer with a doped stack, similar to stack 902 depicted in Lee's Figure 9A to form the pillars for the memory cell structures of Figs. 1A–1B, 2, 7, and 25A. *Id.*; EX1007, ¶¶119, 122, 125, 138–141; *see also id.*, Fig. 13A, ¶¶147–148; Fn. 9. A conductive layer would then be deposited over the doped stack, as taught in Lee's Figure 9A which includes input/output conductor layer 900 to form the first input/output conductors for the memory cell structures of Figs. 1A–1B, 2, 7, and 25A. EX1007, ¶¶139–141, 119, 122, 125, 138; *see also id.*, Fig. 13A, ¶¶147–148; Fn. 9; Sechen, ¶209. After the levels on Wafer A were formed, Wafer A would be flipped upside down and bonded to Wafer B. This process is depicted in the annotated series of figures below:



Sechen, ¶209.

After bonding, a splitting (i.e., cleaving) step would be performed, resulting in the transfer of the desired thin layer (e.g., the doped stack) and conductive layer from Wafer A onto Wafer B. This process is depicted in the annotated series of figures below:



Sechen, ¶210. After bonding, the individual memory cells in level 3104 would be fabricated from the transferred thin layer in the same way they are fabricated in Lee. *E.g.*, EX1007, ¶141; Sechen, ¶211.

A POSITA would have been motivated to use Aspar's Smart-Cut® process to wafer bond bottom level 3104 ("stackable add-on layer") to insulating layer 3102 ("dielectric layer") of Lee's Figure 35 for several reasons. Sechen, ¶212 (citing EX1008, ¶20, Fig. 1). Aspar itself teaches that Smart-Cut® "[r]ealiz[es] multiple SOI layers based on a layer transfer process ... [such as] transferring SOI layers stacks already formed onto a single substrate or a SOI wafer. So multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology." EX1009, 839. In

addition, the Smart-Cut® process was known to have several advantages including “transferring thin layers of very good thickness homogeneity and with a high crystalline quality.” Sechen, ¶212; (quoting EX1009, 834). This combination merely amounts to using a known technique (Aspar's Smart-Cut® process) to improve a similar known device (the structure in Lee’s Figure 35) in the same way (vertically stacking memory devices using SOI technology). *Id.* In addition, the combination would have amounted to applying a known technique (Aspar’s Smart-Cut® process) to address the same known problem recognized by both Lee and Aspar (fabricating 3D structures) using prior art elements according to their established functions (Aspar’s Smart-Cut® process and Lee’s Figure 35 memory device using the memory cell structures of Figure 1A-1B, 2, 7, or 25A). *Id.*; *see Intel*, 61 F.4th at 1380; *KSR*, 550 U.S. at 417.

A POSITA would have also recognized that Aspar’s Smart-Cut® process as compared to monolithic deposition allows for more efficient quality control at the layer formation stage. Sechen, ¶213 (citing EX1016). Specifically, when using Smart-Cut®, quality control can be performed on the stack prior to bonding (e.g., thickness, uniformity, etc.). *Id.* If a quality issue is detected, then only that stack would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would

need to be discarded. *Id.* Thus, Aspar’s Smart-Cut® process minimizes waste resulting from defects detected in quality control. *Id.*

A POSITA would have had a reasonable expectation of success in using Aspar’s Smart-Cut® process to wafer bond bottom level 3104 (“stackable add-on layer”) to insulating layer 3102 (“dielectric layer”) of Lee’s Figure 35. *Id.*, ¶214. Indeed, Lee’s substrate 3105 with driver circuits 3103 therein and insulating layer 3102 on top is suitable for use with SOI technology such as Aspar’s Smart-Cut® process to add a stackable add-on layer. *Compare* EX1007, ¶¶111–208, *with* EX1009, 834, 837 (“major application of this process is...fabrication SOI wafers”), 839. In addition, the Smart-Cut® process was understood as a predictable process at the relevant time, and had been used, for example, to transfer SOI stacks and with metallic bonding layers. Sechen, ¶214 (citing EX1009, 838–839). Further, a POSITA would have recognized Aspar’s process for transferring thin monocrystalline layers as compatible with Lee, which contemplates using single crystal silicon for the thin film transistor (TFT) pillars of its memory cells. *Id.* (citing EX1009, 834; EX1007, ¶¶119, 139).

Alternatively, Aspar teaches repeated transfers of single layers (each a stackable add-on layer of the one or more stackable add-on layers encompassed by 13[b]). EX1009, 838–839. Those single layers would be transferred to a holding wafer and then wafer bonded as a stack to the dielectric, or each individual layer

would be bonded to Wafer B in a series of wafer bonding steps. Sechen, ¶215 (citing EX1024). The conductive layer, including silicon (EX1007, ¶126) or other conductive material, would be transferred as a single layer to the holding wafer or bonded to Wafer B, deposited on the stack of the holding wafer prior to bonding, or deposited on another single layer for bonding with that layer to Wafer B. Sechen, ¶215. The motivation to combine and reasonable expectation of success analyses discussed above would apply equally for these combinations. *Id.*

c. 13[d]

For the same reasons discussed in Section VII.A.1.e, Lee discloses or suggests 13[d].

2. Claims 14–17

Lee discloses the elements of claims 14–17 as discussed in Sections VII.A.2-VII.A.5. Additionally, Section VII.E.1.b describes that the stackable add-on layer is added using Aspar’s Smart-Cut® process which is SOI technology. EX1009, 834, 837 (“major application of this process is...fabrication SOI wafers”), 839. As described in that Section, the doped stack of the stackable add-on layer bonded to Wafer B is used to form pillars (“SOI pillars”) for the memory cell structures of Lee’s Figure 1A–1B, 2, 7, or 25A. Sechen, ¶217.

F. Ground 1F: Obviousness over Lee, Aspar, and Endoh (claims 16–17)

Lee and Endoh render obvious claims 16–17 under PO’s apparent constructions as discussed in Section VII.B. Under the proper constructions of “stackable add-on layer being bonded” and “SOI pillar,” claims 16–17 would have been obvious over Lee, Aspar, and Endoh. The description of the Lee-Aspar combination (Section VII.E), the description of the Lee-Endoh combination (Section VII.B), and the motivation to combine and reasonable expectation of success discussion for the Lee-Aspar (Section VII.E.1.b) and Lee-Endoh (Section VII.B.1) combinations apply equally to this ground. Sechen, ¶218.

Additionally, Section VII.E.1.b describes that the stackable add-on layer is added using Aspar’s Smart-Cut® process which is SOI technology. Aspar, 834, 837 (“major application of this process is... fabrication SOI wafers”), 839. As described in that Section, the doped stack of the stackable add-on layer bonded to Wafer B is used to form the pillars (“SOI pillars”) for the memory cell structures of Lee’s Figure 1A–1B, 2, 7, or 25A. A POSITA would have also found it obvious to form a suitable doped stack of the stackable add-on layer added using SOI technology to form SOI pillars with two memory cells as taught in Endoh for the same reasons described in Sections VII.E.1.b and VII.B.1. Sechen, ¶219.

G. Ground 2A: Obviousness over Johnson (Claim 13)

As discussed in Section VI.A, PO may argue that “the stackable add-on layer being bonded” encompasses any type of layer that is directly or indirectly adhered to the “dielectric layer.” Although not correct, under such a construction, claim 13 would have been obvious over Johnson for the reasons discussed below.

1. Claim 13

a. 13[pre]

To the extent the preamble is limiting, Johnson discloses or suggests it. Sechen, ¶221. Specifically, Johnson discloses a “low cost, high density *semiconductor memor[y]*.” EX1010, 1:7–12, 5:41–45, 6:52–56, 7:49–61, Fig. 4(a).

b. 13[a]

Johnson discloses or suggests 13[a]. Sechen, ¶¶222–227. Johnson teaches “a substrate having electrical devices formed therein.” EX1010, 13:26–35 (“CMOS transistors may be fabricated in the monocrystalline substrate for the peripheral circuitry”). A POSITA would have understood that Johnson’s “CMOS transistors” are “electrical devices” as the ’702 Patent defines them, i.e., “active circuit elements,” namely, those having power gain. Sechen, ¶¶223–225. Further, a POSITA would have known that “CMOS transistors” are types of “FETs” or MOSFETs, which the ’702 Patent and incorporated ’941 Patent each provide as an example of a

“device” (’702Pat., 4:28–34; ’941Pat, 5:51–54, 59-60). Sechen, ¶225. Accordingly, Johnson teaches “a substrate having electrical devices formed therein.”

Regarding “a dielectric layer disposed above the electrical devices,” Johnson’s fabrication starts with a wafer having devices in the substrate and “[a]n insulator then is deposited.” EX1010, 13:26–35. Johnson further teaches the “fabrication sequence for the memory cell” depicted in Figures 6(b)-6(g) involves “deposition and planarization of an interlevel dielectric.” *Id.*, 12:42–54. Accordingly, Johnson teaches “a dielectric layer disposed above the electrical devices.” Sechen, ¶226.

c. 13[b]

Under PO’s apparent construction of “stackable add-on layer,” Johnson discloses or suggests 13[b]. Sechen, ¶¶228-231. First, Johnson discloses “vertically oriented semiconductor memory cells.” The ’702 Patent states: “The term ‘vertical,’ as used herein, means substantially perpendicular to a major surface of a substrate, such as, for example, a semiconductor wafer.” ’702Pat., 4:6–8. Figure 4(a) (reproduced below) depicts one embodiment where the elements of the memory cell “are stacked vertically in a ‘pillar’ shaped arrangement” with current also flowing vertically. EX1010, Fig. 4(a), 1:7–12, 2:33–37, 4:30–51, 5:30–42, 5:66–6:7 (“[T]he steering element 22 and the state change element 23 are stacked vertically in a

‘pillar’ shaped arrangement...The pillar is vertical and so is the current flow.”);
Sechen, ¶229.

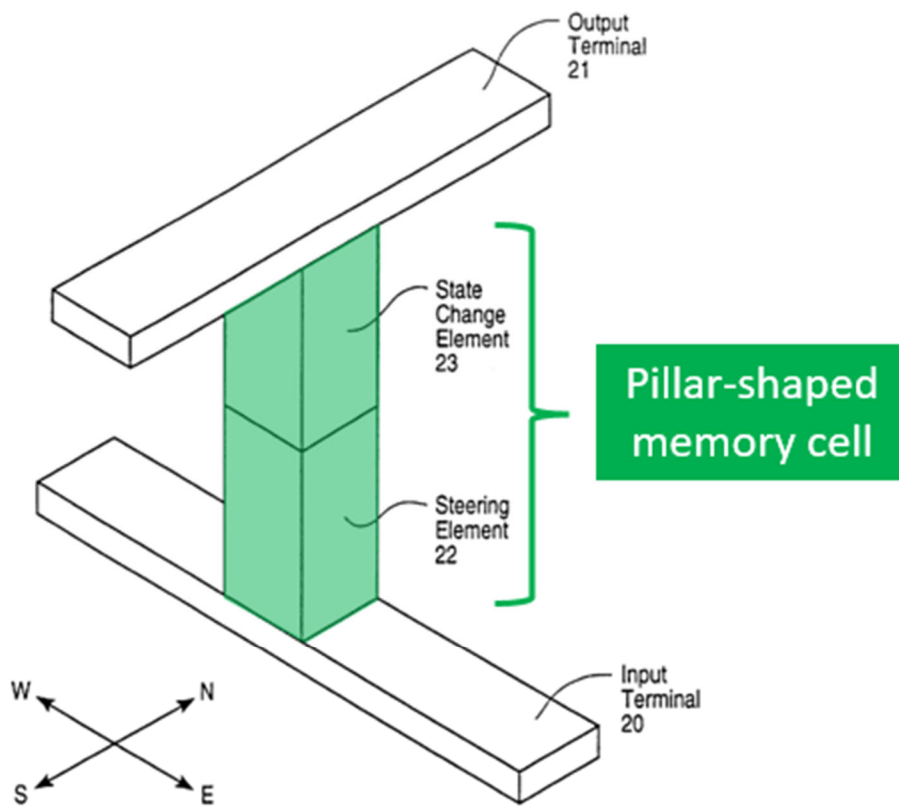


FIG. 4(a)

Second, Johnson discloses “[a] unique organization of these cells in a three dimensional memory array disposed above a substrate.” EX1010, 5:38–40. The memory cells “can be stacked vertically in numerous layers to form a three dimensional array.” *Id.*, 5:30–37. Figure 5 (below) shows an exemplary three

dimensional memory array with each layer having two memory cell pillars (27 in Layer 1). *Id.*, 6:63–7:10, 11:10–25, Fig. 5.

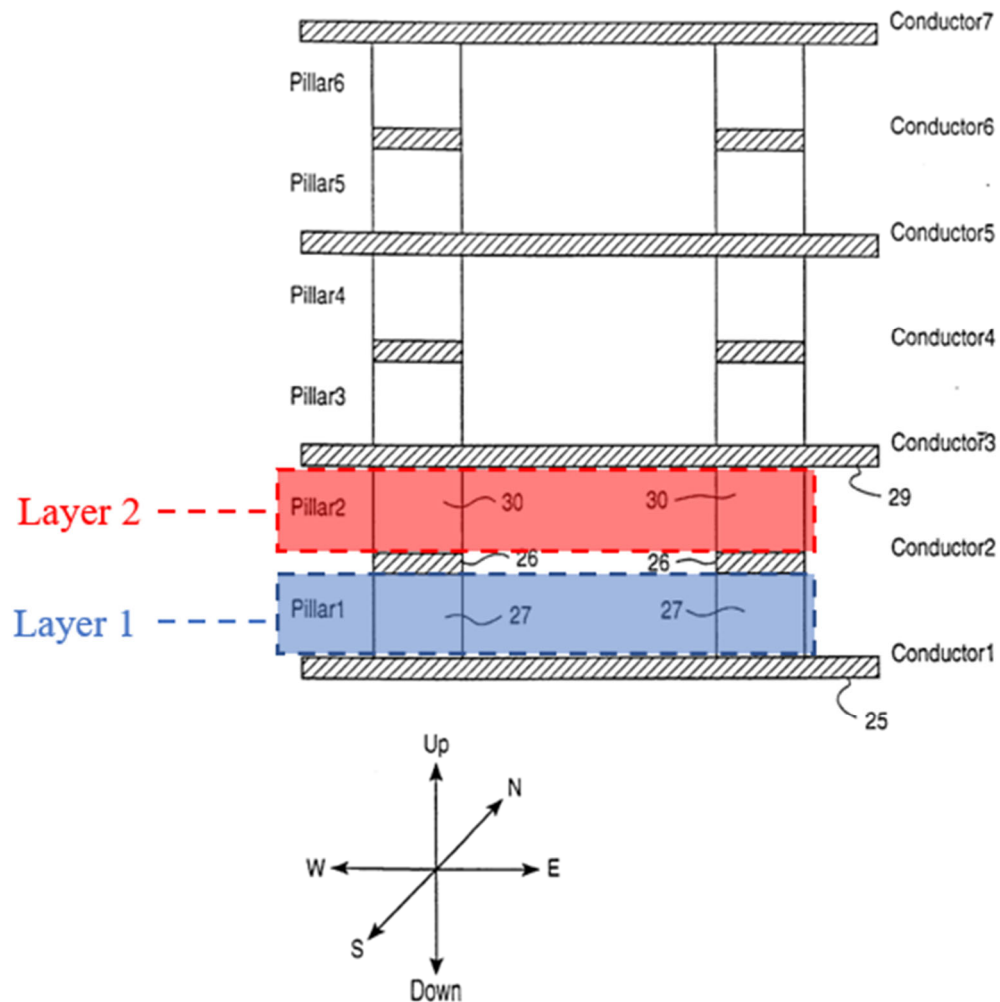


FIG. 5

Bottom layer 1 shown in Johnson’s Figure 5 (with or without Conductor1) teaches a “stackable add-on layer” having a plurality of vertically-oriented semiconductor memory cells under PO’s apparent construction. Sechen, ¶230.

d. 13[c]

Under PO's apparent construction of "stackable add-on layer being bonded," Johnson discloses or suggests 13[c]. Sechen, ¶¶232-238.

Johnson teaches fabrication with a series of deposition and etching steps in Figures 6(b)–6(g). EX1010, 12:42–65. The fabrication process starts with an insulator¹⁴ (not shown) deposited on a wafer. *Id.*, 13:26–35. Next, conductor layer 46 (red) followed by stack 45 (yellow) are deposited. *Id.*, 12:8–12, 13:26–35, Fig. 6(b) (below).

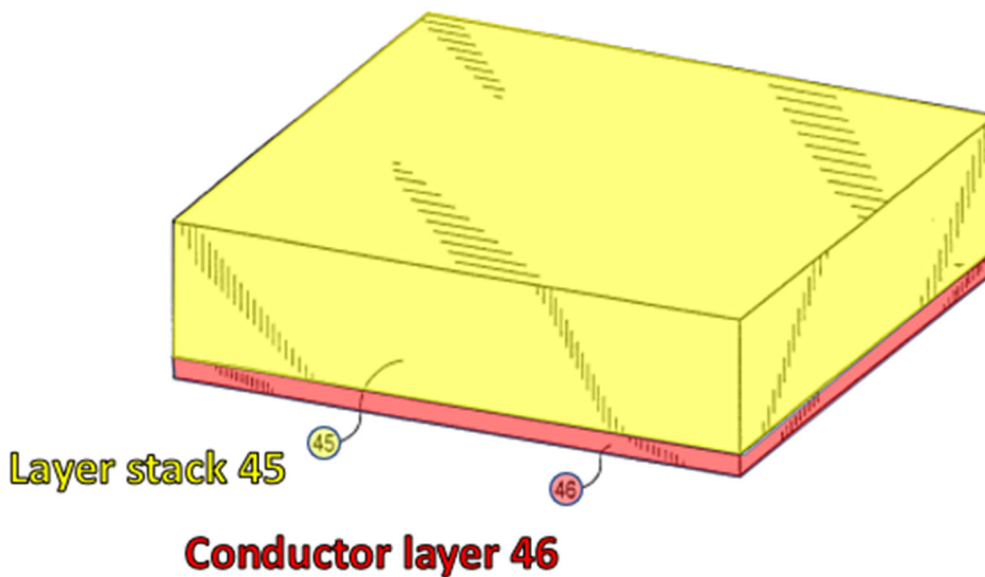


FIG. 6(b)

¹⁴ A POSITA would have understood that an insulating layer is a "dielectric layer." Sechen, ¶233.

Next, Figure 6(c) below illustrates the result of an etching step applied to the stack. *Id.*, 13:36–41.

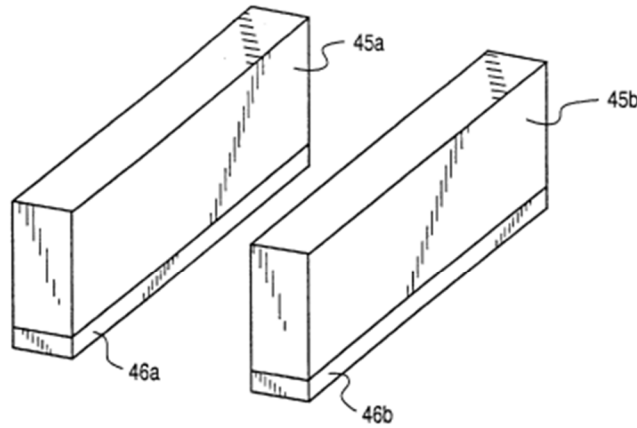


FIG. 6(c)

Next, another conductor layer 50 and stack 51 are deposited (Figure 6(d) below). *Id.*, 13:58–60.

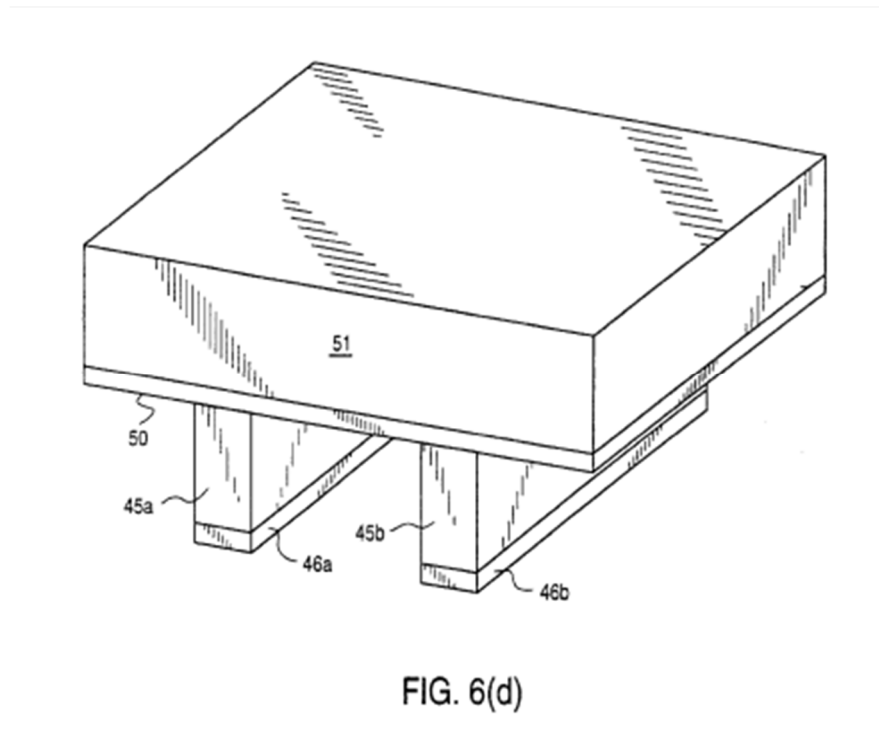


Figure 6(e) below illustrates the result of another etching step that forms four pillars in the bottom layer (45a1, 45a2, 45b1, 45b2). *Id.*, 13:64–14:6. A POSITA would have understood that this bottom layer (with or without conductors 46a, 46b) corresponds to the bottom layer shown in Figure 5 (above) (“stackable add-on layer”). Sechen, ¶236.

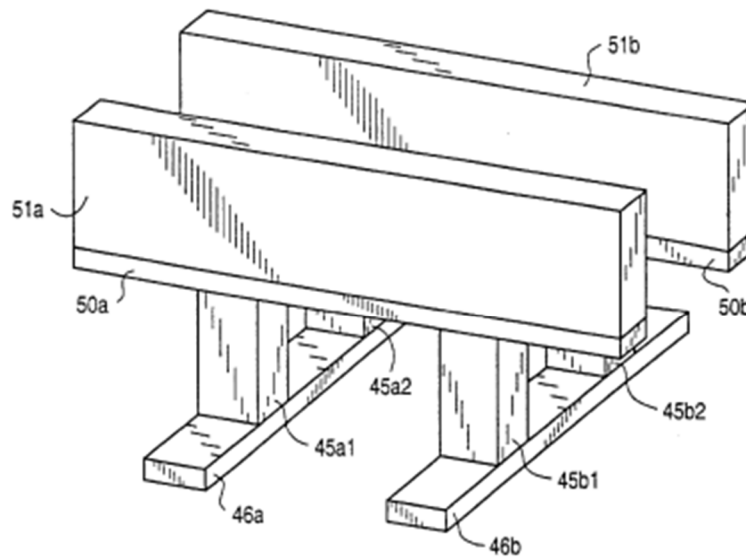


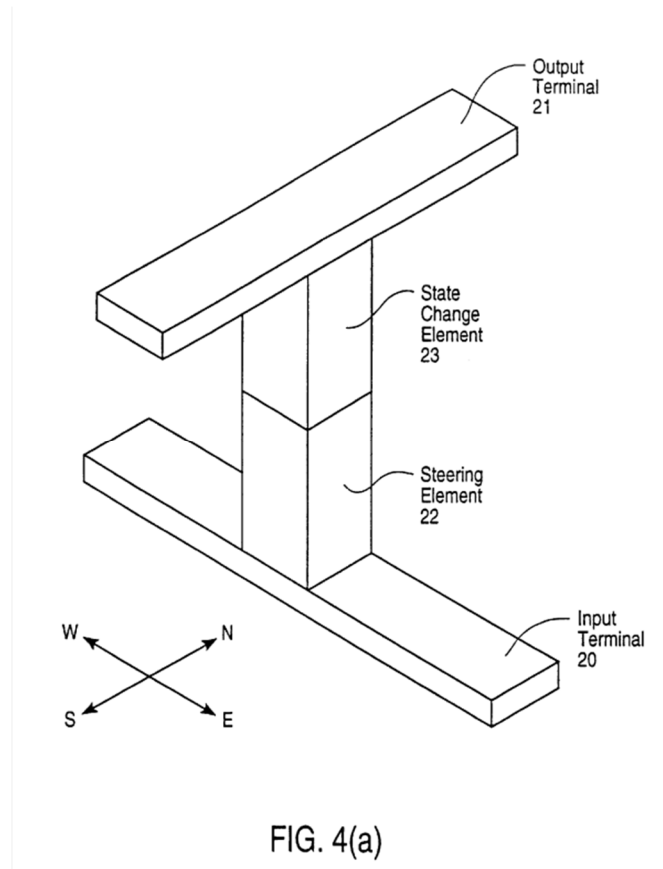
FIG. 6(e)

Johnson teaches a stackable add-on layer monolithically and directly or indirectly created on the insulator, or “dielectric layer,” via a series of deposition and etching steps. *Id.*, 13:26–35; Sechen, ¶¶233–237. As such, Johnson discloses or suggests that the stackable add-on layer (bottom layer 1 shown in Johnson’s Figure 5 (with or without Conductor1)) is directly or indirectly adhered to the dielectric layer (PO’s apparent construction). *Id.*

e. 13[d]

Johnson discloses or suggests 13[d]. Sechen, ¶¶239–243. Johnson is directed to nonvolatile memory cells. *See, e.g.*, EX1010, Title (“Vertically stacked field programmable nonvolatile memory”), 1:7–12, 9:59–62. In Johnson, each

nonvolatile memory cell has at least one transistor because Johnson describes that steering element 22 (Figure 4(a)) can be implemented using “a junction field-effect transistor with gate connected to source (or to drain)” or “a MOSFET with gate either floating, or connected to source or connected to drain.” *Id.*, 5:41–49, 7:61–8:5.



Thus, a POSITA would have understood steering element 22 of Johnson’s nonvolatile pillar memory cell to include at least one transistor because Johnson expressly discloses such implementations. Sechen, ¶¶239-242; EX1010, 7:61–8:5.

H. Ground 2B: Obviousness over Johnson and Kim (Claim 13)

As discussed in Section VI.A, a POSITA would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the “stackable add-on layer” is wafer bonded to “the dielectric layer.” Under this proper construction, claim 13 would have been obvious over Johnson and Kim for the reasons discussed below.

1. Claim 13

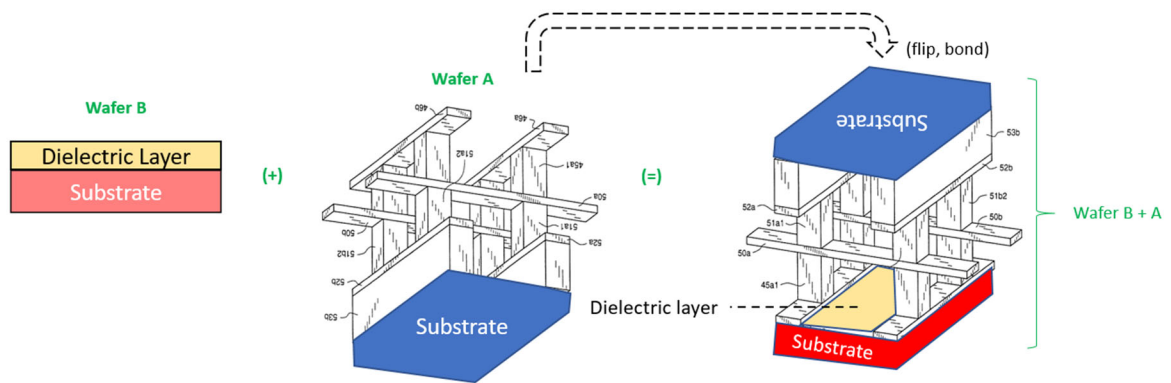
a. 13[pre]-13[b]

For the same reasons discussed in Sections VII.G.1.a–VII.G.1.c, Johnson discloses or suggests 13[pre]–13[b].

b. 13[c]

Under the proper construction of “the stackable add-on layer being bonded,” the combination of Johnson and Kim teaches 13[c]. Sechen, ¶¶246-251. Although Johnson discloses a series of deposition and etching steps as discussed in Section VII.G, a POSITA would have been motivated to use Kim’s wafer bonding techniques when fabricating Johnson’s structure for the reasons explained below. *Id.* Kim’s wafer stacking and bonding technique is discussed in Section VII.C.1.b. Sechen, ¶246.

The figures below illustrate one way a POSITA would have found it obvious to apply Kim’s teachings in Johnson. Sechen, ¶¶247-248.



Johnson’s separately fabricated memory cells (e.g., from Johnson’s Figure 6(e)) would be formed on their own substrate (“Wafer A”). Sechen, ¶248. Wafer A would be flipped and bonded to Wafer B having, for example, Johnson’s “CMOS transistors” (“electrical devices”) and insulating layer (“dielectric layer”). *Id.*; EX1008, ¶20. In the combination, as in Kim Figure 1 where wafer 120 is bonded to wafer 110 using a dielectric layer 102, Johnson’s layer of memory cells (“stackable add-on layer”) would be wafer bonded to Johnson’s insulating layer (“dielectric layer”). Sechen, ¶248.

A POSITA would have been motivated to wafer bond Johnson’s layer of memory cells (“stackable add-on layer”) to its insulating layer (“dielectric layer”) based on Kim’s teachings for several reasons. A POSITA would have recognized that using wafer-bonding to bond Johnson’s layer of memory cells (“stackable add-on layer”) to its insulating layer (“dielectric layer”) would have been a predictable way to non-monolithically build Johnson’s 3D structure. Sechen, ¶249. Specifically, this modification consists of nothing more than using a known technique (Kim’s

wafer bonding) to improve a similar known device (Johnson's structure) in the same way (logic/memory stacking using a wafer bonding process). *Id.* In addition, the combination would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Johnson and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim's wafer bonding and Johnson's structure). *Id.*; see *Intel*, 61 F.4th at 1380; *KSR*, 550 U.S. at 417.

A POSITA would have also recognized that wafer-bonding Johnson's level of memory cells to its insulating layer, as compared to monolithic deposition, allows for more efficient quality control with less potential waste. Sechen, ¶250 (citing EX1016). Specifically, a POSITA would have recognized that quality control can be performed on the memory cells (e.g., testing for shorts). *Id.* If a quality issue is detected, then only that level would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded. *Id.* Thus, Kim's wafer-bonding process minimizes waste resulting from defects detected in quality control. *Id.*

A POSITA would have had a reasonable expectation of success in using wafer bonding to attach Johnson's layer of memory cells to its insulating layer because Kim shows that using such a technique to bond one wafer with electrical devices to

another wafer with memory cells was within the skill of a POSITA. Sechen, ¶251 (citing EX1008, ¶¶19, 20).

c. 13[d]

For the same reasons discussed in Section VII.G.1.e, Johnson discloses or suggests 13[d].

I. Ground 2C: Obviousness over Johnson and Aspar (Claim 13)

As discussed in Section VI.A, a POSITA would have understood “the stackable add-on layer being bonded” as recited in claim 13 to require that the “stackable add-on layer” is wafer bonded to “the dielectric layer.” Under this proper construction, claim 13 would have been obvious over Johnson and Aspar for the reasons discussed below.

1. Claim 13

a. Claim[pre]–13[b]

For the same reasons discussed in Sections VII.G.1.a–VII.G.1.c, Johnson discloses or suggests 13[pre]–13[b].

b. Claim 13[c]

Under the proper construction of “the stackable add-on layer being bonded” as discussed in Section VI.A, the combination of Johnson with Aspar teaches 13[c]. Sechen, ¶¶255-262.

As discussed in Section VII.DVII.E, Aspar discloses a wafer bonding technique called the Smart-Cut® process that transfers a thin monocrystalline layer of “very good thickness homogeneity and with a high crystalline quality.” EX1009, 834. The Smart-Cut® process is a generic process that is compatible with conductive (metallic) bonding layers and can be used “to realize complex structures,” including by “transferring SOI layer stacks already formed onto a single substrate or a SOI wafer.” *Id.*, 838–839.

In the combination, Aspar’s Smart-Cut® wafer bonding process would be used to bond Johnson’s layer of memory cells to its insulating layer. Wafer B would have, for example, Johnson’s “CMOS transistors” (“electrical devices”) and insulating layer (“dielectric layer”). EX1010, 4:19–22, 12:42–54, 13:26–35. Wafer A would have a thin single crystal film with a doped stack, similar to the stack depicted in Johnson Figures 6(a) and 6(b) annotated below. Sechen, ¶257. A conductive layer would then be deposited over the doped stack, as taught in Johnson Figures 6(a) and 6(b). *Id.* This structure is depicted in the annotated figures below.

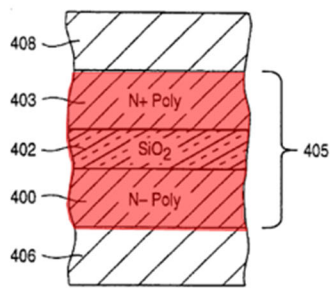


FIG. 6(a)

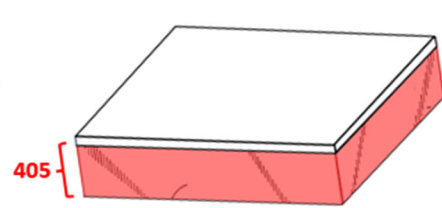
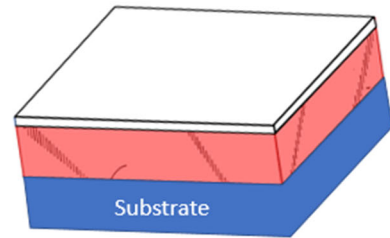
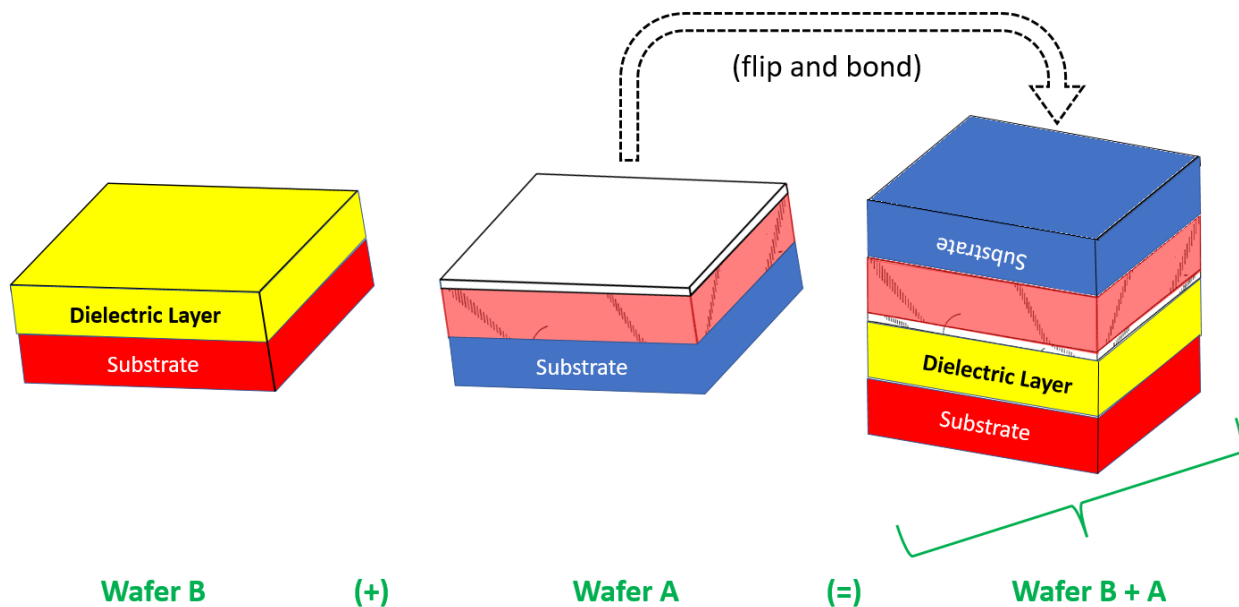


FIG. 6(b)
(inverted)



Wafer A

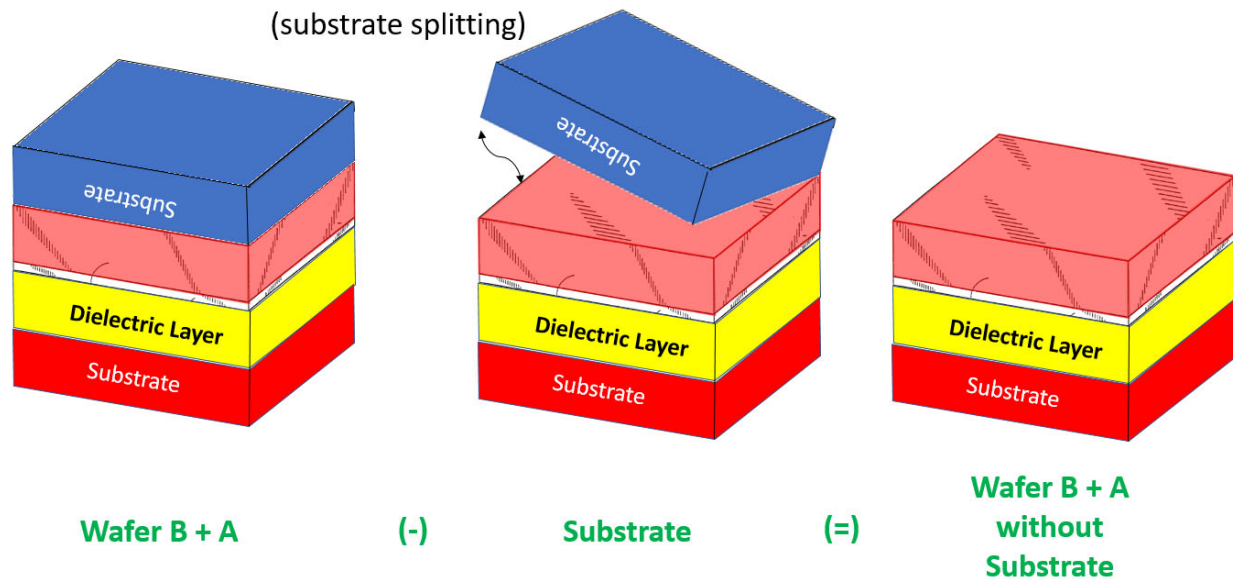
Id. Wafer A would be flipped upside down and bonded to Wafer B. This process is depicted in the annotated series of figures below:



Sechen, ¶258.

After bonding, a splitting (i.e., cleaving) step would be performed, resulting in the transfer of the desired thin layer (e.g., the doped stack) and conductive layer

from Wafer A onto Wafer B. This process is depicted in the annotated series of figures below:



Sechen, ¶259.

A POSITA would have been motivated to use Aspar’s Smart-Cut® process to wafer bond a layer of semiconductor pillars as depicted in Johnson’s Figures 6(a)–(b) (“stackable add-on layer”) to the insulating layer above the substrate (“dielectric layer”) for several reasons. *Id.*, ¶260. Aspar itself teaches that Smart-Cut® “[r]ealiz[es] multiple SOI layers based on a layer transfer process ... [such as] transferring SOI layers stacks already formed onto a single substrate or a SOI wafer. So multiple SOI layers stacks can be easily performed thanks to Smart-Cut technology.” EX1009, 839. In addition, the Smart-Cut® process was known to have several advantages including “transferring thin layers of very good thickness

homogeneity and with a high crystalline quality.” Sechen, ¶260 (quoting EX1009, 834). This combination merely amounts to using a known technique (Aspar’s Smart-Cut® process) to improve a similar known device (Johnson’s structure) in the same way (vertically stacking memory devices using SOI technology). *Id.* In addition, the combination would have amounted to applying a known technique (Aspar’s Smart-Cut® process) to address the same known problem recognized by both Johnson and Aspar (fabricating 3D structures) using prior art elements according to their established functions (Aspar’s Smart-Cut® process and Johnson’s structure). *Id.*; see *Intel*, 61 F.4th at 1380; *KSR*, 550 U.S. at 417.

A POSITA would have also recognized that Aspar’s Smart-Cut® process as compared to monolithic deposition allows for more efficient quality control at the layer formation stage. Sechen, ¶261 (citing EX1016). Specifically, when using Smart-Cut®, quality control can be performed on the stack prior to bonding (e.g., thickness, uniformity, etc.). *Id.* If a quality issue is detected, then only that stack would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded. *Id.* Thus, Aspar’s Smart-Cut® process minimizes waste resulting from defects detected in quality control. *Id.*

A POSITA would have had a reasonable expectation of success in using Aspar’s Smart-Cut® process to wafer bond a stack of materials as depicted in

Figures 6(a)–(b) (“stackable add-on layer”) to the insulating layer above the substrate (“dielectric layer”). *Id.*, ¶262. In addition, the Smart-Cut® process was understood as a predictable process at the relevant time, and had been used, for example, to transfer SOI stacks and with metallic bonding layers. *Id.* (citing EX1009, 838–839). Further, a POSITA would have recognized Aspar’s process for transferring thin monocrystalline layers as compatible with the types of memory cells in Johnson (e.g., a MOSFET with gate either floating, or connected to source or connected to drain (steering element) with, e.g., polysilicon resistor-fuse (state change element)). *Id.* (citing EX1010, 7:49-51, 7:67–8:1, 8:46-55; EX1009, 834; EX1007, ¶¶127, 139).

c. Claim 13[d]

For the same reasons discussed in Section VII.G.1.e, Johnson discloses or suggests 13[d].

J. Ground 3: Obviousness over Park and Kim (Claim 1)

Under either construction of “the stackable add-on layer is bonded” as discussed in Section VI.A, claim 1 would have been obvious over Park and Kim for the reasons discussed below.

1. Claim 1

a. 1[pre]

To the extent the preamble is limiting, the combination of Park and Kim discloses or suggests it. Sechen, ¶¶266-269. Park discloses “a semiconductor memory device,” and more specifically DRAM. EX1011, 2:11–14, 5:20–24, 1:17–21. Kim further discloses vertically integrating memory devices with logic. EX1008, ¶22. A POSITA would have understood Kim’s wafer stack comprising logic devices in combination with Park’s DRAM cells to be “a semiconductor memory structure.” Sechen, ¶266.

Park discloses vertically structured DRAM cells that enable “increased integration.” EX1011, 2:7–10. Kim’s teachings are discussed in Section VII.C. Kim explains that an advantage of “vertically stacking many layers of active IC devices such as processors, programmable devices and memory devices inside a single chip [is] to shorten average wire lengths, thereby reducing interconnect RC delay and increasing system performance.” EX1008, ¶¶7, 22.

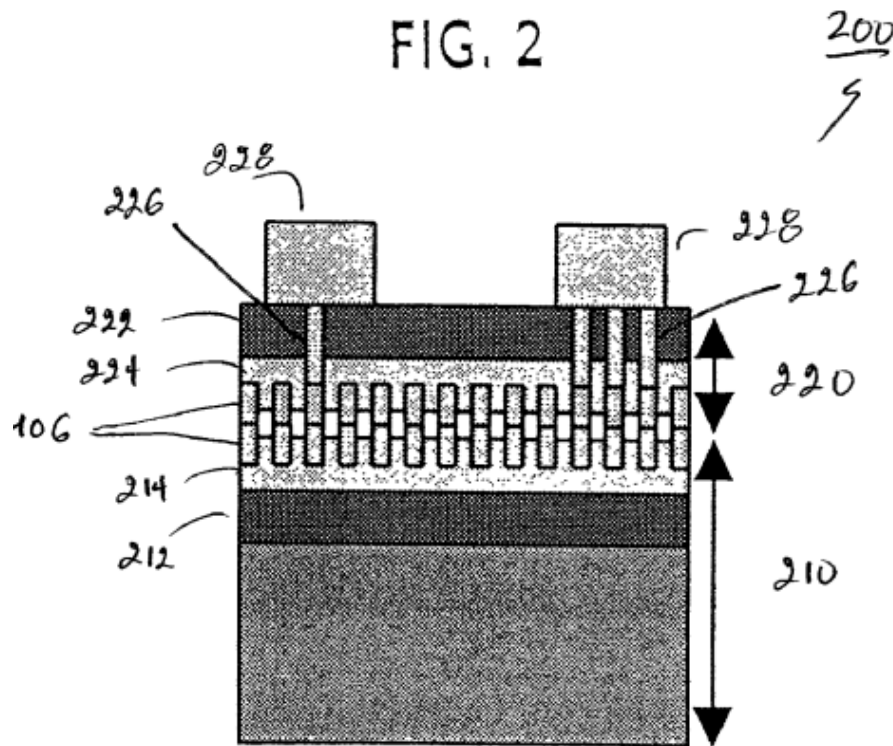
A POSITA would have been motivated to vertically stack, through wafer bonding, Park’s DRAM memory cells on top of logic devices, e.g., one or more microprocessors, based on Kim’s teachings because the combination would have furthered Park’s and Kim’s express goal of increasing integration, and resulted in Kim’s advantage of reducing interconnect RC delay and increasing system

performance. Sechen, ¶¶267-268. Integrating Park's DRAM memory cells with logic per Kim's teachings would have been no more than applying a known technique (Kim's 3D wafer stacking of logic and memory cells) to a known device ready for improvement (Park's vertically structured DRAM cells) to yield predictable results (increased performance through logic/memory stacking). *Id.*, ¶268. It would have further been a simple substitution of one known element (Park's DRAM) for another (Kim's memory cells) to yield predictable results (increased integration of memory devices wafer bonded to logic). *Id.* In addition, the combination would have amounted to applying a known technique (Kim's wafer bonding) to address the same known problem recognized by both Park and Kim (fabricating 3D memory arrays) using prior art elements according to their established functions (Park's and Kim's structures). *Id.*; see *Intel*, 61 F.4th at 1380; *KSR*, 550 U.S. at 417.

A POSITA would have further had a reasonable expectation of success in employing Kim's 3D wafer stacking with Park's vertically-oriented DRAM cells because the teachings of both Park and Kim would have been employed for their intended purposes. Sechen, ¶269. Further, Kim shows that the combination was within the skill of a POSITA because Kim wafer bonds one wafer with electrical devices to another wafer with memory cells. *Id.* (citing EX1008, ¶¶19, 20).

b. 1[a]

The combination of Park and Kim discloses or suggests 1[a]. Sechen, ¶¶270-272. Kim generally discloses a “3D wafer-to-wafer vertical stack,” where, for example, the bottom wafer of a stack may include “one or more microprocessors” and the second wafer includes “one or more memory devices” EX1008, ¶20. Kim then provides a more detailed description of an exemplary two-wafer vertical stack wherein “bottom silicon (Si) wafer 210 may include an active silicon (Si) layer 212 supporting one or more active IC devices (not shown) and an interlayer dielectric (ILD) layer 214.” *Id.*, ¶23; Sechen, ¶270. Kim’s two-wafer vertical stack is illustrated in its Figure 2:



A POSITA would have understood Kim's first wafer 210 including "active silicon (Si) layer 212 supporting one or more active IC devices (not shown)" to be "a substrate having electrical devices formed therein." Sechen, ¶271. Kim further explains that the wafers are "bonded, via a metal bonding layer 106 deposited on opposing surfaces of the bottom wafer 210 and the top wafer 220 at designated bonding areas to establish electrical connections between active IC devices on vertically stacked wafers 210 and 220 and to bond adjacent wafers 210 and 220, while maintaining electrical isolation between bonding areas via ILD [interlayer dielectric] layers 214 and 224." EX1008, ¶23. A POSITA would have understood Kim's ILD layer 214 to teach "at least one dielectric layer" and Kim's metal bonding

layer 106 to be the claimed “at least one interconnect layer,” both of which are disposed above the substrate (i.e., above Kim’s active layer 212). Sechen, ¶272.

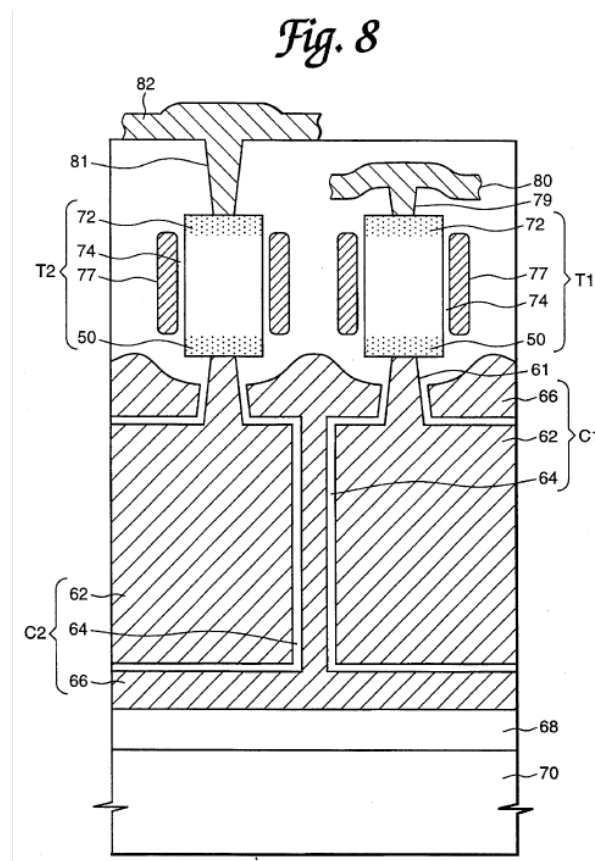
c. 1[b]

The combination of Park and Kim discloses or suggests 1[b]. Sechen, ¶¶273-276. In Kim, a second wafer including active silicon layer 222 with one or memory devices is wafer bonded on top of a first wafer having active IC devices. EX1008, ¶¶20, 22–23, 25. A POSITA would have recognized Kim’s active silicon layer 222 including memory devices on the second wafer, with or without interlayer dielectric layer 224, teaches a “first stackable add-on layer” because the second wafer is stacked on top of the first wafer. Sechen, ¶273.

Further, Park’s semiconductor memory cells include vertical transistors formed from silicon pillars, which are perpendicular with respect to the semiconductor substrate. EX1011, 2:16–25 (“The silicon pillar is extended in a perpendicular (vertical) direction with respect to a semiconductor substrate”), 2:46–56, 1:11–21, Abstract. A POSITA would have understood that because Park’s pillar-shaped transistor stacks the source, drain, and channel regions perpendicular to the substrate, the current flowing through the transistor (i.e., “one or more circuit elements that have characteristics that are voltage variant”) would also be substantially perpendicular to the substrate. Sechen, ¶274. Park further explains that its transistors are incorporated into its DRAM memory cells, which further comprise

a capacitor vertically formed with respect to the transistor. EX1011, 5:33–37, 8:5–23, Figs. 7–9. Thus, a POSITA would have understood Park’s DRAM memory cells to be “vertically oriented.” Sechen, ¶274.

In the combination, the stackable add-on layer (Kim’s top wafer 220) would have a plurality of vertically oriented semiconductor memory cells, as depicted in Park’s Figure 8.



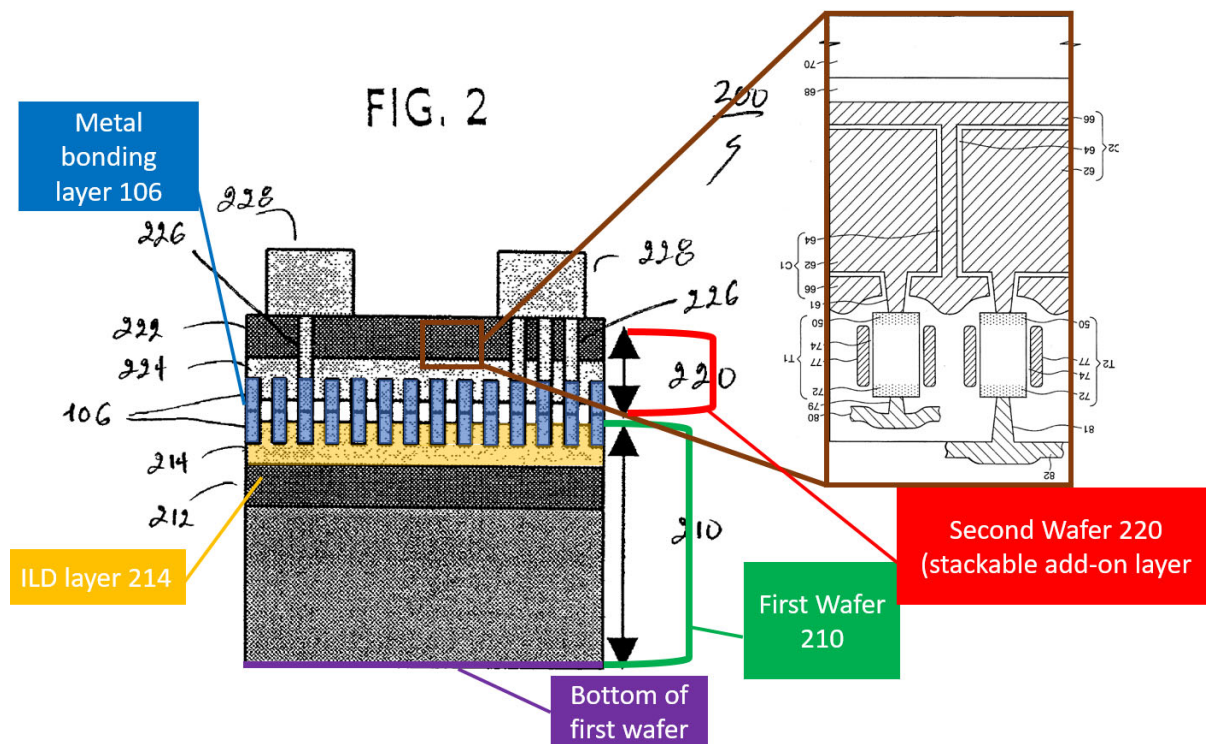
EX1011, Fig. 8; EX1008, ¶¶19–20; Sechen, ¶275.

Finally, Park discloses that each of its vertically structured transistors are “surrounded [] with an insulating film.” EX1011, 2:16–21, 4:9–27 (vertically

oriented transistor surrounded by insulating films 16, 18, 20), Figs. 3, 4:6–8, 5:21–22; Sechen, ¶276. In Park, a dielectric film 64 is also interposed between the plate and storage electrodes of capacitors C1 and C2. EX1011, 5:37–43. Thus, each of Park’s DRAM memory cells is “separated from each other by dielectric material” because both the transistors and capacitors of each memory cell are surrounded by insulating material. Sechen, ¶276. A POSITA would have also understood the need to separate the memory cells with dielectric material for proper operation (e.g., avoiding shorts). *Id.*

d. 1[c]

The combination of Park and Kim discloses or suggests 1[c]. Sechen, ¶¶277–280. In the combination, the bottom wafer (i.e., Kim’s wafer 210 containing one or more microprocessors) would be wafer bonded to the top wafer (i.e., Kim’s wafer 220 containing Park’s vertically oriented DRAM cells) using a metal bonding layer 106. EX1008, ¶¶23–25. The below figure is a schematic representation illustrating how Park’s DRAM cells (brown, schematically represented by Park’s Figure 8), would have been bonded to logic devices on a first wafer (green) using Kim’s teachings (represented by Kim’s Figure 2):



The “stackable add-on layer” (active silicon layer 222 with dielectric 224 (red) in Kim’s Figure 2) containing Park’s vertically-oriented DRAM cells (inserted, brown), is bonded to the ILD layer 214 (orange) of the first wafer via the metal bonding layer 106 (blue). EX1008, ¶¶23–24; Sechen, ¶278. In other words, in the combination, metal bonding layer 106, or alternatively, ILD layer 214 is “a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate.”

A POSITA would have understood “at least one dielectric layer and at least one interconnect layer disposed above the substrate” in 1[a] are both layers “of the substrate,” as recited in 1[c] because 1[a] characterizes the substrate as “having”

those layers. Sechen, ¶279; '702Pat., 5:37–38. Thus, ILD layer 214 and metal bonding layer 106 are each layers “of the substrate.” Sechen, ¶279. Accordingly, a POSITA would have understood that second wafer 220 with active silicon layer 222 and dielectric 224 (“stackable add-on layer”) is bonded, through its own metal bonding layer 106, to metal bonding layer 106 of the first wafer 210 (“a layer of the substrate that is the greatest distance from the substrate as measured from bottom of the substrate” (purple)). *Id.*

A POSITA would have further understood that in the Park-Kim combination schematically represented above, Park’s DRAM cells would be flipped upside down relative to their depiction in Park’s Figure 8 to place Park’s interconnect lines close to the metal bonding layer 106 and accomplish Kim’s stated goal of “shortened [interconnect structure] resulting [in] a faster signal and minimal RC delays.” EX1008, ¶22; Sechen, ¶280. The motivation to combine and reasonable expectation of success for the Park-Kim combination are discussed in Section VII.J.1.a.

e. 1[d]

The combination of Park and Kim discloses or suggests 1[d]. Sechen, ¶281. In the combination, Park’s DRAM memory cells, each with one transistor (EX1011, 2:16–25, 5:20–22, Fig. 8) would be in Kim’s second wafer 220. Sechen, ¶281. The motivation to combine and reasonable expectation of success for the Park-Kim combination are discussed in Section VII.J.1.a.

VIII. THE DISCRETIONARY FACTORS FAVOR INSTITUTION

A. *Fintiv*

Petitioner expects PO will not raise *Fintiv* here because no trial date has been set (EX1029), and the average time to trial in the District of Oregon is 46.3 months (EX1030).

B. *General Plastic*

General Plastic factors 1–3 weigh heavily against exercising discretion to deny institution. This is Petitioner’s first challenge of the ’702 Patent. Micron entities filed IPR2023-00900 challenging only claims 13-17 of the ’702 Patent on May 4, 2023 (less than one month ago). Petitioner here and Micron do not have a substantial relationship, unlike the petitioners in *Valve Corporation v. Electronic Scripting Products, Inc.*, IPR2019-00062, Paper 11, 9 (Apr. 2, 2019) (precedential). For example, unlike in *Valve*, Petitioner and Micron are not co-defendants, their respective district court litigations do not accuse the same product, Petitioner has not sought to join Micron’s prior petition, and Petitioner and Micron do not have a technology licensing agreement. Further, this Petition and the Micron petition do not challenge the same claims (this Petition also challenges independent claim 1).

Importantly, Petitioner filed this Petition before the Preliminary Response to the Micron petition; thus, concerns of road-mapping are not implicated. *NetNut Ltd. v. Bright Data Ltd.*, IPR2021-00465, Paper 11, 7-8 (Aug. 12, 2021); *Code200 v.*

Bright Data Ltd., IPR2022-00861, Paper 18, 5 (Aug. 23, 2022) (precedential, Director Review).

The remaining factors (4–7) also weigh against discretionary denial. Petitioner has diligently worked towards filing this Petition since learning of the asserted prior art, and is filing well in advance of the one-year statutory deadline. Petitioner was in the process of preparing its Petition prior to Micron’s filing, and worked diligently to get this Petition on file quickly thereafter. Finally, the Board will not be unduly burdened by addressing this Petition. *See United Fire Protection Corp. v. Engineered Corrosion Solutions LLC*, IPR2018-00991, Paper 10, 17 (Nov. 15, 2018). To avoid any inefficiency resulting from instituting both this Petition and Micron’s petition, Petitioner is amenable to setting both cases on the same trial schedule or consolidating the cases, if appropriate.

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Parties-in-Interest

Petitioner identifies itself as the real party-in-interest.

B. Related Matters

To the best of Petitioner’s knowledge, only claims 13–17 of the ’702 Patent have been challenged in IPR2023-00900, filed on May 4, 2023 by petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC. In addition, the ’702 Patent is or has been involved in the following

district court litigations:

Name	No.	Court	Filed
<i>BeSang Inc. v. Intel Corporation</i>	3:23-cv-00113-MAH	D. Or.	January 23, 2023
<i>BeSang Inc. v. Micron Technology, Inc. et al</i>	2:23-cv-00028-RG-RSP	E.D. Tex.	January 23, 2023

C. Lead and Backup Counsel

Lead Counsel	Back-Up Counsel
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D. Service Information

Please address all correspondence to lead and back-up counsel at the addresses shown above. Petitioners consent to electronic service by e-mail.

X. FEES

Petitioner concurrently electronically submits the required fees for this Petition. The Board is authorized to charge Arnold & Porter Kaye Scholer LLP's deposit account, No. 50-2387, for any fee deficiency.

Date: June 2, 2023

Respectfully submitted,

/Jessica C. Kaiser/

Jessica C. Kaiser, Lead Counsel

Reg. No. 58,937

CERTIFICATE OF COMPLIANCE

The undersigned hereby certifies that the foregoing Petition for *Inter Partes* Review contains 13,995 words, excluding those portions identified in 37 C.F.R. § 42.24(a), as measured by the word-processing system used to prepare this paper.

/Jessica C. Kaiser/
Jessica C. Kaiser (Reg. No. 58,937)
Lead Counsel

CERTIFICATE OF SERVICE

I certify that on June 2, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 7,378,702 and supporting exhibits to be served via overnight delivery on the Patent Owner at the following correspondence address of record as listed on Patent Center:

Greg L. Martinez
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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel listed below:

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