

Filed on behalf of BeSang Inc.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00991
U.S. Patent No. 7,378,702

PATENT OWNER'S PRELIMINARY RESPONSE

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2002	Docket for <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex.) (as of Sept. 14, 2023)
2003	Docket for <i>BeSang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113 (D. Or.) (as of Sept. 14, 2023)
2004	Defendants' Patent Local Rule 3-3 Disclosure of Invalidity Contentions, <i>BeSang Inc. v. Micron Tech., Inc.</i> , Case No. 2:23-cv-00028 (E.D. Tex. July 11, 2023) (cover pleading)
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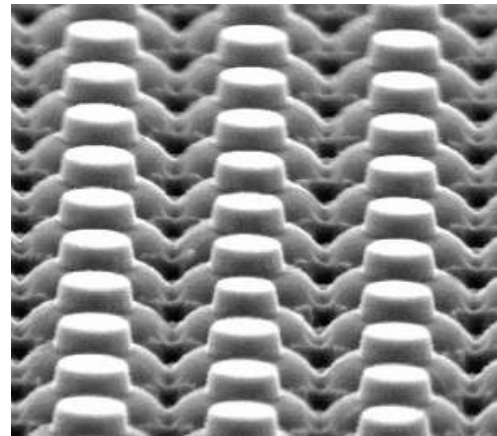
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2016	Andy Patrizio, <i>Impact of Intel and Micron ending their NAND partnership is negligible</i> , Network World (Jan. 12, 2018), https://www.networkworld.com/article/3247746/impact-of-intel-and-micron-ending-their-nand-partnership-is-negligible.html
2017	Intel Corporation’s Invalidity Contentions, <i>BeSang Inc. v. Intel Corp.</i> , Case No. 3:23-cv-00113 (D. Or. July 14, 2023) (cover pleading)
2018	USPTO Assignment Abstract of Title for U.S. Patent Application Publication No. 2003/0157748
2019	U.S. District Courts – Combined Civil and Criminal Federal Court Management Statistics (June 30, 2023), https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-june-2023

I. INTRODUCTION

Patent Owner BeSang Inc. is a pioneering fabless semiconductor company headquartered in Hillsboro, Oregon. BeSang was founded in 2003 with the mission of developing an innovative architecture for 3D memory. By 2008, it had done exactly that.

Collaborating with Stanford University and the National NanoFab Center, in 2008 BeSang achieved “a 3D IC technology breakthrough” by fabricating a 3D IC “on 8-inch wafers with industry standard 0.18 micron CMOS” memory cells “contain[ing] 128 million vertically oriented devices,” as shown at right. EX2005 at 1.



BeSang’s breakthrough received immediate industry praise and put the company on the map. The *EE Times* named BeSang to its prestigious Silicon 60 list of emerging startups. *See infra* § II.A.; EX2007 at 3. The Global Semiconductor Alliance called BeSang a “pioneer” in 3D solutions; *Semiconductor Times* complimented BeSang’s “single-chip, high-density 3D technology provid[ing] a low-cost, high-speed vertical memory solution”; and *Frost & Sullivan* lauded BeSang’s design as having “clear-cut winning edges” over existing technology. *See infra* § II.A.; EX2008 at 17; EX2012 at 1; EX2009 at 1.

Unsurprisingly, the big players in Silicon Valley noticed. Intel, Micron, and others met with BeSang about partnering with, or acquiring, BeSang’s technology. After in-depth discussions and meetings where Micron requested “specific information regarding the technology,” EX2015 at 1-2, and BeSang provided it, *see id.*, Intel and Micron decided to go their own way.

In 2015, Intel and Micron launched their first 3D commercial products, bragging and taking credit for “[t]his new 3D NAND technology, which was jointly developed by Intel and Micron, [and which] stacks layers of data storage cells vertically.” *See infra* § II.A.; EX2006 at 1. They extolled how “[t]his 3D NAND technology has the potential to create fundamental market shifts” and allowed for the “world’s highest-density flash memory.” EX2006 at 1. Their enthusiasm continued with the rollout of their follow-on 3D NAND products in 2018. *See infra* § II.A.; EX2010 at 1-2.

Five years later, after both were accused of patent infringement, Intel and Micron have changed their tune. Now slamming BeSang’s invention with two IPR petitions, they argue that BeSang’s 3D IC architecture would have been obvious. Paper 2 (“Pet.”) at 3; IPR2023-00900, Paper 1 at 3-4. But the 3D IC architecture that Intel and Micron were so eager to acquire was not obvious, and Intel’s Petition should be denied.

Intel's Petition here spans ten separate grounds, based on a collage of six asserted references, to target six patent claims. Pet. at 2-3. These ten grounds are unlikely to prevail for these reasons:

- All Grounds. This is the second challenge in a month to BeSang's patent. Intel's follow-on Petition targets the same Claims 13-17 based on the same Lee and Endoh art. Intel and Micron's longstanding collaboration in the 3D NAND space, shared status as defendants, and request to combine both IPRs on the same trial schedule transparently seek two bites at the apple to challenge the same patent. Intel's second, serial challenge should be denied under Section 314(a) and *General Plastic*.
- All Grounds. Ordering a trial here also is not a good use of Board or party resources under Section 314(a) and *Fintiv*. The same asserted art is at issue in the parallel district court cases. Those litigations are well underway, with the Micron case both forecast and scheduled for a jury trial before the Final Written Decision deadline here.
- Grounds 1A, 1B, 1C, 1D, 2A. Five of the grounds directly rely on claim constructions that Intel repeatedly states are "incorrect." Pet. at 16. The Board has recognized Intel's position fails to satisfy its burden, and Intel cannot credibly ask the Board to proceed with a trial on grounds that Intel itself contends have no merit.

- Grounds 1C, 1E, 1F. Intel’s obviousness combinations based on Lee are rife with hindsight and do not establish the required motivation to combine.
- Grounds 2A, 2B, 2C. Intel’s challenge based on Johnson in Ground 2 is unlikely to prevail because Johnson did not disclose the “dielectric layer” claim limitation. Grounds 2B and 2C further fail because they do not establish any motivation to combine.
- Ground 3. Finally, Ground 3 is unlikely to prevail because Park did not disclose “memory cells separated from each other by dielectric material” as required by unasserted Claim 1.

Intel’s serial and overlapping challenge to the ’702 Patent is a poor use of Board and party resources and is unlikely to prevail. The Board should deny institution and confirm patentability of Claims 1 and 13-17.

II. BACKGROUND

A. Background Of The Invention

Conventional CMOS technology relied on shrinking memory cells to obtain high-capacity storage devices. By the early 2000s, memory devices were approaching the constraints of Moore’s law, the 1965 prediction by Intel’s co-founder that the number of transistors that could be packed into a given area should be expected to double every two years. EX2006 at 1. An outside-the-box solution to further increase capacity was to go vertical. Much like skyscrapers

increasing density by vertically stacking floors as compared to a single-story building, stacking memory cells on top of each other could increase memory density in a given base area without shrinking individual memory cell size.

Compared to the high-temperature devices at the time, BeSang recognized the benefits of manufacturing its 3D integrated circuits at low process temperatures, *i.e.*, below 650°C, including gate oxidation at low temperatures. Among other benefits, BeSang discovered that if the gate dielectric layer has a combination of low temperature thermal oxide, high-K dielectric, and CVD dielectric, then device reliability increases, current-driving capability increases, and on-resistance decreases.

BeSang's innovative 3D IC technology received immediate praise. *Semiconductor Times* explained that "BeSang's 3D technology stacks multi-layer devices within a single chip" and that, "[a]s a result, this single-chip, high-density 3D technology provides a low-cost, high-speed vertical memory solution." EX2012 at 1. Stanford professor Dr. Yoshio Nishi said of BeSang's invention, "Conventional CMOS technology is facing its scaling limits. Therefore, this emerging 3D IC technology will extend the lifespan of CMOS technology, because it is an excellent alternative way to accommodate more devices on a given wafer area." EX2005 at 1. Dr. Simon Sze, the father of CMOS technology who co-invented the floating gate transistor at Bell Labs in 1967, praised "BeSang's

3D IC [as] a very attractive technology” and “one wonders why other companies have not thought about it.” *Id.* at 2.

BeSang’s innovative 3D architecture made the company famous. The following year, the *EE Times* named BeSang to its Silicon 60 list of emerging startups to watch. EX2007 at 3. The Global Semiconductor Alliance called BeSang a “pioneer in the design, development and delivery of unsurpassed three-dimensional (3D) IC solutions.” EX2008 at 17. Market research firm Frost & Sullivan lauded BeSang’s design as having “clear-cut winning edges” over existing technology and providing “freedom to build higher density IC chips by simply adding more layers in 3D directions in a cost-effective manner.” EX2009 at 1-2.

BeSang’s trajectory was not a forgone conclusion. Only a decade before founding BeSang, inventor Sang-Yun Lee immigrated from South Korea with a dream of completing his education in the United States. He first studied for a master’s degree at Washington University in St. Louis, then went on to the Ph.D. program at Arizona State University, eventually earning degrees in electrical engineering from both. After short stints as a low-level engineer at Motorola and Integrated Device Technology, he ventured out on his own in 2003 to found BeSang with the goal of pioneering 3D IC technology.

BeSang has been awarded over 20 U.S. patents for its innovative designs. One of those patents, U.S. Patent No. 7,378,702, is challenged here. The ’702 Patent was

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filed in 2004 and describes BeSang’s 3D IC invention. Titled “Vertical Memory Device Structures,” this foundational patent has been cited by more than 300 patents. The ’702 Patent describes increasing circuit density in ICs by using vertical memory cells to expand the memory array in a third dimension. EX1001 at 3:51-61, Fig. 1. It also teaches placing logic circuitry underneath the memory array to further increase density and achieve faster performance. *Id.* at 5:60-63. This invention not only reduces the cost per bit over existing memory architectures, but also improves reliability. EX2005 at 2.

After BeSang’s breakthrough and with patent applications filed, BeSang’s founder Sang-Yun Lee talked to Intel and Micron about partnering to commercially launch his 3D IC technology. Intel was interested in a joint venture, and Micron discussed acquiring the company. EX1013 ¶ 29; IPR2023-00900, EX1019 ¶¶ 34-35. In 2007, Micron asked BeSang for an “in-depth conversation about [its] technology and business.” EX2014 at 1. After BeSang met with Micron executives in person, Micron “found the technology very interesting” and asked for and received “specific information regarding the technology” including manufacturing details and testing data. EX2015 at 1-2.

Both companies instead decided to create 3D NAND products mimicking BeSang’s idea and introduced their own commercial offerings in 2015. EX2006 at 1-2; *see also* EX2011 (“rather than in prior technologies [that were] trying to cram

. . . more bits on one level of storage, we have now decided to go vertical”). With the launch, Intel and Micron were effusive with their praise of 3D NAND architecture:

- “This 3D NAND technology has the potential to create fundamental market shifts.” EX2006 at 1.
- “3D NAND technology [is] the world’s highest-density flash memory” that can “create storage devices with three times higher capacity than competing NAND technologies.” *Id.*
- The 3D NAND design “enables more storage in a smaller space, bringing significant cost savings, low power usage and high performance to a range of mobile consumer devices as well as the most demanding enterprise deployments.” *Id.*

Intel and Micron’s enthusiasm continued through its launch of more products in 2018:

- Their second-generation 3D NAND architecture “achieves 1 terabit (Tb) density per die, the world’s highest-density flash memory.” EX2010 at 1.
- “These advancements in the cell structure continue the companies’ leadership in producing the world’s highest Gb/mm² areal density.” *Id.*
- “We’re continuing flash technology innovation with our 96-layer structure, condensing even more data into smaller spaces, unlocking the possibilities of workload capability and application construction.” *Id.* at 2.

Just five years later, Intel and Micron challenge BeSang’s invention as obvious. Pet. at 3; IPR2023-00900, Paper 1 at 3-4.

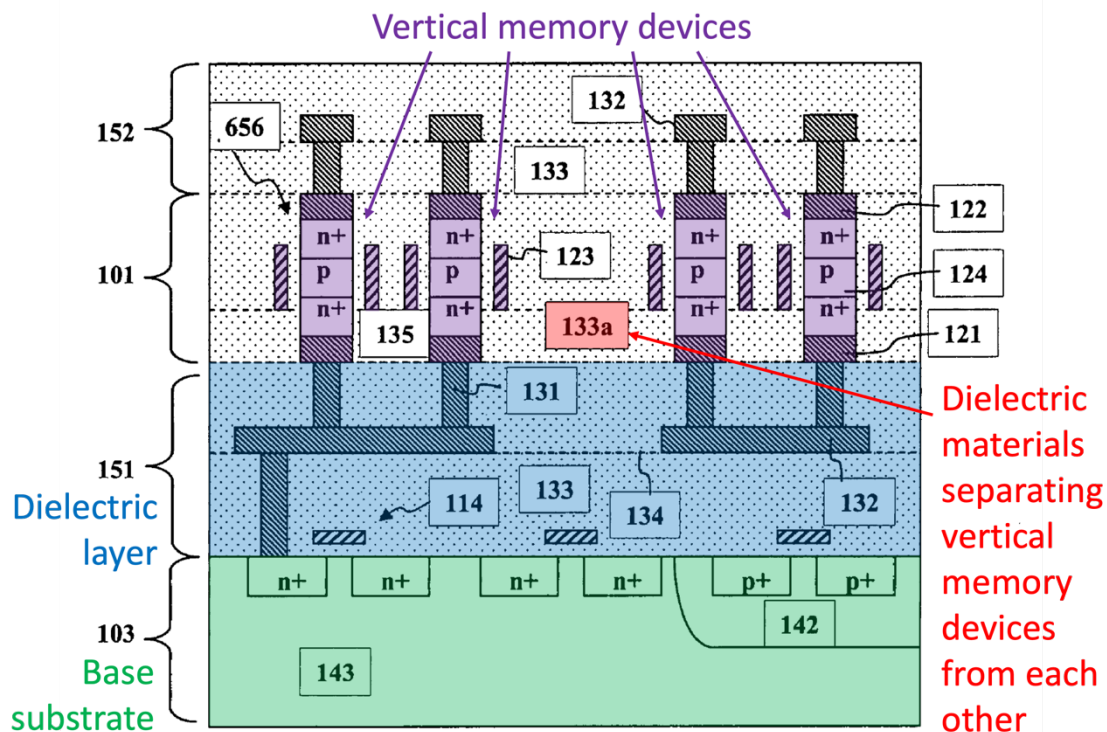
B. The Invention Of The '702 Patent

The '702 Patent is titled “Vertical Memory Device Structures.” The patent innovated by solving the significant practical challenges posed by scaling 2-dimensional memory technologies.

The '702 Patent recognized the need for “structures and methods that are suitable for providing increased circuit density in integrated circuits without necessarily requiring devices to be made smaller.” EX1001 at 1:40-43. It describes the use of vertical memory cells, which allows the memory array to expand in a third dimension, as well as putting logic circuitry underneath the memory array, which further increases density and helps achieve faster performance. *Id.* at 3:51-61, 5:60-63, Fig. 1.

Figure 1 of the '702 Patent, reproduced below, shows “vertical memory devices 656” that “are separated by isolation 135 and have floating structures in the filled dielectric materials 133a.” *Id.* at 5:18-21. Dielectric materials are those that are substantially nonconducting.

Fig. 1



Id. at Fig. 1 (annotated).

As shown in Figure 1, the vertical memory devices are separated from each other by dielectric materials 133a. *See id.* at 1:54-56 (“The regions around and between the vertically oriented memory devices, or cells may have dielectric material disposed therein.”), 6:6-8 (“Various embodiments of the present invention provide floating devices that are separated by dielectric isolation regions.”). Also shown in Figure 1 is dielectric layer 151 located above base substrate 103, *id.* at

5:37-38, which can include electrical devices, such as transistors, *see, e.g., id.* at 10:8-9 (“The select transistors may be placed in base substrate 103....”).

C. U.S. Patent Application Publication No. 2002/0028541 (“Lee”)

Lee disclosed “a monolithic three dimensional array of charge storage devices which includes a plurality of device levels, wherein at least one surface between two successive device levels is planarized by chemical mechanical polishing.” EX1007 at Abstract. Lee explained that “[t]he term ‘monolithic’ means that layers of each level of the array were directly deposited on the layers of each underlying level of the array.” *Id.* ¶ 107. Lee stated that “monolithic” devices “improv[e] device density” as opposed to “two dimensional arrays [that] may be formed separately and then packaged together to form a non-monolithic device.” *Id.* Lee’s disclosure is substantively identical to the issued Lee patent Micron relies on in its earlier IPR challenge to the ’702 Patent. *Compare* EX1007 with IPR2023-00900, EX1007.

Intel asserts invalidity based on Lee both here and in the co-pending litigation. EX2017 at 18, 22.

D. U.S. Patent Application Publication No. 2003/0157748 (“Kim”)

The Petition relies on Kim as a secondary reference for a subset of the Petition’s grounds (Grounds 1C, 1D, 2B, and 3). Pet. at 3. Kim discloses “[a] method of vertically stacking wafers ... to form [a] three-dimensional (3D) wafer stack.” EX1008 at Abstract. Kim’s “wafer stack” or “non-monolithic device”

includes “selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers; [and] bonding the adjacent wafers, via the metallic lines” *Id.*

Kim is used to assert invalidity both here and in the co-pending litigation. EX2017 at 19, 22.

E. The Generic Nature Of The Smart-Cut® Process For Thin Film Transfer (“Aspar”)

The Petition asserts Aspar as a secondary reference for a subset of the Petition’s grounds (Grounds 1E, 1F, and 2C). Pet. at 3. Similar to Kim, Aspar taught a “Smart-Cut® process,” which permitted “transfer of a thin layer from the substrate A onto the support B” to effect wafer stacking, which “is particularly advantageous when a thin monocrystalline layer is required on a support which does not allow epitaxy of this layer.” EX1009 at 1.

Intel relies on Aspar to argue invalidity both here and in the co-pending litigation. EX2017 at 19, 22.

F. U.S. Patent No. 6,034,882 (“Johnson”)

Johnson is asserted against Claim 13 in each of Grounds 2A-2C. Pet. at 3. As shown in Figure 4(b), Johnson was directed to a cross-point memory architecture where memory cells reside at the intersection of word lines and bit lines. Johnson disclosed the “fabrication sequence” for a memory cell in Figures 6(b)-6(g), EX1010 at 12:42-43, but Johnson did not depict a dielectric layer in these figures or explain the relationship between any dielectric layer and other portions of the device.

Intel argues invalidity based on Johnson both here and in the co-pending litigation. EX2017 at 18, 22.

G. U.S. Patent No. 5,571,730 (“Park”)

The Petition relies on Park solely for its Ground 3 challenge to Claim 1. Pet. at 3. Park disclosed memory cells that share gate electrodes with no separation between adjacent cells. *See, e.g.*, EX1011 at 5:49-53, Figs. 7, 9.

Park is used to assert invalidity both here and in the co-pending litigation. EX2017 at 17.

H. U.S. Patent Application Publication No. 2002/0154556 (“Endoh”)

The Petition relies on Endoh as a secondary reference for a subset of the Petition’s grounds (Grounds 1B, 1D, and 1F) and solely for challenged dependent Claims 16 and 17. Pet. at 3.

Intel asserts invalidity based on Endoh both here and in the co-pending litigation. EX2017 at 18, 22.

I. Co-Pending Litigation On The ’702 Patent

In January 2023, BeSang filed suit asserting the ’702 Patent against Intel and Micron. *BeSang Inc. v. Intel Corp.*, No. 3:23-cv-00113 (D. Or.); *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex.). Both the Intel and Micron litigations are quickly advancing. By the time the Board is expected to issue its institution decision, the parties in the Intel case will have exchanged infringement

and invalidity contentions. EX2003 at 4 (case schedule in Docket Entry 45). A jury in the Micron case will decide validity before any Final Written Decision here, with the median time to trial in the Eastern District of Texas predicting a June 2024 trial date, preceding the November 18, 2024 scheduled trial date. EX2019 at 35; EX2001 at 1. Neither of the co-pending district court actions are stayed due to IPR.

III. LEVEL OF ORDINARY SKILL IN THE ART

For purposes of denying institution and finding that Intel has not met its burden to show a reasonable likelihood of prevailing, BeSang submits that the Board need not determine the level of ordinary skill in the art. *Johnson & Johnson Surgical Vision, Inc. v. Alcon Inc.*, IPR2021-01003, 2021 WL 6338373, at *4 (P.T.A.B. Nov. 23, 2021) (denying institution: “For our analysis on whether to institute, we need not determine the level of ordinary skill in the art”).

BeSang reserves the right to address the level of ordinary skill in the event the Board institutes trial.

IV. CLAIM CONSTRUCTION IS NOT NECESSARY TO DENY INSTITUTION HERE

Intel addresses in the Petition the construction of the terms “stackable add-on layer being bonded” (Claim 13) and “SOI pillar” (Claims 14-17). *See* Pet. at 10-16. But in several of the Petition’s grounds, Intel relies on proposed constructions it expressly says are incorrect. *See infra* § VI.A.

For purposes of denying institution and finding that Intel has not met its burden to show a reasonable likelihood of prevailing, BeSang submits that the Board need not construe any terms of the challenged claims but instead can take Intel’s representations at face value. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe ‘only those terms... that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). BeSang reserves the right to assert claim construction positions if trial is ordered.

V. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION

As a threshold matter, the Board should exercise its discretion to deny institution of *inter partes* review under 35 U.S.C. § 314(a). This IPR is the second, serial IPR challenge to the ’702 Patent and overlaps with the patentability disputes raised in the parallel district court proceedings. Both the *General Plastic* and *Fintiv* factors counsel against instituting review here.

A. The Board Should Deny Institution Under Section 314(a) Because The *General Plastic* Factors Support Denial

The Board should deny institution of this second Petition under 35 U.S.C. § 314(a) because Intel’s serial attack on the same patent challenged in IPR2023-00900 favors denying institution. *See General Plastic Indus. Co., Ltd. v.*

Kaisha, IPR2016-01357, 2017 WL 3917706, at *4-9 (P.T.A.B. Sept. 6, 2017) (precedential).

1. Factor 1: Whether the same petitioner previously filed a petition directed to the same claims of the same patent.

The relationship between Intel and Micron supports denying Intel’s second Petition. On May 4, 2023, Micron filed an IPR petition challenging the ’702 Patent. *See* IPR2023-00900, Paper 1 (“Micron Petition”). About a month later, Intel filed this Petition. Pet. at 95. “[W]hen different petitioners challenge the same patent, [the Board] consider[s] *any relationship* between those petitioners when weighing the *General Plastic* factors.” *Valve Corp. v. Elec. Scripting Prods., Inc.*, IPR2019-00062, 2019 WL 1490575, at *4 (P.T.A.B. Apr. 2, 2019) (emphasis added) (precedential).

Intel and Micron plainly have a relationship that supports denial under *General Plastic* factor 1. They jointly developed the same 3D NAND memory technology accused in the parallel litigation. *See* EX1013; IPR2023-00900, EX1019. Intel and Micron publicly acknowledged “their long-term joint development partnership for 3D NAND memory.” EX2016 at 1; *see also* EX2010. Both are also defendants in co-pending litigation accused of infringing the ’702 Patent, with an identical interest in avoiding liability for infringement. Factor 1 thus favors denial. *See, e.g., Valve*, 2019 WL 1490575, at *5 (“significant relationship

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between Valve and HTC with respect to Patent Owner’s assertion of the ’934 patent” favors denying institution).

Intel’s enthusiasm for “setting both cases on the same trial schedule or consolidating the cases,” Pet. at 93, exposes that Intel and Micron are coordinating their attacks on the ’702 Patent and further supports denial under factor 1. *See, e.g., Fresenius Kabi USA, LLC v. Amgen, Inc.*, IPR2019-00971, 2019 WL 5232647, at *3 (P.T.A.B. Oct. 16, 2019) (“the first *General Plastic* factor weighs in favor of denying institution” where petitioner was “willing to coordinate” its IPR with another petitioner’s challenges “to facilitate joint consideration by the Board”).

Finally, the substantial overlap between the patent claims challenged by both petitions supports denial. Both petitions target asserted Claims 13-17. *Compare* Pet. at vi-vii (challenging Claims 1 and 13-17) *with* Micron Petition at 3-4 (challenging Claims 13-17). This Petition challenges Claim 1 too, but Claim 1 shares many of the same limitations as Claim 13. *See* Pet. at vi (setting forth limitations in Claims 1 and 13). Intel is not entitled to an additional trial simply by throwing in an extra, extraneous claim never asserted in the parallel litigations. *See, e.g., PayPal, Inc. v. IOENGINE, LLC*, IPR2019-00884, 2019 WL 4897039, at *5 (P.T.A.B. Oct. 3, 2019) (“the existence of the non-overlapping claims is not substantial enough to tip the first factor to favor instituting trial”).

The significant relationship between Intel and Micron strongly favors denying institution of Intel’s duplicative challenge under factor 1.

2. Factor 2: Whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it.

Factor 2 also strongly supports denying Intel’s follow-on Petition. Here Intel recycles Micron’s asserted art from the first petition. Both petitions assert unpatentability based on Endoh and Lee. *See* Pet. at 2-3 (relying on Endoh and U.S. Pat. Appl. Pub. No. 2002/0028541 to Lee); Micron Petition at v, 3-4, 11 (relying on Endoh and U.S. Patent No. 6,881,994 to Lee, including its prior publication date). Intel’s decision to cite the Lee publication instead of the issued Lee patent that Micron submitted cannot distinguish its Petition, since the Lee publication and issued patent have the same disclosure. *Compare* EX1007 with IPR2023-00900, EX1007.

Intel was well aware of Endoh and Lee when Micron filed its first petition. Intel doesn’t dispute its awareness of these references before Micron’s filing, *see* Pet. at 92-93, instead conceding it “was in the process of preparing its Petition prior to Micron’s filing, and worked diligently to get this Petition on file quickly thereafter,” *id.* at 93. Intel’s knowledge of Endoh and Lee when Micron filed its petition supports denying institution under factor 2. *See, e.g., Valve*, 2019 WL 1490575, at *5 (“Valve knew or should have known of the Welch-HiBall reference

around the time HTC filed its petition in the 1031 IPR because it was one of the two references relied upon by HTC.”).

Intel presumably also was aware of all the art it cites in the Petition at the time of Micron’s earlier petition since Intel “was in the process of preparing its Petition *prior to* Micron’s filing.” Pet. at 93 (emphasis added); *see also id.* (“Petitioner has diligently worked towards filing this Petition since learning of the asserted prior art”).

Factor 2 “includes considering whether the prior art relied on in the later petition ‘could have been found with reasonable diligence.’” *Valve*, 2019 WL 1490575, at *5. Despite Intel’s unsupported attorney argument that it worked diligently “since learning of the asserted prior art,” Pet. at 93, Intel never discloses when it learned of the asserted art. Intel never disputes it easily could have found all of the cited references “through the exercise of reasonable diligence around the time of [Micron]’s petition.” *Valve*, 2019 WL 1490575, at *5; *see* Pet. at 92-93. Locating all of the art wouldn’t have taken much effort. For example, Johnson was cited on the face of Micron’s Lee patent, and Kim is a patent application assigned to Intel itself. IPR2023-00900, EX1007 at 2 (citing “6,034,882 [to] Johnson et al.”); EX2018 at 1 (“20030157748” assigned to “Intel Corporation”). Delays in searching for prior art do not justify a second trial. *See, e.g., Valve*, 2019 WL 1490575, at *5 (“[B]y its own admission, Valve began preparing its petitions on or after August 16,

2018, and filed them less than two months later, which indicates that Valve found the Maeda and Anderson references quickly.”).

Factor 2 supports denying institution.

3. Factor 3: Whether at the time of filing of the second petition the petitioner already received the patent owner’s preliminary response to the first petition or received the Board’s decision on whether to institute review in the first petition.

Intel plainly benefitted from Micron’s earlier petition, which provided Intel with a strategic advantage. Intel’s Petition also relies on the Endoh and Lee references and presents similar arguments to Micron’s challenge. *E.g., compare* Pet. at 16-31 (Ground 1A challenge to Claim 13) *with* Micron Petition at 46-54 (Ground 3 challenge to Claim 13). These similarities show Intel benefitted from filing second and support denying institution of Intel’s follow-on petition. *See, e.g., Fresenius*, 2019 WL 5232647, at *4 (“a significant portion of the arguments and contentions in the present Petition are similar to those in Adello’s petition ... which supports Amgen’s position that Fresenius benefited from Adello’s petition”).

Factor 3 also weighs against institution.

- 4. Factors 4 and 5: The length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition; and whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent.**

“*General Plastic* factors four and five focus on the period of delay and any excuse for that delay.” *PayPal*, 2019 WL 4897039, at *7. Intel never explains or excuses its delayed filing because Intel never specifies when it actually “learned of the asserted prior art,” leaving the Board unable to “determine, with any certainty, the length of time that elapsed between when Petitioner learned of the asserted prior art and the filing of the Petition.” *United Fire Prot. Corp. v. Engineered Corrosion Sols., LLC*, IPR2018-00991, 2018 WL 6016749, at *7 (P.T.A.B. Nov. 15, 2018). Thus, factor 4 is neutral. *Id.*

Regarding factor 5, Intel asserts that it “was in the process of preparing its Petition prior to Micron’s filing,” Pet. at 93, but does not otherwise “provide any explanation related to the timing of filing its Petition in relation to the petition” filed in IPR2023-00900. *United Fire*, 2018 WL 6016749, at *7. Accordingly, factor 5 supports denying institution. *Id.*

5. Factors 6 and 7: The finite resources of the Board; and the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review.

“The sixth and seventh factors are efficiency considerations.” *Valve*, 2019 WL 1490575, at *7. “[O]ne petition should be sufficient to challenge the claims of a patent in most situations.” Consolidated Trial Practice Guide at 59 (Nov. 2019). Here, factors 6 and 7 weigh against institution because “[t]wo or more petitions filed against the same patent at or about the same time ... may place a substantial and unnecessary burden on the Board and the patent owner and could raise fairness, timing, and efficiency concerns.” *Id.*

Intel’s assertion that it is “amenable to setting both cases on the same trial schedule or consolidating the cases,” Pet. at 93, shows that Intel unfairly seeks a second bite at the apple to challenge the ’702 Patent claims. Instituting trial on both this Petition and Micron’s petition in IPR2023-00900 would be an inefficient use of Board and party resources. *See, e.g., Applied Materials, Inc. v. Demaray LLC*, IPR2021-00105, 2021 WL 1923420, at *4 (P.T.A.B. May 12, 2021) (“[W]e disagree with Petitioner that the Board has routinely instituted two parallel petitions”); *see also* Consolidated Trial Practice Guide at 59 (“[A] substantial majority of patents have been challenged with a single petition.”).

Intel’s serial second petition should therefore be denied.

6. The *General Plastic* Factors Favor Denying Institution.

The *General Plastic* factors weigh in favor of the Board exercising its discretion to deny review of Intel’s second challenge to the ’702 Patent. Trials on both of these duplicative challenges is unwarranted.

B. The Board Also Should Deny Institution Under Section 314(a) Because The *Fintiv* Factors Support Denial

The Board should also discretionarily deny institution under 35 U.S.C. § 314(a) because none of the *Fintiv* factors support proceeding with a trial here. *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, 2020 WL 2126495, at *2 (P.T.A.B. Mar. 20, 2020) (precedential); *see also Mylan Labs. Ltd. v. Janssen Pharmaceutica NV*, IPR2020-00440, 2020 WL 5580472, at *11 (P.T.A.B. Sept. 16, 2020) (“No factors in our analysis weigh towards institution.”). Intel does not seriously dispute this, acknowledging *Fintiv* but pointedly declining to address it, *see* Pet. at 92, despite a jury deciding the overlapping patentability challenges presented here before any Final Written Decision.

1. Factor 1: Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted.

Fintiv factor 1 is neutral. Intel stated it will seek a stay of the parallel litigation pending the Board’s institution decision, but it has not filed a motion and the district court has not stayed the case pending IPR. *See, e.g., Code200 v. Luminati Networks Ltd.*, IPR2020-01266, 2020 WL 7682243, at *3 (P.T.A.B. Dec. 23, 2020) (factor

neutral where the district court had not yet ruled on petitioner’s opposed stay motion filed after the IPR petition was filed). The Oregon court’s brief stay to decide an expedited motion does not change the analysis. *See, e.g., Ethicon, Inc. v. Bd. of Regents*, IPR2019-00406, 2020 WL 3088846, at *4 (P.T.A.B. June 10, 2020) (factor neutral because “[a]lthough the Western District of Texas did institute a stay for a discrete period of time, that stay was lifted”). Similarly, the district court in the parallel Texas case has not ruled on Micron’s opposed stay motion pending IPR. EX2002 at 3-6.

2. Factor 2: The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.

Intel’s assertion that “no trial date has been set,” Pet. at 92, overlooks that Micron’s co-pending litigation in Texas will undoubtedly go to trial first. The median time to trial in the Eastern District of Texas predicts a June 2024 civil trial date—six months before the anticipated Final Written Decision deadline here. EX2019 at 35 (16.7 months median time from filing to trial); Paper 3; *see also* Director’s Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022), at 8-9. The November 18, 2024 trial date is also before the statutory deadline. EX2001 at 1.

This earlier Texas trial date tips factor 2 in favor of discretionary denial. *See, e.g., TCO AS v. NCS Multistage Inc.*, PGR2020-00077, 2021 WL 662165, at *5

(P.T.A.B. Feb. 18, 2021) (“Although the TCO litigation is set for a month after our projected due date of the final written decision, we determine that the Nine litigation weighs more heavily toward exercising discretion to deny institution because it will resolve all of the same invalidity issues that are presented in the Petition.”); *Fitbit, Inc. v. Philips N. Am. LLC*, IPR2020-00828, 2020 WL 6470312, at *4-5 (P.T.A.B. Nov. 3, 2020) (trial date in a parallel Garmin case before final written decision deadline was “relevant” and “weighs in favor of invoking our discretion to deny institution” of Fitbit’s petition).

3. Factor 3: Investment in the parallel proceeding by the court and the parties.

The co-pending district court cases have been moving forward since January 2023. In the Texas case, infringement and invalidity contentions have been exchanged, and discovery and depositions are underway. EX2001 at 5. By the Board’s institution deadline on December 14, 2023, *see* Paper 3, the parties will be in the home stretch of discovery. EX2001 at 3 (showing completion of fact discovery by June 12, 2024). Likewise, in the Oregon case, the parties will have exchanged infringement and invalidity contentions. EX2003 at 4 (case schedule in Docket Entry 45).

Based on the considerable resources already expended on contentions and discovery in the district court, *Fintiv* factor 3 weighs “in favor of denying

institution.” *See, e.g., TCO*, 2021 WL 662165, at *5-6 (as of the preliminary response filing, the parties had “exchanged infringement contentions and invalidity contentions and exchanged substantial document productions”).

4. Factor 4: Overlap between issues raised in the petition and in the parallel proceeding.

Intel’s invalidity contentions in the co-pending Oregon case challenge asserted Claims 13, 14, and 16, based on the identical Lee, Kim, Aspar, Johnson, Park, and Endoh references cited in the Petition. EX2017 at 2, 17-19, 22. The parallel Texas litigation addresses Claims 13-16 based on the same references. EX2004 at 1, 5-7, 9-10. Thus, “the patentability disputes before the [district courts] will resolve all or substantially all of the patentability disputes between the parties,” including whether Claim 13, the only asserted independent claim, is patentable. *SK Innovation Co., Ltd. V. LG Chem, Ltd.*, IPR2020-00991, 2020 WL 7029919, at *7 (P.T.A.B. Nov. 30, 2020).

Despite the overlap in issues raised in the Petition and at the district court, Intel decided not to provide any stipulation, much less a *Sotera* stipulation, to eliminate the duplication, which weighs strongly in favor of denying institution of this Petition. *See, e.g., KeyMe, LLC v. Hillman Grp., Inc.*, IPR2020-01028, 2021 WL 129094, at *6 (P.T.A.B. Jan. 13, 2021) (factor supports denial because “Petitioner fails to stipulate that it will not pursue in the district court any ground

raised or that could have reasonably been raised in this proceeding”); *Code200*, 2020 WL 7682243, at *4 (factor “strongly favors” denial notwithstanding that “the Petition challenges four claims that are not asserted in the Texas Litigation”).

5. Factor 5: Whether the petitioner and the defendant in the parallel proceeding are the same party.

Intel is both the Petitioner here and the defendant in the parallel Oregon litigation. As discussed in connection with *General Plastic* factor 1 above, Intel is a former business partner that is closely aligned with Micron, the defendant in the parallel Texas proceeding. *See supra* § V.A.1. “Even when a petitioner is unrelated to a defendant, ... if the issues are the same as, or substantially similar to, those already or about to be litigated, or other circumstances weigh against redoing the work of another tribunal, the Board may, nonetheless, exercise the authority to deny institution.” *Fintiv*, 2020 WL 2126495, at *6. Factor 5 supports denying institution.

6. Factor 6: Other circumstances that impact the Board’s exercise of discretion, including the merits.

Where “the Board’s analysis of *Fintiv* factors 1-5 favors denial of institution, the Board shall then assess compelling merits.” *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, 2023 WL 2237986, at *2 (P.T.A.B. Feb. 27, 2023). As explained, Intel’s patentability challenge is deeply flawed because the Petition fails to show obviousness for any ground, and Intel even asserts that several of the Petition’s grounds are unlikely to prevail. The weakness of the Petition’s merits

heavily favors discretionary denial. *See, e.g., Code200*, 2020 WL 7682243, at *5 (“[W]e do not find that the merits outweigh the other *Fintiv* factors favoring denial of institution.”); *Fitbit*, 2020 WL 6470312, at *9 (“[T]he merits of the proceeding weigh in favor of denying institution....”).

7. None Of The *Fintiv* Factors Supports Institution

The weight of the *Fintiv* factors supports the Board exercising its discretion to deny review under Section 314(a) here, thereby conserving Board and party resources and preventing duplicative proceedings evaluating the same invalidity challenges against the same patent. None of the six *Fintiv* factors supports institution here.

VI. THE PETITION’S CHALLENGES ARE NOT REASONABLY LIKELY TO PREVAIL

Even if the Board declines to discretionarily deny institution under *General Plastic* or *Fintiv*, it should deny institution on the merits.

Trial is not warranted because the Petition fails to show a reasonable likelihood of prevailing on any of the various 10 grounds. Five grounds (1A, 1B, 1C, 1D, 2A) rely on constructions that Intel states are “incorrect,” thus admitting that Intel itself contends they are unlikely to prevail. The remaining grounds are also unlikely to prevail. Grounds 1C, 1E, and 1F fail to show a motivation to combine, and are riddled with improper hindsight bias. Johnson in Grounds 2A, 2B, and 2C did not disclose the claimed “dielectric layer,” and Grounds 2B and 2C are also

lacking a motivation to combine. Finally, Ground 3 will not succeed because Park did not disclose the “memory cells separated from each other by dielectric material” claim limitation.

A. Five Grounds Are Unlikely To Prevail Because They Rely On “Incorrect” Claim Constructions

Five of the ten grounds are deficient on their face because they rely on claim constructions that Intel itself argues are “incorrect.” Pet. at 16. “Having proposed constructions it alleges are incorrect, Petitioner is unlikely to prove in a trial that those constructions are correct.” *Ebates Performance Mktg., Inc. v. Int’l Bus. Machs. Corp.*, IPR2022-00439, 2022 WL 5048425, at *5 (P.T.A.B. Oct. 3, 2022). Intel cannot reasonably ask the Board to invest in a trial based on grounds that Intel itself refuses to defend.

1. Intel Both Bears The Burden Of Proof To Provide A Claim Construction And To Show Unpatentability Based On That Construction

Under Board rules, Intel bears the burden to show “[h]ow the challenged claim is to be construed” and “[h]ow the construed claim is unpatentable.” 37 C.F.R. § 42.104(b)(3)-(4). “In an *inter partes* review, the burden of persuasion is on the petitioner to prove unpatentability by a preponderance of the evidence, and that burden never shifts to the patentee.” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (internal citations and quotations omitted). If Intel itself

argues that a ground is not plausible when it bears the burden of proof on that ground, it cannot possibly carry its burden.

Following its rules, the Board has denied institution of petitions that asserted unpatentability under admittedly incorrect claim constructions. *See, e.g., Hologic, Inc. v. Enzo Life Scis., Inc.*, IPR2018-00019, 2018 WL 1897623, at *3-4 (P.T.A.B. Apr. 18, 2018); *Ebates*, 2022 WL 5048425, at *5.

2. Grounds 1A, 1B, 1C, 1D, And 2A Are Improperly Keyed To Claim Constructions Intel Says Are Incorrect

At the outset of the Petition, Intel lays out its proposed constructions of two claim terms: “stackable add-on layer being bonded” (Claim 13) and “SOI pillar” (Claims 14-17). *See* Pet. at 10-16. Then the Petition changes course and relies on constructions of the same claim terms that Intel says are “incorrect” in five of the Petition’s grounds. *Id.* at 16. Specifically:

Ground 1A. Instead of relying on the constructions it proposed to argue unpatentability of Claims 13-17, Intel proffers other constructions of “stackable add-on layer being bonded” and “SOI pillar” that it says are “incorrect.” *Id.* at 16 (“Such constructions are incorrect, but under them, claims 13-17 would have been obvious over Lee.”); *see also* EX1003 at ¶¶ 71-92 (Intel’s expert: opining that these constructions are allegedly incorrect with supporting analysis). Then it argues unpatentability based on those “incorrect” constructions. *See* Pet. at 16-41.

Ground 1B. This Ground relies on the same constructions of “stackable add-on layer being bonded” and “SOI pillar” in Ground 1A that Intel said were “incorrect.” *Id.* at 16; *see also id.* at 41-42.

Grounds 1C and 1D. The Ground 1C challenge to Claims 14-17 and Ground 1D rely on the same construction of “SOI pillar” in Ground 1A that Intel said was “incorrect.” *Id.* at 16; *see also id.* at 50, 55.

Ground 2A. This Ground relies on the same construction of “stackable add-on layer being bonded” in Ground 1A that Intel said was “incorrect.” *Id.* at 16; *see also id.* at 65.

3. The Board Does Not Institute Trial For Petitions Based On Allegedly Incorrect Claim Constructions

Because Intel asserts the constructions on which it relies are incorrect, it cannot credibly ask the Board to embark on a trial based on those constructions. This falls far short of Intel’s burden to show “[h]ow the challenged claim is to be construed” and “[h]ow the construed claim is unpatentable.” 37 C.F.R. § 42.104(b)(3)-(4). Institution should be denied on this basis.

Indeed, the Board has denied institution for this very reason. *See Hologic*, 2018 WL 1897623, at *3-4. In *Hologic*, the petition identified “how Petitioner believe[d] the challenged claims should be construed” but did “not explain how the challenged claims are unpatentable *as so construed*.” *Id.* at *3. Instead, the *Hologic*

petition argued “how the challenged claims would be unpatentable if they are given a different construction, namely one that Petitioner consider[ed] to be erroneous.”

Id. The Board denied institution, explaining that “[b]ecause the Petition does not map the challenged claims, as Petitioner considers them to be correctly construed, to the asserted prior art, there is not a reasonable likelihood that Petitioner would prevail” *Id.* at *4.

“Having proposed constructions it alleges are incorrect, Petitioner is unlikely to prove in a trial that those constructions are correct.” *Ebates*, 2022 WL 5048425, at *5 (denying institution). “The Board is under no obligation to subject a patent owner to the burden and expense of discovery and trial where a petition asserts patentability challenges that are keyed to an incorrect claim construction.” *United Microelecs. Corp. v. Lone Star Silicon Innovations LLC*, IPR2017-01513, 2018 WL 2338800, at *2 (P.T.A.B. May 22, 2018) (denying institution).

In addition to not satisfying its burden to show unpatentability under supported claim constructions, Intel’s tactics also run afoul of the Board’s Consolidated Trial Practice Guide requiring that a “petitioner must include a statement identifying a proposed construction of the particular term *and where the intrinsic and/or extrinsic evidence supports that meaning.*” Consol. Trial Practice Guide at 44 (emphasis added). Not only does the Petition assert constructions that Intel says are unsupported by the evidence, but in failing to provide support for them,

Intel’s Petition violates the Consolidated Trial Practice Guide. Instead of support, Intel provides the opposite—submitting expert testimony disavowing the constructions it says are “incorrect.” *See, e.g.*, Pet. at 16 (arguing constructions of “stackable add-on layer being bonded” and “SOI pillar” that are “incorrect”); EX1003 ¶ 84 (Intel’s expert: rejecting construction of “bonded” and stating: “I have reviewed the intrinsic record of the ’702 patent, and it does not support such a construction”); *id.* ¶ 92 (same opinion for construction of “SOI pillar”).

The Board should reject Intel’s improper invitation to evaluate unpatentability based on constructions that Intel contends are “incorrect.” *See, e.g., Ebates*, 2022 WL 5048425, at *5 (“[W]e decline to adopt and apply allegedly incorrect constructions, even if it might be possible to apply prior art to such incorrect constructions”). Institution should be denied.

B. Grounds 1C, 1E, And 1F Do Not Meet Their Burden To Show A Motivation To Combine And Are Not Reasonably Likely To Prevail

Grounds 1C and 1E are not reasonably likely to prevail because the Petition never shows it would have been obvious to combine the teachings of Lee with those of Kim or Aspar. Because Ground 1F relies on Ground 1E, *see* Pet. at 64, it fails for the same reason.

To combine Lee with Kim or Aspar, the Petition inaccurately says that Lee provides no teaching on how layers are added, requiring resort to Kim or Aspar. But

Lee does provide such teaching, and even if it didn't, the Petition provides no reason to modify Lee's monolithic array. The Petition's inaccuracies and failure to articulate a rationale show its obviousness argument is unlikely to prevail.

Neither Ground 1C nor 1E assert that Lee disclosed "the stackable add-on layer being bonded" as required by limitation 13[c]. *See id.* at 51-54, 56-63. Instead, both Grounds 1C and 1E rely on "wafer bonding" for Claim 13's bonding requirement. *See id.* Ground 1C relies on Kim and asserts that one of skill in the art "would have been motivated to apply Kim's wafer bonding teachings to implement Lee's Figure 35 memory device as a non-monolithic one." *Id.* at 52. Similarly, Ground 1E relies on Aspar and asserts that one of skill in the art "would have been motivated to use Aspar's Smart-Cut® process," which the Petition contrasts with "monolithic deposition," "to wafer bond bottom level 3104 ('stackable add-on layer') to insulating layer 3102 ('dielectric layer') of Lee's Figure 35." *Id.* at 60-61.

However, the Petition's premise for combining Lee with wafer bonding techniques from Kim (Ground 1C) and Aspar (Ground 1E) is inaccurate. Both Grounds 1C and 1E incorrectly assert that Lee does not "describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102" and that "[c]onsequently, a POSITA would have looked to" other art, such as Kim and Aspar, "for details about attaching bottom level 3104 to insulating layer 3102." *Id.* at 51, 56. But the Petition acknowledges in both grounds that, "[i]n Lee, each level

3104 is **deposited** on the underlying level of array 3101.” *Id.* at 51, 56 (emphasis added) (citing EX1007 ¶ 107). The cited passage in Lee disclosed “a monolithic three dimensional array of charge storage devices comprising a plurality of device levels” and explained that “[t]he term ‘monolithic’ means that layers of each level of the array were directly deposited on the layers of each underlying level of the array.” EX1007 ¶ 107.

Indeed, Lee disclosed a monolithic array. *See, e.g., id.* at Abstract (“There is provided a monolithic three dimensional array of charge storage devices which includes a plurality of device levels”), ¶ 111 (Figure 35: “The array of charge storage logic or memory devices 3101 are thus arranged as a three dimensional monolithic array....”). Describing Figure 35, Lee also disclosed that “[t]he array 3101 has a plurality of device levels 3104, preferably separated by interlayer insulating layers.” *Id.* ¶ 111. Thus, Lee disclosed that, in a preferred embodiment, each device level 3104 is deposited onto an insulating layer, with the bottom level 3104 deposited onto insulating layer 3102. EX1003 ¶¶ 136-37. The Petition is thus wrong in suggesting that Lee did not describe how the bottom level 3104 of three-dimensional array 3101 is formed on insulating layer 3102. *Cf. Dish Network Corp. v. Entropic Commc’ns, LLC*, IPR2023-00392, Paper 7 at 15-16 (P.T.A.B. Aug. 11, 2023) (denying institution: “Petitioner’s argument relies on its assertion that Carnero does not disclose the source of the information input into the microprocessor that allegedly

causes the microprocessor to select a channel. We agree, however, with Patent Owner that Carnero does disclose its source of this information.” (internal citation omitted)).

Even if Lee were silent on how the bottom level 3104 of array 3101 is formed on insulating layer 3102, the Petition provides no reason why one of skill in the art would have “implement[ed] Lee’s Figure 35 memory device as a non-monolithic one,” Pet. at 52, when Lee clearly taught that, in Figure 35, “[t]he array of charge storage logic or memory devices 3101 are ... arranged as a three dimensional monolithic array” EX1007 ¶ 111.

The Petition’s assertion in Ground 1C that “a POSITA, at the suggestion of Lee, was looking to separately form a two-dimensional array of memory devices and ‘package it together,’” Pet. at 51-52, is contradicted by Lee itself. Intel cites in support the Sechen declaration, *see id.* (citing EX1003 ¶¶ 190-92), which in turn quotes an incomplete passage from Lee, *see* EX1003 ¶ 192 (citing EX1007 ¶ 107). Contrary to the incomplete passage relied upon by Intel and Dr. Sechen, Lee expressly taught a preference for a monolithic three-dimensional array.

Lee explained that “[t]he present inventors have realized that the cost of memory and logic devices would be decreased if the device density was increased. Thus, the present inventors have provided an ultra dense matrix array of charge storage semiconductor devices which has an increased density and a lower cost.”

EX1007 ¶ 106. Thus, the fundamental purpose of Lee’s invention is to reduce cost by increasing density. Lee described how that fundamental purpose is achieved:

One method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels. The term “monolithic” means that layers of each level of the array were directly deposited on the layers of each underlying level of the array.

Id. ¶ 107. Thus, Lee expressly taught reducing cost by using monolithic three-dimensional arrays of charge storage devices.

Lee presented separately formed two-dimensional arrays as a contrast against the preferred monolithic three-dimensional arrays of the invention: “In contrast, two dimensional arrays may be formed separately and then packaged together to form a ***non-monolithic*** memory device.” *Id.* (emphasis added). Lee neither explained what a non-monolithic memory device might look like nor recommended its use, focusing instead on the “three dimensional monolithic array” presented in Figure 35, *id.* ¶ 111, and relied upon by Intel. As explained by Lee, the monolithic three-dimensional array “improv[es] device density” and thereby “lower[s] cost.” *Id.* ¶¶ 106-07.

Intel’s assertion that Lee “suggest[s]” separately forming a two-dimensional array of memory devices and packaging it together, Pet. at 51-52, is simply false. Lee expressly taught higher density and reduced cost through use of a monolithic three-dimensional array. EX1007 ¶¶ 106-07. Intel does not explain why one of skill

in the art relying upon Lee’s disclosure would choose a less dense and more costly configuration than the one actually recommended by Lee and thus is unlikely to prevail on this obviousness challenge. *See, e.g., Wolfspeed, Inc. v. The Trustees of Purdue Univ.*, IPR2022-00761, Paper 19 at 28 (P.T.A.B. July 20, 2023) (“Constrained by the record before us, it is enough for us to observe that the relied-upon disclosure does *not* support a reason for selecting the ‘conventional’ layout of Figure 1.”).

Intel additionally argues a host of obviousness rationales, such as “using a known technique [(Kim’s wafer bonding) / (Aspar’s Smart-Cut® process)] to improve a similar known device (the structure in Lee’s Figure 35) in the same way [(logic/memory stacking using a wafer bonding process) / (vertically stacking memory devices using SOI technology)].” Pet. at 53, 61. But Intel does not explain how Kim’s wafer bonding or Aspar’s Smart-Cut® process would “improve” Lee’s monolithic three-dimensional array of Figure 35, which Lee itself taught is more dense and less costly as a monolithic three-dimensional array. EX1007 ¶¶ 106-07. Intel’s additional conclusory obviousness rationales provide nothing more. *See* Pet. at 53, 61.

Intel finally concludes by asserting that departing from Lee’s preferred more dense and less costly monolithic three-dimensional array “allows for more efficient quality control.” Pet. at 53, 61 (citing EX1003 ¶¶ 196, 213; EX1016)). Dr. Sechen

opines that “Testing layers of devices prior to stacking has well-known benefits.”

EX1003 ¶¶ 196, 213. He quotes EX1016 (Fung) as follows: “Assuming a 70% yield for each finished wafer, by stacking two wafers, the maximum yield achievable is 49% (i.e., 0.7×0.7).” *Id.* (quoting EX1016 at 1:33-47). Dr. Sechen goes on to explain that Fung’s proposed solution “is to test each wafer before stacking ‘to screen out defective ones.’” *Id.* (quoting EX1016 at 1:48-52). The problem, of course, with this alleged motivation is it simply explains a way to improve yield in the manufacture of non-monolithic stacked wafers. It **does not** provide a reason to use non-monolithic stacked wafers as compared to monolithic three-dimensional arrays. Dr. Sechen does not cite or discuss any yields for monolithic three-dimensional arrays as compared to non-monolithic stacked wafers. Thus, Lee’s teaching that monolithic three-dimensional arrays are more dense and less costly remains the sole comparison teaching in Intel’s cited art.

On this record, Intel cannot prove its assertion that one of skill in the art would have been motivated to use Kim’s or Aspar’s non-monolithic stacked wafers as opposed to Lee’s preferred monolithic three-dimensional array, which is more dense and less costly according to Lee itself.

C. The Johnson-Based Grounds Are Unlikely To Prevail

1. Grounds 2A, 2B, And 2C Do Not Meet Their Burden To Show That Johnson Disclosed A “Dielectric Layer Disposed Above The Electrical Devices”

For the Ground 2 challenges, Intel fails to meet its burden to show obviousness of Claim 13 based on Johnson. *See Magnum Oil Tools*, 829 F.3d at 1375.

In Ground 2A, the Petition relies on Johnson for the Claim 13 limitation requiring “a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices,” EX1001 at 12:25-27, which the Petition labels limitation 13[a], Pet. at vi, 65. The second half of limitation 13[a], “further having a dielectric layer disposed above the electrical devices,” requires that limitation 13[a]’s substrate includes a dielectric layer that is *part of* the substrate. *See, e.g., id.* at 90-91 (stating that “a substrate... further having at least one dielectric layer” in limitation 1[a] means that the dielectric layer is a “layer[] ‘of the substrate,’ as recited in 1[c] because 1[a] characterizes the substrate as ‘having’ th[at] layer[]”).

Intel relies exclusively on Johnson to satisfy the second half of limitation 13[a]. The Petition asserts that “Johnson teaches ‘a dielectric layer disposed above the electrical devices,’” *id.* at 66, citing the following disclosure from Johnson:

The processing may begin with a wafer that may have received prior processing steps, for example, CMOS transistors may be fabricated in

the monocrystalline substrate for the peripheral circuitry. An insulator then is deposited

Id.; EX1010 at 13:26-35. But Intel’s assertion that “Johnson’s fabrication starts with a wafer having devices in the substrate and ‘an insulator then is deposited,’” Pet. at 66, says nothing about whether the insulator (the Petition’s alleged dielectric layer) is disposed above any electrical devices, as required by limitation 13[a]. At most, Johnson disclosed that an insulator is deposited after “processing [that] may begin with a wafer.” EX1010 at 13:26-29. Johnson did not disclose an insulator being deposited above any electrical devices, and the Petition does not point to any such disclosure in Johnson. *See id.*; Pet. at 66.

The Petition’s failure to show that Johnson disclosed “a dielectric layer disposed above the electrical devices” can be demonstrated by Intel’s Ground 1A reliance on Lee for this same limitation. In Ground 1A, the Petition provides the below annotated figure from Lee, asserting that “insulating layer 3102 (‘dielectric layer’) is ‘disposed above the electrical devices’” shown in green. Pet. at 19-20. As shown, Lee disclosed the depth of the insulating layer 3102 (the alleged “dielectric layer”) relative to the top of driver circuits 3103 (the alleged “electrical devices”).

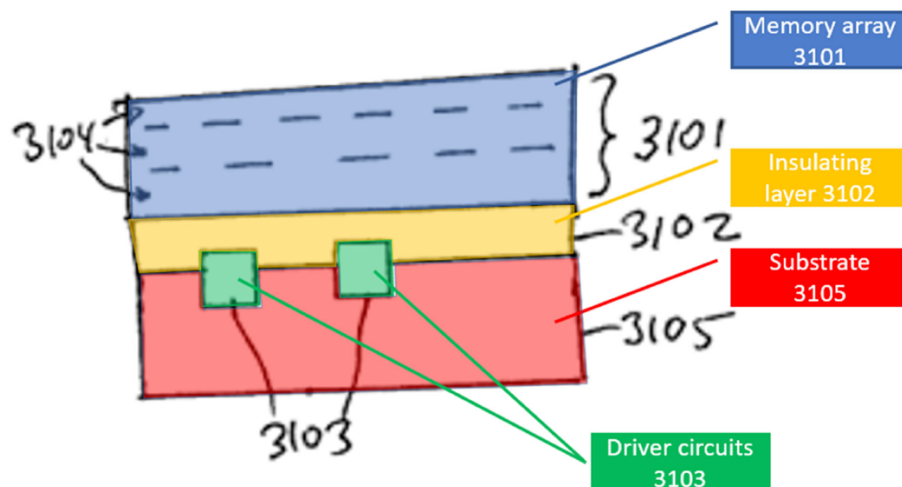


FIGURE 35

Id. at 19. In contrast to Lee in Ground 1A, in Ground 2A Johnson is silent as to the depth of any dielectric layer in relation to the height of any electrical devices. *See* EX1010 at 13:26-35.

Johnson’s silence regarding limitation 13[a]’s requirement of “a dielectric layer disposed above the electrical devices” cannot satisfy Intel’s burden to show that Johnson disclosed every limitation of Claim 13. *Magnum Oil Tools*, 829 F.3d at 1380 (“It is the petitioner that bears the burden of proof in IPRs”); *see also BMW of N. Am., LLC v. Blitzsafe Tex., LLC*, IPR2018-01142, 2018 WL 6190428, at *6 (P.T.A.B. Nov. 26, 2018) (denying institution: “[T]he point is that Herley is silent as to a structural separation, if any, between the controller and any of the other depicted components. Petitioner as the proponent of Herley’s controller and high-

speed interface comprising the ‘interface’ has the burden of explaining that this separation requirement is met”).

Intel also asserts that “Johnson further teaches the ‘fabrication sequence for the memory cell’ depicted in Figures 6(b)-6(g) involves ‘deposition and planarization of an interlevel dielectric.’” Pet. at 66 (quoting EX1010 at 12:42-54). For at least the same reasons discussed above, Johnson’s general reference to “deposition and planarization of an interlevel dielectric” also says nothing about whether the dielectric is disposed above any electrical devices, as required by limitation 13[a]. Moreover, none of Johnson’s Figures 6(b)-6(g) show a dielectric layer, much less a dielectric layer disposed above any electrical devices, nor does the Petition rely on any of Figures 6(b)-6(g) in its discussion of limitation 13[a]. See Pet. at 65-66. Finally, Johnson’s reference to an “interlevel dielectric” could not satisfy the claimed dielectric layer because an “interlevel dielectric” is one that is disposed between two layers, and thus would not be part of the claimed substrate as required by limitation 13[a].

Intel’s only citation for its assertion that “Johnson teaches ‘a dielectric layer disposed above the electrical devices,’” *id.* at 66, is to a paragraph in Dr. Sechen’s declaration. *Id.* (citing EX1003 ¶ 226). Dr. Sechen’s declaration relies on the same disclosures in Johnson as the Petition. Compare Pet. at 66 (citing EX1010 at 12:42-54, 13:26-35) with EX1003 ¶ 226 (same). Dr. Sechen’s statement that “these

disclosures when read together teach a dielectric layer deposited onto a substrate containing electrical devices,” EX1003 ¶ 226, notably does not address the claim requirement of “a dielectric layer disposed above the electrical devices.” His next statement that “[a]ccordingly, Johnson teaches ‘a dielectric layer disposed above the electrical devices,’” *id.*, is “only a *verbatim* restatement of the assertion being supported, without any supporting evidence or technical reasoning” which is insufficient and “particularly problematic in cases where, like here, expert testimony is offered ... to supply a limitation missing from the prior art.” *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, 2022 WL 3648989, at *6 (P.T.A.B. Aug. 24, 2022) (precedential). Dr. Sechen’s unsupported opinion cannot substitute for Johnson’s lack of disclosure and should be given no weight.

Additionally, the Petition presents no argument, much less any separate analysis, that the claimed “dielectric layer disposed above the electrical devices” would have been obvious. *See* Pet. at 66. Thus, Intel could not prevail on a theory that the claimed positioning of the dielectric layer relative to the electrical devices was obvious. *See Magnum Oil Tools*, 829 F.3d at 1381 (the Board is not “free to adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR”); *see also Garmin Int’l, Inc. v. LoganTree, LP*, 825 F. App’x 894, 898-99 (Fed. Cir. 2020) (“bare assertion through implication that a reference discloses a claim limitation” insufficient where “there was no explicit

disclosure” in the reference and petitioner did not assert that the limitation “would have been obvious to one of ordinary skill in the art”); *Dongguan Juxing Power Co. Ltd. v. NOCO Co.*, IPR2018-00503, 2018 WL 3413857, at *6 (P.T.A.B. July 11, 2018) (denying institution: “The analysis in the Petition identifies a disclosure in the prior art corresponding only to the polarity sensor; the Petition says nothing about a vehicle isolation sensor comprising an optically coupled isolator phototransistor. Nor does the Petition offer a reason that a vehicle isolation sensor comprising an optically coupled isolator phototransistor would have been obvious in view of the prior art’s disclosure of a polarity sensor comprising an optically coupled isolator phototransistor....” (internal citation omitted)).

Because the Petition fails to show that Johnson disclosed limitation 13[a], the Board should find no reasonable likelihood of success on the Ground 2A challenge to Claim 13. The Grounds 2B and 2C challenges to Claim 13 rely on the Ground 2A discussion of limitation 13[a]. *See* Pet. at 74, 77. Accordingly, Grounds 2B and 2C fail with the Ground 2A challenge.

2. Grounds 2B And 2C Do Not Meet Their Burden To Show A Motivation To Combine And Are Not Reasonably Likely To Prevail

Grounds 2B and 2C are also unlikely to prevail because Intel does not show it would have been obvious to combine the teachings of Johnson with those of Kim or Aspar.

Neither Ground 2B nor 2C relies on Johnson for teaching “the stackable add-on layer being bonded” as required by limitation 13[c]. *See* Pet. at 74-82. Instead, both grounds resort to “wafer bonding” for Claim 13’s bonding requirement. *See id.* Ground 2B relies on Kim and asserts that it disclosed an alternative “way to non-monolithically build Johnson’s 3D structure.” *Id.* at 75. Likewise, Ground 2C relies on Aspar’s Smart-Cut® process as an alternate way for “fabricating 3D structures.” *Id.* at 81. But the existence of a purported alternative approach does not provide a motivation for wholesale substitution of Johnson’s “deposition,” Pet. at 74, with Kim’s or Aspar’s wafer bonding.

Even if considered, Intel’s proposed substitution of wafer bonding for Johnson’s deposition is discounted by Intel’s own references explaining the problems with wafer bonding, such as reduced density, which is contrary to the essence of 3D structures. *See, e.g.*, EX1016 at 1:39-47 (explaining the problem of alignment in wafer bonding and the requirement that the “interconnect required for stacking needs to be very large which, in turn, degrades the density and performance of the 3D-IC”); *see also* EX1003 ¶¶ 250, 261 (citing EX1016 for problem of low yield in wafer stacking).

Intel’s contention that Johnson’s 3D structure *could be* implemented with wafer stacking, Pet. at 75, 78, does not show that one of skill in the art *would have been motivated to do so*. Intel’s assertions that “[i]n the combination... Johnson’s

layer of memory cells (‘stackable add-on layer’) would be wafer bonded to Johnson’s insulating layer (‘dielectric layer’),” *id.* at 75, and that “[i]n the combination, Aspar’s Smart-Cut® wafer bonding process would be used to bond Johnson’s layer of memory cells to its insulating layer,” *id.* at 78, merely address “whether a skilled artisan... *could have made* [not whether a skilled artisan] *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015); *see also Personal Web Techs., LLC v. Apple, Inc.*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (“But that reasoning seems to say no more than that a skilled artisan, once presented with the two references, would have understood that they *could be* combined. And that is not enough: it does not imply a motivation to pick out those two references and combine them to arrive at the claimed invention.”).

The Petition’s sole support for its alleged obviousness rationales, *see* Pet. at 75-76, 80-81, are citations to twin paragraphs in Dr. Sechen’s declaration which “merely parrot[] the words in the Petition” and are thus entitled to no weight. *One World Techs., Inc. v. Chevron (HK) Ltd.*, PGR2020-00059, 2020 WL 7222691, at *16 (P.T.A.B. Dec. 7, 2020); *compare* Pet. at 75-76, 80-81 *with* EX1003 ¶¶ 249, 260.

Finally, Intel’s assertion that “wafer-bonding Johnson’s level of memory cells to its insulating layer,” Pet. at 76, or using “Aspar’s Smart-Cut® process,” *id.* at 81,

“as compared to monolithic deposition[,] allows for more efficient quality control,” misses the mark. *Id.* at 76, 81 (citing EX1003 ¶¶ 250, 261; EX1016). Dr. Sechen opines that “Testing layers of devices prior to stacking has well-known benefits.” EX1003 ¶¶ 250, 261. He quotes EX1016 (Fung) as follows: “‘Assuming a 70% yield for each finished wafer, by stacking two wafers, the maximum yield achievable is 49% (i.e., 0.7x0.7).’” *Id.* (quoting EX1016 at 1:33-47). Dr. Sechen goes on to explain that Fung’s proposed solution “is to test each wafer before stacking ‘to screen out defective ones.’” *Id.* (quoting EX1016 at 1:48-52). But this alleged motivation simply explains a way to improve yield in the manufacture of non-monolithic stacked wafers. It **does not** provide a reason to use non-monolithic stacked wafers as compared to monolithic deposition. Dr. Sechen does not cite or discuss any yields for monolithic deposition as compared to non-monolithic stacked wafers. Thus, Dr. Sechen’s comparison does not provide a reason to substitute Johnson’s deposition with Kim’s or Aspar’s wafer bonding.

Petitioner has thus failed to show that it is likely to prevail on Grounds 2B and 2C.

D. Ground 3 Does Not Meet Its Burden To Show That Park Disclosed “Memory Cells Separated From Each Other By Dielectric Material”

Intel is also unlikely to prevail on its Ground 3 challenge to Claim 1—a claim not asserted in the district court cases. Unasserted Claim 1 requires “the plurality of

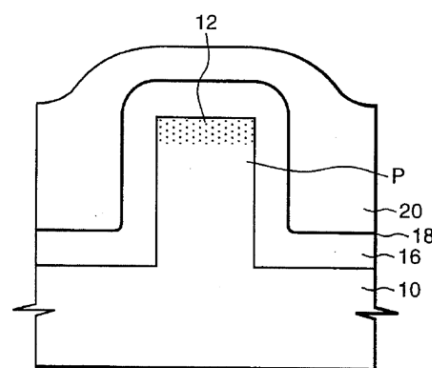
vertically oriented semiconductor memory cells [be] separated from each other by dielectric material,” EX1001 at 10:55-57, which the Petition labels as part of limitation 1[b], Pet. at vi. Intel cannot prevail on its challenge because it relies exclusively on Park, which neither disclosed nor suggested memory cells separated from each other by dielectric material.

Intel argues that “Park discloses that each of its vertically structured transistors are ‘surrounded with an insulating film.’ EX1011, 2:16-21, 4:9-27 (vertically oriented transistor surrounded by insulating films 16, 18, 20), Figs. 3, 4:6-8, 5:21-22; Sechen, ¶276.” Pet. at 88-89. Even if that were true, none of Intel’s citations to Park disclosed the limitation 1[b] requirement of *memory cells*, as opposed to “transistors,” separated from each other by dielectric material.

The first citation to Park (EX1011) at 2:16-21 nowhere discussed dielectric material separating *memory cells*. The Petition relies on the language “surrounded with an insulating film” from Park, but that is an incomplete quotation from Park, which read in context explained that “[t]he *silicon pillar* is ... surrounded [] with an insulating film.” EX1011 at 2:18-21 (emphasis added). Similarly, the next sentence explained that a “gate insulating film is interposed between the silicon pillar and a gate electrode surrounding the silicon pillar.” *Id.* at 2:21-23. Each reference to “insulating film” in this passage referred to an insulating film that is part of a single memory cell, not an insulating film separating different memory cells.

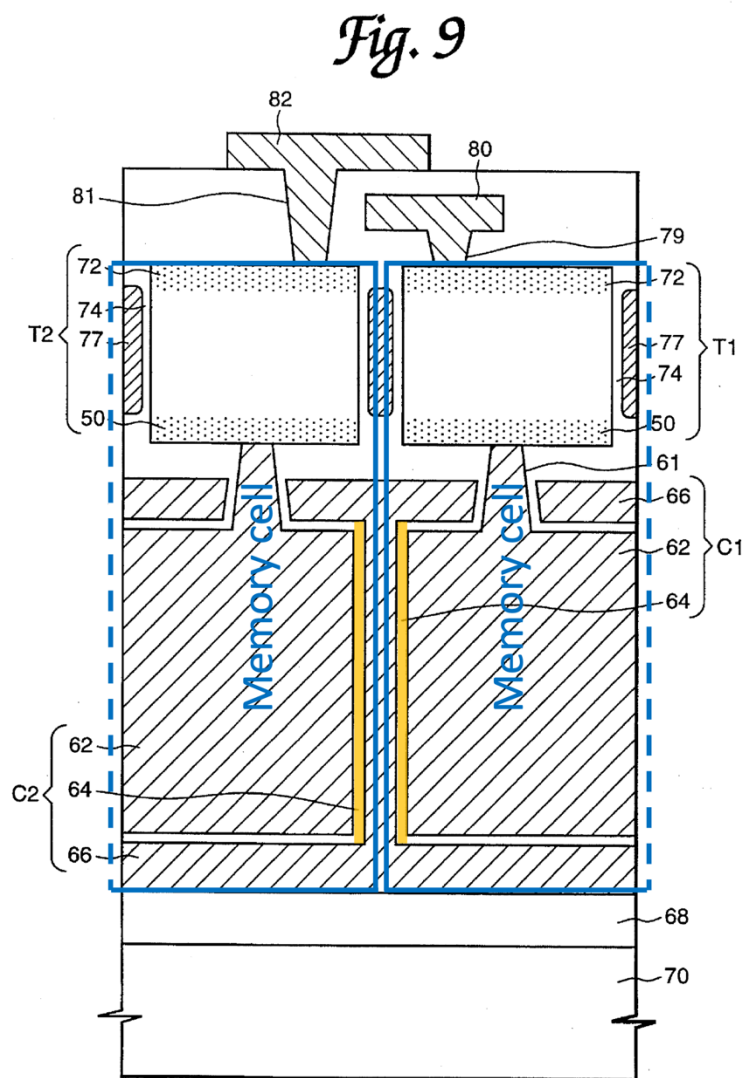
Intel’s reliance on Park’s Figure 3 and its description at 4:9-27 is also misplaced. Figure 3 does not show any transistor, much less a memory cell. Figure 3 merely shows a silicon pillar being formed before formation of a transistor or capacitor needed to form the DRAM memory cell. *See* EX1011 at Fig. 3, 4:9-10 (“FIG. 3 shows the formation of a pillar P ...”). Figure 3 (shown below) and its corresponding description did not disclose or suggest a memory cell at all, much less the Claim 1 requirement of “memory cells separated from each other by dielectric material.”

Fig. 3



The Petition also relies on the “dielectric film 64” of Park’s Figures 8 and 9, which are different views of the same embodiment. *See* Pet. at 89; EX1011 at 5:33-35. But the Petition itself acknowledges that, “[i]n Park, a dielectric film 64 is ... interposed between the plate and storage electrodes of capacitors C1 and C2,” *i.e.*, between electrodes 62 and 66. Pet. at 89; EX1011 at 5:37-43 (“A plate electrode 66 surrounds the entire surface of the storage electrode 62, with a dielectric film 64 interposed therebetween.”). In each of C1 and C2 in Figures 8 and 9, the dielectric film 64 is contained within a single memory cell and is not disposed between separate memory cells. Thus, Park’s Figures 8 and 9 disclosed a dielectric

film that is a part of a memory cell, not a dielectric material separating two or more memory cells.



EX1011 at Fig. 9 (annotated).

Intel’s assertion that “each of Park’s DRAM memory cells is ‘separated from each other by dielectric material’ because both the transistors and capacitors of each memory cell are surrounded by insulating material,” Pet. at 89, is refuted by Park

itself. For example, as shown in the annotations above, if a box is drawn around a memory cell in Park's Figure 9 and a separate box around the adjacent memory cell (blue boxes above), the two memory cells are not "separated from each other by dielectric material" as required by Claim 1. The Petition misleadingly relies on Figure 8 without addressing Figure 9. Pet. at 88. But as Park itself plainly states: "Transistors T1, T2 are formed so that they are isolated by an insulating material between the gate electrodes 33 in the bitline direction (see FIG. 8) and so that *they share a gate electrode 77 in a direction which is perpendicular to the bitline direction, i.e., the wordline direction (see FIG. 9).*" EX1011 at 5:49-53 (emphasis added). As shown in the annotated Figure 9 above, adjacent memory cells that share electrodes are not "separated from each other by dielectric material." *See id.* at Fig. 7 (plan view of Fig. 9's DRAM cell showing no separation in adjacent cells in the vertical direction).

Finally, the Petition's conclusory assertion that "[a] POSITA would have also understood the need to separate the memory cells with dielectric material for proper operation (e.g., avoiding shorts)," Pet. at 89, cannot substitute for Park's failure to disclose the claimed "memory cells separated from each other by dielectric material." The Petition's sole support for its assertion is a citation to a twin paragraph in Dr. Sechen's declaration which "merely parrots the words in the Petition." *One World Techs.*, 2020 WL 7222691, at *16; *compare* Pet. at 89 with

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EX1003 ¶ 276. That is insufficient. *Xerox Corp.*, 2022 WL 3648989, at *6 (offering “only a *verbatim* restatement of the assertion being supported, without any supporting evidence or technical reasoning” is insufficient and “particularly problematic in cases where, like here, expert testimony is offered ... to supply a limitation missing from the prior art”). Moreover, Park’s teaching of adjacent memory cells with no separation between them, *see* EX1011 at Figs. 7, 9, contradicts Intel’s assertion that separation was necessary to avoid shorts.

Because Park did not disclose memory cells separated from each other by dielectric material, Intel’s Ground 3 challenge is not reasonably likely to prevail.

VII. CONCLUSION

For these reasons, the Board should deny institution of the Petition.

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing **PATENT OWNER’S PRELIMINARY RESPONSE**, exclusive of the parts exempted as provided in 37 C.F.R. § 42.24, contains 11,549 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER'S PRELIMINARY RESPONSE** is being served electronically on September 14, 2023 to the following lead counsel for Petitioner to the following email addresses:

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