Stanford, Korean nanofab center, Oregon-based semi startup claim 3D IC breakthrough

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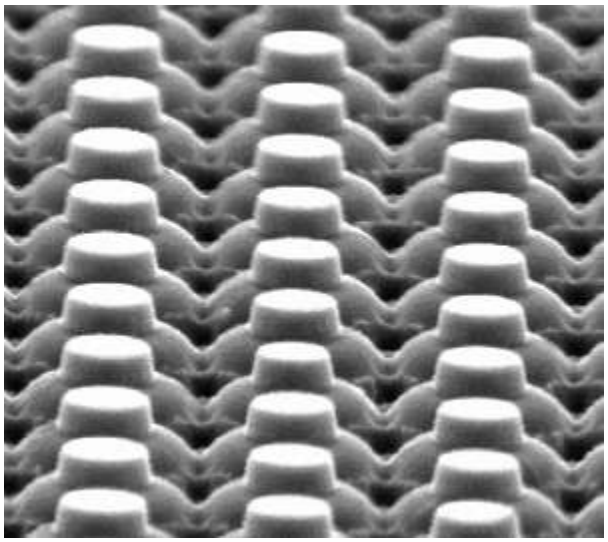
Ann Steffora Mutschler August 13, 2008

To allow low-cost memories and high-performance logic products with large embedded memory blocks, Stanford University's Nanofabrication Facility (SNF) along with Daejeon, Korea-based National NanoFab Center (NNFC) and Beaverton, Ore-based BeSang Inc are reporting what they say is a 3D IC technology breakthrough.

The 3D IC, which was processed on 8-inch wafers with industry standard 0.18-micron CMOS technologies both at NNFC and SNF, contains 128 million vertically oriented devices as a test vehicle, and was uniquely processed at low temperatures — below 400 degree Celsius, the parties explained. Also, a sub-micron-thick single crystalline silicon layer was initially formed above the silicon substrate with two metal interconnect layers, followed by vertical devices and additional metal layer.



This technology (shown left) forms full 3D interconnects below and above the vertical devices, whereas conventional semiconductor technologies contain planar devices on the surface of the semiconductor substrate and interconnects only above the planar devices.

Stanford University Professor and head of SNF, Dr. Dr. Yoshio Nishi explained in a statement, "One of unique features of BeSang's 3D IC is the capability of unrestricted 3D interconnections using conventional via technologies that does not require wafer alignment nor through-silicon vias for 3D interconnects. Conventional CMOS technology is facing its scaling limits. Therefore, this emerging 3D IC technology will extend the lifespan of CMOS technology, because it is an excellent alternative way to accommodate more devices on a given wafer area."

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While chip level 3D IC has been explored for many years by the semiconductor industry, market introduction of chip level 3D IC has been delayed due to technical challenges, including high-temperature processing, defects in semiconductor layers, limited 3D interconnections, and a complex process.

However, BeSang said it will be able to address these problems and has generated high-performance and reliable devices on single crystalline silicon layers that are subsequently formed above another silicon substrate at low temperature, which is an important aspect of this technology.

“BeSang’s 3D IC is a novel combination of short process steps, formation of array blocks in 3D, thin layer transfer using unique wafer bonding, followed by low temperature processing. Hence, there is a high possibility for this breakthrough 3D IC to provide low-cost manufacturing solutions for the semiconductor industry. BeSang’s 3D IC is a very attractive technology and one wonders why other companies have not thought about it. However, I always believe in the dynamics of small companies as my colleague, Dawon Kahng, and I worked as a small team within a large organization when we co-invented the non-volatile memory in 1967 at Bell Labs,” commented said Dr. Simon Sze, professor at National Chiao Tung University.

BeSang said the technology was successfully demonstrated at SNF in early 2007 and has been further developed at the commercial level technologies at NNFC since July 2007.

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