

Global Semiconductor Alliance



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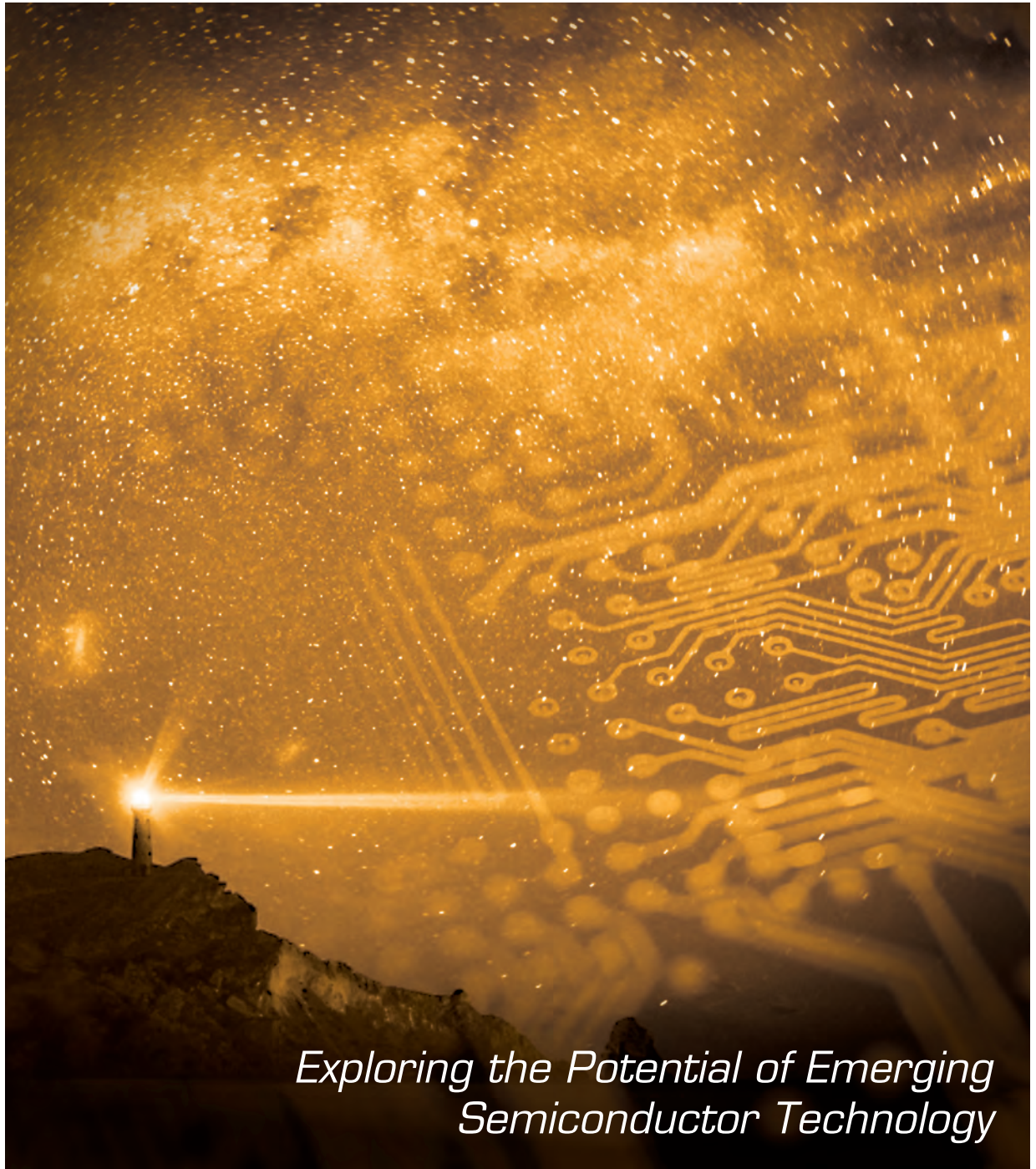
SEMICONDUCTOR LIGHT—LET IT SHINE!

AUTOMOTIVE FOUNDRY AND BACKEND FLOW

POWER MANAGEMENT IC TRENDS AND COST-EFFECTIVE TESTING

ELECTRONIC SYSTEM DESIGN CONSIDERATIONS TO MEET EMERGING MARKET NEEDS

*MEMORY SOLUTIONS FOR MEDICAL, SMART GRID, INDUSTRIAL AND OTHER
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MISSION AND VISION STATEMENT

SEMICONDUCTOR LIGHT — LET IT SHINE!

DR. PAUL RUSSO, CHAIRMAN AND CHIEF EXECUTIVE OFFICER, GEO SEMICONDUCTOR

“Let there be semiconductor light,” and the world will be happier and green!

Overview

Semiconductor-generated light is here—and there is no turning back. Light-emitting diodes (LEDs) are being shipped by the billions, with unit prices collapsing (nothing new here for the semiconductor industry) and the cost per light output following a new kind of Moore’s Law, whereby LED devices output more light each year at a lower cost per unit of light. LEDs are proliferating—and applications range from mobile devices (e.g., smartphone/tablet display backlights, pico-projectors and even flashlights) to general lighting, including street lights and computer and TV display backlights. LEDs are generating substantial energy and lifecycle savings while also extending product lives. Not yet at the same maturity level as LEDs, semiconductor laser devices are progressing, but, except for low-power devices, lasers are not yet ready for prime time. However, can anyone doubt that it is just a matter of time?

Lasers and LEDs are somewhat complementary, with each shining in specific applications. And there is the eventual mass production of organic LEDs (OLEDs), an ongoing promise that may finally arrive in larger, brighter and more numerous forms later this decade.

This article will discuss current and evolving applications, emerging technologies and predictions for the decade through 2020.

There is no doubt that many traditional industries such as incandescent light bulbs and fluorescent light sources (with their toxic chemicals), including those used for liquid crystal display (LCD) backlights, will gradually fade. These transitions will spawn major new semiconductor device opportunities (digital and analog) which will allow new emerging chip companies to ride new waves before these become massive markets requiring massive resources to compete and, hence, become the domain of massive semiconductor companies.

Semiconductor LEDs

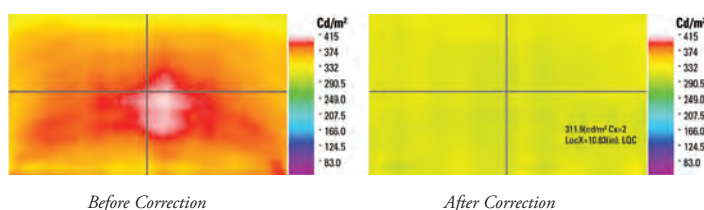
LEDs have been around for many decades, but today there is a veritable explosion in LED investment resulting in rapidly improving efficiency, light output and cost per unit of light. So it’s goodbye to

traditional light sources (i.e., incandescent and fluorescent bulbs) for computer display backlights, street lights, holiday lights and, soon, automotive, residential and office lighting. Still, LEDs have issues.

- There is a wide variation in inter-LED performance between batches (like any semiconductor process) from high-volume manufacturing. This large brightness variation (up to 30 percent) results in the need to bin LEDs to achieve the needed uniformity and performance in multi-LED lighting solutions.
- LEDs are very temperature-sensitive, and light output will fade over time.
- Backlight performance will vary with image brightness. These effects result in more severe non-uniformity issues in color and brightness than those associated with traditional backlights.

Many companies are working on both analog and digital solutions to reduce LED backlight costs and improve color and brightness uniformity. Figure 1 shows results before and after digital correction of a 4-megapixel, 27-inch industry-leading computer display.

Figure 1. 4-Megapixel, 27-inch LED-backlit LCD Monitor (Before and After Digital Uniformity Correction)



The benefits of LED lighting are clear—large energy savings and major reductions in lifecycle costs. For street lights, LEDs result in a five times reduction in energy use as well as much lower lifecycle costs. More and more automobiles use LEDs, allowing for not only lower costs, but also greater flexibility for fitting these lights into the design.

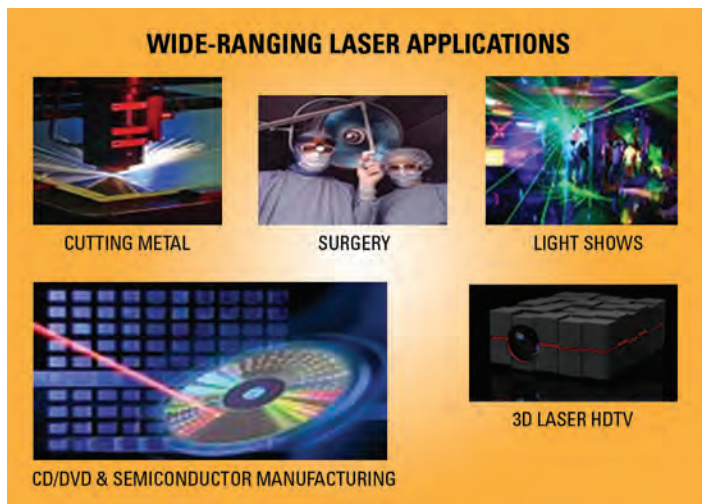
In addition to the large and growing need for LED fabs and related equipment, there are rapidly growing needs for analog and digital semiconductor devices to support all the above applications.

Semiconductor Lasers

Lasers were invented in the 1960s, but these were bulky gas lasers. Laser diodes are now shipping in huge quantities in digital video disc (DVD) players and, soon, in pico-projectors. The military has developed building-size lasers that will eventually be capable of shooting down incoming missiles and satellites. But what will really drive laser adoption will be when reasonably powered lasers (e.g., 10-30 watts) become affordable. That development is underway and expected to occur this decade. This will spur a new wave of laser displays, from 3D home theaters and dynamic signage to commercial projection applications.

As in the case of LEDs, life costs for laser systems will become much lower, and new categories of products will emerge. Figure 2 illustrates some of the many uses of lasers as new applications continue to come to life.

Figure 2. Laser Applications



Lasers are used in compact disc (CD)/DVD, metal and semiconductor manufacturing, as well as in medical surgery (body and eyes), digital 3D cinematography, military functions and artistic applications such as art shows.

Front- and rear-projection laser 2/3D high-definition TVs (HDTVs) will provide a significant new semiconductor opportunity. This will be driven by several trends, including consumer desire for ever-larger screens, the need to reduce energy consumption (given that many TVs are powered on six hours or more every day) and consumer preference for passive low-cost glasses for 3D content. If a 80-inch rear-projection laser TV is compared to an 80-inch LCD TV, the laser system's color is far richer, the power dissipation is as much as 80 percent lower, the weight is much lower (allowing just two people to move and install the device instead of many) and, most importantly, since only passive polarized glasses are needed, laser systems will accelerate the prevalence of 3D technology. 3D glasses will evolve into polarized designer eyeglasses and, eventually, be used for many functions outside of 3D content viewing. Imagine wearing one pair of eyeglasses for driving and then using the same pair to watch 3D HDTV!

One of the challenges to producing large and very thin rear-projection laser displays is to reduce the cost of the complex short-throw optical components as well as assembly and optical alignment costs. Geometric processing technologies and related ICs will help achieve these goals and give rise to new intellectual property (IP)-centric fabless IC companies. Likewise, lasers will give rise to another wave of component manufacturing semiconductor companies as

well as related manufacturing and test equipment businesses. Finally, several new ICs are needed to deal with semiconductor laser display characteristics (i.e., color and brightness uniformity, de-speckling, optical components and optical alignment issues). The future for lasers is very clear—only blue skies ahead.

OLED Displays

OLEDs are an emerging display technology. Already in use in mobile devices, some believe that, ultimately, this will be the technology to replace standard LED panels. OLEDs are more energy-efficient, emit light directly, and have richer colors and simpler manufacturing. There is even talk of using OLEDs as light sources. A lot of funding is being applied to this space. A very large range of new product opportunities will be enabled by the potential of OLED to provide very high energy efficiency combined with manufacturing simplicity.

OLEDs consist of an organic material deposited on a conductive film. Electrons excite the material which then generates light. The light color comes from the organic material used. The simple regular structure of OLEDs, as well as a range of new applications, is illustrated in Figure 3.

Figure 3. OLED Structure and Applications



OLEDs can enable many new applications. Their structure promises low-cost manufacturing with outstanding performance.

OLEDs, even more so than LEDs, have significant issues with the life of organic materials as well as color and brightness uniformity across displays. These issues represent another semiconductor opportunity, which is to create low-cost digital and analog semiconductor solutions to enable wide deployment of OLEDs.

Summary

As LED and laser manufacturers continue to pursue rapid improvements in cost, light output and efficiency, their usage will, over time, replace a number of large existing markets and create a number of new ones.

Furthermore, as the adoption of OLEDs grows and laser displays emerge, a potential scenario is that lasers may dominate the larger screen sizes (60 inches and up), while OLEDs dominate certain classes of smaller displays (e.g., up to 32 inches) and LCD and plasma dominate the mid-size mainstream markets. OLEDs are the display of the future.

LEDs, lasers and OLEDs will change all the industries that create light for our eyes to see—from mobile devices, computer

Marvell finished its fiscal year ending January 2011 with revenues up 29 percent from the previous year and posted the highest free cash flow in its history. In GSA's interview with Dr. Sehat Sutardja, chairman, president and chief executive officer of Marvell, Dr. Sutardja discussed how the company was able to accomplish this through its complex integrations enabling them to meet customer demands; the importance of strong, established partnerships in times of tight supply; opportunities accompanying the proliferation of smartphones in the mobile devices market; and much more.

— Jodi Shelton, President, GSA



DR. SEHAT SUTARDJA

Chairman, President and Chief Executive Officer, Marvell Technology Group Ltd.

Q: *The foundation of Marvell's growth and leadership is its development of breakthrough technology, dedication to customers and consistent delivery of high quality products. Tell us about some of your most recent offerings and what your customers require.*

A: In our business, the chip design cycle is quite long. For example, we recently introduced a silicon solution, which we started working on three or four years ago, that powers the OnLive Game System. This chip is specifically made to tackle the future of video entertainment products such as set top boxes (STBs), Blu-ray players and cloud-based gaming. This device enables our customers to build STBs the size of a smartphone.

In the past, our customers wanted silicon solutions optimized for a specific application to cut costs. But as more consumers now desire a consistent user experience, whether they are using their STB, Blu-ray player, video media player or connected TV, our customers are now looking for more powerful, integrated solutions to address multiple consumer markets. This has created an opportunity for Marvell because we excel at increasing chip functionality and performance, and differentiate ourselves through complex integrations and high-performance processing.

Q: *With the excitement surrounding the mobile devices market, specifically smartphones, how does Marvell plan to position itself to take advantage of that market opportunity?*

A: It's common knowledge that the biggest market opportunity right now for semiconductors is smartphones. Marvell expects that in the near future practically every

phone will be a smartphone. The only differentiation will be whether it is an entry-level smartphone versus a high-end smartphone.

Marvell has been involved in the high-end smartphone market for the past four years. Now, we are expanding our reach into mainstream, high-volume smartphones. The way to take advantage of this opportunity is to use higher integrations and more advanced process technology to lower the product cost.

Q: *According to reports, Marvell gained an Armada processor design win on an Android-based tablet platform, started shipping one Android-based OPhone last month and will ship another four to six models in the first half of 2011. So this positive development signals that Marvell is expanding its baseband+apps processor customer base beyond RIM, which foretells incremental growth potential going forward. Can you explain how these great developments are likely to propel Marvell forward?*

A: As an example, Marvell has developed the industry's first highly integrated single-chip TD-SCDMA platform to address the China market and supply China Mobile, the largest carrier in the world with more than 500 million subscribers. As China Mobile migrates their customer base from 2G to 3G as well as to Long-Term Evolution (LTE) further down the road, this creates a substantial growth opportunity for Marvell. Over the next several years, however, we will focus on providing consumers with lower cost smartphones to help facilitate the transition to 3G.

There are, of course, other growth opportunities for Marvell in the smartphone market outside of China. The world is still primarily

based on the UMTS 3G platform, so Marvell has yet another 3G platform focused on that market segment.

Q: *Following the Consumer Electronics Show (CES), The Wall Street Journal published an article titled "Chip Makers Target Everything But Kitchen Sink." Considering the fact that Marvell initially focused on supplying chips for the storage market but now offers chips for everything from routers to cellphones, do you agree that this is now the norm and that it is a requirement to be successful? Is it a requirement to focus on many different markets?*

A: Our customers prefer suppliers that have all the necessary technology under one roof, so when they need to build products that address multiple market segments, they don't have to scramble to find solutions from three or four different suppliers. System original equipment manufacturers (OEMs) now, in fact, prefer more than having all the necessary technology under one roof—they want everything except the kitchen sink on a single chip.

Q: *While lead times are decreasing slightly, capacity shortage is still an element that plagues the industry. What measures is Marvell taking to secure sufficient foundry capacity in 2011?*

A: There are only a few things we can do to manage the shortage of capacity that is expected in 2011. First, we must design our chips so they use a smaller silicon area so we can then produce more parts out of a given number of wafers. Second, we must take advantage of advanced process technology nodes so we can tap into newer capacity and newer fabs that are being built by our foundry partners. The newer



Recently honored with EDN's Innovation of the Year Award for analog ICs, NXP Semiconductors also delivered better-than-anticipated top-line revenue results during the first quarter of 2011. In GSA's interview with Richard Clemmer, executive director, president and chief executive officer of NXP, Mr. Clemmer discussed the numerous benefits of the high-performance mixed-signal market, exciting possibilities within high-growth markets and the remarkable potential for NFC technology. In addition, Mr. Clemmer identified four major macro-level trends driving electronic growth, offered insight into positioning customers for a time-to-market advantage, and touched upon Europe's semiconductor value and potential.

— Jodi Shelton, President, GSA

RICHARD L. CLEMMER

Executive Director, President and CEO, NXP Semiconductors

Q: *NXP is targeting many of the high-growth markets GSA has identified such as medical, smartphones and light-emitting diode (LED). What high growth market is NXP most excited by, and which do you consider to hold the greatest opportunity?*

A: NXP is very excited about the broad-based, high-performance mixed-signal market. Key areas of opportunity in this mixed-signal market include microcontrollers for industrial and energy metering applications and high-performance radio frequency (RF) technology, which is key in developing radio base stations to enable the continued explosion of both wireless-connected devices and the volumes of data being transferred.

Also, the use of IC drivers for energy-efficient and dimmable compact fluorescent lamps (CFLs) as replacements for incandescent bulbs is an area of growth we foresee for 2011 and beyond. Furthermore, near field communication (NFC) that can turn your phone into an electronic wallet is a high-growth market.

Looking at application areas beyond the normal growth of our served markets allows us to approach things from more of an ecosystem viewpoint, potentially driving much stronger leadership—similar to what Intel has done in the microprocessor environment, where it's not just the silicon content they provide, but the software, the ecosystem, etc. Our first proof point on that is NFC, a new communication standard that we co-invented seven or eight years ago that we are now taking to a total solutions viewpoint.

Another area is authentication. A report out of KPMG says that 10 percent of the world's economy

is driven by counterfeit goods. Thus, if a company can provide the technology and capability for manufacturers to authenticate their brand, companies can protect not only their brand, but also associated revenues. Consequently, three or so years from now, the opportunity for authentication could be as large as NFC.

Q: *NXP has long promoted NFC technology. Now that the momentum for this technology is here and other players are entering the market, thus driving competition, how does NXP plan to retain a leadership position in this area?*

A: As a co-inventor of NFC technology, NXP holds a strong intellectual property (IP) position. Though many semiconductor groups are discussing NFC technology, most are referring to a NFC radio and the ability to transmit a radio signal. NXP, however, is focused on a total NFC solution, where we provide not only the radio, but also the secure element and associated software. I'm not aware of any other company that can provide all of those key aspects in one solution. For NXP, it's about focusing on the ecosystem, which includes not only our customers but the software suppliers, the carriers and the financial institutions.

Thus, it's not a typical semiconductor play, but rather more of an ecosystem play where we're using our semiconductor technology to facilitate and drive implementation. NXP is the clear leader in NFC, with the broadest portfolio of hardware and software solutions combined with the deepest situational knowledge to help our customers implement a complete and robust solution. Our expertise and understanding of the complete secure

transaction ecosystem is why more and more customers choose NXP as their partner of choice to implement mobile transaction solutions.

Q: *It is common knowledge that Smart Grid technology offers significant growth opportunities for semiconductor companies, and the potential for semiconductors in hybrid cars, smart electricity and solar has been established. Can you identify some of the lesser known areas for opportunity in relation to Smart Grid?*

A: NXP is very focused on the green energy concept and how we can impact the world by reducing overall energy consumption and impacting hydrocarbons. This question relates to products where we combine wireless IP connectivity with our energy-efficient lighting and power conversion technologies in a compact, low-cost solution. We are transforming the way we design, control and manage lights. For individual consumers, smart lighting means highly personalized, intelligent lighting environments—lights that turn on and off when and where you need them at the desired level of brightness, therefore, saving power and electricity costs. We think this will offer significant energy savings and direct application well beyond the total grid. The overall smart home/smart building opportunity, as applied at the individual user level in a home or business, represents a potential market of \$4 to \$4.5 billion by 2014.

NXP is focused on other areas that impact Green as well. For example, we ship a number of automotive components aimed at increasing automotive efficiency and reducing carbon dioxide (CO₂) emissions. In addition, NXP's GreenChip

AUTOMOTIVE FOUNDRY AND BACKEND FLOW

PETER PANN, SECTION MANAGER, FOUNDRY ENGINEERING, AUSTRIAMICROSYSTEMS AG

An automotive wafer fabrication process must have an excellent level of quality and reliability. Field failure rates of less than 0.1 parts per million (ppm) are specified for automotive production processes. Excellent defect density values of less than $0.1\text{D}/\text{cm}^2$ are necessary to produce automotive-class silicon.

What does such an automotive flow, designed to operate in parallel with industrial or consumer flows, look like? It can be divided into five separate elements.

Automotive Wafer Fabrication

Fabs which are running both automotive and industrial or consumer wafer production may choose to reserve particular equipment for higher quality processes, but there is the risk of losing flexibility once the production process reaches full capacity. The better solution, therefore, is to establish fabs with automotive-class equipment across the board. Special additional measures then support the high-quality requirements of automotive wafers.

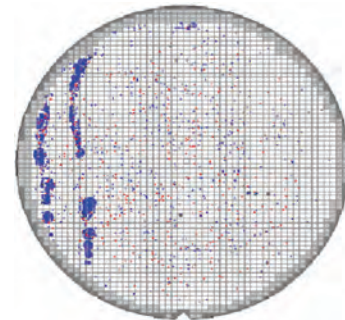
In general, defect engineering should be performed. On certain key process steps, an optical system must be used to detect and classify defects. If defects are found on the wafer surface, cleaning with special equipment such as scrub cleaners is possible; but, in general, the rework of hard layers is not permissible. Rework of soft layers such as photoresist in some cases may be permitted.

Figure 1 shows the electronic output of a defect measurement tool. Such electronic maps are directly linked to electrical wafer probe stations as pre-recorded information for the wafer handler. Implementing wafer probe procedures using defect maps is called geographic part average testing (GPAT). For example, assume that a scratch on a silicon wafer is detected during the defect measurement process: It would not be sufficient to identify only those circuits that are directly affected by the scratch. Circuits adjacent to the scratch also potentially host hidden reliability problems. GPAT procedures therefore define a certain “off-zone” around such defects.

At the end of the wafer fabrication process, an electrical wafer acceptance test (WAT) is performed on special test structures which are usually located within the scribe line. Usually, there are two

categories of WAT parameters: “pass/fail” and “info.” For automotive applications, additional categories such as “performance” and “reliability” should be defined.

Figure 1. Defect Map



Source: austriamicrosystems

Such special categories can have different pass criteria. For instance, the reliability parameter in WAT tests can have a pass criterion of five out of five sites, whereas other parameters remain at the industry-standard level of three out of five sites. In case of fails, special procedures such as 100 percent WAT can be applied, which means that each test structure must be measured on every wafer of a suspect lot.

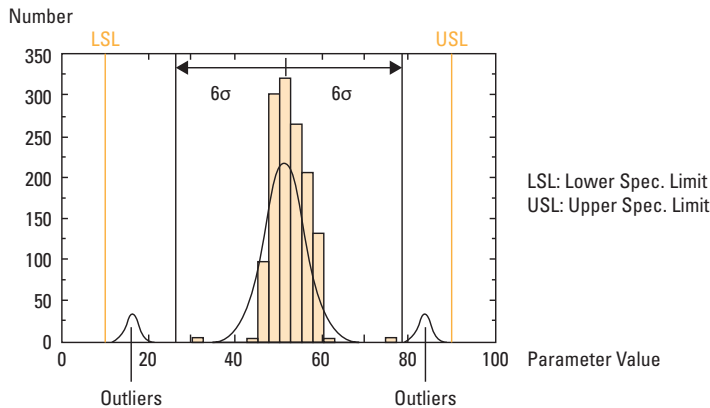
Before a lot is released, it is mandatory to perform an automatic optical inspection (AOI) on every square micron on all wafers.

Automotive Wafer Probe Test

In addition to GPAT, critical electrical test parameters are defined for parametric part average testing (PPAT). Outliers from normal distributions are suspect and must be eliminated as shown in Figure 2. Advanced systems even implement algorithms to dynamically adjust the limits for each wafer. The yield and defect management should be controlled by a material review board (MRB) consisting of experts from various disciplines such as product engineering, fab engineering and quality assurance.

The MRB must be authorized to scrap wafers that are judged to possess an increased risk of unreliability. The MRB can also prescribe detailed failure analysis or the introduction of special screening methods.

Figure 2. PPAT



Source: austriamicrosystems

Many wafer fabrication steps are performed in chambers for single wafers. This means that a single wafer yield drop provides evidence of equipment problems. To avoid any risk arising from single-wafer events, a statistical yield limit (SYL) for wafers must be defined. Design and test failure mode and effects analysis (TFMEA) is a useful method to define critical test parameters which must be monitored and controlled with tighter statistical bin limits (SBL).

In general, automotive wafer probe test should only be performed in a cleanroom to avoid particle contamination. The probe is rated for a certain number of probe needle touchdowns on bonding pads. It is advisable to perform an AOI for scratches that could have been caused by probe needles due to handling errors or probe malfunction.

Automotive Packaging

The most obvious requirement for automotive packages is an extended temperature range: Temperatures from negative 40 C to 150 C are necessary for some applications such as sensors in the engine compartment. The selected packages must also meet specifications for other parameters such as prevention of moisture ingress. In general, electromagnetic compatibility (EMC) is also a big issue in the selection of IC packages.

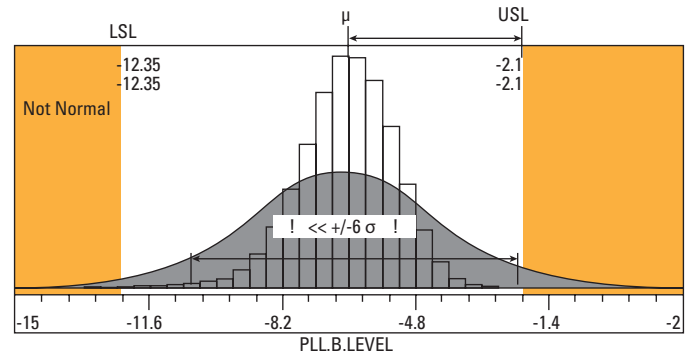
The assembly process must be performed according to strictly defined specifications for materials, and must comply with assembly-related design rules, which might differ from consumer rules. In addition to the 100 percent optical inspection in the wafer fab, two additional 100 percent optical inspections for automotive packaging are also required: the second optical inspection after wafer dicing and the third after wire bonding.

Automotive Final Test

Automotive test program development is a special challenge and should be performed according to strict rules. It starts with TFMEA and needs a careful correlation between the test results from production tests and application bench tests. In general, the test coverage for both digital and analog tests must be very high. Test coverage values greater than 98 percent are typical targets for the automotive industry. Process capability (Cpk) analysis (Figure 3) gives information about expected yield and appropriate limits.

Suitable temperature insets to these limits must be chosen to guarantee that every test parameter that is tested at room temperature will also pass the test at minimum and maximum temperature. Such a three-temperature test is usually performed only on a sample basis, but can be extended to all parts for critical applications.

Figure 3. C_{pk} Analysis



Source: austriamicrosystems

In relation to three-temperature testing, it is necessary to perform correlation tests on reject parts; parts which fail extreme temperatures must also fail the room temperature test when tighter limits are applied. Such test limit insets are defined in the light of the temperature characterization. Furthermore, PPAT, SBL and SYL, as implemented at the wafer probe level, must also be performed at final test.

Test program release procedures for automotive test are more extensive than those for consumer or industrial test. One of the release checks is an open socket test. Each individual test must be developed in such way that a disconnection of the device under test (DUT) from the tester channel will be detected. A repeatability test (where each test is performed in a loop with certain cycles) makes sure that individual tests are stable and reproducible.

Gauge repeatability and reproducibility (GR&R) tests ensure test procedures give the same result when using different test hardware modules, test boards, handlers or even different tester platforms. The formal production release is usually performed in several steps—from a limited release for a certain number of fab lots to final release without any limitations.

In general, the final test program for packaged parts is used for wafer probe too. The only difference could be that the wafer probe test is a multi-site test with multiple parallel die tests at the same time. The test program, therefore, must be able to cover both single-site and multi-site test schemes. For the multi-site test approach, a comparison of test results for each site is necessary before test program release.

Usually, a foundry business model follows the steps described above and is closed by a production part approval process (PPAP).

Automotive Safe Product Launch

The automotive industry strongly recommends the introduction of safe product launch concepts. These procedures include the fabrication of a corner lot (Table 1). The corners should reflect a parameter variation which can occur during a longer period of production. The goal for a corner lot is that such parameter variation should be simulated with just one lot. The corners must be aligned with corner models which have been used during the design phase of the product.

Ripples in the Semiconductor Supply Chain

Michell Prunty, Senior Consumer Analyst, Semico Research Corporation

Japan is a major producer and consumer of semiconductors as well as materials and equipment used in the production of semiconductors. Thus, it is no surprise that the March 2011 earthquake, in particular, is raising fears that semiconductor production capabilities may be hindered throughout 2011 into 2012, affecting the whole supply chain's bottom line.

The seismic activity in Japan was not just one large magnitude-9 quake; it spurred a ripple effect that many are still dealing with. Following the initial quake, there were four magnitude-7 quakes, and more than 75 magnitude-6 aftershocks in addition to the tsunami and nuclear disaster. While the damage to semiconductor facilities was, in most cases, not significant, the roads and electrical grid are another matter.

In some cases, for example, Sony's manufacturing plant in Sendai, the tsunami caused waves as high as five feet, bringing debris and mud along with the water. Sony is considered one of the manufacturers most affected by the disaster, with seven different plants originally shut down.

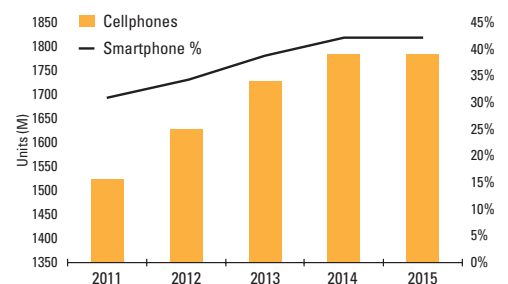
Most end-use products are manufactured outside Japan, either in Asia Pacific or the Americas. However, those end-use plants ship specialized and high-end semiconductor components from Japan, with some products being almost entirely manufactured in Japan.

End-use Markets Affected by the Earthquake

Cellphones

A key component for cellphones is a chemical adhesive for lithium-ion (Li-on) batteries called polyvinylidene fluoride (PVDF). Kureha Corporation, based in Japan, produces about 70 percent of the world's PVDF supply in Iwaki, where their plant remains closed. While Kureha was ready to reopen their Iwaki plant in mid-April, the magnitude-7 quake and 6.2-magnitude aftershocks that hit on April 11 and 12, respectively, caused additional damage, making reopening impossible at that time. If everything goes according to plan, Kureha expects production of PVDF to restart in early May, which would result in a delay of two or more months, in a supply chain that functions with less than a two-month inventory, thus indicating a potential shortage of Li-on batteries during the third quarter 2011.

Figure 1. Smartphone Percentage of Total Cellphone Units



Source: Semico Research, Market Analysis and Planning (MAP) Model

The cellphone market won't see much of an impact in overall end-use shipments, with worldwide units increasing 7 percent year-over-year (YoY) from 2011 to 2012. For vendors, there may be a shift in market share rankings because Apple, Huawei, HTC and Samsung all moved quickly to find suppliers of key components in other regions—a move that may put them ahead of Nokia, Research in Motion (RIM) and Sony during the third quarter. Additionally, other market dynamics are in play. For instance, as shown in Figure 1, smartphones will increase to over 40 percent of the total cellphone market by 2014, and Apple has recently displaced Nokia as the No. 1 supplier of smartphones.

Digital Cameras

In addition to Sony, three other camera vendors suffered plant closures. Panasonic's Fukushima plant, where they make Lumix cameras, was shut down and suffered from damage as well as injured employees. Partially in response to the earthquake and partially due to the sluggish world economy, Panasonic recently announced a shift in its business from "Japan-oriented" to "globally-oriented." While Panasonic has downplayed any lasting effects from the earthquake, the company acknowledges declining sales of mobile phones and digital cameras.

Canon shut down their lithography and digital camera lens plant. Production continues to be on hold, potentially causing an inventory shortage spanning the third quarter 2011 to the first quarter 2012. Similar to Panasonic, Canon remains uncertain about recovery into 2012, even as their sales of cameras and printers rose 11 percent in the first quarter 2011. As a result of the earthquake and their plant closure, Canon is predicting a 10 percent decline YoY.

Nikon originally closed multiple plants, including seven subsidiary plants; however, all were operational by the end of March. Though parts were obtained quickly from business partners, Nikon also anticipates inventory issues during the third and fourth quarters of 2011. Nevertheless, unless the power interruptions continue longer than

expected, normal operations should resume in 2012.

As with the cellphone market, these vendors' inventory issues could mean a change in market share ranking for Sony and Olympus. Canon and Nikon are No. 1 and No. 2, respectively, in the digital camera market. Sony's camera manufacturing facility was not damaged, and Sony is now discounting their cameras to increase sales.

Game Consoles

With so few vendors competing in the handheld console market, being a "first mover" is a huge benefit. Currently, there are only two major players—Sony and Nintendo, the acknowledged leader in the game console market. Nintendo's Dual Screen (NDS) did extremely well, with sales of NDS and NDS Lite reaching 100 million units in 2009 and 150 million in 2010. Sony's PlayStation Portable (PSP) sold just under 70 million units as of February 2011.

Sony and Nintendo have made small changes to their devices over the last few years, with Sony releasing the PSP Go (now out of production) and Nintendo releasing the NDS Lite. However, there were no real changes or new entrants to this market until Nintendo released their upgrade to the NDS—3D. Sales have been lagging, only reaching half of what Nintendo expected. This can be attributed, in part, to the earthquake, as personal spending has consequently gone down. Although, as consumers are unhappy with the game lineup and product price, the earthquake cannot be fully blamed.

Now would have been an ideal time for Sony to release their next-generation portable (NGP) device; however, due to production interruptions (Nintendo did not experience any direct damage from the earthquake), the NGP will be delayed until the first quarter of 2012, if not later. Even so, this gives Nintendo ample time to develop a comprehensive strategy to buoy sales before the holiday shopping season.

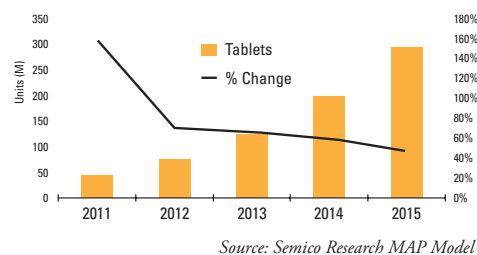
Tablets

Due to chip production interruptions, there is

some uncertainty about the industry's ability to bring new tablets to market in 2011. Multiple tablet parts are manufactured in Japan: NAND flash, mobile dynamic random access memory (DRAM), touch screens and batteries. Apple, with 85 percent of the market, is said to control about 60 percent of the touch screen supply. Therefore, as Apple secured suppliers in other regions, their move created a shortfall for everyone else.

The forecast for tablets will take a small hit during 2012, with units increasing only 70 percent YoY compared to 159 percent YoY from 2010 to 2011. This year, shipments will reach approximately 44 million units, and tablets may have enough inventory in production to cause an uproar during the holiday season, much like the Tickle Me Elmo frenzy.

Figure 2. Worldwide Tablet Forecast



Automobiles

Perhaps one market most affected by the earthquake is the automotive market, where both Honda and Toyota's domestic production fell by 63 percent and is not expected to recover until the end of the year. Honda's profits have dropped 38 percent, and the company only recently restarted production.

In terms of market share, Toyota is concerned about slipping to No. 3 due to the production interruption. South Korea's Hyundai Motors and Kia Motors have both had bump ups in sales, along with General Motors (GM) and Ford, though some attribute at least some of this increase to their line of smaller vehicles.

Materials

If we look closer at the supply chain, there are many plant closures that affect every end-use market.



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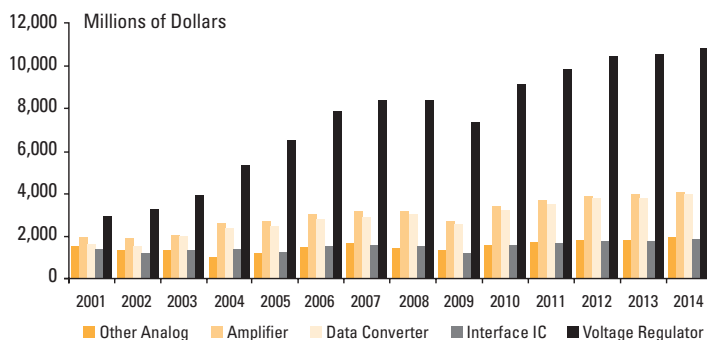
POWER MANAGEMENT IC TRENDS AND COST-EFFECTIVE TESTING

DONALD W. BLAIR, PRINCIPAL CONSULTANT, VERIGY LTD.

Power management ICs (PMICs) are used in electronic applications or devices to manage the voltage and current. PMICs can contain battery management, voltage regulation, charging and digital current to digital current (DC-DC) converters¹ among other functions. In Figure 1, PMICs constitute a large portion of the “voltage regulator” revenues, and the continued growth in market size is shown. The growing demand of portable applications, the volume of which is consumer driven, is a large component of this growth. As a result, two trends have emerged.

One is for lower cost, simple PMICs, many of which are being integrated into their host IC’s package, thus becoming a system-on-chip (SoC) (e.g., entry-level, single-chip cellphone ICs with an integrated PMIC). These devices supply very basic features (many of the phones are voice only) to emerging cellphone markets.

Figure 1. Analog IC Revenue by Type



Source: Gartner (2010)²

The other trend is to have more complex PMICs (for higher end stand-alone applications) become part of the chipset of the application. Examples of this are feature-rich cellphones or mobile computing devices.

Because cellphones and mobile computing devices are marketed in consumer markets, lower cost pressures are always present, and, in fact, include cost-of-test (COT) targets that continually decrease year-over-year (YoY).

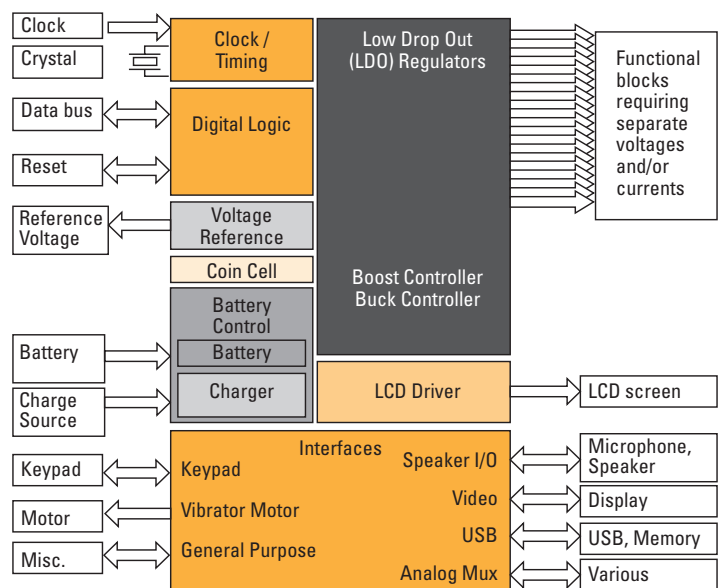
Another continuing trend pertaining to the functional technology of PMICs is improved efficiency to extend the battery life of the mobile appliances the PMICs are used in. In synergy with this, is

lower power consumption of the applications they support.

PMIC Device Overview

The block diagram in Figure 2 shows a PMIC designed to supply multiple voltages to a complex consumer device (in this case, a cellphone). A stand-alone PMIC would be very similar, but would have fewer low-dropout (LDO) outputs and interfaces. The colored blocks are functions internal to the PMIC device, while the white blocks are functions interfaced to the outside of the device.

Figure 2. PMIC Block Diagram for a Cellphone



The battery control monitors incoming power sources and charges the main battery as needed. The voltage reference section contains the bandgap reference, which is used as a reference voltage throughout the device. This section is individually trimmed during test, and accuracy is critical for the remainder of the device to pass required manufacturing tests. Accuracy is covered further in the next section. The clock and timing section provides clock distribution and timing to the digital logic section and determines the device power-up and power-down sequences. The device has a very specific

process to go through for each of these operations to avoid damage caused by surges or overloads. The LDO regulator section provides the different voltages and currents to the different “power domains” the PMIC supplies. A power domain is an individual supply separate from the other supplies. In SoC devices, this is very application-driven and could encompass as many as 20 or more domains. The LDO allows for a diminutive difference in the voltage between the input and the output (I/O), which allows a much greater range of input voltages still supplying the correct output voltage. This block also contains boost (step-up) and buck (step-down) voltage functions used internally. The liquid crystal display (LCD) driver drives the phone video display, and the interface section complies with different interface standards to move video, digital and audio data in and out of the PMIC. Other functions in this section include the speaker I/O used to interface the phone’s microphone and speaker, the keypad interface and the motor driver for “silent mode” ringing. Voltage “level shifters” are used to interface to the subscriber identity module (i.e., SIM card), and the Universal Serial Bus (USB) data interface is most common.

Critical Tests

This article will focus on critical tests and provide an economic perspective.

The bandgap reference test is critical because based on the accuracy closest to its designed value, the part will fail (or not) because the other voltages of the LDOs use this reference. This means that a good part could fail if the reference is trimmed incorrectly, or a marginal part can be made to pass by having a very accurate trim.

The test carries out several “trims” or voltage measurements and then a correction, usually by using a digital register (DR) value or by blowing fuses inside the device connected to resistor trees to correct the voltage value. Voltage accuracy is critical for this test, not only to get parts to pass, but also because the production pass yield can be improved by a more accurate trim. Voltage measurement accuracies in the 200 ultraviolet (UV) range can have a positive impact on test economics by improving yield.

The clock and timing tests measure the frequencies of the clocks internal to the PMIC that supply the timing throughout the IC. The clocks also feed the digital logic block, which controls much of the functionality of the device through register control. This influences the control of the other blocks, including the battery control section which will determine the best power source and also when to charge the battery. This is even an important safety issue because most cellphones use lithium-ion (Li-On) batteries which can overheat and even explode if charged incorrectly.

LDOs are “mission-critical” test items. Two critical tests include the testing of:

- Line regulation, where varying input voltages simulating a battery voltage discharging should produce the same output voltage.
- Load regulation, where different current loads (at the output) simulating various features on the phone being used on-demand should produce the same output voltage.

Economic Challenges

Typically, PMICs integrated into SoCs require fewer tests than standalone PMICs. This is because many of the PMIC functions are already tested by tests which exercise the SoC functional blocks,

while stand-alone PMICs have no such luxury. Thus, the ratio of the number of tests from stand-alone PMICs as compared to the SoC-integrated PMICs can be 5 to 1; however, the stand-alone PMIC has a much lower average selling price (ASP) than the SoC-integrated one. As such, a different set of rules must apply to the economics of testing them.

Add to this the technical differences between the two, and different capabilities emerge from an economic perspective of tester requirements.

Stand-alone PMIC Tester Requirements

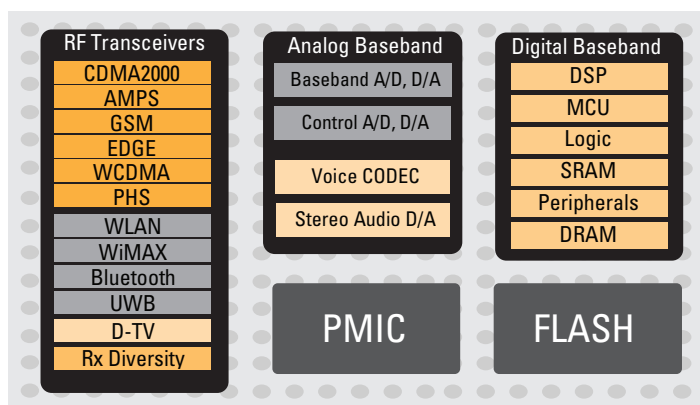
The tester must have the capability to test the PMIC functions shown in Figure 2, including the digital capability for the logic and registers, high-precision DC pins for the LDOs and bandgap reference, higher power DC resources for the power supplies and audio type (1–3 KHz) source and measure capability for the speaker and microphone functions (Figure 2). Since there is much more testing of PMIC functions for a lower ASP part, this requires much more parallelism of test in terms of the functions of individual device (concurrent test) and much more multi-site parallelism. Concurrent test is the ability to test separate blocks within the device in parallel. For example, the design of the device could allow the LDOs to be tested in parallel with the LCD driver (Figure 2). To maximize this, the tester must be configured to test as many functional intellectual property (IP) blocks in parallel as the device design will allow, and at the same time test on the order of eight to 16 devices in parallel with multi-site efficiency (MSE) in the 95 percent range. This means additional devices take on the order of 5 percent additional test time as the initial device.³ For example, at 95 percent MSE, a single-site test time of 4 seconds would take 5.2 seconds to test eight devices.

SoC-integrated PMIC Tester Requirements

The tester must have full capabilities to test the PMIC part of the device listed above and also the SoC part of the device, which performs the end application. Figure 3 shows a generic example of a single-chip cellphone which would require:

- Radio frequency (RF) capability for the RF transceiver front-end.
- Analog mixed-signal capability for the baseband analog-to-digital (A/D) and digital-to-analog (D/A) blocks.
- Voice codec and audio functions.
- Digital capability for the digital logic, digital signal processor (DSP) and microcontroller unit (MCU) onboard the IC.

Figure 3. SoC-integrated PMIC Block Diagram



GLOBAL MARKET TRENDS

ASIA

10% – The maximum share allowance for Chinese investors in Taiwan's local thin film transistor liquid crystal display (TFT-LCD) panel and semiconductor industries. – *Ministry of Economic Affairs (MOEA)*

\$7.1 billion – Estimated revenue for light emitting diodes (LEDs) in China by 2014, up from \$3.4 billion in 2009 and representing a compounded annual growth rate (CAGR) of 12.8%. – *IHS iSuppli*

16.5% – Japan's share of global consumer electronics equipment factory revenue in 2010. – *IHS iSuppli*

1 – The Asia Pacific's (outside of Japan) ranking in semiconductor production among the world's major chip manufacturing regions. The Americas ranked No. 2, Japanese-headquartered companies ranked No. 3, and Europe, Middle East and Africa (EMEA) ranked No. 4. – *IHS iSuppli*

6.2% – Japan's share of the world's large-sized LCD panel production in 2010. – *IHS iSuppli*

\$11.6 billion – Estimated value of Indonesia's consumer electronics industry by 2014. – *Research and Markets*

\$63.3 billion – Value of microchip revenue in 2010 for companies headquartered in Japan, representing 20.8% of the worldwide market. – *IHS iSuppli*

\$22.1 billion – Forecasted value of Taiwan's foundry industry by 2013. – *Digitimes Research*

130 – Number of production semiconductor fabrication lines in 53 locations in Japan. – *IHS iSuppli*

18% – South Korea's share of the small/medium LCD panel market. – *IHS iSuppli*

51.5 million – Number of LCD TV units exported from China in 2010, up from 39.7 million units in 2009. – *IHS iSuppli*

58% – Taiwan's share of the small- and medium-sized LCD panel market. – *IHS iSuppli*

\$4.7 billion – Forecasted value of China's microcontroller (MCU) market by 2015, representing an expansion by two-thirds from the \$2.8 billion recorded in 2010. – *IHS iSuppli*

51% – South Korea's share of the large-sized LCD panel market. – *IHS iSuppli*

\$783 million – China's MCU revenue derived from the industrial market in 2010. – *IHS iSuppli*

\$100 million – Forecasted capital spending for China's long-term evolution (LTE) market in 2011, with \$300 million expected in 2012 and \$600 million in 2013, ultimately hitting \$1.3 billion by 2014. – *IHS iSuppli*

1,500 – Estimated number of active base stations in the Philippines supporting 802.16e WiMAX. – *In-Stat*

<10% – Taiwan-based companies combined share of the global market for analog ICs in 2010. – *WorldWideTech & Science*

27% – South Korea's share of the display driver semiconductor market. – *IHS iSuppli*

33–36% – Gross margin for Taiwan's IC suppliers in 2010, down from 43% in 2008. – *WorldWideTech & Science*

80% – Percentage of mobile personal computers (PCs) produced in the Shanghai area. – *IHS iSuppli*

85% – Asia's predicted share of worldwide photovoltaic (PV) cell

production by the end of 2011. – *IMS Research*

10% – Japan's share of worldwide dynamic random access memory (DRAM) manufacturing supply based on wafer production. – *IHS iSuppli*

97% – Percentage of the rare earth global market controlled by China. – *Deutsche Welle (DW-World)*

49% – South Korea's data Flash memory (NAND) contribution. – *IHS iSuppli*

+300 – Number of businesses specializing in PV applications in China. – *IHS iSuppli*

25% – Percentage of the world's semiconductor wafer supply suspended by Japan's magnitude-9.0 earthquake in March 2011. – *IHS iSuppli*

+3 billion – Projected number of cellular subscriptions in Asia-Pacific by 2015. – *In-Stat*

59% – South Korea's DRAM contribution to global electronics production. – *IHS iSuppli*

25% – Percentage of cellphones made in Shenzhen. – *IHS iSuppli*

INDIA

\$10.2 billion – Forecasted value of India's semiconductor design market in 2012. – *Indian Semiconductor Association (ISA)*

3,000 – Number of engineering schools in India, with a capacity for 1.5 million students. – *National Association of Software and Services Companies*

\$5 billion – Estimated cost for two second-hand fabs in India. – *Ministry of Communications and Information Technology*

8% – Price increase for flat-panel TVs in May by electronics companies in India due to a shortage of panel and semiconductor supply. – *The Economic Times*

\$10.2 billion – Estimated value of India's very-large-scale integration (VLSI) and embedded systems design market in 2012. – *ISA*

12–15% – Planned wage increase for India-based staff at Wipro Ltd., India's third largest software services exporter. – *The Financial Express*

160,000 – Number of people employed by the Indian semiconductor design industry in 2010, with approximately 82% of jobs in the embedded software space. – *ISA*

EUROPE, THE MIDDLE EAST AND AFRICA (EMEA)

297 million – Estimated number of cellular machine-to-machine (M2M) connections worldwide by 2015, with 110 million in Europe. – *ABI Research*

81% – European countries share of the worldwide solar PV installations market in 2010. – *Digitimes Research*

\$230 million – Forecasted capital investment for Israeli start-ups in 2011. No capital investments were made in Israeli start-ups in 2010. – *International Data Corporation (IDC)*

7,000 – Predicted number of LTE base stations to be deployed in France in 2014. – *In-Stat*

\$3.1 billion – Value of Europe's semiconductor materials market in 2010, representing a 25% year-over-year (YoY) increase from the \$2.51 billion reported in 2009. – *SEMI*

45% – Europe's predicted share of the worldwide PV cell market in 2014, down from 78% in 2010. – *IHS iSuppli*

5,000 – Predicted number of GSM GPRS & EDGE/EDGE+ base stations deployed in Nigeria in 2011. – *In-Stat*

7 – Number of old reactors shut down in Germany following the crisis at Japan's Fukushima Daiichi nuclear plant. – *IHS iSuppli*

THE AMERICAS

7.5% – Brazil's economic growth in 2010, making Brazil's economy the fifth largest in the world. – *Future Horizons*

15.6% – Projected CAGR for the U.S. renewable manufacturing and technology market for the time period 2010 – 2015. – *Zpryme & ICP projection*

\$5 billion – Forecasted business spending on non-handset 3G and 4G services in the U.S. by 2014. – *In-Stat*

6.6 – Number of portable devices, on average, that U.S. buyers of Apple iPads (in 2010) reported owning, including notebooks, smartphones, MP3 players and portable navigation devices. – *IDC*

22% – YoY growth of new base stations in Canada in 2010. – *In-Stat*

22.5% – Percentage of TVs bought in the U.S. in Q4 2010 that were LED-backlit LCD TVs. – *IHS iSuppli*

185,000 – People in the U.S. employed by America's critical semiconductor industry, which provides the enabling technology for America's \$1.1 trillion high-tech industry, with a U.S. workforce of nearly six million people. – *Semiconductor Industry Association (SIA)*

\$1.7 billion – Amount spent by North America on LTE infrastructure for 2011. – *IHS iSuppli*

77% – The top 20 fabless IC suppliers' combined share of the \$59.9 billion fabless market in 2010, with U.S.-based suppliers capturing 9 of the top 10 places and 13 of the top 20 positions. – *IC Insights* ■

ELECTRONIC SYSTEM DESIGN CONSIDERATIONS TO MEET EMERGING MARKET NEEDS

AVEEK SARKAR, VICE PRESIDENT, PRODUCT ENGINEERING AND SUPPORT, APACHE DESIGN SOLUTIONS INC.

The use of smartphones has expanded from the corporate market to the mass consumer market as these devices perform an increasing number of applications and functions. The overall smartphone market is expected to grow by 49.2 percent in 2011, with 450 million smartphones expected to be sold in 2011¹. As the penetration of mobile handsets continues to saturate developed countries, handset manufacturers are focusing on emerging markets, especially Brazil, Russia, India and China (BRIC), which represent a significant market, both in terms of current and new users. However, though the BRIC markets have been serviced by traditional cellphones that provide voice and texting needs, consumers in these economies are increasingly demanding smartphones that deliver several additional functions and provide a platform to enjoy the myriad applications available².

Statistics indicate that the forecasted increase in mobile handset sales in the emerging economies will be derived from the sale of smartphones. In 2011, the smartphone market is expected to grow more than four times faster than the overall mobile phone market¹. Driven by the growing popularity of digital electronic products such as flat-panel TV sets and smartphones, and with a total market opportunity expected to reach \$38.4 billion by 2015, Brazil is undoubtedly an attractive market³. According to Nielsen, the sale of smartphones in Brazil was up 128 percent in 2010 compared to 2009⁴. Also, Nielson predicts that China's smartphone market will experience the largest growth worldwide, reaching sales of close to 100 million units in 2015⁵. In Russia, the handset market is expected to grow to \$5.4 billion, aided by the growing demand for smartphones and 3G handsets⁶.

The growth in these markets will be driven by the adoption of the burgeoning middle class and falling handset prices. The majority of these middle-class consumers are extremely cost-sensitive, and handset manufacturers have to respond accordingly. In the Nielsen report, the average price of smartphones dropped 2 percent in the first six months of the year, compared to the same period in 2009, and by 5 percent against 2008⁴. These same consumers also change their phones frequently, looking for new and improved functionalities such as frequency modulation (FM) tuners, MP3 playback and global positioning system (GPS)-based location services⁴. They also demand faster response time and increased battery life from handsets⁷. To meet the needs of this market, handset manufacturers must turn customized designs around quickly using advanced processors and radios, while

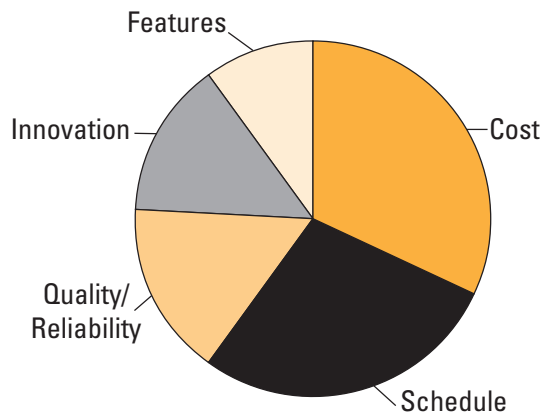
keeping component costs down as much as possible across the supply chain.

The Market Challenges

These industry trends present opportunities and challenges for IC and handset design teams. To meet application requirements, IC designs will need to become increasingly sophisticated, providing support with multiple processor cores and radio frequency (RF) circuits that need to be simultaneously power-efficient and high-performance⁷. For example, the upcoming OMAP5 processors from Texas Instruments feature two Cortex-A15 cores running at 2 GHz along with two Cortex-M4 low-power processors that are fabricated using 28 nanometer technology⁸. The upcoming Snapdragon processors from Qualcomm provide speed up to 2.5 GHz on multi-core architectures using 28 nanometer process technology and integrating multiple radios that allow Wi-Fi, GPS, Bluetooth and FM connectivity⁹. These processors integrate dual-channel low-power double data rate (LPDDR) memory interfaces to provide high-speed connectivity between the application processors and the increased memory. To address low-cost market needs, ARM has introduced single-core and multi-core versions of the Cortex-A5 processor design. These are also planned to run at GHz speeds using advanced process technology nodes¹⁰.

For handset manufacturers and IC suppliers, the challenge involves meeting rapidly evolving market needs while managing margins. This becomes increasingly relevant because multiple handset manufacturers are converging on a few common platforms. Take the case of the Android operating system, which is poised to become the leading platform this year¹. The margins enjoyed in the early days of its adoption period may erode as consumers increasingly base their choices on the prices of handsets and certain specific features introduced from a collection of similar looking handsets all running the same platform¹¹. Thus, handset manufacturers will have to differentiate by marketing certain unique functionalities in their devices. Time-to-market will be critical as others rush to introduce equivalent technologies to match and exceed what was previously introduced. To survive in the increasingly competitive landscape of decreasing margins, especially the BRIC markets, these handsets must be introduced to the market quickly and at the lowest cost. Figure 1 underscores this trend showing that the top market factors driving product design goals are cost and schedule, followed by the need to innovate and differentiate¹².

Figure 1. Factors Driving Product Design Goals



Source: Aberdeen Group, June 2010

Result from survey of 157 respondents ranking the top two factors cited leading to increased product success¹².

The Technology Challenges

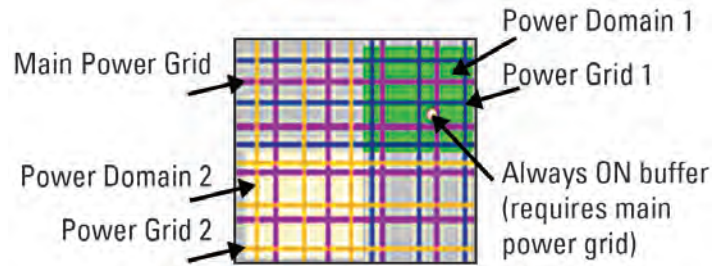
An electronic circuit operates by drawing current or power from the battery or regulator. This flow of current through the IC, package and printed circuit board (PCB) interconnects causes fluctuations or deviations from the nominal supply voltage (also known as power/ground noise). The electronic circuits that constitute the advanced application processors used in smartphone handsets must operate at GHz+ speed, drawing minuscule amounts of current to conserve battery life. To reduce their power consumption and meet 28/22 nanometer technology requirements for reliability, these processors must operate at extremely low supply voltage levels. However, supply voltage scaling has not seen a commensurate decrease in the threshold voltage of the metal-oxide semiconductor (MOS) devices that make up these circuits (Figure 2c). This reduces the noise margin that acts as a buffer for an electronic circuit against power/ground noise and increases the chance of failure or performance reduction. This is especially true for high-performance portions of a design such as the processor core, graphics engine or the high-speed input/output (I/O) DDR interface. These circuits operate at high speed and have the smallest tolerance against any fluctuations from the nominal. Predicting the level of power/ground noise accurately is therefore required to understand where corrective actions must be undertaken.

However, accurate prediction of power/ground noise is a complex problem since it is a function of several factors, including the activity on the chip, the current drawn for various operations, the available decoupling capacitance and chip-package-system (CPS)/PCB power delivery network (PDN) parasitics. The estimation of power/ground noise requires detailed time domain simulations which, unlike a static or direct current (DC) voltage drop analysis method, can include a myriad of factors to predict noise levels and model the impact of this noise on the IC's performance. Timing or on-chip cross-talk noise analysis can be partitioned and solved on a local scale. But power/ground noise is both a local and a global system-wide problem. Localized switching causes areas of "hotspots" during critical periods of a circuit's operation, while the overall chip current interacts with the CPS parasitics affecting the power supply of the entire chip.

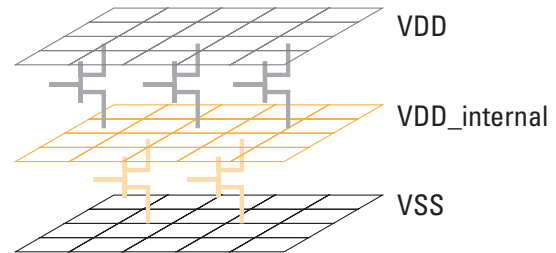
Given the shared nature of the power/ground network in a CPS PDN, and the capacitive and inductive coupling that occurs between the various components, the power/ground noise analysis requires a comprehensive full-chip and system-level approach that considers all

switching sources, all current flow pathways and all parasitic elements. This is increasingly important as circuits adopt complex design techniques to control power in a chip while ensuring the highest levels of performance. Figures 2a and 2b highlight some of these commonly used methods, which add increasing layers of complexity in these circuits that already must contend with lower supply voltages (Figure 2c), increasing functionality, speed requirements and smaller process technologies (Figure 2d).

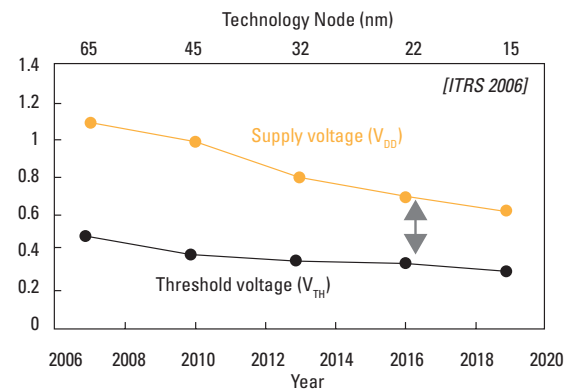
Figure 2. Technology and Design Trends that Impact the Design and Reliability of the Power Supply Network



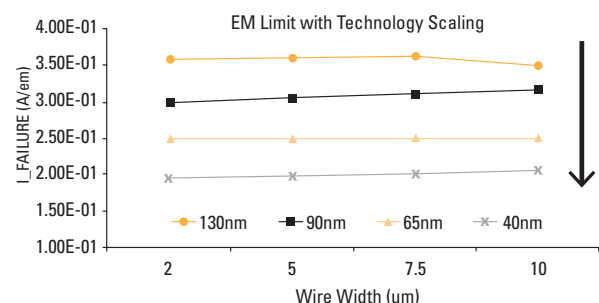
(a) Multiple voltage islands



(b) Power gates/MTCMOS



(c) Shrinking noise margin in low-power designs from lowering supply voltage. Figure 2c is from ITRS reports¹³.



(d) "EM" limit decrease in advanced technology nodes impacting circuit reliability. Figure 2d is extrapolated from¹⁴ modified following personal communication with the authors.

Aptina Imaging is a fabless provider of complementary metal-oxide semiconductor (CMOS) imaging technologies and solutions with a growing portfolio of high-quality imaging products that can be found in all leading mobile phone and notebook computer brands as well as a wide range of products for digital and video cameras, surveillance cameras, medical, automotive, industrial, video conferencing, barcode scanners, toys and gaming applications across the globe.

A leading innovator of new CMOS imaging technologies, Aptina invests in solutions to the hard engineering problems and the rapid delivery of these technologies with industry-leading performance and reliability. Aptina A-Pix technology, for example, is a series of advanced pixel technologies featuring lightguide and deep photodiode and 65 nanometer pixel design rules that cost-effectively advance pixel performance. With Aptina's A-Pix technology, mobile phone camera users have access to the picture quality and overall imaging experience as close as possible to that available with a digital still camera. It also enables a new class of hybrid camera that combines digital still image capture with advanced high-performance, high-definition

(HD) video. Aptina DR-Pix is another example of innovation the company is integrating into its products to improve performance and reliability.

A core focus for the company is dedicated customer support from concept to launch, thus enabling Aptina customers to be first to market with the best possible sensor technology. The company is able to offer flexibility, fast cycle times and tremendous supply chain advantages through key technology partnerships and industry relationships, such as with the Global Semiconductor Alliance, that enable customers to meet the needs of an ever-changing marketplace. ■

"GSA enhances our ability to connect to key industry leaders, and the organization offers outstanding research. Each of these helps make Aptina more relevant to our customers and partners, and more informed about the industry as a whole."

— Dave Orton, CEO, Aptina Imaging Corporation



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THIS SECTION IS DESIGNED TO ACQUAINT READERS private showing WITH GSA'S PRIVATE SEMICONDUCTOR MEMBERS

BeSang Inc. is a pioneer in the design, development and delivery of unsurpassed three-dimensional (3D) IC solutions, providing unmatched process and design technologies for 3D IC as well as technology licenses to customers. The company's proprietary and cutting-edge True 3D IC technologies enable vertical stacking of multiple device layers and offer ultra low-cost and high-performance solutions to central processing unit (CPU), digital signal processor (DSP), graphics processing unit (GPU), application-specific IC (ASIC), field-programmable gate array (FPGA), system-on-chip (SoC), dynamic random access memory (DRAM), standard random access memory (SRAM), Flash, image sensor and solid-state drive (SSD) applications.

Having accumulated eight years of experience in 3D IC since being incorporated in 2003, BeSang has successfully developed True 3D ICs and currently holds more than a dozen foundational patents around the world. The first prototype of True 3D IC was successfully demonstrated in 2007 at Stanford NanoFab, and the commercial-level sample was demonstrated in 2008.

Presently, BeSang is working on a market introduction of True 3D IC products for the first time in the industry. The first volume production of memory devices made in this technology is expected to be available to the market in 2012. It is anticipated to eventually change the semiconductor industry standard from two-dimensional (2D) device shrinking to 3D stacking.

BeSang was listed as one of the 60 emerging start-ups in EE Times' 2009 Silicon 60, and was also tipped as the "3D IC winner" by market research company Frost & Sullivan. "3D IC Architecture and Business Model for High-density Memories," an article co-written by President and CEO Sang-Yun Lee, was featured in the March 2010 issue of GSA Forum. The fabless semiconductor company is headquartered in Beaverton, Oregon. ■

BeSang Inc.
TRUE 3D IC Solutions

"BeSang has been a member of GSA since 2007. GSA is an invaluable resource that provides an excellent environment in which BeSang can connect, gain insight and share information with others in the semiconductor industry."

— Sang-Yun Lee, President and CEO, BeSang Inc.

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MEMORY SOLUTIONS FOR MEDICAL, SMART GRID, INDUSTRIAL AND OTHER LONG-LIFECYCLE APPLICATIONS

SEAN LONG, MARKETING DIRECTOR, INDUSTRIAL, MEDICAL AND MILITARY MARKETS, INTEGRATED SILICON SOLUTION INC.

The memory needs of medical device and industrial equipment manufacturers are very different from those of personal computer (PC) and consumer product manufacturers. This presents unique challenges to the project team (i.e., product, design, quality and component managers, and engineers) requiring them to evaluate their memory solutions closely to ensure they can support their stringent requirements. The characteristics of a typical embedded system memory are defined below:

- Long product lifecycles: Seven to 10 years is typical, and often up to 15 years.
 - Significant development and qualification time.
 - Long production life.
- High-quality and reliability requirements: Over an extended temperature range, embedded systems place an emphasis on quality and reliability. The “five nines” expectation (99.999 percent uptime) means that quality starts from design and continues through manufacturing with the expectation of a long operating life.
 - Rugged products (e.g., including copper lead frame options for enhanced reliability at extended temperatures and long life without risk of “whiskering”).
 - Extended temperature range: must support negative 40 C to 85 C and have the option for extended temperatures to 105 C or 125 C.

High-mix, low-volume market segments have special needs in terms of industry specifications, strict qualification cycles, long-life requirements (without product changes permitted), and extremely long in-field use with the highest reliability standards expected.

The challenge for memory vendors is to ensure that by the end

of the design cycle they meet the requirement for long-term support covering extended production time with minimal design changes.

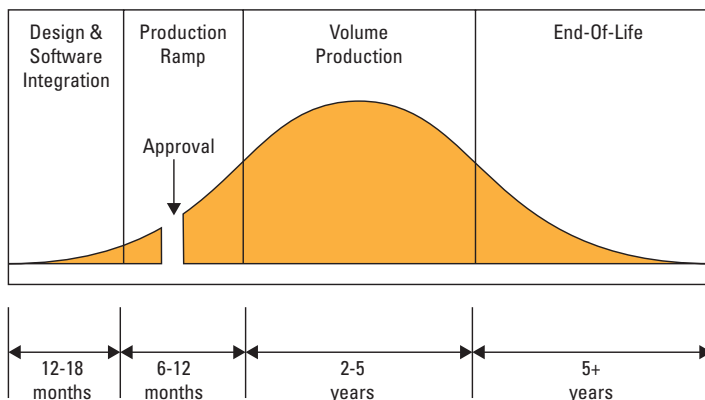
Medical and Industrial Embedded System Product Lifecycle

The typical industrial embedded system has a design and qualification cycle of one to three years, followed by a five- to 10-year production and ramp-down period. For many industrial systems, there is also an extended requirement to support installed equipment, requiring “spare” products to be available for an additional five years or more.

Example: Embedded Systems Requiring Long-term Support for Memory

Embedded systems have a significant development and qualification time, as well as production time. A typical product lifecycle (Figure 1) helps explain why it is critical to have a memory partner that guarantees long-term support.

Figure 1. Typical Embedded System Product Lifecycle



System	Design	Approval	Production
Medical Device	Prototype & software development	Federal Drug Administration (FDA) defines different classifications for medical devices, requiring different level of approval / qualification. May take up to 12 months for approval.	For Class 3 products, any component change may require FDA re-certification.
Factory Automation / Logic Controller	Often redesign a card to fit in existing form factor or set of interfaces.	After reliability testing at the PCB level, the end user will qualify the new card within their deployed system.	In complex systems, component or software changes are often prohibited.

Phase 1: Design, Approval and Production Ramp

In the design, approval and production ramp phase, it is critical that the selected memory vendor does not change a die revision for a product undergoing approval. Many commodity memory vendors perform frequent die revisions, making it extremely costly if an embedded system must be requalified by a regulatory body.

Embedded system microcontroller units (MCUs) typically have built-in support for a memory interface via a port such as an external memory interface (EMIF) with an integrated dynamic random access memory (DRAM) controller. At the time a MCU series is designed, the semiconductor vendor selects the type of memory interface (i.e., product family) to support (e.g., synchronous dynamic random access memory (SDRAM) or double data rate 2 (DDR2) SDRAM). With leading embedded processor vendors offering “product longevity programs” guaranteed to support defined devices for a minimum period of 15 years, the question the system engineer must ask is “Will my memory devices still be available in 15 years?”

Phase 2: Volume Production

Once in production, the memory vendor needs to maintain long-term support for the product family, preferably with the initially qualified die revision. In addition, the memory vendors have to ensure the highest levels of quality and reliability. At some point during an extended product lifecycle, the memory vendor may introduce a die shrink product. However, those vendors with a strategy for long-term support continue to offer the product family in both current and next-generation processes to minimize any requalification for the embedded system designer.

The phrase “design shrink” is often used by semiconductor vendors to denote a new generation of product manufactured on a more advanced process node (e.g., moving from 90 nanometer to 65 nanometer nodes). Memory devices such as DRAMs are designed to JEDEC-defined standards to ensure functional and pin compatibility between different vendors’ products. While a vendor may claim “100 percent compatibility,” many embedded system engineers have learned from experience that while the devices may meet all published datasheet specifications, when they are tested in a real-

world environment they often experience incompatibilities due to the unique nature of their application.

Phase 3: End-of-life/Sustaining Mode

Successful products continue to sell in low-to-medium volumes even as new generations are released. Furthermore, products with a large installed user base still require support for spares. All of this requires a memory vendor who can offer seven- to 10-year support. In such scenarios, memory vendors need to support an extended life with high-mix, low-volume manufacturing strategies.

The product life between consumer memory shrinks may be as short as six to nine months, which is not usually an issue for consumer products, but is a major headache for embedded systems. Embedded system engineers must consider the following memory issues for long-life markets:

- **Requalification of a new die revision:** Are the two products 100 percent compatible in the target application?
- **Time:** How long does it take to qualify the new die revision in the system and at end customers compared to the short-term availability of the consumer memory product?
- **Resources:** With engineering resources typically focused on new product development, who can support the requalification? Plus, for many older systems, the original engineer may not even be with the company.
- **Cost:** Requalification can be a significant expense, particularly if the complete system needs to undergo regulatory approval with extra testing and delays.
- **End-of-life (EOL):** The worst-case scenario is where the memory vendor has made the product type obsolete and announces an EOL. Semiconductor vendors usually support a last time buy (LTB), but the length of time where a product can be ordered is typically only around 12 months. If the embedded system is in the early part of its product life, this forces the company to forecast total volume over the lifecycle to purchase and store the memory as inventory. This can be extremely costly with significant upfront cash flow required, and there is always the potential concern of system demand exceeding the forecast.

Industrial Equipment Requiring Enhanced Quality and Reliability

Industrial equipment is often exposed to extended temperatures and harsh environments, requiring at the die and packaging levels higher quality and long-term reliability from the semiconductor components. To address these applications, memory vendors must design and test rather than screen for quality.

Die-level Reliability

For industrial applications, the memory must be tested to ensure operation at both temperature extremes, typically 85 C or 105 C for hot and negative 40 C for cold. In addition, the test flow needs to consider how to remove both infant mortality effects (i.e., early failure) as well as ensuring long-term reliability. Reliability engineers are familiar with the “bath tub” curve shown in Figure 2. The memory flow shown in Figure 2 addresses infant mortality with 100 percent burn-in using both temperature and voltage acceleration factors. In addition to testing over the full temperature range, the test flow uses wafer lot-based sampling to perform a calculation for early life failure

An inside look at innovative semiconductor start-ups

Start-ups often rush out of the gate with a technological focus, but struggle to find a mass market. **GreenPeak Technologies BV** appears to have gone through that process before latching onto the remote control market. GreenPeak was formed in July 2007 through the merger of Xanadu Wireless and Ubiwave to develop ultra low-power wireless modules for wireless sense and control applications. GreenPeak's mission is "to be a leader in the next wireless revolution and to help build a greener world." The company is focused on ZigBee RF4CE and ZigBee GreenPower for wireless and batteryless light switches.

Infrared (IR) remote controls have been around for ages, yet have several limitations. They require line-of-sight to function, only provide one-way communication and have low data rates. In contrast, a ZigBee RF4CE remote control system (compliant with the IEEE 802.15.4 standard, operating in the 2.4 GHz global frequency band) is faster, more reliable, includes richer bi-directional communication and provides greater range.

GreenPeak is focused on capturing this emerging market opportunity and has developed a family of ICs allowing for the development of robust and low-cost ZigBee RF4CE remote control applications for TVs and set-top boxes (STBs). The company offers RF4CE ICs for STBs and TVs, and a complete low-cost "remote control on a chip."

The company's ultra low-power and synchronization optimized for remote controls enables single-coin cell battery operation for 10 years or more. The devices offer excellent interference robustness against Wi-Fi, Bluetooth and other radio frequency (RF) signals that operate in the 2.4 GHz band. The devices are optimized for low cost, ease of integration and fast time-to-market by requiring only a simple configuration step to achieve a complete RF4CE-compliant end product.

The bi-directional RF4CE controller chips also enable value-added features such as "find-me" and "push-messaging" applications

with minimal impact on battery life. Push-messaging enables new remote control capabilities such as tele-voting, gaming, personal messages, reminders, real-time sports results, stock information, residential sensor network monitoring and advertising. Find-me enables users to push a "find-me" button on the TV or STB, which generates an alert on the remote control.

GreenPeak believes it is addressing an overall annual market of 1 billion units. A recent report from IMS Research forecasts that over 250 million RF4CE ICs will be shipped in 2015, driven by a strong transition in remote controls from IR to RF. Several semiconductor companies are targeting the ZigBee RF4CE market. With a growing family of highly optimized devices designed to serve this market, GreenPeak appears well-poised to capture this opportunity. The company argues that its advantages include robustness to Wi-Fi interference and ultra-low power, which results in no battery replacement during the expected lifespan of the remote control. ■

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OVERCOMING THE STABILITY BARRIER TO HIGH-DENSITY MRAM

BARRY HOBERMAN, CHIEF MARKETING OFFICER, CROCUS TECHNOLOGY
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Successful memory chips must support a wide variety of specific performance and reliability requirements. The physics, technology and design of each memory type dictate the specifications which define the memory's reliability and performance envelope. At the IC level, data retention, write endurance, susceptibility to ionizing radiation, read and write access and cycle time, read and write voltage requirements, and power are sensitive to the physics and characteristics of the core storage element.

For example, information in dynamic random access memory (DRAM) is stored in the form of an electrical charge retained in a small capacitor. The characteristics of the capacitor and surrounding circuits directly affect data retention, susceptibility to ionizing radiation, read voltage, read access time and power. The charge tends to leak out of the capacitor, and so the device requires a regular charge refresh (which requires power) to maintain reliable data retention over extended periods of time. If power to the device is shut down, the charge stored on each capacitor leaks away rapidly and the data is lost, hence DRAM's designation as "volatile memory." Flash memory is a type of "non-volatile memory" (NVM), which characteristically retains its stored information when power is removed from the chip. Stability of stored data in NVM (regardless of whether power is applied or not) is a key performance specification in such devices.

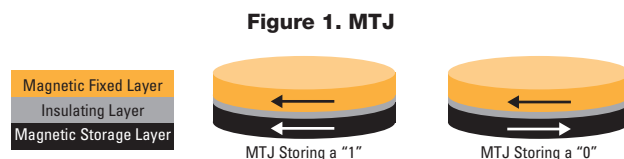
Magnetoresistive RAM (MRAM) is a memory technology that blends the best characteristics of volatile and non-volatile memories. In MRAM, as in Flash memory, data storage is non-volatile, but the write endurance of the memory cell is unlimited, and reading and writing are very fast (similar to DRAM and static RAM (SRAM)). As with other memory technologies, MRAM is constrained by its own physical limits to define the chip performance envelope. Data retention is governed by the fundamental stability of the physical quantity being stored. In a magnetic memory, magnetic polarization is stored rather than electrical charge. This is achieved by controlling the orientation of magnetization in a small magnetic element (analogous to the orientation of a compass needle). As for all memory technologies, data retention is of particular importance and essential

to the future of MRAM as a mainstream memory technology. As such, the stability of the magnetic orientation of the MRAM's bits is crucial.

Thermal Stability in MRAM

At the heart of all memories, a fundamental tension exists between the stability factors that govern data retention and the ability to scale that memory cell to a smaller lithographic feature size. The critical tension in MRAM is that the stability of the magnetic orientation is proportional to the volume of the magnetic particle, so as an MRAM bit is scaled down, its stability generally declines. This destabilizing effect can be countered, however, in several creative ways with differing effectiveness. The various approaches to maintaining MRAM data stability while scaling to competitively small feature sizes (i.e., 90 nanometer and smaller) is one of the distinguishing characteristics of competing approaches to advanced MRAM.

The core storage element in MRAM is a device called a magnetic tunnel junction (MTJ), as depicted in Figure 1. A very thin (1 to 2 nanometer) insulating layer is sandwiched between two thin magnetic layers. In a typical configuration, one of these layers has a fixed magnetic orientation for the life of the device and can be referred to as the reference layer. The second layer, which can be referred to as the storage layer, has a magnetic orientation that can be reversed depending on whether the stored data is a '0' or '1.' The read-back signal is derived from a transverse resistance measurement across both layers and changes from low to high depending on whether the storage layer magnetization is aligned parallel or anti-parallel to the reference layer, respectively.



Stored data follows the magnetization direction (parallel or anti-parallel) of magnetic layers in the MTJ.

The storage layer is designed to have two stable orientations (Figure 1), where the magnetization in the storage layer is either oriented to the left or to the right. Each of the stable orientations has an associated energy level. The energy levels of both orientations are equivalent, but there is an energy barrier to overcome when switching from one orientation to the other. The stability of a given magnetic state over time is intrinsically linked to the magnitude of the energy barrier between the two possible stable orientations of magnetization. It is critical to observe that the ability to write to a new state is also intrinsically linked to the height of this energy barrier. Indeed, during the write process, energy must be supplied to orient the magnetization of the storage layer in the desired direction. The greater the energy barrier between the two orientations, the greater the magnitude of the energy required for the writing process will be. This increase in writing energy tied to an increased stability gives origin to the fundamental tension that exists between the stability factors governing data retention and the ability to scale that memory cell to smaller lithographic feature sizes.

Modeling Memory Chip Stability

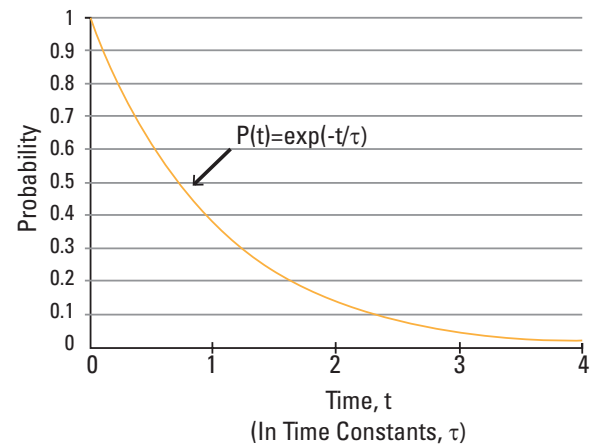
When examining the stability of MRAM, it is important to understand that each individual bit is subject to a potential thermal disturbance of its magnetic orientation, with the previously described energy barrier as the “keeper” of the existing state. The thermal disturbance of an individual bit can be equated to a randomly fluctuating magnetic field that acts to potentially disturb the magnetic state. The magnitude of this equivalent random field is proportional to the device temperature. The effects of such random thermal fluctuations depend on the relative magnitudes of the energy barrier and the available thermal energy, which is proportional to the device temperature. If the energy barrier is high enough, the probability of overcoming it with only random thermal fluctuations is negligibly small. For example, in macroscopic systems such as a compass needle, once magnetized to point north, the needle will continue to do so forever unless it is remagnetized in the opposite direction. If the energy barrier in a MTJ is comparable to the ambient thermal energy available to cause fluctuations, there is a good chance that the orientation can spontaneously flip from one orientation to the other in a random manner within the specified operating life of the device, thus creating a data storage error.

The chance of flipping from one orientation to the other has a mathematical probability profile that is exponential in nature (Figure 2). The characteristic lifetime τ over which flipping occurs depends on the relative magnitudes of the energy barrier and the thermal energy (with the thermal energy quantified as kT , where T is the temperature and k is Boltzmann's constant). The energy barrier is proportional to the volume of the magnetic dot and can be expressed as KxV , where K is an energy density describing the material and shape of the dot and V is the volume of the magnetic dot. Thus, the characteristic lifetime required to overcome such an energy barrier can be expressed as

$$\tau = \tau_0 e^{(KV/kT)}$$

where τ_0 is the minimum time required to reverse magnetization and is typically on the order of 1 nanosecond. It is clear that the energy barrier and characteristic lifetime increases with increasing volume (i.e., the size of the dot), thereby making the dot more stable, but decreases with increasing temperature, thereby making the dot less stable.

Figure 2. Probability of MTJ Data Retention over Time



This characteristic lifetime determines the reliability statistics of a memory chip relating to its data stability. The probability that an individual bit retains its data follows an exponential decay that depends on the characteristic lifetime:

$$P(t) = e^{(-t/\tau)}$$

(where τ is the characteristic lifetime).

In a memory application, the question is now what τ is required, so over the 20-year life of the device, no bits erroneously change state. For a single 64 Mbit device, this would lead to the requirement that

$$P(20 \text{ years}) = e^{(-20 \text{ years}/\tau)} > 1 - (1/6.4 \times 10^7).$$

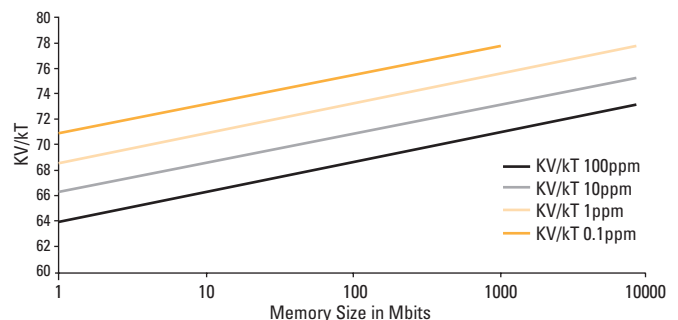
In production, this criterion must apply to all outgoing product, so the requirement becomes even more stringent. Application of the basic rules of probability and straightforward approximations yield the required probability for a given memory density and quality level (typically expressed in parts per million (ppm) of fallout):

$$P(20 \text{ years}, 100 \text{ ppm}) = e^{(-20 \text{ years}/\tau)} > 1 - (\text{ppm_Rate}/\text{Memory_Size})$$

This immediately imposes a lower limit on the ratio KV/kT since $KV/kT = \ln(-20 \text{ years}/(\tau_0 \times \ln(P(20 \text{ years}))))$. For example, for a 64 Mbit memory and a 100 ppm quality level over 20 years, $P(20 \text{ years}) = 1 - 1.6 \times 10^{-12}$, and so KV/kT must be greater than 68.2.

The conventional wisdom within the MRAM community is that production of megabit density memories requires the factor $KV/kT > 60$, which is in line with the above example. Figure 3 specifies this stability requirement by denoting the minimum KV/kT requirement as a function of memory density and acceptable fallout level while assuming a 20-year life.

Figure 3. Minimum KV/kT Required vs. Memory Size



Developers and customers of MRAM technology should evaluate the performance of considered technology against the preceding criteria. The first-generation MRAM technologies, with bit densities up

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PROGRAM

8:30 a.m. Registration Opens

Session I: Outlook, Memory & Supply-Chain Partnership Infrastructure9:15 a.m. Keynote: State of the Industry
Lloyd Kaplan, COO, IHS iSuppli9:45 a.m. Keynote: Flash Memory - The Key to Accelerating Moore's Law (suggested title)
Sanjay Mehrotra, President & CEO, SanDisk Corporation

10:15 a.m. Networking Break

10:45 a.m. Roundtable Session: The Joint-Venture Partnership Model...Supply-Chain Best Practices

11:45 a.m. Networking Lunch sponsored by GLOBALFOUNDRIES

Session II: Technology & Security Optimization Infrastructure1:15 p.m. Keynote: Security & the Smart Technology Evolution
Tudor Brown, President, ARM

1:45 p.m. Panel: Improving Device Performance - Simplifying Software/Hardware Integration

2:45 p.m. Networking Break

Session III: Global Investment Opportunities & Funding Infrastructure3:15 p.m. Keynote: Macro-Economic & Social Trends - The Future of Semiconductor Growth in Emerging Markets
Dan Niles, CEO, Alpha One Capital Partners LLC

3:45 p.m. Panel: Semiconductor Investment - Redefining the Funding Model

4:45 p.m. Conversational Interview

- **Dr. Aart de Geus**, Chairman & CEO, Synopsys, Inc.
- **Scott McGregor**, President & CEO, Broadcom



5:15 p.m. Closing Remarks

5:30 p.m. VIP Reception sponsored by GLOBALFOUNDRIES

7:00 p.m. VIP Dinner sponsored by eSilicon

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THE PERFECT STORM: EXPLOSIVE DEMAND FROM EMERGING MARKETS, RAPIDLY EVOLVING SEMICONDUCTOR TECHNOLOGY AND INNOVATIVE MIXED-SIGNAL SOLUTIONS

RAVI SUBRAMANIAN, PRESIDENT AND CEO, BERKELEY DESIGN AUTOMATION INC.

Trends and innovations can spark a market evolution, but there are times when multiple forces come together and trigger a perfect storm. This is what is happening in the semiconductor industry as we enter the second decade of the 21st century. Demand for electronic products—from computer systems to mobile phones—is maturing into sophisticated consumer-driven platforms that enable instant access to voice, media, social networking, commerce and information, with services localized to specific markets. As a result, the semiconductor industry is dramatically changing, driven by demand from the new middle class in emerging markets, enabled by deep nanometer semiconductor technology, and requiring retooling and innovations in mixed-signal circuit design. This article discusses the drivers, enabling technologies and challenges in this perfect storm.

Evolution of the Electronics Industry

The evolution of computing cycles has been a critical factor in wealth creation worldwide. With each new cycle (currently, the early stages of the mobile Internet cycle), new products ramp faster and in far greater volume, thus fueling growth in the semiconductor industry. Evolutions in computing have enabled innovations in communications and networking, in turn enabling game-changing technologies and services, including wireless (3G/4G), search (Google, Baidu), video (YouTube, YouKu), electronic commerce (Amazon, DangDang) and social networking (Facebook, RenRen). With each evolution in computing cycles, the number of devices connected to networks grows by orders of magnitude—from tens of millions in the minicomputer era to nearly 10 billion in the mobile Internet era.

In 2008, total mobile Internet traffic measured around 33K terabytes per month. The prediction for 2013 is over 2.1 million terabytes per month¹. This compounded annual growth rate (CAGR) of 130 percent is set to continue with the increasing demand for video services over the Internet. Furthermore, with advances in cloud computing, software-as-a-service and cloud storage, individuals are no longer tethered to a desktop personal computer (PC) and are increasingly using wireless appliances to perform their job.

The demand for instant wireless communication is also rejuvenating the auto industry. Automotive electronics no longer

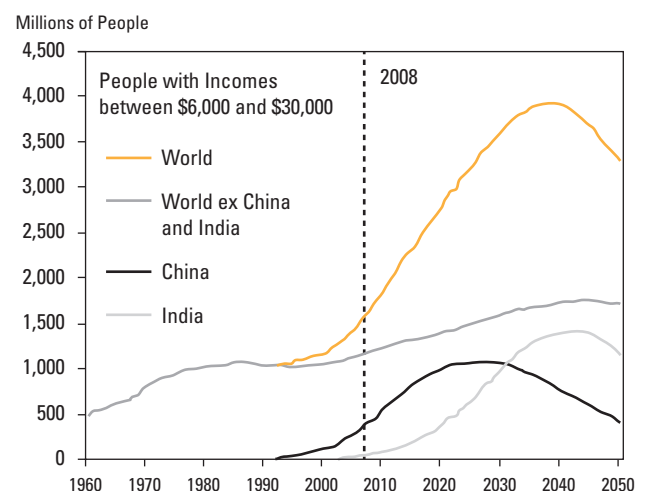
manage only the immediate engine control, transmission and power functionality, but also reach into the wireless universe for navigation, entertainment, tracking and safety. Because of these drivers, analysts estimate a dramatic growth rate for automotive semiconductors.

Finally, electronics is poised to grow significantly in the healthcare industry in the next decade, enabled by advances in computing power, sensors, transceivers and networking and driven by the pressure in the healthcare industry to reduce medical costs worldwide.

Emerging Economies: Defining the Demand Picture

These new product drivers are coupled with significant changes in the supply and demand dynamics for electronic products. Emerging economies are redefining the demand picture for electronics. Explosive demand growth is arriving via the new middle class in emerging markets, as shown in Figure 1². Approximately 460 million people will enter the emerging middle class between 2010 and 2015 (that is 170 people per minute), creating new and rapidly growing electronics markets that span consumer, wireless, automotive, medical, power and lighting applications.

Figure 1. The Expanding Middle Class



Source: Goldman Sachs

These same emerging economies are demonstrating faster gross domestic product (GDP) growth rates compared to the traditional industrialized economies, yet they are characterized by average income levels that are two to 10 times lower than the industrialized economies^{3,4}.

For example, the percentage share of global consumption in China will grow from 6.4 percent in 2008 to 16.4 percent in 2015, with an average per capita income (PCI) of \$3,000. India will grow from 2.2 percent to 3.9 percent with a PCI of \$1,000, while the U.S. will decline from 29.3 percent to 23.5 percent with a PCI of \$47,500.

This shift in worldwide consumption to regions with lower (but still growing) PCI, defines the pressures on the prices of electronic products. Electronic products must be significantly cheaper to capture this new demand. For example, in the mobile communications industry, the sub-\$100 smartphone is one such target for 2012.

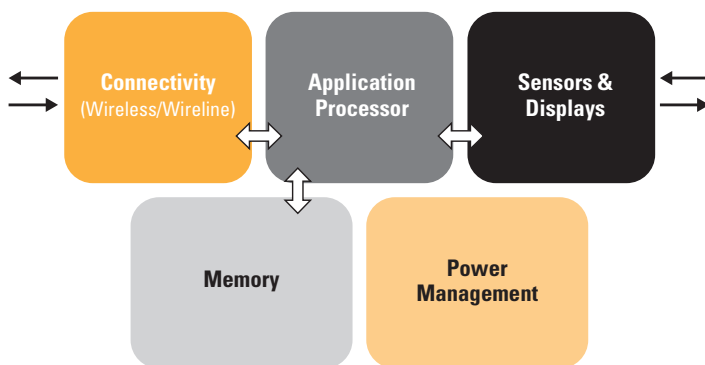
The Response: Platforms and Nanometer Technology

The electronics industry is responding to these challenges with a fundamental shift in product design and production. The old model of specialty products catering to developed markets is giving way to platform-based designs manufactured in lower cost nanometer-scale complementary metal-oxide semiconductor (CMOS) technologies that enable mass customization and localization.

In the old product development model, equipment manufacturers could often rely on new technology and performance as sole differentiators. Consumers would pay a premium to have the latest gadget, thus producers could afford to develop and market unique products. However, to meet the price points that emerging markets demand, producers are moving to significantly reduce product development costs through platform-based designs.

The advantage of a platform-based approach to product development is that it allows a limited number of semiconductor designs to be used in a large number of product applications. The basic components of these platforms include wireless and wireline connectivity, application processors, sensor and displays, memory and power management (Figure 2).

Figure 2. Fundamental Components of Electronic Platforms

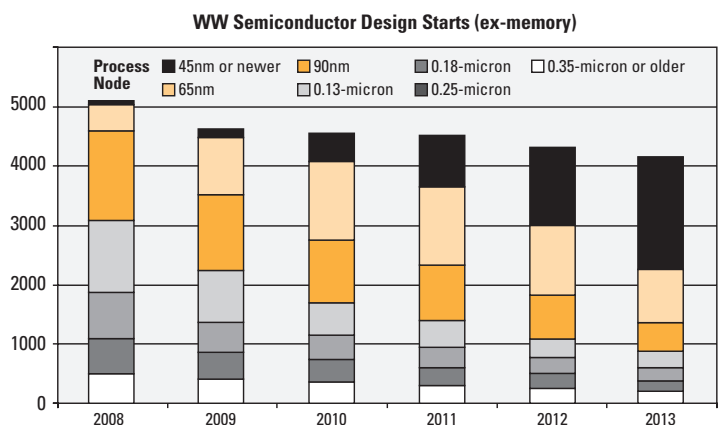


The complexity of these platforms is formidable. One can find application processors running at 1 GHz, radio transceivers delivering 10 Mbits/sec, 10+ megapixel image sensors, multi-axis micro-electrical-mechanical systems (MEMS) accelerometers, gigabytes of memory for video storage, and highly efficient power management and distribution.

These platforms are characterized by increasing mixed-signal content in each component defined by critical functions provided by connectivity, high-speed interfaces, displays and power management. Connectivity refers to transceivers to enable transmission and reception of signals over wired or wireless channels. High-speed interfaces span the gamut from Universal Serial Bus (USB) 3.0, High-Definition Multimedia Interface (HDMI), Peripheral Component Interconnect (PCI), serializer/deserializer (SerDes) and double data rate (DDR) memory input/output (I/O), among many others. Displays include a wide range of image sensors and displays, and power management spans supply regulation, voltage regulation and distribution. Virtually every electronic product platform can be seen via such a platform framework.

The manufacturing cost of platform-based designs is further reduced by prudent integration of digital, analog and radio frequency (RF) circuits in bulk nanometer CMOS processes together with “more-than-Moore” integration technologies. The combination of these techniques can drastically reduce the base cost of the components and platform while improving supply chain logistics and reliability. Figure 3 shows how the pressures of emerging economy price points are rapidly driving the vast majority of design starts for semiconductor platforms into deep nanometer nodes⁵.

Figure 3. Platform Components are Rapidly Moving to Nanometer Nodes



Source: iSuppli, Sept. 2009

The Challenge: Winners Defined by Nanometer Analog/RF/Mixed Signal

The shift to platform-based products in nanometer CMOS technology requires further evolution of digital design methodologies and significant retooling in the analog and RF design domains. Digital design methodologies and tools have evolved over the past two decades along with Moore’s Law for the traditional computing aspects of the new platforms. Typically, at every other new process node, the digital design flow is completely retooled. This includes better synthesis, faster prototyping, lower power methodologies, advanced implementation and design for manufacturing (DFM). As a result, design margin requirements are down and parametric yield meets target.

Whereas the complexity of analog and RF circuits have grown by orders of magnitude, analog and RF tools have typically shown very few improvements over the last decade. The move to bulk nanometer CMOS for analog and RF circuits creates a growing gap between the capability of the existing toolset and the new design and

A PERSPECTIVE ON THE IMPACT OF JAPAN'S DISASTER

BILL MCCLEAN, PRESIDENT, IC INSIGHTS

Researchers estimate that globally there are about 80,000 earthquakes each year, with most too minor to notice. Since the earliest days of IC production in Silicon Valley, the IC industry has always had the majority of its fabrication facilities located in seismically active regions. Moreover, it appears that over time, IC producers and their customers have accepted this situation as a fact of life.

Table 1 shows that in 2010, almost two-thirds of worldwide IC industry capacity was located in seismically active areas. As shown, Japan and Taiwan had essentially the same level of IC capacity in 2010, and, with both countries considered entirely seismically active, had the same amount of IC capacity exposed to potential earthquake damage.

Table 1. Seismically Risky IC Industry Capacity

Region	2010 Capacity* (M of Starts/Yr.)	% of Capacity in Seismically Active Area	Seismically Active Capacity* (M of Starts/Yr.)	% of Total WW Seismically Active Capacity
Japan	32.52	100%	32.52	34.8%
Taiwan	31.92	100%	31.92	34.2%
South Korea	22.56	0%	0.00	0.0%
Americas	21.72	12%	2.61	2.8%
Rest-of-World	15.00	78%	11.70	12.5%
China	12.48	100%	12.48	13.4%
Europe	12.00	18%	2.16	2.3%
Total	148.20	63%	93.39	100%

*200mm Equiv

Source: IC Insights' Global Wafer Capacity 2010-2011

In an attempt to assess the impact of the Japanese earthquake and tsunami on the semiconductor industry, one can only make assumptions regarding the most basic business issues: supply and demand. Taking a top-down approach, the first consideration is worldwide gross domestic product (GDP) growth and how this

growth might be affected by the current situation in Japan.

Effect on GDP

Presently, Japan's 2011 economic growth is impossible to predict. Early estimates indicate that the earthquake and tsunami damage will cause Japan's GDP to decline by 1 to 3 percent in 2011. However, shortly after the first few weeks of the earthquake, the majority of estimates for Japan's GDP growth in 2011 ranged from negative 1 percent to 1 percent. Most economists agree there is little doubt that Japan's economy will take a significant hit in the first half of 2011 and possibly enter a recession (i.e., two quarters in a row of negative GDP). Yet, over the long run, advanced economies facing significant disasters have oftentimes performed better than initially expected as increased investment outlays to rebuild infrastructure helped foster strong economic growth. This rebuilding growth spurt is expected to begin in Japan in the fourth quarter 2011.

Japan represented 7.5 percent of worldwide GDP in 2010. In what might be considered a "worst-case" scenario, Japan's GDP declined 5.2 percent in the severe global recession of 2009.

It should be noted that although Japan's economy may not register a 5.2 percent decline this year, IC Insights believes that the supply chain disruptions resulting from the earthquake could still cause worldwide GDP to drop to 3.4 percent, and result in a \$260 billion shortfall in worldwide GDP this year as compared to original expectations of 3.9 percent growth.

A worldwide GDP growth rate of 3.4 percent would be 0.2 percentage points below the long-term average worldwide GDP growth rate of 3.6 percent. However, in IC Insights' opinion, this level of growth would still be sufficient to support its current 2011 semiconductor market growth forecast of at least 10 percent.

Effect on Electronic System Sales

Moving one step down from worldwide GDP, electronic system sales were \$1,237 billion in 2010, which represented only 2.2 percent of worldwide GDP. Taking into account the pessimistic situation of a 3.4 percent worldwide GDP growth rate in 2011 and the associated \$260 billion negative impact on worldwide GDP, and multiplying that by 2.2 percent yields an electronic system sales loss, as compared to IC Insights' original forecast of \$5.7 billion. Subtracting \$5.7

billion from IC Insights' current 2011 electronic system sales forecast of \$1,348 billion would put electronic system sales at about \$1,342 billion for the current year, an 8.5 percent increase over 2010 as compared to IC Insights' current forecast of 9.0 percent. This 8.5 percent increase would still be much better than the 6.0 percent long-term growth rate for electronic system sales.

IC Insights believes that any negative impact on electronic system sales from the current situation in Japan will only delay those sales, not destroy the demand for the systems. Thus, any shortfall in electronic system sales experienced in 2011 due to the Japan earthquake is likely to be gained back in 2012.

It is estimated that the Japanese market (i.e., consumption) represented approximately 9 percent of the world's electronic system sales in 2010, which equates to about \$111 billion. Thus, if the entire \$5.7 billion potential electronic system sales shortfall was due to a decline in demand from the Japanese market, the 2011 Japanese electronic systems market would decline about 5 percent to \$105 billion.

Not taking into account supply chain interruptions, the Japanese earthquake should not have much of an effect on the rest of the world's demand for electronic systems. It should be noted that it is likely that the psychology of the Japanese people will be to act in a conservative manner in the current environment, which of course will have a negative effect on electronic system demand from Japanese consumers. However, rebuilding electronic infrastructure in the hard hit areas of Japan is likely to partially offset some of the softness from the Japanese consumer portion of the electronic systems market.

Effect on Semiconductor Sales

Assuming a loss of \$5.7 billion in worldwide electronic system sales this year, and assuming that about 25 percent of electronic system sales are semiconductor content—a loss of about \$1.4 billion in worldwide semiconductor sales value would result. Using the “pessimistic” scenario (i.e., 3.4 percent worldwide GDP and a loss of \$5.7 billion in electronic system sales) and subtracting \$1.4 billion from IC Insights' current 2011 forecast of \$346.8 billion for the worldwide semiconductor market, puts the worldwide semiconductor market at \$345.4 billion, still a 10 percent increase over 2010.

Japan Electronics and Information Technology Industries Association (JEITA) stated that \$43.4 billion worth of semiconductors were produced in Japan last year. That amount represented about 14 percent of the 2010 worldwide semiconductor market of \$314.2 billion; 24 percent of the worldwide optoelectronics, sensors and discretes (O-S-D) market; and 12 percent of the worldwide IC market.

Thus, it appears that the world's electronic supply chain is twice as dependent on Japan-based production for O-S-D devices than it is for ICs.

Although it appears that major dynamic random access memory (DRAM) and Flash memory fabs were not significantly damaged by the earthquake and tsunami, Flash memory and DRAM spot prices jumped by 20 percent in the days immediately following the quake.

As evidenced by this example, supply does not necessarily need to be actually disrupted for prices to surge. Just the potential of a supply disruption can cause component buyers to step up their purchases for the “just-in-case” scenario. IC Insights expects that through the third quarter of 2011, many electronic system producers will attempt to acquire extra IC inventory, especially in anticipation of the seasonally strong second half of the year.

The semiconductor industry's supply chain is long and complex. Moreover, in many cases, removing one link (e.g., a specialty gas, molding compound, silicon wafers, a key module for a piece of semiconductor production equipment or raw material) will disjoint the supply chain and cause the whole process to come to a standstill.

It is believed that current inventory levels of wafers and packaging materials will help to avert serious shortages. Also, materials facilities (e.g., raw wafers and plastic resin) can often be brought back online much quicker than IC fabs, as evidenced many years ago when Sumitomo Chemical's plastic resin facility had a major fire. Although there were some short-term disruptions, serious long-term supply chain problems did not materialize.

IC Insights believes that other disruptions to the semiconductor supply chain are likely to emerge in 2011 that no one can anticipate today. However, major disruptions are not expected to last past the third quarter 2011.

Summary

In the final analysis, there is no doubt that supply will be constrained in numerous areas relating to the electronic system and semiconductor industries due to the earthquake and tsunami in Japan. However, on a worldwide basis, demand for electronic systems and semiconductors is expected to be only slightly lessened. Moreover, any lessening of system or semiconductor demand in 2011 due to the earthquake is forecasted to be delayed and pushed into 2012, but not destroyed.

Table 2 looks at the typical quarterly seasonal patterns for worldwide electronic system and semiconductor sales as well as the “post-earthquake” quarterly effects on Japan's GDP and worldwide semiconductor sales. With regard to worldwide electronic system and semiconductor sales, the effects of the earthquake would have been much more severe if it had occurred in the third quarter when the strong seasonal upturn usually begins.

Table 2. 2011 Post-earthquake Quarterly Outlook

1Q11	2Q11	3Q11	4Q11
Seasonal Electronic System Sales Pattern			
Moderate	Weak	Moderate	Strong
Seasonal Semiconductor Sales Pattern			
Weak	Moderate	Strong	Moderate
Earthquake Effect on Japan's GDP			
Slightly Negative	Strongly Negative	Moderately Negative	Moderately Positive
Earthquake Effect on Worldwide Semiconductor Sales			
Slightly Negative	Moderately Negative	Moderately Positive	Slightly Positive
1Q11	2Q11	3Q11	4Q11

Source: IC Insights

Because the earthquake happened so late in the first quarter 2011, the effect on Japan's first-quarter GDP was not too severe. As shown

CHALLENGES OF MONITORING HIGH-VOLTAGE BATTERY PACKS IN HYBRID AND ELECTRIC VEHICLES

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Worldwide concerns of climate change and oil supply have triggered great interest in the electric vehicle (EV) and hybrid EV (HEV) segment of the automotive market. This rapid growth segment is also stimulated by the development of rechargeable batteries. As these “green” vehicles are powered by high-voltage (HV) battery packs consisting of hundreds of series-connected cells, the complexity of such packs has dramatically grown. Thus, the safety, reliability and efficiency of these packs are inherently dependent upon a sophisticated battery management system (BMS).

A primary task of the BMS is to monitor the battery state-of-charge (SOC) by collecting run-time information of pack current, cell voltage and temperature. This creates challenges for intellectual property (IP)-focused fabless companies to provide high-performance, cost-effective and flexible analog front ends (AFEs) to be integrated into competitive battery monitoring-specific ICs to meet various automotive market needs.

This article presents a brief overview of the underlying issues of such monitoring ICs, explains the two dedicated data acquisition AFEs required for individual cell characteristic monitoring and pack current measurement, and introduces the need for application-level simulation to guarantee AFE performance at the system level.

HV Battery Pack Monitoring ICs

Among rechargeable battery types, a lithium-ion (Li-ion) battery is expected to dominate the market, thanks to advantages such as a higher energy density, lower self-discharge rate and flexible form factor. However, Li-ion batteries still face several challenges:

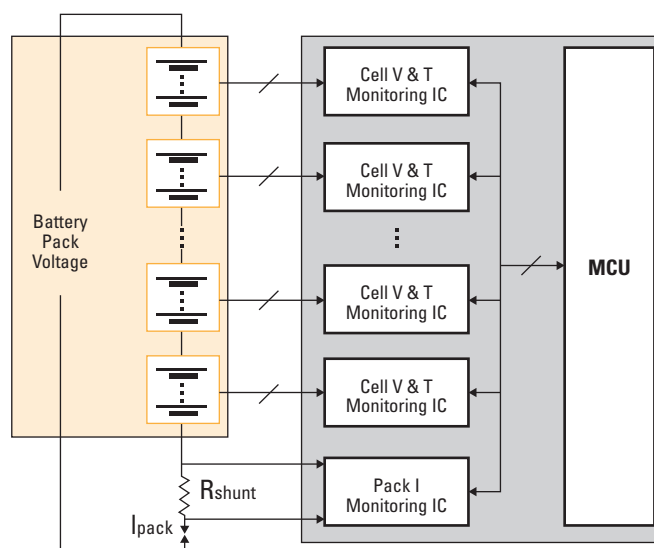
- A cell may catch fire or even explode if excessively over charged.
- A cell may be irreversibly damaged if excessively over discharged.
- Temperature-dependent charge and discharge behaviors.
- Flat discharge characteristic.

Moreover, the performance of the battery pack is limited by the weakest cell in the string. In other words, a fault in one cell may cause catastrophic consequence to the entire pack. This is why a Li-ion battery must be treated respectfully by using a sophisticated BMS to prolong its lifetime, maximize the automotive driving range and protect drivers from potential hazards due to battery failure.

Key functions of a BMS are battery state monitoring, protection, data computation and communication with other devices. Among these, the footstone is state monitoring as it provides primary data for a BMS to perform and manage other functions. Regarding modern Li-ion battery packs in EV and HEV, such data includes pack current,

individual cell voltage and temperature. By using an advanced algorithm, one can estimate the battery SOC and determine whether each cell is within its safe operating window.

Figure 1. Simplified Schematic of Battery Pack Monitoring



A typical approach for monitoring this data is illustrated in Figure 1. By dividing the long battery string into smaller groups, the voltage and temperature of each individual cell within any group are measured by sharing one dedicated monitoring IC. Such ICs typically incorporate a multiplexed AFE, and therefore can handle multiple cells which, in turn, reduces the cost and power consumption. On the other hand, the pack current is a single-point measurement as cells are connected in series. For current sensing, a shunt resistor or a hall-effect sensor can be placed somewhere in the string. The corresponding monitoring IC that incorporates high-precision AFE must have the capability of measuring small bidirectional charging/discharging current over time for accurate battery SOC estimation.

General requirements for data acquisition AFEs which make up these specific monitoring ICs are:

- Ability to measure multiple cells, typically from four to 12.
- Voltage and temperature measurements of each individual cell.
- Precise and fast measurements.
- High common mode voltage rejection.
- Low power consumption.
- Secure and fast communications with various devices.

The two types of AFEs used for measuring cell voltage/temperature and pack current are discussed in detail in the following sections. It is worth noting that a complete monitoring system is actually more complex than Figure 1 illustrates if other functional blocks are included (e.g., galvanic isolation, redundant monitor and self-diagnostic).

Multiplexed AFEs for Cell Voltage Measurement

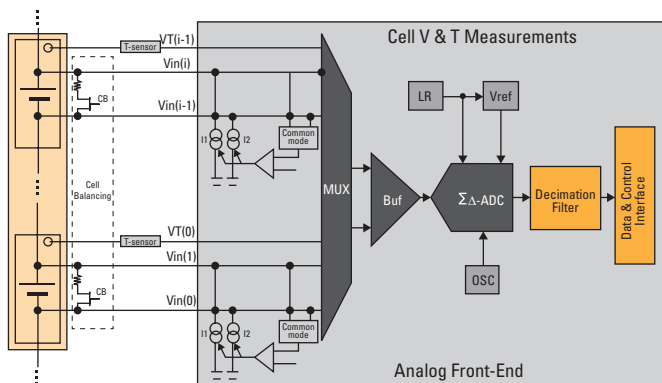
Cell voltage and temperature are essential characteristics which must be measured for correct SOC estimation and autonomy of the battery. Since modern Li-ion batteries have a flat discharge curve, a decrease of a few millivolts (mV) represents significant battery capacity variation. For example, the battery SOC changes about 1 percent for every decrease of 5 mV. To achieve system accuracy of 0.1 percent, taking into account all the sources of error, the analog-to-digital converter (ADC) should have at least 12 bits. Such ADCs have been used for years in multiple applications and can be found in catalogues of many IP suppliers. On the other hand, in HV battery monitoring ICs, the challenge is to provide an AFE containing multiplexed $\Sigma\Delta$ -ADCs that can handle a high common mode voltage while maintaining high accuracy, low power and low cost. The use of a $\Sigma\Delta$ -ADC architecture is due to its capability to easily reject the switching noise induced at 10 kilohertz (kHz) by the switching inverter, and its accuracy (as it has higher common mode rejection and can eliminate crosstalk). In contrast, to realize a Nyquist ADC with the same resolution to reject frequencies higher than 10 kHz, low-pass filters with settling times of a few milliseconds must be used, which consequently prevents the use of Nyquist ADCs in a multiplexed configuration.

Figure 2 presents the schematics of a multiplexed AFE that can digitize the voltages of multiple cells, allowing power and area savings in comparison to an ADC per cell approach as the number of required ADC channels is significantly reduced. The use of a $\Sigma\Delta$ -ADC in this multiplexed configuration has different requirements than conventional usage:

- Need of low-latency filters to achieve multiplexing frequencies of a few kHz.
- Drawback of using this filter is that the noise bandwidth to consider is higher.
- To remove the switching noise with a sufficient rejection, digital filters need to have higher orders.

Since the voltage change is imposed by the frequency of the motor inverter, the ADC must have a bandwidth of a few kHz.

Figure 2. Multiplexed AFE for Cell Voltage and Temperature Measurements



Dealing with High Common Mode Voltage

As previously discussed, a battery pack contains hundreds of series-connected cells. This leads to common mode voltage that can be higher than, for instance, 370 volts (V). However, to realize a very low-cost IC, a standard complimentary metal-oxide semiconductor (CMOS) process without HV options must be used. Because this process does not allow for voltages higher than 5V, it is mandatory to suppress the high common mode signals before the ADC inputs. Some techniques can be used to remove the common mode voltage:

- A straightforward solution uses a bridge divider to reduce this common mode voltage. As both the input signal and the common mode voltage are reduced, it requires a 20-bit ADC instead of a 13-bit ADC. Another drawback is that to satisfy the system requirements, resistors with an accuracy of 0.1 percent or lower must be used.
- Floating the chips at the cell's pack voltage, the drawback is that HV process is needed.
- The proposed solution, as shown in Figure 2, uses internally matched current sources combined to a differential amplifier, allowing for a cost reduction as a HV process is not needed. This is also easier to handle since the chip designer can set the differential gain and the common mode rejection independently.

Temperature-dependent Measurement Performance

In Li-ion batteries, autonomy and cell voltage depend on cell temperatures. Thus, temperature measurement is essential for realizing the real battery autonomy and also preventing battery damage from overheating. Between -20 C and 60 C, the cell voltage decrease is approximately 5 mV/C, which means that a measurement error of 1 C will result in an error of 1 percent of the SOC measurement. As a 12-bit ADC is sufficient to measure the temperature variation, the proposed configuration uses the same ADC for voltage and temperature measurement. However, as temperature change is slow, the temperature of the ADC does not need to be measured at the same frequency as the cell voltage. Furthermore, the accuracy of the required reference voltage is sensitive to temperature change. The reference voltage can affect measurement accuracy in two ways:

- Reference noise can increase the ADC output noise.
- As ADC gain is proportional to the reference voltage which is temperature-dependent, a reference with low temperature drift coefficient must be used.

To achieve 0.1 percent system performance, it is necessary to embed a reference voltage with an absolute accuracy below 0.05 percent and a temperature drift coefficient of few parts per million (ppm)/C. These characteristics can be achieved only with a reference voltage calibration.

AFE for Battery Pack Current Measurement

Current must be measured because cell capacity is dependent on the discharge rate. Correlating with the battery cell voltage gives the cell internal resistance which allows for an increase in the SOC accuracy. As all cells are series-connected, it is sufficient to measure the current of the entire battery pack. Figure 3 shows the scheme for measuring pack current. The current sensor is typically a shunt resistor that converts the current into a differential voltage. The resistance of the shunt resistor stays low to minimize power loss ($P=RI^2$). The AFE input stage must have the ability to amplify a weak signal delivered by the shunt resistor. This signal is fed back into a high-resolution

POWER: A BUSINESS PROBLEM

PAUL VAN BESOUW, PRESIDENT AND CEO, OASYS DESIGN SYSTEMS

Power has become the major challenge in delivering electronic systems that meet the business objectives of the end user and the semiconductor components company. It is now almost a cliché to say “power is the new timing.”

In portable devices such as wireless phones and tablet computers, power is clearly important. Power translates directly into parameters such as standby time and talk time that consumers use in making product choices. However, power is also important in tethered applications, including servers and routers. Increasingly, the capacity of a datacenter is no longer limited by the physical size of the equipment, but rather by the ability to bring power into the building and transfer heat out. Even in less aggressive tethered systems such as set-top boxes (STBs), power is a primary driver of acceptability. STBs sit in people’s living rooms and, typically, should not have noisy fans. Furthermore, they must continue to work if the cat decides that the top of the warm digital video recorder (DVR) is the perfect place for a nap.

More subtly, the power budget is the primary limitation on performance. This is most obvious in the chips from companies such as Intel, NVIDIA and Advanced Micro Devices (AMD) that are placed into all types of personal computers (PCs) (i.e., servers, notebooks, etc). For several years now, it has not been possible to increase the raw performance of individual cores due to power reasons, and the number of cores on a chip is often limited as much by power considerations as area.

The current champion on the power front for individual chips seems to be IBM’s experimental 3D chips with server processors, memories and an interposer to connect it all, distribute power and decouple noise. It is all in the same package under a huge heat sink. These dissipate 1–200 watts (w). With a 1 volt (v) power supply, this means supplying 100–200 amps. To put that into perspective, that is the typical current used for arc welding, although at a higher voltage.

This power ceiling constraint has led to more and more chips delivering computing power not in the form of a single high-performance processor, but in multiple cores. The cores may be heterogeneous, with different types of cores and functionality statically partitioned among them. This has been the case with cellphones since signal processing logic was replaced with digital signal processors (DSPs). The alternative is the multi-core symmetrical multi-processing (SMP) architecture. Here, multiple identical cores can be dynamically scheduled depending on the workload. However, the difficulty of programming multi-core designs has been completely underestimated by processor manufacturers. In the market for servers (primarily those delivering Website content), the different parallel users can be spread among the cores and do not require any subtle analysis. But in single-user systems such as PCs or smartphones, Amdahl’s law comes into effect. When designing parallel computers in the late 1970s, Gene Amdahl observed that performance was not limited by what could be made parallel, but by what could not. If,

for example, 10 percent of a workload could not be parallelized, then the maximum speedup would be asymptotically limited to 10 times if the parallelized part of the workload ran infinitely fast; and with practical speedups, this would be significantly less.

Right now this is not an enormous problem since multi-core designs typically contain only two or four cores, so there is a lot of scope for finding concurrent functionality. But a corollary of Moore’s law is that the number of cores on a chip is increasing exponentially too. It is not obvious yet since the number of cores is on the flat part of the curve. For a general-purpose program, how to make use of large numbers of cores remains an open question; and the biggest worry is that this is a question without a solution.

One area where the number of cores has left the flat part of the curve is the design of graphics processors. These address a so-called “embarrassingly parallel” application where there is almost arbitrary amounts of workload that can be run concurrently since there is very little interaction between different parts of the workload. Even here, power is one of the big constraints on the amount of graphic processing that can be delivered. Further, the inability of the main processor to deliver enough data at a fast rate due to power limitations means that graphics processors cannot always maintain a full load. Although there are some other issues such as designing low-power motors for fans and disk drives, most of these big picture constraints come down to one—designing low-power ICs for the semiconductor content of these systems.

In the past, process and chip designers had a big weapon for reducing power: Reduce the power supply voltage at each process node. Since the voltage is squared in the power equations, a small change in voltage can have an outsize effect in reducing power. For various technical reasons associated with leakage current and noise immunity, it is no longer possible to reduce the power supply voltage at each process node to compensate for higher clock frequencies and higher component counts.

The tools and design approaches for reducing power are somewhat limited. Power is a chip-level issue. Obviously, there is a sense in which the power dissipated is the sum of the power of all the blocks (or even all the gates and interconnect), but this is not very useful since it is difficult to guess what the power limit for an individual block should be. There are a number of proven approaches to reducing power, most of which have some level of support in current design flows:

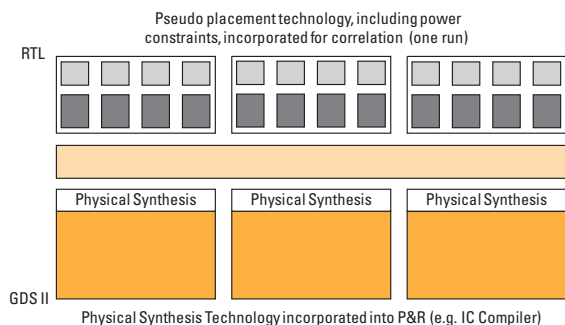
- **Multi-voltage threshold libraries:** Since leakage current is an increasing part of the power problem, it is good practice to use high-threshold, low-leakage, low-performance cells on non-critical nets and keep the low-threshold, high-leakage, high-performance cells for the timing-critical parts of the design. The synthesis tool can make the selection dynamically, based on the criticality of the nets.
- **Voltage domains:** Some parts of the design are much more

critical for power or timing than others, so the design can be separated into separate voltage domains with different performance/power tradeoffs. The Common Power Format (CPF) from Si2 and Accellera's Universal Power Format (UPF) standards are a way to capture this policy. Power-aware synthesis can read these files, automatically infer the required level shifters between voltage domains, and take account of the impact on timing and power.

- **Voltage areas:** Though voltage areas can be powered down, this is something above the level of the system-on-chip (SoC)—typically controlled by a high level of the control software (Is a phone call in progress?). Synthesis tools cannot automatically decide to power down an area, but they can take into account the timing due to isolation cells described in the CPF or UPF.
- **Clock gating:** In the distant past, the golden rule was never to gate a clock. Instead, a register containing an unchanging value was looped back to its input through a multiplexor. Today, in the low-power era, that structure is best replaced by the synthesis tool with a gated clock, especially if the register is large (since the clock can be gated for the entire register rather than for each flop in the register).

The challenge with traditional synthesis tools is that there is really no good way to partition the power budget among the large number of blocks on a chip that traditional methodologies create for a chip in a leading-edge process node such as 45 nanometer or 28 nanometer. Even if a reasonable division of the power budget among the various parts of the design is found, iterating the design to analyze different “what-if” scenarios is too slow.

Figure 1. Physical Synthesis



Traditional design flows cannot handle power constraints efficiently.

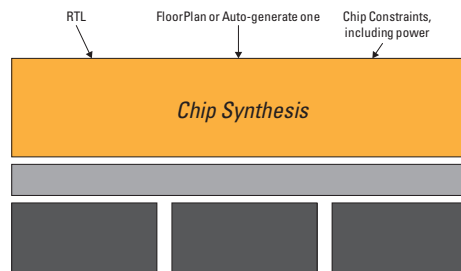
For example, imagine a block in its voltage island. Lowering the voltage to that island has the potential to save a lot of power. But it is not feasible to only lower the voltage and re-run timing analysis. If the synthesis tool has done a passable job, the block will just make timing (otherwise slower, lower power cells could have been chosen), thus the whole block must be re-synthesized at the lower voltage.

Worse than that, the time budgeting should also be updated and the surrounding blocks re-synthesized. Further, since timing is totally dependent on placement, especially at the most advanced nodes, the whole placement of the design needs to be redone to ensure confidence in the analysis. For a typical design using traditional block-based approaches, analysis for a single case can take days or even weeks.

Since power is a chip-level problem, it needs to be addressed at the chip level. Chip synthesis operates at either the level of the entire chip or over a handful of largely independent large blocks (microprocessors, memory subsystems, etc). Experimenting with the

voltage of a particular block (voltage island) requires resynthesizing the whole chip from the register transfer level (RTL) and generating an updated placement. The ramifications of the voltage change propagate throughout the chip in an optimal manner. If the analysis of the change looks good, then updated CPF or UPF needs to be created either as input to the chip synthesis tool or, if the voltage change was made interactively inside the tool, written back out.

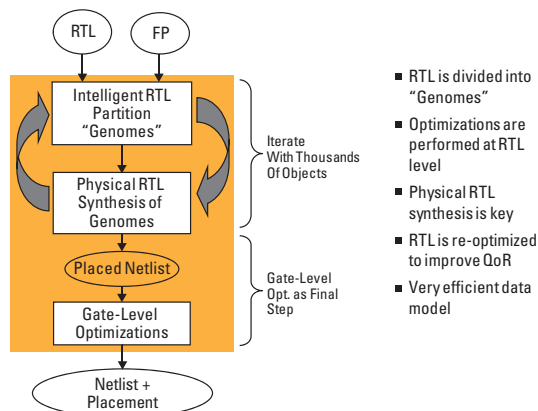
Figure 2. Chip Level



Since power is a chip-level problem, it needs to be addressed at the chip level with chip synthesis.

One challenge in modern IC design is that chip-level issues need to be handled at the chip level. Increasingly, approaches that divide the design into large numbers of blocks to be handled independently are not efficient because it is not possible to have good budgets for timing, power, area, congestion and so on between the various blocks. While each block may be implemented efficiently on its own, the reassembly of these blocks to form the whole chip is far from optimal. Additionally, power is the new timing in electronic systems and has become a business problem.

Figure 3. Chip Synthesis



Chip synthesis is faster and more efficient.

When dealing with chip-level problems such as power at the chip level, using chip synthesis is the way to escape from this increasingly ineffective method of design. ■

About the Author

Paul van Besouw is president, chief executive officer and co-founder of Oasys. Mr. van Besouw has an extensive technical and management background in the electronics industry. Prior to Oasys, van Besouw was responsible for managing the synthesis and physical synthesis teams at Cadence. Prior to Cadence, he was one of the first members of the Ambit Design Systems engineering team, where he led the development of the RTL and datapath synthesis technology. He holds a Master of Science in electrical and computer engineering from the Eindhoven University of Technology in the Netherlands.

ON-CHIP ESD PROTECTION FOR WIRELESS INTERFACES IN CMOS ICs

BART KEPPENS, DIRECTOR, TECHNICAL MARKETING, SOFICS BVBA

The number of wireless-enabled systems is very diverse and steadily growing. System makers include wireless functions in mature applications such as fixed-line telephones and TVs, increase the wireless features in mobile phones with the support of multiple standards, and come up with new device types that thrive on constant wireless connectivity for the newest content¹. Further, the transport, security, medical and payment sectors are quickly switching to wireless interfaces for improved user experience. Intelligent wireless bus, subway and train tickets replace paper versions. Expensive equipment or resources, in general, are traced by radio frequency identification (RFID) tags. Sensor body networks reduce the cost of medical care while increasing reaction speed as needed. Near field communication (NFC) bank cards replace the smartcard and magnetic strips used today.

Wireless communication comes in many forms, each designed or optimized for a specific task and application, and sometimes constrained by differences in local legislation². Moreover, existing standards are typically upgraded a few years down the road to enable higher data rates or to extend the range³. Wireless standards can be grouped or compared based on different parameters such as center frequency, primary use, encoding protocol, degree of mobility or range. An overview of industry standards and proprietary formats can be found online⁴.

Requirements for On-chip ESD Protection

Despite the improved electrostatic discharge (ESD) awareness and control in assembly factories and the related push for a reduction of component-level ESD performance^{5,6}, ICs still need adequate ESD protection. In many cases, traditional ESD protection devices used for low-speed digital interfaces are not suited for RF interfaces for a number of reasons:

- Capacitive loading shunts a large part of the RF signal to supply (Vdd/Vss) lines through high parasitic junction and metal capacitance of ESD clamps.
- Excessive noise is injected at the receiver due to series resistance used between primary and secondary ESD clamps.
- Direct current (DC) leakage degrades the quality factor (Q-factor) and influences the size of the bias circuits.

Furthermore, to reduce the cost of consumer electronics devices,

designers try to combine different standards into a single silicon chip³, adding another constraint for the ESD protection approaches: The clamp parasitic influence should be as stable as possible across a large frequency band and voltage range.

Various Protection Approaches

IC designers use a variety of ESD protection approaches to protect ICs against ESD stress. The well-known dual diode-based ESD protection (Figure 1, left, pad type A) has been used by many designers for the protection of analog circuits, thanks to the small area, straightforward implementation, low leakage and low capacitive loading.

Recently, however, various researchers have predicted the end of dual diode-based ESD design for RF circuits in advanced complementary metal-oxide semiconductor (CMOS) (65 nanometer and beyond) due to the increasing sensitivity of RF circuits⁸⁻¹³. They reason that to ensure effective protection, the diodes connected to the input/outputs (I/Os) must be designed with a larger perimeter to reduce the voltage drop ($R_{on} \times I_{ESD}$) which, in turn, leads to higher leakage and higher capacitive loading—worsening the RF performance of the connected circuits.

Fortunately, there are alternatives to protect RF circuits against ESD stress. This section briefly outlines different protection approaches^{11,14} and provides relevant references:

- **Plug-n-play, minimal parasitic capacitive loading:** The parasitic capacitance of the ESD devices at the I/O pad is minimized such that the degradation of the RF performance is limited without a need to adapt the actual functional RF circuits. Researchers have compared different device types for this purpose¹⁵⁻¹⁷. Besides the active ESD devices, people have used low-frequency filters for high-frequency applications (>5 GHz)¹⁸⁻²¹ in a plug-n-play approach.
- **Inductor-capacitor circuit (LC) cancellation techniques:** In various publications, designers compensated the parasitic effects of ESD devices by adding tuned LC elements^{10,13,22}.
- **Co-design:** Through the use of co-design, traditional ESD solutions with high capacitive loading can still be used because the negative effects are compensated for in the matching circuits^{23,24}.

Many researchers⁸⁻²⁴ claim that the “plug-n-play” ESD protection concept using active devices such as diodes, MOS or silicon-controlled rectifiers (SCRs) is only feasible below 5 GHz. The following sections provide case studies to prove that it can be taken much further based on proprietary, low-capacitive SCR protection concepts (Figure 1, left, pad type B or C) or novel local I/O clamps to replace dual diode cells.

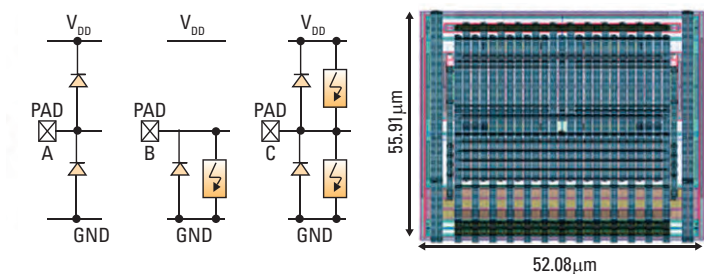
Case Study 1: 90 Nanometer RFID

A SCR-based protection clamp is validated for an 8.5 GHz low-noise amplifier (LNA) designed in TSMC 90 nanometer low power (LP). The ESD protection is designed to protect the ultra-wideband RF circuits based on the IEEE 802.15.4a standard,⁷ which is an alternate physical layer (PHY) and adds location awareness, low power and higher data rates to the PHY and MAC specification for ZigBee devices. The circuit can be used for accurate real-time indoor location of resources/assets and in wireless sensors for health, retail, manufacturing and security sectors. One of the key requirements is the low-leakage core and I/O circuits: The chip operates off a single watch battery for up to 10 years.

The proprietary circuit to be protected consists of 3.3V transistors with a transient failure voltage of 11.4V, enabling various ESD protection concepts. To leave room for a large analog circuit including coils on the top metal, the I/O ring is designed such that there is only a low-resistive Vss bus available at the RF interfaces, which means that a dual diode protection approach is not feasible. Clamp type B is used instead (Figure 1). To enable the high-frequency signals, the parasitic junction capacitance of ESD clamps must be below 100 fF. Furthermore, the clamp leakage at room temperature must be below 1 nA.

The selected protection design consists of an SCR clamp triggered by a MOS device^{25,26} with dynamic gate bias. The design includes the SCR clamp, NMOS trigger, RC ESD detection filter, reverse diode and all required guard bands within an area of 55.91 micron by 52.08 micron. Thanks to this small area, the ESD cell could be located under the bond pad (circuit under pad or CUP), leaving room for the large area inductors of the RF circuit.

Figure 1. ESD Protection Approaches and Example Protection for 90 Nanometer RFIO



On-chip ESD I/O protection concepts: dual diode (pad type A) or local clamp protection (pad types B, C). Layout plot (right) for the I/O ESD clamp (type B) with a total capacitance of 98.62 fF. The ESD clamp (SCR, trigger, RC ESD detection filter, reverse diode and all required guard bands) fits within an area of less than 3000 micron² and is placed under the bond pad.

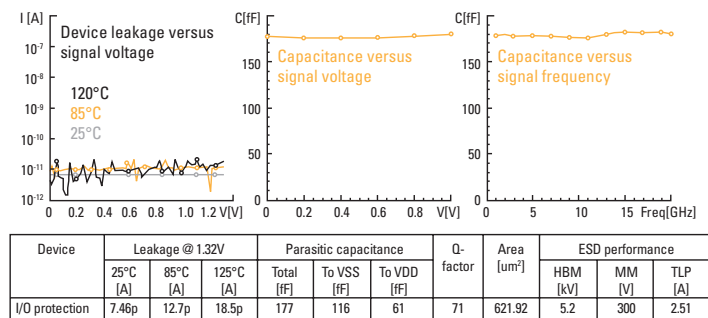
The ESD design guarantees effective ESD protection up to 2 kV Human Body Model (HBM), well above the standard requirement

used for RF interfaces in advanced CMOS technology. This means that the chip can be handled in low-cost assembly houses, reducing the cost of the system. Thanks to the capacitive loading of 98.62 fF and leakage below 0.1 nA (at 25 C), 55 nA (at 125 C), the clamp does not influence the RF behavior, thus the design of the RF circuit is greatly simplified.

Case Study 2: 40 Nanometer Bluetooth

For a Bluetooth interface chip in TSMC 40 nanometer CMOS, an ESD protection clamp is developed with a parasitic capacitance below 180 fF and at least 2 kV HBM performance. Different SCR-based protection concepts are compared for ESD-relevant parameters using transmission line pulse (TLP), HBM and machine model (MM). The leakage current from I/O to Vss is analyzed at different temperatures. The selected device has a leakage current of less than 20 pA (Figure 1, left). Finally, the different clamps were measured with RF S-parameter equipment. After de-embedding based on “open” and “short” structures, the device parasitic capacitance (junction and metal combined) is determined as a function of I/O bias voltage (between 0 and 1V) and frequency (between 1 and 20 GHz). Both plots (Figure 2, middle and right) show that the capacitance level variation is less than 6 percent for the selected device.

Figure 2. Low-leakage and Low-capacitance SCR-based I/O Protection in TSMC 40 Nanometer LP



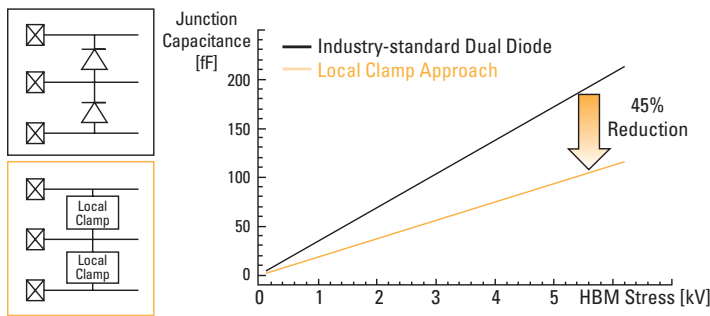
Summary of the key parameters of the SCR-based protection approach in TSMC 40 nanometer technology. The ESD protection clamp leakage (left) is very low even at a high temperature. The capacitance stays below 200 fF and is very stable across signal voltage and signal frequency (up to 20 GHz). The capacitance level can be easily reduced further (below 100 fF for 2 kV HBM).

Case Study 3: 65 Nanometer RFIO

The dual diode (pad type A in Figure 1) is one of the most used ESD protection concepts for RF interfaces because of its many benefits:

- It occupies a very small silicon area.
- The connections are simple.
- IC designers believe that the concept has the lowest parasitic capacitance for a given ESD performance.

However, that is about to change with a novel local clamp approach that has the potential to reduce the parasitic capacitance by half. This can enable circuits with much higher frequencies. A comparison between the industry-standard dual diode approach and the local clamp concept is given in Figure 2 based on silicon analysis in GLOBALFOUNDRIES’ 65 nanometer process.

Figure 3. Local Clamp Approach to Replace Dual Diode

Novel approach with two local I/O protection clamps to replace the dual diode approach in use by the industry. The novel clamp can reduce the capacitance loading at the I/O signal pad by more than 45 percent.

Conclusion

This article provided evidence that the “plug-n-play” approach based on active ESD devices can be used for interfaces operating well above 5 GHz.

This publication provided information about SCR-based ESD protection clamps for RF circuits validated in 90 nanometer and 40 nanometer CMOS technologies. The ESD protection clamps described have excellent figures of merit. Due to the low parasitic capacitance, low leakage and high Q-factor, the influence on the RF performance is limited. RF designers can rely on these SCR device types without the need for extensive co-design optimizations between RF (matching) circuitry and ESD protection devices.

A new local clamp approach is introduced that reduces the parasitic capacitance of the industry-standard dual diode protection concept by almost 50 percent, enabling much higher frequencies.

While this article focused on Bluetooth, global positioning system (GPS) and the IEEE 802.15.4a standard used for real-time location systems (RTLS), the ESD device concepts can be used more broadly for both high-frequency RFIOs as well as high-speed differential digital interfaces such as High-Definition Multimedia Interface (HDMI), Universal Serial Bus (USB) 3.0, Peripheral Component Interconnect Express (PCIe) and fast Ethernet. ■

About the Author

Bart Keppens received his engineering degree in electronics from the Technical University Groep T, Leuven in 1996. That same year, Mr. Keppens joined IMEC and was responsible for device electrical characterization and support for the ESD group and layout and testing for the non-volatile memory (NVM) group. From May 2002, he joined Sarnoff Europe, Belgium, solving ESD-related problems for customers worldwide, first as an ESD engineer and later as a technical leader and ESD design specialist. From 2006, Mr. Keppens supported business development initiatives as technical director for ESD. After a management buyout in June 2009, Sarnoff Europe became SOFICS – Solutions for ICs, where Mr. Keppens is now director of technical marketing, working with semiconductor companies worldwide. Bart has co-authored 25 peer-reviewed published articles in the field of on-chip ESD protection and testing. Invited papers on ESD solutions and TLP analysis techniques were delivered at the RCJ ESD symposium in Japan in 2006, 2007, 2008, 2009 and 2010.

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Table 1. Corner Lot Definition

BiCMOS/SiGe-BiCMOS								
Condition	NMOS Transistor		PMOS Transistor		Bipolar Transistor BETA	HR Poly and/or Poly 2 SHEET RESISTANCE	Capacitor VALUE	Number of Wafers
	LEFF	VT	LEFF	VT				
Typical Mean	typ	typ	typ	typ	typ	typ	typ	3
Worst Case Speed	>	>	>	>	<	>	>	3
Worst Case Power	<	<	<	<	>	<	<	3
Worst Case One	typ	<	typ	>	typ	typ	typ	3
Worst Case Zero	typ	>	typ	<	typ	typ	typ	3

Source: austriamicrosystems

During the design FMEA (DFMEA), design-specific corners can be defined. For special devices such as micro-electrical-mechanical systems (MEMS) sensors, the corner definition can also include geometrical parameters. Such special parameters could be layer thicknesses or spacing between critical elements in MEMS structures.

Another effective measure for a safe product launch is the introduction of burn-in during the product ramp-up phase; parts will be tested before and after a dynamic burn-in procedure at high temperature for a certain period of time. The purpose of this burn-in is to eliminate early fails, attributable, for instance, to thin oxide breakdowns which can occur when isolation layers are contaminated

by particles. In addition to burn-in, the mandatory 100 percent test at three temperatures can be specified during the product ramp-up phase.

In some cases, especially if an integrated device manufacturer (IDM) provides a foundry service, an extended foundry model can be offered to support automotive product qualification. Under such a business model, the foundry acts as a consultant for product qualification, and performs qualification tests according to the end customer's specification.

Summary

The author describes an advanced automotive foundry flow which enables fabless IC vendors or pure design houses to collaborate with the automotive industry. Furthermore, he recommends an extended foundry flow for full backend automotive production. The article is divided into five chapters. Chapter one describes the difference between automotive, industrial and consumer wafer fabrication. Chapter two gives an overview of special measures required during wafer probe test. Chapter three describes the special requirements for packaging. Chapter four highlights special procedures for the final testing of packaged parts. And in the last chapter, the author recommends a safe product launch concept. ■

About the Author

Peter Pann received his master's degree in communications engineering in 1983 from the HTL Braunau am Inn, Austria and received his master's degree in electronics and communications technology in 1989 from the Graz University of Technology, Austria. He has held several positions in customer engineering, product engineering, ESD development and engineering laboratory management as well as operations at austriamicrosystems. Mr. Pann is currently section manager of foundry engineering within the Full Service Foundry strategic business unit of austriamicrosystems. He can be reached at +43-0-3136-500-5335 or peter.pann@austriamicrosystems.com.

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MOS-AK/GSA Modeling Workshop

September 16, 2011 ■ Helsinki, Finland

GSA Semiconductor Ecosystem Summit

October 6, 2011 ■ Santa Clara, CA

Silicon Series Luncheon

October 20, 2011 ■ Boston, MA

GSA Semiconductor Leaders Forum Taiwan

October 26, 2011 ■ Taipei, Taiwan

Silicon Series Luncheon

October 27, 2011 ■ Austin, TX

MOS-AK/GSA Modeling Workshop

December 2011 ■ Washington, D.C.

Awards Dinner Celebration

December 8, 2011 ■ Santa Clara, CA

analysis requirements. Driven by the performance requirements of wireless connectivity (RF), fast processing speed (clocking), low-power requirements and interfaces with the analog world (sensors), designers are facing tremendous challenges in analog/RF design and verification, having to cope with lower supply voltages, greater interference and nanometer physical effects limiting the electrical performance of these circuits. As a result, design margins for mixed-signal circuits are higher and parametric yield is a challenge.

The Circuits: Platform Design Bottlenecks

The circuits that require particular attention in this new paradigm of nanometer platforms include data conversion, radio transceivers, clock generation, high-speed input/output (I/O), power management, memory and sensors. Designers face a wide variety of challenges in verifying data conversion functionality against performance specifications. In nanometer geometries, new physical effects need to be taken into account because they now have a significant impact on electrical behavior. The inherent random noise of semiconductor devices limits the achievable performance of converters, thereby requiring new types of analysis to quantify the behavior of these circuits.

The challenges in clock generation and high-speed I/O are dominated by the requirements of the phase-locked loop (PLL) or clock and data recovery (CDR) circuitry. Key requirements include low phase noise or clock signal jitter, fast locking, minimum area and low power. At nanometer process nodes, random device noise and parasitics have a significant impact on PLL phase noise and jitter behavior, making it extremely challenging for designers to meet performance specifications with tight constraints.

Image sensors require high-performance and high-accuracy data converters as well as signal drivers that require accurate noise predictions to assure performance specifications are met. In addition, it is desirable to verify all of the converters at the same time (full-circuit verification), which requires high-performance and high-capacity circuit simulators.

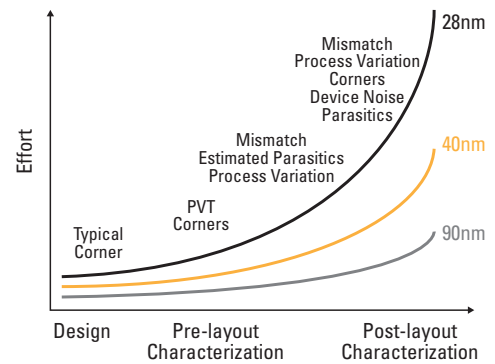
Radio transceivers are evolving rapidly with advanced techniques in communication theory, requiring dramatically more complex transceiver circuitry. Radio architectures rapidly evolving as powerful techniques that increase the capacity of wireless channels are adopted for many applications such as multiple-input multiple-output (MIMO) for cellular Wi-Fi and wireless HD. For example, 4G standards treble the required number of frequency bands to be supported in a platform, thereby putting tremendous pressure on frequency synthesizer design complexity.

The Impact of Characterization Requirements

Further verification challenges for all analog/RF circuits come from the impact of the physical process effects that are present in nanometer CMOS. While they may be second- and third-order effects in older geometries, they come to the fore in the nanometer era.

The impact of device noise, layout parasitics, process variation and device mismatch makes it paramount to have a thorough characterization process. The verification tools used in characterization must have the accuracy, capacity and performance to predict the impact of these nanometer physical effects, and the tools must apply statistical methods to ensure that manufacturing yield meets price point requirements. Figure 4 shows the impact of these nanometer effects in analog/RF characterization.

Figure 4. Nanometer Analog/RF/Mixed-signal Characterization Requirements



Addressing Platform Design Bottlenecks: Analog/RF Retooling

The complexity and nanometer-effect sensitivity of analog/RF designs requires the verification flow to support transistor-level simulation with nanometer Simulation Program with Integrated Circuit Emphasis (SPICE) accuracy, much higher performance, much higher capacity and a completely new functionality (required to address critical nanometer CMOS verification challenges such as post-layout, device noise and variation analyses). In many cases, this means that designers may need to retool their platforms and adjust their design methodology.

In previous technologies, designers relied on simplified block-level verification approaches and used estimates for full-circuit performance, with the estimates often based on models using linear approximations. In nanometer CMOS, analog/RF designers must verify their full circuit at the transistor level with nanometer SPICE accuracy in the presence of nonlinear effects. This verification must include the impact of random device noise as well as architectural characteristics such as quantization noise. In addition, verification tools need to include post-layout parasitics and support automated post processing to calculate the key performance metrics. Verification alone is not sufficient. Design teams require a toolset that supports intensive full-circuit characterization that includes process/voltage/temperature (PVT) corners, parameter sweeps and Monte Carlo statistical analysis—all the while accounting for device noise, device mismatch and detailed parasitics, which adds complexity to the process and requires much greater capacity.

Companies are finally responding to these emerging requirements by delivering breakthrough design technologies to address new types of specialized analyses together with the required accuracy, performance and capacity for the design and verification of nanometer mixed-signal circuits for new platform-based products being developed for emerging markets.

Summary

Emerging semiconductor technology, mixed-signal innovations and growing demand in emerging markets create a “perfect storm” of semiconductor change and growth. The electronics industry is driven by explosive growth in the new middle class. Nearly a half-billion people will join the middle class in developing countries between 2010 and 2015, creating the bulk of new demand for electronic products. These markets require new electronics platforms for delivering complex products at the required price points. These platforms are enabled by new semiconductor technology and mixed-

signal designs that deliver breakthrough advances in connectivity, application processors, solid-state storage, sensors and power management. This shift to platform design requires innovation and retooling in the mixed-signal design flow, so electronic product manufacturers can address the tremendous and exciting opportunity wrought by this new demand in emerging markets. ■

About the Author

Ravi Subramanian, president and CEO of Berkeley Design Automation Inc., earned his B.S.E.E. (honors) from the California Institute of Technology and a Ph.D. in EECS from the University of California at Berkeley. Since entering the wireless communications and semiconductor industry at AT&T Bell Laboratories 17 years ago, Ravi's experience has spanned research, product development, marketing, sales and general management roles. He is the lead author on 16 issued United States patents on digital radio architectures and signal processing techniques in mobile communications. In 2010, Ravi was elected to the EDA

Consortium's (EDAC) board of directors.

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High-density MRAM continued from page 22

to about 16 megabit, rely on a KV/kT on the order of 60 for successful chip products. Next-generation MRAM technologies intended for manufacture with 65 nanometer lithography and finer are targeting densities that start at 64 Mbit with a roadmap up to gigabit densities and beyond, requiring KV/kT in excess of 70 (Figure 3).

Achieving High-stability MRAM

The challenge for next-generation MRAM technologies is keeping this stability factor high enough to produce reliable memory while sustaining a writing mechanism that allows for a minimum lithographical size. The problem links back to the previously described energy barrier. The barrier is kept high to maintain stability, but increased barrier height impedes production of a very small memory cell due to the high energy required for writing (i.e., larger currents and voltages are required, thus necessitating larger transistors and other structures in the memory cell).

Thermal-assisted switching (TAS) is an important breakthrough for solving this tension. In TAS, the essential concept is that the KV/kT can be set at different values when "holding" data and when "writing" data. As a result, a very high KV/kT (typically >150) can be engineered for holding data, and a much lower KV/kT (typically <40) applies for writing data. As a result, the maintenance of high data stability ceases to be a constraint in reducing the size of the bit cell, opening a path to 45 nanometer lithography and enabling gigabit memory densities.

To make TAS work, the holding KV/kT applies when the MTJ is at normal operating temperature. During writing, the MTJ is heated in several nanoseconds to about 220 C—the temperature at which the material characteristics of the MTJ change and the KV/kT falls to a much lower level, thereby facilitating a very low-energy write operation. This low-energy write operation, coupled with high stability during the hold, provides for use of a lithographically minimum data bit cell with extremely high stability. As shown in Figure 3, TAS technology enables stability factors that can produce memory chip densities in excess of 10 GB. TAS technology has been proven at the 130 nanometer process node and will enter production in 2011.

Across the industry, there are two writing mechanisms under

development for advanced MRAM technologies, one using locally generated magnetic fields and the other using electron spin polarization (often referred to as spin transfer or spin torque). The TAS concept for stabilization can be used with either of these writing mechanisms, and in both cases resolves the stability barrier looming on the path to very high-density MRAM. Without TAS, each step forward in MRAM density will require innovation in MTJ device structure and writing mechanism to provide acceptable stability and a small bit area. It is not proven that production-worthy commercial MRAM of 64 Mbit and larger densities can be achieved without an advanced stabilization mechanism such as TAS.

Summary

The road to high-density MRAM requires a strong solution for the problem of maintaining data stability while reducing feature size. Most MRAM device approaches are constrained by the challenge of materials and device physics that cannot simultaneously provide stability and a reduced feature size. TAS is a new MRAM technology that decouples the limiting interaction between stability and scaling, thereby opening the door to very high-density MRAM technology that scales reliably to 45 nanometer, 32 nanometer and smaller. ■

About the Authors

Barry Hoberman is the chief marketing officer at Crocus Technology. Mr. Hoberman possesses 30 years of experience within the semiconductor industry. Previously, he was the founder and chief executive officer of inSilicon, a leading semiconductor intellectual property (IP) supplier serving the communications and connectivity markets, which was acquired by Synopsys in 2002. His industry leadership experience also includes CEO positions with Virtual Silicon and TZero Technologies. In addition, Mr. Hoberman has held various product management and development positions at Monolithic Memories and Advanced Micro Devices (AMD). Mr. Hoberman earned Bachelor of Science degrees in electrical engineering and biology from the Massachusetts Institute of Technology and holds 14 U.S. patents.

Ken Mackay is director of magnetic cell engineering for Crocus Technology. With over 20 years combined semiconductor and magnetics experience, including past positions at IBM and Hitachi, Mr. Mackay is responsible for magnetic technology and core memory cell integration at Crocus Technology.

Solutions

The first step towards ensuring the success of these complex electronic systems is to adopt a simulation- and analysis-driven product design strategy, especially for the IC, package and PCB PDN. The old “correct-by-construction” and “over-design” approaches, while admirable in intent, often fall short—especially for these advanced circuits. For example, as the number of unique power/ground supply networks in an IC reaches 50 or more, it is not possible to over-design every, or for that matter, any one network. Additionally, over-designing one part of the overall system does not benefit the system’s performance if the other parts are not optimized. However, creating and using a simulation- and analysis- driven product design cycle helps increase the chances of “getting it right” the first time and enabling better decision making for tradeoffs, cost optimization and failure prevention.

Dr. Mondira (Mandy) Pant, a lead technologist and power delivery architect for next-generation Xeon and Itanium server products at Intel Corporation notes, “Accurate pre-silicon power delivery simulations are an essential tool to predict the impacts of tester and system power delivery performance on silicon frequency and reliability.” Similar sentiments were seen in a survey conducted by the Aberdeen group¹², which noted that “best-in-class” design teams are three times more likely to adopt and use a simulation- and analysis-based design approach. These “best-in-class” performers are more likely to start analyzing a design from its prototype phase through the design cycle to predict its behavior and to validate their design approach¹².

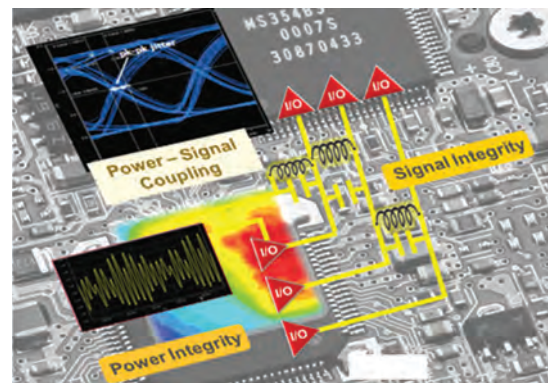
The second step is to consider the design of the electronic system holistically. The IC, package and PCB together affect the cost of the system and determine the electrical, thermal and electromagnetic interference (EMI) signature of the final electronic system. Given the performance, size and cost constraints, packages and boards used in today’s mobile systems can no longer be “off-the-shelf” or based on “design re-use.” They must be designed together with the ICs, taking into consideration the various electrical characteristics of the IC including its power profile, its I/O interface design and its thermal signature. This co-design approach helps IC designers to model the impact of the package and PCB on the performance and reliability of their designs. This approach helps handset designers to verify their board’s PDN and signal routing along with other component specifications. This not only helps accelerate the design cycle, preventing multiple iterations of the design, but also helps in reducing the overall system cost by optimizing the system in a holistic manner.

However, this methodology requires information sharing and collaboration between the various teams from the start of the design process. IC vendors must provide appropriate power and I/O models, enabling an IC-aware system-level validation flow. Package/PCB designers must provide accurate models of their designs that allow a package/PCB-aware IC-level validation flow. A strategic tie-in between IC and handset manufacturers through an integrated CPS-aware analysis environment will enable faster design convergence and higher design optimization, resulting in the reduction of overall system costs.

The benefit of this approach will be most apparent in the successful use of high-speed DDR interfaces that handle increasing volumes of data transferred between an application processor and its associated memories, enabling the image- and video-based applications that run on today’s smartphones. However, this signal propagation is affected by both power and signal noise coming from the chip, package and board parasitics. As seen in Figure 3, various coupling mechanisms exist that impact the quality and the speed of the signal transmission. Typically, the design focus has been on the “signal integrity” aspect of

this transmission pathway, but given the reduced supply voltage levels, faster transmission speeds and shrinking jitter budgets, the impact of voltage supply fluctuations (“power integrity”) is increasingly seen. As noted earlier, unlike signal integrity, the accurate prediction of power/ground noise requires a holistic simulation framework that not only includes the parasitics and coupling present in the power/ground/signal interconnects of the package and PCB, but also the resistive, capacitive and inductive (RLC) parasitics of the on-die power/ground networks. These parasitic elements (self and coupled together with the switching current that results from the simultaneous switching of the I/O drivers) generate fluctuations or noise not only on the power/ground, but also on the signal interconnects. Based on the circuit activity, this noise varies from one clock period to another, impacting the speed of signal transmission and increasing the jitter. Predicting this jitter level is critical to undertake corrective actions on the IC, in the package or on the board, preventing design iterations or field failures.

Figure 3. Coupling Mechanisms Affecting the Transmission of Signals between ICs in a High-speed I/O DDR Interface



Summary

With more smartphones being sold than personal computers (PCs), the market opportunities from the sale of smartphones and other mobile devices, especially in the emerging BRIC economies, are considerable. Due to a variety of reasons, the BRIC markets require handset manufacturers to be nimble in providing differentiated or matching designs quickly and at the lowest possible prices. In terms of mobile and smartphone applications, consumers in these markets are highly segmented and vary considerably in their demands, purchasing ability and needs. Thus, to meet these needs, handset manufacturers must deliver new models quickly, keeping the component costs as low as possible to be competitive and to preserve their margins. To meet these goals, design teams from chip, package and system companies must work together, sharing data and models to enable a simulation- and analysis-driven design methodology. The target is to turnaround a handset design comprised of advanced application and baseband processors using compact, low-cost packages on a small form-factor PCB quickly, and to reach the market ahead of the competition.

Power consumption and delivery continue to present design and technology challenges for mobile system designers. The global nature of the CPS power/ground supply networks and its impact on system performance, reliability and functionality requires a systematic and strategic collaboration between these various parties. By adopting a comprehensive simulation-based design development flow, these teams cannot only ensure reduced design iterations, but also optimize the cost of the components across the system. ■

About the Author

Since joining Apache Design Solutions as a senior applications engineer, Aveek Sarkar has taken on different roles and responsibilities inside Apache, including director of product engineering. Prior to joining Apache, Mr. Sarkar worked for several years in Sun Microsystems on several generations of UltraSparc processors. Prior to Sun Microsystems, Mr. Sarkar held engineering positions at Cadence Design Systems and National Semiconductor. Mr. Sarkar holds a bachelor's degree in technology from the Indian Institute of Technology, Kanpur, a Master of Science degree in electrical engineering from Oregon State University, and a MBA from Santa Clara University.

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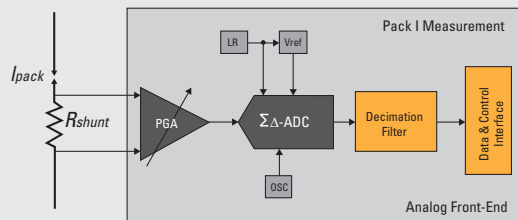
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differential ADC with bandwidth up to 10 kHz. The bandwidth requirement is related to the converter switching frequency that transforms continuous voltage into an alternative form required by EV and HEV engines. A data acquisition interface with a resolution between 16 bit and 21 bit permits measuring of charging/discharging currents from 2 mA up to 200A peak with a shunt resistor of 1 mΩ.

Figure 3. AFE for Battery Pack Current Measurement



Application Hardware Simulation for Guaranteeing System-level Performance

Even a well-designed AFE must be validated through simulation by coupling with system implementations and constraints to avoid system-level performance degradation and increase yield (e.g., how well the AFE can handle the high common mode voltage and reject switching noise, how each peripheral component contributes to the error budget and affects the total measurement accuracy, and how sensitive the system performance is to interactions among the involved components). To perform application-level simulation in a reasonable time, a multi-domain, multi-level and mixed-signal simulator is required. Moreover, appropriate high-level description models of all involved components are indispensable as well. These models include not only the AFE, but also the batteries, sensors, application schematics, processing unit, etc. For example, the battery model which incorporates multiple cells with different common mode voltages allows for the simulation of the AFE's performance of common mode voltage rejection.

By jointly simulating system hardware for target application, the

AFE's system-level performance can be assessed at an early stage, and the system-on-chip (SoC) integrator and end user can simulate the complete system to verify the charging and cell-balancing algorithm. This approach also helps to choose appropriate components and identify potential integration risks for guaranteeing system performance and reducing the bill-of-material (BoM).

Conclusion

Driven by continued development in rechargeable batteries, fabless companies must provide high-performance and flexible AFEs for building more reliable and competitive battery monitoring ICs. The two architectures of dedicated AFEs, presented herein, address the challenges of such ICs in terms of accuracy, cost, silicon area and power consumption. This article has focused on HV battery pack monitoring in EV and HEV; however, the highlighted issues are common to any system powered by a series-connected Li-ion battery pack. ■

About the Authors

Wei Guo received his doctorate in micro/nano-electronics from Grenoble Institute of Technology. He began his semiconductor career at Spintec of the French Atomic Energy Commission as a hybrid CMOS/magnetic IC design engineer and MRAM device modeling engineer. Mr. Guo has authored or co-authored several publications and holds an international patent. In 2010, he joined Dolphin Integration as an integration/application engineer. He was awarded the 2010 Chinese Outstanding Student Abroad. Mr. Guo can be reached at jazz@dolphin.fr.

Christian Domingues began his semiconductor career at the Techniques of Informatics and Microelectronics for Integrated Systems Architecture (TIMA) laboratory, where he worked as an analog research engineer for two years. In 2006, he joined Dolphin Integration as an analog designer, working in the field of high-performance measurement ΣΔ ADCs. He received a master's degree and a doctorate from the Polytechnical National Institute of Grenoble (INPG) in France in 2001 and 2005, respectively. Mr. Domingues can be reached at cdo.jazz@dolphin.fr.

Since these devices have a higher ASP, it would appear that there would be less COT and pricing pressure. However, since this device contains much more complexity, the capital costs of the tester also increases, so IP blocks still need to be tested in parallel and there still needs to be multisite at a high efficiency (95 percent), but the multi-site numbers are relaxed to the four-to-eight in-parallel range. Another large part of this relaxing is due to the higher cost of more complex SoC tester resources (e.g., RF or digital) as compared to those required for stand-alone PMICs (e.g., DC).

Since tester capital cost adds to the overall COT, there is always a decision to be made for more parallelism versus tester and handler capital costs. This would include higher capital costs for a larger configuration of the tester and, potentially, a higher capital cost for the handler offset by the faster effective test time of higher density multisite. Higher multi-site handlers can cost more depending on the baseline of sites used; for example, if the baseline is derived from the cost of a one- or four-site handler, then an eight- or 16-site handler will typically be more expensive.

Tester Trends

Automatic test equipment (ATE) manufacturers working with customers have applied several techniques to address PMIC testing needs.

One technique involves a higher integration of resources. Before parallelism drove cost pressures, a tester resource board might have a few “pins” per personal computer (PC) board. Pins are defined as independently functioning resources that allow each pin to have different settings (e.g., voltage levels, timing and clocks). A higher level of integration allows for much more than this. For example, now 128 individual digital pins per board are available.

Another technique involves the integration of multiple functions within a pin. For example, it is now possible to have digital pins with individual clocks, voltage levels, timing and DC capability per board. Even for more sophisticated resources such as analog and mixed-signal, the number of resources per board has increased significantly.

Because of the previous two points and the higher integration of these resources to a lower cost infrastructure of the system for the simpler stand-alone PMIC devices, the test-head fixture these boards typically plug into has shrunk significantly. For more complex integrated PMICs, the larger test-head footprint is still used as needed.

ATE resources are being designed more efficiently to lower overhead in testing multiple devices and concurrently testing IP blocks. The net result is a lowered individual test time and an increased MSE. An example of this includes resources designed with

dual port memories so test data can be uploaded and download simultaneously while testing the device. The bandgap reference trim is a good test to do in parallel on multi-site applications because it requires parallel DC measurements and digital register reads and writes on a per-device basis. Also, DC tests are done as part of the digital functional tests which are testing clocks and digital logic.

Conclusion

PMICs continue to be a growing market segment due to many factors, but the growing demand for portable consumer devices is a primary driver. Two diverging market segments for PMICs have been shown; there are some similarities and many differences in testing and economic requirements. Stand-alone PMICs have very low ASPs, requiring digital, accurate DC resources and audio capabilities. They must have a high degree of efficient parallelism both inside the individual device (concurrent test) and in multisite (eight to 16 sites). The PMICs that are integrated into SoCs must have all the test capability that stand-alone PMICs have and also the additional requirements of RF, analog/mixed-signal and higher end digital capability. Furthermore, they must have a high degree of efficient concurrent test capability, but usually relaxed numbers of multisite (four to eight sites), mainly due to the increased capital cost of the more complex tester resources that are required.

The higher cost of added concurrency and multisite has been offset by ATE manufacturers through product offerings. These include a higher integration of tester resources, adding more functionality per resource and the building of a smaller, lower cost infrastructure for the tester footprint. ■

About the Author

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and TV displays, and general lighting to automotive applications, artistic expressions, medical procedures and industrial applications. Semiconductor light sources will save huge amounts of energy and costs, while making our products and experiences better and our planet greener.

Let semiconductor light sources shine! ■

About the Author

Dr. Paul Russo currently serves as chairman and chief executive officer of GEO Semiconductor. He also serves as director or lead director of three other

venture-funded technology companies, including FONOLO, SiOnyx – the “Black Silicon” Company and SBG Labs. Dr. Russo received his bachelor’s degree in engineering from McGill University and his master’s and doctorate in electrical engineering and computer science from the University of California at Berkeley.

Dr. Russo holds six U.S. patents, is a Fellow of the IEEE and has received numerous RCA and industry awards, including the IEEE Centennial Medal and the 2006 Tech Pioneer Award from the World Economic Forum. Dr. Russo is a member of the Global Semiconductor Alliance (GSA) Emerging Company CEO Council and participates in its EDA interest group.

capacities are being built at the leading edge. Third, we must maintain strong partnerships with our foundry suppliers.

Marvell's foundry suppliers know that we are true long-term partners, and as a result, we have our fair share of foundry allocation. Our customers are the "who's who" in the industry, so our foundry partners want to help us meet their requirements. Furthermore, many of our products are portable across many different foundries, which is a great safety measure if a given fab happens to be in a situation of tight supply.

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In the area of systems-on-chip (SoCs), Renesas had seven plants shut down in March, including plants that manufactured SoC large-scale integrations (LSIs) for automotive, digital camera, and mobile phone manufacturers. Fujitsu had two SoC plants affected, and while one resumed partial production at the end of March, the other was not ready until recently due to aftershocks. Toshiba's SoC LSI plant was hit multiple times, and another magnitude-7.1 aftershock halted the company's ability to restart production.

Wafers, the backbone of the semiconductor industry, saw a halt in production as Shin-Etsu Handotai (Shin-Etsu), MEMC and SUMCO all temporarily shut down production. Shin-Etsu alone produces a quarter of the world's wafer supply.

Shin-Etsu was probably the hardest hit in terms of 300mm wafer manufacturing capability. Their fab in Fukushima Prefecture was not expected to restart operations until the end of April. Even then, as electrical supply is still a question, the facility is not expected to perform at 100 percent. MEMC has resumed production at their 300mm wafer facility in Utsunomiya. Also, SUMCO's Yonezawa plant in Yamagata Prefecture resumed operations quickly.

Most large semiconductor manufacturers have adamantly stated that there are no material supply issues and there should be no semiconductor production constraints due to material shortages. Major semiconductor manufacturers that currently use 300mm wafers have stated that production is not expected to be interrupted due to the earthquake in Japan.

Liquid crystal display (LCD) panels are not just for TVs, they are in cellphones, digital cameras, tablets, etc., and Japan supplies almost 60 percent of the world's LCD components. One of those components is indium tin oxide (ITO) film produced by Kuramoto in Japan. They have the majority market share, and their production has been interrupted. Toshiba's Fukaya plant lost a month of LCD production targeted for the TV and cellphone market, as well as many others.

Looking across the board, these closures may imply that the whole industry will suffer significant issues with inventory, but there are other suppliers available in Asia Pacific that many vendors are partnering with during this time. Smaller vendors may find themselves pushed out of the market as component prices increase while end-use average selling prices (ASPs) remain constant, digging into their profit margins.

Q: *Marvell has been a long-time member of GSA since 1999 and currently sits on its board of directors. What has been one of the greatest benefits of being a GSA member?*

A: GSA has always been a great proponent of collaboration, integration and innovation in the semiconductor industry. Marvell is happy to aid in fostering technological advancement with our customers and amongst fellow semiconductor companies. ■

As Japan is a major consumer of technology, an immediate effect is the decline in personal spending. Sales in Japan declined 8.5 percent in March YoY. As uncertainty continues and the infrastructure continues to take a beating, this decline will become a trend for the second and third quarter in Japan, affecting consumer end-use sales for this region. If manufacturers can bring production online for the holiday shopping season, then consumer confidence will increase by the first quarter 2012. In addition, the growing demand for high-end technology such as smartphones and cameras in developing countries is offsetting Japan's decline in consumer demand.

Conclusion

In conclusion, when discussing the consumer electronics market, the earthquake will not have a lasting effect on the supply chain. There will be interruptions throughout 2011 that will be felt the hardest during the holiday purchasing season, and with the threat of aftershocks continuing to plague Japan, the situation may worsen.

In general, vendors carry approximately a month of component supply and then another month of finished product in sales channels—giving most vendors who can find the materials time to adjust their production line before consumers are aware of any change.

Significant uncertainty surrounding Japan remains as aftershocks continue to threaten rebuilding efforts and seismologists warn of another magnitude-8 earthquake. Most companies are still evaluating the total affect of the earthquake and are forecasting 2011 and 2012 as "uncertain." ■

About the Author

Michell Prunty is the senior consumer analyst for Semico Research Corporation. Her responsibilities include conducting research for the Semico MAP Model and authoring MAP Model studies. Ms. Prunty's emphasis is on emerging consumer markets that complement the Digital Home Portfolio. Before joining Semico, she worked on numerous consulting projects, including process improvement for Rogers Corporation and system analysis for Grand Canyon University. Ms. Prunty's background in programming and IT management combined with a degree in small business from Arizona State University provide her with insight into the semiconductor industry from the end-user point of view.

in Table 2, Japan's economy is expected to suffer the biggest negative impact in the second quarter 2011. However, beginning in late third quarter 2011 or early fourth quarter 2011, Japan's GDP is forecasted to grow once again as the rebuilding process, with its attendant spending and investment programs, begins in earnest. IC Insights believes that this rebuilding process will gain momentum in the first half of 2012 and continue to impact Japan's GDP in a positive way.

Similar to Japan's GDP, first quarter 2011 worldwide semiconductor sales were only slightly impacted by the earthquake and the second quarter of 2011 is likely to be most affected. With a spurt of semiconductor inventory building likely to occur in the second quarter 2011, semiconductor sales are expected to be only moderately negatively impacted. Moreover, any "lost" sales in second quarter 2011 are forecasted to be shipped in the third or fourth quarter 2011.

IC Insights believes that the slightly negative first quarter 2011 and slightly positive fourth quarter 2011 effects on worldwide semiconductor sales will essentially cancel each other out. The same is true for the moderately negative second quarter 2011 and moderately positive third quarter 2011 effects. This assumption of a "cancelling" effect is the primary reason that IC Insights has not changed its full-year forecast of at least 10 percent semiconductor industry growth in 2011.

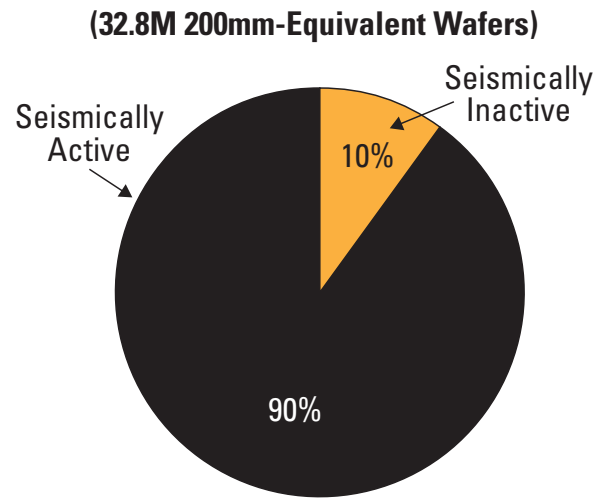
If key components of the semiconductor supply chain are constrained for an extended period of time, there is a potential shortfall to IC Insights' current forecast for IC unit volume shipment growth of 9 percent in 2011. However, assuming that electronic system and IC demand remains strong, any significant constraint to IC supply will likely lead to increasing IC average selling prices (ASPs), especially during the seasonally strong second half of the year. With IC Insights' current forecast calling for only a 1 percent increase in the overall IC ASP in 2011, there is considerable upside potential to this forecast.

Overall, IC Insights expects that the IC market will grow by at least 10 percent in 2011, with any shortfall in unit volume shipments being offset by increasing IC ASPs.

As shown in Figure 1, fully 90 percent of pure-play IC foundry capacity is located in seismically active regions! Since the two largest IC foundries in the world (i.e., Taiwan Semiconductor Manufacturing Company (TSMC) and United Microelectronics Corporation (UMC)) have such a significant presence in Taiwan, a disastrous earthquake or typhoon in that country would have serious ramifications for the entire electronics supply chain. In fact, it is IC Insights' opinion that because IC foundries have so many different

customers and are sole-source producers for such a wide variety of part types, the ramifications of damage to IC foundry fabrication facilities would be much greater than damage done to the IC fabs of individual integrated device manufacturers (IDMs).

Figure 1. Seismically Active Pure-play Foundry Capacity in 2010



Source: IC Insights

Although the majority of the IC industry's fabrication capacity has always been located in "dangerous" areas, most buyers of ICs don't give this a second thought. However, while these tragic events are impossible to predict, they are not impossible to plan for. IC Insights believes that the March 11, 2011 Japan earthquake might be the wake-up call that spurs the entire electronics supply chain to create new contingency plans, especially with respect to the IC foundry industry.

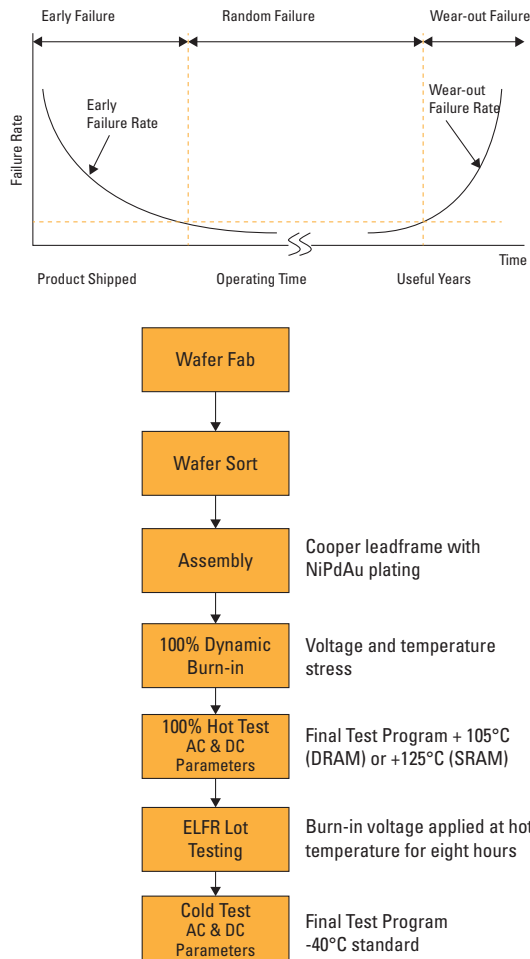
In terms of the supply chain, we should keep in mind that one company's misfortune is another's opportunity. Whether the product is automobiles, electronic systems, silicon wafers or Flash memory, other suppliers worldwide will aggressively attempt to compensate for any shortfall in supply. And though it is not always easy to switch suppliers of key products, businesses eventually find a way to move forward. ■

About the Author

Bill McClean began his market research career in the IC industry in 1980 and founded IC Insights in 1997. During his 31 years of tracking the IC industry, Mr. McClean has specialized in market and technology trend forecasting and developed the IC industry-cycle model. At IC Insights, he serves as managing editor of the company's market research studies and reports. In addition, he is an instructor for IC Insights' seminars and has been a guest speaker at many important annual conferences held worldwide (e.g., SEMI's ISS and Electronic Materials Conferences, The China Electronics Conference and The European Microelectronics Summit). Mr. McClean received his Bachelor of Science degree in marketing and an associate degree in aviation from the University of Illinois.

rate (ELFR) to predict low failure-in-time (FIT) performance and ensure long-term reliability.

Figure 2. Bath Tub Curve with Enhanced Reliability Test Flow



Package-level Reliability

One key point to consider when selecting a semiconductor device for long operating life is package reliability. The use of copper for leadframe material has been shown to enhance long-term reliability by contributing to the durability of solder joints and improving thermal dissipation. By using nickel-palladium-gold (NiPdAu) for the solder plating of the leads, this eliminates the potential for “whiskering.”

Enhanced Joint Reliability and Improved Thermal Dissipation

During the service life of an electronics system, the printed circuit board (PCB) and the soldered components may be subjected to repeated thermal changes over a period of time from negative 40 C to 85 C. Every type of material on the PCB has a different coefficient of thermal expansion (CTE). The differing expansion rates can result in pushing and pulling stresses being concentrated at the points where they interface, which are often the solder joints. Over a long lifecycle, the effects of the stress may accumulate to the point that a crack appears, causing an electrical discontinuity.

Thin small outline package (TSOP) types used for memory use leadframes with Alloy42 (CTE of about 5 parts per million (ppm)/C), which match to the chip inside (CTE of about 3 ppm/C) and expand at similar rates, minimize internal forces. However,

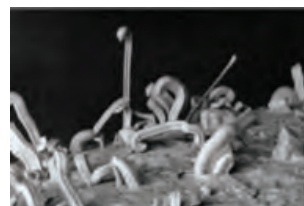
parts are mounted on a PCB with copper traces and landing pads. Copper has a CTE of 17 ppm/C and expands more readily than those made of Alloy42. Memory manufacturers can enhance joint reliability by using a copper leadframe, which expands and contracts proportionally to the copper pads on the PCB, minimizing the stresses at the respective solder joints.

In theory, the higher the temperature levels at the die level, the shorter the lifespan of a part. A copper leadframe with improved thermal conductivity has the benefit of reducing the thermal resistance of the component and improving heat transfers by allowing better heat dissipation from the die to the leadframe and eventually to the free air. The die (or junction) temperature is given by the formula $T_j = T_a + \theta_{ja} \times P$, where P is the power the device consumes in watts, and θ_{ja} is thermal resistance. Using a copper leadframe with a lower θ_{ja} provides a substantial reduction in junction temperature of typically 5 C to 10 C.

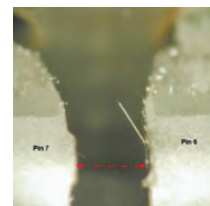
Whiskering

One of the disadvantages of lead-free plating solutions for packaging is a phenomenon called “whiskering,” where over long-term operation, a component can sprout “whiskers” from the solder plating on its terminals. If not prevented, these whiskers can bridge metal contacts causing a short circuit.

Figure 3. Whiskering



Whiskers forming on anonymous part. (Photo by NASA)



If a whisker bridges this gap across the pins, or it breaks, there could be a short-circuit and a system could fail. (Photo by NASA)

One whisker mitigation method recommended by JEDEC is to use pure matte tin (Sn) as the lead-free plating material and to anneal this. The International Electronics Manufacturing Initiative (iNEMI) recommends an improved method, which lists NiPdAu as the preferred plating material for eliminating the risk of whiskering. By offering memory devices with copper leadframes and NiPdAu, plating memory vendors can guarantee improved long-term reliability at both die and package levels.

Summary

A number of memory vendors have recognized the requirements to support markets with long-life and quality demands, including extended temperature applications. When selecting memory, the system engineer needs to consider qualifying multiple sources for each component to mitigate the risk of component obsolescence. Furthermore, the system engineer needs to select a memory vendor with a well-defined product strategy to ensure long-term availability of each product family so the engineer is not forced to redesign the complete system or carry out a very expensive and risky LTB. ■

About the Author

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technology for notebook supplies enables savings of 80 to 85 percent of energy consumed when the device is not being physically charged. We are now rolling that out in handheld devices as well as low-power adaptor capabilities.

Q: *The European Commission has acknowledged the strategic importance of advanced manufacturing to Europe's growth, yet little has been done to promote this. As a Europe-based company, what are your thoughts on this, and with your manufacturing outsourced largely to Asia and 34 percent of your 2010 revenue coming from China, do you think a renewed focus on advanced manufacturing in Europe is important?*

A: In the semiconductor business, it's important to be a leader in the markets you serve and to drive the strength of your technology, but it's much more critical to be a worldwide leader than to be a regional factor. Certainly, there is a significant opportunity to use the thought leadership from our technologists in Europe, but in conjunction have the heavy lifting of absolute product design performed in areas that can drive more effective utilization. It's critical that Europe continues to maintain core technology so the thought leadership can be provided for mass usage. Protecting and maintaining that technology leadership allows Europe to protect and stimulate the economy. That said, I think Europe could use a little more of a—for lack of a better term—"Silicon Valley approach" that is more supportive of entrepreneurial start-ups in technology. Indeed, it's more about creating an entrepreneurial climate to advance technological start-ups and create additional value than just advanced manufacturing.

Q: *In an article you authored for EE Times Asia earlier this year, you identified four major macro-level trends that are expected to drive electronic growth—sustainable, energy-efficient development; affordable, personalized healthcare; comfortable, efficient and safe mobility; and low-power fit for purpose security. Could you elaborate on the opportunities these trends offer and discuss NXP's plans for capturing the resultant growth?*

A: These key mega trends (i.e., mobile connected devices, security and healthcare) drive a \$1.1 trillion market. With the leadership position NXP holds, we expect to continue to drive growth propelled by these key societal trends. Though NXP is already active in the healthcare market, the "big opportunity" in healthcare is more of a long-term opportunity. However, in the near term, security is increasingly critical with electronic transactions. When you consider Maslow's Hierarchy of Needs, security is, in whatever form you identify it, a significant need. Being able to facilitate that from an electronic viewpoint represents a significant growth opportunity, which requires a different mindset, where we have to facilitate the ecosystem as opposed to just shipping and selling semiconductor components.

Q: *NXP targets applications that require stringent overall system and subsystem performance and, consequently, has gained deep applications expertise. How does this expertise enhance NXP's engagement in its customers' product platforms?*

A: High-performance mixed-signal solutions are increasingly

desired by customers serving a broad range of applications, including automotive, identification, wireless infrastructure, lighting, industrial, mobile, consumer and computing. Designing high-performance mixed-signal solutions requires deep application insight, systems design capabilities, architect-level customer relationships, a broad portfolio of both analog and digital technologies, and an ability to develop sophisticated analog and mixed-signal process technologies. Historically, this expertise has only been developed by the largest and most sophisticated semiconductor companies who have a deep understanding of the challenges that accompany analog design, miniaturization, integration, digital processors and systems solutions, and also in developing and running specialty manufacturing processes at high volumes and yields. NXP strives to engage with customers so we can drive a solution that will provide for lower costs, faster time-to-market and higher performance than competitors.

Q: *With customer demand consistently driving ever shorter design cycles, how does NXP assist customers in meeting their time-to-market goals?*

A: NXP has implemented a new approach to serving our customers, investing significant additional resources in our sales and marketing organizations. Despite the recent economic downturn, we hired over 100 additional field application engineers in 2009 and 2010 to better serve our customers. In addition, we have created "application marketing" teams that focus on delivering solutions that include as many suitable NXP components as possible in their system reference designs, thus assisting us to achieve greater cross selling between our product lines while also helping our customers accelerate their time-to-market. With the increased number of application engineers and our applications marketing approach, we are able to engage with more design locations, ranging from our largest, highest volume customers to our mid-size customers.

Q: *NXP recently announced an expanded collaboration with ARM on the design of ARM cores and ARM-based microcontroller units (MCUs). How does this partnership benefit NXP customers, and in what way do you expect this collaboration to assist NXP in breaking new ground?*

A: With 100 million ARM processor-based microcontrollers shipped, NXP has reached a major milestone in our commitment to deliver the broadest range of choice available for customers migrating from eight- or 16-bit architectures to 32-bit ARM. NXP's portfolio of Cortex-M0, Cortex-M3 and Cortex-M4 series processor-based microcontrollers offers a wide range of unique features, peripherals and memory options. The LPC1100 series, based on the energy-efficient Cortex-M0 processor, features the industry's lowest active power and a tiny footprint starting at 5mm².

Looking ahead, this strategic licensing agreement gives us the ability to continue to break new ground with ARM on the future of the 32-bit MCU landscape. Under the agreement, NXP will also be working with ARM in developing and expanding ARM's future microcontroller roadmap in various areas, including performance and energy efficiency. ■