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UNITED STATES DISTRICT COURT
DISTRICT OF OREGON
PORTLAND DIVISION

BESANG INC.,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 3:23-cv-00113-HZ

**INTEL CORPORATION'S
INVALIDITY CONTENTIONS**

1- INTEL'S INVALIDITY CONTENTIONS

Pursuant to the case schedule set by the court's in the minutes of the Rule 16 telephone conference (Dkt. 46) and N.D. Cal. Local Patent Rules 3-3 and 3-4, Defendant Intel Corporation ("Intel") provides its Invalidity Contentions to Plaintiff BeSang LLC ("BeSang") with respect to U.S. Patent No. 7,378,702 ("the '702 patent" or "the Asserted Patent"). These contentions address claims 13, 14, and 16 of the '702 patent (collectively, the "Asserted Claims") as asserted by BeSang in its Infringement Contentions served on May 12, 2023 ("Infringement Contentions"). Intel's investigation in connection with this lawsuit is continuing. Accordingly, Intel reserves the right to amend and supplement these Invalidity Contentions as the case proceeds.

I. PRELIMINARY STATEMENT AND RESERVATION OF RIGHTS

These Invalidity Contentions consider and apply BeSang's apparent view of the scope and interpretation of the Asserted Claims as set forth in BeSang's Infringement Contentions as understood by Intel. BeSang's Infringement Contentions contradict the teaching of the Asserted Patent, contradict the understanding of the claim terms by a person of ordinary skill in the art at the time of the alleged invention, and are vague and conclusory concerning how certain claim limitations supposedly read on the accused products. Accordingly, Intel is unable to discern BeSang's position regarding the construction of numerous claim limitations and has provided these Invalidity Contentions based in part on its present understanding of BeSang's apparent constructions. Where noted, these Invalidity Contentions also address the teachings of the prior art under claim interpretations that differ from BeSang's apparent constructions.

Any assertion herein that a particular limitation is disclosed by a prior art reference or references may be based in part on BeSang's apparent interpretation and is not (nor is it intended to be) an admission by Intel that any such apparent construction is supportable or correct. Further, BeSang's Infringement Contentions lack the specificity to put Intel on adequate notice as to BeSang's infringement theories. For instance, BeSang failed to identify with adequate specificity the accused features and further failed to provide explanations for how the accused

products practice the asserted claim language. Thus, Intel was not put on notice as to what specific products allegedly infringe and how they allegedly infringe. BeSang's Infringement Contentions therefore do not satisfy N.D. Cal. Local Patent Rule 3-1(c)'s requirement of providing "a chart identifying specifically where and how each limitation of each asserted claim is found within each Accused Instrumentality." To the extent that BeSang is granted leave to amend its Infringement Contentions to attempt to address these deficiencies, Intel reserves the right to supplement these Invalidity Contentions in response to BeSang's amendments.

Any statement herein describing or tending to describe any claim limitation is provided solely for the purpose of understanding the relevant prior art. Intel expressly reserves all its rights with respect to claim construction. Nothing contained in these Invalidity Contentions or any accompanying claim chart exhibits should be understood or deemed to be an express or implied admission or contention with respect to the proper constructions of any terms in the Asserted Claims. The information provided shall not be deemed an admission regarding the scope of any claims or the proper construction of those claims or any terms contained therein. Intel expressly reserves the right to take positions with respect to claim construction issues that are inconsistent with, or even contradictory to, claim construction positions expressed or implied in these Invalidity Contentions. Moreover, nothing herein admits in any way that the accused products, or any of Intel's other products or services, infringe any of the Asserted Claims. These Invalidity Contentions are made in the alternative and should not be interpreted to rely upon, or in any way affect, the noninfringement arguments that Intel may or intends to assert in this case. Intel does not adopt any of the constructions or interpretations of the Asserted Claims impliedly or expressly applied by BeSang in its infringement contentions, and Intel denies infringement of each and every Asserted Claim.

To the extent that prior art cited for a particular limitation discloses features that are the same or similar in some respects to the alleged features of the accused products as set forth in BeSang's Infringement Contentions, Intel does not concede that those limitations are in fact met

by those accused products.

Intel further reserves the right to supplement and amend these Invalidity Contentions and associated documents based on information discovered from its ongoing investigation, analysis, and discovery, Intel's consultation with experts and others, and contentions or court rulings on relevant issues such as claim construction. For example, since discovery has just begun, deposing the alleged inventor may reveal information that affects the disclosures and contentions herein. Also, Intel has not yet completed discovery from third parties who have information concerning the prior art cited herein and possible additional art.

Intel reserves the right to amend these Invalidity Contentions and to modify the selection of prior art references in the event BeSang serves supplemental or amended Infringement Contentions.

Because Intel is continuing to search for and analyze relevant prior art, Intel reserves the right to revise, amend, and supplement the information provided herein, including identifying, charting, and relying upon additional prior art references, relevant disclosures, and bases for Invalidity Contentions. Additional prior art, disclosures, and invalidity defects, whether cited in this disclosure and whether known or not known to Intel, may become relevant as investigation, analysis, and discovery continue. Intel is currently unaware of the extent, if any, to which BeSang will contend that limitations of the Asserted Claims are not disclosed in the prior art identified by Intel. To the extent that such an issue arises, Intel reserves the right to identify and rely upon other references or portions of references regarding the allegedly missing limitation(s).

Further, Intel intends to diligently seek discovery from third parties to demonstrate earlier invention by other parties under at least 35 U.S.C. § 102(g).¹ Intel further intends to take discovery on issues including but not limited to inventorship and/or derivation under 35 U.S.C. § 102(f), public use and/or the on-sale bar under 35 U.S.C. § 102(b), and/or the requirements of

¹ All references to 35 U.S.C. §§ 102 and 103 in these Invalidity Contentions relate to pre-AIA versions.

35 U.S.C. § 112. Intel reserves the right to present additional prior art references and/or disclosures under 35 U.S.C. §§ 102, 103, and/or 112, and to supplement or amend these Invalidity Contentions if and when further information becomes available.

Subject to its reservation of rights, Intel identifies below each item of prior art that anticipates or renders obvious one or more of the Asserted Claims in Section III. To the extent references listed in Section III are not identified as items of prior art that anticipate or render obvious an asserted claim, Intel intends to rely on these references as background and as evidence of the state of the art at the time of the alleged invention. As stated above, Intel reserves the right to rely upon additional prior art that may be uncovered during continuing investigation and discovery.

The claim chart exhibits accompanying these Invalidity Contentions include, but are not limited to, exemplary obviousness combinations of references under 35 U.S.C. § 103. The disclosed combinations are not meant to be exhaustive. As reflected in the attached exhibits, the discussion herein, and in the references themselves, all limitations of the Asserted Claims were disclosed in the prior art, and one of ordinary skill in the art would have been motivated to combine the teachings of the prior art. Each of the references cited herein or in the attached exhibits may be combined and modified in a number of obvious ways to achieve the claimed features, including those disclosed in the attached exhibits. Further, the suggested obviousness combinations are in the alternative to Intel's anticipation contentions. The obviousness contentions set forth in these contentions should not be construed to suggest that any reference is not anticipatory in its own right.

Additionally, many of the prior art references are related patent applications and issued patents that contain substantially the same subject matter (e.g., published U.S. patent applications, and issued U.S. patents, foreign applications or issued patents). Any citation to or quotation from any of these patent applications or patents, therefore, should be understood as encompassing any parallel citation to the same subject matter in other related or corresponding

applications or patents. Intel reserves the right to later rely upon all references or portions of references provided in Section III to supplement or amend its disclosures contained herein. Also, to the extent not expressly mentioned herein, Intel incorporates by reference (1) any and all prior art contained or identified in documents produced thus far by BeSang in this case, and (2) any and all additional materials regarding invalidity that should have been produced to Intel but has not been produced to date, to the extent that any exist.

Finally, Intel is investigating and anticipates seeking discovery from BeSang regarding knowledge or use by others under § 102(a), public use or on-sale bar under § 102(b), derivation or prior inventorship under §§ 102(f)/(g), and the identity of persons or entities involved in and the circumstances surrounding the making of the claimed invention. Intel reserves all rights to rely on conception and reduction to practice documents produced (or to be produced) by BeSang.

II. ANTICIPATION AND OBVIOUSNESS

The prior art references or systems/products identified in these contentions anticipate one or more of the Asserted Claims under 35 U.S.C. §§ 102(a), (b), (e), and/or (g). These references or systems/products also invalidate the Asserted Claims under 35 U.S.C. § 103. To the extent any of the identified prior art references incorporate or refer to other prior art references, the full disclosure of all such references is a single piece of prior art under 35 U.S.C. § 102. Each claim chart provided for a prior art reference or system/product should be understood to incorporate by reference all other prior art references or systems/products incorporated or referred to in the prior art and all claim charts provided for those other references or systems/products.

As a general matter, all portions of each prior art item are relied upon to support the disclosure of each patent claim limitation, as all portions provide general support. Supporting citations are nevertheless provided, but do not necessarily represent every location where a particular claim term may be found in the prior art reference or system/product. Intel reserves the right to rely on additional, or different, portions of the prior art references or systems/products other than those specifically cited in these claim chart exhibits and to supplement and/or amend

the accompanying claim chart exhibits.

A person having ordinary skill in the art would have been motivated to combine or adapt known or familiar systems and methods in the art. Each of the prior art references or systems/products identified in these contentions relate to systems and methods that were known to offer certain advantages or improvements over the state of the art. A person having ordinary skill in the art at the time of the alleged invention would have been motivated to combine or modify the identified prior art references or systems/products.

In addition to the exemplary prior art references or systems/products and teachings identified in these contentions, the common knowledge of those of ordinary skill in the art also constitutes prior art, and may be relied on by Intel through testimony or declarations in combination with the identified prior art. The knowledge of a person of ordinary skill in the art at the time of the alleged invention would also include, for example, the known advantages and disadvantages of each of the limitations recited in the Asserted Claims. It would have been obvious to combine the references and teachings identified herein with one another, based on the nature of the problem to be solved, the general knowledge of a person of ordinary skill in the art at the time of the alleged invention, the teachings of other art in existence at that time, and the recognition of similarities between the art and the claimed features. On these bases, each identified prior art reference or product/system can be combined with the others if a particular prior art item lacks or does not disclose a limitation or feature of an asserted claim.

More particularly, and without limitation, all of the following recognized rationales support a finding of obviousness:

- 1) Combining prior art elements according to known methods to yield predictable results;
- 2) Simple substitution of one known element for another to obtain predictable results;
- 3) Use of known techniques to improve similar devices, methods, or products in the same way;

- 4) Applying a known technique to a known device, method, or product ready for improvement to yield predictable results;
- 5) “Obvious to try”—i.e., choosing from a finite number of known, predictable solutions, with a reasonable expectation of success;
- 6) Known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to one of ordinary skill in the art; and
- 7) Some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art item(s) or to combine prior art teachings to arrive at the claimed invention.

The rationales identified above would have motivated a person of skill in the art at the time of the alleged invention to combine the above-identified prior art items and teachings. As the Supreme Court held in *KSR*, “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007). The Supreme Court further held that:

[w]hen a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 417.

Moreover, the Supreme Court held that “in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.* at 420. Indeed, the Supreme Court held that it is sufficient that a combination of elements was “obvious to try,” holding that, “[w]hen there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to

pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense.” *Id.* at 421.

Patents like the one asserted here are invalid, the Supreme Court explained, because “[g]ranting patent protection to advances that would occur in the ordinary course without real innovation retards progress and may, in the case of patents combining previously known elements, deprive prior inventions of their value or utility.” *Id.* at 419. Here, each of the prior art items identified in Intel’s Invalidity Contentions is directed to the same field as that of the Asserted Patent. Further, each prior art item was directed to the same problem or problems that the Asserted Patent purportedly solved. The Asserted Claims therefore represent—at the very most—mere “ordinary skill and common sense,” not innovation. Stated differently, the alleged inventions are, at most, obvious combinations or adaptations of well-known technology used in predictable ways.

Although a teaching, suggestion, or motivation to combine references is not required, a motivation to modify a particular reference or system/product or to combine any two or more references or systems/products comes from (1) the nature of the problem being solved; (2) the teachings of the prior art; (3) the knowledge and common sense of persons of ordinary skill in the art at the time of the alleged invention; (4) the fact that all of the references and systems/products concern systems and methods related to the subject matter of the Asserted Patent; (5) the fact that many of the authors of the references and developers of systems/production were part of the same industry or community; (6) the existence of similar improvements in similar applications; (7) the number of identified, predictable solutions to the problem addressed by the asserted patents; and (8) considerations of efficiency, effectiveness, convenience, cost-savings, and accessibility. The illustrative obviousness combinations described in the attached claim charts are not intended to be exhaustive, and in many instances, a prior art reference in combination with the common knowledge and/or the state of the art prior to the respective filing or asserted priority date of the Asserted Patent would have been enough to render obvious one or more of the Asserted Claims. A person of ordinary skill in the art at the time of the alleged invention also would have had a

reasonable expectation of success in implementing the combinations.

Many documents in the file history and other publicly available documents before the Asserted Patent's (and related patents and applications) effective filing dates anticipate the claimed invention(s) and/or show a motivation to modify and/or combine elements to render obvious the Asserted Claims. Intel incorporates by reference any statements and reasons set forth by the Examiner during prosecution of the '702 patent, related patent applications, and any patents or patent applications incorporated by reference in the '702 patent and related patent applications as to why it would have been obvious to modify or combine references or systems/products to achieve the limitations of the Asserted Claims.

The suggested obviousness combinations are not to be construed to suggest that any reference does not anticipate the claimed subject matter on its own. In particular, Intel is currently unaware of the extent, if any, to which BeSang will contend that certain elements of the Asserted Claims are not disclosed in the prior art identified by Intel as anticipatory. In many instances where a particular contention calls for, or requires, combining references, any one of a number of references or systems/products can be combined. The inclusion of certain exemplary combinations does not exclude other combinations of the prior art, including prior art identified in these contentions. At this stage of the litigation, prior to further factual and expert investigation, Intel cannot identify and list all potentially relevant combinations. If and to the extent that BeSang challenges the combination of any of these references or systems/products with respect to any limitations of the Asserted Claims, Intel reserves the right to identify other prior art references or systems/products and combinations of the same, which may make obvious the addition of the allegedly missing element to the disclosed system or method, and to supplement its contentions to identify additional reasons to combine particular references with one another. In addition, Intel expects to provide expert analysis and testimony showing that combinations would have been obvious to one of ordinary skill in the art in the relevant timeframe.

By way of example only, to the extent that any reference or system/product described in

these contentions is found not to disclose the “being bonded” limitation of claim 13 under BeSang’s apparent construction, it would have been obvious to combine that reference or system/product with, for example, U.S. Patent Appl. Pub. No. 2002/0028541A1 (“Lee”), U.S. Patent No. 6,034,882 (“Johnson ’882”), U.S. Patent No. 6,525,953 (“Johnson ’953”), U.S. Patent No. 5,091,762 (“Watanabe”), U.S. Patent No. 5,571,730 (“Park”), U.S. Patent No. 8,791,581 (“Leedy”), U.S. Patent Appl. Pub. No. 2005/0112846 (“Meyer”), Chinese Pat. No. CN 1099695C (“Zhang”), the Matrix Semiconductor 3D PROM product (“Crowley”), Novel Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell (“Endoh”), U.S. Patent No. 5,882,987 (“Srikrishnan”), U.S. Patent Appl. Pub. No. 2005/0133851 (“Forbes”), Silicon Processing Vol. 1 (“Wolf 1”), Silicon Processing Vol. 4 (“Wolf 4”), U.S. Patent No. 5,330,935 (“Dobuzinsky”), U.S. Patent No. 5,563,084 (“Ramm”), U.S. Patent No. 5,936,274 (“Forbes ’274”), U.S. Patent No. 5,981,341 (“Kim”), U.S. Patent No. 6,355,501 (“Fung”), and/or U.S. Patent No. 6,449,186 (“Noble”). *See, e.g.*, Lee at ¶¶107-111; Johnson ’882 at 11:59-12:65; Johnson ’953 at 8:35-53; Watanabe at 5:11-26; Park at 6:57-7:22; Leedy at 9:3-49; Zhang at pp 4, 9; Crowley at ¶¶1, 3; Endoh at 947 col. 2 - 948 col. 2; Srikrishnan at 5:25-45; Forbes at ¶¶28-32; Wolf 1 at 259-61; Wolf 4 at 537-50; Dobuzinsky at 6:32-33; Ramm at 4:33-52; Forbes ’274 at Figs. 5, 10-12; Kim at 5:47-54; Fung at 6:15-51; Noble at 3:59-64. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to incorporate these teachings because, for example, they related to techniques that were known in the prior art and implementing them would have yielded predictable results, including the operation of memory cells. The combination also would have improved systems into which the teachings were incorporated by providing benefits, including increasing integration density, thereby improving wafer utilization, and would have been the use of known techniques to improve similar apparatus in the same way.

By way of example only, to the extent that any reference or system/product described in these contentions is found not to disclose the “being bonded” limitation of claim 13 under a

construction that requires wafer bonding, it would have been obvious to combine that reference or system/product with, for example, U.S. Patent No. 5,091,762 (“Watanabe”), U.S. Patent No. 5,571,730 (“Park”), U.S. Pat. No. 8,791,581 (“Leedy”), U.S. Patent Appl. Pub. No. 2005/0112846 (“Meyer”), U.S. Patent No. 5,882,987 (“Srikrishnan”), Silicon Processing Vol. 1 (“Wolf 1”), Silicon Processing Vol. 4 (“Wolf 4”), U.S. Patent No. 6,943,067 (“Greenlaw”), Creating 3D Circuits (“Sailer”), Real-Time Microvision (“Kee-Ho”), The Generic Nature of the Smart-Cut® Process for Thin Film Transfer (“Aspar”), and Frontiers of Silicon-on-Insulator (“Celler”). *See, e.g.*, Watanabe at 5:11-26; Park at 4:32-52; Leedy at 9:3-49; Meyer at ¶¶4-22; Srikrishnan at 5:25-45; Wolf 1 at 259-61; Wolf 4 at 537-50; Greenlaw at 3:36-5:60; Sailer at 26-27; Kee-Ho at 834-35; Aspar at 834; Celler at 4960-66. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to incorporate these teachings because, for example, they related to techniques that were known in the prior art and implementing them would have yielded predictable results, including the formation of memory structures and their peripheral devices in a substrate underneath the memory array. The combination also would have improved systems into which the teachings were incorporated by providing benefits, such as more flexible thermal budget during device fabrication allowing separate optimization of the processes for fabricating memory cells and periphery circuitry, greater yield, and improved device quality, and would have been the use of known techniques to improve similar apparatus in the same way.

By way of example only, to the extent that any reference or system/product described in these contentions is found not to disclose the “SOI pillar” limitations of claims 14 and 16 under a construction requiring a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology, it would have been obvious to combine that reference or system/product with, for example, U.S. Patent Appl. Pub. No. 2005/0133851 (“Forbes”), U.S. Patent No. 5,936,274 (“Forbes ’274”), U.S. 6,580,124 (“Cleaves”), U.S. Patent Appl. Pub. No. 2002/0109138 (“Forbes ’138”), U.S. Patent Appl. Pub. No. 2003/0038318 (“Forbes ’318”), The Generic Nature of the Smart-Cut® Process for Thin Film Transfer (“Aspar”), and Frontiers of

Silicon-on-Insulator (“Celler”). *See, e.g.*, Forbes at ¶¶10-20, Forbes ’274 at 4:63-5:3, Cleaves at 2:16-28, Forbes ’138 at ¶¶35-37, Forbes ’318 at ¶¶6-17, Aspar at 837-39, Cellar at 4969-75. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to incorporate these teachings because, for example, they related to techniques that were known in the prior art and implementing them would have yielded predictable results. The combination also would have improved systems into which the teachings were incorporated by providing benefits, such as higher device density and larger memory storage capacity, and would have been the use of known techniques to improve similar apparatus in the same way.

Cited references may relate to additional references and/or products, services, or projects. Cited references may also cite software, hardware, or systems. Intel may rely upon such cited additional references and copies or exemplars of such software, hardware, or systems. Intel will produce or make available for inspection any such cited references, software, hardware, or systems that it intends to rely upon. Intel may also rely upon the disclosures of the references cited and/or discussed during the prosecution of the Asserted Patent and/or the assertions presented regarding those references.

Intel reserves the right to further streamline and reduce the number of anticipation or obviousness references relied upon with respect to a given asserted claim and to exchange or otherwise modify the specific references relied upon for anticipation and within each obviousness combination for each asserted claim. Discovery has just begun, and BeSang has not provided its contentions with respect to claim limitations that are allegedly lacking or not obvious in the prior art.

III. IDENTIFICATION OF PRIOR ART

Each Asserted Claim is invalid at least for lack of novelty under 35 U.S.C. § 102 or obviousness under 35 U.S.C. § 103. Pursuant to N.D. Cal. Patent Local Rule 3-3(a) and (b), Intel identifies below prior art patents, publications, disclosures, uses, sales, and offers for sale that anticipate or render obvious the Asserted Claims under 35 U.S.C. §§ 102 or 103. Pursuant to

Patent Local Rule 3-3(c), Intel attaches claim chart exhibits 1–10 to these Invalidity Contentions identifying exemplary prior art that anticipates or renders obvious each of the Asserted Claims.

For each Asserted Claim that is anticipated or rendered obvious by an exemplary reference or combination, the corresponding claim chart exhibit includes citations to that reference or describes exemplary combinations for each limitation. Where Intel cites to a particular figure in a prior art reference, the citation should be understood to encompass the caption and description of the figure as well as any text relating to the figure in addition to the figure itself. Conversely, where a cited portion of text refers to a figure, the citation should be understood to include the figure as well. Furthermore, while Intel has identified at least one citation per limitation present in a reference or combination, each and every disclosure of the same or similar limitation in the same reference or combination is not necessarily identified. In an effort to focus the issues, Intel cites only portions of identified references, even where a reference or combination may contain additional support for a particular claim element. Thus, Intel may rely on un-cited portions of the prior art references for additional support for a particular element.

Intel may rely upon other prior art identified in future supplements, corroborating references, documentation, products, testimony, or invalidity contentions served by other accused infringers in cases involving the Asserted Patent or patents related thereto, including materials obtained through further investigation and third-party discovery of the prior art identified herein, that demonstrates the invalidating features identified in these Invalidity Contentions or that show the state of the art in the relevant time period (irrespective of whether such references themselves qualify as prior art to the Asserted Patent), and expert testimony to provide context to or aid in understanding the cited portions of the identified prior art.

Additionally, persons of ordinary skill in the art at the time of the alleged invention generally read a prior art reference as a whole and in the context of other publications and literature. Numerous prior art references, including those identified herein and in the attached

exhibits, reflect common knowledge and the state, scope, and content of the prior art before the priority date of the Asserted Claims of the Asserted Patent. Intel may rely on un-cited portions of the prior art references and on other publications and expert testimony to provide context and as aids to understanding and interpreting the portions that are cited. To the extent any limitation is deemed not to be exactly met by an item or combination of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art.

Although Intel's investigation is ongoing, one or more of the Asserted Claims is invalid for failure to comply with 35 U.S.C. § 112. Based upon BeSang's apparent claim interpretations, the Asserted Claims are invalid under 35 U.S.C. § 112 for at least the following reasons: (i) the specification of the Asserted Patent lacks a written description of the claimed inventions in full, clear, concise, and exact terms as required by 35 U.S.C. § 112(1); (ii) the specification of the Asserted Patent lacks an enabling disclosure as required by 35 U.S.C. § 112(1); and (iii) the Asserted Claims are invalid as indefinite under 35 U.S.C. § 112(2) because the claims fail to particularly point out and distinctly claim the subject matter which the applicant regarded as his invention.

In particular, the specification of the Asserted Patent lacks a written description of the alleged invention in full, clear, concise and exact terms as required by 35 U.S.C. § 112(1), and thus fails to provide sufficient information in the original disclosure to show the inventor possessed the invention at the time of the original filing. *See Univ. of Rochester v. Searle & Co.*, 358 F.3d 916, 927–28 (Fed. Cir. 2004). Intel thus contends that one or more of the Asserted Claims are invalid under 35 U.S.C. § 112(1).

Further, the specification of the Asserted Patent lacks an enabling disclosure as required by 35 U.S.C. § 112(1). *See Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 1000 (Fed. Cir. 2008) (holding that the inventors must set forth sufficient information in the specification to enable one

of ordinary skill in the art to make and use the invention without undue experimentation). Intel thus contends that one or more of the Asserted Claims of the Patents-In-Suit are not enabled.

Additionally, United States patent law requires that a patent contain one or more claims “particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.” 35 U.S.C. § 112(2). A claim is considered indefinite, however, if it does not “give notice to the public of the extent of the legal protection offered by the patent, so that interested members of the public, e.g., competitors or the patent owner, can determine whether or not they infringe.” *Default Proof Credit Card Sys. Inc. v. Home Depot U.S.A., Inc.*, 412 F.3d 1291, 1302–03 (Fed. Cir. 2005) (internal quotes and citations omitted). Such a claim is invalid. *See id.*; *Cardiac Pacemakers, Inc. v. St. Jude Med., Inc.*, 296 F.3d 1106, 1114 (Fed. Cir. 2002). Intel thus contends that one or more of the Asserted Claims are invalid for failure to satisfy the definiteness requirement of 35 U.S.C. § 112(2). Intel also notes that its charting of a prior art reference for a claim or limitation that Intel contends is invalid for lack of definiteness in no way represents an admission or concession that the scope of the claim or limitation is definite or ascertainable. A claim fails to claim the subject matter which the applicant regards as his invention where a person of skill in the art would understand the claim to be different from or contrary to the applicant’s invention in light of the specification, the prosecution history, and/or inventor testimony. *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1377–1380 (Fed. Cir. 2000). *See also Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1349 (Fed. Cir. 2002); *Synchronoss Technologies, Inc. v. Dropbox, Inc.*, 987 F.3d 1358, 1366–67 (Fed. Cir. 2021). Like indefiniteness, this failure also renders a claim invalid. *Allen Eng’g*, 299 F.3d 1336, at 1348–49. Intel thus contends that one or more of the Asserted Claims are invalid for failure to satisfy the “regards as his invention” requirement of 35 U.S.C. § 112(2). Intel also notes that its charting of a prior art reference for a claim or limitation that Intel contends is invalid for failing to claim the subject matter which the applicant regards as his invention in no way represents an admission or

concession that the scope of the claim or limitation claims the subject matter which the applicant regards as his invention.

A. Invalidity of the Patents-In-Suit Under 35 U.S.C. §§ 102 and 103

Intel contends that the prior art references and systems/products described in the attached claim chart exhibits anticipate and/or render obvious each Asserted Claim of the Asserted Patent. To the extent that any claim limitation is not anticipated pursuant to 35 U.S.C. § 102, Intel contends that the claimed invention would have been obvious to one of ordinary skill under 35 U.S.C. § 103. Each Asserted Claim would have been obvious in view of each reference or system/product cited in the attached claim chart exhibits either alone or combined with the knowledge that was possessed by one of ordinary skill in the art at the time of the alleged invention. Additionally, each Asserted Claim would have been obvious to one of ordinary skill in the art at the time of the alleged invention in view of the combination of any one of the prior art references or systems/products identified in the attached claim chart exhibits with one or more of the other references or systems/products identified.

Intel identifies the following non-exhaustive list of prior art references that anticipate and/or render obvious each of the Asserted Claims of the Asserted Patent. In the attached claim chart exhibits, Intel also provides exemplary combinations of references and motivations to modify or combine the prior art.

Patents and Patent Applications		
Patent Number	Country of Origin	Date of Issue or Publication
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Publications			
Title	Date of Publication	Author	Publisher
Novel Ultrahigh-Density Flash memory with A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell	2003	Tetsuo Endoh et al.	IEEE
New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology Without Photolithography Process for Tera-Bits and Beyond	4/27/2004	Hiroshi Sakuraba et al.	The Japan Society of Applied Physics
The Generic Nature of the Smart-Cut® Process for Thin Film Transfer	2001	B. Aspar et al.	J. Electronic Materials
ROS: An Extremely High Density Mask ROM Technology Based on Vertical Transistor Cells	1996	E. Bertagnolli	IEEE

Publications			
Title	Date of Publication	Author	Publisher
Frontiers of silicon-on-insulator	5/1/2003	G.K. Celler et al.	American Institute of Physics
Evaluation of a Three-Dimensional Memory Cube System	1993	Claude L. Bertin et al.	IEEE
Fujitsu Designs World's Smallest Chip-Size Module Adopting Advanced System-in-Package Technology	2002	—	Fujitsu
High Density Packaging of Flash Memory	1998	Keith D. Gann	IEEE
Real-Time Microvision System with Three-Dimensional Integration Structure	1996	Kee-Ho Yu et al.	IEEE
Maleville - Multiple SOI Layers by Multiple Smart-Cut Transfers	2000	C. Maleville et al.	IEEE
Silicon Processing for the VLSI Era, vol. 1, 2d Ed.	2000	Stanley Wolf et al.	Lattice Press
Silicon Processing for the VLSI Era, vol. 4, 2d Ed.	2002	S. Wolf	Lattice Press
Vertical p-i-n Polysilicon Diode With Antifuse for Stackable Field-Programmable ROM	5/2004	S.B. Herner	IEEE
Creating 3D Circuits Using Transferred Films	1997	Philip M. Sailer et al.	IEEE
Three-Dimensional Shared Memory Fabricated Using Wafer Stacking Technology	2000	K.W. Lee et al.	IEEE
512Mb PROM with 8 Layers of Antifuse/Diode Cells	2003	M. Crowley et al.	IEEE
Intel StrataFlash Wireless Memory System (LV18/LV30 SCSP)	2003	—	Intel Corporation

To the extent BeSang disputes whether any of these references disclosed particular limitations of the Asserted Claims of the Asserted Patent or would have been combined by a person of ordinary skill in the art at the time of the alleged invention to render any limitation obvious, Intel reserves the right to supplement these Invalidity Contentions to identify additional

combinations, motivations to modify or combine, or explanations for particular references with additional particularity.

Additionally, certain systems/products constitute prior art to the Asserted Patent because they were on sale, publicly known, and/or publicly used prior to the alleged invention date of the Asserted Patent. For example, based on Intel's investigations to date, Intel believes that at least the following systems may alone, or in combination with other prior art, render the Asserted Claims invalid.

Sale, Public Use, or Public Knowledge		
Item	Date(s) of Offer, Sale, or Use	Entity Who Sold Item or Made Item Publicly Known or Used
Matrix Semiconductor 3D PROM	2003 ²	Matrix Semiconductor
Intel StrataFlash Wireless Memory System (LV18/LV30 SCSP) and related Stacked Chip Scale Package products	2003	Intel Corporation

For example, under BeSang's sweeping apparent construction of the limitation "the stackable add-on layer being bonded to the dielectric layer," the vertical stacking of memory arrays in the Intel StrataFlash Wireless Memory System (LV18/LV30 SCSP) and related Stacked Chip Scale Package products rendered obvious that limitation. *See, e.g.*, Intel StrataFlash Wireless Memory System (LV18/LV30 SCSP) Datasheet (98100DOC00002689-98100DOC00002742).

References cited in claim chart exhibits describing or relating to a prior art system/product should be understood to disclose the system/product's capabilities generally and examples of specific deployments of the system/product for specific customers. Those references also demonstrate how each system/product is prior art at least because it was made, publicly used, offered for sale, sold, or otherwise made available to the public at least as early as the dates of those references, and is evidence that the inventions contained in the identified prior art

² *See, e.g.*, 98100DOC00006792.

system/product were conceived of and reduced to practice with diligence, thereby demonstrating prior invention under 35 U.S.C. § 102(g). To the extent the references describe various implementations of the same underlying system/product, that underlying system/product is a single piece of prior art under 35 U.S.C. § 102. Each claim chart exhibit provided for a prior art system/product should be understood to incorporate by reference printed publications describing or relating to that prior art system/product and all claim chart exhibits provided for those printed publications. In addition, each of the printed publications itself qualifies as prior art on separate grounds as a publication under 35 U.S.C. §§ 102(a) and/or 102(b). Furthermore, it would have been obvious to combine the features described in each prior art reference relating to the same system/product.

Intel cites exemplary evidence providing BeSang with notice of the nature of prior art systems/products and Intel's contentions regarding how these systems/products relate to the Asserted Claims. Intel reserves the right to rely on additional evidence to further prove the nature of these systems/products and to demonstrate the operation of such systems/products. As this case is in its preliminary stages, Intel's investigation into the prior art, including the prior art systems/products identified above, has just begun. Intel is continuing its investigation into these products and related companies. Intel reserves the right to supplement these Invalidity Contentions to provide additional claim charts with regard to these products/systems and to identify additional references, combinations, motivations to modify or combine, or explanations relating to particular references as discovery progresses.

Intel attaches the following invalidity claim chart exhibits.

Ex.	Reference or System/Product
1	U.S. Patent Application Publication No. 2002/0028541A1 ("Lee")
2	Lee in view of U.S. Patent Appl. Publ. No. 2002/0154556, U.S. Patent Appl. Publ. No. 2003/0157748, and/or "The Generic Nature of the Smart-Cut® Process for Thin Film Transfer"
3	U.S. Patent No. 6,034,882

Ex.	Reference or System/Product
4	U.S. Patent No. 6,525,953
5	U.S. Patent No. 5,091,762
6	Novel Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell
7	U.S. Pat. No. 8,791,581
8	U.S. Patent Application Publication No. 2005/0112846
9	Chinese Pat. No. CN 1099695C
10	Matrix Semiconductor 3D PROM

BeSang has identified, and Intel is aware of, no evidence of any indicia of non-obviousness, including any long-felt but unsolved need; copying; failure of others; commercial success due to the patented invention; industry praise; unexpected results; industry skepticism; or licensing. To the extent BeSang identifies any such evidence, Intel reserves the right to respond.

B. Invalidity of the Asserted Patent Based on 35 U.S.C. § 112

Subject to Intel's reservation of rights, Intel provides below an identification of Asserted Claims along with an identification of the specific limitations that are invalid pursuant to 35 U.S.C. § 112 as indefinite, failing to claim the subject matter which the applicant regards as his invention, lacking enablement, and/or lacking written description. Intel's contentions are based on its present understanding of the Asserted Claims and BeSang's apparent construction of those claims in its Infringement Contentions, unless otherwise indicated. By asserting grounds for invalidity based on BeSang's apparent claim construction or any other particular claim construction, Intel is not adopting BeSang's claim construction, nor admitting to the accuracy of any particular claim construction. Intel's contentions that the following claims are invalid under 35 U.S.C. § 112 are made in the alternative, and do not constitute, and should not be interpreted as, admissions that any of the Asserted Claims are not anticipated or rendered obvious by any prior art. Intel reserves the right to supplement these contentions to further identify bases for invalidity under 35 U.S.C. § 112 after subsequent case events, including the Court's claim construction order and BeSang's disclosure of any amended or supplemental infringement

contentions in this action. In addition, Intel's investigation is ongoing, as is discovery in this action. Intel may accordingly supplement these contentions to further identify bases for invalidity under 35 U.S.C. § 112 as additional information becomes available.

1. Written Description and Enablement (§ 112(1))

Intel contends that the Asserted Claims of the '702 patent are invalid for failing to satisfy the written description and/or enablement requirements due to at least the following claim language or limitations:

- “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells” (claim 13);
- “the stackable add-on layer being bonded to the dielectric layer” (claim 13);
- “wherein the memory cells are nonvolatile memory cells having at least one transistor” (claim 13);
- “a vertical transistor having a floating gate and a control gate on a SOI pillar” (claim 14);
- “formed with a first SOI pillar” (claim 16).

2. Indefiniteness (§ 112(2))

Intel contends that the Asserted Claims of the '702 patent are invalid for failing to satisfy the definiteness requirement of 35 U.S.C. § 112, paragraph 2 with respect to at least the following claim language or limitations:

- “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells” (claim 13);
- “the stackable add-on layer being bonded to the dielectric layer” (claim 13);
- “wherein the memory cells are nonvolatile memory cells having at least one transistor” (claim 13);
- “on a SOI pillar” (claim 14);
- “formed with a first SOI pillar” (claim 16).

3. Subject Matter Regarded as the Invention (§ 112(2))

Intel contends that the Asserted Claims of the '702 patent are invalid for failing to claim the subject matter which the applicant regards as his invention, as required by 35 U.S.C. § 112, paragraph 2 with respect to at least the following claim language or limitations:

- “a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells” (claim 13);
- “the stackable add-on layer being bonded to the dielectric layer” (claim 13).
- “a vertical transistor having a floating gate and a control gate on a SOI pillar” (claim 14);
- “formed with a first SOI pillar” (claim 16).

IV. DOCUMENT PRODUCTION

Pursuant to Patent Local Rule 3-4, Intel has produced the following under separate cover and identifies below by production number which documents correspond to each category:

N.D. Cal. Patent Local Rule	Category of Documents	Production Number
3-4(a)	Source code, specifications, schematics, flow charts, artwork, formulas, or other documentation sufficient to show the operation of any aspects or elements of an Accused Instrumentality identified by the patent claimant in its Patent L.R. 3-1(c) chart.	98100DOC00006796 - 98100DOC00020650 Additionally, Intel has made Manufacturing Process Information for the accused products available for inspection at Perkins Coie’s Dallas office. BeSang outside counsel will be able to review these materials once a supplemental protective order regarding Manufacturing Process Information has been entered by the Court.
3-4(b)	A copy or sample of the prior art identified pursuant to Patent L.R. 3-3(a) which does not appear in the file history of the patent(s) at issue.	98100DOC00002511 - 98100DOC00006792

3-4(c)	All agreements that the party opposing infringement contends may be comparable to a license that would result from a hypothetical reasonable royalty negotiation.	98100DOC00020651 - 98100DOC00020927 Intel also identifies the following agreements: September 26, 2013 Patent Assignment Agreement between Intel Corporation and IBM Corporation, September 27, 2012 Patent License Agreement between Intel Corporation and KAIST-IP Co., Ltd , and December 5, 2011 Patent License Agreement between Intel Corporation and the Foundation for Advancement of International Science. These agreements will be produced pursuant to the protective order as soon as issues concerning notice and consent to production by third parties to those agreements have been resolved.
3-4(d)	Documents sufficient to show the sales, revenue, cost, and profits for accused instrumentalities identified pursuant to Patent L.R. 3-1(b) for any period of alleged infringement.	98100DOC00006793 - 98100DOC00006795
3-4(e)	All agreements that may be used to support the party denying infringement's damages case.	98100DOC00020651 – 98100DOC00020927 Intel also identifies the following agreements: September 26, 2013 Patent Assignment Agreement between Intel Corporation and IBM Corporation, September 27, 2012 Patent License Agreement between Intel Corporation and KAIST-IP Co., Ltd , and December 5, 2011 Patent License Agreement between Intel Corporation and the Foundation for Advancement of International Science. These agreements will be produced pursuant to the protective order as soon as issues concerning notice and consent to production by third parties to those agreements have been resolved.

DATED: July 14, 2023.

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I hereby certify that I served the foregoing **INTEL CORPORATION'S INVALIDITY**

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to be sent by the following indicated method or methods, on the date set forth below:

- ☐ by sending via the court's electronic filing system
☒ by email
☐ by mail
☐ by hand delivery

DATED: July 14, 2023

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