

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
Petitioner,

v.

BESANG INC.,
Patent Owner.

IPR2023-00991
Patent 7,378,702 B2

Before JON B. TORNQUIST, KIMBERLY McGRAW, and
ELIZABETH M. ROESEL, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. *Background and Summary*

Intel Corporation (“Petitioner”) filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1 and 13–17 of U.S. Patent No. 7,378,702 B2 (Ex. 1001, “the ’702 patent”). BeSang Inc. (“Patent Owner”) filed a Preliminary Response to the Petition. Paper 6 (“Prelim. Resp.”). With authorization, Petitioner subsequently filed a reply to the Preliminary Response (Paper 7, “Prelim. Reply”) to which Patent Owner filed a Sur-reply (Paper 8, “Prelim. Sur-reply”).

We have authority to determine whether to institute an *inter partes* review. 35 U.S.C. § 314 (2018); 37 C.F.R. § 42.4(a) (2023). The standard for institution is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted “unless the Director determines . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”

For the reasons set forth below, Petitioner demonstrates a reasonable likelihood of prevailing with respect to at least one claim of the ’702 patent. Accordingly, we institute an *inter partes* review.

B. *Real Parties in Interest*

Petitioner identifies itself as the real party in interest and Patent Owner identifies itself as the real party in interest. Pet. 93; Paper 4, 1.

C. *Related Matters*

The parties identify the following district court proceedings as related matters: *BeSang Inc. v. Micron Tech., Inc.*, No. 2:23-cv-00028 (E.D. Tex.) (“Texas litigation”) and *BeSang Inc. v. Intel Corp.*, No. 3:23-cv-00113 (D. Or.) (“Oregon litigation”). Pet. 94; Paper 4, 1. The parties also note that the ’702 patent is currently being challenged in IPR2023-00900. Pet. 93;

Paper 4, 1; *Micron Tech., Inc. v. Besang Inc.*, IPR2023-00900, Paper 9 (PTAB Nov. 17, 2023).

D. The '702 Patent

The '702 patent is titled “Vertical Memory Device Structures,” and issued May 27, 2008, from an application filed September 3, 2004, which is a continuation-in-part of an application filed June 21, 2004. Ex. 1001, codes (22), (45), (54), (63).

The '702 patent explains that “integrated circuits contain transistors that are primarily implemented on a single major surface of a substrate, such as a semiconductor wafer.” *Id.* at 1:27–30. “These laterally oriented devices,” however, “consume significant amounts of chip area.” *Id.* at 1:30–31. The '702 patent explains that one method of reducing the lateral area consumed by the transistors was to reduce the lateral dimensions of the transistors and interconnects, but the equipment and technology needed to support the manufacture of such chips “becomes increasingly expensive with each new generation of smaller devices.” *Id.* at 1:31–39. To resolve this problem, the '702 patent discloses the use of “a plurality of vertically oriented semiconductor memory devices, or cells,” that may be added to a separately fabricated substrate that includes electrical devices and/or interconnect lines. *Id.* at 1:40–50.

Figure 1 of the '702 patent is reproduced below:

Fig. 1

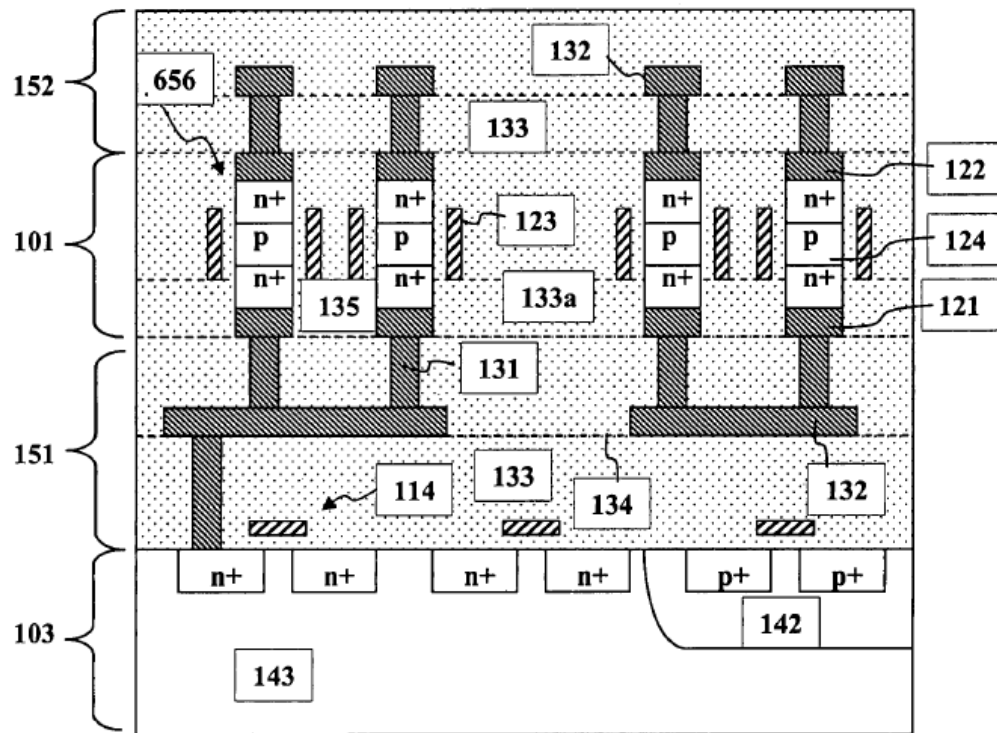


Figure 1 is a cross-sectional view of an embodiment that includes a base semiconductor substrate and add-on vertical memory devices. *Id.* at 2:13–15. As shown in Figure 1, vertical memory devices 656 are separated by isolation 135 and have floating structures in the filled dielectric materials 133a. *Id.* at 5:18–21. These vertical memory devices are referred to in the '702 patent as floating devices (FLD). *Id.* at 5:21–22. Inter-layer dielectric (ILD) layers 133 are disposed above and below FLD layer 101. *Id.* at 5:29–32. Interconnect lines 132 and vias 131 connect FLDs directly or indirectly within an FLD layer, or to another FLD layer or to a base substrate. *Id.* at 5:32–36.

In the embodiment shown in Figure 1, base substrate 103 is bonded to lower dielectric layer 151. *Id.* at 5:37–38. Dashed line 134 denotes a border, or interface, between two ILD layers. *Id.* at 5:43–44. The first ILD layer 151 has interconnections and vias, and base substrate 103 shares these interconnections and vias with first FLD layer 101. *Id.* at 5:44–47. The bottom of the FLD layer is connected to metal layer 121, which is also directly connected to vias 131 in ILD layer 151, thereby forming a preformed electrode and contact. *Id.* at 6:35–38. The top of the FLD layer may be connected to metal layer 122, which is also directly connected to vias 131 in ILD layer 152. *Id.* at 6:38–40. The ’702 patent notes that multiple FLD layers can be stacked, thereby increasing the effective device density. *Id.* at 6:41–42; *see also id* at 5:38–41, 5:47–50 (disclosing a “second FLD layer” not shown in Figure 1).

E. Illustrative Claim

Petitioner challenges claims 1 and 13–17 of the ’702 patent. Pet. 1. Claim 13, reproduced below, is illustrative of the challenged claims:

13. A semiconductor memory structure, comprising:
 - [a] a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;
 - [b] a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and
 - [c] the stackable add-on layer being bonded to the dielectric layer; and
 - [d] wherein the memory cells are nonvolatile memory cells having at least one transistor.

Ex. 1001, 12:24–34 (paragraph identifications [a]–[d] are added to align with the parties’ arguments); Pet. vi (claims listing).

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1 and 13–17 of the '702 patent would have been unpatentable on the following grounds (Pet. 3):

Ground	Claim(s) Challenged	35 U.S.C. §¹	Reference(s)/Basis
1A	13–17	103	Lee ²
1B	16, 17	103	Lee, Endoh ³
1C	13–17	103	Lee, Kim ⁴
1D	16, 17	103	Lee, Kim, Endoh
1E	13–17	103	Lee, Aspar ⁵
1F	16, 17	103	Lee, Aspar, Endoh
2A	13	103	Johnson ⁶
2B	13	103	Johnson, Kim
2C	13	103	Johnson, Aspar
3	1	103	Park ⁷ , Kim

In support of its ground of unpatentability, Petitioner relies upon the declaration of Dr. Carl Sechen. Ex. 1003.

¹ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. The '702 patent issued May 27, 2008. Ex. 1001, code (45). Accordingly, on this record, we apply the pre-AIA version of § 103. See 35 U.S.C. § 100(i)(1)(B).

² US 2002/0028541 A1, published March 7, 2002. Ex. 1007 (“Lee”).

³ US 2002/0154556 A1, filed March 28, 2002, and published October 24, 2002. Ex. 1012 (“Endoh”).

⁴ US 2003/0157748 A1, published August 21, 2003. Ex. 1008 (“Kim”).

⁵ Aspar, et. al., *The Generic Nature of the Smart-Cut® Process for Thin Film Transfer*, 30 J. Elec. Materials, 834–840 (2001). Ex. 1009 (“Aspar”).

⁶ US 6,034,882, issued March 7, 2000. Ex. 1010 (“Johnson”).

⁷ US 5,571,730, issued November 5, 1996. Ex. 1011 (“Park”).

II. ANALYSIS

A. *Claim Construction*

In this proceeding, the claims of the '702 patent are construed “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). Under that standard, the words of a claim are generally given their “ordinary and customary meaning,” which is the meaning the term would have had to a person of ordinary skill at the time of the invention, in the context of the entire patent including the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc).

Petitioner contends that the terms “stackable add-on layer . . . the stackable add-on layer [is]/[being] bonded” and “SOI pillar” require construction. Pet. 10–16. Patent Owner contends claim construction is not necessary to deny the Petition and, for purposes of this Decision, the Board may take Petitioner’s claim construction “representations at face value.” Prelim. Resp. 14–15.

Upon review of the parties’ arguments and the evidence of record, we determine that only the terms “stackable add-on layer . . . the stackable add-on layer [is]/[being] bonded” and “SOI pillar” require discussion. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.”)).

1. “*stackable add-on layer*”

Claim 1 requires “a first stackable add-on layer” that “is bonded to a layer of the substrate.” Ex. 1001, 10:52–53, 10:58–59. Claim 13 requires “a

stackable add-on layer” “being bonded to the dielectric layer.” *Id.* at 12:29–32. Petitioner contends that based on the plain language of the claim “a stackable add-on layer” “must be its own structure capable of being stacked and added onto the other recited structures.” Pet. 10 (citing Ex. 1003 ¶ 71). Petitioner analogizes the claimed memory structure to a layer cake in which each layer is baked individually and then stacked on top of each other to form the final product. *Id.* at 10–11.

Petitioner contends the intrinsic record supports this understanding. *Id.* at 11. According to Petitioner, the ’702 patent describes a Silicon-on-Insulator (“SOI”) layer as “a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer,” and explains that such an SOI layer may be thought of as a “stackable add-on structure.” *Id.* (quoting Ex. 1001, 4:48–57).

Patent Owner does not address this portion of Petitioner’s proposed construction, but Petitioner contends Patent Owner’s district court complaint appears to interpret this claim to encompass “any type of layer that is directly or indirectly adhered to the recited layer of the substrate.” *Id.* at 12 (citing Ex. 1013), 29.

On this preliminary record, we agree with Petitioner that the term “stackable add-on layer” requires something more than just any type of layer that is directly or indirectly adhered to the substrate or dielectric layer. First, the plain language of the claim does not require merely a “layer” having a plurality of vertically oriented semiconductor memory cells, but rather “a stackable add-on layer.” Ex. 1001, 12:29–32.

Second, the written description of the ’702 patent strongly suggests that a “stackable add-on layer” is formed separately from the substrate and then stacked on and bonded to the substrate or a dielectric layer above the

substrate. For example, the written description of the '702 patent explains that in the invention “a plurality of vertically oriented semiconductor memory devices, or cells, may be *added to a separately fabricated substrate* that includes electrical devices and/or interconnect lines.” *Id.* at 1:47–50 (emphasis added). Likewise, the specification explains that an SOI layer refers to “a relatively thin, single crystal portion of a semiconductor wafer that can be cleaved and bonded to another previously fabricated wafer, or similar type of substrate.” *Id.* at 4:47–51. “In this context,” the '702 patent explains, “the SOI layer may be thought of as an attachment layer, or stackable add-on structure which is suitable for bonding to a semiconductor substrate already containing devices and/or interconnections.” *Id.* at 4:53–57. Again, this suggests that a “stackable add-on layer” is separately formed and then bonded to a previously fabricated substrate.

Given the structure of the claims and the description of the invention in the written description of the '702 patent, we preliminarily construe “stackable add-on layer” to be a layer that is formed separately from the substrate and then bonded to the substrate or a dielectric layer above the substrate. We do not understand a “stackable add-on layer” to include memory cells that are formed by sequential deposition on or above a substrate or dielectric layer without being added to a separately formed substrate.

2. “*the stackable add-on layer [is]/[being] bonded*”

Petitioner also contends that the “the stackable add-on layer [is]/[being] bonded” portion of the claim term requires that the “stackable

add-on layer” is “wafer bonded⁸ to the recited layer of the substrate.”

Pet. 12. Petitioner asserts that wafer bonding was well known by 2004, and various wafer bonding methods are cited in U.S. Patent No. 7,052,941 (Ex. 1005), which is incorporated by reference in its entirety in the ’702 patent. *Id.* at 4, 11 (citing Ex. 1001, 1:7–10; Ex. 1003 ¶42). Petitioner also directs our attention to the ’702 patent’s disclosed method of constructing an SOI layer on a separate wafer substrate and then bonding this layer to a previously fabricated wafer that already contains devices and/or interconnections. *Id.* at 11 (citing Ex. 1001, 4:48–57). According to Petitioner, one of ordinary skill in the art would have understood that the ’702 patent’s description of its “SOI layer” requires wafer bonding. *Id.*

Independent claims 1 and 13 do not specify how the stackable add-on layer is bonded to the dielectric layer. Nor does Petitioner assert that the plain and ordinary meaning of “bonding” refers to “wafer bonding.” Thus, to limit the claims to wafer bonding, Petitioner must identify a clear expression of intent in the ’702 patent to define “bonding” as “wafer bonding,” or a clear disavowal of claim scope demonstrating that non-wafer bonding methods are outside the reach of the claims. *See Thorner v. Sony Comp. Entm’t Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). Petitioner does not contend that the patentee acted as its own lexicographer by defining “bonding” as “wafer bonding,” a term that does not even appear in the ’702 patent. *Id.* at 1365. Nor are we directed to any clear disavowal indicating that methods of bonding other than “wafer bonding” are outside the scope of the claims. *Id.* at 1366. Thus, we decline to construe “bonded” in claims 1

⁸ Wafer bonding is a method in which semiconductor layers are formed on separate wafers and then bonded together to create a stacked semiconductor structure. Ex. 1003 ¶41.

and 13 to require wafer bonding. *See Thorner*, 669 F.3d at 1365–66 (noting that the standards for lexicography and disavowal are “exacting”).

As noted by Petitioner, the ’702 patent describes an SOI layer that is wafer bonded to a previously fabricated substrate. Ex. 1001, 4:47–53. Independent claims 1 and 13, however, do not require an SOI layer, and the disclosure of a single embodiment in which wafer bonding is used is not sufficient to import such a limitation into the claims. *See Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1354 (Fed. Cir. 2012) (“While claim terms are understood in light of the specification, a claim construction must not import limitations from the specification into the claims.”); *Computer Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1374 (Fed. Cir. 2008) (“Nonetheless, this court will not countenance the importation of claim limitations from a few specification statements or figures into the claims.”).

In summary, we preliminarily construe “stackable add-on layer . . . the first stackable add-on layer is/being bonded” to require a separate layer that is formed apart from the substrate and then subsequently bonded to the substrate or a dielectric layer above the substrate.⁹ We do not construe independent claims 1 or 13 to require any particular form or method of bonding.¹⁰

⁹ This construction is preliminary. The parties are encouraged to provide formal constructions of this term during trial and to support such constructions with citations to the claims, specification, and, if relevant, the prosecution history.

¹⁰ On this record, it is unclear what methods beyond wafer bonding would allow for a “stackable add-on layer.” Absent express reasons for doing so, however, we decline to exclude methods beyond “wafer bonding” from the scope of claims 1 and 13.

3. “*SOI pillar*”

Petitioner contends the term “SOI pillar” in claims 14–17 “requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology.” Pet. 13. Petitioner provides intrinsic record support for its proposed construction. Pet. 13–5. Petitioner further contends that, to the extent Patent Owner contends an “SOI pillar” “encompasses any pillar-shaped structure with insulating material below it,” such a construction would read out the term “SOI” from the claims. *Id.* Patent Owner does not address the proper construction of “SOI pillar,” but contends that for purposes of this decision the Board may take Petitioner’s “representations at face value.” Prelim. Resp. 14. As such, for purposes of this decision and based on the intrinsic evidence provided by Petitioner, we apply Petitioner’s proposed construction of “SOI pillar.”

B. *General Plastic*

Patent Owner contends we should exercise discretion under § 314(a) to deny the Petition because a prior petition was filed against the ’702 patent by a different petitioner in IPR2023-00900. Prelim. Resp. 15–23. In *General Plastic Industries Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 15–16 (PTAB Sept. 6, 2017) (precedential), the Board articulated a non-exhaustive list of factors to be considered in determining whether to exercise discretion under § 314(a) to deny a petition that challenges the same patent as a previous petition. These factors are

1. whether the same petitioner previously filed a petition directed to the same claims of the same patent;
2. whether at the time of filing of the first petition the petitioner knew of the prior art asserted in the second petition or should have known of it;
3. whether at the time of filing of the second petition the petitioner already received the patent owner’s preliminary response to the

- first petition or received the Board’s decision on whether to institute review in the first petition;
4. the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition;
 5. whether the petitioner provides adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent;
 6. the finite resources of the Board; and
 7. the requirement under 35 U.S.C. § 316(a)(11) to issue a final determination not later than 1 year after the date on which the Director notices institution of review.

Id. at 16.

1. *Factor 1*

Under the first *General Plastic* factor, we consider “whether the same petitioner previously filed a petition directed to the same claims of the same patent.” *General Plastic*, Paper 19 at 16. Petitioner has not previously filed a petition directed to the challenged claims of the ’702 patent. Pet. 92. Patent Owner contends, however, that Micron Technologies (“Micron”) previously challenged the ’702 patent in IPR2023-00900, roughly one month before the Petition was filed, and Petitioner and Micron “plainly have a relationship that supports denial” under factor 1. Prelim. Resp. 16. In support of its argument, Patent Owner asserts that Petitioner and Micron jointly developed the same 3D NAND memory technology accused of infringement in the parallel litigation, are both are defendants in co-pending litigation related to the ’702 patent, and have an identical interest in avoiding liability for infringement. *Id.*

In analyzing factor 1, we must consider the relationship between the multiple petitioners challenging a patent. *Valve Corp. v. Electronics Scripting Products, Inc.*, IPR2019-00062, Paper 11 at 9 (PTAB Apr. 2, 2019) (precedential). In *Valve*, the two petitioners were co-defendants in the

same district court litigation, were accused of infringing the same patent based on the same product that incorporated technology licensed from Valve, and Valve employees provided technical assistance during the development of the accused devices. *Id.* at 9–10. Accordingly, the Board found (1) that there was a “significant relationship” between the two petitioners with respect to the patent owner’s assertion of infringement in the district court, and (2) that *General Plastic* factor 1 favored denial of institution. *Id.* at 10.

The evidence of record demonstrates that Petitioner and Micron jointly developed the 3D NAND technology that is generally at issue in the district court litigation, and the parties have acknowledged “their long-term joint development partnership” for this technology. Ex. 1013 (district court complaint); Ex. 2010 (“Micron and Intel Extend their Leadership in 3D NAND Flash memory.”); Ex. 2016 (discussing the end of Intel’s and Micron’s NAND partnership). There is no assertion, however, that *all* 3D NAND technology infringes the challenged claims of the ’702 patent, and Micron and Intel are not accused of infringing the ’702 patent based on the same products and are not co-defendants in any district court litigation. Further, Patent Owner presents no persuasive evidence that the two parties collaborated on the development of either of the accused products, as opposed to general 3D NAND technology, and Petitioner represents that the two parties filed their petitions independently and without coordination or cooperation. Prelim. Reply 1–2; Ex. 2016, 1 (noting that each company sought to independently develop 3D NAND technology in order to “forge” their own path for future NAND development and “better optimize the technology and products for their individual business needs”).

In view of the foregoing, we determine there is no significant relationship between Petitioner and Micron, and Petitioner is not the same petitioner as the petitioner in IPR2023-00900. Thus, *General Plastic* factor 1 weighs against discretionary denial.

2. *Factor 3*

Under the third *General Plastic* factor, we consider whether, at the time the second petition was filed, the petitioner already received the patent owner's preliminary response to the first petition or the Board's decision on whether to institute review. *General Plastic*, Paper 19 at 16.

Petitioner contends that it filed its Petition well before the preliminary response was filed in the Micron case. Prelim. Reply 5.

Patent Owner does not assert that, at the time the second petition was filed, Petitioner had already received the patent owner's preliminary response in the Micron case, much less a decision on whether to institute review. Rather, Patent Owner contends that the similarities in arguments between the Micron petition and the present Petition show that Petitioner plainly benefitted from Micron's earlier petition, which provided it with a strategic advantage. Prelim. Resp. 20.

Given that the Petition was filed before the preliminary response in the Micron case, and well before any decision on whether to institute review, *General Plastic* factor 3 weighs against discretionary denial. *General Plastic*, Paper 19 at 17 (noting that "factor 3 is directed to Petitioner's potential benefit from receiving and having the opportunity to study Patent Owner's Preliminary Response, as well as our institution decision on the first-filed petitions, prior to its filing of follow-on petitions").

3. *Factors 2, 4, and 5*

General Plastic factors 2, 4, and 5 are used “to assess and weigh whether a petitioner should have or could have raised new challenges earlier.” *General Plastic*, Paper 19 at 18. These factors are generally applicable when the same Petitioner, or two parties with a sufficiently close relationship, file multiple petitions against the same patent. *Id.* at 16, 18. Petitioner has not filed more than one petition against the ’702 patent and, as we discuss above, we determine that there is not a sufficient relationship between the two parties to attribute Micron’s petition to Petitioner. Thus, the relevance of *General Plastic* factors 2, 4, and 5 in this case is diminished. In any event, Petitioner diligently filed its Petition nearly eight months before the statutory deadline and only one month after the petition in IPR2023-00900 was filed. Prelim. Reply 5. Such diligent action counsels against denial under *General Plastic* factors 2, 4, and 5.

4. *Factors 6 and 7*

General Plastic factors 6 and 7 address the finite resources of the board (factor 6) and the requirement to issue a final written decision within one year of the institution decision (factor 7). *General Plastic*, Paper 19 at 16.

We determine that the finite resources of the Board are not implicated in this case because Petitioner and Micron do not have a sufficiently close relationship with respect to the products accused of infringement in the Oregon or Texas litigations. We further determine that the requirement to issue a final written decision within one year of the institution decision is not implicated in this case, nor is the general concern for potential abuse caused by multiple, staggered petitions discussed in *General Plastic*. *See General Plastic*, Paper 19 at 17.

5. *Summary*

Upon review of the parties' evidence and arguments, we determine that the *General Plastic* factors do not favor discretionary denial.

C. *Fintiv*

Under 35 U.S.C. § 314(a) we have discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016). Patent Owner contends we should discretionarily deny institution under § 314(a) in view of the Texas and Oregon litigations. Prelim. Resp. 23.

We consider several factors when determining whether to deny institution under § 314(a) based on a parallel district court proceeding, specifically

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) (“Fintiv”). We also consider “several clarifications” made by the Director of the United States Patent and Trademark Office (“USPTO”). See USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District

Court Litigation, 2 (June 21, 2022), available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf (“Director’s Memo”).

1. *Factor 1 – Whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted*

Under the first *Fintiv* factor, we consider “whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted.” *Fintiv*, Paper 11 at 6. Patent Owner contends factor 1 is neutral because Petitioner has not filed a motion to stay the Oregon litigation and the district court has not stayed the case pending a decision on whether to institute *inter partes* review in this proceeding. Prelim. Resp. 23–24. Patent Owner further contends that the district court in the Texas litigation has not ruled on Micron’s opposed stay motion. *Id.* at 24.

On October 10, 2023, and after reply and sur-reply briefing concluded in this case, the district court in the Oregon litigation denied Petitioner’s motion to extend a temporary stay of deadlines until such time as a decision on whether to institute review is rendered in this proceeding. Ex. 2022. This order, however, does not clearly indicate whether a stay might be granted if *inter partes* review is instituted in this proceeding. *Id.* at 4. As such, we determine that *Fintiv* factor 1 is neutral.

2. *Factor 2 – The proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision*

Under the second *Fintiv* factor, we consider the “proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision.” *Fintiv*, Paper 11 at 6. Petitioner contends that no trial

date has been set in the Oregon litigation and “the average time to trial in the District of Oregon is 46.3 months.” Pet. 92 (citing Ex. 1030).

Patent Owner contends Petitioner overlooks the fact that the co-pending Micron litigation in Texas will undoubtedly go to trial first. Prelim. Resp. 24. According to Patent Owner, “[t]his earlier trial date tips factor 2 in favor of discretionary denial.” *Id.*

No trial date has been set in the Oregon litigation and the estimated time to trial is well after the projected statutory deadline for a final written decision in this case. Pet. Reply 2; Ex. 1030; *see also* Ex. 2022, 5 (district court order requiring the parties to file a proposed case schedule through claim construction). As such, this factor does not favor discretionary denial. *Fintiv*, Paper 11 at 3 (noting that in the case where the district court has set a trial date after the Board’s deadline to issue a final written decision, “the Board may be less likely to deny institution”), 9 (explaining that when the court’s trial date is “significantly after” the projected statutory deadline for issuing a final written decision, “the decision whether to institute will likely implicate other factors discussed herein, such as the resources that have been invested in the parallel proceeding”) (footnote omitted).

As noted by Patent Owner, the Texas litigation is likely to go to trial before any final written decision in this case. Prelim. Resp. 24. Given the stipulations discussed below for *Fintiv* factor 4, however, the Texas litigation is unlikely to address all (or a majority of) the issues raised in the Petition. Moreover, Petitioner is not a party to the Texas litigation. As such, the Texas litigation trial date does not tip *Fintiv* factor 2 in favor of discretionary denial. *See Dolby Laboratories, Inc. v. Intertrust Techs Corp.*, IPR2020-01123, 2021 WL 54756 (PTAB Jan. 6, 2021) (addressing *Fintiv* factors 2 and 5 together).

3. *Factor 3 – Investment in the parallel proceeding by the court and the parties*

Under the third *Fintiv* factor, we consider the “investment in the parallel proceeding by the court and the parties.” *Fintiv*, Paper 11 at 6. Patent Owner contends that by the time of an institution decision the parties in the Oregon litigation will have exchanged infringement and invalidity contentions, and the parties in the Texas litigation will have exchanged infringement and invalidity contentions, with discovery and depositions underway. Prelim. Resp. 25.

The investment in the Oregon and Texas litigations is minimal. No substantive rulings relating to invalidity have been issued by either district court and the parties are at the early stages of discovery. Prelim. Resp. 25; IPR2023-00900, Exhibit 2001; Ex. 2022, 2 (discussing the status of the Oregon litigation). As such, we determine that *Fintiv* factor 3 weighs against discretionary denial.

4. *Factor 4 – Overlap between issues raised in the petition and in the parallel proceeding*

Under the fourth *Fintiv* factor, we consider the “overlap between issues raised in the petition and in the parallel proceeding.” *Fintiv*, Paper 11 at 6. In both the Texas litigation and the Oregon litigation, the petitioners have submitted stipulations not to pursue certain issues and/or grounds before the district court. In the Texas litigation, the petitioner stipulates that it will not pursue “any obviousness ground that includes the primary references in [the] Petition,” i.e., Lee¹¹ and Watanabe. IPR2023-00900, Exhibit 1031. In the Oregon litigation, Petitioner stipulates that

¹¹ In IPR2023-00900, the petitioner relies on U.S. Patent No. 6,881,994 B2 to Lee. IPR2023-00900, Exhibit 1007. In this proceeding, Petitioner relies

if the PTAB institutes an *inter partes* review (“IPR”) proceeding for the ’702 patent on the grounds presented in Intel’s petition in IPR2023-00991, and so long as the PTAB does not vacate its institution decision or otherwise terminate the instituted IPR, Intel will not pursue an invalidity defense in this lawsuit that the patent claims subject to the instituted IPR are invalid based on grounds that were raised or reasonably could have been raised during the IPR.

Ex. 1034. 2.

The stipulation filed in the Texas litigation mitigates, to an extent, concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB.¹² Director’s Memo at 7. Similarly, Petitioner’s stipulation in the Oregon litigation (i.e., that it will not pursue an invalidity defense that the claims challenged in this IPR proceeding are invalid based on grounds that were raised or reasonably could have been raised during the IPR) also mitigates concerns of potentially conflicting decisions and duplicative efforts.

Patent Owner contends Petitioner’s stipulation falls short of a *Sotera* stipulation by carving out any circumstance that “otherwise terminate[s] the instituted IPR.” Prelim. Sur-reply 2–3. Patent Owner interprets this carve-

on the patent application publication of the Lee patent. Ex. 1007. Because the disclosures of the Lee patent and patent application publication are substantively identical, we consider the stipulation not to pursue any obviousness ground based on Lee to apply with equal force to Lee’s patent application publication.

¹² The stipulation in the Texas litigation bars the defendant from pursuing “any obviousness ground that includes” Lee or Watanabe. IPR2023-00900, Exhibit 1031. Here, Petitioner’s grounds 1A–1F challenge claims 13–17 based in whole or in part on Lee, and grounds 2A–2C and 3 challenge claims 1 and 13 based on combinations of references that do not include Lee or Watanabe. Pet. 3. As such, the grounds to be resolved by the PTAB will differ somewhat from those presented in the Texas litigation.

out to mean the stipulation will not take effect until the Board issues a final written decision, thereby rendering the stipulation an “empty promise” as the district court in the Texas litigation will undoubtedly resolve validity before a final written decision in this case. *Id.* at 3. We disagree. We do not understand Petitioner’s stipulation to require that a final written decision be issued before the stipulation takes effect. Rather, so long as an *inter partes* review is instituted, and until such time as the IPR is terminated or vacated, Petitioner will not pursue any invalidity defense before the district court that is “based on grounds that were raised or could have been raised during the IPR.” Ex. 1034.

In summary, given the stipulations filed by the petitioners in the Oregon and Texas litigations, it appears that there will be minimal, if any, overlap between the issues raised in the petitions and in the parallel district court proceedings. Accordingly, *Fintiv* factor 4 weighs against discretionary denial.

5. *Factor 5 – Whether the petitioner and the defendant in the parallel proceeding are the same party*

Under the fifth *Fintiv* factor, we consider “whether the petitioner and the defendant in the parallel proceeding are the same party.” *Fintiv*, Paper 11 at 6. Petitioner contends it is a defendant in the Oregon litigation but is not involved in the Texas litigation. Prelim. Reply 3.

Patent Owner contends Petitioner is a defendant in the Oregon litigation and is closely related to the defendant in the Texas litigation. Prelim. Resp. 27.

Because the trial in the Oregon litigation is currently set to occur after the issuance of a final written decision in this case, Petitioner’s status as a defendant in the Oregon litigation does not support discretionary denial.

See, Samsung Electronics Co., Ltd. v. Mypaq Holdings Ltd., IPR2022-00307, Paper 10 at 13 (PTAB May 23, 2022). Moreover, Petitioner is not the defendant in the Texas litigation. Accordingly, *Fintiv* factor 5 is, at best, neutral.

6. *Factor 6 – Other circumstances that impact the Board’s exercise of discretion, including the merits*

Under the sixth *Fintiv* factor, we consider “other circumstances that impact the Board’s exercise of discretion, including the merits.” *Fintiv*, Paper 11 at 6. Petitioner contends this factor weighs against discretionary denial as its recited grounds “present compelling merits.” Prelim. Reply 4. Patent Owner contends Petitioner’s “patentability challenge is deeply flawed” and “fails to show obviousness for any ground.” Prelim. Resp. 27.

The Director’s Memo instructed “PTAB panels to only consider compelling merits if they first determined that *Fintiv* factors 1–5 favored a discretionary denial.” *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 4–5 (PTAB Feb. 27, 2023) (decision on Director review) (precedential). On review of *Fintiv* factors 1–5, as a whole, we determine that the lack of a trial date in the Oregon litigation, the stipulations filed in both the Oregon and Texas litigations, and the lack of investment by the district courts and parties in the Oregon and Texas litigations all weigh against exercising our discretion under § 314(a). The remaining *Fintiv* factors are, at best, neutral. Thus, *Fintiv* factors 1–5 do not favor discretionary denial, and we do not reach the compelling merits analysis of *Fintiv* factor 6.

7. *Summary*

For the reasons discussed above, upon a holistic review of the *Fintiv* factors, we determine that the circumstances presented do not warrant

exercising our discretion under § 314(a) to deny institution of an *inter partes* review.

D. Claims 13–17 over Lee (Ground 1A)

Petitioner contends the subject matter of claims 13–17 would have been obvious over the disclosures of Lee. Pet. 16–41.

1. Lee

Lee is titled “Dense Arrays and Charge Storage Devices, and Methods for Making Same” and published March 7, 2002. Ex. 1007, codes (43), (54).

Lee aims to reduce the cost of memory and logic devices by increasing device density. *Id.* ¶ 106. Lee states it achieves these objectives by providing “a monolithic three dimensional array of charge storage devices comprising a plurality of device levels.” *Id.* ¶ 107. In this context “monolithic” means that the layers of each level of the array are directly deposited on the layers of each underlying level of the array. *Id.* This is in contrast to two-dimensional arrays, which “may be formed separately and then packaged together to form a non-monolithic memory device.” *Id.*

Figure 35 is reproduced below:

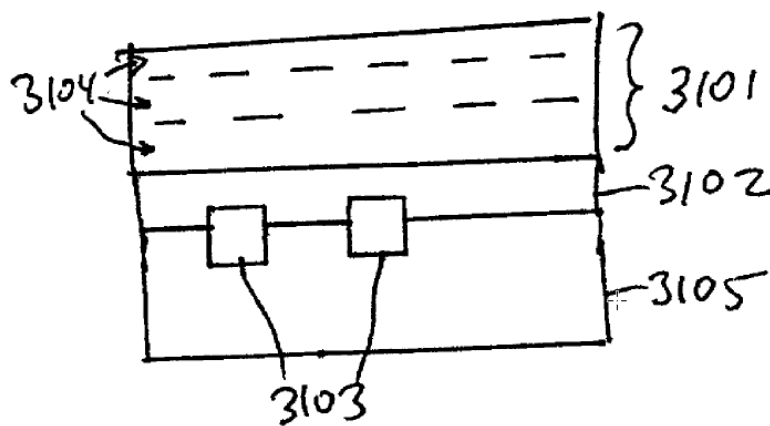


FIGURE 35

Figure 35 is a schematic of a three-dimensional array of devices. *Id.* ¶ 60. In the device of Figure 35, driver circuits 3103 are disposed in monocrystalline substrate 3105 as CMOS or other transistors, and interlayer insulating layer 3102 is then disposed on monocrystalline substrate 3105. *Id.* ¶ 111. Charge storage logic or memory devices 3101 have a plurality of device levels 3104 that are preferably separated by interlayer insulating layers. *Id.*

Lee explains that “[t]he charge storage devices of the array may be any type of semiconductor devices which store charge, such as EPROMs or EEPROMs.” *Id.* ¶ 113. Such charge storage devices may be formed in various configurations, “such as a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, a rail stack TFT EEPROM, and various other configurations.” *Id.*

Figure 1A of Lee is reproduced below:

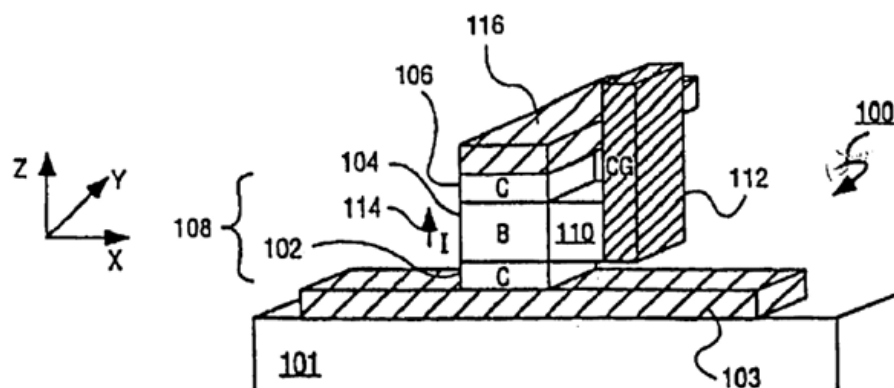


FIG. 1A

Figure 1A is an illustration of a pillar memory. *Id.* ¶ 38. In Figure 1, “[p]illar memory device 100 includes a first contact region 102 formed on a first input/output (I/O) 103 conductor formed on or above a plane (x-y) of a single crystal substrate 101.” *Id.* ¶ 122. Semiconductor body 104 is formed directly on first contact region 102 and a second contact region 106 is

formed on body 104. *Id.* A second I/O region 116 is formed on second contact region 106. *Id.* Lee explains that first contact region 102, body 104, and the second contact region 106 are each vertically aligned to form a pillar 108. *Id.* “Adjacent to and in contact with body 104 is a charge storage medium 110,” with control gate 112 formed adjacent to and in direct contact with charge storage medium 110. *Id.*

Lee explains that:

The programmed and unprogrammed state of the pillar memory device is determined by whether or not charge is stored in charge storage medium 110. The charge stored in the charge storage medium adds or subtracts from the voltage applied to the control gate, thereby altering the voltage required to form a conducting channel in body 104 to enable a current (e.g., read current I_R) to flow between the first and second contact (source/drain) regions.

Id. ¶ 123.

Figure 2 is reproduced below:

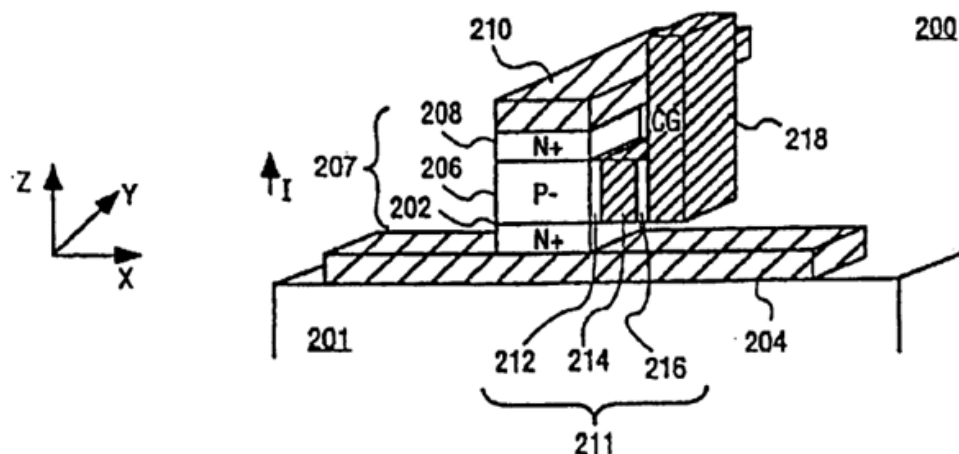


FIG. 2

Figure 2 is an illustration of a pillar memory. *Id.* ¶ 41. In this embodiment, pillar 207 includes a first source/drain contact region 202 comprising a

heavily doped N⁺ silicon film that is formed on a first input/output 204 (e.g. bit line) that is formed on or above a substrate 201. *Id.* ¶ 126. Body 206 is composed of a lightly doped P- type silicon film 206 that is formed on and in direct contact with N⁺ source/drain contact region 202. *Id.* Second drain region 208 is composed of a heavily doped N⁺ silicon film and is formed on and in direct contact with P type silicon film 206. *Id.* “A second conductive input/output (e.g. word line/bit line) 210 is formed on the second N⁺ source/drain region 208.” *Id.* Charge storage medium 211 comprises a tunnel dielectric 212, floating gate 214, and control gate dielectric 216. *Id.* ¶ 127. Control gate 218 is formed adjacent to, and in direct contact with, control gate dielectric 216. *Id.* “Control gate 218 is formed of a conductor such as but not limited to doped silicon or a metal such as tungsten.” *Id.*

Figure 9A is reproduced below:

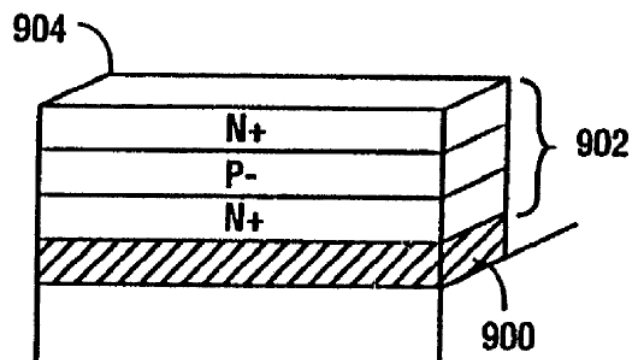


FIG. 9A

Figure 9A illustrates a method of forming a pillar utilizing an intersection etch technique. *Id.* ¶ 48. In Figure 9A, first I/O conductor 900 is blanket deposited, “followed by the sequential blanket deposition of the film stack 902 (e.g., N⁺/P⁻/N⁺) of the desired pillar.” *Id.* ¶ 141. “The first I/O film

900 and the pillar film stack 902 are then etched to form a plurality of pillar strips 904 as shown in Fig. 9a.” *Id.* Pillar strips 904 may then be etched to form individual pillars with associated I/O films. *Id.*

2. *Analysis – Claim 13*

Petitioner contends Lee discloses every limitation of independent claim 13. Pet. 16–31. With respect to claim 13[a], Petitioner contends that Figure 35 of Lee discloses a substrate 3105 having driver circuits 3103 disposed therein. *Id.* at 18 (citing Ex. 1007 ¶¶ 110–111). Petitioner further contends that Figure 35 discloses interlayer insulating layer 3102 that is above substrate 3105 and driver circuits 3103. *Id.* at 19–20 (citing Ex. 1007 ¶ 111; Ex. 1003 ¶ 118). With respect to claim 13[b] and 13[c], Petitioner asserts that, if Patent Owner argues that a “stackable add-on layer” encompasses any type of layer that is directly or indirectly adhered to the “dielectric layer,” then bottom-most level 3104 in Figure 35 teaches the limitations of claim 13[b] and 13[c]. *Id.* at 20–27, 29–30. With respect to claim 13[d], Petitioner contends that one of ordinary skill in the art would have understood that the memory cells depicted in Figures 1A–1B, 2, 7, and 25A, are all nonvolatile memory cells. *Id.* at 30–31 (citing Ex. 1007 ¶¶ 6, 113, 122, 125; Ex. 1003 ¶ 139).

On this record, we preliminary adopt Petitioner’s construction of “stackable add-on layer,” which Petitioner does not assert is disclosed in Lee under its proposed construction. That is, Petitioner does not assert that Lee’s method of direct deposition of each layer of its array would result in a “stackable add on layer” under its construction of that term. As such, Petitioner does not demonstrate a reasonable likelihood that claim 13 would have been obvious based on Lee alone. Prelim. Resp. 32–33 (Patent Owner

asserting that we should not institute on grounds based only on Lee because Petitioner does not agree that claim 13 reads upon Lee's disclosures).

3. *Analysis – Claims 14–17*

Claims 14–17 each depend, directly or indirectly, from claim 13. Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to claim 13. Accordingly, Petitioner does not demonstrate a reasonable likelihood that claims 14–17 would have been obvious over Lee.

E. *Claims 16 and 17 over Lee and Endoh (Ground 1B)*

Petitioner contends "Lee and Endoh teach claims 16 and 17's additional limitations under [Patent Owner's] apparent interpretation of 'SOI pillar.'" Pet. 41–42. On this record, we preliminarily adopt Petitioner's construction of "SOI pillar," and not Patent Owner's apparent interpretation upon which this ground depends. Moreover, claims 16 and 17 depend from claim 13 and Petitioner's arguments with respect to these claims do not remedy the deficiencies noted above with respect to claim 13. As such, Petitioner does not demonstrate a reasonable likelihood that claims 16 and 17 would have been obvious based on Lee and Endoh.

F. *Claims 13–17 over Lee and Kim (Ground 1C)*

Petitioner contends that claims 13–17 would have been obvious over the combined disclosures of Lee and Kim, under Petitioner's construction of "stackable add-on layer." Pet. 50–54.

1. *Kim*

Kim discloses a "process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimum metal bonding areas." Ex. 1008 ¶ 1. Kim notes that as integrated circuit (IC) technology progresses, there is a desire for a

“system on a chip” in which the functionality of all the IC devices of the system are packaged together without a conventional printed circuit board. *Id.* ¶ 4. “In practice, however, it is very difficult to implement a truly high-performance ‘system on a chip’ because of vastly different fabrication processes and different manufacturing yields for the logic and memory circuits.” *Id.*

Kim explains that one known method of vertically stacking wafers was three-dimensional (3D) wafer-to-wafer vertical stack technology, in which multiple layers of active IC devices, such as processors, programmable devices and memory devices, are vertically stacked inside a single chip. *Id.* ¶ 7. A major challenge to such methods “is the bonding between wafers and between die in a single chip.” *Id.* ¶ 8. For example, in one prior art method, polymer glue may be required to bond the vertically stacked wafers. *Id.* In another prior art method, copper may be used to bond the vertically stacked wafers. *Id.* One drawback to this second method is that a carrier wafer is required to transport thinly stacked wafers, and a polymer glue is used to affix the carrier wafer on the top wafer during the vertically stacked wafer processing. *Id.* According to Kim, there existed a need “for a simpler but more efficient process of vertically stacking multiple wafers supporting different active IC devices on a single die with low cost and high via density with optimal metal bonding areas.” *Id.*

Figure 1 of Kim is reproduced below:

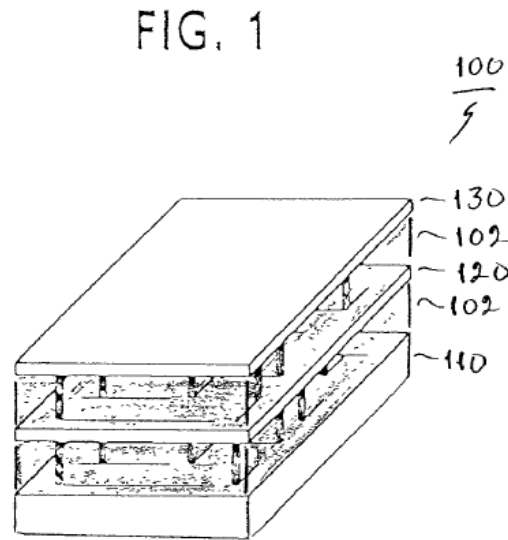


Figure 1 “illustrates an example three-dimensional (3-D) wafer-to-wafer vertical stack forming a single chip.” *Id.* ¶ 10. In Figure 1, 3-D vertical stack (chip) 100 may comprise any number of active device polysilicon (Si) wafers, such as wafers #1 (110), #2 (120), and #3 (130). *Id.* ¶ 20. Wafer #1 may include, for example, one or more microprocessors; wafer #2 may include one or more memory devices; and wafer #3 may include one or more radiofrequency (RF) or optical communication devices. *Id.* Kim notes that the disclosed invention is “applicable for use with all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, MOS transistors, CMOS devices, MOSFETs, and new memory devices and communication devices.” *Id.* ¶ 19.

Kim notes that, “[t]ypically, a dielectric layer 102 is used to bond the active device wafers 110, 120 and 130.” *Id.* ¶ 20. However, a “metal to metal” bond can also be used to stack wafers 110, 120, and 130 to form vertical stack 100. *Id.* ¶ 21. “This metal to metal bond method may serve not only as electrical connections to active IC devices on the vertically

stacked wafers 110, 120, and 130 . . . but also [to] bond adjacent wafers 110, 120, and 130.” *Id.*

Kim explains that a “2-wafers vertical stack” may also be formed according to the process of the invention. *Id.* ¶ 22, Fig. 2. This “vertical stack can effectively integrate diverse process technologies on a single wafer process, such as, for example, logic/memory stacking, processor stacking, optical interconnect, system-on-chip, and RF interconnect.” *Id.*

2. Analysis – Claim 13

With respect to claims 13[a] and [b], Petitioner contends that Lee discloses these limitations for the same reasons discussed above with respect to obviousness based on Lee alone. Pet. 50. With respect to claim 13[c], Petitioner contends that Kim discloses a method of forming a three-dimensional (3-D) wafer-to-wafer vertical stack that is applicable for use with “all types of semiconductor wafers and integrated circuit (IC) devices, including, for example, . . . CMOS devices, MOSFETs, and new memory devices.” *Id.* at 51 (citing Ex. 1008 ¶¶ 19–20). Petitioner further contends that Kim teaches that the vertical stack may comprise “any number” of wafers, including a wafer with one or more microprocessors and a wafer including one or more memory devices, and that dielectric layer 102 may be used to separate and bond the wafers. *Id.* (citing Ex. 1008 ¶¶ 20, 22, Fig. 1).

With respect to the reason to combine Lee and Kim, Petitioner contends that Lee discloses that each level 3104 is deposited on the underlying level of array 3101, but “does not clearly describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102.” *Id.* (citing Ex. 1007 ¶¶ 107–113). Consequently, Petitioner contends that one of ordinary skill in the art would have looked to other art, such as Kim, for details about attaching bottom level 3104 to insulating layer 3102. *Id.* This

is “especially so,” according to Petitioner, where a person of ordinary skill in the art, “at the suggestion of Lee, was looking to separately form a two-dimensional array of memory devices and ‘package [it] together’ with Lee’s substrate 3105 having driver circuits 3103 formed therein and insulating layer 3102 on top ‘to form a non-monolithic memory device.’” *Id.* at 51–52 (citing Ex. 1003 ¶¶ 190–192; Ex. 1007 ¶ 107); *see also id.* at 52 (asserting that Kim contemplates bonding a wafer having CMOS devices, like Lee’s substrate 3105, with a wafer having memory devices, like Lee’s level 3104).

Petitioner asserts that a person of ordinary skill in the art would have recognized that using wafer-bonding to bond level 3104 to insulating layer 3102 would constitute “nothing more than using a known technique (Kim’s wafer bonding) to improve a similar device (the structure in Lee’s Figure 35) in the same way (logic/memory stacking using a wafer bonding process).” *Id.* at 53. Petitioner further asserts that using Kim’s method of wafer bonding to bond level 3104 to insulating layer 3102 “would have amounted to applying a known technique (Kim’s wafer bonding) to address the same known problem recognized by both Lee and Kim (fabricating 3D memory arrays above a substrate containing electrical devices) using prior art elements according to their established functions (Kim’s wafer bonding and Lee’s memory cell structures in Figures 1A–B, 2, 7, or 25A in Lee’s Figure 35 structure).” *Id.* (citing Ex. 1003 ¶ 195; *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023); *KSR*, 550 U.S. at 417).

Petitioner also asserts that a person of ordinary skill in the art would have understood that wafer-bonding Lee’s bottom level 3104 to insulating layer 3102 would allow for more efficient quality control with less potential waste, as compared to monolithic deposition. *Id.* at 53–54. Petitioner reasons that using a wafer-bonding method would allow quality control (e.g.,

testing for shorts) to be performed on stacked memory cells one at a time and, “[i]f a quality issue is detected, then only that level 3104 would need to be discarded, whereas with deposition, the whole underlying structure (e.g., substrate with electrical devices, any previously-deposited stacks, etc.) would need to be discarded.” *Id.* at 54 (citing Ex. 1003 ¶ 196).

Patent Owner contends Petitioner’s reasons for combining Lee and Kim are inaccurate. Prelim. Resp. 34. First, Patent Owner contends that Lee in fact discloses how level 3104 is formed on insulating layer 3102, i.e., through direct deposition to form a monolithic array. *Id.* at 34–35 (citing Ex. 1007 ¶ 107). Second, Patent Owner contends that Lee does not suggest forming a two-dimensional array, as asserted by Petitioner, but instead expresses a clear preference for a monolithic array. *Id.* at 36–37 (“Lee presented separately formed two-dimensional arrays as a contrast against the preferred monolithic three-dimensional arrays of the invention.”). And, according to Patent Owner, Petitioner “does not explain why one of ordinary skill in the art relying upon Lee’s disclosure would choose a less dense and more costly configuration than the one actually recommended by Lee.” *Id.* at 37–38. Third, Patent Owner contends that Petitioner does not explain how Kim’s wafer bonding would “improve” Lee’s monolithic three-dimensional array depicted in Figure 35, “which Lee itself taught is more dense and less costly” than a non-monolithic array. *Id.* at 38 (citing Ex. 1007 ¶¶ 106–107). Finally, Patent Owner contends Petitioner’s alleged motivation of quality control simply “explains a way to improve yield in the manufacture of non-monolithic stacked wafers[,] [i]t **does not** provide a reason to use non-monolithic stacked wafers as compared to monolithic three-dimensional arrays.” *Id.* at 39.

We agree with Patent Owner on several points. For example, contrary to Petitioner’s arguments (Pet. 34–35), Lee appears to explain how the bottom level 3104 of array 3101 is formed and bonded to dielectric layer 3102, i.e., through direct deposition on the dielectric layer. Ex. 1007 ¶¶ 107, 122. Also, Lee does not appear to advocate for stacking two-dimensional arrays, but rather contrasts this method with its potentially more efficient monolithic arrays. *Id.* ¶ 107 (teaching that device density is improved by providing “a monolithic three dimensional array of charge storage devices comprising a plurality of device levels”). Petitioner also does not appear to adequately explain how Kim’s known method of wafer bonding would “improve” Lee’s device. Pet. 53.

Petitioner provides other explanations, however, as to why one of ordinary skill in the art would have implemented Kim’s method of wafer bonding to bond level 3104 of Lee to insulating layer 3102 (as shown in Figure 35). First, Petitioner contends that wafer-bonding Lee’s bottom level 3104 to insulating layer 3102 would minimize waste resulting from electrical defects. Pet. 53–54; Ex. 1016, 1:30–37 (noting that the yield for silicon-on-insulator wafers is typically 70% and by stacking two wafers the maximum yield achievable is therefore 49%). Patent Owner disagrees, asserting the benefit identified by Petitioner merely provides a way to improve yield in non-monolithic arrays, and does not provide a reason to use stacked wafers as compared to a monolithic array. *Id.* We determine that Petitioner’s asserted benefit is adequate for purposes of institution.

Petitioner asserts that using Kim’s wafer bonding method to construct Lee’s memory cells would have provided the ability to individually test each layer before it is added to the stack, thereby reducing waste. Pet. 53–54. We agree with Patent Owner that Dr. Sechen does not compare

yields for monolithic three-dimensional arrays to yields for non-monolithic stacked wafers. Prelim. Resp. 39. Nevertheless, there remains a fact issue as to whether Petitioner’s asserted benefit would have outweighed the competing benefits of improved density and lowered costs of monolithic arrays identified in Lee (Ex. 1007 ¶¶ 106–107). This issue is best resolved on a complete trial record. *See Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 795–796 (Fed. Cir. 2021) (noting that the presence of “simultaneous advantages and disadvantages” does not necessarily obviate motivation to combine, and that the relative advantages and disadvantages must be weighted to determine if the identified disadvantages outweigh “any reason to combine”); *Arctic Cat Inc. v. Polaris Indus., Inc.*, 795 F. App’x 827, 833 (Fed. Cir. 2019) (“The Board must weigh the benefits and drawbacks of the modification against each other, to determine whether there would be a motivation to combine.”); *see also In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004) (noting that “a particular combination” need not be the preferred, or the most desirable, combination described in the prior art in order to provide motivation to combine).

Second, the parties’ contentions present a fact issue as to whether fabricating Lee’s vertical memory structure using Kim’s wafer bonding method would have amounted to nothing more than applying a known technique to address a known problem using prior art elements according to their established functions, as Petitioner contends (Pet. 53), or whether the combination would not have been viewed as an improvement of Lee’s monolithic three-dimensional arrays, as Patent Owner contends (Prelim. Resp. 38–39). *See KSR*, 550 U.S. at 417 (“[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.”); *see also id.* at 416 (“when a patent claims a

structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result.”).

In view of the foregoing, we determine that Petitioner sufficiently identifies where Lee and Kim disclose each limitation of claim 13 and provides a rationale for combining the prior art disclosures that is sufficient to meet the reasonable likelihood standard at the institution stage.

3. *Analysis - Claims 14–17*

Claims 14–17 each require an “SOI pillar.” Ex. 1001, 12:35–52. Petitioner contends that if Patent Owner argues that an “SOI pillar” “encompasses any pillar-shaped structure with insulating material below it,” then Lee discloses or suggests the subject matter of claims 14–17. Pet. 31–41 (contentions based on Lee alone), 54 (relying on the same contentions for combination of Lee and Kim as presented for Lee alone).

Patent Owner contends Petitioner’s arguments do not support institution because they are based on a claim construction Petitioner does not agree with. Prelim. Resp. 31.

Petitioner’s arguments in this ground are based on a claim construction Petitioner does not support and we do not adopt. As such, Petitioner does not demonstrate a reasonable likelihood that claims 14–17 would have been obvious over Lee and Kim.

G. *Claims 16–17 over Lee, Kim, and Endoh (Ground 1D)*

Petitioner contends that, to the extent Patent Owner’s apparent construction of “SOI pillar” is adopted, the subject matter of claims 16–17 would have been obvious over the combined disclosures of Lee, Kim, and Endoh. Pet. 55.

Patent Owner contends Petitioner's arguments with respect to this ground do not support institution because they are based on a construction of "SOI pillar" that Petitioner does not agree with. Prelim. Resp. 31.

Petitioner's arguments in this ground are based on a claim construction Petitioner does not support and we do not adopt. As such, Petitioner does not demonstrate a reasonable likelihood that claims 16–17 would have been obvious over Lee, Kim, and Endoh.

H. Claims 13–17 over Lee and Aspar (Ground 1E)

1. Aspar

Aspar is an article published in the Journal of Electronic Materials and is titled *The Generic Nature of the Smart-Cut® Process for Thin Film Transfer*. Ex. 1009. Aspar explains that the Smart-Cut process "is based on ion implantation and wafer bonding." *Id.* at 834. Aspar notes that ion implantation induces formation of an in-depth weakened layer that leads to delamination of a thin film from a thick substrate. *Id.* Wafer bonding and layer transfer then enable different materials to be associated to form multilayer substrates. *Id.* According to Aspar, the Smart-Cut process was "first developed to obtain silicon-on-insulator (SOI) materials," and is now "an industrial process which provides high quality materials in large quantities." *Id.*

Figure 1 of Aspar is reproduced below:

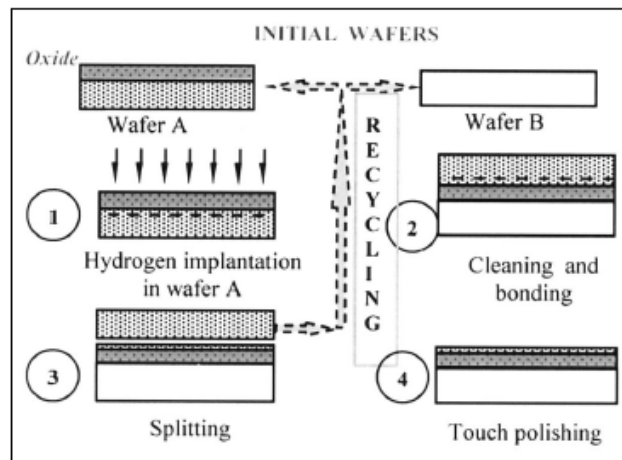
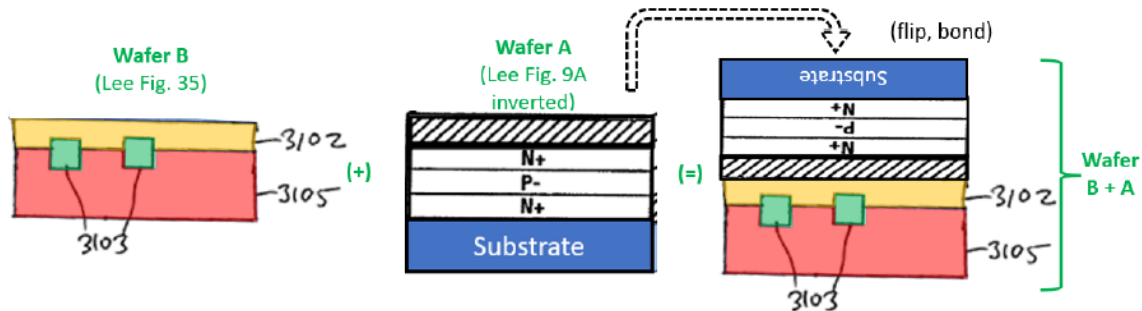


Figure 1 is a “[s]chematic description of the Smart-Cut® process, used to obtain SOI wafers.” *Id.* at 835. The process for obtaining an SOI wafer begins with hydrogen implantation in substrate A, which induces formation of an in-depth weakened layer. *Id.* at 834. Substrate A is then bonded to a support B by wafer bonding. A splitting step is then performed, allowing the transfer of a thin layer from substrate A onto support B. *Id.* A final treatment may then be performed to remove the rough surface left after splitting. *Id.*

2. Analysis – Claim 13

Petitioner contends that Lee and Aspar disclose the limitations of claims 13[a] and [b] for the same reasons discussed above with respect to the ground based on Lee alone. Pet. 56. With respect to limitation 13[c], Petitioner contends that Aspar discloses “transferring SOI layer stacks already formed onto a single substrate or a SOI wafer,” and one of ordinary skill in the art would have sought to use this method to wafer bond bottom level 3104 (“stackable add-on layer”) in Lee’s Figure 35 to insulating layer 3102 (“dielectric layer”). *Id.* at 56–58. Petitioner provides the following illustration of its proposed combination:



The illustration above is Petitioner’s depiction of the combination of Wafer B (a portion of Figure 35 of Lee) and Wafer A (Figure 9A of Lee (inverted and applied to a substrate)) to form a combined Wafer B + A. *Id.* at 59. As shown in the above figure, Petitioner contends that one of ordinary skill in the art would have formed the substrate and dielectric layer of Figure 35 of Lee and then wafer bonded the substrate and device layer of Figure 9A of Lee to this substrate. *Id.* Then, the substrate (blue) would be removed and individual memory cells in level 3104 fabricated from the transferred thin layer in the same way they are fabricated in Lee. *Id.* at 60.

Petitioner contends one of ordinary skill in the art would have been motivated to make such a combination for several reasons. First, Petitioner contends that Aspar itself teaches that the disclosed Smart-Cut process allows the formation of multiple SOI layers stacks and that this process was known to have several advantages, including “transferring thin layers of very good thickness homogeneity and with a high crystalline quality.” *Id.* at 60–61 (quoting Ex. 1003 ¶ 212; Ex. 1009, 834).

Petitioner also contends that the proposed combination would constitute using a “known technique (Aspar’s Smart-Cut® process) to address the same known problem recognized by both Lee and Aspar (fabricating 3D structures) using prior art elements according to their established functions (Aspar’s Smart-Cut® process and Lee’s Figure 35

memory device using the memory structures of Figure 1A–1B, 2, 7, or 25A).” *Id.* at 61 (also asserting that the combination of Lee and Aspar would have constituted the combination of a known technique, to improve a similar known device, in the same way). Petitioner also contends that use of Aspar’s process as compared to monolithic deposition would allow “for more efficient quality control at the layer formation stage.” *Id.* (citing Ex. 1003 ¶ 213). In particular, Petitioner contends that quality control can be performed on each stack prior to bonding, allowing defective stacks to be discarded as opposed to the entire structure. *Id.* at 61–62.

Patent Owner generally repeats its arguments discussed above with respect to Kim. Prelim. Resp. 33–39. In particular, Patent Owner argues that there is no evidence that Aspar’s system would “improve” Lee’s monolithic device, and quality control for non-monolithic devices (the proposed device of Lee and Aspar) does not provide a reason to switch from Lee’s monolithic structure to a stacked structure. Prelim. Resp. 38–39.

After considering the parties’ arguments and evidence, we determine that Petitioner’s asserted quality control benefit and *KSR*-based rationales provide a sufficient basis on which to institute review, and the parties’ contentions present factual issues that are best resolved on a full record after trial.

3. *Analysis – Claims 14–17*

Petitioner contends that Lee discloses the elements of claims 14–17, relying on the same contentions for the combination of Lee and Aspar as Petitioner presents for Lee alone. Pet. 63. In addition, Petitioner contends that Aspar discloses using its Smart-Cut process to form SOI wafers, which constitute a doped stackable add-on layer that is bonded to Wafer B to form pillars (“SOI pillars”). *Id.*

Patent Owner does not address Petitioner's arguments with respect to claims 14–17 over Lee and Aspar, apart from its motivation to combine arguments with respect to independent claim 13. Prelim. Resp. 33–39.

On this record, it is unclear whether Petitioner's arguments for claims 14–17 are based on its proposed construction for “SOI pillar” or on a claim construction Petitioner does not support and we do not adopt. In addition, Petitioner does not appear to explain how the combination of Lee and Aspar would have resulted in an “SOI pillar” under Petitioner's construction for that term.

I. Claims 16–17 over Lee, Aspar, and Endoh (Ground 1F)

Petitioner contends that the subject matter of claims 16 and 17 would have been obvious over the combined disclosures of Lee, Aspar, and Endoh based on Petitioner's proposed claim constructions. Pet. 64. Petitioner argues that one of ordinary skill in the art would have “found it obvious to form a suitable doped stack of the stackable add-on layer added using SOI technology to form SOI pillars with two memory cells as taught in Endoh for the same reasons described” in earlier sections of the Petition addressing Lee in combination with Aspar and Lee in combination with Endoh. *Id.*

Patent Owner contends this ground fails because, for the reasons discussed above, Petitioner fails to demonstrate that one of ordinary skill in the art would have combined Lee and Aspar. Prelim. Resp. 33.

On this record, we are concerned that Petitioner's cross-reference to other sections of the Petition may not be sufficient to support a challenge based on Lee, Aspar, and Endoh. *See In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (holding that petitioner's burden of demonstrating obviousness is not met by a conclusory argument that “the

same analysis” for one combination of references applies to a different combination of references).

J. Claim 13 over Johnson (Ground 2A)

Petitioner contends the subject matter of claim 13 would have been obvious over the disclosures of Johnson. Pet. 65–73.

1. Johnson

Johnson is titled “Vertically Stacked Field Programmable Nonvolatile Memory and Method of Fabrication,” and issued March 7, 2000. Ex. 1010, codes (45), (54).

Johnson discloses a “very high density field programmable memory” that includes an array that “is formed vertically above a substrate using several layers, each layer of which includes vertically fabricated memory cells.” *Id.* at code (57). The fabrication process for the memory cells of Johnson is schematically illustrated in Figures 6(b)–6(g). *Id.* at 12:42–43. Figure 6(b) is reproduced below:

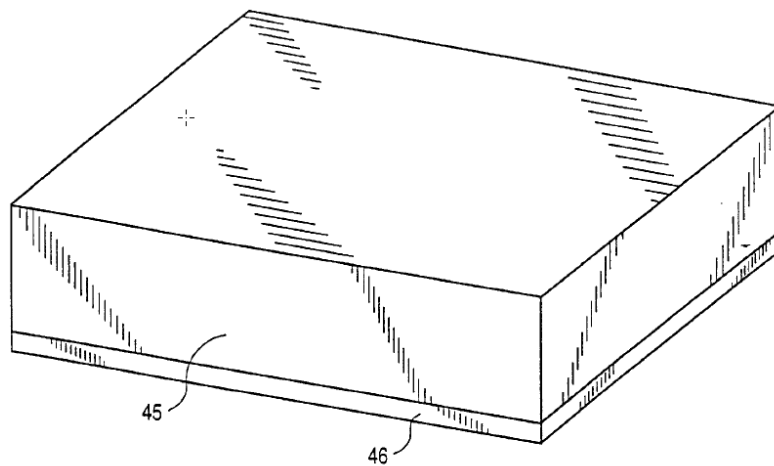


FIG. 6(b)

Figure 6(b) is a perspective view of a conductor layer and layer stack used in the fabrication of a memory cell. *Id.* at 4:38–39. Johnson explains that fabrication of the memory cell begins with a wafer that may have CMOS transistors for the peripheral circuitry fabricated in the monocrystalline substrate. *Id.* at 13:26–29. An insulator is then deposited and, preferably, planarized. *Id.* at 13:30–33. Neither of these steps or structures are depicted in Figure 6(b). *Id.* at 13:35–36. Then, first conductor layer 46 and layer stack 45 are sequentially deposited. *Id.* at 13:32–35. Next, a mask that defines the features of the conductor layer is applied and these features are etched into both pillar layer stack 45 and first conductor layer 46. *Id.* at 13:37–39. An insulator is then deposited on the wafer and planarized. *Id.* at 13:39–40.

Figure 6(c) is reproduced below:

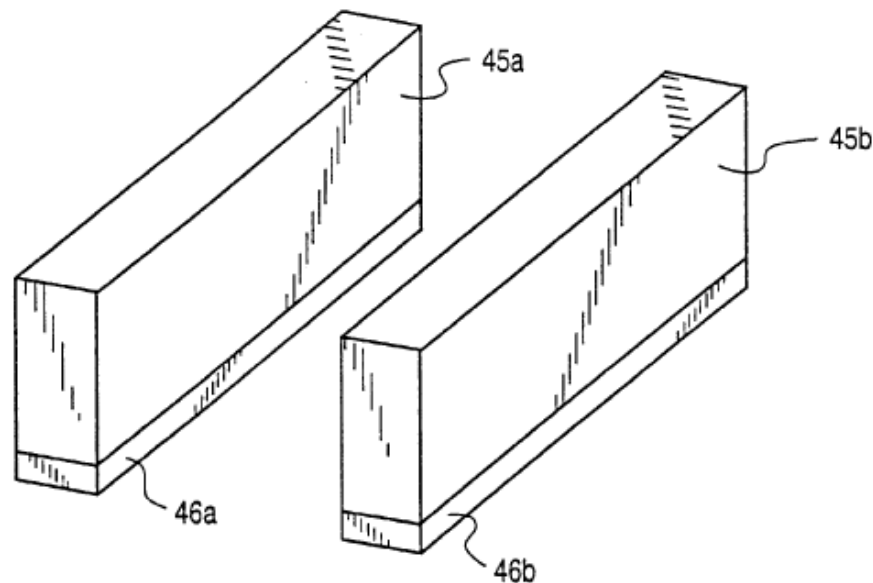


Figure 6(c) depicts the wafer after etching and depositing of the insulator layer on the wafer, and shows individual pillar layer strips, as opposed to isolated individual pillars. *Id.* at 13:41–45. Although not shown in Figure

6(c), Johnson explains that a dielectric fills the voids between the strips and pillars, adding support to the array. *Id.* at 13:51–53.

Johnson explains that this process is repeated multiple times to form multiple levels of conductors and vertically stacked pillars. *Id.* at 13:58–14:27. Figure 6(g) depicts a stack with three conductor layers. *Id.* at 14:21–22.

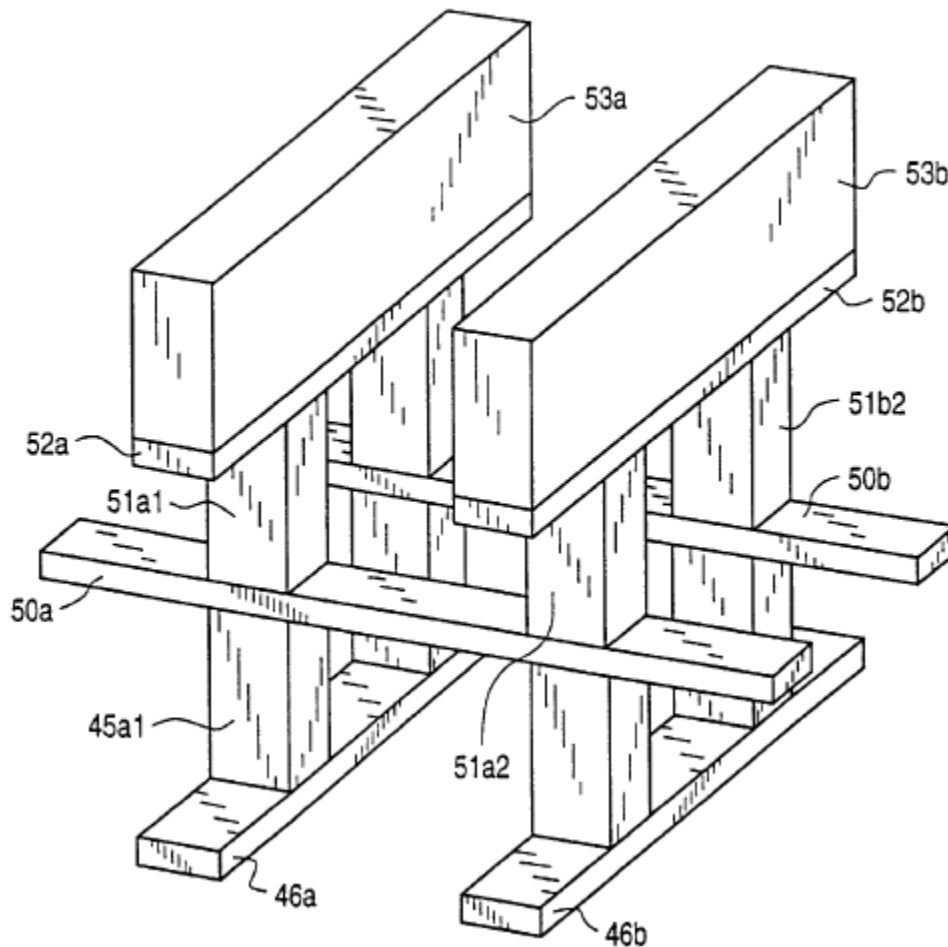


Figure 6(g) depicts the wafer after three levels of conductors and layer stacks have been deposited, but before all of the masking and etching steps have been applied to the upper most layer. *Id.* at 14:10–19.

2. *Analysis: Claim 13*

Petitioner contends that Johnson discloses every limitation of claim 13, at least under Patent Owner’s apparent construction of “stackable add-on layer.” Pet. 65–73. With respect to claim 13[a], Petitioner contends that Johnson discloses forming CMOS transistors, i.e., electrical devices, within a monocrystalline substrate and depositing a dielectric insulating layer over the substrate and electrical devices. *Id.* at 65–66 (citing Ex. 1010, 13:26–35; Ex. 1003 ¶ 226). With respect to claim 13[b], Petitioner contends that Johnson discloses vertically oriented semiconductor memory cells and a “stackable add-on layer” under Patent Owner’s apparent construction of this term, i.e., a monolithically and directly deposited layer created on an insulator. *Id.* at 66–68, 72. With respect to claim 13[c], Petitioner contends that the “stackable add-on layer” of Johnson is bonded to an insulator deposited on a wafer. *Id.* at 69–72 (citing Ex. 1010, 12:8–12, 12:42–65, 13:26–35, Fig. 6(b)). With respect to claim 13[d], Petitioner contends that Johnson is directed to non-volatile memory cells that include at least one transistor. *Id.* at 72–73.

On this record, we preliminarily adopt Petitioner’s construction of “stackable add-on layer,” which Petitioner does not assert is disclosed in Johnson under its proposed construction. As such, Petitioner does not demonstrate a reasonable likelihood that claim 13 would have been obvious based on Johnson alone. Prelim. Resp. 31 (Patent Owner asserting that Petitioner’s ground based solely on Johnson fails because it is based on a claim construction that Petitioner does not agree with).

K. *Claim 13 over Johnson and Kim or Aspar (Grounds 2B, 2C)*

Petitioner contends the subject matter of claim 13 would have been obvious over the combined disclosures of Johnson and Kim or Aspar.

Pet. 74–77 (Johnson and Kim), 77–82 (Johnson and Aspar). Petitioner’s arguments for these two grounds are similar to the arguments discussed above with respect to the combinations of Lee and Kim or Aspar. *Compare* Pet. 50–63 *with id.* at 74–82.

Patent Owner presents two arguments against the combination of Johnson and Kim or Aspar: (1) that there is insufficient evidence that the dielectric layer of Johnson is disposed above the electrical devices; and (2) that Petitioner presents insufficient reasoning to support the combination of Johnson and Kim or Aspar. Prelim. Resp. 40–48. We address these issues in turn.

1. “a dielectric layer disposed above the electrical devices”

Claim 13 requires “a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices.” Ex. 1001, 12:25–27.

Petitioner contends that “Johnson’s fabrication starts with a wafer having devices in the substrate and ‘[a]n insulator then is deposited.’” Pet. 66 (quoting Ex. 1010, 13:26–35). Petitioner further contends that the fabrication sequence of the memory cells depicted in Figures 6(b)–6(g) of Johnson “involves ‘deposition and planarization of an interlevel dielectric.’” *Id.* (quoting Ex. 1010, 12:42–54). Accordingly, Petitioner contends that Johnson teaches “a dielectric layer disposed above the electrical devices.” *Id.* (citing Ex. 1003 ¶ 226).

Patent Owner contends that Johnson “says nothing about whether the insulator (the Petition’s alleged dielectric layer) is disposed above any electrical devices, as required by limitation 13[a].” Prelim. Resp. 41. Patent Owner contends that in contrast to Lee Figure 35 which expressly depicts devices in the substrate and covered by dielectric layer 3102, “Johnson is

silent as to the depth of any dielectric layer in relation to the height of any electrical devices.” *Id.* at 41–42.

On this record, we find that Petitioner contention that Johnson discloses “a dielectric layer disposed above the electrical devices,” as recited in claim 13, is sufficient for purposes of institution. For example, Johnson discloses that CMOS transistors for the peripheral circuitry may be fabricated in the monocrystalline substrate. Ex. 1010, 13:26–29. Then, an insulator is deposited on the substrate, first conductor layer 46 is deposited above the insulator, and first layer stack 45 is deposited on the first conductive layer. *Id.* at 13:30–35, Fig. 6(b). Johnson discloses that layer stack 45 “is a continuous sheet that extends across the entire integrated circuit (indeed across the entire wafer) such as shown in Fig. 6(b).” *Id.* at 12:42–47.

2. *Reason to Combine Johnson and Kim or Aspar*

Petitioner contends that a person of ordinary skill in the art “would have been motivated to use Kim’s wafer bonding techniques when fabricating Johnson’s structure.” Pet. 74. According to Petitioner’s proposed combination, “Johnson’s separately fabricated memory cells . . . would be formed on their own substrate,” which would then be “flipped and bonded” to a wafer having, “for example, Johnson’s ‘CMOS transistors’ . . . and insulating layer.” Pet. 75. Petitioner contends one of ordinary skill in the art would have sought to wafer bond Johnson’s layer of memory cells to its insulating layer based on the teachings of Kim and Aspar because (1) this modification “consists of nothing more than” using a known technique to improve a similar known device in the same way (*id.* at 75–76); (2) this modification “would have amounted to applying a known technique,” to address the same known problem recognized in both Johnson and Kim and

Aspar, using prior art elements according to their established functions (*id.* at 76); and (3) this modification would allow for more efficient quality control with less potential waste (*id.*).

Patent Owner contends Petitioner’s assertions that Johnson’s layer of memory cells would be wafer bonded to Johnson’s insulating layer, and that Aspar’s Smart-Cut bonding process would be used to bond Johnson’s layer of memory cells to its insulating layer, merely address whether a skilled artisan “could have made” the proposed combination. Prelim. Resp. 46–47 (citing Pet. 75, 78). According to Patent Owner, assertions that Johnson’s 3D structure *could be* implemented with wafer stacking do not demonstrate that one of ordinary skill in the art *would have been motivated to make* the combinations or modification of prior art to arrive at the claimed invention. *Id.*

Patent Owner also contends that the fact that wafer bonding was a potential alternative to Lee’s monolithic method of fabricating 3D structures “does not provide a motivation for wholesale substitution of Johnson’s” deposition method with Kim’s or Aspar’s wafer bonding. Prelim. Resp. 46. Patent Owner also contends that Petitioner’s proposed substitution of wafer bonding for Johnson’s deposition “is discounted by [Petitioner’s] own references explaining the problems with wafer bonding, such as reduced density, which is contrary to the essence of 3D structures.” *Id.* (citing Ex. 1016, 1:39–47; Ex. 1003 ¶¶ 250, 261)

After considering the parties’ arguments and evidence, we determine that Petitioner’s asserted quality control benefit and *KSR*-based rationales provide a sufficient basis on which to institute review, and the parties’ contentions present factual issues that are best resolved on a full record after trial.

L. Claim 1 over Park and Kim (Ground 3)

Petitioner contends the subject matter of claim 1 would have been obvious over the combined disclosures of Park and Kim. Pet. 82–91.

1. Park

Park is titled “Semiconductor Device Having Vertical Metal Oxide Semiconductors and a Method for Manufacturing the Same,” and issued November 5, 1996. Ex. 1011, codes (45), (54).

Park notes that conventional memory devices “traditionally form a transistor in a lateral direction on a semiconductor substrate.” *Id.* at 1:22–23. Park explains, however, that “it is substantially impossible to realize a semiconductor memory device of a continued higher capacity using the conventional planar layout.” *Id.* at 1:31–33.

To allow for higher capacity memory devices, Park discloses the use of a silicon pillar that “is extended in a perpendicular (vertical) direction with respect to the semiconductor substrate” and surrounded by an insulating film. *Id.* at 2:15–20. “A gate insulating film is interposed between the silicon pillar and a gate electrode surrounding the silicon pillar” and impurity regions “are formed in upper and lower portions of the silicon pillar to form the source and drain regions.” *Id.* at 2:20–25.

Figure 9 of Park is reproduced below:

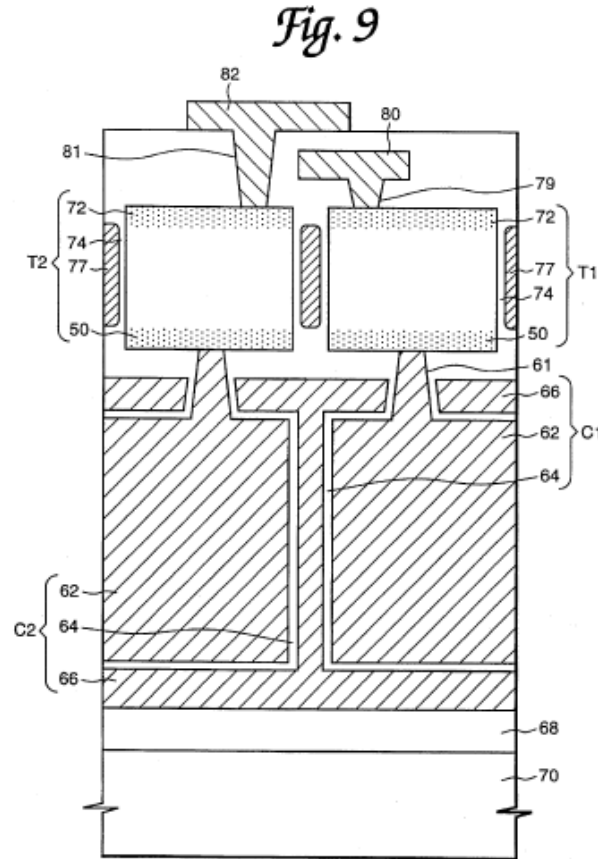


Figure 9 is a cross-sectional view of a DRAM cell manufactured according to the invention of Park. *Id.* at 5:33–35. In Figure 9, transistors T1 and T2 are formed with a vertical channel structure. *Id.* at 5:36–37. Capacitors C1 and C2 are formed under first and second transistors T1 and T2 and are comprised of storage electrodes 62 connected to source regions 50 of the first and second transistors T1 and T2. *Id.* at 5:39–41. Plate electrode 66 surrounds the entire surface of the storage electrode 62, with a dielectric film 64 interposed therebetween. *Id.* at 5:41–43. First bitline 80 is connected to drain region 72 of first transistor T1, and second bitline 82 is connected to drain region 72 of second transistor T2. *Id.* at 5:43–46.

2. *Analysis: Claim 1*

Petitioner contends the use of Kim’s wafer stack comprising logic devices in combination with Park’s DRAM cells teaches or suggests every limitation of claim 1. Pet. 83–93. Petitioner further contends that one of ordinary skill in the art would have been motivated to vertically stack Park’s DRAM memory cells using Kim’s wafer stack method because this combination would “increase integration” and result in reduced interconnect RC delay and increased system performance. *Id.* at 83–84.

The parties’ dispute regarding this combination centers around whether Park discloses “memory cells separated from each other by dielectric material.” Pet. 88–89; Prelim. Resp. 48–53. Petitioner contends that Park discloses that each of its vertically structured transistors are “surrounded [] with an insulating film” and that dielectric film 64 is also interposed between the plate and storage electrodes of capacitors C1 and C2. Pet. 88–89 (citing Ex. 1011, 2:16–21, 4:6–27, 5:21–22, 5:37–43, Fig. 3). Petitioner further contends that one of ordinary skill in the art “would have . . . understood the need to separate the memory cells with dielectric material for proper operation (e.g., avoiding shorts).” *Id.* at 89. According to Petitioner, “because both the transistors and capacitors of each memory cell are surrounded by insulating material,” each of Park’s DRAM memory cells are “separated from each other by dielectric material,” as recited in claim 1. *Id.* at 89.

Patent Owner contends this ground fails because Petitioner relies entirely on Park for the disclosure of the disputed claim term, but Park “neither disclosed nor suggested memory cells separated from each other by dielectric material.” Prelim. Resp. 49. Patent Owner asserts that Park’s disclosure of surrounding transistors with a dielectric does not demonstrate

that the *memory cells* as a whole are separated from each other by dielectric material. *Id.* Patent Owner further asserts that dielectric film 64 in Figures 8 and 9 is interposed between the plate and storage electrodes of capacitors C1 and C2, but is “not disposed between separate memory cells.” *Id.* at 50–51.

On this record, Patent Owner raises a significant issue as to whether Park discloses *memory cells* that are separated from each other by dielectric material. As shown in Figure 9 of Park, some portions of the memory cells are separated by, or share, dielectric material, whereas other portions of the memory cells are separated by, or share, plate electrode 66, which neither party asserts is a dielectric material. Ex. 1011, Figs. 8–9.

III. CONCLUSION

For the reasons discussed above, Petitioner demonstrates a reasonable likelihood of prevailing in showing that at least one claim of the ’702 patent would have been obvious over the prior art of record. Specifically, Petitioner demonstrates a reasonable likelihood that it will prevail on at least one its challenges to independent claim 13 based upon the asserted combinations based on Lee or Johnson.

IV. ORDER

Accordingly, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1 and 13–17 of the ’702 patent is instituted with respect to all grounds set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the ’702 patent shall commence on the date of this Decision, and notice is hereby given of the institution of trial.

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Patent 7,378,702 B2

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