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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00991
U.S. Patent No. 7,378,702

**PATENT OWNER'S RESPONSE TO
PETITION FOR *INTER PARTES* REVIEW**

TABLE OF CONTENTS

I.	INTRODUCTION.....	1
II.	BACKGROUND.....	4
A.	A New Breakthrough In 3D Memory	4
B.	The '702 Patent Invention.....	5
C.	Serial NAND vs. Parallel NOR Memory.....	7
D.	Lee Application (EX1007).....	8
E.	Kim Application (EX1008).....	9
F.	Aspar Article (EX1009).....	9
G.	Johnson (EX1010)	11
H.	Park (EX1011)	13
I.	Endoh (EX1012)	14
III.	LEVEL OF ORDINARY SKILL IN THE ART.....	14
IV.	CLAIM CONSTRUCTION	14
A.	“stackable add-on layer” / “the stackable add-on layer [is]/[being] bonded”	15
B.	“SOI pillar”	16
V.	LEGAL REQUIREMENTS TO SHOW OBVIOUSNESS	18
VI.	THE PETITION DOES NOT MEET ITS BURDEN TO SHOW OBVIOUSNESS BASED ON LEE AND KIM (GROUNDS 1C-1D).....	20
A.	Intel Does Not Establish A Motivation To Combine Lee With Kim (Grounds 1C-1D Claims 13-17).....	20
1.	The Petition Fails To Show A Motivation To Stack Lee’s Interleaved Levels.....	21

2.	“Quality Control” And “Less Waste” Provide No Reason To Switch To Kim’s Non-Monolithic Stacked Wafers.....	26
B.	No Reasonable Expectation Of Success For Using Kim To Build Lee’s Interleaved Levels (Grounds 1C-1D Claims 13-17).....	30
C.	Intel Improperly Argues Unpatentability Under A Claim Construction Of “SOI Pillar” It Claims Is Incorrect (Ground 1C-1D Claims 14-17).....	31
D.	Lee Did Not Disclose Memory Cells “Serially Connected Together” (Ground 1C Claims 16-17)	33
E.	The Petition’s Cross-Referencing To Earlier Grounds With Incompatible Claim Constructions Lacks Particularity (Ground 1D Claims 16-17)	35
F.	This Ground Fails To Address All Claim Limitations (Ground 1D Claims 16-17)	37
G.	The Petition Provides No Motivation To Combine Lee’s NOR With Endoh’s NAND Design With Any Reasonable Expectation Of Success (Ground 1D Claims 16-17)	39
VII.	THE PETITION DOES NOT MEET ITS BURDEN TO SHOW OBVIOUSNESS BASED ON LEE AND ASPAR (GROUNDS 1E-1F) ...	43
A.	Intel Does Not Establish A Motivation To Combine Lee With Aspar (Grounds 1E-1F Claims 13-17).....	44
1.	The Petition Fails To Show A Motivation To Stack Lee’s Interleaved Levels.....	44
2.	One Of Skill Would Not Risk Applying Aspar’s High-Temperature Annealing To Lee.....	45
3.	“Quality Control” and “Less Waste” Provide No Reason To Switch to Aspar	49

B.	No Reasonable Expectation Of Success For Combining Lee With Aspar (Grounds 1E-1F Claims 13-17)	50
C.	The Petition’s Ambiguous Construction Of “SOI Pillar” Does Not Establish Unpatentability (Ground 1E Claims 14-17)	52
D.	Lee Did Not Disclose Memory Cells “Serially Connected Together” (Ground 1E Claims 16-17).....	53
E.	The Petition’s Cross-Referencing To Grounds With Conflicting Claim Construction Positions Lacks Particularity (Ground 1F Claims 16-17)	53
F.	This Ground Fails To Address All Claim Limitations (Ground 1F Claims 16-17)	54
G.	The Petition Provides No Motivation To Combine Lee, Aspar, And Endoh With Any Reasonable Expectation Of Success (Ground 1F Claims 16-17)	55
VIII.	THE PETITION DOES NOT MEET ITS BURDEN FOR THE GROUNDS 1A-1B CHALLENGES BASED ON LEE	55
A.	The Petition Improperly Argues Unpatentability Under Claim Constructions For “Stackable Add-On layer” And “SOI Pillar” It Claims Are Incorrect (Ground 1A-1B Claims 13-17).....	55
B.	Lee Did Not Disclose Memory Cells “Serially Connected Together” (Ground 1A Claims 16-17)	56
C.	The Petition Provides No Motivation To Combine Lee And Endoh, Let Alone A Reasonable Expectation Of Success (Ground 1B Claims 16-17)	56
D.	This Ground Fails To Address All Claim Limitations (Ground 1B Claims 16-17)	56

IX.	THE PETITION DOES NOT MEET ITS BURDEN TO SHOW OBVIOUSNESS BASED ON JOHNSON AND KIM (GROUND 2B)	57
A.	Johnson Does Not Disclose Or Suggest “Memory Cells Having At Least One Transistor” (Claim 13).....	57
B.	One Of Skill Would Not Have Been Motivated To Modify Johnson’s Diode Design With Any Reasonable Expectation Of Success (Claim 13)	62
C.	Intel Does Not Establish A Motivation To Combine Johnson With Kim (Claim 13).....	65
1.	Merely Asserting That Johnson Could Be Combined With Kim Does Not Show A Motivation To Combine	65
2.	“Quality Control” And “Less Waste” Provide No Motivation To Switch To Kim	67
D.	The Petition Provides No Reasonable Expectation Of Success In Combining Johnson And Kim (Claim 13).....	68
X.	THE PETITION DOES NOT MEET ITS BURDEN TO SHOW OBVIOUSNESS BASED ON JOHNSON AND ASPAR (GROUND 2C)	69
A.	Johnson Does Not Disclose Or Suggest “Memory Cells Having At Least One Transistor” (Claim 13).....	70
B.	One Of Skill Would Not Have Been Motivated To Modify Johnson’s Diode Design (Claim 13).....	70
C.	Intel Does Not Establish A Motivation To Combine Johnson With Aspar (Claim 13).....	70
D.	The Petition Has Not Established A Reasonable Expectation Of Success In Combining Johnson With Aspar (Claim 13)	73
XI.	THE PETITION DOES NOT MEET ITS BURDEN FOR GROUND 2A BASED ON JOHNSON.....	74
A.	Johnson Does Not Disclose Or Suggest “Memory Cells Having At Least One Transistor” (Claim 13).....	75

B.	One Of Skill Would Not Have Been Motivated To Modify Johnson’s Diode Design (Claim 13).....	75
C.	The Petition Improperly Argues Unpatentability Under A Construction Of “Stackable Add-On Layer” It Claims Is Incorrect (Claim 13).....	75
XII.	THE PETITION DOES NOT MEET ITS BURDEN FOR GROUND 3 BASED ON PARK AND KIM.....	75
XIII.	CONCLUSION	79

TABLE OF AUTHORITIES

	Page No(s).
<i>Belden v. Berk-Tek</i> , 805 F.3d 1064 (Fed. Cir. 2015)	19, 66, 72
<i>CIVIQ Smartscales v. Mfg. Res. Int’l</i> , IPR2018-00774, 2018 WL 4625764 (P.T.A.B. Sept. 25, 2018)	30, 35
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<i>Dish Network v. Entropic Commc’ns</i> , IPR2023-00392, 2023 WL 5193078 (P.T.A.B. Aug. 11, 2023)	21
<i>Ebates Performance Mktg. v. IBM</i> , IPR2022-00439, 2022 WL 5048425 (P.T.A.B. Oct. 3, 2022)	32, 56, 75
<i>Funai Elec. v. Gold Charm</i> , IPR2015-01491, Paper 15 (P.T.A.B. Dec. 28, 2015)	18
<i>Hartness Int’l v. Simplimatic Eng’g</i> , 819 F.2d 1100 (Fed. Cir. 1987)	38
<i>Hewlett Packard Enter. v. K.Mizra</i> , IPR2022-00843, 2022 WL 16556406 (P.T.A.B. Oct. 31, 2022)	40
<i>Hilti v. Milwaukee Elec. Tool</i> , IPR2015-01166, Paper 81 (P.T.A.B. Nov. 14, 2016)	41, 43
<i>Hologic v. Enzo Life Scis.</i> , IPR2018-00019, 2018 WL 1897623 (P.T.A.B. Apr. 18, 2018)	31, 56, 75
<i>Intamin v. Magnetar Techs.</i> , 483 F.3d 1328 (Fed. Cir. 2007)	78
<i>Intelligent Bio-Sys. v. Illumina Cambridge</i> , 821 F.3d 1359 (Fed. Cir. 2016)	18

Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

<i>KSR Int’l v. Teleflex</i> , 550 U.S. 398 (2007)	19, 20, 26, 66, 72
<i>Lyft v. Quartz Auto Techs.</i> , IPR2020-01450, 2021 WL 838289 (P.T.A.B. Mar. 4, 2021).....	36, 54
<i>In re Magnum Oil Tools</i> , 829 F.3d 1364 (Fed. Cir. 2016)	31, 37, 53, 54
<i>Microchip Tech. v. HD Silicon Sols.</i> , IPR2021-00872, 2021 WL 6339555 (P.T.A.B. Dec. 15, 2021).....	42
<i>Microsoft v. Koninklijke Philips N.V.</i> , IPR2018-00026, 2018 WL 1997727 (P.T.A.B. Apr. 27, 2018)	26, 27, 40, 67
<i>MobileMedia Ideas v. Apple</i> , 780 F.3d 1159 (Fed. Cir. 2015)	19, 43
<i>Netflix v. Robocast</i> , IPR2023-00081, 2023 WL 5162380 (P.T.A.B. May 11, 2023).....	78
<i>Nitro Fluids v. Cameron Int’l</i> , IPR2020-00691, 2020 WL 5031954 (P.T.A.B. Aug. 25, 2020)	64
<i>In re Nuvasive</i> , 842 F.3d 1376 (Fed. Cir. 2016)	20, 40, 66
<i>One World Techs. v. Chevron (HK) Ltd.</i> , PGR2020-00059, 2020 WL 7222691 (P.T.A.B. Dec. 7, 2020).....	36, 40, 53, 54, 78
<i>Palo Alto Networks v. Finjan</i> , IPR2015-01979, 2017 WL 1040259 (P.T.A.B. Mar. 15, 2017).....	19
<i>Personal Web Techs. v. Apple</i> , 848 F.3d 987 (Fed. Cir. 2017)	66, 72
<i>Phillips v. AWH</i> , 415 F.3d 1303 (Fed. Cir. 2005)	14

Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

<i>Polaris Indus. v. Arctic Cat</i> , 882 F.3d 1056 (Fed. Cir. 2018).....	62
<i>Qualcomm v. Intel</i> , 6 F.4th 1256 (Fed. Cir. 2021).....	36, 54
<i>Raytheon Techs. v. Gen. Elec.</i> , 993 F.3d 1374 (Fed. Cir. 2021).....	61
<i>Realtime Data v. Iancu</i> , 912 F.3d 1368 (Fed. Cir. 2019).....	15, 16
<i>Redline Detection v. Star Envirotech</i> , 811 F.3d 435 (Fed. Cir. 2015).....	48, 72
<i>Robotic Vision Sys. v. View Eng’g</i> , 189 F.3d 1370 (Fed. Cir. 1999).....	38
<i>Samsung Elecs. v. Elm 3DS Innovations</i> , 925 F.3d 1373 (Fed. Cir. 2019).....	<i>passim</i>
<i>SkinMedica v. Histogen</i> , 727 F.3d 1187 (Fed. Cir. 2013).....	18
<i>Sony v. Fujifilm</i> , IPR2018-01751, 2019 WL 1581942 (P.T.A.B. Apr. 12, 2019).....	27, 40, 67
<i>Streck v. Ravgen</i> , IPR2021-01577, Paper 62 (P.T.A.B. Apr. 18, 2023)	49, 72
<i>Xerox v. Bytemark</i> , IPR2022-00624, 2022 WL 3648989 (P.T.A.B. Aug. 24, 2022)	26, 36, 52, 54, 78

OTHER AUTHORITIES

37 C.F.R. § 42.65.....	36
37 C.F.R. § 42.100.....	14, 18
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35 U.S.C. § 312	36, 52

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Exhibit No.	Description
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Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

Exhibit No.	Description
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I. INTRODUCTION

Intel’s also-ran Petition is a mishmash of ten separate grounds, searching for a path to void BeSang’s groundbreaking invention. The Board found most of these grounds deficient and instituted a trial to explore the combinations of Lee/Kim (or Aspar) and Johnson/Kim (or Aspar). These grounds also cannot be sustained.

To undo BeSang’s ’702 Patent, Intel cannot rely on whimsical combinations divorced from the challenges of pioneering a new semiconductor design. It’s incumbent on Intel to proffer “specific evidence” showing a reason to combine them with a reasonable expectation of success. *Samsung Elecs. v. Elm 3DS Innovations*, 925 F.3d 1373, 1382 (Fed. Cir. 2019). Its Petition fell far short on every single ground.

Ground 1A-1B. The Board already found Intel’s Lee (and Endoh) grounds deficient because they relied on claim constructions Intel and its expert affirmatively said were wrong. They also fail to show Lee’s parallel NOR device disclosed memory cells “serially connected together,” or any reason to replace Lee’s ultra-dense 4 control-gate-per-pillar memory cells with Endoh’s “two memory cells” instead, confirming patentability of Claims 16-17.

Ground 1C-1D. The Board ordered trial on the Lee and Kim grounds, but Intel cannot sustain its burden to show that using Kim’s stacking on Lee’s monolithic

design would have been obvious. The Petition's pretext for this combination quickly evaporated because Lee plainly explained how to deposit layer 3104.

Intel never demonstrates a motivation for stacking Lee's interleaved memory cells using Kim, let alone with any reasonable expectation of success. Intel provides no explanation of how to pull off Lee's control gates shared between upper and lower levels with Kim's stacking, particularly given Lee's non-endorsement of a stacked approach. Intel also did not sustain its unwieldy combination either by improved quality control (Lee's device already would be fab tested) or less waste (Kim's spendthrift method discards nearly an entire wafer for each layer it stacks).

These grounds also are deficient: (1) for urging unpatentability based on a construction of "SOI pillar" it affirmatively rejects; (2) because Lee's parallel NOR device didn't teach serial memory cells; (3) for cryptic cross-referencing to other grounds based on inconsistent claim constructions; (4) failing to show a motivation to combine Lee and Endoh.

Ground 1E-1F. Intel's theory that Aspar's Smart-Cut stacking should be applied to Lee is charred by Aspar's teaching to bake (anneal) Lee's device at 1100°C. There's nothing to test because Intel's combination combines unpatterned wafers, and overbaking Lee's device doesn't reduce waste but multiples it. Simply put, Grounds 1E-1F are a less-skilled impersonation of Lee/Kim: basically the same arguments (and more) also apply to the Lee/Aspar combination.

Ground 2A-2C. Johnson (and Kim or Aspar) also do not sustain Intel’s burden to show unpatentability of Claim 13. Johnson’s self-aligned 2-terminal diode/antifuse memory did show disclosure or obviousness of “memory cells having at least one transistor,” and in fact taught away from a 3-terminal implementation. Intel did not establish a working disclosure of or motivation to replace the diode with a 3-terminal transistor design in Johnson’s high-density array, particularly with any reasonable expectation of success. And Ground 2A for Johnson alone was based on a claim construction Intel affirmatively attacked.

The combination with Kim (or Aspar) in Grounds 2B-2C fail because Johnson advocated self-aligned deposition as “an extremely important advantage” to achieve his high-density design, providing zero reason to jettison it in favor of Kim’s less-precise and alignment-error-prone stacking technique. Aspar in Ground 2C was again a non-starter because of its 1100°C annealing.

Ground 3. Park and Kim only challenge unasserted Claim 1. This ground should also be rejected because Park didn’t satisfy “memory cells separated from each other by dielectric material” because its adjoining capacitors share a plate and its transistors are connected by a common electrode.

In sum, pulling off BeSang’s invention of 3D memory is a complex puzzle, and Intel’s Petition fails to show it was obvious. BeSang achieved its paradigm-shifting invention only after summing the significant challenges of designing

memory cells and control logic with a compatible and manufacturable architecture. The '702 Patent told the world how to build its architecture with low-temperature processing and vertically stacking multiple memory cells in a single chip. BeSang's invention took years of creativity and hard work, and its breakthrough made the company famous. Intel acknowledged this feat of engineering at the time, and these insufficient *post hoc* combinations seeking to cancel the '702 Patent now only underscore the magnitude of BeSang's innovation.

The challenged claims should be confirmed.

II. BACKGROUND

A. A New Breakthrough In 3D Memory

Conventional CMOS technology relied on shrinking memory cells to obtain high-capacity storage devices. BeSang was trying to achieve an outside-the-box solution: further increasing memory capacity by going vertical like a skyscraper. EX1001 at 1:23-2:3. The issue was how to design a manufacturable chip to achieve the potential of this 3D memory.

In 2004, inventor Sang-Yun Lee filed the application that issued as the '702 Patent containing his solution. Start-up BeSang, in collaboration with Stanford University, by 2008 had achieved “a 3D IC technology breakthrough” by fabricating a 3D IC “contain[ing] 128 million vertically oriented devices.” EX2005 at 1. BeSang was suddenly famous: widely praised in the industry and called a “pioneer”

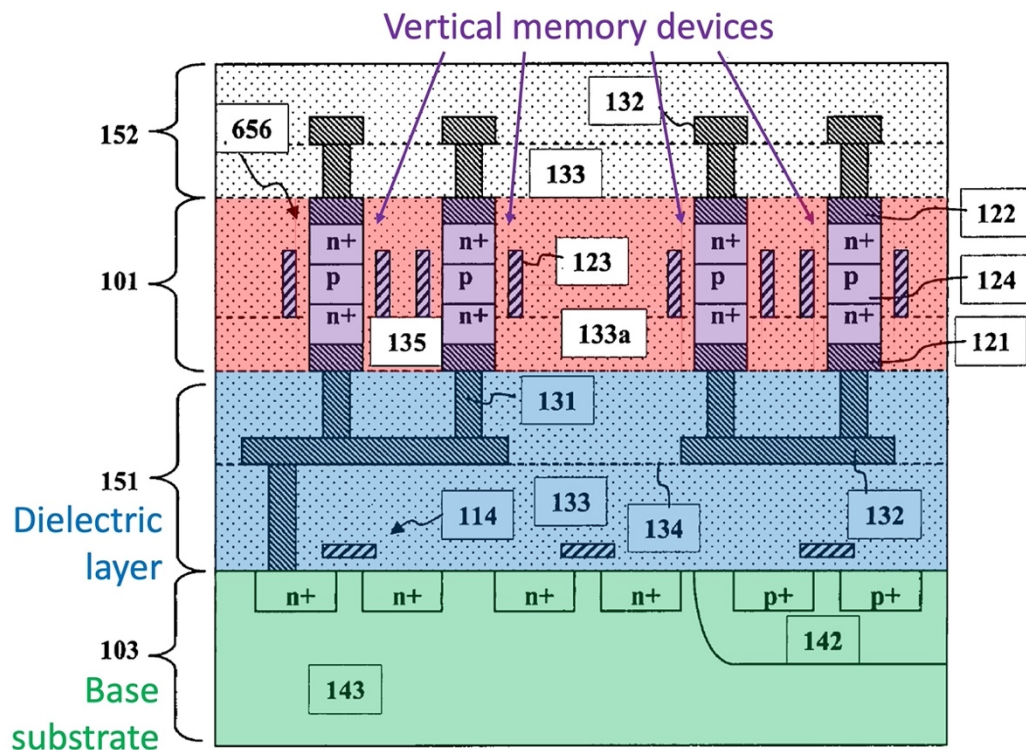
in 3D solutions with a design presenting “clear-cut winning edges” over existing memories. EX2008 at 17; EX2009 at 1; *see also* Paper 6 (“POPR”) at 1, 5-6. It took the rest of the industry seven years to catch up, including Micron and Intel who had initially expressed a lot of interest in working with BeSang. EX2014 at 1; EX2015 at 1-2; EX1013 ¶¶29; IPR2023-00900, EX1019 ¶¶34-35; *see also* POPR at 7.

B. The ’702 Patent Invention

The ’702 Patent is titled “Vertical Memory Device Structures” and solved the practical challenges posed by scaling two-dimensional memory. It recognized the need for “structures and methods that are suitable for providing increased circuit density in integrated circuits without necessarily requiring devices to be made smaller.” EX1001 at 1:40-43. The patent describes vertical memory cells, allowing the memory array to expand in a third dimension, and putting logic circuitry underneath the array to further increase density and performance. *Id.* at 3:51-61, 5:60-63, Fig. 1; EX2029 ¶¶39-48.

Figure 1 below shows “vertical memory devices 656” that “are separated by isolation 135 and have floating structures in the filled dielectric materials 133a” that serve as insulators. EX1001 at 5:18-21.

Fig. 1

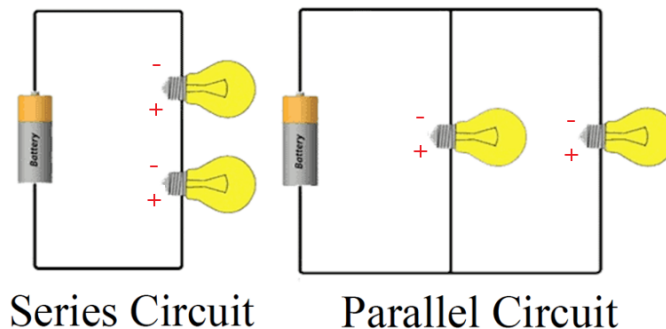


EX1001 at Fig. 1 (annotated); *see also id.* at 1:54-56 (dielectric material between memory cells), 6:6-8.

The '702 Patent taught the need for low-temperature processing of 3D integrated circuits under 650°C, including gate oxidation at low temperatures. *See, e.g., id.* at 7:15-35. Among other benefits, BeSang discovered that if the gate dielectric layer has a combination of low temperature thermal oxide, high-K dielectric, and CVD dielectric, then device reliability and current-driving capability increase, while on-resistance decreases. EX1005 at 21:52-22:2.

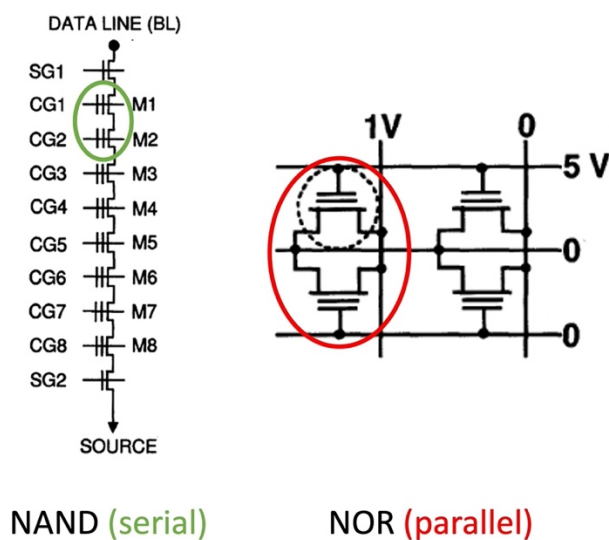
C. Serial NAND vs. Parallel NOR Memory

Serial and parallel circuits are fundamental concepts in electronics:



EX2023 (annotated); *see also* EX2039 at 48:18-49:16.

Like these lightbulb circuits, memory devices can use different circuits to connect their memory cells. As shown below, NAND memory devices are connected in series, meaning that the source of one cell is connected to the drain of the next, while NOR devices are connected in parallel (source-to-source and drain-to-drain):



EX2024 at 39, 42, Figs. 1.33(c), 1.35 (both annotated); EX2043 at 1:32-49; EX2039 at 53:3-55:22.

D. Lee Application (EX1007)

Lee taught a “directly deposited” monolithic three-dimensional memory array to achieve “increased density and a lower cost.” EX1007 ¶¶106-07, Abstract. Lee contrasted its improved monolithic approach with “non-monolithic” devices using separately formed memory arrays. EX1007 ¶107.

Lee’s devices employed a unique, interleaved three-dimensional NOR matrix with memory cells densely packed and sharing control gates between levels. *E.g.*, EX1007 at Figs. 13-28, ¶¶161-69.

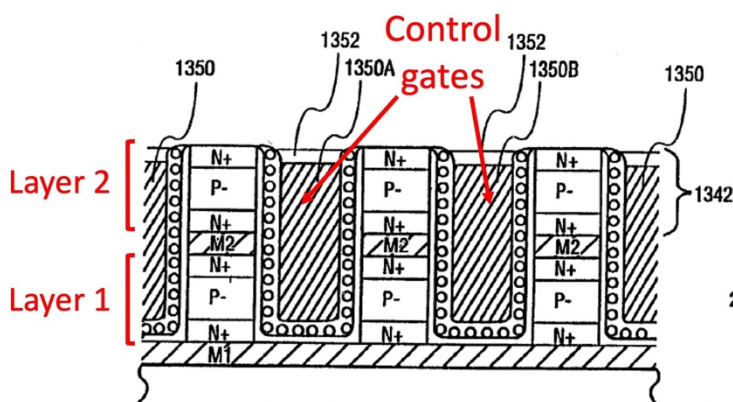


FIG. 25A

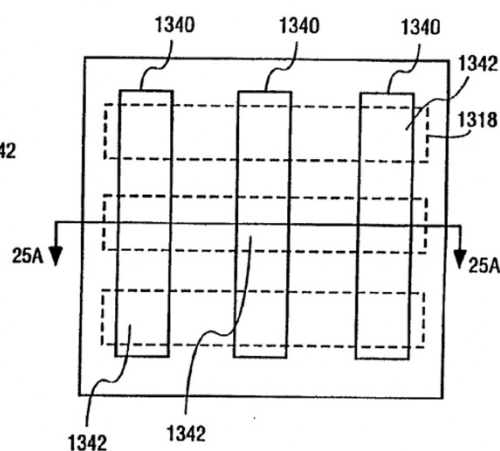


FIG. 25B

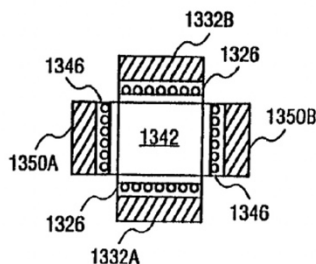


FIG. 26

Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

EX1007 at Figs. 25-26. Lee’s Figures 13-28 taught the process for forming an interleaved array of memory devices, where adjoining levels shared control gates. EX1007 ¶¶52, 147-69; EX1003 ¶¶155-56; EX2039 at 45:18-46:3; EX2029 ¶¶50-70.

E. Kim Application (EX1008)

Kim disclosed a “wafer-to-wafer” stacking technique. EX1008 ¶20; EX2029 ¶¶72-73.

F. Aspar Article (EX1009)

Aspar, published in the Journal of Electronic Materials, described the Smart-Cut® technique. EX1009 at 834. It studied “homogenous thin film transfer[s]” onto other wafers. EX1009 at 839. Aspar’s thin films were unpatterned layers that did not contain any transistors or similar devices. *E.g.*, EX1009 at Figs. 12, 14, 16.

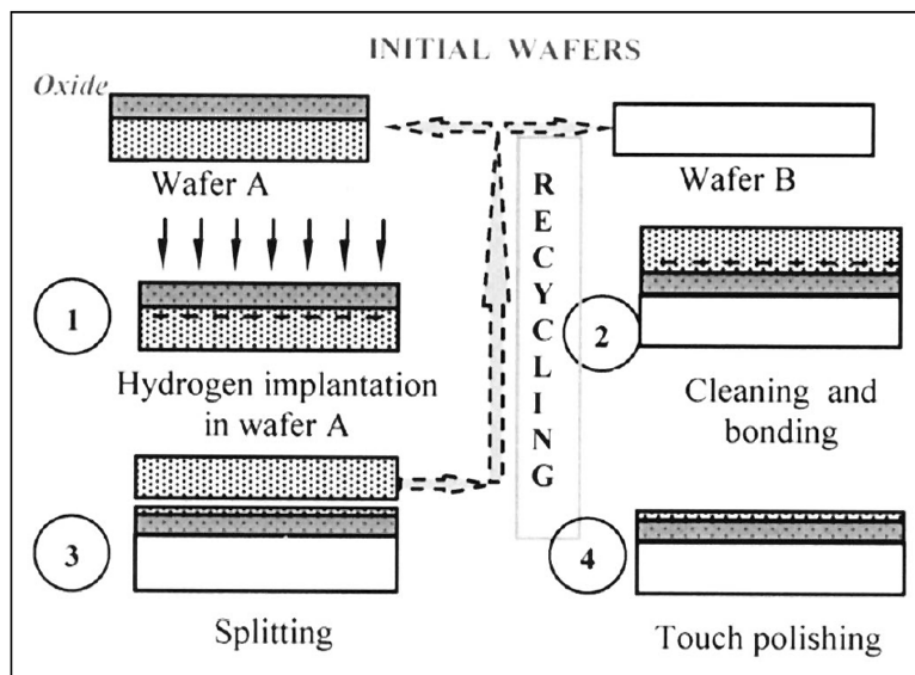


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

Aspar explained that Smart-Cut includes the following steps:

1. Implanting hydrogen in Wafer A to create a weakened layer.
2. Wafer bonding Wafer A to support Wafer B.
3. Transferring a thin layer from Wafer A to Wafer B by splitting Wafer A along the weakened layer from step 1.
4. Removing the rough surface remaining after splitting.

EX1009 at 834, Fig. 1; EX2029 ¶¶75-79.

Intel's other exhibits describe additional details of Aspar's Smart-Cut:

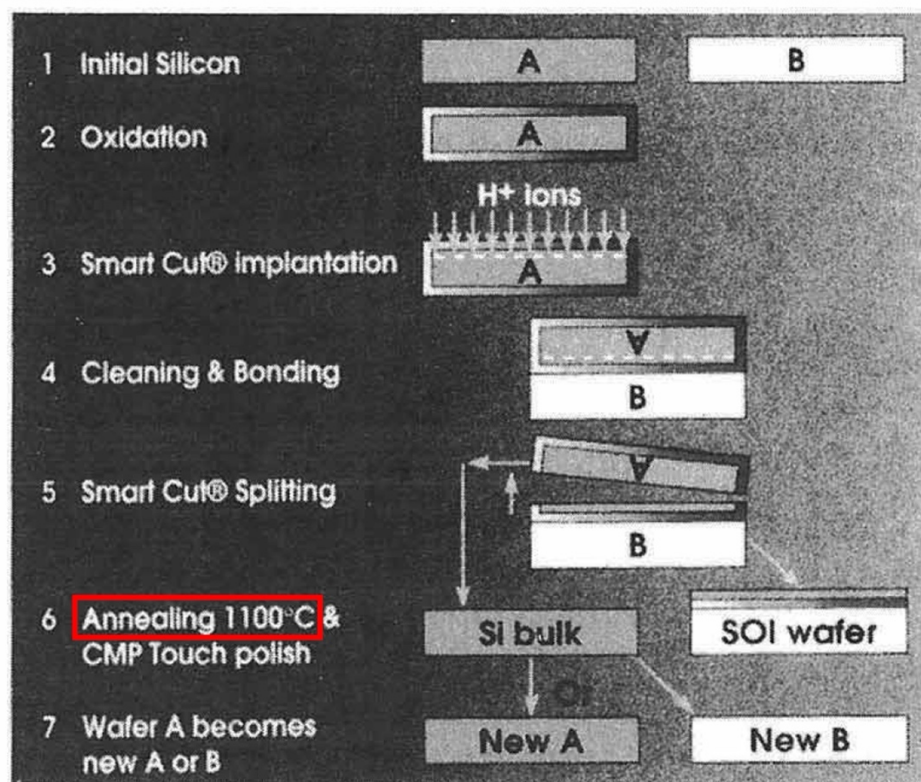


Fig. 11-24 Process flow for fabricating Smart-Cut® wafers.

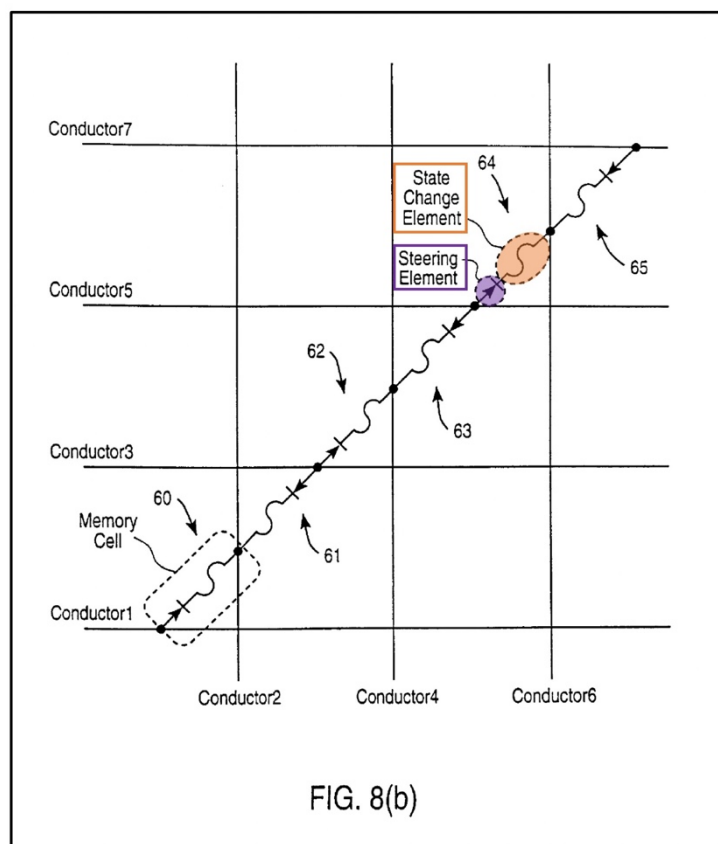
EX1015 at 543, Fig. 11-24 (annotated), quoted by EX1003 ¶46; EX2039 at 118:10-119:2. After splitting, “[b]oth wafers are then annealed at 1100°C to remove defects.” EX1015 at 544; *see also* EX1014 at 260-61, Fig. 7-29; EX1003 ¶¶46-47 (citing EX1014-1015); EX2039 at 121:8-11 (“Q. So figure 11[-]24, which you put in your declaration shows that annealing step at 1100 degrees Celsius; correct? A. Yes.”); EX2039 at 117:17-121:11.

G. Johnson (EX1010)

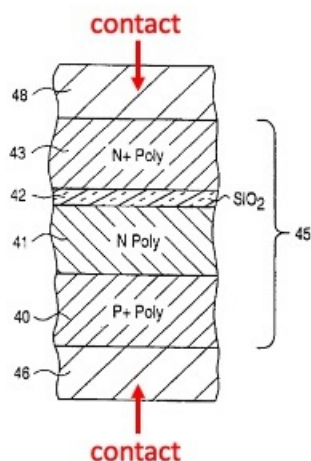
Johnson teaches a NOR diode cross-point memory. EX2029 ¶81; EX1010 at Figs. 6(g), 8(b). When the Johnson patent was filed in 1998, nonvolatile memories

came in two primary flavors: (1) factory pre-programmed cheap mask ROMs; or (2) expensive, field-programmable “write/erase/rewrite” EEPROM or “write once” PROM. EX1010 at 1:20-42. These field-programmable memories typically used transistors, “allow[ing] only very limited integration vertically into the third dimension.” EX1010 at 2:28-36. But they were less dense and higher cost compared to mask ROMs. EX1010 at 2:21-27. Johnson set out to “achiev[e] the cost and density of a mask ROM” in a field-programmable memory. EX1010 at 1:57-61.

Johnson created NOR memory cells with a “two terminal structure” using a diode and antifuse. EX1010 at 5:41-65, 7:45-8:45; EX2029 ¶¶82, 168. Johnson placed “steering element 22” (purple diode) that controlled the current direction, and a “change element 23” (orange antifuse) that stored data. *Id.*; EX1010 at Fig. 8(a)-8(b) (annotated). The diode permitted current in only one

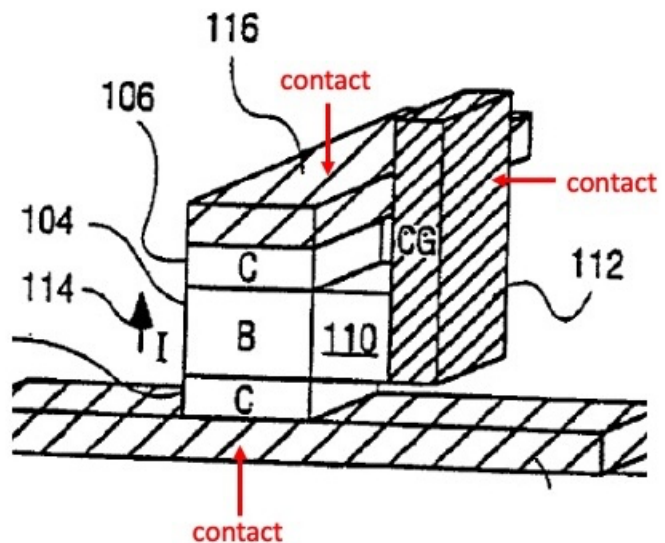


direction, so the change element could be individually accessed. EX1010 at 5:50-58, 7:58-61.



Johnson's diode

Fig. 6(a) (excerpted, annotated)



Lee's transistor

Fig. 1A (excerpted, annotated)

Johnson's 2-terminal architecture was self-aligned and easy to manufacture because each memory cell pillar was defined and patterned by the intersecting conductors above it. EX1010 at 11:49-57. Johnson's design was simplified compared to 3-terminal transistor memories, which were harder to manufacture because they required precise alignment and required large "misalignment tolerances, which increase die size, decrease density, and increase cost." EX1010 at 3:6-8; *see also* EX1010 2:37-3:8. Johnson disclosed the "fabrication sequence" for his memory in Figures 6(b)-6(g). EX1010 at 12:42-65.

H. Park (EX1011)

The Petition relies on Park solely for its Ground 3 challenge to Claim 1. Pet. at 3. Park disclosed DRAM memory cells that share capacitor plates and gate

electrodes with no separation among adjacent cells. *See, e.g.*, EX1011 at 5:49-53, Figs. 8-9; EX2029 ¶84.

I. Endoh (EX1012)

The Petition cites to Endoh’s Figures 1171-72 as a secondary reference solely for its challenge to dependent Claims 16-17. Pet. at 3; EX2029 ¶86.

III. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the time of the invention would have had a bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa. EX2029 ¶¶34-38. Intel proposes a person with “at least three years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent.” Pet. at 9; EX1003 ¶37. The Board can confirm patentability under either definition.

IV. CLAIM CONSTRUCTION

Claims in an IPR are “construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b).” 37 C.F.R. § 42.100(b); *see also Phillips v. AWH*, 415 F.3d 1303, 1312-17 (Fed. Cir. 2005) (en banc).

A. “stackable add-on layer” / “the stackable add-on layer [is]/[being] bonded”

The Board provided its interpretation of “stackable add-on layer” at institution:

a layer that is formed separately from the substrate and then bonded to the substrate or a dielectric layer above the substrate. We do not understand a “stackable add-on layer” to include memory cells that are formed by sequential deposition on or above a substrate or dielectric layer without being added to a separately formed substrate.

I.D. at 9. The Board also preliminarily construed the “stackable add-on layer [is]/[being] bonded” limitation to “require a separate layer that is formed apart from the substrate and then subsequently bonded to the substrate or a dielectric layer above the substrate.” *Id.* at 11.

BeSang respectfully disagrees with the Board’s preliminary constructions because they are incorrect. Although Intel must establish that its constructions are both correct and are met by the asserted art to prove invalidity, the Board may confirm the patentability of the Challenged Claims for reasons unrelated to the construction of these terms. *Realtime Data v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) (“The Board is required to construe only those terms that are in controversy, and only to the extent necessary to resolve the controversy.” (cleaned up)).

B. “SOI pillar”

For purposes of institution, the Board applied Intel’s construction of “SOI pillar” requiring “a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology.” I.D. at 12.

BeSang respectfully submits that no construction of “SOI pillar” is necessary to confirm the patentability of the claims in this IPR. *Realtime Data*, 912 F.3d at 1375. But if the Board deems construction necessary, “SOI pillar” should be construed according to its ordinary and customary meaning as “a silicon-on-insulator structure taller than it is wide.” EX2029 ¶¶89-95. This definition accords with well-understood concepts of pillar structures and the SOI pillar embodiments in the ’702 Patent.

There is no dispute that “SOI” is an acronym meaning silicon-on-insulator. Pet. at 4 (Intel: “In the ’702 Patent, ‘[t]he acronym ‘SOI’ generally refers to Silicon-on-Insulator’...”); EX1003 ¶87 (Sechen: same); EX1001 at 4:45-46.

Dictionaries define “pillar” as a structure that is “relatively slender in proportion to its height.” *E.g.*, EX2031 at 1469 (Webster’s: “pillar” defined as “an upright shaft or structure, of stone, brick, or other material, relatively slender in proportion to its height....”); EX2032 at 988 (same). This definition is consistent with the ’702 Patent’s depictions and descriptions of SOI pillars. The below figures show proportionally slender pillars:

Fig. 4

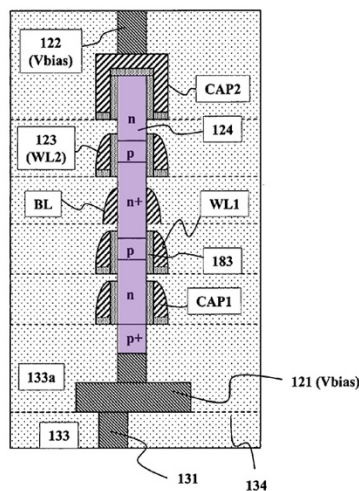


Fig. 20

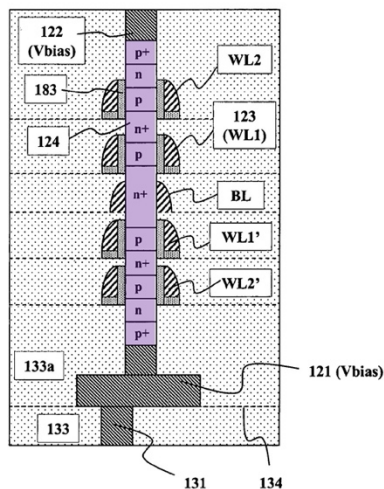
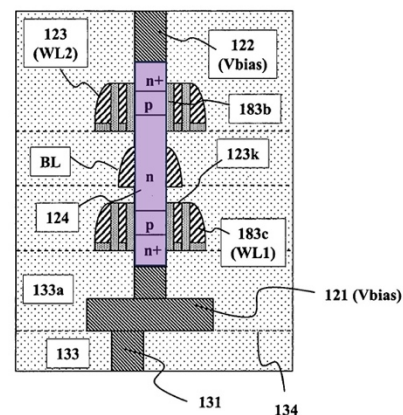


Fig. 27



EX1001 at Figs. 4, 20, 27 (depicting SOI pillars annotated in purple). For Figure 4, the '702 Patent explains that “the aspect ratio of SOI pillar 124 remains relatively small” given its larger height relative to its width. *Id.* at 8:5-10.

As explained in the Micron IPR, Micron’s submitted evidence also supports this construction. *See, e.g.*, EX2041 at 947, Figs. 3(a)-(b) (depicting flash memory with “pillar” structures having height larger than width), Fig. 5 (showing SEM photograph of S-SGT structured cell with silicon pillars); EX2042 at 2217 (showing “S-SGT pillars” in Figure 1).

Intel’s 16-word proposal that ““SOI pillar”... requires a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology” is both incorrect and unhelpful. *See* Pet. at 13 (citing EX1003 ¶¶85-91). Construing “pillar” to mean “pillar-shaped” and “SOI” to mean “SOI” unhelpfully defines the

Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

limitation using its own language. *Cf. Funai Elec. v. Gold Charm*, IPR2015-01491, Paper 15 at 13 (P.T.A.B. Dec. 28, 2015).

Intel’s own expert couldn’t justify its construction. Claim terms are given their plain and ordinary meaning, 37 C.F.R. § 42.100(b), and Dr. Sechen acknowledged that “pillar” had “some plain and ordinary meanings[;] I’m sure they exist,” EX2039 at 21:2-14. In a rather extraordinary exchange, Dr. Sechen admitted: “I honestly haven’t looked at a dictionary to come up with something” and “ha[d] not attempted a definition” of “pillar.” EX2039 at 17:14-22:2.

Second, Intel and its expert based their definition on the ’702 Patent’s reference to “individual doped stack structures (i.e., pillar structures).” Pet. at 13 (quoting EX1001 at 6:26-29); EX1003 ¶86 (same). Their unnatural interpretation has it exactly backward—the Federal Circuit has held that using “i.e.” does not define what follows the “i.e.” based on what precedes it. *See, e.g., SkinMedica v. Histogen*, 727 F.3d 1187, 1201 (Fed. Cir. 2013).

Intel’s nonsense construction should be rejected.

V. LEGAL REQUIREMENTS TO SHOW OBVIOUSNESS

To prove obviousness, Intel must establish a motivation to combine the references and that one of ordinary skill would have had a reasonable expectation of success in making the combination. *Intelligent Bio-Sys. v. Illumina Cambridge*, 821 F.3d 1359, 1367-68 (Fed. Cir. 2016). One of skill “would not have been motivated

to combine... references to arrive at the claimed invention” where doing so “would be beyond the technical ability of a skilled artisan.” *MobileMedia Ideas v. Apple*, 780 F.3d 1159, 1167-68 (Fed. Cir. 2015). An obviousness analysis also requires a determination of “whether a person of ordinary skill in the art, having all the teachings of the references before him, is able to produce the structure defined by the claim.” *Samsung*, 925 F.3d at 1382-83 (citation omitted). In complex “integrated-circuit technology,” a petitioner should show “specific evidence that a person of ordinary skill in the art would have reasonably expected success in combining” the references. *Id.* at 1382-83.

“[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden v. Berk-Tek*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (emphasis in original). “It is not enough to assert that the prior art provides two options and that it would have been predictable to implement either.” *Palo Alto Networks v. Finjan*, IPR2015-01979, 2017 WL 1040259, at *24 (P.T.A.B. Mar. 15, 2017). Instead, Petitioner must identify “a design need or market pressure to solve a problem” before looking for potential solutions. *Id.* (quoting *KSR Int’l v. Teleflex*, 550 U.S. 398, 421 (2007)).

Simply put, a motivation to combine requires “explain[ing] the *reason why* a PHOSITA would have been motivated to modify” a reference in view of another to

include a feature taught by the claimed invention. *In re Nuvasive*, 842 F.3d 1376, 1384 (Fed. Cir. 2016) (emphasis in original). Establishing a reason or motivation to combine the prior art is a critical guardrail against “the distortion caused by hindsight bias” and the “temptation to read into the prior art the teachings of the invention in issue.” *KSR*, 550 U.S. at 421 (quoting *Graham v. John Deere Co.*, 383 U.S. 1, 36 (1966)).

VI. THE PETITION DOES NOT MEET ITS BURDEN TO SHOW OBVIOUSNESS BASED ON LEE AND KIM (GROUNDS 1C-1D)

The Board ordered trial to further consider Lee/Kim in Grounds 1C-1D. Because the Petition shows no supported motivation to fabricate Lee’s interleaved levels using Kim’s stacking, let alone with a reasonable expectation of success, all claims should be confirmed. Proffering claim constructions Intel and its expert affirmatively refute, fundamentally misunderstanding Lee and Endoh, and cryptically cross-referencing other, inconsistent grounds further does not meet Intel’s burden here. These grounds should be rejected.

A. Intel Does Not Establish A Motivation To Combine Lee With Kim (Grounds 1C-1D | Claims 13-17)

Grounds 1C-1D theorize that one of skill would have switched from Lee’s interleaved, monolithic levels to Kim’s non-monolithic stacking method to satisfy limitation 13[c]. That lacks any support. Claims 13-17 should be confirmed over Grounds 1C-1D.

1. The Petition Fails To Show A Motivation To Stack Lee's Interleaved Levels

The Petition fails to establish a motivation to replace Lee's deposited, interleaved levels with stacked layers from Kim. Pet. at 51-54. The pretext for this combination is that Lee purportedly did not "clearly describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102" in Figure 35. Pet. at 51. As the Board observed, Lee did. I.D. at 35 (level 3104 is formed "through direct deposition on the dielectric layer" (citing EX1007 ¶¶107, 122; Pet. at 34-35)).

Dr. Sechen can't even defend this pretext. He admitted that Lee's Figures 13-28 describe how to make the structure shown in Figure 35. EX2039 at 88:2-89:6; EX1003 ¶¶103-110 (describing same process using Lee's figures); EX1003 ¶155 (describing Lee's "fabrication process" with reference to Figs. 13-28). There is no serious dispute that the lowest "device level 3104" is deposited on "insulating layer 3102" in Figure 35. EX1007 ¶111; *id.* ¶¶107, 122, 147-48; Pet. at 51 (Intel: "In Lee, each level 3104 is deposited on the underlying level...."); EX2029 ¶¶115-16. Intel cannot sustain its burden. *See, e.g., Dish Network v. Entropic Commc'ns*, IPR2023-00392, 2023 WL 5193078, at *6 (P.T.A.B. Aug. 11, 2023) (rejecting obviousness based on "assertion that Carnero does not disclose the source of the information" as unsupported because Carnero did).

Dr. Sechen proposes adding individual memory cells from Figures 1-2, 7 or 25A as a single layer using Kim. EX1003 ¶¶193-94. But Dr. Sechen’s individual memory cells plucked from Figures 1-2 or 7 are not what Lee discloses as a layer 3104, EX1007 ¶111, and he admits that Lee’s Figure 25A is incomplete, EX2039 at 44:21-45:5 (acknowledging Lee’s Figure 25A is in an “intermediate form before it’s converted to actual pillars”); EX1007 ¶¶165-66; EX2029 ¶119.

Lee’s Figures 13-23 describe how levels 1-2 of its device are deposited. EX1007 ¶¶147-62; EX2029 ¶120. Figures 24-25 shows depositing in gap 1343 a

control gate 1350

adjacent to the pillars on

both level 1 (item 1342)

and level 2 (item 1340).

EX1007 ¶¶163-65. Lee

plainly depicts the control

gates 1350 overlapping

levels 1 *and* 2 of its

structure: “[A]s shown in

FIG. 25A a control gate

1350 is formed between

second pillar strip 1340 as

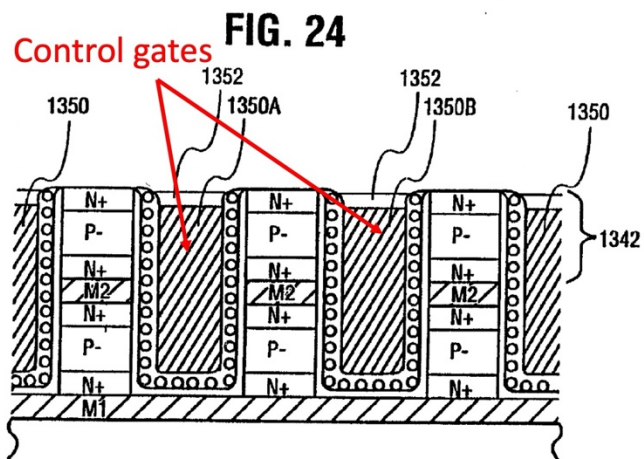
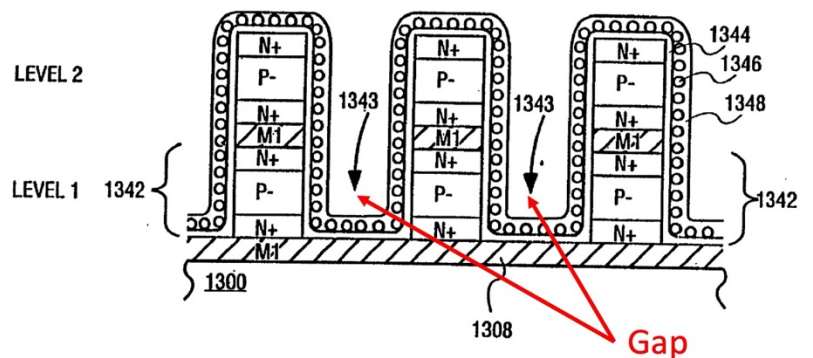


FIG. 25A

well as in the gaps 1343 between pillars 1342.” EX1007 ¶165; EX2039 at 45:18-46:3. After completing Figure 25A, Lee says: “At this point, the fabrication of the first level of memory devices is complete.” EX1007 ¶166; EX2029 ¶120.

Later, after Lee adds level 3, level 3 is used to complete formation of level 2’s strips into pillars, and to create another set of control gates that overlap levels 2 and 3 as shown in Figure 27A. EX1007 ¶167; *see also* EX2039 at 43:12-15 (Sechen: agreeing that Lee’s level 2 is used to form level 1), 45:6-17 (agreeing that level 3 is used to form level 2).

To do this, the control gates from Figure 25A were not removed as Dr. Sechen wrongly interpreted this figure. *See* EX2039 at 46:5-48:5. Figure 27A simply shows a different view of level 1. EX1007 ¶167 (“FIGS. 27A and 27B [are] FIG. 26 rotated

90°”); EX2029 ¶¶121-22.

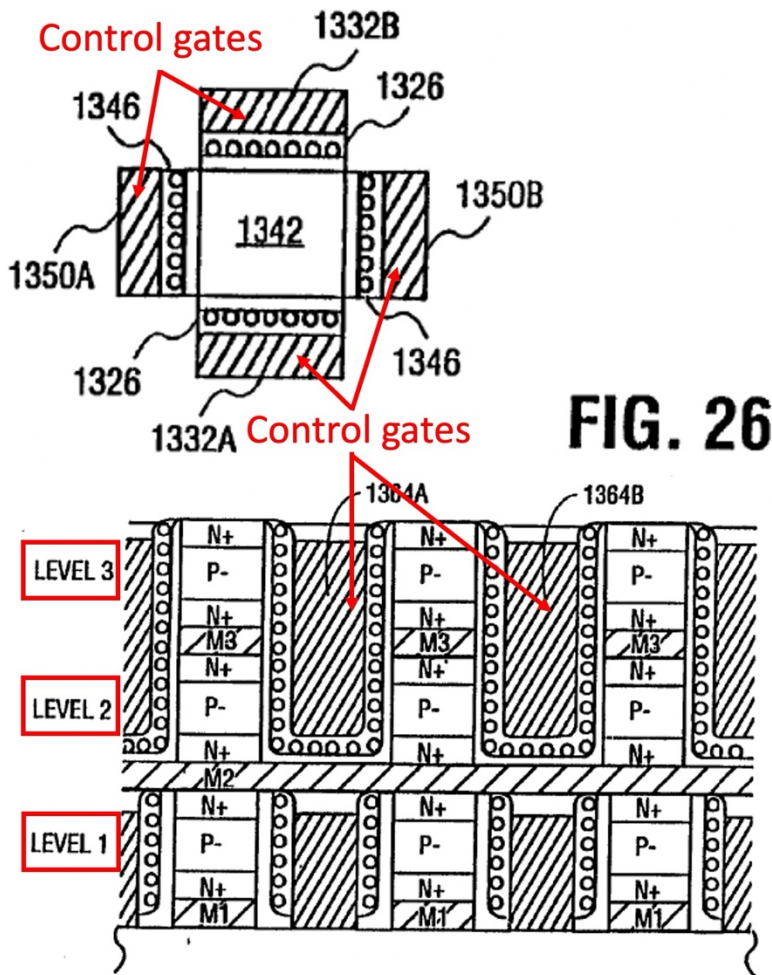


FIG. 27A

As Lee explains for the top-down view in Figure 26, each pillar contains two pairs of control gates, 1332A-B and 1350A-B, and “[e]ach control gate 1350 [in Fig. 26] will be shared with the subsequently formed pillar memory device position[ed] vertically above, in Level 2....” EX1007 ¶166.

Lee’s pattern continues by interleaving control gates between levels. EX1007 ¶167 (“[T]he steps of FIGS. 20-25 can be repeated... to pattern the second pillar strips 1340 into a plurality of second pillars 1362 on a second level and to form a

second pair of control gates 1364 adjacent to the second pillars.”); EX2029 ¶123.

Thus, Lee’s method both uses the next level to pattern the level below, and interleaves control gates between the levels. EX2029 ¶123.

The result of Lee’s shared control gates is no clean horizontal partition point between Lee’s levels. EX1007, Figs. 25A-27A; EX2029 ¶124. Indeed, Intel offers no explanation for how Lee’s deposited, interleaved levels could be recreated by stacking, and Dr. Sechen’s failure to recognize Lee’s levels were interleaved moots his declaration testimony on this point. *See* Pet. at 51-54; EX1003 ¶¶193-94; EX2039 at 46:5-48:5. Lee’s disclosure was predicated on deposition to fabricate its interleaved levels. EX1007 ¶¶163-69, Figs. 24-27. Neither the Petition nor Dr. Sechen provide any credible reason that one of skill would have been motivated to look to stacking instead.

The Petition also argues that “a POSITA, at the suggestion of Lee, was looking to separately form a two-dimensional array of memory devices and ‘package it together.’” Pet. at 51. As the Board recognized, Lee was antagonistic towards such a non-monolithic approach. EX1007 ¶107; I.D. at 35 (“Lee does not appear to advocate for stacking two-dimensional arrays, but rather contrasts this method with its potentially more efficient monolithic arrays.”); POPR at 36-38. Lee focused on “directly deposit[ing]” monolithic arrays for “increased density and a lower cost.”

EX1007 ¶¶106-07. It did this by using one level to pattern another and by interleaving the levels. EX1007 ¶¶163-69, Figs. 24-27; EX2029 ¶¶117-18.

The Petition never explains why one relying on Lee’s disclosure would choose a less-dense and more-costly configuration that was incompatible with Lee’s design. *See* Pet. at 51-52 (citing EX1003 ¶¶190-92). Dr. Sechen’s declaration selectively quotes and twists Lee’s paragraph 107 to suggest Lee endorsed a non-monolithic approach. EX1003 ¶192. This unsupported testimony should be given no weight. *Xerox v. Bytemark*, IPR2022-00624, 2022 WL 3648989, at *6 (P.T.A.B. Aug. 24, 2022) (precedential).

Intel has not met its burden to show a motivation to combine.

2. “Quality Control” And “Less Waste” Provide No Reason To Switch To Kim’s Non-Monolithic Stacked Wafers

Intel generically argues that “Kim’s wafer bonding” was a “known technique” that purportedly would improve Lee’s Figure 35. Pet. at 53. But the Petition never explains how. *See* Pet. at 53; I.D. at 35 (finding same). Just because something is already known does not make it obvious. *KSR*, 550 U.S. at 418-19 (“[I]nventions in most, if not all, instances rely upon building blocks long since uncovered [that are] already known.”). Lee knew about non-monolithic devices and did not endorse them for his interleaved device, EX1007 ¶107, and the Petition has no explanation why one of skill would depart from Lee’s monolithic design, *see* Pet. at 51-53; *Microsoft*

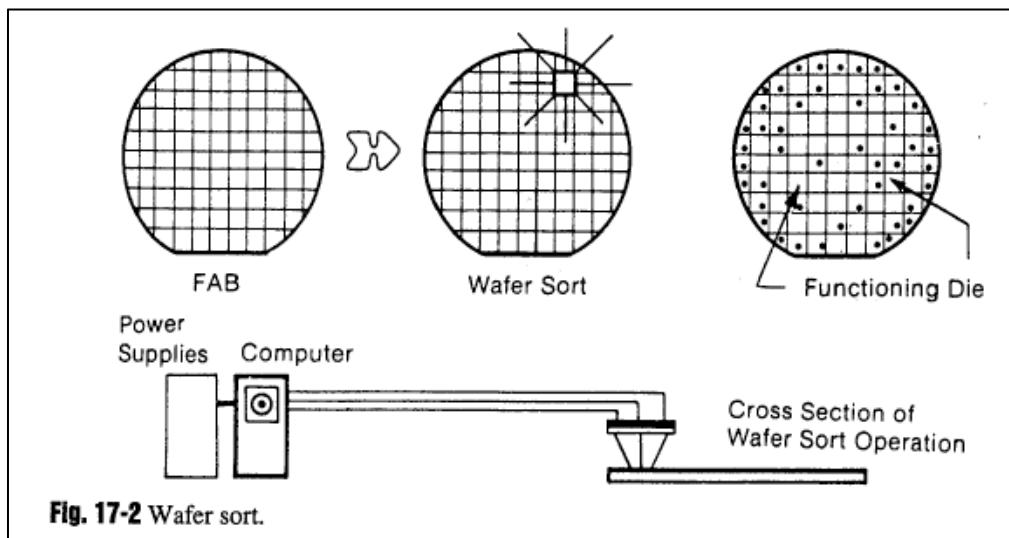
Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

v. Koninklijke Philips N.V., IPR2018-00026, 2018 WL 1997727, at *6 (P.T.A.B. Apr. 27, 2018); *Sony v. Fujifilm*, IPR2018-01751, 2019 WL 1581942, at *5 (P.T.A.B. Apr. 12, 2019).

The Petition asserts the superiority of “wafer bonding” over monolithic deposition because it “allow[ed] for more efficient quality control with less potential waste” because the memory cells could be first “test[ed] for shorts.” Pet. at 53-54 (citing EX1003 ¶196; EX1016). The Board ordered trial to examine this. I.D. at 35-36. Both assertions are baseless.

No quality control improvement. Lee did not recommend wafer bonding, let alone extol its quality control benefits, *e.g.*, EX1007 ¶107, and Kim says nothing about quality control or pre-bonding testing for shorts, *see generally* EX1008; EX2029 ¶125. Yet Intel and its expert assert that wafer bonding allows “testing for shorts.” Pet. at 53-54 (citing EX1003 ¶196); EX1003 ¶196 (Dr. Sechen: describing “test[ing] each wafer before stacking ‘to screen out defective ones.’”).

There’s no dispute semiconductor fabs routinely test monolithic devices they build. EX2039 at 114:14-115:15 (Sechen acknowledging “typical chip fabrication process” involves testing devices). Intel’s own exhibits describe electrical testing by fabs, where any failed dies are marked with a drop of ink so they can be discarded:



EX1014 at 841 (describing “wafer sort”.... to determine which of their die are functional”), Fig. 17-2; EX1016 at 1:48-49 (“the chips in each wafer are tested to screen out defective ones”); EX2029 ¶127. Testing stacked wafers is not a benefit over monolithic wafers. EX2029 ¶127.

Dr. Sechen relies on the Fung patent (EX1016), which he says shows that testing “layers of devices before stacking” would improve “yield loss.” EX1003 ¶196 (quoting EX1016 at 1:33-52). First, Dr. Sechen’s comparison is in reference to stacking without testing, *id.*, and he provides absolutely no data “compar[ing] yields for monolithic three-dimensional arrays to yields for non-monolithic stacked wafers” to support his opinion. I.D. at 35-36; *see also* POPR at 38-39.

Second Fung doesn’t support Dr. Sechen, instead warning of the “several problems associated with stacking wafers”: a potential “maximum yield” of 49% after stacking (which “forcibly results in a significant increase in cost”) and the

“common occurrence” of layer misalignment. EX1016 at 1:32-52. Sechen admits that “maintain[ing] good alignment... [is] standard practice,” EX2039 at 78:7-13, and Fung only torpedoed Dr. Sechen’s claim that a skilled artisan would have looked to Kim’s stacking, EX1016 at 1:44-56; EX2029 ¶¶125-26, 128-29.

Kim only creates more trash. The Petition’s argument that Kim leads to “less potential waste” has it backwards: Kim’s stacking technique is much more extravagant than Lee’s. Pet. at 53-54. Lee’s deposition method builds many levels on a single wafer, EX1007 ¶¶107, 111, and there’s no serious dispute that finding an error in one die (or several) would not dictate discarding an entire wafer’s worth of dies, EX1014 at 841 (describing “wafer sort”); EX1016 at 1:48-49; EX2029 ¶130. Dr. Sechen acknowledged that “discard[ing] the whole wafer” is “very unlikely to ever happen because the chips are individualized,” and “you surely don’t want to throw away a whole wafer because it has a bad die.” EX2039 at 113:12-114:12.

But Kim instructed throwing away almost an entire wafer after every stacking. EX2029 ¶131. After the two wafers 210 and 220 are bonded, Kim teaches “the top wafer 220 can also be thinned,” EX1008 ¶25, by “a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process,” EX1008 ¶27; *see also* EX2029 ¶131. Simply put, after Kim adds a layer, almost all of the top wafer is ground or etched off. *See id.*; EX2029 ¶¶131-32. Kim’s technique does not reduce waste, it multiplies it. *Id.*

The Petition sets forth no supported rationale for combining Lee and Kim.
See Pet. at 53-54.

B. No Reasonable Expectation Of Success For Using Kim To Build Lee’s Interleaved Levels (Grounds 1C-1D | Claims 13-17)

In complex “integrated-circuit technology,” a petitioner should show “specific evidence that a person of ordinary skill in the art would have reasonably expected success in combining” the references. *Samsung*, 925 F.3d at 1382-83. Yet the Petition’s single conclusory sentence, Pet. at 54 (citing EX1003 ¶197 (same)), falls far short of meeting Intel’s burden here.

Intel and its expert overlooked the reasons Lee preferred monolithic structures: patterning levels using higher levels and interleaved control gates between levels in its NOR array. *Supra* § VI.A.1; Pet. at 53-54; EX1003 ¶¶193-94; EX1007 ¶¶163-69, Figs. 24-27; EX2039 at 46:5-48:5. Dr. Sechen’s fundamental misunderstanding of Lee’s structure in his declaration, which he did not understand is interleaved, renders his testimony on likelihood of success irrelevant. *See* EX1003 ¶¶193-94; EX2039 at 45:18-48:5 (Sechen: interleaved control gates are removed); *CIVIQ Smartscapes v. Mfg. Res. Int’l*, IPR2018-00774, 2018 WL 4625764, at *7 (P.T.A.B. Sept. 25, 2018) (“misunderstanding of Heady’s disclosures” fails to show obviousness).

The Petition makes no effort to explain how these interleaved levels could be created by stacking, Pet. at 51-54, and a skilled artisan would not have thought that recreating this interleaved structure with separate, stacked layers was likely to succeed, especially where the next level is used to pattern the lower level, EX2029 ¶¶119-24, 133; EX1007 ¶¶163-69, Figs. 24-27. Lee’s own skepticism of non-monolithic fabrication, EX1007 ¶107, shows that Lee himself did not think it could be pulled off. The Petition’s lack of “specific evidence” showing a reasonable expectation of success provides yet another basis to confirm the claims over Grounds 1C-1D. *Samsung*, 925 F.3d at 1382-83.

C. Intel Improperly Argues Unpatentability Under A Claim Construction Of “SOI Pillar” It Claims Is Incorrect (Ground 1C-1D | Claims 14-17)

Intel cannot prevail based on a construction of “SOI pillar” that both the Petition and Intel’s expert assert is incorrect.

“In an *inter partes* review, the burden of persuasion is on the petitioner to prove unpatentability by a preponderance of the evidence, and that burden never shifts to the patentee.” *In re Magnum Oil Tools*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (cleaned up). Intel must establish “[h]ow the challenged claim is to be construed” and “[h]ow the construed claim is unpatentable.” 37 C.F.R. § 42.104(b)(3)-(4); *Hologic v. Enzo Life Scis.*, IPR2018-00019, 2018 WL 1897623, at *3-4 (P.T.A.B. Apr. 18, 2018) (denying institution: grounds “based on a different

construction that Petitioner considers to be erroneous” insufficient under 37 C.F.R. § 42.104(b)(3)-(4)); *Ebates Performance Mktg. v. IBM*, IPR2022-00439, 2022 WL 5048425, at *5 (P.T.A.B. Oct. 3, 2022); POPR at 29-33.

The Petition exclusively asserts unpatentability of Claims 14-17 in Grounds 1C-1D based on BeSang’s “apparent construction of ‘SOI pillar,’” Pet. at 50, 55, which Intel says is “incorrect,” Pet. at 16. Dr. Sechen follows suit, EX1003 ¶¶187, 200, unequivocally blasting this same construction of “SOI pillar” as “not supported by the intrinsic evidence” and “incomplete,” EX1003 ¶92, yet admitting he has “not seen any evidence that patent owner has taken that position.” EX2039 at 22:4-21. Yet Dr. Sechen acknowledged never offering an opinion under any construction of “SOI pillar” he thought was correct. EX2039 at 24:2-17; EX1003 ¶187 (Sechen: Ground 1C based on incorrect “apparent construction of ‘SOI pillar’”).

As the Board recognized for both grounds, that’s not good enough. *See* I.D. at 37 (Ground 1C did not demonstrate a reasonable likelihood “based on a claim construction Petitioner does not support and we do not adopt.”); I.D. at 38 (Ground 1D: same). Intel cannot meet its burden here by proffering claim constructions that it contends are wrong. *See id.*

D. Lee Did Not Disclose Memory Cells “Serially Connected Together” (Ground 1C | Claims 16-17)

Claims 16-17 should be confirmed over Ground 1C for the additional reason that the Petition never establishes Lee disclosed “two nonvolatile memory cells... serially connected together.” EX1001 at 12:44-52.

Ground 1C cross-references back to Ground 1A to show unpatentability. Pet. at 54 (citing § VII.A.2-VII.A.5). Ground 1A exclusively relies on Lee’s Figure 25A, saying “Figure 25A’s two memory cells are ‘serially connected together’” because they are electrically connected by “conductor layer M2”:

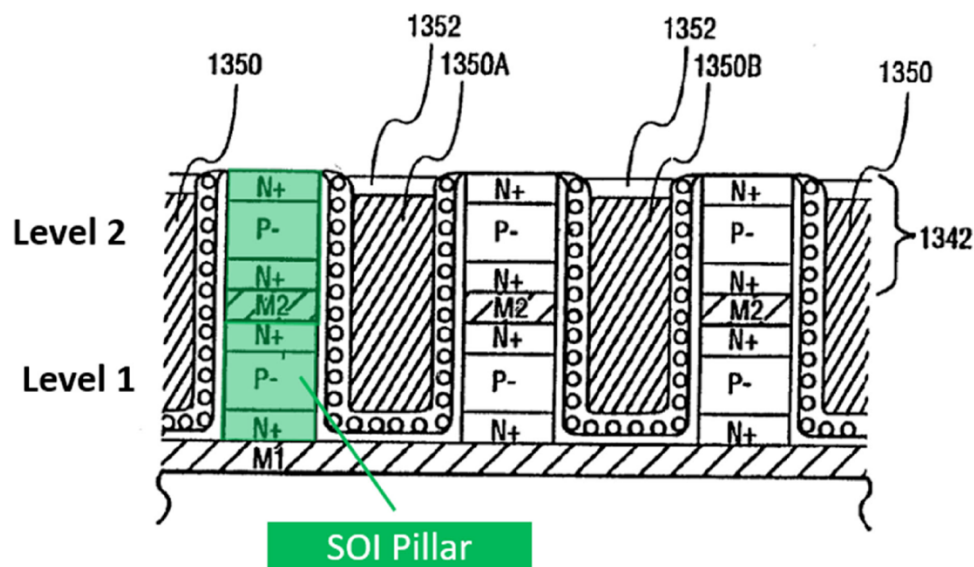


FIG. 25A

Pet. at 37-38 (Intel’s annotated figure); EX1003 ¶¶155-56, 159 (same).

Intel and Dr. Sechen’s declaration fundamentally misunderstand Lee’s architecture, and Dr. Sechen has now recanted. He conceded under cross-

examination that Lee's Figure 25A shows a NOR architecture. EX2039 at 59:17-60:7; EX2029 ¶¶98-100. As explained, NOR devices are not connected in series, source-to-drain, but instead are connected in parallel, source-to-source and drain-to-drain. EX2029 ¶108; *see also* EX2039 at 53:3-22 (Sechen: admitting that adjacent NOR transistors are not in series in EX2024); *supra* § II.C.

This is evident in Lee. Figure 25A is a cross-section of the three-dimensional NOR array shown in Figure 25B, where M1 (purple) runs along the page and M2 (orange) emerges from the page, perpendicular to M1:

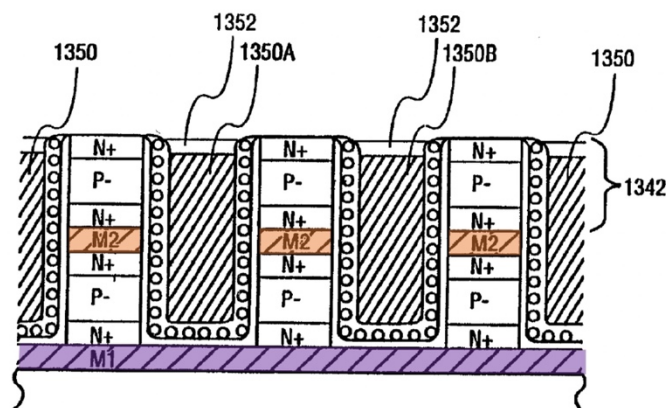


FIG. 25A

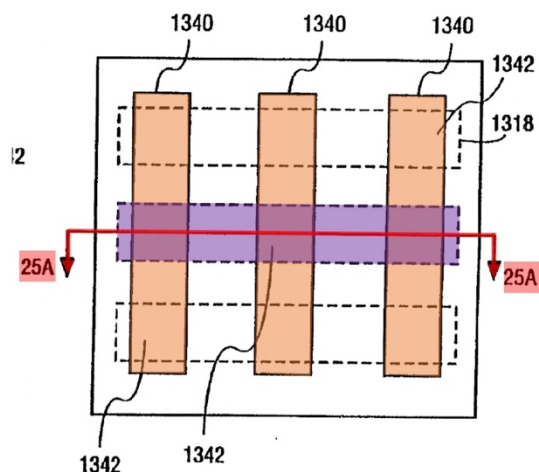


FIG. 25B

EX1007, Figs. 25A-25B (annotated), ¶¶157, 165; EX2029 ¶¶57, 99. Lee's multi-dimensional memory cells are also illustrated in Lee's single-cell conceptual drawings, for example Figure 2, where bit line 204 is oriented the same way as M1 and word line 210 runs the same way as M2:

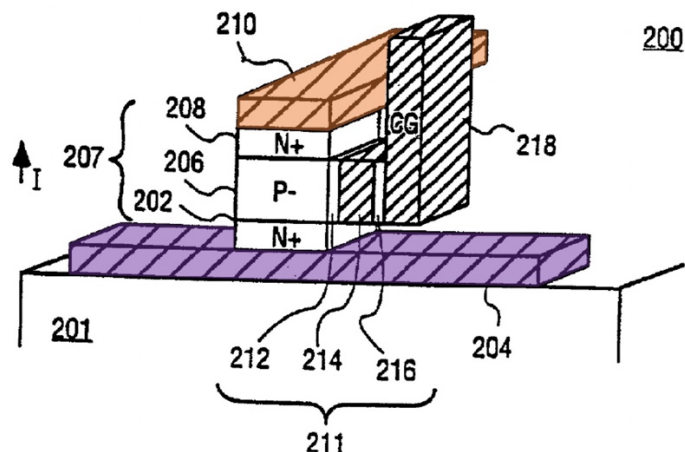


FIG. 2

EX1007 at Fig. 2 (annotated), ¶¶124, 126. In Lee, the M2 contact in Figure 25 does not mean the top-and-bottom NPN stacks are in series. EX2029 ¶¶98-100; *see also* EX2039 at 53:3-22 (Sechen: admitting that adjacent NOR transistors are not in series in EX2024 despite similar connections); EX2024 at Fig. 1.33.

Intel’s misunderstanding of its own proffered reference cannot sustain its burden to show that Claims 16-17 are unpatentable. *See, e.g., CIVIQ*, 2018 WL 4625764, at *7 (“misunderstanding of Heady’s disclosures [does] not adequately show[] that Heady discloses each limitation of claim 1”).

E. The Petition’s Cross-Referencing To Earlier Grounds With Incompatible Claim Constructions Lacks Particularity (Ground 1D | Claims 16-17)

Intel’s Ground 1D is a single paragraph. Pet. at 55. To assert unpatentability, the Petition cross-references its prior discussion of its Lee/Endoh and Lee/Kim

grounds. Pet. at 55 (citing Grounds 1B and 1C). Dr. Sechen’s declaration follows suit. *Compare* EX1003 ¶200 with Pet. at 55; *One World Techs. v. Chevron (HK) Ltd.*, PGR2020-00059, 2020 WL 7222691, at *16 (P.T.A.B. Dec. 7, 2020) (expert testimony that “merely parrots the words in the Petition... is entitled to little or no weight”); *Xerox*, 2022 WL 3648989, at *6; 37 C.F.R. § 42.65(a).

These assorted cross-references do not sustain Intel’s statutory requirement to establish unpatentability “with particularity.” 35 U.S.C. § 312(a)(3).

Grounds 1B and 1C each rely on a different set of proposed claim constructions for “stackable add-on layer” and “SOI pillar.” *Compare* Pet. at 41-42 with *id.* at 50. Yet the Petition provides nothing to decrypt which of these constructions it purports to rely on for Ground 1D, failing to provide BeSang with notice and an opportunity to respond. *Qualcomm v. Intel*, 6 F.4th 1256, 1262-63 (Fed. Cir. 2021) (APA violation where “claim construction was a moving target”); *see also Lyft v. Quartz Auto Techs.*, IPR2020-01450, 2021 WL 838289, at *6 (P.T.A.B. Mar. 4, 2021) (“Petitioner [must] set out its patentability contentions in a readily discernable way that does not require us to speculate” about claim construction.). The Board flagged a similar error for Ground 1E. *I.D.* at 42 (Petition’s claim construction positions “unclear”).

Further, even if Petitioner had met its burden in Grounds 1B-1C (it hasn’t), logic would not dictate that establishing obviousness based on A+B (Lee+Kim) and

A+C (Lee+Endoh) necessarily establish obviousness based on three A+B+C (Lee+Kim+Endoh). Those are different combinations, and the Petition provides no identification of how these three references would be combined, let alone how any resulting combination would satisfy all limitations of Claims 16-17. *Magnum Oil Tools*, 829 F.3d at 1380 (burden of demonstrating obviousness not met by conclusory argument that “the same analysis” for one combination of references applies to a different combination of references); *cf.* I.D. at 42 (Ground 1F: “[W]e are concerned that Petitioner’s cross-reference to other sections of the Petition may not be sufficient to support a challenge based on Lee, Aspar, and Endoh.”); EX2029 ¶¶135-38.

Intel’s mishmash of Ground 1D is insufficient and should be rejected.

F. This Ground Fails To Address All Claim Limitations (Ground 1D | Claims 16-17)

Ground 1D should be rejected for never establishing that Lee, Kim, and Endoh satisfy all the requirements of Claims 16-17, including the Claim 13 limitations from which they depend.

Here the Petition simply incorporates Lee/Endoh from Ground 1B to show obviousness based on Lee, Kim, and Endoh. *See* Pet. at 55 (citing Ground 1B). Ground 1B’s challenge to Claims 16-17 is that Lee “teaches claim 13’s limitations” and “Lee and Endoh teach claims 16 and 17’s additional limitations” for the

nonvolatile memory cells. *See* Pet. at 41-42. But to show obviousness of Claims 16-17 over Lee and Endoh, Intel needs to show the entirety of those claims are obvious over Lee *and* Endoh—including the additional limitations that Claims 16-17 incorporate from independent Claim 13. *See, e.g., Robotic Vision Sys. v. View Eng’g*, 189 F.3d 1370, 1376 (Fed. Cir. 1999) (“Claims 11 and 12 are dependent claims of claim 1 and are to be construed to incorporate by reference all the limitations of claim 1.”).

This is no mere oversight. As explained in Section VI.G, Intel asserts that one of skill would combine Lee’s NOR architecture with Endoh’s NAND design to arrive at the “memory cells” of Claims 16-17. But Claim 13 has its own requirements for those “memory cells,” EX1001 at 12:24-34, and the Petition never bothers addressing Claim 13 to show its proposed combination of Lee *and* Endoh satisfy Claim 13’s requirements as well, Pet. at 41-50; *Hartness Int’l v. Simplimatic Eng’g*, 819 F.2d 1100, 1108 (Fed. Cir. 1987) (“[W]e hold that the district court erred in failing to consider that dependent claim 3 included all the limitations of claim 1” in evaluating obviousness.). Ground 1D (and 1B) fails to meet its burden for this additional reason.

G. The Petition Provides No Motivation To Combine Lee’s NOR With Endoh’s NAND Design With Any Reasonable Expectation Of Success (Ground 1D | Claims 16-17)

Even if the Board finds Ground 1D’s cryptic cross-referencing and incomplete theories are adequate, *supra* § VI.E-F, it still fails to show a motivation to combine Lee, Kim, and Endoh. Ground 1D cites back to Ground 1B to assert a motivation to combine Lee and Endoh. Pet. at 55. But Intel fails to meet its burden because it shows no motivation to combine Lee’s NOR device with Endoh’s fundamentally incompatible NAND memory, particularly when doing so could result in a four-times reduction in Lee’s memory cell density. EX2029 ¶¶104-11, 135-38.

Ground 1B points to Endoh’s Figures 1171 and 1172 from Production Example 52, asserting that one of skill “would have been motivated to modify Lee’s device level 3104 in array 3101 to incorporate two memory cells on each pillar as taught in Endoh.” Pet. at 46-47. In the same paragraph, Intel acknowledges that “Lee itself” already taught a “memory structure with two memory cells on each pillar.” Pet. at 47. Intel asserted that Lee and its “two memory cells” met all the limitations of Claims 16-17 all by itself in Ground 1A, *see* Pet. at 37-41, yet one sub-ground later, Intel changed course to assert one of skill would be motivated to replace Lee’s “two memory cells” with Endoh’s “two memory cells” without providing any reason why, *id.* at 47-48. Dr. Sechen’s repetitive opinion provides no further

illumination. *Compare* Pet. at 47-48 with EX1003 ¶¶177-80; *One World*, 2020 WL 7222691, at *16 (parroting testimony entitled to “little or no weight”).

Indeed, Lee showed four control gates on a single memory cell: 1332A-B and 1350A-B. EX2029 ¶59; EX1007 ¶166, Fig. 26 right). Switching out two of Lee’s memory cells for two of Endoh’s memory cells would result in up to a four-fold reduction

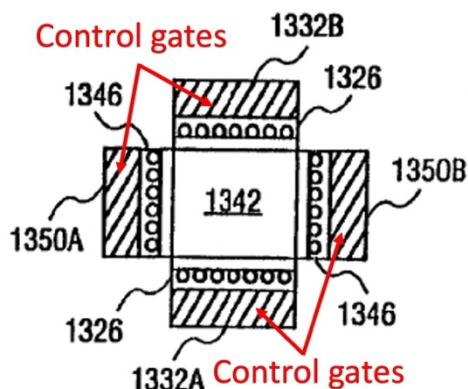


FIG. 26

in density. *See id.* The Petition was required to articulate some reason to depart from Lee’s existing design to Endoh’s less-dense design. *Nuvasive*, 842 F.3d at 1384; *Microsoft*, 2018 WL 1997727, at *6 (“Petitioner does not explain why a skilled artisan would have modified Korhonen to include Westerman’s feature... when Korhonen already provides” that feature.); *Sony*, 2019 WL 1581942, at *5. Lacking one, the Petition instead recites the adage that its “combination merely amounts to using a known technique... to improve a similar known device... in the same way....” Pet. at 47. Even if true, asserting that one of skill *could* have made the combination is legally insufficient. *See, e.g., Hewlett Packard Enter. v. K.Mizra*, IPR2022-00843, 2022 WL 16556406, at *7 (P.T.A.B. Oct. 31, 2022) (petitioner must “show that the artisan *would* have made the combination” (emphasis in original)).

One of skill would have had ample reason *not* to modify Lee’s “two memory cells” in Figure 25A. Not only would it have reduced Lee’s density, but Endoh’s “two memory cells” in Figures 1171-72 were fundamentally incompatible. EX2029 ¶¶109-11. There’s no dispute that Lee’s Figure 25A shows a parallel NOR architecture. EX2039 at 59:17-60:7; EX2029 ¶¶98-100; *supra* § VI.D. Even if this were not self-evident, Micron’s first-filed petition apprised that Lee was a NOR device. IPR2023-00900, Paper 1 at 62 (Micron: Lee’s “memory arrangement is known as the NOR Virtual Ground (NVG) Array.”). Everyone also agrees that Endoh’s Figures 1171-72 memory cells use serially-connected NAND cells. EX2039 at 124:4-19 (Sechen: admitting Figures 1171-72 show a NAND memory configuration); EX1012 ¶1206 (Endoh: “the transistors are connected in series... as shown in FIG. 1171 and FIG. 1172”); EX2029 ¶¶107-08. Yet the Petition skirts past this glaring NOR/NAND incompatibility without ever addressing it. *See* Pet. at 46-47.

Intel and Dr. Sechen never explain how or why one of skill would have transformed Lee’s parallel NOR memory into a NAND architecture, let alone while maintaining Lee’s density. Pet. at 41-48, 55; EX1003 ¶¶170-81, 200. Its conclusory statements that combining Lee and Endoh amounted to little more than a “known technique” is plainly insufficient considering their actual, diverging architectures. *See* Pet. at 47-48; *see, e.g., Hilti v. Milwaukee Elec. Tool*, IPR2015-01166, Paper 81

at 18 (P.T.A.B. Nov. 14, 2016) (“Petitioner does not provide adequate specific reasoning as to why one of ordinary skill in the art would have been led to modify Takano to connect cells in parallel when Takano clearly discloses a series connection.”). Lee used a unique pillar design, EX2029 ¶¶50-61, 105-06, and nonvolatile NAND and NOR memory devices have distinct architectures. EX2043 at 1:29-63; EX2029 ¶¶108-11. They use incompatible data flows, bit lines, sensing amplifiers, read and write protocols, and control circuitry. EX2029 ¶¶110-11.

The Petition goes on to declare a reasonable expectation of success in combining Lee and Endoh. Pet. at 48 (citing EX1003 ¶180). Sechen’s supporting analysis doesn’t explain how to combine them, or even acknowledge the distinctions between Lee’s unique NOR pillars and Endoh’s NAND serial design. See EX1003 ¶180. Failing to provide “specific evidence” is insufficient to meet Intel’s burden to show any reasonable expectation of success in combining semiconductor designs. See, e.g., *Samsung*, 925 F.3d at 1382-83.

Because memory cell logic design, layout, and architecture are intimately intertwined, modification of the memory cells or design routinely results in an overhaul of the layout and chip architecture. EX2029 ¶¶110-11. One of skill cannot simply swap out NOR memory cells for NAND cells. EX2029 ¶¶107-11; *Microchip Tech. v. HD Silicon Sols.*, IPR2021-00872, 2021 WL 6339555, at *7 (P.T.A.B. Dec. 15, 2021) (Petitioner did not “provide persuasive explanation as to how either

reference would be modified to accommodate the distinct architecture of the other reference... in a combination.”). This is not a small tweak—it would require building an entirely new chip from the ground up. EX2029 ¶¶110-11; *Hilti*, IPR2015-01166, Paper 81 at 18. One of skill would confront a cascading list of modifications to the entire memory device, including: redesigning the pillars, control gates, routing paths, bit lines, command interface, control logic, sense amplifiers, address decoders and voltage generators, as explained by Dr. Przybylski. EX2029 ¶¶110-11. But Intel never explains how one of skill reasonably would accomplish it. *MobileMedia*, 780 F.3d at 1167-68 (no motivation if combination “beyond the technical ability of a skilled artisan”).

Absent the required showing of any motivation to combine Lee and Endoh, let alone with any reasonable expectation of success, Claims 16-17 should be confirmed.

VII. THE PETITION DOES NOT MEET ITS BURDEN TO SHOW OBVIOUSNESS BASED ON LEE AND ASPAR (GROUNDS 1E-1F)

The Board also ordered trial to address Claim 13 over the Lee/Aspar combination. I.D. at 41. Grounds 1E-1F are a rinse-and-repeat of the Lee/Kim grounds: asserting Lee alone meets the claim except for 13[c], where Intel proposes swapping out Lee’s interleaved deposited levels for Aspar’s Smart-Cut stacking method. Pet. at 55-63. Intel fails to meet its burden to show one of skill would have

done such a thing. Plus, Aspar is plainly a non-starter because it instructs annealing the wafers at 1100°C, far exceeding the device’s thermal budget.

A. Intel Does Not Establish A Motivation To Combine Lee With Aspar (Grounds 1E-1F | Claims 13-17)

Intel also does not meet its burden to show that a skilled artisan would have departed from Lee to use Aspar’s stacking technique. Intel never shows: (1) Aspar’s stacking was compatible with Lee’s interleaved levels, and (2) deploying Aspar’s high-temperature Smart-Cut that risked an inoperable device was desirable.

1. The Petition Fails To Show A Motivation To Stack Lee’s Interleaved Levels

Grounds 1E-1F recycle the same pretext that Lee’s Figure 35 purportedly did not “clearly describe” how to form layer 3104 on insulating layer 3102. Pet. at 56. As explained, the Board correctly found that Lee taught that layer 3104 was deposited, and even Dr. Sechen could not maintain the pretense. *Supra* § VI.A.1.; I.D. at 35; Pet. at 56; EX2039 at 88:2-89:6; EX1007 ¶107; EX2029 ¶¶142-43. As with Lee/Kim, Intel also fails to show one of skill would be motivated to replace Lee’s deposited, interleaved levels with Aspar’s stacked layers. EX2029 ¶¶119-24, 144. Grounds 1E-1F may be rejected for these reasons alone.

2. One Of Skill Would Not Risk Applying Aspar's High-Temperature Annealing To Lee

The Petition argues at length that one of skill would discard Lee's sequential deposition in favor of stacking layers using Aspar's Smart-Cut. Pet. at 55-63. This is implausible.

Aspar is an academic study, examining "homogenous thin film transfer[s]" onto other wafers using Smart-Cut. EX1009 at 839. Indeed, Aspar's research doesn't depict any of its thin films containing any transistors or devices fabricated in its layers. *E.g.*, EX1009 at Figs. 12-16; EX2029 ¶¶160-61.

Intel's Exhibit 1015 indisputably describes the same Smart-Cut process used in Aspar. EX2039 at 118:10-119:2.

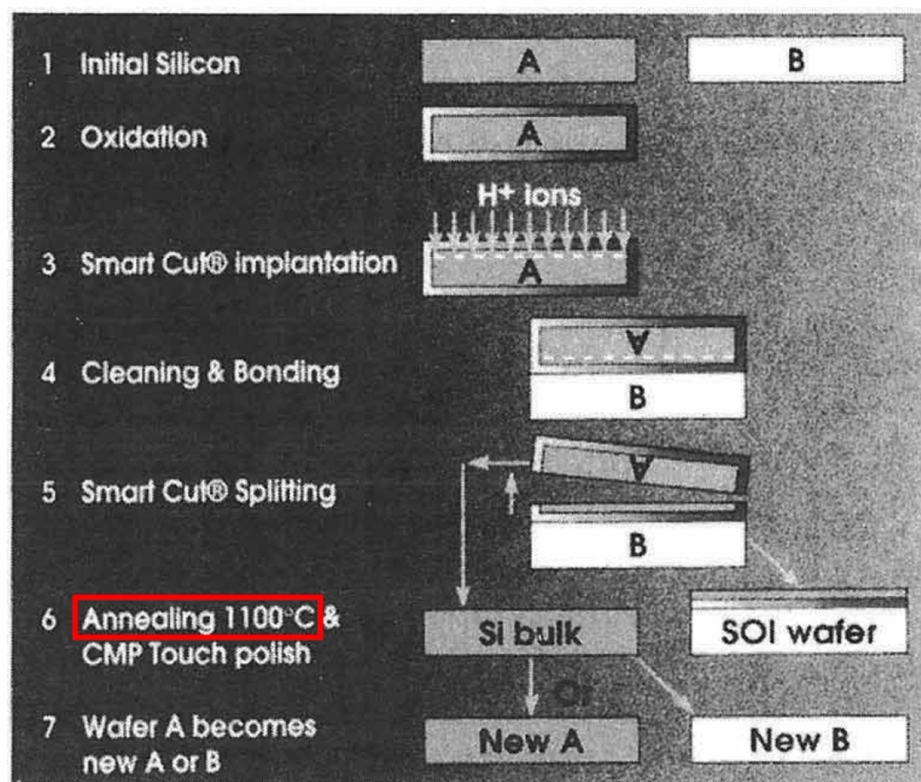
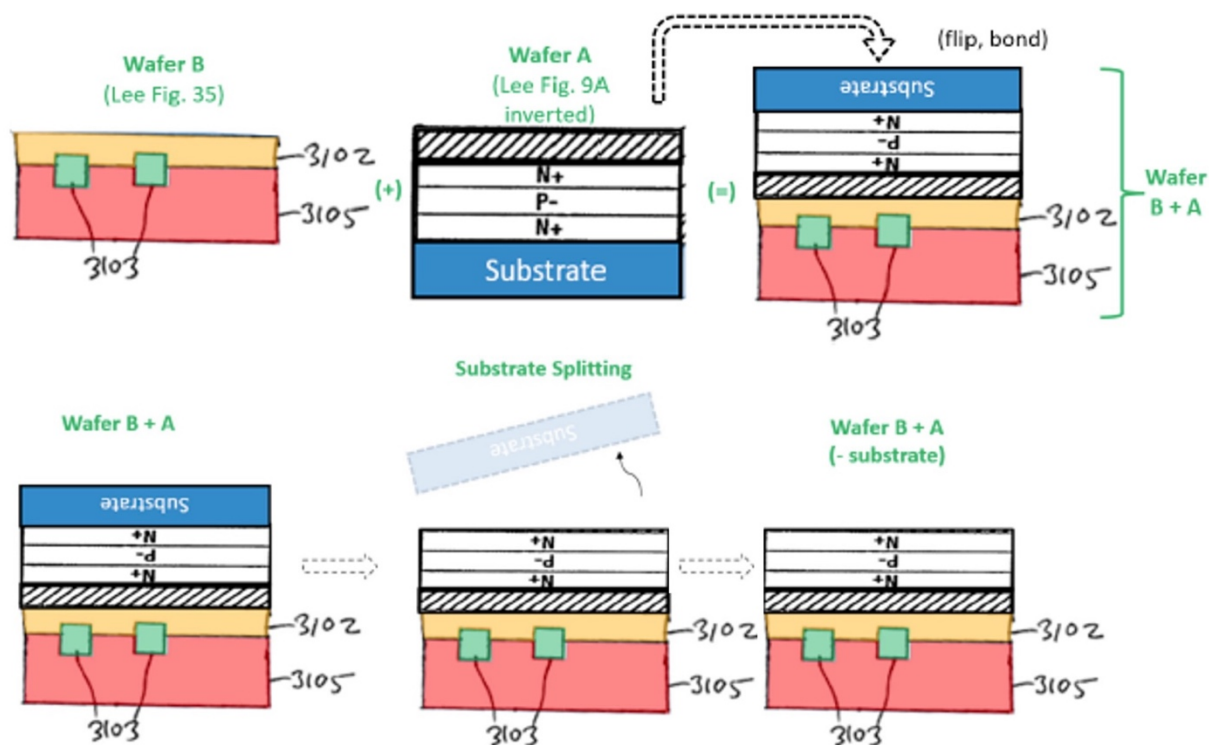


Fig. 11-24 Process flow for fabricating Smart-Cut® wafers.

It describes and depicts how Smart-Cut taught that “[b]oth wafers are then annealed at 1100°C to remove defects” after the splitting step. EX1015 at 543-44, Fig. 11-24 (annotated); *see also* EX1014 at 260-61 (same), Fig. 7-29; EX1003 ¶¶46-47 (citing EX1014-1015); EX2029 ¶148. Dr. Sechen acknowledged this fact both in his declaration and at deposition. EX1003 ¶46; EX2039 at 121:8-11 (“Q. So figure 11[-]24, which you put in your declaration shows that annealing step at 1100 degrees Celsius; correct? A. Yes.”); *see also id.* at 117:17-121:11.

Here Intel and Dr. Sechen purport to apply Smart-Cut by first sectioning Lee's substrate onto Wafer B and its stacked layers onto Wafer A, then bonding them and splitting off Wafer A's substrate (blue):

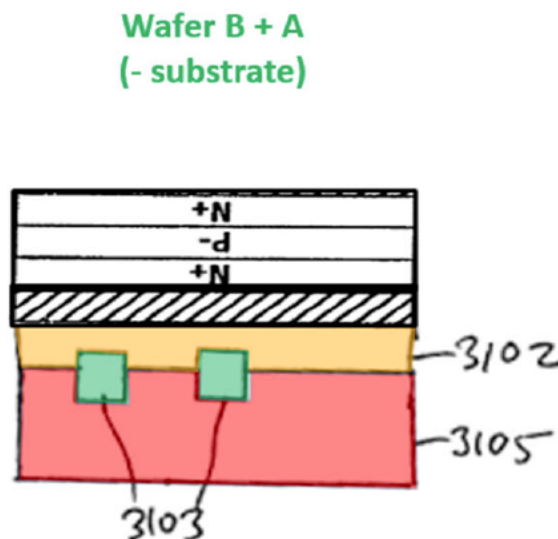


Pet. at 58-60 (citing EX1003 ¶¶209-11). The Petition analogizes this process to “making a layer cake” where “each layer is baked individually.” Pet. at 10-11. Unfortunately, Smart-Cut teaches overbaking the cake. See Pet. at 59-60.

Smart-Cut was a non-starter applied to Lee's memory: its high-temperature annealing of both wafers at 1100°C after splitting risked frying Lee's device. EX2029 ¶¶148-52. There's no doubt that a skilled artisan in 2004 knew that transistors were subject to a thermal budget constraining subsequent high-

temperature processing steps. EX2039 at 102:12-103:3; EX2029 ¶¶150-51; *see also* EX2039 at 99:12-100:5, 102:7-11. But Aspar's Smart-Cut blew well past the budget.

According to Intel and Dr. Sechen, the combined Wafer A+B contains Lee's control circuitry (driver circuits 3103, which Intel colors green). Pet. 58-60; EX1003 ¶209. Subjecting Lee's control circuitry to Smart-Cut's annealing was certainly a no-no, EX2028 at 123:13-124:7, 125:6-126:7, and also risked further



diffusion of the doped ions in the NPN stacks from Figure 9A, degrading their function away from their design parameters, EX2029 ¶152; EX2039 at 101:15-102:6, 99:12-100:5, 102:12-103:3. A skilled artisan knew to keep subsequent processing at lower temperatures—less than 650°C. EX2029 ¶151; EX2027 at 715. In fact, the '702 Patent expressly teaches this low-temperature processing. EX1001 at 7:15-35.

Scorching Lee's device does not meet Intel's burden to show a motivation to combine for Grounds 1E-1F. EX2029 ¶¶148-52, 162; *Redline Detection v. Star Envirotech*, 811 F.3d 435, 453 (Fed. Cir. 2015) (no motivation to combine where

result “can damage closed EVAP systems with volatile compounds”); *Streck v. Ravgen*, IPR2021-01577, Paper 62 at 87 (P.T.A.B. Apr. 18, 2023).

3. “Quality Control” and “Less Waste” Provide No Reason To Switch to Aspar

As with Lee/Kim, the Petition also invokes better “quality control” and “minimizes waste” as motivations to adopt Aspar’s Smart-Cut stacking technique, Pet. at 61-62, but Aspar shows these rationales are unsupported.

First, Aspar’s stacking technique would not improve Lee’s quality control. EX2029 ¶145. According to Intel, one of skill using Smart-Cut would put Lee’s Figure 9A stack into Wafer A. Pet. at 59; EX1003 ¶209. But there would be nothing to test “on the stack prior to bonding,” Pet. at 61 (citing EX1003 ¶213), because the memory devices haven’t been formed yet, EX2029 ¶145. Dr. Sechen conceded that before stacking, Lee’s Figure 9 in Wafer A is just an unpatterned wafer with no memory devices. EX2039 at 90:5-20. Dr. Sechen and Intel concede that the memory devices are made *after* Wafer A is attached to the substrate. EX2039 at 90:21-91:15; Pet. at 60 (Intel: “After bonding, the individual memory cells in [Lee’s] level 3104 would be fabricated...”); EX2029 ¶145. Aspar’s academic study is no help—it also shows transferring unpatterned wafers. EX1009 at Figs. 12-16; EX2029 ¶145.

Intel’s second rationale that Smart-Cut would reduce waste also withstands no scrutiny. Pet. at 61-62. Smart-Cut’s annealing at 1100°C only risked burning

Lee's device, resulting in far more waste than Lee's tried-and-true deposition technique. EX2029 ¶¶145; EX1007 ¶107.

B. No Reasonable Expectation Of Success For Combining Lee With Aspar (Grounds 1E-1F | Claims 13-17)

One of skill would have had no reasonable expectation of success deploying Aspar's Smart-Cut in Lee.

First, as previously explained, the Petition provides no explanation how Lee's interleaved levels could be pulled off using Aspar's stacking. *Supra* § VII.A; EX2029 ¶¶119-24, 144. We can stop here.

Second, one of skill would have recognized that Aspar's high-temperature annealing would ruin Lee's device. *Supra* § VII.A.2; EX2029 ¶¶148-52, 157-59. Or we can stop there.

Third, Intel takes Aspar far beyond its limited teachings to a fantasy realm. Aspar was an academic article that simply described transferring thin films. EX1009 at 839; EX2029 ¶¶153-62.

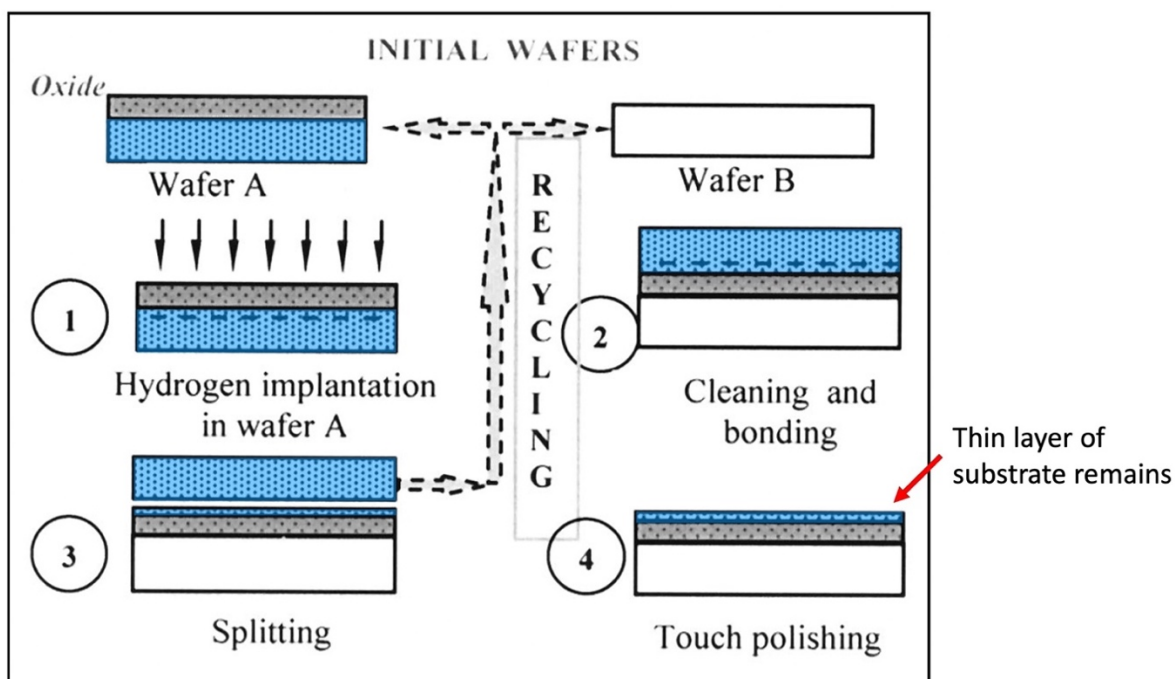


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

As shown above, and confirmed by Dr. Sechen, Smart-Cut’s step 4 indisputably left a thin film remaining, EX1009 at Fig 1; EX2039 at 68:19-73:21 (Sechen: “you get a thin silicon layer on top of the oxide” remaining after splitting and polishing), and Intel never explains how to avoid that thin layer of monocrystalline Si that would obstruct Lee’s upper metal contact (M2 in Lee’s Fig. 25A). EX2029 ¶¶146-47, 153-56.

Intel omits the annealing and Si layer in its hypothetical application of Smart-Cut to Lee. In the complicated field of semiconductors, Intel needs to provide “specific evidence” justifying its significant departures and extensions from Aspar’s actual disclosure. *Samsung*, 925 F.3d at 1382-83. Proposing a vague idea divorced

from the complexities is unreasonable, and certainly doesn't meet Intel's burden here.

C. The Petition's Ambiguous Construction Of "SOI Pillar" Does Not Establish Unpatentability (Ground 1E | Claims 14-17)

Claims 14-17 should be confirmed over Ground 1E because neither the Petition's one-paragraph argument, nor its citation to Dr. Sechen, specifies the construction of "SOI pillar" it applies. Pet. at 63; EX1003 ¶217. The Board flagged this ambiguity at institution. I.D. at 42. Indeed, the Ground simply refers back to its Ground 1A asserting obviousness based on Lee alone, Pet. at 63 (citing Pet. § VIII.A.2-5), and based on a claim construction that Intel and Dr. Sechen condemn as "incorrect," Pet. at 16; EX1003 ¶92, even though Dr. Sechen has seen no evidence that BeSang has adopted such a construction, EX2039 at 22:4-21.

The Board also found that Petitioner never explained how Lee/Aspar taught an "SOI pillar" under Intel's construction, I.D. at 42, which Dr. Sechen confirmed, EX2039 at 24:2-17 (Sechen: no offered opinion of obviousness for Claims 13-17 over Lee if "SOI pillar were construed in the manner you believe is correct").

Here Intel cannot establish its challenge with particularity. *See* Pet. at 63; 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(3)-(4). Even if this ground were not hopelessly unclear, proffering an opinion based on a construction of "SOI pillar" that both it and its expert reject cannot sustain its burden. *Xerox*, 2022 WL 3648989,

at *6; *One World*, 2020 WL 7222691, at *16. Claims 14-17 should be confirmed for this additional reason.

D. Lee Did Not Disclose Memory Cells “Serially Connected Together” (Ground 1E | Claims 16-17)

Claims 16-17 require memory cells that are “serially connected together,” EX1001 at 12:44-52, and the Petition cross-references back to Ground 1A’s argument that Lee’s Figure 25A showed a serial connection, Pet. at 63 (cross-referencing Pet. § VII.A.4-5). But Lee’s Figure 25A instead shows a NOR architecture with parallel memory cells. *Supra* § VI.D; EX2039 at 59:17-60:7; EX2029 ¶¶98-100. Claims 16-17 should be confirmed patentable for the same reasons.

E. The Petition’s Cross-Referencing To Grounds With Conflicting Claim Construction Positions Lacks Particularity (Ground 1F | Claims 16-17)

The entirety of Ground 1F alleging obviousness based on Lee, Aspar, and Endoh is a single page of impenetrable cross-referencing to Grounds 1B and 1E that is inadequate to meet Petitioner’s burden. *See* Pet. at 64. The Board expressed “concern[] that Petitioner’s cross-referenc[ing] may not be sufficient to support” the challenge. I.D. at 42 (citing *Magnum Oil*, 829 F.3d at 1380). Its concern is well grounded.

First, Grounds 1B and 1E rely on conflicting sets of proposed constructions for both “stackable add-on layer” and “SOI pillar.” *Compare* Pet. at 41-42 *with id.*

at 55. Again, neither the Petition nor Dr. Sechen provide any guideposts to discern which constructions Intel relies on for Ground 1F. Pet. at 64 (citing EX1003 ¶¶218-19). As explained for Ground 1D, this ambiguity does not sustain Intel’s burden. *Supra* § VI.E; *Qualcomm*, 6 F.4th at 1262-63; *Lyft*, 2021 WL 838289, at *6.

Second, Ground 1F asserts Claims 16-17 are satisfied based on earlier “description[s] of” combinations of subsets of references: the “Lee-Endoh combination” in 1B and “Lee-Aspar” in 1E. Pet. at 64 (citing EX1003 ¶¶218-19). Dr. Sechen says the same and adds nothing here explaining how the three references would be combined by one of skill. *Compare* EX1003 ¶¶218-19 with Pet. 64; *Xerox*, 2022 WL 3648989, at *6; *One World*, 2020 WL 7222691, at *16; EX2029 ¶¶163-66. Again, obviousness based on A+B (Lee+Aspar) and A+C (Lee+Endoh) is not the same combination as Ground 1F’s A+B+C combination. *Supra* § VI.E; *Magnum Oil Tools*, 829 F.3d at 1380.

F. This Ground Fails To Address All Claim Limitations (Ground 1F | Claims 16-17)

As explained in Ground 1D, this ground should be rejected for never establishing that Lee, Aspar, and Endoh satisfy all the requirements of Claims 16-17, including the limitations of Claim 13. *See* Pet. at 64; *supra* § VI.F.

G. The Petition Provides No Motivation To Combine Lee, Aspar, And Endoh With Any Reasonable Expectation Of Success (Ground 1F | Claims 16-17)

Ground 1F also exclusively relies on Ground 1B to supply a motivation to combine Lee and Endoh for Claims 16-17. Pet. at 64. As explained in Ground 1D, the Petition supplies no motivation to replace Lee’s dense NOR matrix with two memory cells from Endoh’s fundamentally incompatible NAND architecture. *Supra* § VI.G; EX2029 ¶¶104-11, 163-66. Intel cannot sustain Ground 1F either.

VIII. THE PETITION DOES NOT MEET ITS BURDEN FOR THE GROUNDS 1A-1B CHALLENGES BASED ON LEE

Grounds 1A-1B based on Lee did not survive institution, and these additional arguments only confirm the challenged claims should be sustained over them.

A. The Petition Improperly Argues Unpatentability Under Claim Constructions For “Stackable Add-On layer” And “SOI Pillar” It Claims Are Incorrect (Ground 1A-1B | Claims 13-17)

The Board correctly found that Ground 1A cannot meet its burden because Intel and its expert relied on a construction of “stackable add-on layer” which they assert is incorrect. *See* I.D. at 28-29; Pet. at 12-13, 16. Dr. Sechen exclusively relied on an assumed claim construction of “stackable add-on layer” that he thought was “incorrect,” despite having seen no evidence BeSang would adopt it. EX2039 at 16:14-17:13, 24:2-7; EX1003 ¶¶84, 93. He confirmed he never offered any opinions under a construction he “believes is correct.” EX2039 at 24:2-17.

Grounds 1A and 1B have the same problem for “SOI pillar.” Pet. at 16; EX1003 ¶¶92-93; EX2039 at 22:4-21, 22:22-24:17; *supra* § VI.C. As the Board recognized in Ground 1B, Intel cannot meet its burden based on a claim construction that Intel and its expert argue are incorrect. I.D. at 29. The Board should confirm patentability over Grounds 1A-1B. *Hologic*, 2018 WL 1897623, at *3-4; *Ebates*, 2022 WL 5048425, at *5; POPR at 29-33.

B. Lee Did Not Disclose Memory Cells “Serially Connected Together” (Ground 1A | Claims 16-17)

Again, Ground 1A incorrectly asserts that Lee’s Figure 25A has serial memory cells. EX1001 at 12:44-52; Pet. at 37-39. Lee’s NOR array doesn’t, which takes out this challenge too. *Supra* § VI.D; EX2029 ¶¶98-101.

C. The Petition Provides No Motivation To Combine Lee And Endoh, Let Alone A Reasonable Expectation Of Success (Ground 1B | Claims 16-17)

Again, Ground 1B argues Claims 16-17 are obvious by replacing Lee’s “two memory cells” with Endoh’s “two memory cells.” Pet. at 46-48. This argument again fails and unravels this challenge too. *Supra* § VI.G; EX2029 ¶¶104-12.

D. This Ground Fails To Address All Claim Limitations (Ground 1B | Claims 16-17)

As explained in Ground 1D, this ground should be rejected for never establishing that Lee and Endoh together satisfy all the requirements of Claims 16-17, including the limitations of Claim 13. *See* Pet. at 41-50; *supra* § VI.F.

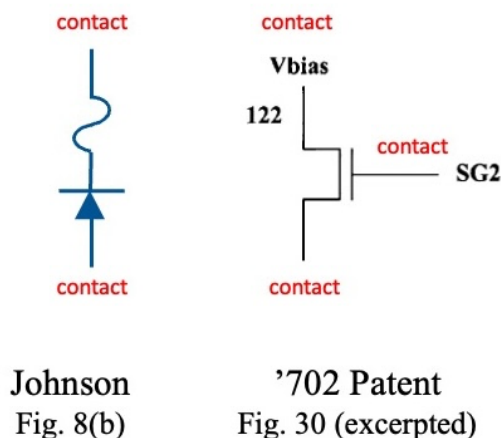
**IX. THE PETITION DOES NOT MEET ITS BURDEN TO SHOW
OBVIOUSNESS BASED ON JOHNSON AND KIM (GROUND 2B)**

The Board ordered trial to consider the Johnson/Kim and Johnson/Aspar combinations challenging only Claim 13 in Grounds 2B-2C. None of these grounds should be sustained.

A. Johnson Does Not Disclose Or Suggest “Memory Cells Having At Least One Transistor” (Claim 13)

Johnson’s diode memory does not establish obviousness of Claim 13[d]’s requirement of “nonvolatile memory cells having at least one transistor.” EX1001 at 12:33-34.

As previously explained, Johnson taught a unique field-programmable NOR memory design that used 2-terminal devices. *See* § II.G; EX2029 ¶¶81-82, 168. Johnson’s 2-terminal design allowed a specific, self-aligned architecture where memory cells were etched from the conductors above it, EX1010 at 11:42-51. According to Johnson, his design was much denser and easier to manufacture than field-programmable memories using transistors. EX1010 at 2:38-52, 6:23-24. Johnson’s 2-terminal memory cell consisted of (1) a diode to steer the current in one direction with (2) an antifuse to store data (0 or 1). EX1010 at 5:41-65, Fig. 8(b).



As illustrated above, Johnson’s 2-terminal diode/antifuse memory is distinct from the transistor memory cell taught by BeSang’s ’702 Patent. EX2029 ¶168.

The Petition relies on Johnson’s description of its “steering element” circuitry that mentions seven diodes, plus a JFET or MOSFET, as potential options to steer current. Pet. at 72-73 (citing EX1010 at 5:41-49, 7:61-8:5); *id.* at 77. The experts agree that’s all Johnson says about transistors in the steering element, EX2039 at 103:4-21, 105:6-12; EX2029 ¶169, but Intel disregards Johnson’s actual teachings.

Johnson explains exactly how to use the diodes, JFET, or MOSFET in the steering element. All (*including* the JFET and MOSFET) are being used as 2-terminal devices, not a 3-terminal implementation. See EX1010 at 5:41-43, 7:44-47, Fig. 8(b); EX2029 ¶169. Johnson actually says:

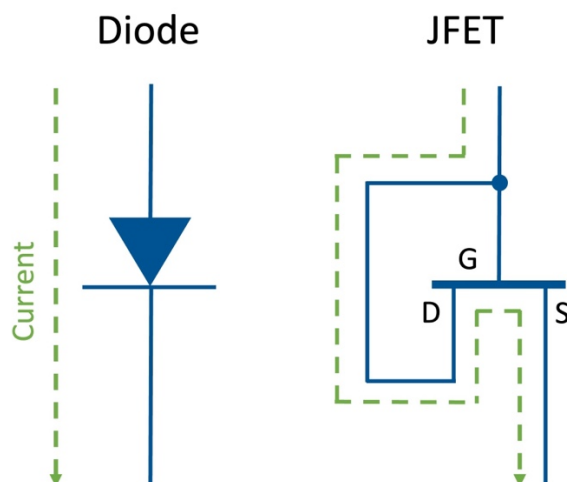
Some possible implementations of the steering element are

- (i) a PN junction diode...;
- (ii) a metal-semiconductor Schottky diode;

- (iii) a *junction field-effect transistor* with gate connected to source (or to drain);
- (iv) a *MOSFET* with gate either floating, or connected to source or connected to drain;
- (v) a Zener diode, avalanche diode, or tunnel diode;
- (vi) a four-layer diode (SCR);
- (vii) a P-I-N diode....

EX1010 at 7:58-8:5 (emphases and formatting added).

Johnson does not disclose separately connecting the control gate in the JFET or MOSFET steering element and using it like a 3-terminal device. *See id.*; EX2029 ¶171. Instead, Johnson says the JFET’s “gate [is] connected to source (or to drain),” EX1010 at 7:65-66, to make it a 2-terminal device, EX2029 ¶¶170-73. But that simply results in the JFET operating as a “current regulator diode” that typically passes near-constant current in only one direction. EX2029 ¶¶174-77; EX2045 at 166-70. As shown below, Johnson teaches wiring the JFET to act as a diode, not a transistor:



EX2029 ¶174.

Johnson’s MOSFET steering element fares no better. Again, Johnson describes a 2-terminal “MOSFET with gate either floating, or connected to source or connected to drain.” EX1010 at 7:66-8:1. Unlike an asymmetrical diode, a MOSFET is a symmetrical device that passes current in either direction when the channel is active. EX2029 ¶179. If the gate were connected to the drain, then the MOSFET could act, at best, as a weak diode, not a transistor. EX2029 ¶179. But the MOSFET with a “floating” gate would be nonfunctional in Johnson’s design because it would operate as either a wire or open circuit, depending on the type of MOSFET. EX2029 ¶178.

Simply put, Johnson’s exclusive teaching of 2-terminal memory cells does not disclose or render obvious “nonvolatile memory cells having at least one transistor” required by Claim 13. Nor to the extent it discloses them does it enable the use of a

transistor in its design. EX2029 ¶¶178 (MOSFET would be “inoperable”), 184 (JFET requires “undue experimentation”), 186 (MOSFET requires “undue experimentation”), 189 (transistors require “undue experimentation”); *Raytheon Techs. v. Gen. Elec.*, 993 F.3d 1374, 1380 (Fed. Cir. 2021).

Johnson’s own criticisms taught away from using transistors. *DePuy Spine v. Medtronic Sofamor Danek*, 567 F.3d 1314, 1327 (Fed. Cir. 2009). Unlike his diode design, Johnson was critical of existing field-programmable memories that used transistors. EX2029 ¶180; EX1010 at 2:6-20. He explained transistor-based designs, EX1010 at 2:28-32, added the complexity of “more than one circuit element” and “consume extra silicon area.” EX1010 at 2:12-18. Thus “these devices have generally suffered from lower density and higher cost” than mask ROMs. EX1010 at 2:25-27; *see also id.* at 1:54-56. They also required “a number of sequential photolithographic steps” to form the memory cells which resulted in alignment problems that further reduced density. EX1010 at 2:38-40; *see also id.* at 2:40-3:12. These transistor memory cells also “allow[ed] only very limited integration vertically into the third dimension.” EX1010 at 2:28-36.

Simply put, using more complex 3-terminal transistor memory cells was not obvious because Johnson himself criticized them. *See DePuy*, 567 F.3d at 1327 (reference teaches away and does not establish obviousness if it teaches away by

“criticiz[ing], discredit[ing], or otherwise discourag[ing] investigation into the invention claimed” (citation and internal quotation marks omitted)).

B. One Of Skill Would Not Have Been Motivated To Modify Johnson’s Diode Design With Any Reasonable Expectation Of Success (Claim 13)

One of skill also would not have been motivated to modify Johnson’s diode architecture to include memory cells with transistors, let alone with any reasonable expectation of success. EX2029 ¶¶180-89.

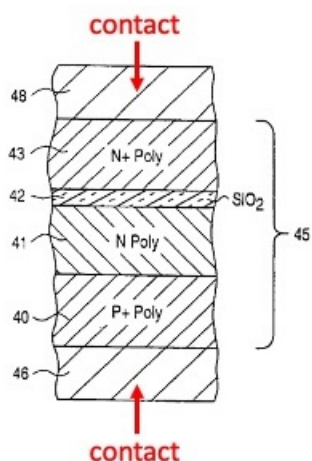
As explained in the prior section, Johnson taught away from using transistor memory cells. *Supra* § IX.A; EX2029 ¶¶168-80; EX1010 at 1:54-56, 2:6-3:12. Even if it hadn’t, one of skill would not have been motivated, with any reasonable expectation of success, to replace Johnson’s diode pillar with a 3-terminal transistor. *Polaris Indus. v. Arctic Cat*, 882 F.3d 1056, 1069 (Fed. Cir. 2018) (remanding IPR decision to consider teaching away because “even if a reference is not found to teach away, its statements regarding preferences are relevant to a finding regarding” motivation to combine); EX2029 ¶¶181-89.

Johnson focused on the design and implementation of memory pillars with a diode “steering element” having “a strongly asymmetric current-versus-voltage characteristic; it conducts more readily in one direction than in the other.” EX1010 at 5:50-54, Fig. 8(b). Figures 6(a)-6(g) taught fabricating its pillars using a “PN junction diode.” EX1010 at 11:59-67, 12:42-43, Figs. 6(a)-6(g). Johnson’s pillar

shown in Figure 6(a) just had contacts 46 and 48 on the bottom and top of its vertical pillar “form[ing] a PN junction diode (the steering element), and [an] antifuse.”

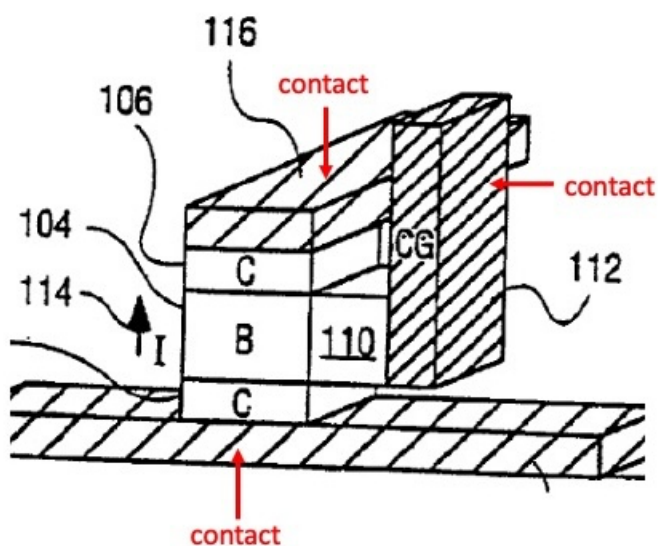
EX1010 at 12:1-12; EX2029 ¶187. Figure 6(a) never showed gates or the additional contacts needed to wire a 3-terminal transistor memory cell as, for example, in Lee.

EX1010 at 12:1-41, Fig. 6(a); EX2029 ¶187. The difference is striking:



Johnson's diode

Fig. 6(a) (excerpted, annotated)



Lee's transistor

Fig. 1A (excerpted, annotated)

Not only does Johnson omit this extra wiring, the foundation of his design is a streamlined pillar with minimal top-and-bottom contacts. EX1010 at 11:22-67; EX2029 ¶188. Unlike Lee, Johnson’s diode design dispensed with any gates or wiring alongside his pillars to simplify deposition and increase memory cell density. EX1010 at 11:22-25; Figs. 4(a), 6(g); EX2029 ¶188. He used the contacts to self-align and etch the pillar underneath, and in his words, this “makes stacking especially simple and flexible” and generated the structure in Figure 6(g) (right). EX1010 at 11:21-24, Figs. 6(a)-6(g); EX2029 ¶188.

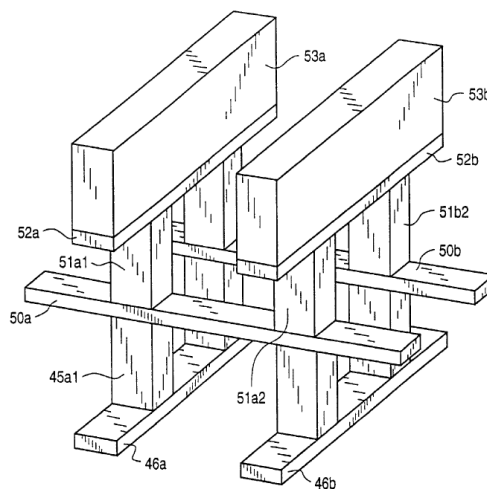


FIG. 6(g)

Johnson knew about transistor memory cells and used diodes instead to achieve a simpler, more cost-effective design. EX1010 at 2:38-61, 11:42-58. He provided no roadmap to implement transistors in his simplified diode pillar, and Intel fails to show that one of skill would have been motivated, let alone with a reasonable expectation of success, to squeeze larger and more complicated 3-terminal devices, and their supporting circuitry, into Johnson's tightly-packed pillar matrix, particularly when Johnson counseled against it. EX2029 ¶¶168-89; *see, e.g., Nitro Fluids v. Cameron Int'l*, IPR2020-00691, 2020 WL 5031954, at *10 (P.T.A.B. Aug.

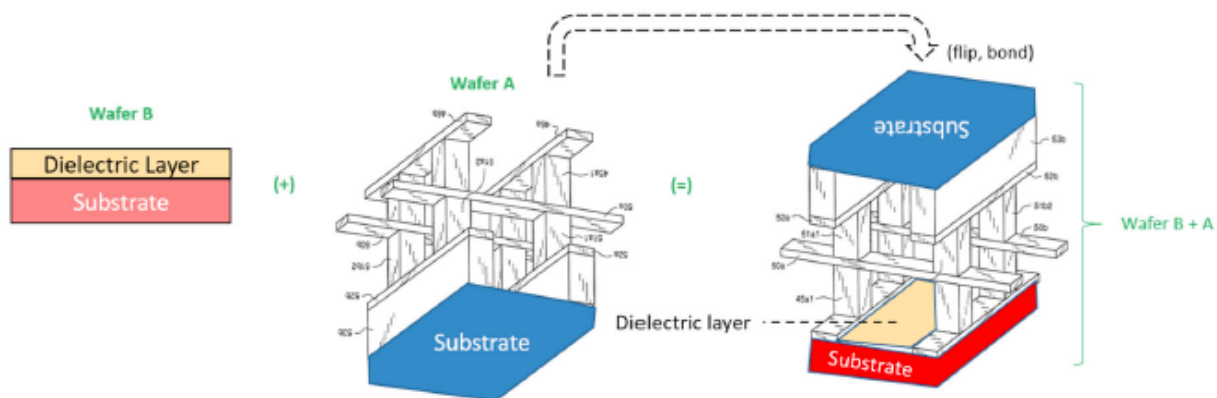
25, 2020) (no motivation to replace a “simpler” design with “a more complex rigid” design).

C. Intel Does Not Establish A Motivation To Combine Johnson With Kim (Claim 13)

Ground 2B is also insufficient for another reason—it does not meet Intel’s burden to show a motivation to combine Johnson and Kim.

1. Merely Asserting That Johnson Could Be Combined With Kim Does Not Show A Motivation To Combine

It’s undisputed that Johnson teaches deposition, Pet. at 74, yet the Petition proposes jettisoning it in favor of using Kim to wafer-bond Johnson’s memory cells to Johnson’s “insulating layer” on the substrate. Pet. at 75. It does so by fabricating Johnson’s substrate on Wafer B, building Johnson’s pillars upside down on another wafer (Wafer A), and then flipping them over and wafer bonding, which it conceptualizes like this:



Pet. at 75.

Intel never provides the required reason why one of skill would have abandoned Johnson’s self-aligned deposition technique for Kim’s wafer bonding. Pet. at 74-77; *Nuvasive*, 842 F.3d at 1384. Johnson relied on its tightly-packed, self-aligned levels to achieve its dense diode architecture, which Johnson described as “an extremely important advantage” and allowed for a “higher density and lower cost” design. EX1010 at 11:52-58; *see id.* at 11:42-52; EX2029 ¶¶188, 195. Intel’s own exhibit explains the problems with wafer bonding, including lower yields and reduced density. EX1016 at 1:32-52. One of skill would not switch Johnson to a less-precise bonding technique plagued with alignment problems. EX2029 ¶¶193, 195.

Intel also argues that using stacking in Johnson was “predictable” and involved using “a known technique.” Pet. at 75-76 (citing EX1003 ¶249). “[T]hat is not enough.” *Personal Web Techs. v. Apple*, 848 F.3d 987, 993-94 (Fed. Cir. 2017) (finding no “motivation to pick out those two references and combine them to arrive at the claimed invention”). Not all ideas are good ideas, and just because something is “known” does not make it obvious or a better choice. *KSR*, 550 U.S. at 418. Saying something was predictable, or “could have” been done, does not mean one of skill “*would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention.” *Belden*, 805 F.3d at 1073 (emphasis in original).

2. “Quality Control” And “Less Waste” Provide No Motivation To Switch To Kim

The Petition’s empty assertions that Kim would “improve” Johnson or “allow[] for more efficient quality control with less potential waste” also cannot be sustained. Pet. at 75-76. Intel admits that Johnson already “discloses a low cost, high density semiconductor memory,” Pet. at 65 (internal quotation marks omitted), and never explains exactly how Kim would purportedly “improve... Johnson’s structure.” See Pet. at 76. Again, failing to identify any specific improvement dooms Intel’s combination. *Microsoft*, 2018 WL 1997727, at *6; *see also Sony*, 2019 WL 1581942, at *5.

The Petition’s “quality control” rationale fares no better, Pet. at 76 (citing EX1003 ¶250; EX1016), because Intel never establishes Kim’s wafer-bonding provides any demonstrated improvement over the testing that semiconductor fabs already perform nor supplies any data backing up its assertion. *Supra* § VI.A.2; EX2039 at 114:14-115:15; EX1014 at 841-42; I.D. at 35-36; EX2029 ¶¶125-32, 197. Testing is infeasible in any event: Dr. Sechen admitted that Johnson did not disclose any access points to test for shorts, EX2039 at 107:18-112:4.

The Petition cannot sustain its claim of “less potential waste” when Kim grinds off almost an entire wafer after each bonding. *Supra* § VI.A.2; EX1008 ¶25;

EX2029 ¶¶131, 197. Ground 2B may be entirely rejected for providing no motivation to combine Johnson and Kim.

D. The Petition Provides No Reasonable Expectation Of Success In Combining Johnson And Kim (Claim 13)

The Petition recites a single sentence that one of skill would have a reasonable expectation of success in using Kim's wafer bonding with Johnson. *See* Pet. at 76-77. That claim does not survive the most cursory review, and Dr. Sechen couldn't defend it on cross-examination.

Johnson's self-aligned deposition technique used each level's strips to mask the etching of the lower-level pillars, which achieved his dense diode design. EX2029 ¶¶193-95; EX1010 at 11:42-58, 12:42-65. Yet Intel inexplicably reverses Johnson's process, without comment, to build its diode memory backwards to attempt to shoehorn it into Kim's bonding process. Pet. at 75; EX2029 ¶192. But Intel provides no explanation how Johnson's densely packed and self-aligning levels could be built using stacking, or how it would overcome the significant alignment problems Johnson's specific deposition approach was designed to overcome. *See* Pet. at 75; EX1010 at 2:38-61; EX2029 ¶¶192-95.

One of skill would also recognize that Intel's proposal leaves strips 53a and 53b without any purpose, *see* Pet. at 75, which only increases costs and lowers yield, EX2029 ¶193. Further, Intel's reliance on Figures 6(e) and 6(g) is also a non-starter

because both are intermediate steps in Johnson’s interleaved “fabrication sequence,” EX1010 at 12:42-43, and one of skill would have appreciated they were incomplete and inoperable themselves, EX2029 ¶196. Even Dr. Sechen conceded that he would need to look outside of Ground 2B to Aspar to accomplish the Johnson/Kim combination. EX2039 at 105:14-107:17 (“Q. Okay. So you meant to refer to Aspar there? A. Yes.”). If Intel’s own expert admits he’d need help to combine Johnson/Kim, *id.*, Intel can hardly volunteer one of ordinary skill to pull it off from just the teachings in Johnson and Kim, EX2029 ¶196.

Intel’s omission of the inconvenient aspects of Johnson’s recipe to purportedly satisfy the claim limitations only shows the ’702 Patent is non-obvious. Absent “specific evidence” one of skill could make the combination with a reasonable expectation of success, Claim 13 should be confirmed over Johnson and Kim. *Samsung*, 925 F.3d at 1382-83.

**X. THE PETITION DOES NOT MEET ITS BURDEN TO SHOW
OBVIOUSNESS BASED ON JOHNSON AND ASPAR (GROUND 2C)**

Ground 2C is another rehash of Ground 2B, exchanging Kim for Aspar’s 1100°C Smart-Cut technique. Patentability should be confirmed over Ground 2C.

A. Johnson Does Not Disclose Or Suggest “Memory Cells Having At Least One Transistor” (Claim 13)

For the same reasons as Ground 2B, Johnson’s 2-terminal diode pillar does not disclose or suggest “nonvolatile memory cells having at least one transistor.”

Supra § IX.A; EX2029 ¶¶168-80, 200.

B. One Of Skill Would Not Have Been Motivated To Modify Johnson’s Diode Design (Claim 13)

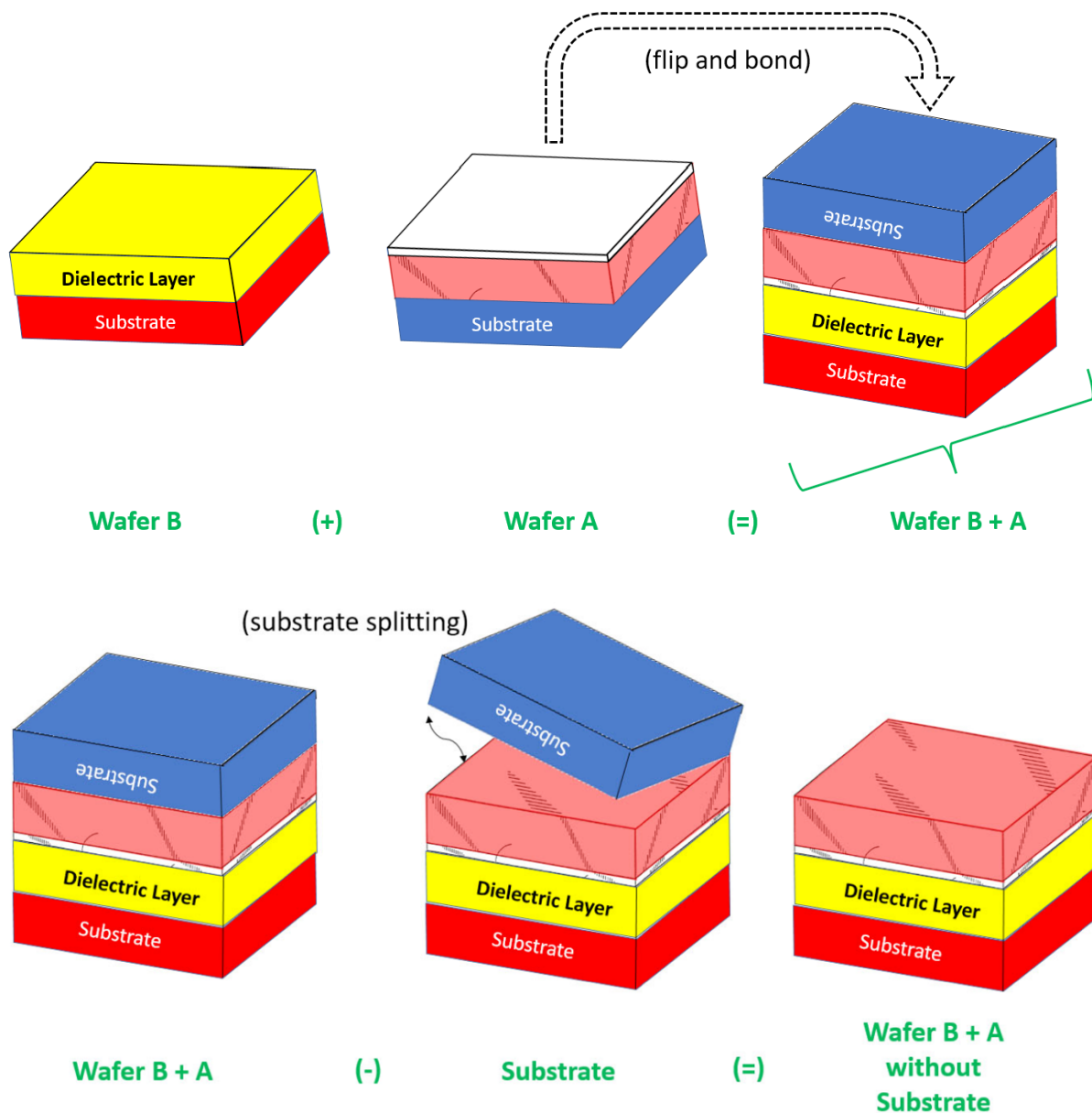
Claim 13 alternatively may be confirmed as explained in Ground 2B because one of skill would not have a motivation to modify Johnson’s diode pillar to use a 3-terminal transistor, let alone with any reasonable expectation of success, particularly when Johnson warned against it. EX1010 at 2:28-61, 11:42-58; *supra* § IX.B; EX2029 ¶¶168-89, 200.

C. Intel Does Not Establish A Motivation To Combine Johnson With Aspar (Claim 13)

The Board should also reject Ground 2C because Intel fails to show a motivation to combine Johnson and Aspar.

Although Johnson indisputably instructs using deposition to fabricate its device, Pet. at 74; *supra* § IX.C.1, again the Petition proposes jettisoning Johnson’s deposition for “Aspar’s Smart-Cut® wafer bonding process,” Pet. at 78. Intel and its expert head to fantasyland once again, imagining fabricating Johnson’s self-aligned diode pillars on Wafer A and its CMOS transistors on Wafer B, flipping

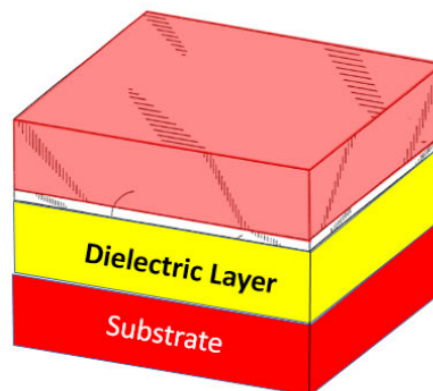
Wafer A on top of Wafer B, and splitting the Wafer A substrate (blue) off the top like this:



Pet. at 79-80 (citing EX1003 ¶¶258-260). As with Kim in Ground 2B, Intel again doesn't show how reversing Johnson's self-aligned deposition process could be built using stacking instead, or how it would overcome the alignment pitfalls Johnson's

method avoided. Pet. at 79-80; *supra* § IX.A; EX1010 at 2:28-61, 11:42-58; EX2029 ¶¶192-95, 199-201, 204. Simply asserting that one of skill *could have* made the proposed combination, or that something was “predictable” or “known,” does not establish a motivation to combine. *Supra* § IX.C.1; *Belden*, 805 F.3d at 1073; *Personal Web*, 848 F.3d at 993-94; *KSR*, 550 U.S. at 418.

Again, using Smart-Cut was a non-starter. Aspar’s 1100°C annealing after splitting was a terrible idea that would have surpassed Johnson’s thermal budget. *Supra* § VII.A.2; EX1015 at 543-44, Fig. 11-24; EX1003 ¶¶46-47; EX2039 at 117:17-121:11; EX2029 ¶¶148-51, 203. According to Intel and its expert, the combined Wafer A+B shown at right contains “Johnson’s ‘CMOS transistor[.]’” control circuitry (red) and diode “doped stack” (pink), Pet. at 78, and one of skill would have known



**Wafer B + A
without
Substrate**

better than to expose them to high temperature, EX2039 at 101:15-103:3, 99:12-100:5; EX2029 ¶203; EX2027 at 715; EX1001 at 7:15-35. Intel cannot establish a motivation to combine by proposing a combination that would damage Johnson’s device. *Supra* § VII.A.2; EX2029 ¶203; *Redline Detection*, 811 F.3d at 453; *Streck*, IPR2021-01577, Paper 62 at 87.

The Petition regurgitates the same better “quality control” and “minimizes waste” motivations from Grounds 1E-1F as an excuse to depart from Johnson to adopt Aspar’s Smart-Cut technique. Pet. at 81. These rationales again fall short. *Supra* § VII.A.3. Because Wafer A is just an unpatterned doped stack from Johnson’s Figure 6(a) with no diodes formed yet, *see* Pet. at 78-80; EX1010 at 12:1-10, 12:42-52, Fig. 6(a), there is nothing to test. EX2029 ¶202; EX2039 at 90:5-20 (Dr Sechen: unpatterned wafers don’t have memory devices). Plus, there’s no dispute Johnson didn’t disclose any access points for testing anyway, EX2039 at 110:21-112:4 (Sechen: identifying none); EX2029 ¶202, and Intel proffers no data supporting its improved quality control claim, Pet. at 81; EX2029 ¶202; I.D. at 35-36. Certainly, overbaking Johnson’s device can hardly be called less wasteful than Johnson’s disclosed deposition technique. EX2029 ¶202; Pet. at 69 (Intel: Johnson teaches deposition). Simply asserting “Aspar’s Smart-Cut® process” would “improve... Johnson’s structure,” cannot meet Intel’s burden. *See* Pet. at 81.

The claims should be confirmed over Ground 2C because Intel has not shown a motivation to apply Aspar’s stacking to Johnson either.

D. The Petition Has Not Established A Reasonable Expectation Of Success In Combining Johnson With Aspar (Claim 13)

Given Smart-Cut’s obvious flaws, the Petition’s single-paragraph reasonable expectation of success analysis falls short. *See* Pet. at 81-82.

First, we can start and end the analysis with this: Aspar’s annealing at 1100°C would not have instilled a reasonable expectation of success in the skilled artisan. *Supra* §§ II.F, VII.A.2; EX2029 ¶¶148-51, 203.

Second, Intel carelessly turns Johnson’s self-aligned deposition method on its head and says to fabricate its Figure 6(a) diode pillar upside down, Pet. at 79 (“FIG 6(b) (inverted)”), but never explains how one of skill would accomplish this with any reasonable expectation of success, *supra* § IX.D; EX2029 ¶¶199-201, 204. Declaring that combining Johnson and Aspar was a “predictable process,” Pet. at 82, is disingenuous when Intel itself ignores or departs from the tricky bits like the Si layer its expert admits Smart-Cut would leave on the top surface. *Supra* § VII.B; EX2029 ¶¶205-06. Intel’s vague ideas divorced from the reality of designing and building a new, workable memory device don’t come close to the “specific evidence” required to show a *reasonable* expectation of success. *Samsung*, 925 F.3d at 1382-83. Ground 2C should be confirmed for this reason as well.

XI. THE PETITION DOES NOT MEET ITS BURDEN FOR GROUND 2A BASED ON JOHNSON

Like Grounds 1A-1B, Ground 2A never made it past institution because even Intel and its expert contest it, and the additional nails in the coffin below only confirm it should be rejected.

A. Johnson Does Not Disclose Or Suggest “Memory Cells Having At Least One Transistor” (Claim 13)

As explained, Johnson’s 2-terminal diode pillar does not disclose or suggest “nonvolatile memory cells having at least one transistor.” *Supra* § IX.A; EX2029 ¶¶168-80.

B. One Of Skill Would Not Have Been Motivated To Modify Johnson’s Diode Design (Claim 13)

Johnson taught away from using a 3-terminal transistor in its diode pillars, and the Petition shows no motivation to modify them with any reasonable expectation of success. *Supra* § XI.B; EX2029 ¶¶168-89.

C. The Petition Improperly Argues Unpatentability Under A Construction Of “Stackable Add-On Layer” It Claims Is Incorrect (Claim 13)

The Board correctly found that Ground 2A cannot meet its burden because Intel and its expert argue that the construction of “stackable add-on layer,” on which Ground 2A depends, is “incorrect.” *See* I.D. at 46; *see also* Pet. at 12, 65; EX1003 ¶84; EX2039 at 16:14-17:13. Patentability should be confirmed. *Hologic*, 2018 WL 1897623, at *3-4; *Ebates*, 2022 WL 5048425, at *5; POPR at 29-33.

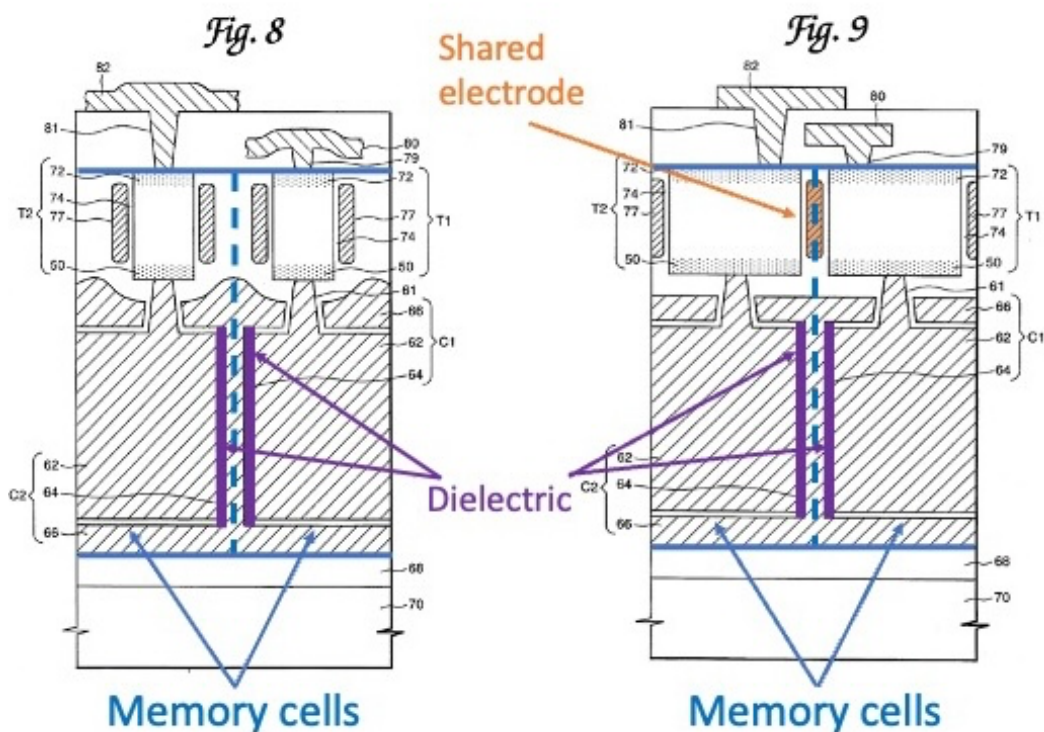
XII. THE PETITION DOES NOT MEET ITS BURDEN FOR GROUND 3 BASED ON PARK AND KIM

Claim 1 is not asserted against Intel (or Micron) in district court. The Institution Decision correctly found a “significant issue as to whether Park discloses

memory cells that are separated from each other by dielectric material.” I.D. at 53 (emphasis original). Claim 1 should be sustained for this reason.

Intel relies exclusively on Park to show “memory cells separated from each other by dielectric material.” Pet. at 88; EX1001 at 10:55-57. It points to transistors separated by insulating film, Pet. at 88 (citing EX1011 at 2:16-21, 4:9-27), but admits that, “[i]n Park, a dielectric film 64 is... interposed between the plate and storage electrodes of capacitors C1 and C2,” *i.e.*, between electrodes 62 and 66. Pet. at 89.

Figures 8-9 below are different views of the same structure. EX1011 at 5:33-35. The Petition overlooked that capacitors C1-C2 form part of the memory cell and store the data. EX1011 at 5:36-43. As the Board recognized, Figures 8-9 plainly show the adjoining “memory cells... share plate electrode 66,” I.D. at 53, and thus the capacitors are not isolated by dielectric:



EX1011 at Figs. 8-9 (annotated). The “dielectric film 64” Intel identifies (purple) is entirely inside and an integral part of the capacitor of Park’s memory cell, not “separating” them as required by Claim 1[b]. *See id.*; EX2029 ¶¶209-10. Intel’s argument that the “capacitors of each memory cell are surrounded by insulating material,” Pet. at 89, is refuted by Park itself, *see* EX1011 at Figs. 8-9, 5:33-54.

Intel’s assertion that the “transistors” are “surrounded by insulating material” is also unsupported. Pet. at 89. Park explained its transistors are only “isolated by an insulating material between the gate electrodes 33 in the bitline direction (see FIG. 8)” but “*they share a gate electrode 77 in... the wordline direction* (see FIG.

9).” EX1011 at 5:49-54 (emphasis added). This is plainly shown in Figure 9. *See also* EX1010 at Fig. 7 (plan view same); EX2029 ¶211.

Intel and Dr. Sechen’s theory that separating “the memory cells with dielectric material for proper operation (e.g., avoiding shorts)” would also be obvious cannot substitute for Park’s express teaching of the opposite. *Compare* Pet. at 89 with EX1003 ¶276; *One World*, 2020 WL 7222691, at *16; *Xerox*, 2022 WL 3648989, at *6. Indeed, Park’s Figures 8-9 showing memory cells with a shared capacitor plate 66 gives lie to Intel’s claim. *See* EX1011 at Figs. 7-9; EX2029 ¶210.

Intel’s new argument on preliminary reply asserted that “complete separation is not required.” Paper 7 at 5 (citing EX1001 at Figs. 9-10). This pivot only confirms Intel’s new argument was not in its Petition, *see* Pet. at 87-89, and it is too late to add it now, *Netflix v. Robocast*, IPR2023-00081, 2023 WL 5162380, at *14 n.8 (P.T.A.B. May 11, 2023) (rejecting “improper new argument” in preliminary reply under 37 C.F.R. § 42.23(b)). Regardless of how Claim 1 is construed, the “share[d] gate electrode” between transistors shows they are electrically connected, not “separated” by dielectric. EX1011 at 5:49-53; EX2029 ¶¶210-11. Intel’s new argument is unsupported because its resort to Figures 9-10 of the ’702 Patent misunderstands that “a claim need not cover all embodiments,” *Intamin v. Magnetar Techs.*, 483 F.3d 1328, 1337 (Fed. Cir. 2007), and Claim 1’s requirement is supported by at least Figure 1, EX1001 at 5:18-21.

Intel Corporation v. BeSang Inc.
Patent No. 7,378,702 – IPR2023-00991

Claim 1 should be confirmed patentable over Ground 3.

XIII. CONCLUSION

For each of the foregoing reasons, BeSang respectfully requests the Board confirm patentability of the Challenged Claims.

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that foregoing **PATENT OWNER’S RESPONSE TO PETITION FOR *INTER PARTES* REVIEW**, exclusive of the parts exempted as provided in 37 C.F.R. § 42.24, contains 13,947 words and therefore complies with the type-volume limitations of 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

The undersigned certifies that pursuant to 37 C.F.R. § 42.6(e), a true copy of the foregoing **PATENT OWNER’S RESPONSE TO PETITION FOR *INTER PARTES* REVIEW and EX2023-EX2024, EX2027-EX2033, EX2039, EX2041-EX2046** are being served electronically on March 13, 2024 to the following lead counsel for Petitioner to the following email addresses:

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