

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

BESANG INC.,
Patent Owner.

Case No. IPR2023-00991
U.S. Patent No. 7,378,702

**DECLARATION OF STEVEN A. PRZYBYLSKI
IN SUPPORT OF PATENT OWNER'S RESPONSE
TO PETITION FOR *INTER PARTES* REVIEW**

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I, Steven A. Przybylski, hereby declare as follows:

I. INTRODUCTION

1. I have prepared this Declaration in connection with Patent Owner's Response to the Petition for Inter Partes Review of U.S. Patent No. 7,378,702 ("the '702 Patent").

2. In the course of preparing this Declaration, I reviewed the '702 Patent, its prosecution file history, the asserted prior art, as well as the documents listed in Section III and/or discussed in this Declaration.

3. I have been retained by BeSang Inc. ("BeSang" or "Patent Owner") as an expert in the field of memory devices and semiconductor design. I am being compensated at my normal consulting rate for my time. My compensation is not dependent on and in no way affects the substance of my statements in this Declaration. I have no financial interest in BeSang, the '702 Patent or the owner of the '702 Patent.

II. BACKGROUND AND QUALIFICATIONS

4. Further details regarding my qualifications, including my employment and academic history, are set forth in my curriculum vitae. Ex. 2030.

5. I earned a Bachelor of Applied Science from the University of Toronto in 1980. I was enrolled in the Engineering Science program, completing a course of study combining the Electrical Engineer and Computer Science options.

6. I earned a Master of Science in Electrical Engineering degree and a Ph.D. in Electrical Engineering in 1982 and 1988 respectively, both from Stanford University.

7. I also earned a Masters of Business Administration from the Haas School of Business at the University of California at Berkeley in 2000.

8. I have extensive experience with memory semiconductor integrated circuits and the memory systems constructed of them. At Stanford, my dissertation was on the optimization of single- and multi-level cache hierarchies to maximize system-level performance. Also at Stanford, I was a member of the core team that architected, designed, built, and tested the seminal MIPS processor. I was responsible for the design of the instruction decode and control units as well as architecting the virtual memory support. I assembled and debugged the entire microprocessor design and oversaw its fabrication and testing. In 1984 and 1985, I took a leave of absence from Stanford to become a member of the founding team of MIPS Computer Systems, a startup in California that designed, built, and sold processors and computer systems. In 1989, after finishing my doctorate and brief post-doctorate at Stanford, I returned to MIPS Computer Systems. Throughout my two periods of employment at MIPS Computer Systems, I had a number of titles and worked on a variety of projects. Noteworthy were stints as processor architect, systems architect, hardware-software team liaison, and Chief Scientist of the High-

End Systems group. During the second period, I also served as a Consulting Assistant Professor in the Department of Electrical Engineering at Stanford. I designed and taught an advanced graduate level course on cache and memory system design.

9. In 1991, I left MIPS to become an independent consultant. In that capacity I have provided technical, strategic, marketing, and intellectual property services to a large number of clients both domestically and internationally.

10. The technical consulting I performed was principally related to advancements in semiconductor memories and their application in systems. Specifically with respect to non-volatile memories and Flash memories in particular, I advised companies on a variety of memory types and on trends in NAND and NOR Flash memories and the processes used in their manufacture. In the 2000's, in the time period relevant to the present matter, I helped develop a new NAND Flash architecture and separately a universal memory interface that was optimized for use in heterogeneous memory systems and that was equally applicable to DRAMs and to NAND Flash devices.

11. I am a member of both the Institute of Electrical and Electronics Engineers (IEEE) and the Association of Computing Machinery (ACM). In addition, in 1997 I became a registered patent agent. I am listed as the inventor on 11 domestic patents and their foreign counterparts. The subject matters include memory devices,

memory subsystems, networks, error detection and correction codes, processors and cache memories. Between 1994 and approximately 2000, I was a leading independent analyst following, writing, and teaching about both the technical and business aspects of the DRAM industry. Overall, I have written three books and over 25 articles in the areas of memory, processors, and computer systems. In particular, I wrote and revised an 850-page book entitled “New DRAM Technologies: A Comprehensive Analysis of the New Architectures.” I have presented many lectures, classes and seminars on semiconductor memories and their memory systems, processors and computer systems. I have presented full and half-day seminars on discrete and embedded DRAMs to over 2,500 engineers, marketers, managers, and financial analysts.

III. MATERIALS CONSIDERED

12. I have reviewed the '702 Patent (Ex. 1001) and its file history (Ex. 1002). Additionally, and in addition to any other documents cited or referenced herein, I have reviewed the following materials in preparing this Declaration:

- a. Petition for *Inter Partes* Review (Paper 2);
- b. Declaration of Dr. Carl Sechen (Ex. 1003);
- c. U.S. Patent Application Pub. No. 2002/0028541 (“Lee”) (Ex. 1007);
- d. U.S. Patent Application Pub. No. 2003/0157748 (“Kim”) (Ex. 1008);

- e. Aspar et al., *The Generic Nature of the Smart-Cut[®] Process for Thin Film Transfer*, 30 J. Elec. Materials 834 (2001) (Ex. 1009);
- f. U.S. Patent No. 6,034,882 (“Johnson”) (Ex. 1010);
- g. U.S. Patent No. 5,571,730 (“Park”) (Ex. 1011);
- h. U.S. Patent Application Pub. No. 2002/0154556 (“Endoh”) (Ex. 1012);
- i. Stanley Wolf, Ph.D. & Richard Tauber, Ph.D., *Silicon Processing for the VLSI Era*, Vol. 1 (2d ed. 2000) (Ex. 1014);
- j. Stanley Wolf, Ph.D., *Silicon Processing for the VLSI Era*, Vol. 4 (2002) (Ex. 1015);
- k. U.S. Patent No. 6,355,501 (“Fung”) (Ex. 1016);
- l. U.S. Patent No. 5,882,987 (“Srikrishnan”) (Ex. 1023);
- m. Perrine Batude, et al., *3-D Sequential Integration: A Key Enabling Technology for Heterogeneous Co-Integration of New Function with CMOS*, IEEE J. on Emerging & Selected Topics in Circuits and Systems, Vol. 2, No. 4 (Dec. 2012) (Ex. 2027);
- n. Deposition of Dr. Jack C. Lee, *Micron Tech., Inc. v. BeSang Inc.*, IPR2023-00900 (Feb. 6, 2024) (Ex. 2028);
- o. *Webster’s New Universal Unabridged Dictionary* (Barnes & Noble Publ’g 2003) (excerpt) (Ex. 2031);

- p. *Random House Webster's College Dictionary* (2d ed. 1997) (excerpt) (Ex. 2032);
- q. Gary S. May, Ph.D. & Costas J. Spanos, Ph.D., *Fundamentals of Semiconductor Manufacturing and Process Control* (2006) (excerpts) (Ex. 2033);
- r. Transcript of Deposition of Dr. Carl Sechen (Feb. 27, 2024) (Ex. 2039);
- s. Tetsuo Endoh, et al., *Novel Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell*, IEEE Transactions on Electron Devices, Vol. 50, No. 4 (Apr. 2003) (Ex. 2041);
- t. Hiroshi Sakuraba, et al., *New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology without Photolithography Process for Tera-Bits and Beyond*, Japanese J. of Applied Physics, Vol. 43, No. 4B (2004) (Ex. 2042);
- u. G. Groeseneken, et al., Basics of Nonvolatile Semiconductor Memory Devices, in *Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices* (William D. Brown & Joe Brewer eds., 1997) (Ex. 2044);

- v. Linden T. Harrison, Current Sources & Voltage References (2005) (Ex. 2045);
- w. The Electrical Engineering Handbook (Wai-Kai Chen ed., 2005) (Ex. 2046);
- x. Petition for *Inter Partes* Review of U.S. Patent No. 7,378,702, *Micron Tech., Inc. v. BeSang Inc.*, IPR2023-00900, Paper 2 (P.T.A.B. May 4, 2023); and
- y. Declaration of Dr. Jack C. Lee, *Micron Tech., Inc. v. BeSang Inc.*, IPR2023-00900, Ex. 1002 (P.T.A.B. May 4, 2023).

IV. SUMMARY OF ASSERTED GROUNDS

13. The following table enumerates the Grounds found in Intel’s Petition and claims and references referred to accordingly.

Ground	Type	Claims	References
1A	35 U.S.C. § 103	13-17	Lee
1B	35 U.S.C. § 103	16-17	Lee, Endoh
1C	35 U.S.C. § 103	13-17	Lee, Kim
1D	35 U.S.C. § 103	16-17	Lee, Kim, Endoh
1E	35 U.S.C. § 103	13-17	Lee, Aspar
1F	35 U.S.C. § 103	16-17	Lee Aspar, Endoh
2A	35 U.S.C. § 103	13	Johnson

2B	35 U.S.C. § 103	13	Johnson, Kim
2C	35 U.S.C. § 103	13	Johnson, Aspar
3	35 U.S.C. § 103	1	Park, Kim

V. RELEVANT LAW

14. I am not an attorney. For the purposes of this Declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is summarized below.

15. I have been informed and understand that determining whether a patent claim is valid requires a two-step analysis. First, the claim must be construed. Second, the properly construed claim must be compared to the prior art.

16. I have been informed and understand that claim construction is a matter of law and that the final claim constructions for this proceeding will be determined by the Patent Trial and Appeal Board.

17. I have been informed and understand that in the context of an inter partes review, claims are construed from the perspective of a person of ordinary skill in the art at the time of the purported invention (which is approximated based on the earliest priority date of the patent). I understand that absent disclaimer or express definition, claim terms are given their plain and ordinary meaning to a person of

ordinary skill in the art in view of the specification and file history and knowledge of a person of skill in the art.

18. I have been informed and understand that a patent claim is invalid if it is anticipated by the prior art; in other words, it lacks novelty. I understand that anticipation requires the disclosure in a single prior art reference of every limitation of the claim, expressly or inherently, with the limitations arranged as specified in the claim.

19. I have been informed and understand that, although not expressly disclosed, subject matter may be inherently disclosed in a prior art reference where that subject matter is necessarily present in the expressly disclosed subject matter and would be understood to be so by those of ordinary skill in the art. I understand that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.

20. I have been informed and understand that a patent claim is obvious and therefore invalid if the claimed subject matter, as a whole, would have been obvious to a person of ordinary skill in the art as of the priority date of the patent based on one or more prior art references and/or the knowledge of one of ordinary skill in the art. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-

obviousness (such as unexpected results, industry praise, commercial success, long-felt but unmet need, failure of others, copying by others, and skepticism of experts).

21. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. § 103. I understand that a reference may also be combined with the knowledge of a person of ordinary skill in the art, and that this knowledge may be used to combine multiple references. I further understand that a person of ordinary skill in the art is presumed to know the relevant prior art. I understand that the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

22. In determining whether a prior art reference could have been combined with other prior art or other information known to a person having ordinary skill in the art, I understand that the following principles may be considered:

23. (a) A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;

24. (b) The substitution of one known element for another is likely to be obvious if it yields predictable results;

25. (c) The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

26. (d) The application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;

27. (e) Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;

28. (f) A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and

29. (g) The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success” – not “absolute predictability” of success – in achieving the claimed invention by combining prior art references.

30. I am informed that whether a prior art reference invalidates a patent claim as obvious is determined from the perspective of a person of ordinary skill in the art. While there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole, or individually, as filtered through the knowledge of one skilled in the art. In addition, the inferences and creative steps a person of ordinary skill in the art would employ are also relevant to the determination of obviousness.

31. When a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. If a

person of ordinary skill in the art can implement a predictable variation and would see the benefit of doing so, that variation is likely to be obvious. In many fields, there may be little discussion of obvious combinations, and in these fields market demand – not scientific literature – may drive design trends. When there is a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art has good reason to pursue those known options.

32. It is my understanding that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But, I understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. This test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and it seeks to counter impermissible hindsight analysis.

33. It is also my understanding that to render a claim obvious, the prior art, taken as a whole, must enable a skilled artisan to make and use the claimed invention. I understand that if an obviousness case is based on a non-self-enabled reference, and no other prior art reference or evidence would have enabled a skilled artisan to make the claimed invention, then the invention cannot be said to have been obvious.

VI. LEVEL OF ORDINARY SKILL IN THE ART

34. In Micron’s IPR on the ’702 Patent, Micron proposes a definition for a person of ordinary skill in the art as of June 2004 to be a practitioner with “a bachelor’s degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa.” Micron Petition, p. 8; Micron Ex. 1002 ¶¶ 2, 34.

35. In this IPR, Intel proposes a definition for a person of ordinary skill in the art “at the relevant time” as having a “bachelor’s degree in electrical engineering, computer engineering, *materials science*, or a related field, and at least *three years* of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa.” Petition, p. 9 (emphases added); citing Ex. 1003 (Sechen Declaration) ¶ 37.

36. Intel acknowledges the difference: “The IPR2023-00900 petitioner proposes a slightly different articulation of the level of skill. The unpatentability grounds below apply equally under that articulation.” Petition, p. 9 at fn. 5.

37. In the above paragraphs I bolded the two differences in the definitions that Micron, Intel, and their experts propose. As Intel acknowledges, these

definitions are “slightly different” adding one more year of experience and/or a background in materials science.

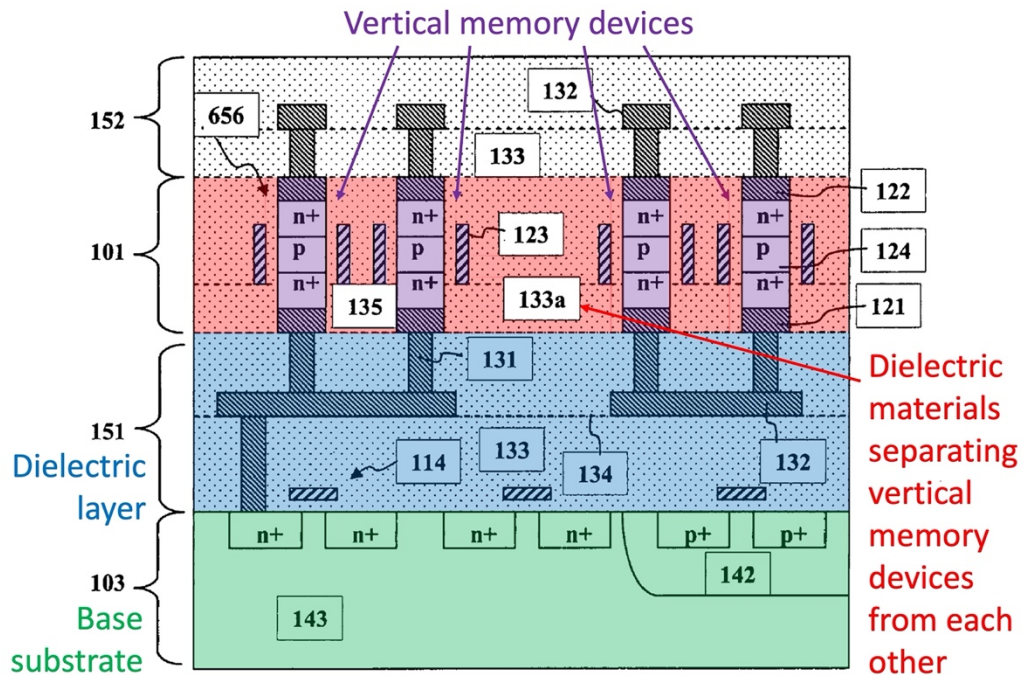
38. As I did in my prior declaration in the Micron IPR, and for purposes of this IPR, I adopt Micron’s definition. My analysis would be the same under Intel’s similar proposed definition in this IPR.

VII. OVERVIEW OF THE ’702 PATENT

39. Most integrated circuits (ICs) since their invention in 1958 have had the same physical structure: transistors are formed in a base substrate of a semiconductor material and the IC is mounted and packaged into a chip.

40. The ’702 patent discloses and claims a radically different physical structure in which not only are transistors formed in the base substrate, but additionally memory cells are fabricated in layers above the base substrate. These memory cells or “floating devices” are interconnected with each other and the transistors in the base substrate by interconnections provided in layers between base substrate and the floating devices layer and above the floating devices layer. The resulting device is called a 3-D integrated circuit to differentiate it from traditional integrated circuits with transistors only in the substrate. Ex. 1001 (’702 Patent), 3:51-61, 5:18-36.

Fig. 1



Ex. 1001 ('702 Patent), Figure 1, annotated.

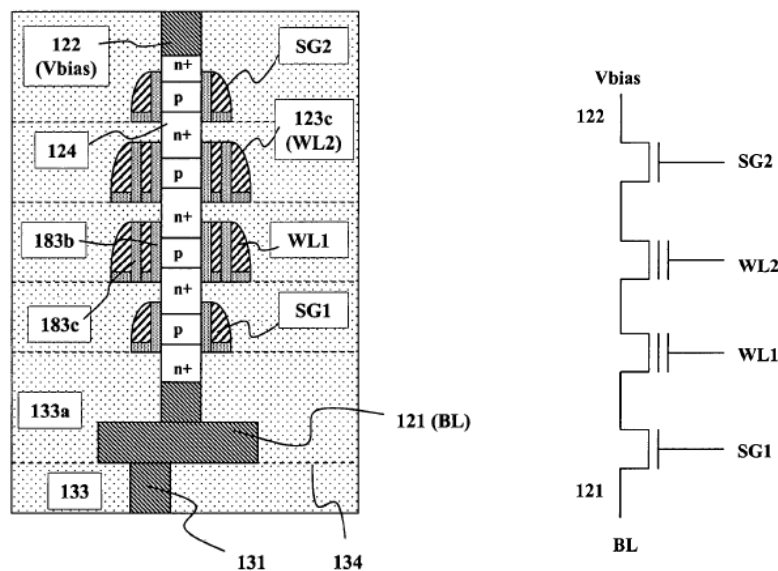
41. The embodiment of Figure 1 shows a number of layers.
42. Layer 103 is a base substrate, which includes CMOS circuitry comprising transistors. Ex. 1001 ('702 Patent), Figure 1 & 5:37-38.
43. Layer 151 is a lower dielectric layer that comprises interconnect and gates for the transistors embedded in the base substrate. Ex. 1001 ('702 Patent), Figure 1 & 5:37-38, 5:56-59.
44. Layer 101 is a floating devices layer (FD) in which vertically oriented transistors are formed. These transistors are distinct from and in addition to the

conventional, horizontally oriented transistors in the base substrate 103. Ex. 1001 ('702 Patent), Figure 1 & 5:18-22, 5:38-43. As shown in Figure 1, “vertical memory devices 656” “are separated by isolation 135 and have floating structures in the filled dielectric materials 133a.” Ex. 1001 ('702 Patent), 5:18-21. Dielectric materials are those that are substantially nonconducting.

45. Layer 152 is a second interlayer dielectric layer comprising further interconnections. Ex. 1001 ('702 Patent), Figure 1 & 5:48-50.

46. The patent discloses that the vertically oriented transistors are in stacks, as depicted, for example in Figure 1. Ex. 1001 ('702 Patent), Figures 1, 4, 20, 27, 29.

47. The '702 Patent describes how memory cells can be formed in the floating device layer(s). In particular, nonvolatile memory cells can be formed in the device layers, such that a plurality of transistors can be formed in each of a plurality of pillar structures. Ex. 1001 ('702 Patent), 5:60-64.



Ex. 1001 ('702 Patent), Figures 29, 30 & 9:59-64.

48. In this embodiment the transistors are connected serially into a chain as found in NAND Flash memory integrated circuits. These structures are referred to in the specification as SOI (Silicon on Insulator) pillars. Ex. 1001 ('702 Patent), Figures 29, 30 & 9:59-64.

VIII. CHALLENGED CLAIMS IN THE '702 PATENT

A. Claim 1

1[pre] A semiconductor memory structure, comprising:

1[a] a substrate having electrical devices formed therein, and further having at least one dielectric layer and at least one interconnect layer disposed above the substrate; and

1[b] a first stackable add-on layer, the first stackable add-on layer including a plurality of vertically oriented semiconductor memory cells disposed within the first stackable add-on layer, the plurality of vertically oriented semiconductor memory cells separated from each other by dielectric material;

1[c] wherein the stackable add-on layer is bonded to a layer of the substrate that is the greatest distance from the substrate as measured from the bottom surface of the substrate; and

1[d] wherein the memory cell is a DRAM having at least one transistor.

B. Claim 13

13[pre] A semiconductor memory structure, comprising:

13[a] a substrate having electrical devices formed therein, and further having a dielectric layer disposed above the electrical devices;

13[b] a stackable add-on layer having a plurality of vertically oriented semiconductor memory cells; and

13[c] the stackable add-on layer being bonded to the dielectric layer; and

13[d] wherein the memory cells are nonvolatile memory cells having at least one transistor.

C. Claim 14

14. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a floating gate and a control gate on a SOI pillar.

D. Claim 15

15. The semiconductor memory structure of claim 13, wherein the vertically oriented semiconductor nonvolatile memory cell comprises a vertical transistor having a charge-trapping gate insulator and a gate on a SOI pillar.

E. Claim 16

16. The semiconductor memory structure of claim 13, wherein at least two nonvolatile memory cells are vertically oriented and serially connected together and formed with a first SOI pillar.

F. Claim 17

17. The semiconductor memory structure of claim 16, wherein the at least two nonvolatile memory cells on the first SOI pillar are serially connected with an interconnect line disposed on a dielectric layer, to a nonvolatile memory cell formed with a second SOI pillar.

IX. OVERVIEW OF THE CITED REFERENCES

A. U.S. Patent Application Publication No. 2002/0028541 (“Lee”) (Exhibit 1007)

49. Lee’s application was published on March 7, 2002. For my analysis, I have been asked to assume that Lee is prior art.

50. Lee shows semiconductor memory devices with charge storage devices on a plurality of device levels. Ex. 1007 (Lee), Abstract, Figure 1, [0003], [0121]-[0122]. The non-volatile memory cell is formed in a vertical structure, with the control gate optionally surrounding the middle portion of the stack, thereby forming a non-volatile EEPROM memory cell.

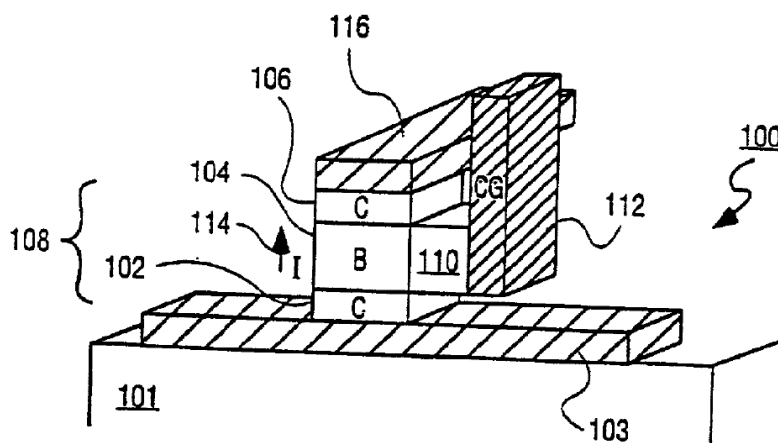


FIG. 1A

Ex. 1007 (Lee), Figure 1A.

51. The parts of Lee relied on by the Petition are only from the first part of its specification. The last paragraph cited is ¶ 208 (of ¶ 417) and the last figure

referred to is Figure 37 of 101. In addition to the embodiments related to single vertical-oriented memory cells and the processing steps to form them (for example, the embodiment of Ex. 1007, Figure 1A, above, and Figures 3-10), there are embodiments relating to 2-dimensional arrays of such cells. Ex.1007, Figure 11, [0145]. Figure 11C shows 3 vertically oriented pillars (annotated A, B, and C below) in which each pillar has two memory cells, one on each side of the structure.

52. The resulting 6 memory cells are annotated with a red oval in the reproduction below. The right memory cell of the second pillar (B, below) and the left memory cell of the third pillar share a common gate control node 1108.

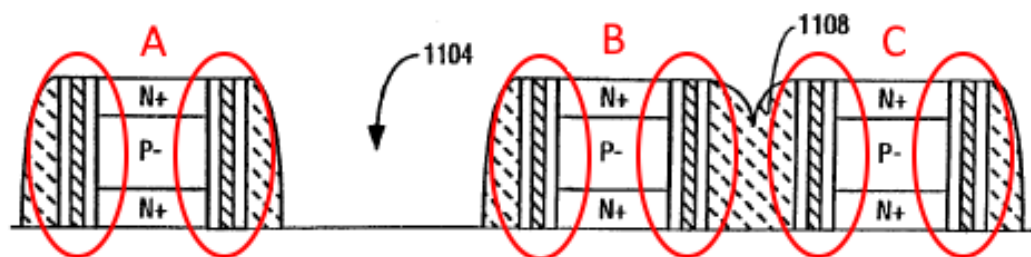


FIG. 11C

Ex. 1007, Figure 11C, annotated.

53. The idea that each pillar can have multiple memory cells at one level was introduced in connection with Figure 1C, which showed a horizontal cross section of a pillar in the shape of a rectangular prism, where each of the four sides has its own control gate, each of the four control gates controlling a distinct channel

at each of the four surfaces of the region B shown in Figure 1A. These four memory cells are annotated with red ovals below.

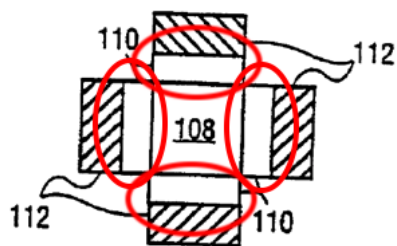
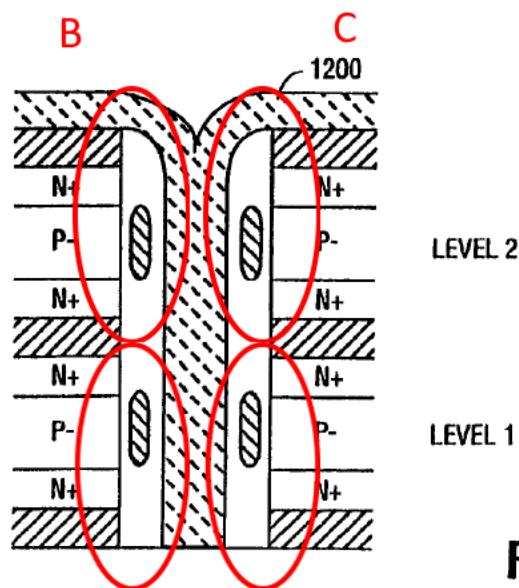


FIG. 1C

Ex. 1007, Figure 1C, annotated.

54. Lee discloses two embodiments cited by Petitioner that relate to the stacking of these memory cells. The first, shown in Figure 12, illustrates a floating gate embodiment with levels of memory cells of the style illustrated in Figure 11C, with the second level deposited directly on the first. Figure 12B shows the right half of one pillar (annotated as B to conform with the annotation of Figure 11C, above) and the left half of the adjacent pillar (annotated C). Figure 12B shows 4 memory cells, one on each side of each level of the structure. Again, these four cells are annotated with red ovals below. These four memory cells all share the same control gate signal, made of conductor 1200. Ex. 1007, [0146].



Ex. 1007, Figure 12B, annotated.

55. The second embodiment shown in Figures 13 through 28 illustrates charge trapping memory cells. The steps for manufacturing a 3-dimensional virtual ground NOR EEPROM array using structures related to that of Figure 12B. The end result is shown in Figure 27 in one cross section. It shows 3 levels of devices. It shows the control gates for levels 2 and 3 are shared vertically as in Figure 12B with each of the control gate regions 1364A and 1346B controlling four memory cells. Figure 27A also shows that the control gates for pairs of memory cells in level 1 as viewed from this cross section are shared only within that level, as shown in Figure 11C. Other representations of the embodiment of Figures 13-28 show that some of the control gates controlling level 1 memory cells also control level 2 memory cells. Ex. 1007, Figure 25A

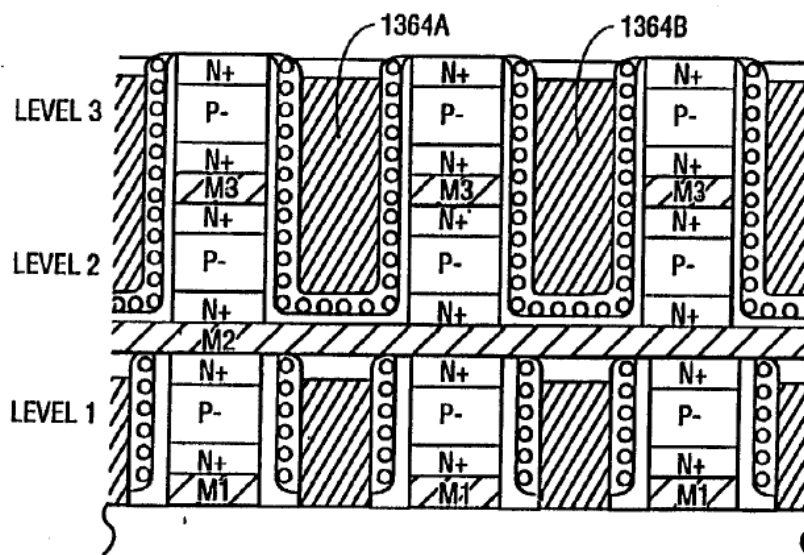


FIG. 27A

Ex. 1007, Figure 27A.

56. Figure 27B shows that Figure 27A is a longitudinal cross section down the middle of one of the plurality of second pillar strips 1340, which have now been patterned “into a plurality of second pillars 1362.” Ex. 1007, [0161], [0167].

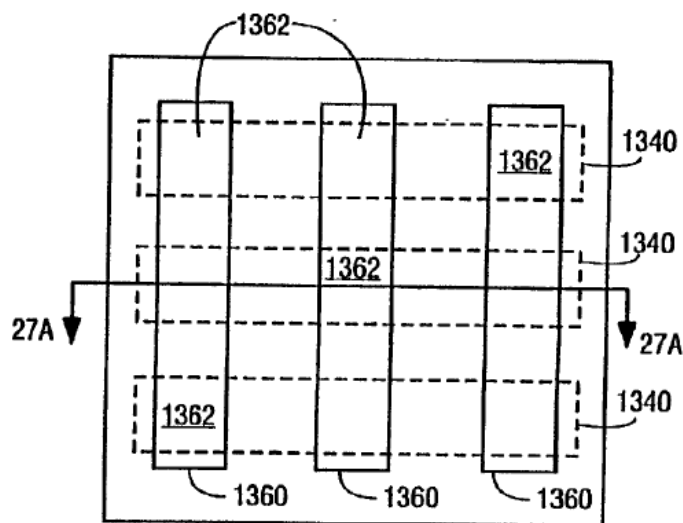


FIG. 27B

Ex. 1007, Figure 27B.

57. But Figure 25 shows the same structure at an earlier point in its fabrication before the third level of pillar strips are deposited and etched. However, Figure 25A is along a cross section that is perpendicular to pillar strips 1340, as shown by Figure 25B. The three level 1 pillars with their level 2 pillar strips crossing above sliced perpendicularly through the level 2 pillar strips by the cross section 25A are annotated A, B, and C below.

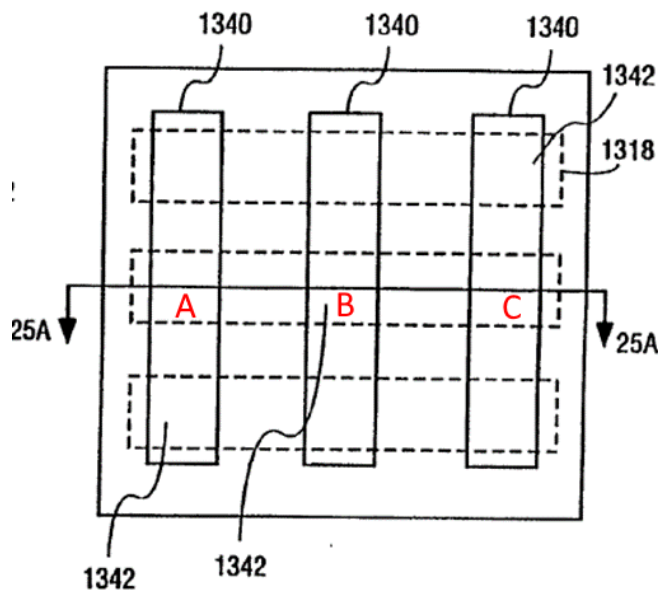


FIG. 25B

Ex. 1007, Figure 25B, annotated.

58. Figure 25A shows that when viewed from this direction in the cross section, the control gates are shared among adjacent memory cells in levels 1 and 2. In total there are 12 memory cells in Figure 25A, and each of the control gate conductors 1350A and 1350B control 4 of these.

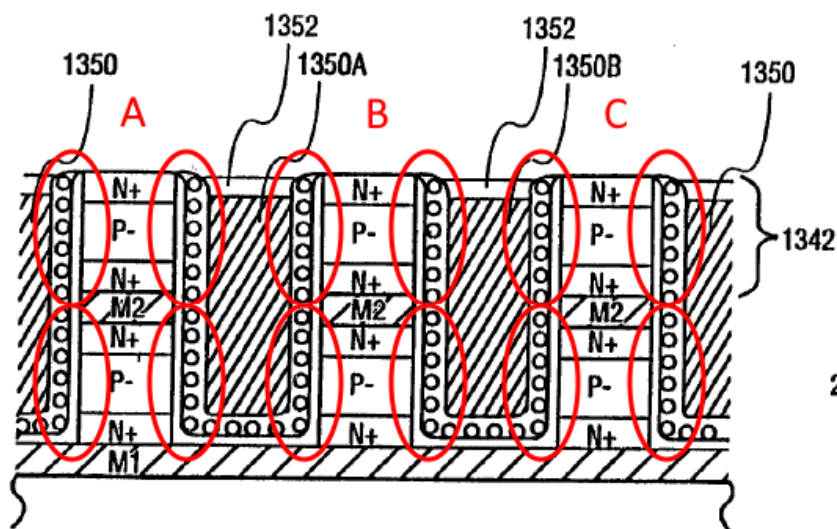
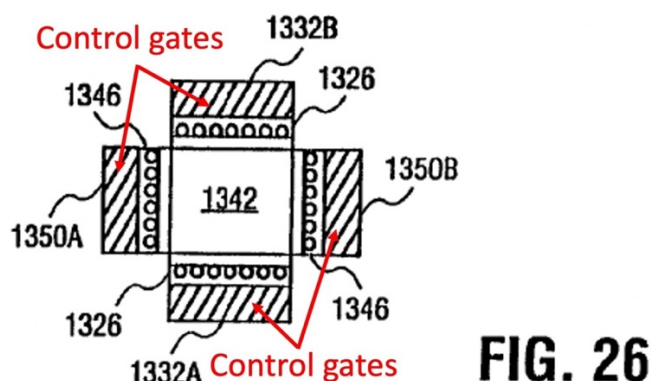


FIG. 25A

Ex. 1007, Figure 25A, annotated.

59. Figure 26 shows another view of this structure: a horizontal cross section of one of the pillars of level 1 (the one annotated B in red in Figures 25A and 25B above). It shows that the four memory cells on level 1 are controlled by control gates 1332A, 1332B, 1350A, and 1350B in opposing pairs. The first two of these are shown in Figure 19A which shows the structure after only the first level is constructed. The second pair of control gate signals (1350A and 1350B) are shown in Figure 25A as being shared with transistors in the second level. Thus, after complete formation by etching patterned by third level pillar strips, the pillars at the second level (items 1362) have opposing memory cells in one direction controlled by control signals shared with memory cells in level 1 (1350A and 1350B), and the

control gates for the other two opposing memory cells are controlled by signals shared with the memory cells in the third level (1364A and 1364B). Ex. 1007, [0168]. The pairs of control signal conductors are perpendicular to each other.



Ex. 1007, Figure 26, annotated.

60. Figure 23C is a cross section of the embodiment at the stage of its construction after the second level of pillar strips have been etched. Ex. 1007, [0161]. It shows the cross section along cut 23C shown in Figure 23B. In particular it is a cross section through the level 1 control gate conductor 1332 for the level 1 memory cells facing each other in pillars A, B, C, D, E, and F underlying second level pillar strips 1340, annotated in Figure 23B, below.

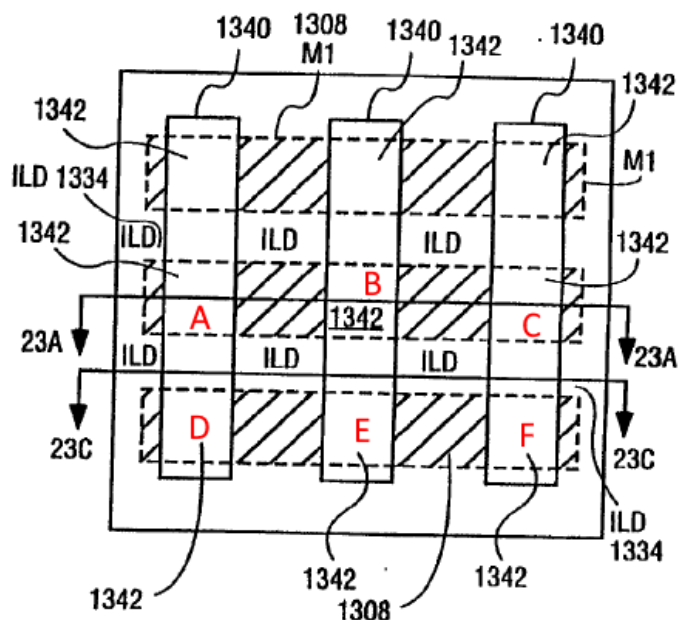


FIG. 23B

Ex. 1007, Figure 23B, annotated.

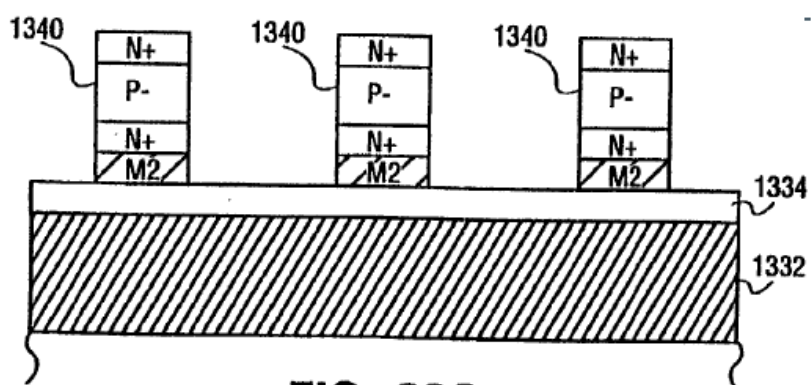


FIG. 23C

Ex. 1007, Figure 23C.

61. This idea of different conductors connecting devices in different directions is carried forward into the metal M1, M2, M3 and (ultimately M4 and beyond) which connect up the N+ sources and drains of the memory cell transistors.

M1 and M3 are laid out in one direction, and M2 and M4 connect memory cell N+ sources and drains in the perpendicular direction. Ex. 1007, Figures 13, 20, 27.

62. This embodiment is an intricate and beautiful jigsaw puzzle that can be difficult to visualize. But when all the memory cells and their interconnects are laid out, the circuit Lee implemented is a NOR architecture EEPROM with a virtual ground array (VGA). Ex. 1007, [0014]. A NOR VGA architecture is illustrated in Figure 1.28 of Ex. 2044 (Basics of Non-Volatile Semiconductor Memory Devices), as explained on pp. 34-35.

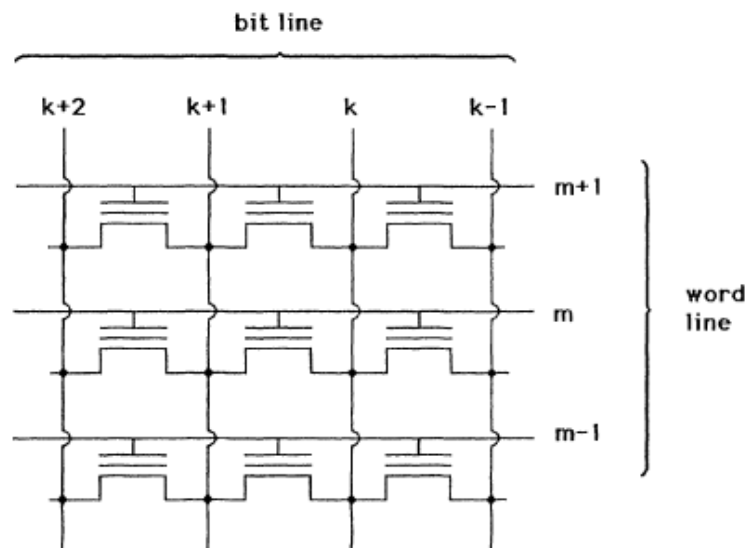


Figure 1.28 The virtual ground array architecture [1.70, 1.73, 1.74]. In this architecture, the common ground line in the array, as well as the drain contact in each memory cell, is eliminated.

Ex. 2044 (Basics of Non-Volatile Semiconductor Memory Devices), p. 35, Figure 1.28.

63. The essential characteristics of a NOR VGA device is that each EEPROM memory cell is connected to two bit lines connected to its source and drain terminals and one word-line connected to its control gate input. By controlling the voltages on a word-line and the two bit-lines, a cell can be read, erased or programmed. Ex. 1007, [0014]; Ex 1026, 38:9-39:29.

64. Lee's embodiment of Figures 13-28 is inexorably a VGA NOR EEPROM array. I annotated 4 pillars from Lee's Figures 13-28 as A, B, C, and D, shown for example in Figure 23B:

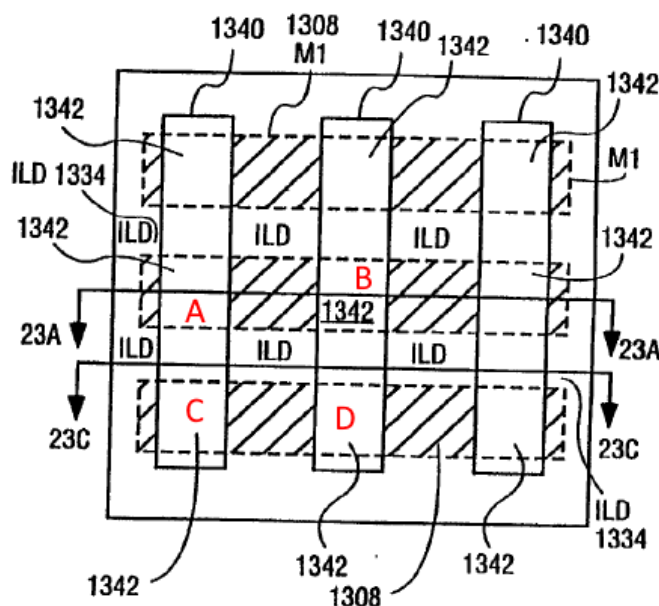
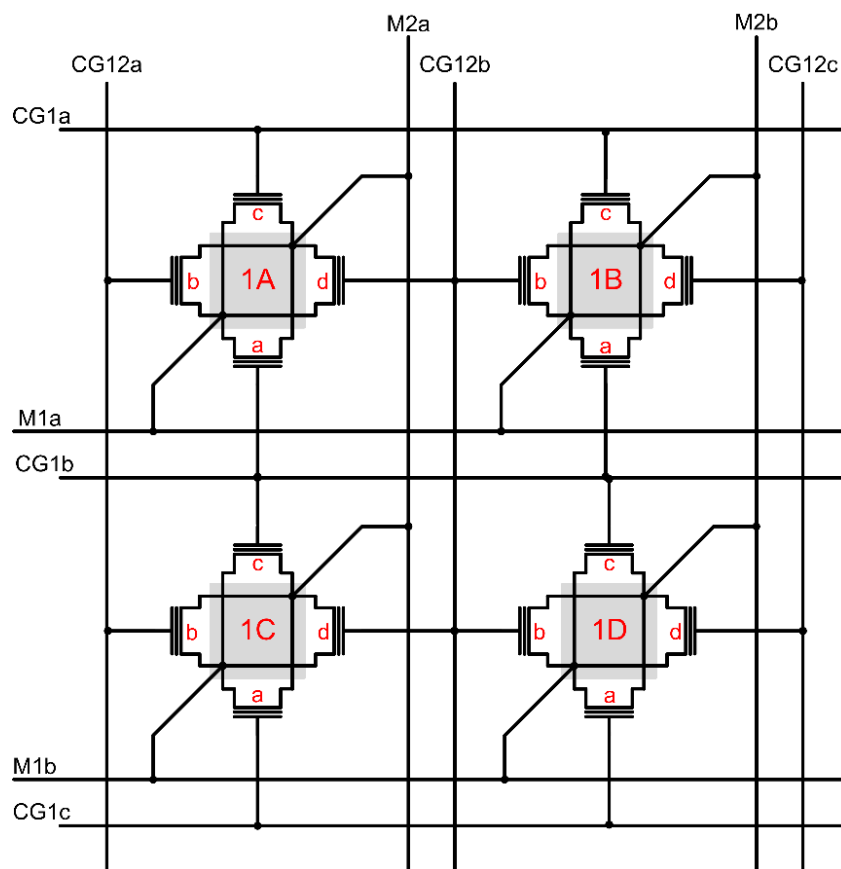


FIG. 23B

Ex. 1007, Figure 23B, annotated.

65. Each of these four pillars would include 4 memory cells on each level and would include three such levels as shown in Figure 27. The schematic for the 16

memory cells on the lowest level (bottom level of each pillar) is derived from Figures 23 and 27 of Lee by following each of the metal lines and control gate conductors and seeing which transistors are connected to which lines. This I have done and the results for level 1 are presented below:

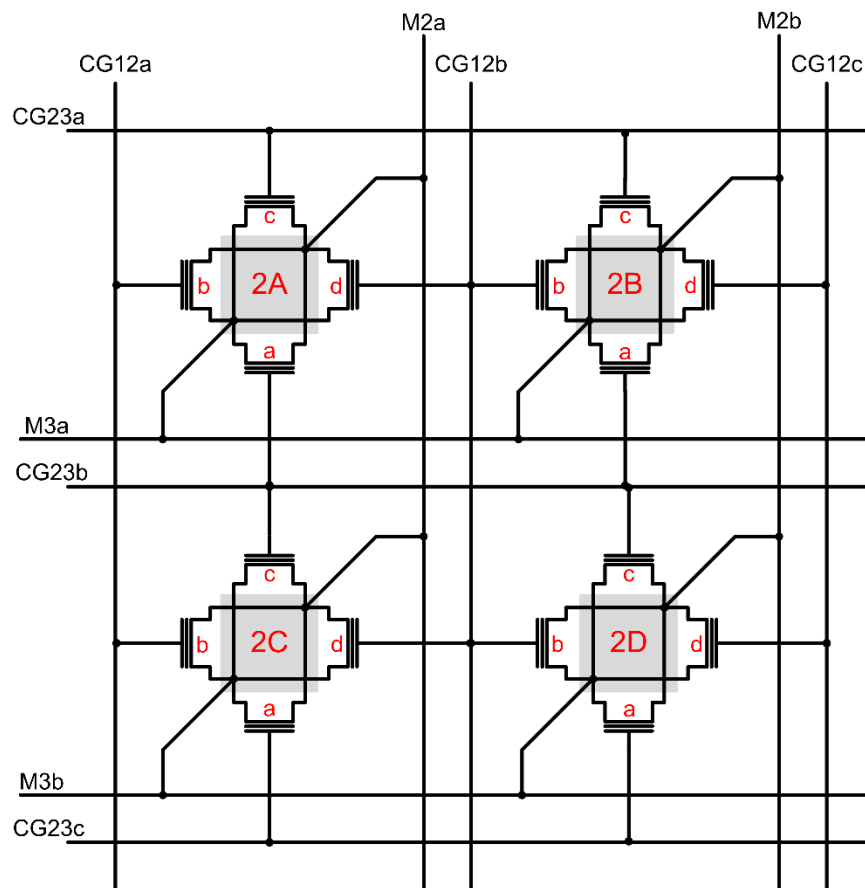


Ex. 1007, Figures 23, 27, transformed into a schematic of level 1.

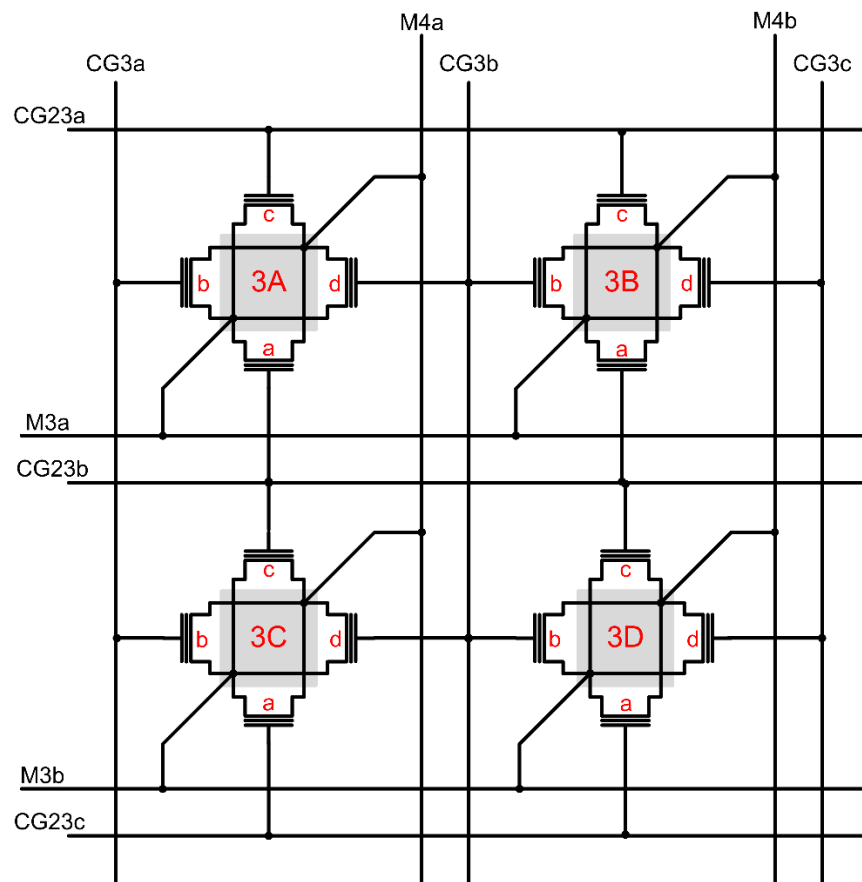
66. The M1 wires under these 4 pillars are annotated M1a and M1b by me for clarity. The M2 wires in the middle of these pillars, deposited orthogonally to the M1 wires, are called M2a and M2b here by me. There are a total of 6 control gate conductors which traverse this portion of the memory array at this level. They

correspond to word-lines. The three traversing the memory array in the same direction as M1a and M1b I have called CG1a, CG1b and CG1c. Per Lee's Figure 23C, these connect to the control gates of memory cells only in level 1. The control gate conductors that control memory cells in levels 1 and 2 are here labelled CG12a, CG12b, CG12c. They transverse this 2x2 array of pillars in the perpendicular direction to that of the CG1a,b,c conductors. The four transistors along the boundaries of pillar A in level 1 are labelled here 1Aa,b,c,d.

67. Comparable circuit schematics for the transistors in these pillars in levels 2 and 3 are presented below. The same naming convention is used here as in the above schematic of level 1.



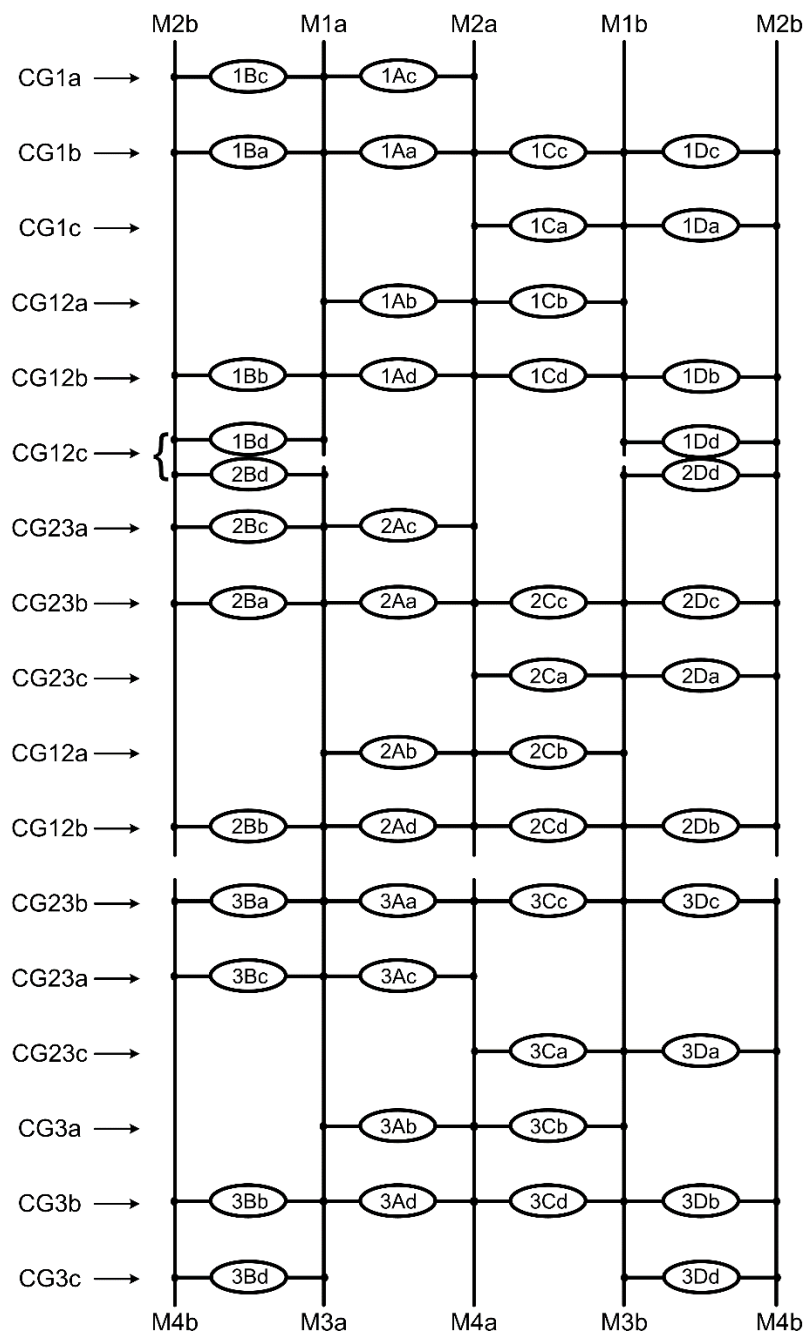
Ex. 1007, Figures 23, 27, transformed into a schematic of level 2.



Ex. 1007, Figures 23, 27, transformed into a schematic of level 3.

68. These three schematics are part of one circuit comprising 4 pillars, 8 metal conductors (or bit-lines), 12 control gate conductors (or word-lines) and 48 memory cells. The following table is organized in the same fashion as the NOR VGA memory array shown above from Ex. 2044. Ex. 2044 (Basics of Non-Volatile Semiconductor Memory Devices), p. 35, Figure 1.28. All the metal bit-lines are shown vertically; all the control gate conductors for all three levels are shown horizontally. Each memory cell in the four pillars is represented by an oval. The row the oval is in indicates which control gate conductor/word-line controls that memory

cell, and the two metal bit-lines coupled to the cell are connected to the oval by horizontal lines. Because of the complex interplay of the layout and circuit configuration some control gate conductors and metal bit-lines are duplicated to simplify the presentation of the overall circuit.



Ex. 1007, Figures 23, 27, transformed into a circuit schematic.

69. That the Lee embodiment of Figures 13-28 implements a NOR VGA architecture is now clear. Each memory cell is controlled by a word-line and is coupled to two bit-lines. Each memory cell can be read, programmed, or erased by adjusting the voltages and states of the corresponding 3 lines.

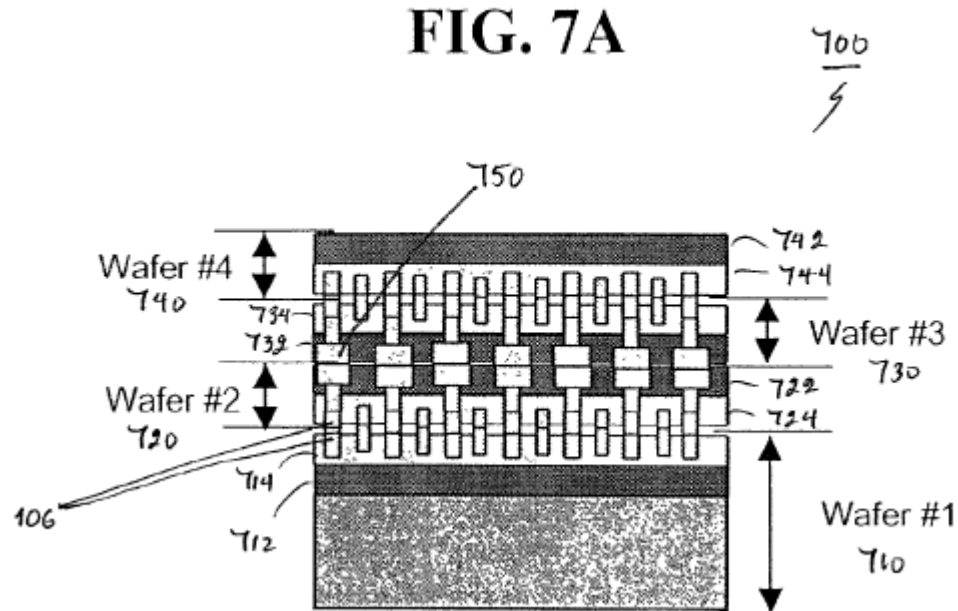
70. Lee's process of creating the monolithic three-dimensional arrays relies heavily on chemical mechanical polishing or "CMP." This is a technique for leveling the top surface of a wafer by grinding down all the undulations formed by the processing steps. Ex. 1007 (Lee), 11:33-65; Ex. 2033 (Fundamentals of Semiconductor Manufacturing), p. 61 ("The CMP process consists of moving the sample surface against a pad that carries slurry between the sample surface and the pad. Abrasive particles in the slurry cause mechanical damage on the sample surface, loosening the material for enhanced chemical attack or fracturing off the pieces of surface into a slurry where they dissolve or are swept away."). For example, Lee (Ex. 1007, 65:7-16) describes how a polysilicon layer is added on top of and into the canyons of Figure 88C and then, using, for example, CMP, the top surface is made smooth again, as shown in Figure 88D.

B. U.S. Patent Application Publication No. 2003/0157748 (“Kim”) (Exhibit 1008)

71. The Petition relies on Kim as a secondary reference for a subset of the Petition’s grounds (Grounds 1C, 1D, 2B, and 3). Petition, p. 3. For purposes of my analysis, I have been asked to assume that Kim is prior art.

72. Kim discloses “[a] method of vertically stacking wafers ... to form [a] three-dimensional (3D) wafer stack.” Ex. 1008 (Kim), Abstract. Kim’s “wafer stack” or “non-monolithic device” includes “selectively depositing a plurality of metallic lines on opposing surfaces of adjacent wafers; [and] bonding the adjacent wafers, via the metallic lines” Ex. 1008 (Kim), Abstract.

73. Kim discloses a method of creating a stack of semiconductor wafers each including an active silicon layer, an interlayer dielectric layer and metallization. By mirroring the top level metallization on a first and second wafer, the second can be flipped over and metal-to-metal bonded to the first wafer. After the pair are bonded together, the topmost of the pair (wafer 2) can be thinned to remove the supporting substrate from it. Subsequent pairs of wafers can be further metal-to-metal bonded to the first pair by etching vias through the second and third wafers and forming contact pads of their respective “bottoms” that can be aligned and mated/bonded to each other.



Ex. 1008 (Kim), Figure 7A.

C. “The Generic Nature of the Smart-Cut Process for Thin Film Transfer” (“Aspar”) (Exhibit 1009)

74. Aspar is an academic article published in 2001 in the Journal of Electronic Material (Vol. 30, No. 7, pp. 834-840). For purposes of my analysis, I have been asked to assume that Aspar is prior art.

75. Aspar was about a method of creating a weakness in a silicon wafer below the surface of the wafer to provide a cleavage plane along which the top of the wafer, and any layers above it can be separated from the bulk of the wafer. This provides a mechanism for creating silicon-on-insulator wafers with thin top silicon layers. Ex. 1009 (Aspar), p. 837 (“The Smart-Cut process is well suited to obtaining SOI wafers, especially for very thin top silicon layers <1.5 μm .”; “Furthermore, this

technique enabled us to obtain very good crystalline quality of the top silicon layer.”), p. 836 (“When the implanted wafer is bonded to a stiffener, splitting can be obtained on the full wafer.”).

76. The Petition asserts Aspar as a secondary reference for a subset of the Petition’s grounds (Grounds 1E, 1F, and 2C). Petition, p. 3. Aspar taught a “Smart-Cut® process,” which permitted “transfer of a thin layer from the substrate A onto the support B” to effect wafer stacking, which “is particularly advantageous when a thin monocrystalline layer is required on a support which does not allow epitaxy of this layer.” Ex. 1009 (Aspar), p. 834.

77. Further, multiple layers can be stacked on top of each other to create complex multi-layer structures, though the details of how such structure would be integrated with metallization and interconnections generally are not disclosed.

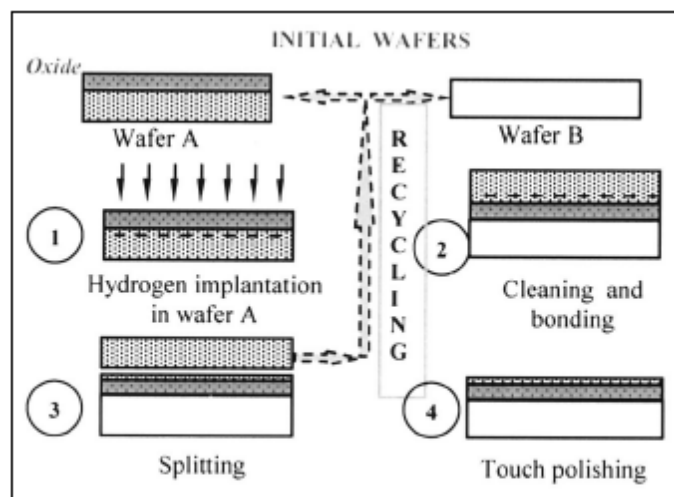


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

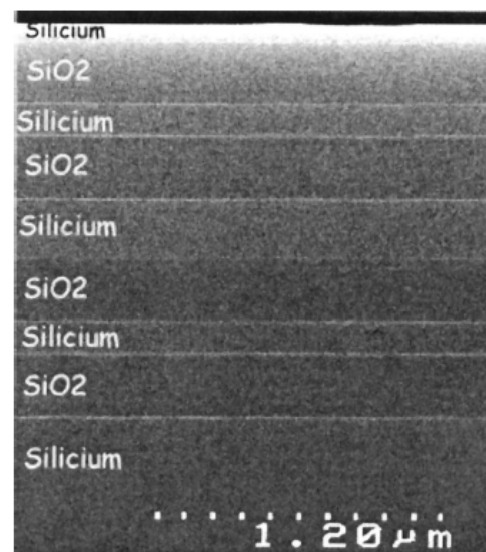


Fig 14. SEM view of multiple SOI layer stack.

Ex. 1009 (Aspar), Figures 1, 14.

78. Aspar and its related references describe how hydrogen implantation occurs after the formation of the oxide layer. Ex. 1009 (Aspar), Figure 1; Ex. 1023 (Srikrishnan), Figures 2, 4, 6, 4:56-5:15. The depth of the greatest concentration of H⁺ ions within the Wafer A determines where Wafer A will cleave in Step 3. Ex. 1009 (Aspar), p. 834 (“Ion implantation (hydrogen, helium) induces formation of an in-depth weakened layer, located at the mean ion penetration depth, which leads to delamination of a thin film from a thick substrate”; “Hydrogen is implanted in a substrate A. This step induces formation of an in-depth weakened layer”), p. 835 (“platelets or microcavities confined around the maximum hydrogen concentration depth (Rp) can be found”). The depth Rp is determined by the energy of the H⁺ ions implanted into Wafer A. Ex. 1023 (Srikrishnan), 5:4-14 (“[T]he proper implantation

voltage can be selected so as to have the peak of the implanted hydrogen occur at the desired depth below the etch stop layer.”). The experiments presented by Aspar required implantations energy of around 70 keV. Ex. 1009 (Aspar) at 836. Deeper cleavage planes would require higher implantation energies, which in turn would cause more damage to the layers the H⁺ ions were passing through. Ex. 1009 (Aspar), p. 836.

79. As shown above in Figure 14, Aspar discloses that the layer transfer process can be repeated several times on a same structure to realize complex, multi-layer structures. Figure 14 shows alternating layers of silicon (labelled “Silicium”) and silicon dioxide. As disclosed, one iteration of the Smart-Cut© process deposits one additional pair of uniform silicon–silicon dioxide layers. One such pair is what is transferred from “Wafer A” onto “Wafer B” in steps 1 through 4 of Figure 1 in Aspar. No other complex structure other than this alternating Si/SiO₂ SOI structure is disclosed by Aspar.

D. U.S. Patent No. 6,034,882 (“Johnson”) (Exhibit 1010)

80. Johnson is asserted against Claim 13 in each of Grounds 2A-2C. Petition, p. 3. For purposes of my analysis, I have been asked to assume that Johnson is prior art.

81. As shown in Figure 4(b), Johnson was directed to a cross-point memory architecture where memory cells reside at the intersection of word-lines and bit-

lines. Johnson disclosed the “fabrication sequence” for a memory cell in Figures 6(b)-6(g). Ex. 1010 (Johnson), 12:42-43.

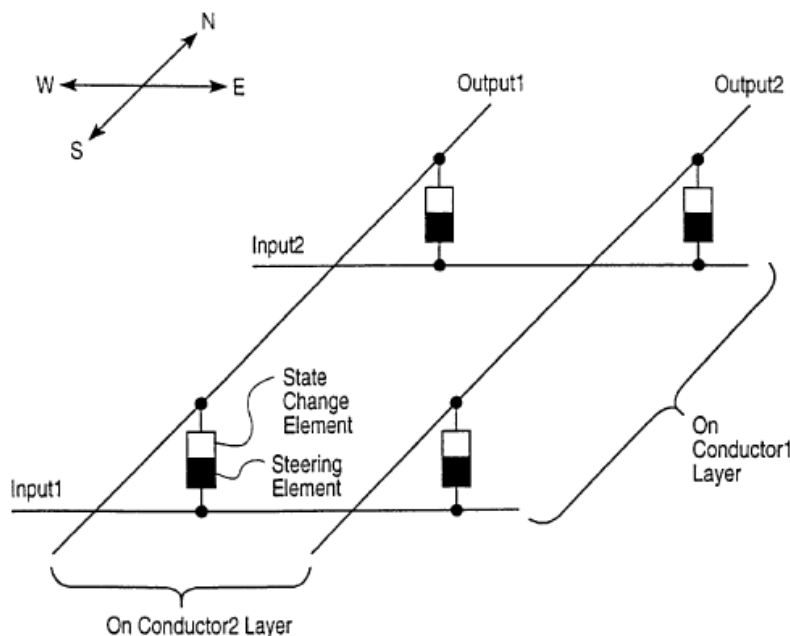


FIG. 4(b)

Ex. 1010 (Johnson), Figure 4(b).

82. Further, Johnson is principally drafted toward the creation of stacked two-terminal state change element and a diode-based steering element in which each storage element is formed at the intersection of perpendicularly oriented conductors.

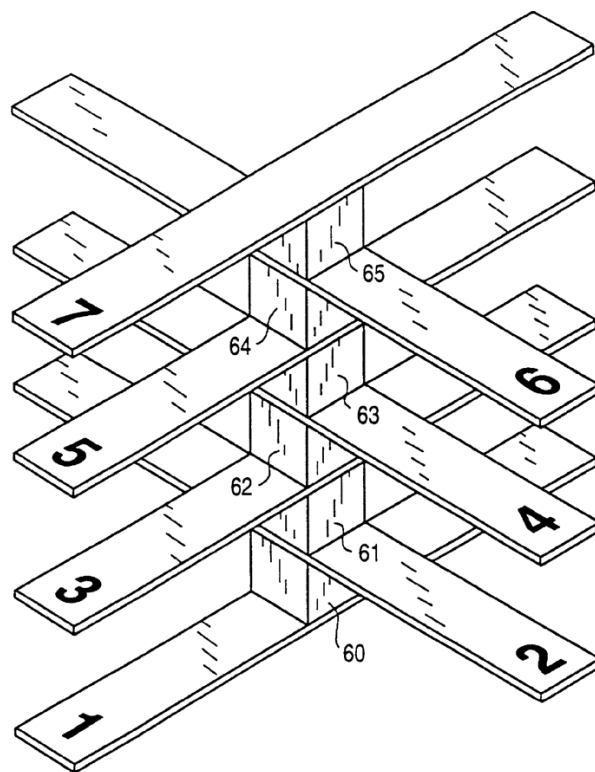


FIG. 8(a)

Ex. 1010 (Johnson), Figure 8A.

E. US. Patent No. 5,571,730 (“Park”) (Exhibit 1011)

83. The Petition relies on Park solely for its Ground 3 challenge to Claim 1. Petition, p. 3. For purposes of my analysis, I have been asked to assume that Park is prior art.

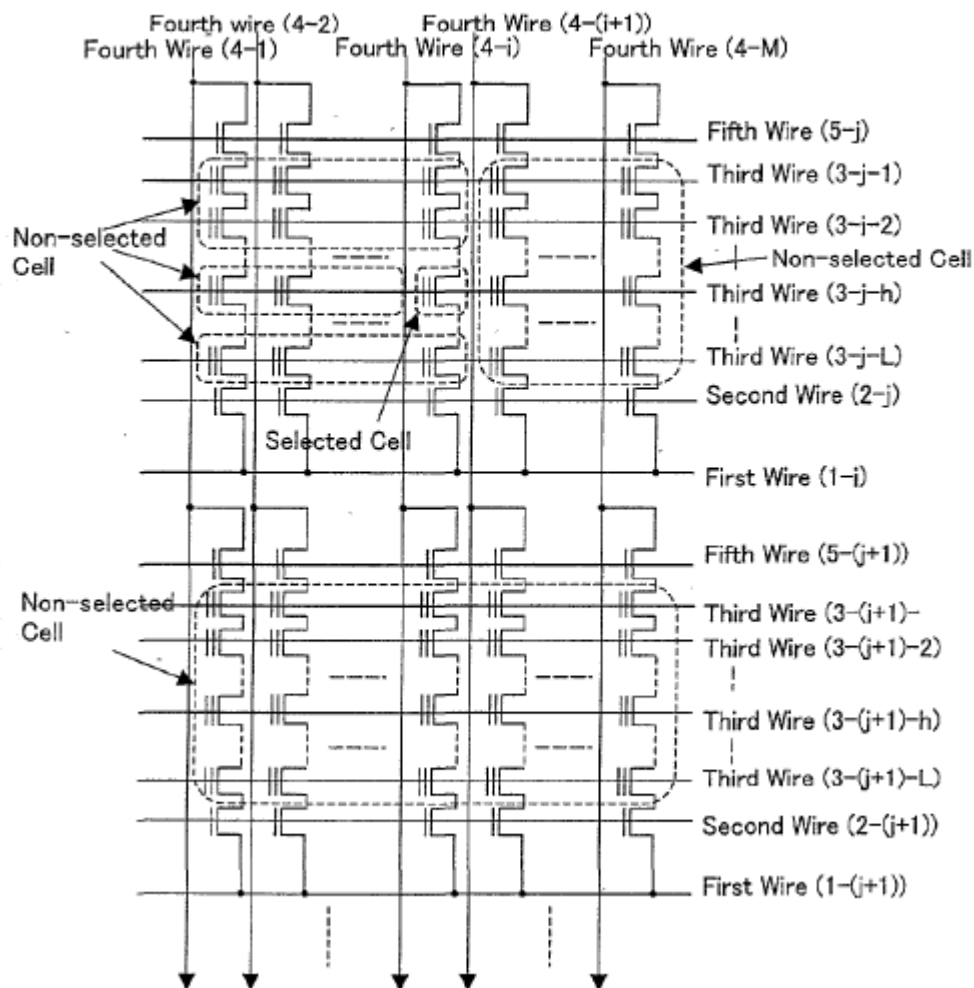
84. Park disclosed DRAM memory cells that share gate electrodes. Ex. 1011 (Park), 5:49-53, Figures 7, 9. Figures 8-9 show a dielectric film 64 that is an integral part of the capacitors of each individual memory cell. Ex. 1011 (Park), 5:36-43, Figures 8-9.

F. U.S. Patent Application Publication No. 2002/0154556 (“Endoh”) (Exhibit 1012)

85. Endoh is a massive patent application filed in 2002 with 1660 figures and 1664 paragraphs in the specification. For purposes of my analysis, I have been asked to assume that Endoh is prior art.

86. Endoh “relates to a semiconductor memory and its production process.” Ex. 1012 (Endoh), [0003]. The “Description of Related Art” states that: “As a memory cell of an EEPROM, is known a device of a MOS transistor structure having a charge storage layer and a control gate in a gate portion, in which an electric charge is injected into and released from the charge storage layer by use of a tunnel current.” Ex. 1012 (Endoh), [0004]. Endoh includes numerous sequences of figures and descriptions that describe the sequences of steps needed to fabricate the semiconductor memory and the circuitry implemented therein.

Fig. 65



Ex. 1012 (Endoh). Figure 65 above shows the NAND memory array implemented in an embodiment of Endoh.

X. CLAIM CONSTRUCTION ANALYSIS

87. Petitioner has proposed constructions for (1) “stackable add-on layer ... the stackable add-on layer [is]/[being] bonded” in Claims 1 and 13, and (2) “SOI pillar” in Claims 14-17.

A. “stackable add-on layer ... the stackable add-on layer [is]/[being] bonded” (Claims 1, 13)

88. I have not been asked to provide an opinion on the construction of “stackable add-on layer.” I have been asked to assume that Intel’s proposed construction is correct and apply it as appropriate in my analysis for purposes of responding to Dr. Sechen’s opinions.

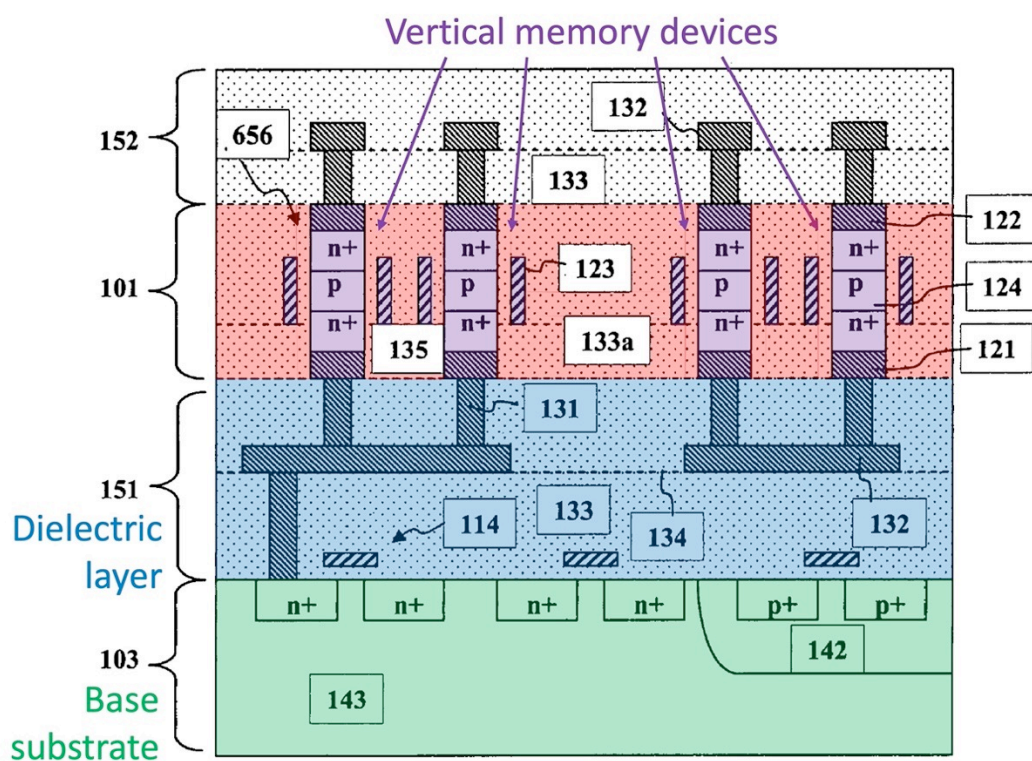
B. “SOI pillar” (Claims 14-17)

89. In its Petition, Intel argued that “SOI pillar” should be construed to mean “a pillar-shaped doped stacked structure formed in a stackable add-on layer added using SOI technology.” Petition, p. 16. In its decision instituting this review, the Board preliminarily adopted Petitioner’s proposed construction. Institution Decision, p. 12. As explained below, I disagree with Petitioner’s proffered construction.

90. As explained in the ’702 Patent specification, “SOI” is an acronym for “Silicon-on-Insulator.” Ex. 1001 (’702 Patent), 4:45-46. Petitioner and its expert both agree. Petition, p. 4 (“In the ’702 Patent, ‘[t]he acronym ‘SOI’ generally refers to Silicon-on-Insulator”); Ex. 1003 (Sechen Declaration) ¶ 87 (same). A POSITA would be familiar with this term and understand it to refer to a semiconductor device structure in which silicon structures are fabricated on or above an insulating layer. A variety of different types of insulating layers were understood by artisans in 2004.

One possibility was to have the insulating layer be an entire supporting wafer, such as sapphire wafer. In SOI embodiments of the '702 Patent, the supporting wafer is a traditional silicon wafer, and the insulation layer is a layer of silicon dioxide located above that substrate.

Fig. 1



Ex. 1001 ('702 Patent), Figure 1, showing silicon substrate 143, insulating layer 133, and SOI pillar 124, annotated.

91. Other figures show comparable structures that depict SOI pillars.

Fig. 4

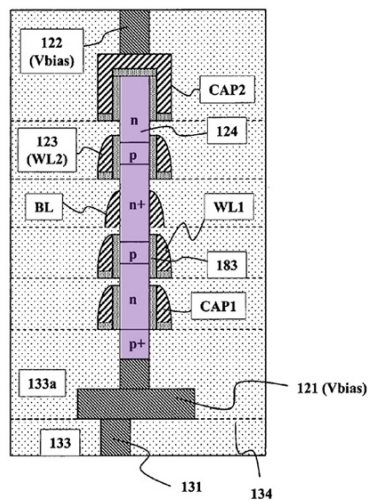


Fig. 20

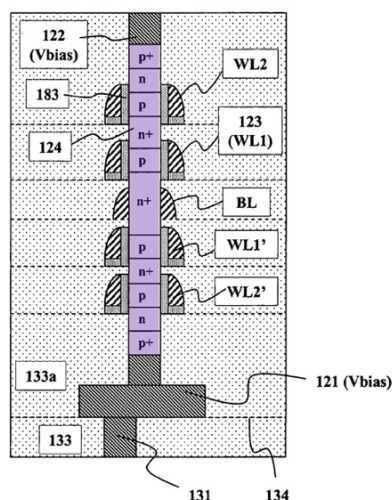
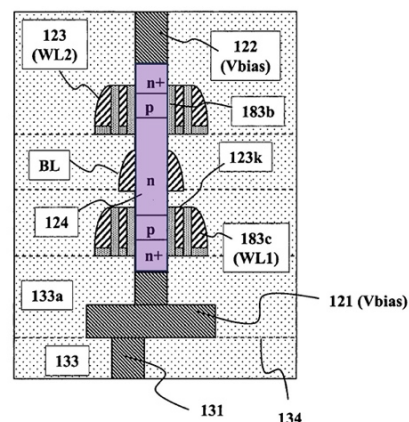


Fig. 27



Ex. 1001 ('702 Patent), Figs. 4, 20, 27 (depicting SOI pillars).

92. For Figure 4, the '702 Patent explains that “the aspect ratio of SOI pillar 124 remains relatively small” given its larger height relative to its width. Ex. 1001 ('702 Patent), 8:5-10. Other references refer to similar structures as pillars, showing flash memories with “pillars” depicted as structures where the height is larger than the width:

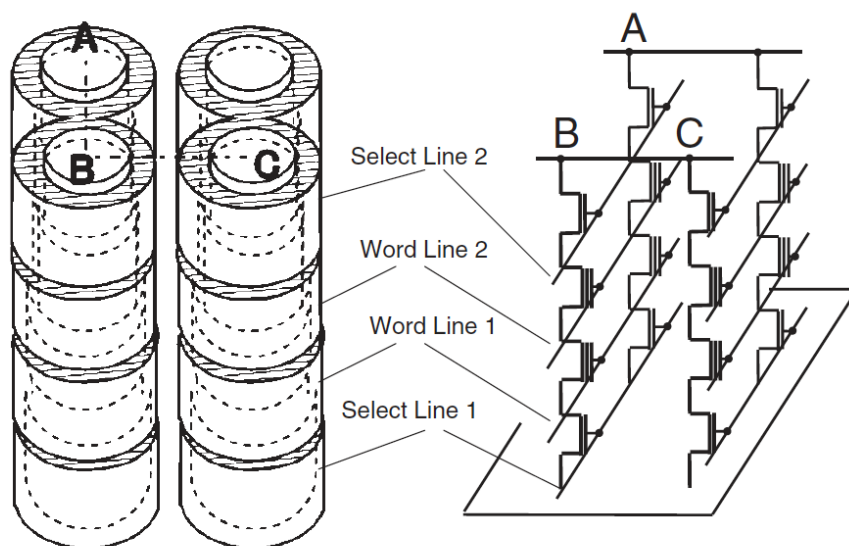
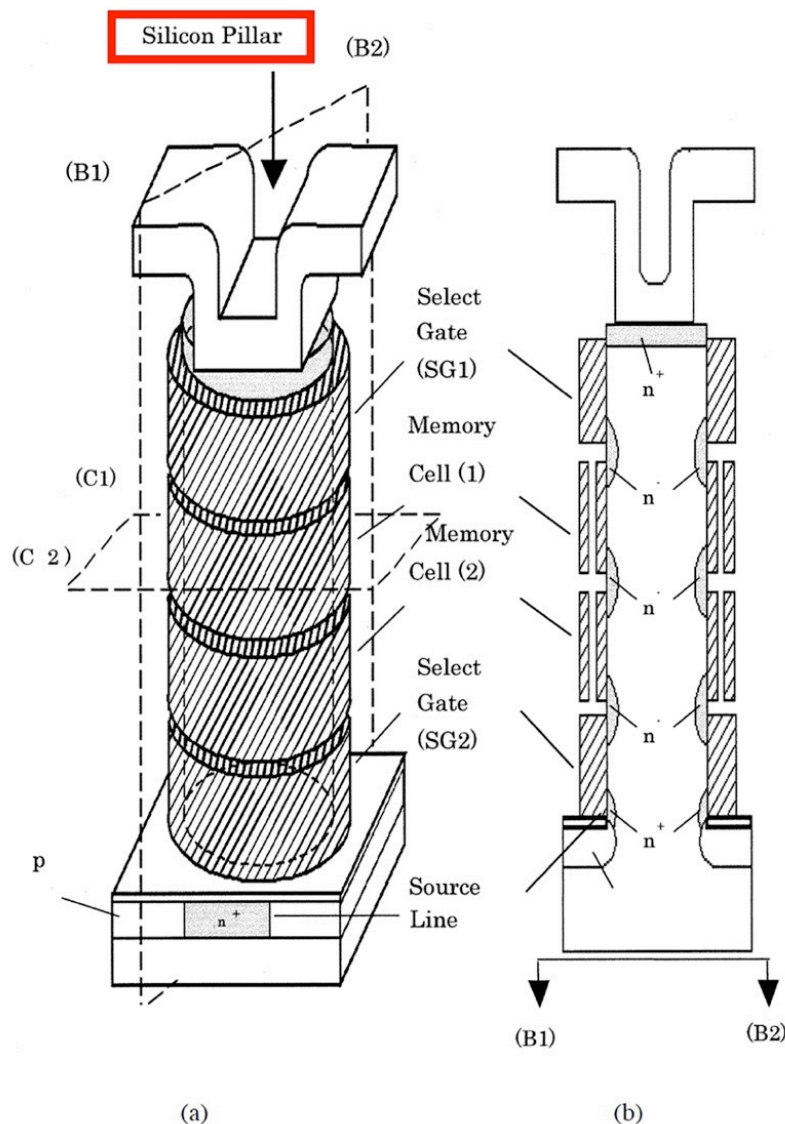


Fig. 1. Bird's eye view of the new three-dimensional high-density S-SGT flash memory and its equivalent circuit.

Ex. 2042 (Sakuraba), p. 2217, Fig. 1; *see also id.*, p. 2217 (“The new three-dimensional high density S-SGT flash memory is fabricated by arraying S-SGT *pillars*. Figure 1 shows the architecture and the equivalent circuit of the new three-dimensional high density S-SGT flash memory.” (emphasis added)).



Ex. 2041 (Novel Ultrahigh-Density Flash Memory), 947, Fig. 3(a)-(b), annotated; *see also id.*, Fig. 5 (showing SEM photograph of S-SGT structured cell with silicon pillars).

93. The '702 Patent specification does not define what a pillar, is but the English word has a plain and ordinary meaning. For example, Webster's New Universal Dictionary from 2003 defines "pillar" as "an upright shaft or structure, of

stone, brick, or other material, relatively slender in proportion to its height....”
Ex. 2031 (Webster’s), p. 1469. Random House Webster’s Dictionary from 1997 has the same definition. Ex. 2032 (Random House), p. 988. There is nothing in the ’702 Patent to suggest the inventor intended the use of pillar to have any connotation other than its plain and ordinary meaning. The examples above from the ’702 Patent and other references indicate that “pillar” as used in the field of semiconductor memory structures and as understood by a POSITA is used according to its plain and ordinary meaning. Thus, the term “pillar” by itself means a structure that is taller than it is wide.

94. Thus, in the context of the present proceeding and the ’702 Patent, in my opinion an “SOI pillar” is “a silicon-on-insulator structure taller than it is wide.”

95. I understand that Dr. Sechen testified at deposition that a plain and ordinary meaning of “pillar” exists, but that he had not looked at any dictionaries and had not even attempted a definition. Ex. 2039 (Sechen Deposition), 17:14-22:2. Therefore, in my opinion, to the extent Petitioner’s construction of “pillar” is based on Dr. Sechen, it is unsupported.

XI. REBUTTAL OF THE PETITION’S ARGUMENTS

A. Ground 1A: Obviousness over Lee (Claims 13–17)

96. In Ground 1A, the Petition asserts obviousness of Claims 13-17 based on Lee. Petition, pp. 3, 16.

1. Claims 13-15

97. I have not been asked to opine on whether Claims 13-15 would have been obvious over Lee as specified in Ground 1A.

2. Claim 16

98. Beginning on page 37, Petitioner asserts that Lee discloses or suggests Claim 16's additional limitations, relying exclusively on Figure 25A. Petition, pp. 37-39. This is not true because the two memory cells in Lee's Figure 25A that the Petition points to are not serially connected. Instead, they are connected in parallel.

99. As explained above (in Section IX.A) with respect to the principal embodiment of Figures 13-28 of Lee and the associated text, Figure 25 shows an intermediate step in the fabrication of a 3-dimensional NOR VGA EEPROM memory array. In the completed memory array, each of the two portions of the joint pillar shown in Figure 25A (annotated below in blue and red) forms four non-volatile charge-trapping memory cells as shown in Figure 26 (annotated below). The bottom collection of memory cells (shaded in red below) share an M1 bit-line with other pillars in a first direction, and an M2 bit-line with other pillars in the direction perpendicular to the first direction. The four memory cells in the upper portion of the pillar (shaded in blue below) share the same M2 bit-line with the lower four memory cells. In the final memory array, there is also a M3 bit line on top of the

topmost N⁺ regions that run parallel to the M1 bit-line at the bottom. This M3 bit-line is shown in Figure 27A.

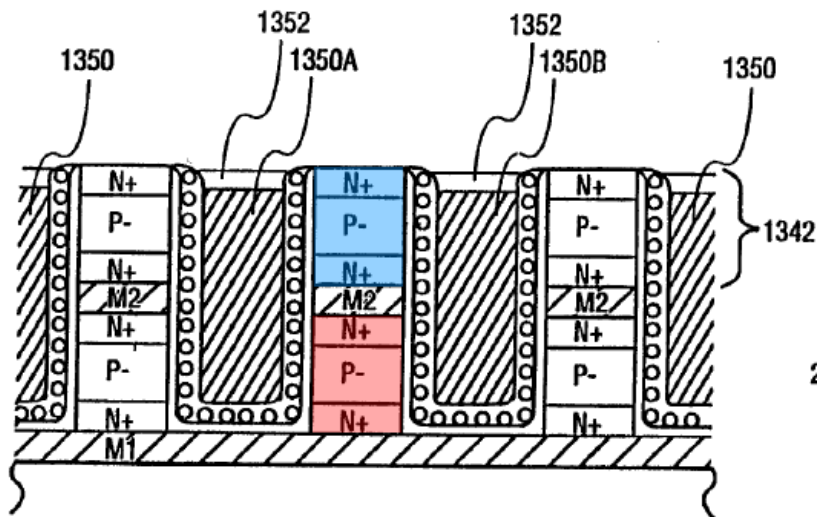


FIG. 25A

Ex. 1007, Figure 25A, annotated.

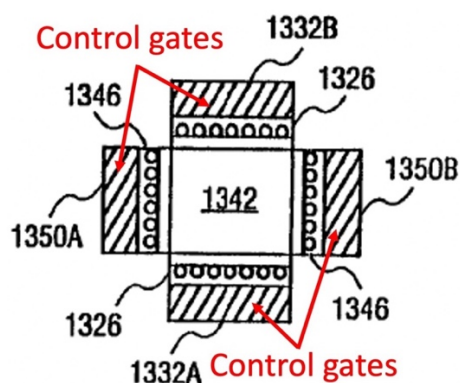


FIG. 26

Ex. 1007, Figure 26, annotated.

100. As described above (in Section IX.A), Figure 25 is an intermediate step towards the fabrication of a NOR VGA EEPROM memory array. Petitioner's expert

Dr. Sechen agreed. Ex. 2039 (Sechen Deposition), 59:17-60:7. As also explained above, NOR memory arrays have their memory arrays arranged in parallel, not in series because during normal operation, the current never flows from one memory cell into another. When one memory cell is being accessed, the voltages applied to the other memory cells adjacent are such that the adjacent cells do not influence the access of the memory cell in question. Ex. 1007, [0014]. The memory cells in the top and bottom portions of the final pillars of the NOR VGA array constructed by the process of Figures 13-28 and the associated text (of which Figure 25 shows an intermediate form) are not serially connected. During his deposition, Dr. Sechen agreed. Ex. 2039 (Sechen Deposition), 53:3-22.

3. Claim 17

101. Claim 17 of the '702 Patent depends on Claim 16. As explained above, Petitioner has failed to show that Claim 16 is rendered obvious by Lee. Further, Petitioner claims that two of the pillars illustrated in Figure 25 are “serially connected” via M1 to each other. Petition, pp. 39-40. This is not true. As also explained above, the M1 shown in Figure 25 is a bit-line that is used to access one of the devices in one of the pillars at a time. There is never any current flow from one pillar, through the M1 conductor into another pillar, as would be required to satisfy the serial connection aspect of Claim 17. For this reason as well, Lee does not render obvious Claim 17.

B. Ground 1B: Obviousness over Lee and Endoh (Claims 16-17)

102. In Ground 1B, the Petition asserts obviousness of Claims 16-17 based on the combination of Lee and Endoh. Petition, pp. 3, 41. I disagree.

1. Claims 13-15

103. Ground 1B only challenges Claims 16-17. I have not been asked to opine on whether Claims 13-15 alone would have been obvious over Lee and Endoh.

2. Claim 16

104. In Ground 1B, Petitioner looks to Endoh’s Production Example 52, illustrated in Figures 1171 and 1172, to find serial connections between memory cells within a single pillar and across two pillars coupled via an interconnect line and to use such a finding to rectify the deficiencies in Lee with respect to Claims 16 and 17. Petition, pp. 42-45.

105. Petitioner says, “A POSITA would have been motivated to modify Lee’s device level 3104 in array 3101 to incorporate two memory cells on each pillar as taught in Endoh.” Petition, p. 47. This is incongruous because the combination from the Petition’s Section VII.A (Ground 1A based on Lee) that the Petitioner is attempting to bolster is based on the disclosure of Figure 35 and paragraph [0111] in combination with Figure 1B. Petition, pp. 18-26. The embodiment of Figure 35 as described in paragraph [0111] already includes a monolithic three dimensional array of thin film devices. Array 3101 comprises a plurality of device levels 3104.

As suggested by Petitioner, Lee already discloses pillars comprising two levels of memory cells in, for example, Figure 25A. Petition, p. 47. Petitioner suggests that a POSITA would have been motivated to modify Lee's device layer 3104 in array 3101 to include two memory cells on each pillar. But Lee already discloses this with respect to Figure 35 (disclosing a plurality of device layers arranged vertically to form a 3-dimensional array of memory cells) and Figure 25A (showing stacks of memory cells in two levels). These two embodiments of Lee are already discussed by Petitioner as a combination with regard to Ground 1A. Petition, pp. 18-26, 37-39. Thus, the proposed modification is not simply to provide "two memory cells in each pillar," Petition, p. 47, but to specifically substitute Lee's multi-memory cell pillars (such as that of Figure 25A) with Endoh's two-level pillars.

106. Petitioner says that this proposed combination of Lee with Endoh would be motivated by a POSITA recognizing "that applying two memory cells in each pillar as taught in Endoh to Lee's level 3104 would further Lee's stated goals of increasing device density." Petition, p. 47. But this is backwards because Lee already teaches fabricating four memory cells per pillar per level, instead of just one as in Endoh. Ex. 1007, [0136], [0166]. Changing from Lee's pillars of Figure 25 to Endoh's pillar of Figure 1172 would likely decrease device density, not augment it.

107. Petitioner goes on to say that "[t]his combination merely amounts to using a known technique (implementing serial memory cells in a pillar as taught by

Endoh) to improve a similar known device (Lee’s memory array 3101) in the same way (serial memory cells in the same pillar to increase density).” Petition, p. 47. This is not true either. The suggested modification involves changing the NOR VGA EEPROM structure of the pillars of Lee with the NAND structures of Endoh. Such a change is so much more than “merely” using a known technique to improve a similar device. Petition, p. 47.

108. In NAND architecture, memory cells of an array are coupled together in series, source-to-drain, between a source line and a column bit line. NOR devices are not connected in series, source-to-drain, but are arranged in parallel, source-to-source and drain-to-drain, and, the case of a VGA NOR memory array, every source and drain connected to a bitline. Dr. Sechen admits that Endoh’s Figures 1171 and 1172 use NAND architecture. Ex. 2039 (Sechen Deposition), 124:4-19 (“Q. Are these figures showing a NAND memory configuration? A. Yes.”).

109. Petitioner fails to recognize the fundamental differences between Lee and Endoh that would prevent a POSITA from being able to make such a modification, or, alternatively, having any expectation of success in such an effort.

110. The differences between Lee’s NOR VGA array structure and Endoh’s NAND array structure are manifest. They extend well beyond what a superficial comparison of figures 25A and 1171, respectively, would reveal. They are present at the physical level (the physical structures that implement the memory array and

the manufacturing processes that create them), the circuit level (the circuits that make up the memory arrays and the peripheral circuits in the two references), the logical level (the command structures and resulting behaviors). For example, the number and orientation of the control gates need to change. In Lee's Figure 25A, the control gate structures would have to be modified to provide separate control gate signals for each memory cell in each level of the structure and include routing paths for each of those control gates. The addition of select transistors needs to be figured out. The configuration of the bit-lines is different, and the sense amplifiers sensing and driving bits of information into and out of the memory array would have to change. The address decoders would have to change as would the control circuits directing read, program and erase operations, as the details of these operations would have to change to facilitate a change from NOR to NAND flash memory. Indeed, because the read, program, and erase procedures are closely coupled to the specific type and configuration of the memory array, the peripheral circuitry which includes the sense amplifiers, address decoders, and voltage generators and control logic and sequencers are different between those of a NOR flash/EEPROM memory array as found in Lee's Figure 25A, and those interfacing with a NAND flash/EEPROM memory array as found, for example, in Endoh's Figures 1171-1172. In brief then, this change is not *trivial* as suggested by Petitioner, but would be *complete*. Every part of Lee's embodiment disclosing a NOR VGA memory device would have to be

redone to the point where little of substance would remain of Lee in the proposed combination of Lee and Endoh.

111. Finally, the magnitude of the task and the subtlety of the engineering of a pillar-oriented NAND EEPROM memory array and integrated circuit generally would be daunting to a POSITA, eliminating any reasonable expectation of success that he/she might have. This is illustrated by the straightforward comparison of the circuits for a NAND Flash memory array and a NOR VGA memory array, placed here side by side.

Fig. 65

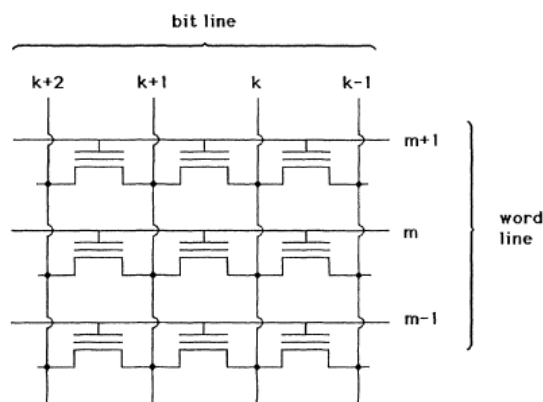
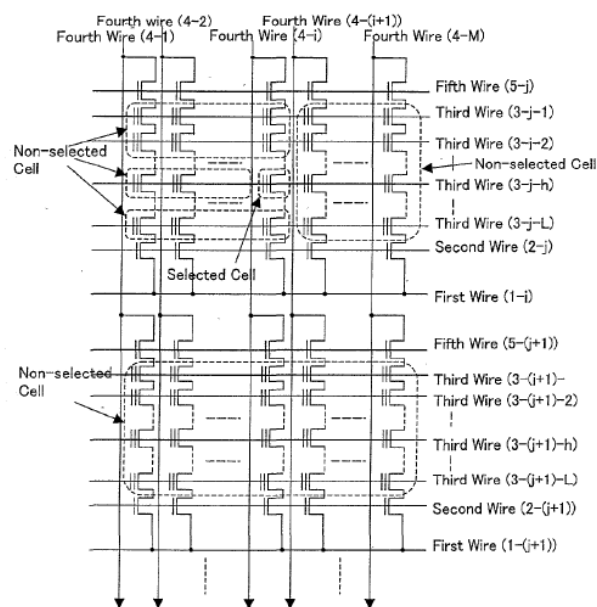


Figure 1.28 The virtual ground array architecture [1.70, 1.73, 1.74]. In this architecture, the common ground line in the array, as well as the drain contact in each memory cell, is eliminated.

Ex. 1012 (Endoh), Figure 65; Ex. 2044 (Basics of Non-Volatile Semiconductor Memory Devices), p. 35, Figure 1.28.

3. Claim 17

112. Claim 17 of the '702 Patent depends on Claim 16. As Petitioner has failed to show that Claim 16 is rendered obvious by Lee in view of Endoh, Petitioner has also failed to show that Claim 17 is rendered obvious.

C. Ground 1C: Obviousness over Lee and Kim (Claims 13–17)

113. In Ground 1C, the Petition asserts obviousness of Claims 13-17 based on the combination of Lee and Kim. Petition, pp. 3, 50. I disagree.

114. Petitioner looks to Kim in Ground 1C for the stackable add-on layer element in Claim 13[c]. This combination fails for the following reasons.

1. No Motivation To Stack Lee's Interleaved Layers

115. Petitioner starts the discussion of the motivation to combine Lee with Kim with two inaccurate statements. First Petitioner says, "Lee does not clearly describe how the bottom level 3104 of array 3101 is formed on insulating layer 3102." Petition, p. 51. This is not so. A POSITA reading Lee understands that the premise underlying all of Lee's disclosure is fabrication using standard sequential deposition of layers using well known photolithographic processes. Indeed, Lee calls out the embodiment of Figure 35 as including "a three dimensional monolithic array [of] thin film transistors." Ex. 1007, [0111]. More specifically, Lee's Figure 35 shows a schematic of a three dimensional array of devices 3101 having "a plurality of device levels 3104, preferably separated by interlayer insulating layers."

Ex. 1007, [0111]. Lee explained that “layers of each level of the array were directly deposited on the layers of each underlying level of the array.” Ex. 1007, [0107]; *see also* Ex. 1007, [0122]. In addition, Figures 13-28 of Lee illustrated methods for forming a multilevel array of memory devices. Ex. 1007, [0052], [0147]-[0170]. Lee stated with respect to Figure 13 that “fabrication starts by providing a substrate 1300 on which the multilevel array of storage devices is to be formed” and that the “top surface 1306 of substrate 1300 will typically include an insulating layer.” Ex. 1007, [0147]. Lee further explained that the process involves “blanket depositing a first conductor layer 1308” on top of the insulating layer on “surface 1306.” Ex. 1007, [0148]. From these disclosures, a POSITA reading Lee would have understood that in Lee’s Figure 35, the bottom-most “device level 3104” would be deposited on “insulating layer 3102.” Dr. Sechen also agreed at his deposition that Lee describes various “fabrication steps” for forming the structure in Lee’s Figure 35. Ex. 2039 (Sechen Deposition), 88:2-89:6.

116. Per Petitioner’s definition of a POSITA or my own, these process steps would have been within a POSITA’s knowledge and experience. Petition, p. 9 (“at least three years of experience in the research, design, or development of semiconductor memory device structures”). As a result, Petitioner’s next statement (“Consequently, a POSITA would have looked to other art, such as Kim, for details

about attaching bottom level 3104 to insulating layer 3102”) is not supported. Petition, p. 51.

117. Second, Petitioner suggests that “a POSITA, at the suggestion of Lee, was looking to separately form a two-dimensional array of memory devices and ‘package [it] together.’” Petition, p. 51, citing ultimately to Ex. 1007, [0107]. This completely mischaracterizes paragraph [0107] of Lee. This paragraph actually says the opposite:

One method of improving device density is to arrange the devices in a monolithic three dimensional array of charge storage devices comprising a plurality of device levels. The term “monolithic” means that layers of each level of the array were directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device.

Ex. 1007, [0107].

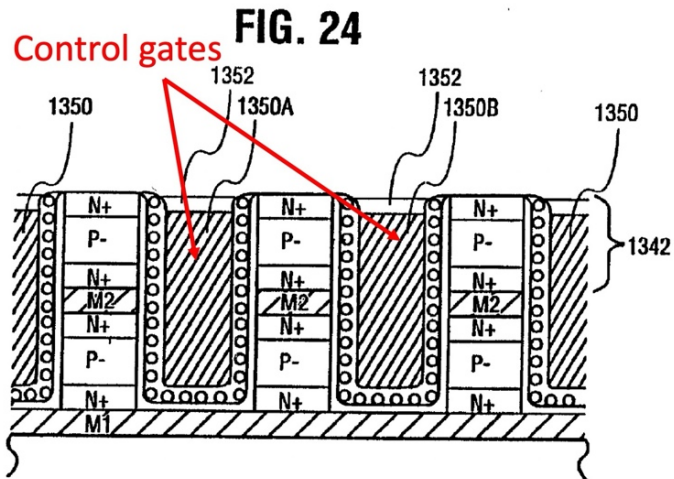
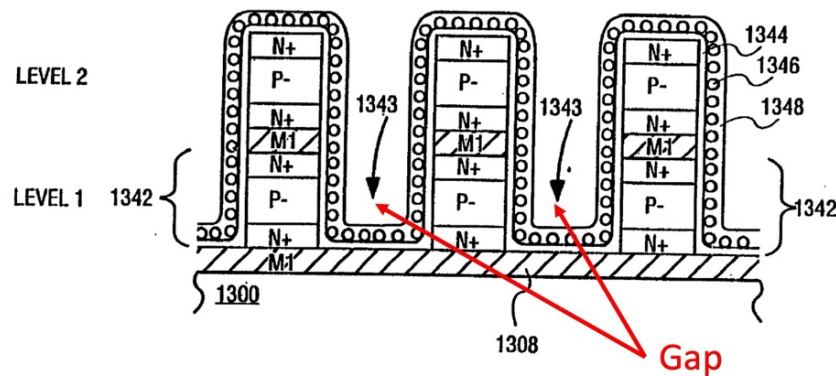
118. This says that monolithic deposition of layers is preferred and that nonmonolithic formation and assembly of two-dimensional arrays is not the same and, by implication, does not accrue the same benefits. In particular, Lee says that cost of memory is decreased if device density is increased, and this is accomplished through monolithic physical construction. Ex. 1007, [0106]-[0107]. As I explain

below, there is a reason Lee preferred monolithic structures. Lee’s use of interleaved control gates and using upper level layers to pattern lower levels in Lee’s embodiment of Figures 13-28 is a feature of Lee’s monolithic construction that could not be readily duplicated using non-monolithic techniques, because there is no clean horizontal partition point between the different levels of Lee. There is a complicated interplay between the successive addition of levels in Lee and the resulting three-dimensional structure of interconnected memory cells. There is no point along that sequence in which any Aspar-like process could be used to construct the same structures and at the same memory densities.

119. In my opinion, the Petition also suffers from another significant flaw. Petitioner and Dr. Sechen provide no reason to stack Lee’s levels which a POSITA would have understood to be interleaved. Both Petitioner and Dr. Sechen propose adding individual memory cells from Lee’s Figures 1A, 1B, 2, 7, or 25A as a single layer using Kim. Petition, pp. 52-53; Ex. 1003 (Sechen Declaration) ¶¶ 193-94 (proposing using “any of the memory structures in Figures 1A, 1B, 2, 7, or 25A”). However, the individual memory cells from Figure 1A, 1B, 2, or 7 are not what Lee discloses as a layer 3104 in Figure 35. Ex. 1007, [0111] (“The array 3101 has a plurality of device levels 3104”). Even if starting with Figure 25A as suggested by Dr. Sechen, Dr. Sechen does not offer any explanation of how a POSITA could have recreated Lee’s interleaved structure or patterning a lower level using the next

upper level with any expectation of success using stacking. Alignment issues inherent in stacking methodologies would, for Lee, result in a lower memory array density than Lee's deposition method. These techniques of patterning and interleaving the structures across levels are also at least easier using direct deposition, and may not even be possible to recreate with stacking.

120. Figures 13-23 of Lee explain how the levels, including levels 1 and 2, are deposited in its Figure 35 device. Ex. 1007, [0147]-[0162]. Figure 24 shows depositing in gap 1343 a control gate adjacent to the pillars on both levels 1 and 2. Ex. 1007, [0163]. As shown in Figure 25A, the control gates 1350 overlap levels 1 and 2 of its structure. Ex. 1007, [0165] (“as shown in FIG. 25A a control gate 1350 is formed between second pillar strip 1340 as well as in the gaps 1343 between pillars 1342”). Lee explains that after Figure 25A is complete, “the fabrication of the first level of memory devices is complete.” Ex. 1007, [0166].



Ex. 1007, Figures 24, 25A, annotated.

121. In a later stage in the fabrication process, level 3 is added on top of levels 1 and 2. The pillar strips at level 3 are used to complete formation of level 2's strips into pillars, and also to form an additional set of control gates that overlap levels 2 and 3 as shown in Figure 27A of Lee. Ex. 1007, [0167]. Dr. Sechen testified that Lee removed the common control gates between levels 1 and 2 (in Figure 25A) when forming the Figure 27A structure. Ex. 2039 (Sechen Deposition), 48:1-5 ("Q. Okay. So do you believe that in forming Figure 27A, the common control gate's

[sic] between levels 1 and 2 in Figure 25A were removed. A. That's my understanding."); *see also id.*, 46:5-48:5. I disagree. Dr. Sechen's understanding is of course incorrect because the control gates in Figure 25A were not removed in the process of forming Figure 27A.

122. Indeed, Lee's Figure 27A is merely showing a different view of level 1. Ex. 1007, [0167] ("FIGS. 27A and 27B [are] FIG. 26 rotated 90°"). As shown in Figure 26 below, Lee shows that each pillar contains a pair of floating gates on each of its two pairs of faces, and "[e]ach control gate 1350 [on left and right in Figure 26] will be shared with the subsequently formed pillar memory device position[ed] vertically above, in Level 2" Ex. 1007, [0166].

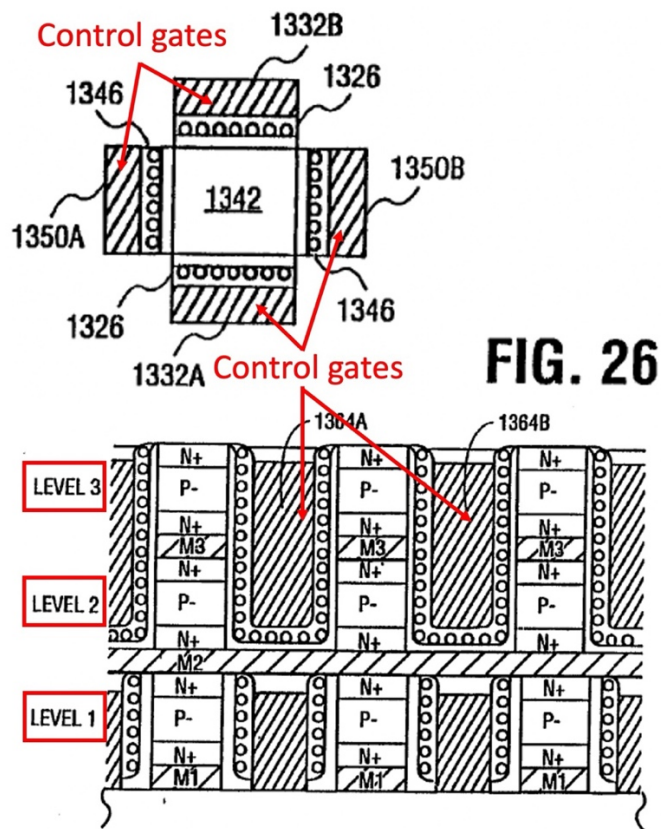


FIG. 27A

Ex. 1007, Figures 26, 27A, annotated.

123. Lee further explained that this process of interleaving control gates between levels can be repeated for subsequent levels:

The process as described with respect to FIGS. 20-25 can be repeated again to complete the fabrication of memory devices on the second level and to begin the fabrication of the memory device on the third level. That is, as shown in FIGS. 27A and 27B (FIG. 26 rotated 90°) the steps of FIGS. 20-25 can be repeated to form third pillar strips

1360 orthogonal to the second pillar strips 1340 which are used to pattern the second pillar strips 1340 into a plurality of second pillars 1362 on a second level and to form a second pair of control gates 1364 adjacent to the second pillars.

Ex. 1007, [0167]. In other words, Lee teaches using each next level to pattern the level below, interleaving control gates between the levels in the process. This last step is what turns the pillar strips on the level below into pillars.

124. A POSITA would have readily understood that because the control gates are shared between levels, there is no clean horizontal partition point between Lee's levels. Ex. 1007, Figures 25A-27A. Neither the Petition nor Dr. Sechen explain forming these interleaved levels by stacking, and a POSITA would not have thought to form Lee's interleaved structure using separate, stacked layers particularly when Lee taught forming them by deposition instead. In my opinion, a POSITA would have also been deterred from using stacking to form Lee's interleaved structure given Lee's process where the next level is used to pattern the level below.

2. No Quality Control Benefit Or Waste Reduction

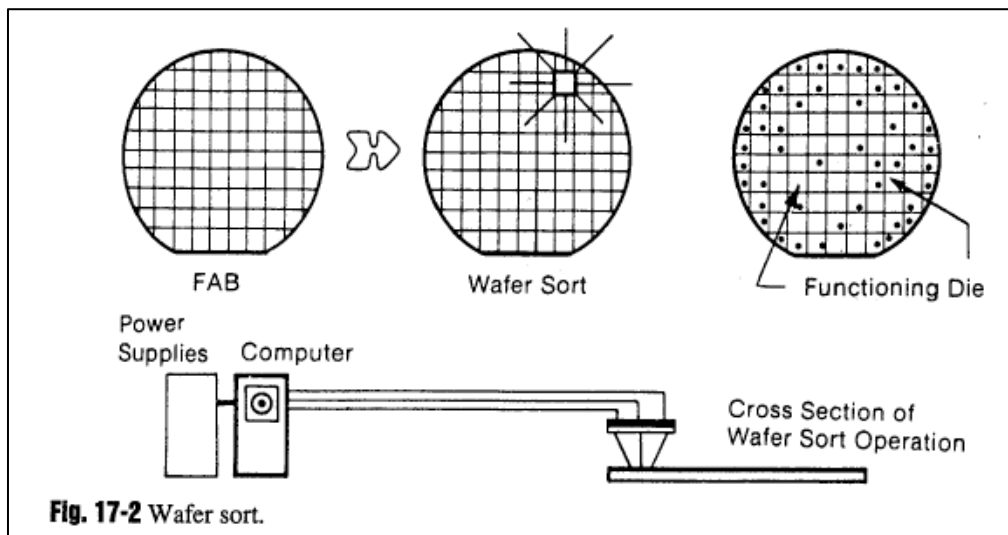
125. Another aspect of Petitioner's presumed motivation to combine Lee and Kim relates to "more efficient quality control." Petition, p. 53. The argument here is that quality control (testing for shorts, according to the Petition) can be

performed on layers prior to bonding and that only known good layers 3104 would be bonded to Lee's lower layers 3105, 3103, and 3102 (Petitioner's Wafer B). I disagree. Kim provides no detail about any quality control or testing for shorts prior to bonding. Ex. 1008 (Kim). Dr. Sechen refers to Fung (Ex. 1016) in support of this argument. But Fung, relying on a yield analysis says the opposite: that "[a]ssuming a typical 70% yield for each finished wafer, by stacking two wafers, the maximum yield achievable is 49%." Ex. 1016 (Fung), 1:33-38. Fung further states that the "low yield forcibly results in a significant increase in cost." Ex. 1016 (Fung), 1:38-39.

126. Importantly, Fung also points out that wafer-to-wafer bonding also suffers from an alignment problem that required interconnect feature size to be increased dramatically over that found in monolithic deposition processes. Ex. 1016 (Fung), 1:33-47. This is because it is difficult to accurately align whole wafers to other wafers. Ex. 1016 (Fung), 1:39-47 ("the feature size of the interconnect required for stacking needs to be very large which, in turn, degrades the density and performance of the 3D-IC"). Applying Kim's teaching to Lee would be detrimental to Lee's goal of high density.

127. I don't see any quality control benefit in combining Lee and Kim that would further improve the normal quality control that monolithic devices already undergo. Semiconductor fabs routinely test the devices they build, including for

shorts. Conventionally, once processing is complete, any failed dies are marked with a drop of ink so they can be discarded after the wafer is sawed into individual die:



Ex. 1014 (Silicon Processing, Vol. 1), 841-42 (“Following the conclusion of the wafer-fabrication process comes an important testing step referred to as *wafer sort*.... to determine which of their die are functional.”), Fig. 17-2; Ex. 1016 (Fung), 1:48-49 (“the chips in each wafer are tested to screen out defective ones”).

128. Further, optical alignment of whole wafers being stacked on top of each other is only possible if the alignment marks on both die are visible. Ex. 1016 (Fung), 1:57-60. There is no suggestion in the Petition that this would be the case in the application of Kim’s teaching to Lee.

129. Overall, Dr. Sechen’s reliance on Fung to support a quality control advantage of Kim’s method over a monolithic deposition process contemplated in Lee is misguided.

130. Finally, Petitioner’s last aspect of their presumed motivation to combine Lee and Kim is that it will reduce waste. Petition, p. 53. That also is untrue. Kim’s stacking is considerably more wasteful than Lee’s. Lee’s deposition method builds many layers on a single wafer. Ex. 1007, [0107], [0111]. Even if there were errors in one die (or more), fabs would not discard the entire wafer because that would waste an entire wafer’s worth of dies. Ex. 1014 (Silicon Processing, Vol. 1), 841 (after “wafer sort,” dies on a wafer that fail testing “are traditionally marked with a drop of ink ... and are eventually discarded”); Ex. 1016 (Fung), 1:48-49 (“the chips in each wafer are tested to screen out defective ones”). Dr. Sechen agrees with me. Ex. 2039 (Sechen Deposition), 113:12-114:12 (“discard[ing] the whole wafer” is “very unlikely to ever happen because the chips are individualized” and “you surely don’t want to throw away a whole wafer because it has a bad die”).

131. By contrast, Kim’s stacking method basically discards an entire wafer for every bonding. After the two wafers 210 and 220 are bonded, Kim teaches “the top wafer 220 can also be thinned,” Ex. 1008 (Kim), [0025], by “a Chemical Mechanical Polish (CMP), grinding, or Silicon (Si) wet etch process,” Ex. 1008 (Kim), [0027]. What that means is that almost the entirety of the top wafer is ground or etched off every time Kim stacks a layer. A POSITA looking to build a multi-layer 3D memory would not seriously entertain discarding numerous wafers to build it. Not only is it very wasteful, it’s also very expensive. Dr. Sechen’s opinion that

combining Lee and Kim would reduce waste is nonsense. Kim's technique would only increase waste.

132. So, overall, Petitioner's rationale for applying Kim's wafer bonding technique to Lee for the purposes of improved quality control and reduced waste is entirely misguided. Performing tests on a wafer-sized add-on layer in order to determine whether it should be bonded to an existing base substrate is not likely to be fruitful or productive or yield the waste reduction that Petitioner suggests. In particular, a short somewhere on the wafer would likely render inoperable one die of the many on the wafer. The add-on layer would only be discarded if the whole wafer-sized layer was seriously and pervasively flawed such that many dice would be ruined by its application to the existing stack. This observation drives the conclusion that the amount of waste reduction would be very much less than the number of shorts found would suggest. Further the wafer bonding process of Kim has costs in its own right that reduce further the reduction in waste. In addition to the reduction in density due to the increased interconnect feature size, the bonding process itself would have a yield less than 100%, as suggested by Fung. Ex. 1016 (Fung), 1:44-47, 1:34-38.

133. Because of all these issues with the proposed combination of Lee and Kim and the challenges in getting full-wafer bonding to yield effective results, a POSITA would not have had a reasonable expectation of success in using Kim's

wafer bonding within the framework of Lee’s embodiments in a way that delivered on the benefits hypothesized by Petitioner, much less any motivation to use Kim’s wafer bonding in lieu of Lee’s monolithic approach that “improv[ed] device density.” Ex. 1007, [0107].

134. In summary then, the proposed modification of Lee in view of Kim as described by Petitioner is without merit or motivation.

D. Ground 1D: Obviousness over Lee, Kim, and Endoh (Claims 16-17)

135. In Ground 1D, the Petition asserts obviousness of Claims 16-17 based on the combination of Lee, Kim, and Endoh. Petition, pp. 3, 55. I disagree.

136. In particular, in Ground 1D Petitioner combines the Petition’s analysis of Lee/Kim presented in Section VII.C (Ground 1C) with the description of Lee/Endoh found in Section VII.B (Ground 1B), relying on the motivations to combine within those sections. No separate motivation to combine for all three references has been provided.

137. Additionally, Grounds 1B and 1C each rely on a different set of proposed claim constructions for “stackable add-on layer” and “SOI pillar.” *Compare* Petition, pp. 41-42 *with* Petition, p. 50. Given the Petition’s cross-referencing to Grounds 1B and 1C, it is unclear to me which of these constructions it purports to rely on for Ground 1D.

138. To the extent I understand Ground 1D, as presented above, both these two-reference combinations in Grounds 1B and 1C fail to be properly motivated and, in both cases, a POSITA would not have had a reasonable expectation of success individually or together as a three-reference combination. Therefore, Claims 16 and 17 have not been shown to be obvious under the hypothetical combination of Lee, Kim and Endoh.

E. Ground 1E: Obviousness over Lee and Aspar (Claims 13-17)

139. In Ground 1E, the Petition asserts obviousness of Claims 13-17 based on the combination of Lee and Aspar. Petition, pp. 3, 55. I disagree.

140. Ground 1E is similar to Ground 1C except that instead of the wafer bonding method of Kim, Petitioner looks to Aspar for an alternate wafer-bonding technique to combine with Lee. This Ground fails for similar reasons as explained above for Ground 1C.

141. Petitioner looks to the Petition’s Section VI.A for its analysis for Claim 13 (except for element 13(c), “stackable add-on layer being bonded to the dielectric layer”). Petition, p. 56. For element 13(c), Petitioner looks to the combination of Lee and Aspar.

142. Petitioner starts the discussion of the motivation to combine Lee with Aspar with an inaccurate statement. They begin by saying “Lee does not clearly describe how the bottom level 3104 of array 3101 is formed on insulating layer

3102.” Petition, p. 56. This is not so. As explained above in my discussion for Ground 1C, a POSITA reading Lee would have understood that in Lee’s Figure 35, the bottom-most “device level 3104” would be deposited on “insulating layer 3102.” Lee’s Figure 35 shows a schematic of a three dimensional array of devices 3101 having “a plurality of device levels 3104, preferably separated by interlayer insulating layers.” Ex. 1007, [0111]. Lee explained that “layers of each level of the array were directly deposited on the layers of each underlying level of the array.” Ex. 1007, [0107]; *see also* Ex. 1007, [0122]. In addition, Dr. Sechen agreed that Lee’s Figures 13-28, which illustrated methods for forming a multilevel array of memory devices, describe various “fabrication steps” for forming the structure in Lee’s Figure 35. Ex. 2039 (Sechen Deposition), 88:2-89:6; Ex. 1007, [0052], [0147]-[0170].

143. Per Petitioner’s definition of a POSITA and my own, these process steps would have been within a POSITA’s knowledge and experience. Petition, p. 9 (“at least three years of experience in the research, design, or development of semiconductor memory device structures”). As a result, Petitioner’s next statement (“Consequently, a POSITA would have looked to and been motivated to apply other art, such as known wafer bonding techniques, for details about attaching bottom level 3104 to insulating layer 3102”) is not supported. Petition, p. 56.

144. As with the Lee/Kim combination in Ground 1C, in Ground 1E Petitioner and Dr. Sechen again provide no reason to stack Lee’s levels, which a POSITA would have understood to be interleaved and formed via deposition. *See* Section XI.C. As explained in Section XI.C above, a POSITA would have readily understood that because the control gates are shared between levels, there is no clean horizontal partition point between Lee’s levels. Ex. 1007, Figures 25A-27A. A POSITA would not have thought to recreate Lee’s deposited interleaved structure using separate, stacked layers, and would have been discouraged from using stacking to form Lee’s deposited interleaved structure given Lee’s process where the next level is used to pattern the level below. Such a structure is most efficiently formed via deposition as described by Lee’s Figures 12-28. This structure could not be effectively manufactured with a stacking process with the same cost or density as it could be with a deposition-based process.

145. In addition, like with Ground 1C based on Lee and Kim, Petitioner asserts that the combination of Lee and Aspar would have better “quality control” and “minimize[] waste.” Petition, pp. 61-62. I disagree. Petitioner’s proposal is using Smart-Cut to put the substrate in Wafer B and the stack from Lee’s Figure 9A into Wafer A. Petition, p. 59; Ex. 1003 (Sechen Declaration) ¶ 209. Dr. Sechen conceded that at that point Lee’s Figure 9A in Wafer A is an unpatterned wafer containing no memory devices. Ex. 2039 (Sechen Deposition), 90:5-20. A POSITA would have

known that Aspar would not improve quality control in Lee because the memory devices are deposited after the layer is transferred using Smart-Cut. Both Petitioner and Dr. Sechen agree. Ex. 2039 (Sechen Deposition), 90:21-91:15 (“Q. So when this layer in Figure 9A is transferred and attached to the substrate in Figure 35, there are no memory devices in that layer; correct? ... [A.] What you -- yeah, what you get is three pure single crystalline layers, doped layers, N+ P- N+ and -- into which you will form the devices for memory cells.”); Petition, p. 60 (“After bonding, the individual memory cells in [Lee’s] level 3104 would be fabricated...”). Petitioner and Dr. Sechen’s suggestion that Smart-Cut permits performing quality control “on the stack prior to bonding” is nonsensical. Petition, p. 61; Ex. 1003 (Sechen Declaration) ¶ 213. Indeed, the memory cell errors a POSITA would want to test for would necessarily arise after Smart-Cut’s bonding and cleaving. And Aspar itself only shows transferring unpatterned wafers. *E.g.*, Ex. 1009 (Aspar), Figure 12. Rather than improve quality control and reduce waste, a POSITA would have recognized that using Aspar’s Smart-Cut with Lee had the potential to increase waste given its high-temperature annealing process that risked exceeding the thermal budget of Lee’s device, as explained further below. As explained above for Ground 1C, Petitioner’s reliance on Fung (Ex. 1016) is also unhelpful because Fung explained that wafer stacking led to low yields and pointed out that it also suffers

from an alignment problem that required interconnect feature size to be increased dramatically over that found in monolithic deposition processes.

146. Despite the lack of any motivation to combine Lee with Aspar, Petitioner nevertheless looks to Aspar’s Smart-Cut® process to try to fill in the deficiencies in Lee. Petition, pp. 56-57; *see also* Section IX.C. As described above in Section IX.C, Aspar’s Smart-Cut method was “first developed to obtain silicon-on-insulator (SOI) materials” comprising a highly uniform monocrystalline silicon layer on top of an oxide layer on top of a carrier substrate. Ex. 1009 (Aspar), pp. 1, 4 (“The major application of this process is at present fabrication [of] SOI wafers”). The process by which these blank SOI wafers are created is illustrated in Aspar’s Figure 1:

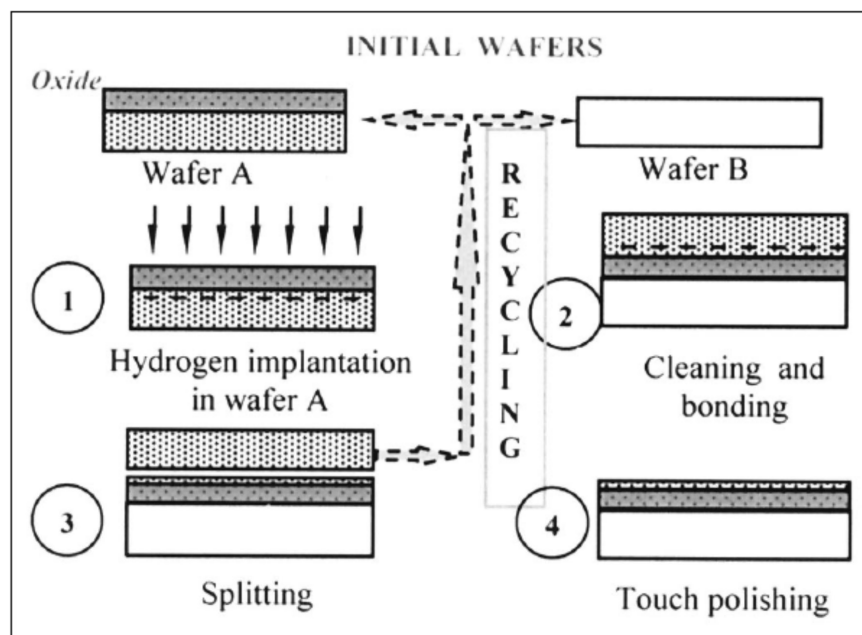


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

Ex. 1009 (Aspar), p. 834, Figure 1.

147. A layer of monocrystalline silicon is the thin top layer of the end product left after step 4 of Aspar's Figure 1. It originated in Wafer A just below the oxide layer and just above the "in-depth weakened layer" caused by the hydrogen implantation. Ex. 1009 (Aspar), p. 834.

1. Exceeding Thermal Budgets

148. After the hydrogen implantation phase of Aspar's Smart-Cut process, an annealing step is required to complete the weakening of Wafer A. Ex. 1009 (Aspar), pp. 835 ("thermal treatment induces the growth of microcavities"), 836. Other of Petitioner's exhibits describing the Smart-Cut process describe annealing steps to remove defects or to increase the bonding strength to the support substrate. Ex. 1015 (Silicon Processing, Vol. 4), pp. 543-44 & Fig. 11-24 ("Both wafers are then annealed at 1100°C to remove defects"); Ex. 1014 (Silicon Processing, Vol. 1), pp. 260-61 & Fig. 7-29 (same); Ex. 1023 (Srikrishnan), 2:36-41 ("Then, the support substrate 220 with the thin silicon layer 207 (device layer) still bonded to it is annealed at a high temperature (approximately 1000° C.) to promote a stronger bonding between the support substrate 220 and the device layer 207"). In his deposition, Dr. Sechen acknowledged that the annealing step was part of the Smart-Cut process. Ex. 2039 (Sechen Deposition), 121:8-11 ("Q. So figure 11[-]24, which you put in your declaration shows that annealing step at 1100 degrees Celsius;

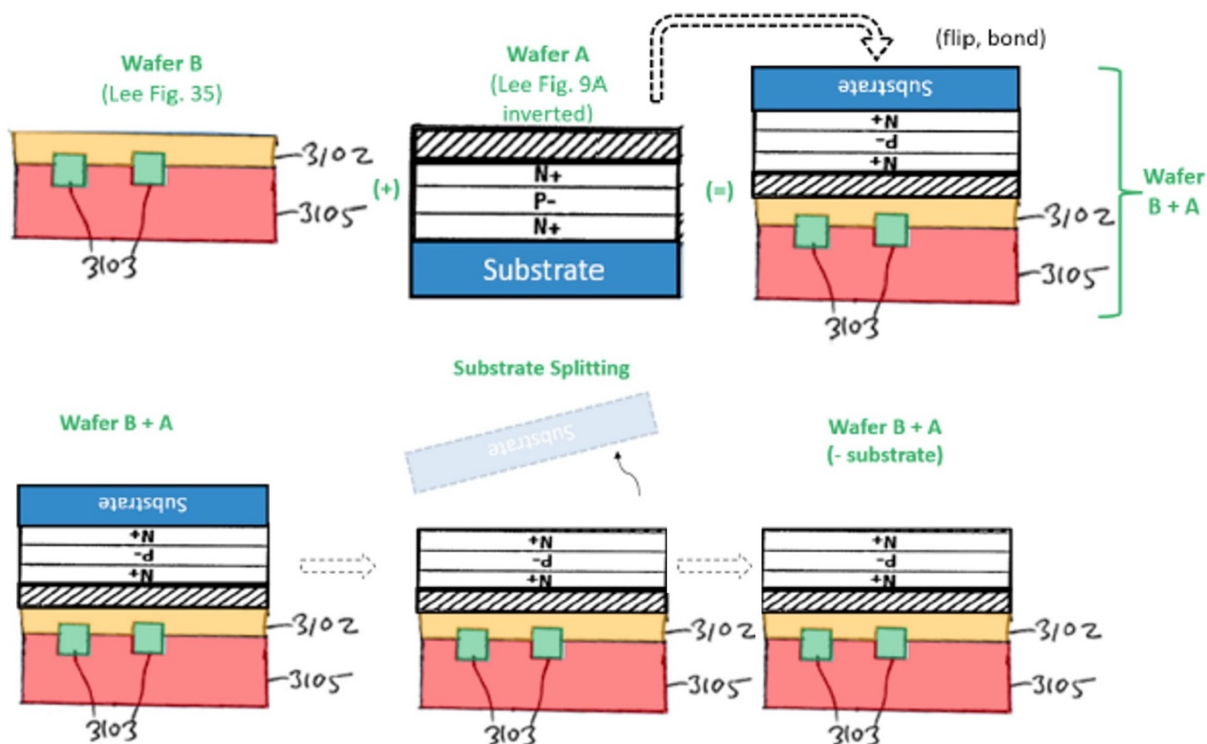
correct? A. Yes.”); Ex. 1003 (Sechen Declaration) ¶ 46 (citing Exhibits 1014 and 1015); *see also* EX2039 (Sechen Deposition) at 117:17-121:11.

149. In contrast, the specification of the ’702 Patent expressly provides for low-temperature processing to avoid the whole issue of reduced thermal budgets at lower process geometries. Ex. 1001 (’702 Patent), 7:15-35.

150. A POSITA would have understood that the manufacturing of integrated circuits with electrical devices (for example, transistors) formed with dopant ions implanted into a silicon substrate is subject to a total thermal budget—the total amount of time spent at high temperatures during and after the formation of those transistors. Ex. 2027 (Batude), pp. 715-716. A thermal budget exists because the dopant ions that form the source and drain move every time the device is raised to an elevated temperature. Ex. 2027 (Batude), p. 715 (“[T]o avoid additional dopant diffusion or interfacial oxide growth on bottom transistor, LT [Low Temperature] (<650° C) top FETs process is mandatory”; “Top MOSFETs are processed with an overall thermal budget of 650° C.”). The formation of the source and drain regions are among the very first steps in the fabrication of an integrated circuit because these regions are in the silicon substrate below all the metallization and interconnect. Once the source and drain have been formed, if the temperature is elevated then those dopants will diffuse further into the substrate than desired, altering the characteristics of the electrical device. The higher the temperature or the longer the substrate is held

at an elevated temperature the more the dopants will diffuse and the greater the degradation of the device characteristics **to the point that they can deviate from the design parameters**. Ex. 2027 (Batude), pp. 715-716; *see also* Ex. 2039 (Sechen Deposition), 101:15-102:6, 99:12-100:5, 102:12-103:3.

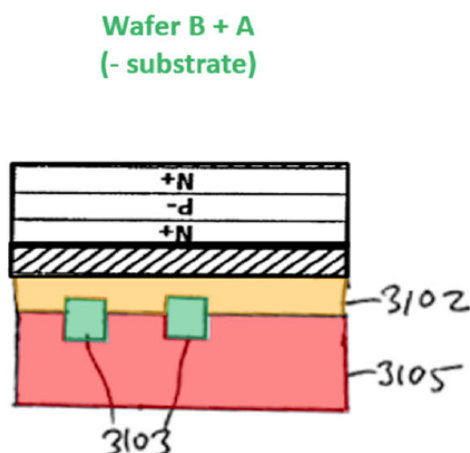
151. By 2004, the general understanding of a POSITA at the time was that once electrical devices, such as transistors, are formed, no subsequent processing step should be conducted at temperatures above 650° C and certainly not at 1100° C as required by Aspar's Smart-Cut process. Ex. 2027 (Batude), p. 715 (“[T]o avoid additional dopant diffusion or interfacial oxide growth on bottom transistor, LT (<650°C) top FETs process is mandatory.”); Ex. 2039 (Sechen Deposition), 102:12-103:3 (Dr. Sechen acknowledging that a POSITA “in 2004, would have been aware of the thermal budget issue”); Ex. 2028 (Lee Deposition in Micron), 123:13-124:7, 125:6-126:7. And yet Petitioner and Dr. Sechen propose using Aspar's Smart-Cut with Lee which risked exceeding the thermal budget of Lee's electrical devices. Specifically, Intel and Dr. Sechen propose sectioning into two wafers Lee's substrate (Wafer B) from its memory cells (Wafer A), then bonding and splitting off Wafer A's substrate (blue) using Aspar's Smart-Cut as shown below:



Petition, pp. 59-60 (citing Ex. 1003 (Sechen Declaration) ¶¶ 209-11).

152. The proposal to use Aspar’s Smart-Cut with Lee shows that the resulting combined Wafer B+A (- substrate) created using Smart-Cut includes Lee’s control circuitry (driver circuits 3103 shown below annotated in green by Petitioner). Petition, pp. 59-60; Ex. 1003 (Sechen Declaration) ¶¶ 209-10. A POSITA would have recognized that Aspar’s Smart-Cut risked exceeding the thermal budget of Lee’s device in its post-split 1100°C annealing step. Because Smart-Cut taught the annealing step was required for transferring each layer 3104, transferring multiple layers to create a 3D array of memory cells 3101 would only aggravate the thermal budget issues, subjecting Lee’s device to repeated annealing steps every time a layer

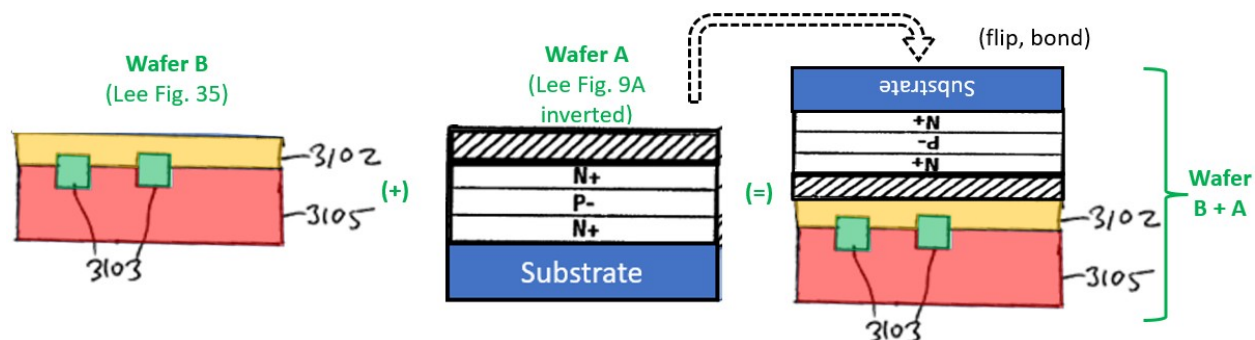
is transferred. Ex. 1009 (Aspar), p. 834, Figure 1; Ex. 1015 (Silicon Processing, Vol. 4), pp. 543-44 & Fig. 11-24 ; Ex. 1014 (Silicon Processing, Vol. 1), pp. 260-61 & Fig. 7-29 (same); Ex. 1023 (Srikrishnan), 2:36-41. It also risked causing diffusion of the doped stack of layers that Petitioner proposes adding as the stacked layer via Aspar's Smart-Cut process, depicted as Lee's Figure 9(a). Ex. 1007 (Lee), Figure 9(a). Those layers as shown above in the Petition's annotated figures are doped to form an NPN stack. Petition, pp. 59-60. Annealing at 1100°C further risked degrading the characteristics of this NPN stack to something that was at least outside specification if not non-functional. The presence of a high-temperature annealing step as part of Aspar's Smart-Cut process teaches away from using Aspar's Smart-Cut with Lee's memory cell layers, and at a minimum eviscerates any motivation to combine Lee with Aspar.



Petition, p.60; *see also* Ex. 1007 (Lee), [0111] (“The driver circuits 3103, such as sense amps and charge pumps, are disposed in the monocrystalline substrate 3105, as CMOS or other transistors.”).

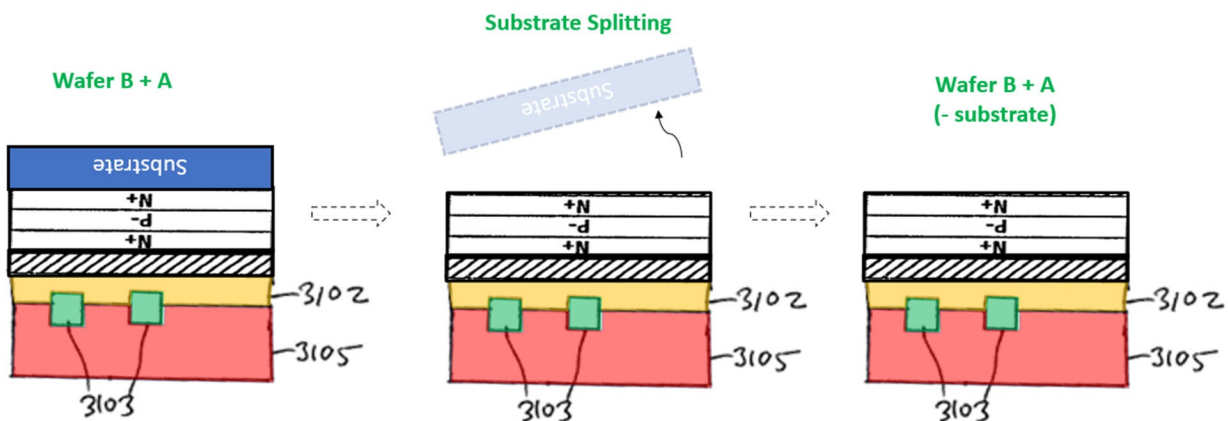
2. No Reasonable Expectation of Success

153. Petitioner augments the disclosure of Aspar substantially to create the structures found in Lee. As shown on page 59 of the Petition, Petitioner labels substrate 3105 with its completed peripheral circuitry 3103 and its dielectric layer 3102 together as Wafer B. Petitioner’s Wafer A is “a single crystal surface layer with a doped stack similar to stack 902 in Lee’s Figure 9A” from which the memory cell structure of Figures 1A-1B, 2, 7, and 25 would be formed. Petition, p. 59



Petition, p. 59.

154. The blue substrate (shaded blue) is then cleaved off, leaving the top N+ doped region exposed.



Petition, p. 60

155. This fabricated process is substantially more complex than disclosed in Aspar and the other references in the record describing the Smart-Cut process. Aspar's Figure 1 shows only an unpatterned oxide layer on Wafer A and a clean Wafer B prior to bonding and cleaving. Also, in Aspar, the hydrogen implantation and cleaving process leaves a thin portion of the substrate of Wafer B behind (see below), which becomes the monocrystalline silicon layer of the SOI wafer.

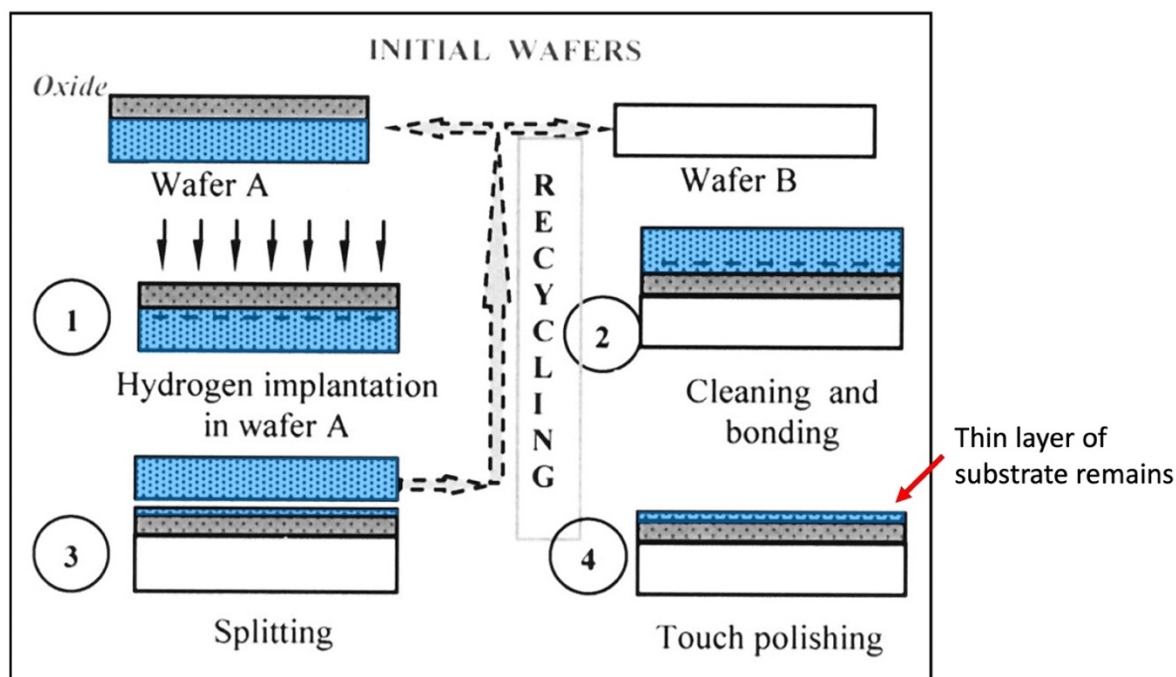


Fig. 1. Schematic description of the Smart-Cut® process, used to obtain SOI wafers.

Ex. 1009 (Aspar), Figure 1, annotated; Ex. 2039 (Sechen Deposition), 68:19-73:21 (Dr. Sechen acknowledging “you get a thin silicon layer on top of the oxide” after splitting and polishing).

156. Petitioner provides no explanation how to avoid the thin layer of monocrystalline silicon remaining after Aspar’s process that would obstruct Lee’s upper metal contact (M2 in Figure 25A of Lee, shown below).

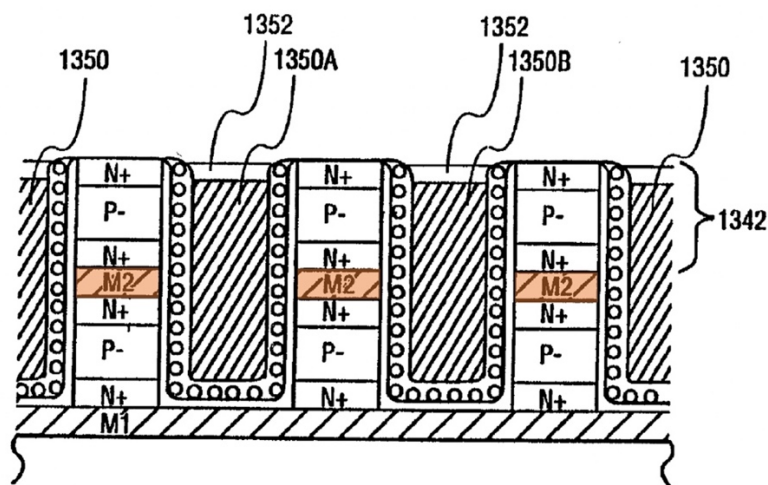


FIG. 25A

Ex. 1007 (Lee), Figure 25A, annotated.

157. In addition, the various annealing stages described above would have significant detrimental effects on pre-existing peripheral circuits shown in Wafer B and in the end result. Ex. 2039 (Sechen Deposition), 95:12-103:3.

158. The result is that the process concocted by Petitioner here with respect to the combination of Lee and Aspar is a fiction. It is, as presented, not supported by the references, and goes well beyond the capabilities of the Smart-Cut process as described in the record. This further emphasizes the non-obviousness of the claimed invention. The application of Aspar's process including its hydrogen implantation and annealing steps would likely exceed the thermal budget of the peripheral circuitry 3103, at a minimum degrading their performance.

159. The reasons that Petitioner provides for why a POSITA would be motivated to use Aspar's Smart-Cut process to wafer bond bottom level 3104 to insulating layer 3102 are all flawed.

160. Petitioner begins with the disclosure of Aspar that Smart-Cut realizes multiple SOI layers as illustrated in Aspar's Figure 14:

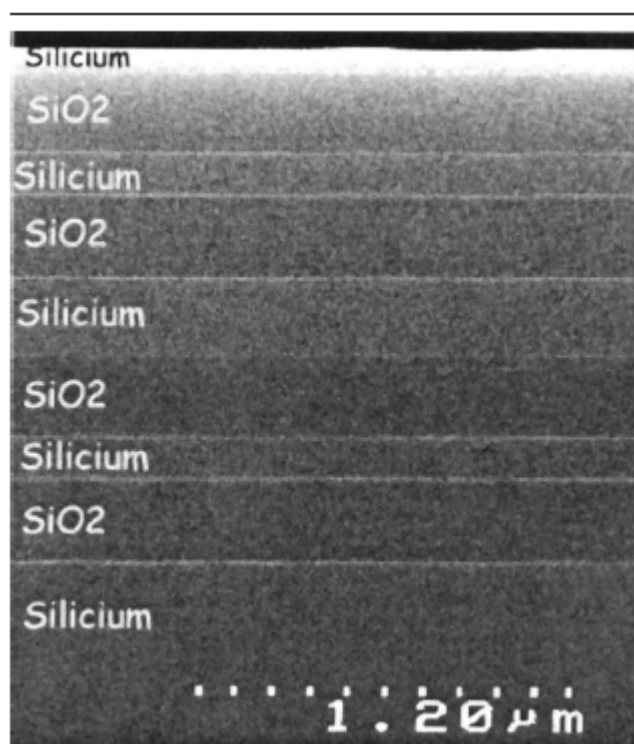


Fig 14. SEM view of multiple SOI layer stack.

Ex. 1009 (Aspar), Figure 14.

161. What Aspar discloses is very different from what Petitioner suggests. Aspar discloses multiple thin SOI layers separated by silicon dioxide layers. The complex structure of the presumed combination is not evident in Aspar or the other references in the record. A POSITA reading these references would not have any

expectation of success in augmenting Smart-Cut to such a substantial degree as suggested by Petitioner. Aspar was a proof-of-concept academic article that described transferring thin films. Ex. 1009 (Aspar), 839. Aspar did not disclose transferring layers with any devices. Ex. 1009 (Aspar), Figures 12, 14, 16. A POSITA would have recognized that a considerable amount of research and development would need to be done for Smart-Cut to be used to create working 3D memory.

162. Overall, Petitioner grossly overstates the motivation to combine, ignores negative effects, and ignores the lack of reasonable expectation of success.

F. Ground 1F: Obviousness over Lee, Aspar, and Endoh (Claims 16-17)

163. In Ground 1F, the Petition asserts obviousness of Claims 16-17 based on the combination of Lee, Aspar, and Endoh. Petition, pp. 3, 64. I disagree.

164. In particular, in Ground 1F Petitioner combines the analysis of Lee/Aspar presented in the Petition’s Section VII.E (Ground 1E) with the description of Lee-Endoh found in Section VII.B (Ground 1B), relying on the motivations to combine within those sections. No separate motivation to combine for all three references has been provided.

165. Additionally, Grounds 1B and 1E each rely on a different set of proposed claim constructions for “stackable add-on layer” and “SOI pillar.”

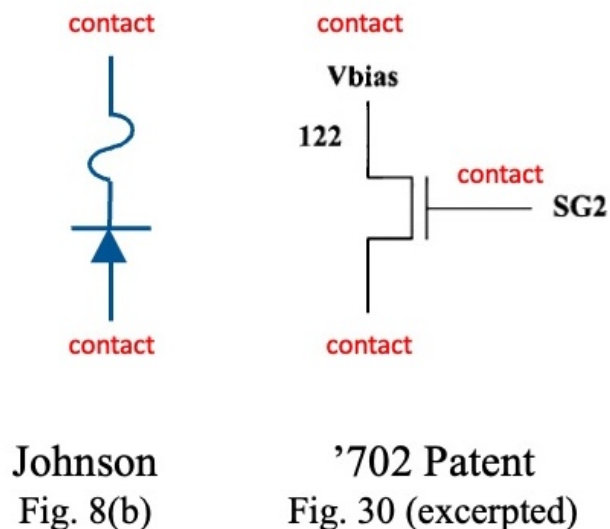
Compare Petition, pp. 41-42 *with* Petition, p. 64. Given the Petition’s cross-referencing to Grounds 1B and 1E, it is unclear to me which of these constructions it purports to rely on for Ground 1F.

166. To the extent I understand Ground 1F, as presented above, both these two-reference combinations in Grounds 1B and 1E fail to be properly motivated and, in both cases, a POSITA would not have had a reasonable expectation of success individually or together as a three-reference combination. Therefore, Claims 16 and 17 have not been shown to be obvious under the hypothetical combination of Lee, Aspar and Endoh.

G. Ground 2A: Obviousness over Johnson (Claim 13)

167. In Ground 2A, the Petition asserts obviousness of Claim 13 based on Johnson. Petition, pp. 3, 65. I disagree.

168. Johnson taught a field-programmable memory design using 2-terminal devices comprising a diode and an antifuse. Ex. 1010 (Johnson), 5:41-65, 7:33-8:5. As shown, for example, in the illustration below, Johnson’s 2-terminal device was distinctly different from the transistor memory cell disclosed in the ’702 Patent. Johnson was directed to a simplified solution, creating NOR memory cells using a diode and an antifuse (which Johnson incorrectly represents with the fuse symbol—an “S” shaped symbol).



Ex. 1010 (Johnson), Figure 8(b), excerpted and annotated; Ex. 1001 ('702 Patent), Figure 30, excerpted and annotated.

169. For claim 13[d], the Petition says that Johnson discloses or suggests element 13[d] which requires “nonvolatile memory cells having at least one transistor.” Petition, p. 73; Ex. 1001 ('702 Patent), 12:33-34. The Petition relies exclusively on Johnson’s disclosure at 7:61-8:5, where it lists “possible implementations of the steering element,” including a JFET and a MOSFET. Petition, p. 73. That is the only mention in Johnson of a transistor in its pillar. The “possible implementations” of the steering element Johnson listed in Johnson (reproduced below), including the JFET and MOSFET, are used in Johnson as 2-terminal devices, not 3-terminal devices.

- (i) a PN junction diode, in amorphous, microcrystalline, polycrystalline or single crystal semiconductor (e.g. Si, Ge, SiGe, GaAs, InP, etc.);
- (ii) a metal-semiconductor Schottky diode;
- (iii) a junction field-effect transistor with gate connected to source (or to drain);
- (iv) a MOSFET with gate either floating, or connected to source or connected to drain;
- (v) a Zener diode, avalanche diode, or tunnel diode;
- (vi) a four-layer diode (SCR);
- (vii) a P-I-N diode in amorphous, microcrystalline, polycrystalline or single crystal semiconductor

Ex. 1010 (Johnson), 7:58-8:5.

170. The Petition goes on to say that “In Johnson, each nonvolatile memory cell has at least one transistor because Johnson describes that steering element 22 (Figure 4(a)) can be implemented using ‘a junction field-effect transistor with gate connected to source (or to drain)’ or ‘a MOSFET with gate either floating, or connected to source or connected to drain.’” Petition, pp. 72-73 (citing to Ex 1010, 7:61-8:5). The Petition also states that “a POSITA would have understood steering element 22 of Johnson’s nonvolatile pillar memory cell to include at least one

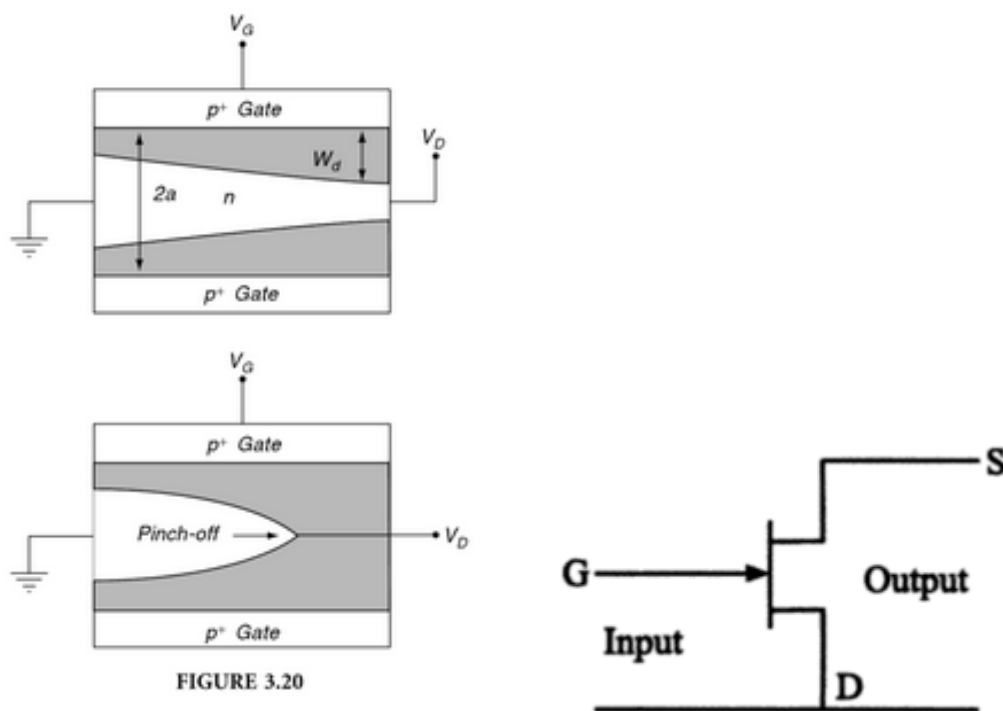
transistor because Johnson expressly discloses such implementations.”
Petition, p. 73.

171. To the extent that Petitioner is relying on Johnson’s express disclosure of transistor embodiments, I disagree that the JFET and MOSFET embodiments of column 7 would be compatible with Johnson’s embodiments relying on 2-terminal “steering elements.” A POSITA would understand that Johnson taught the use of 2-terminal “steering element” pervasively in its memory array. In no instance does Johnson teach or suggest the use of a 3-terminal “steering element.” I also believe that Johnson’s column 7 did not enable a POSITA to construct a 3-terminal “steering element” embodiments without undue experimentation and/or dramatically changing the nature of Johnson’s memory array. To the extent that Petitioner is arguing that Johnson “suggests” transistor embodiments, I disagree that a POSITA would have considered it obvious to use a transistor-based steering element in the memory array embodiments of Johnson. Johnson taught that conventional transistor designs were disfavored for use in its self-aligned and vertically oriented design, and instead used diodes and circuits with the same or better functionality. Ex. 1010, 2:29-37. The principal embodiments of Johnson’s pillar non-volatile memory cells (for example, those of Figures 4, 5, 6, 8) do not show a transistor in the pillar stack.

172. Further, the method of fabrication disclosed by Johnson for its memory array is based on Johnson’s diode design, and a POSITA would have recognized

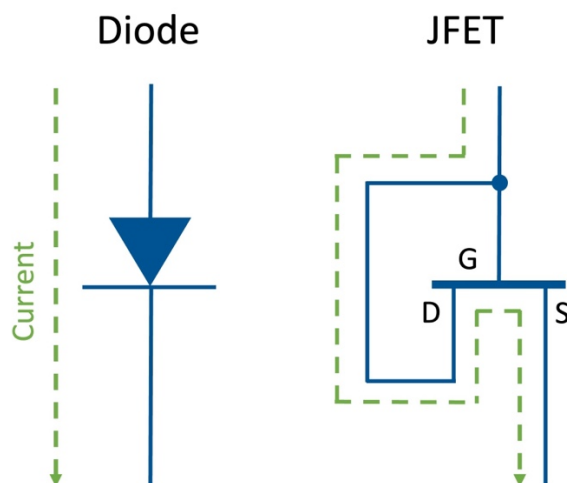
they are incompatible with either a vertically-oriented JFET or a vertically-oriented MOSFET, for reasons expanded upon below. The consequence of the lack of disclosure on anything other than 2-terminal diode-based steering elements means that a POSITA would have not had any expectation of success of combining the limited disclosure of Ex. 1010 (Johnson), 7:65-8:1, regarding the possible use of the transistors in the steering element, with the teaching regarding the fabrication of the pillars as disclosed, for example, in Johnson's Figure 6 and at Ex. 1010 (Johnson), 11:41:14:27.

173. One of the two varieties of transistors disclosed in column 7 of Johnson and cited by the Petition is a vertically-oriented junction field effect transistor (JFET) with its gate connected to source (or to drain), making it a 2-terminal device. Johnson disclosed no implementation of a JFET with a gate not connected to the source or drain. Ex. 1010 (Johnson) at 7:58-8:5. A JFET is a type of transistor that has been rarely used in digital electronics. A JFET is typically formed by a doped region of a semiconductor (a channel region) with gate connections connecting directly to the channel regions. As the voltage on the gate increases, the channel region is pinched. To cut off all current flowing in the channel, the channel has to be pinched off, typically by providing gate contacts on both sides or on all sides of the channel.

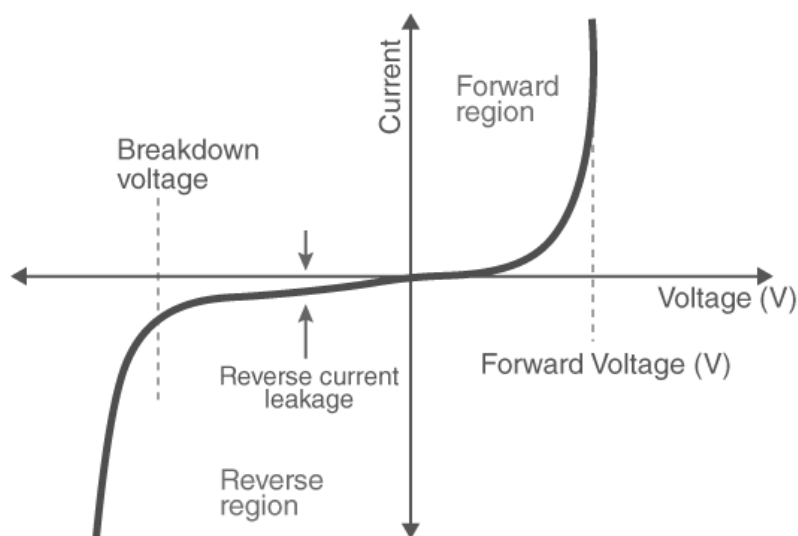


Ex. 2046 (Electrical Engineering Handbook), p. 122, Figure 3.20.

174. As Johnson recommends, a JFET can be connected to behave as a diode by connecting its gate to its source or drain. This 2-terminal configuration is shown below (and compared to a conventional diode) and called a “current regulator diode.”



175. This is called a “current regulator diode” configuration because it has different I-V characteristics than that of a regular PN junction diode or a Schottky diode. The I-V curve of a PN junction diode is characterized by a low resistance when forward-biased and very high resistance when reverse-biased. Johnson’s non-volatile memory relies on both these diode characteristics to allow access of a memory cell without interference from other cells on the same word-lines and bit-lines.



176. In contrast, a JFET connected as a diode does not have an effective reverse biased high-impedance regime, and when forward biased passes a near constant current across its normal operating range of voltages:

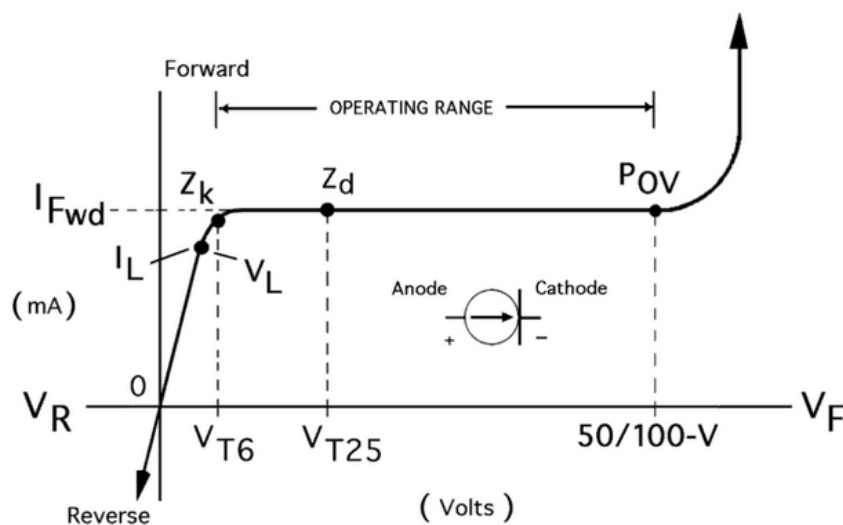


Figure 6.23. The current regulator diode's V-I characteristic curve.

Ex. 2045 (Current Sources & Voltage References), p. 170, Figure 6.23.

177. Both of these differences make the diode-connected JFET a very poor fit for use as a steering element in Johnson’s memory cells. It wouldn’t work very well in Johnson because the access times would be increased because of the nature of the V-I characteristics curve. A POSITA would not have a reasonable expectation of success in attempting to use such a device in combination with the substantive embodiments of Johnson.

178. The other transistor suggested by Johnson (Ex. 1010) at 7:67-8:1 is a “MOSFET with gate either floating, or connected to source or connected to drain.” The first of these options is a regular MOSFET with no connection to the gate. This is different from a floating gate MOSFET used in traditional non-volatile memory cells that have a second control gate. This suggestion of a 2-terminal MOSFET with a “floating” gate would not work to steer current. With a floating gate, the MOSFET in Johnson would function as either a wire or open circuit in both directions, depending on whether it is a depletion or enhancement mode MOSFET. Johnson does not explain how a MOSFET with a floating gate could act as its steering element, and a POSITA would find it inoperable.

179. The issue with a simple MOSFET or any variety with a floating gate is that it is a symmetrical device. With rare exceptions, regardless of whether it as N-channel, P-channel, enhancement mode, depletion mode or intrinsic, a MOSFET’s IV characteristics are symmetrical, and so it does not exhibit different

current flow characteristics when reverse biased. Indeed, unlike an asymmetrical diode, a MOSFET is a symmetrical device that passes current in either direction when it is turned on. This makes it incompatible with Johnson's memory cells unless it is configured appropriately. In particular, as suggested by Johnson, if a MOSFET has its gate connected to its drain, then it could function as a weak diode, blocking current in one direction between source and drain and allowing it to pass in the other. It is important though when connected this way that the current through the memory cells is proportional to the square of the voltage across the source and drain. In contrast, the current through a forward-biased PN junction diode is exponential in proportion to the voltage across the forward-biased junction. This is important because Johnson specifically emphasized the enhanced current flow through the steering element as the first thing mentioned in the Summary of the Invention. Ex. 1010 (Johnson), 4:11-13. This discrepancy between the effectiveness of a PN junction diode and that of a diode-connected MOSFET would dissuade a POSITA from choosing a MOSFET-based steering element over a simpler PN junction diode steering element, as explained below.

180. In contrast to its vertically oriented PN junction or Schottky diode designs, Johnson criticized existing field-programmable memories that used planar transistors. Ex. 1010 (Johnson), 2:6-20. Johnson explained that transistor-based designs came with the complexity of "more than one circuit element" and therefore

“consume extra silicon area.” Ex. 1010 (Johnson), 2:12-18, 2:28-32. Johnson also explained that “these devices have generally suffered from lower density and higher cost” than mask ROMs. Ex. 1010 (Johnson), 1:54-56, 2:25-27. Johnson’s goal is to devise a memory structure with field programmability and the cost and density of mask ROMs. Ex. 1010 (Johnson), 1:57-61. According to Johnson, planar transistor-based memory cells “allow[ed] only very limited integration vertically into the third dimension.” Ex. 1010 (Johnson), 2:28-36. Also, conventional non-volatile memory cells, and memory cells generally, require “a number of sequential photolithographic steps” to form the memory cells, Ex. 1010 (Johnson), 2:38-40. A POSITA would have understood that each photolithographic step bears a cost of performing the step and a cost of incremental degradation of the overall yield of the integrated circuit, a degradation that resulted in part due to alignment problems. Ex. 1010 (Johnson), 2:45-61 (“These misalignment tolerances force memory cell designers to use larger feature sizes than otherwise would be necessary...”), 3:6-8.

181. In this regard, both the JFET and the MOSFET implementations of a steering element in Johnson faced another, more substantial issue that would shatter a POSITA’s expectation of success in combining them with the memory arrays of, for example, Johnson’s Figure 6. The issue is that neither can be manufactured without significantly impacting Johnson’s goal of achieving a higher memory density of the memory array. Specifically, Johnson teaches a method of constructing

the memory cells comprising a steering element 22 and a state change element 23 in vertical pillars in which each of the two comprises a plurality of layers, as illustrated in Figure 6(a). However, if the steering element were made from either a JFET or a MOSFET, then either the transistors would be planar (as roundly criticized by Johnson, Ex. 1010, 2:28-3:12), or they could be built vertically, in the same vein as Johnson's PN junction diode and Schottky Barrier diode embodiments. Regardless of which a POSITA would undertake, there is substantial additional cost and complexity to the construction of these transistor-based field programmable memory cells. Johnson, as described above, indicates that the use of planar transistors would not meet his goals of density and cost relative to mask ROM design. Not only does Johnson not explain how to make this work, Johnson expressly says it will not work. With regard to the possibility of creating vertically-oriented transistors as part of the steering element, nothing in Johnson teaches how to overcome this complexity of fabrication and the inevitable impact to memory density. A POSITA is left alone unguided by Johnson with the daunting task of trying to figure out how to accomplish this. Specifically, in order to construct a vertically-oriented steering element out of a JFET or MOSFET transistor, additional structures need to be formed on at least one and possibly more sides of each pillar to construct the features of the transistors in question. This annotated version of Figure 4(a) shows a red

shaded region to show where on each pillar these features would have to be constructed.

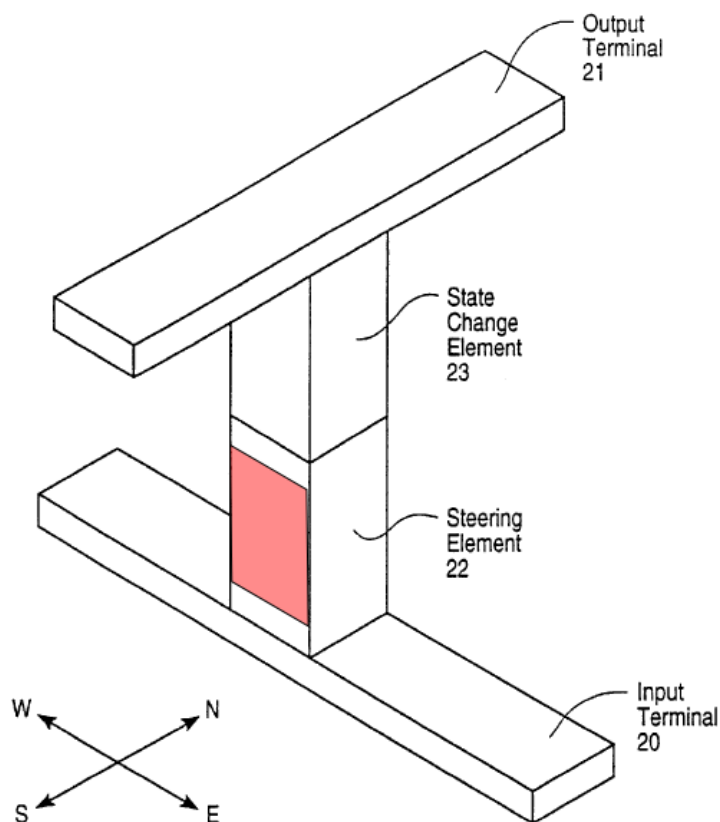
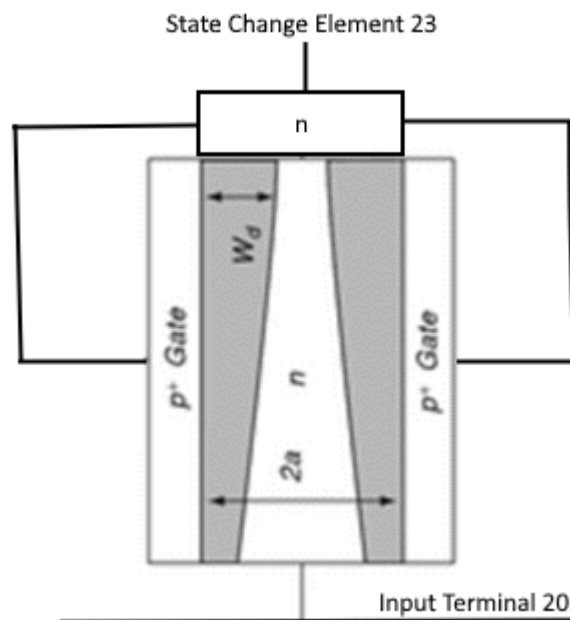


FIG. 4(a)

Ex. 1010 (Johnson), Figure 4(a), annotated.

182. In the case of a hypothetical vertically-oriented JFET-based steering element, the vertical faces of the steering element would have to have a gate material placed on at least two sides and then vertical conductors added to form the connection between these JFET gate terminals and the cathode terminal of the steering element, as shown below.



Ex. 2046 (Electrical Engineering Handbook), p. 122, Figure 3.20, augmented to show necessary addition of vertical features.

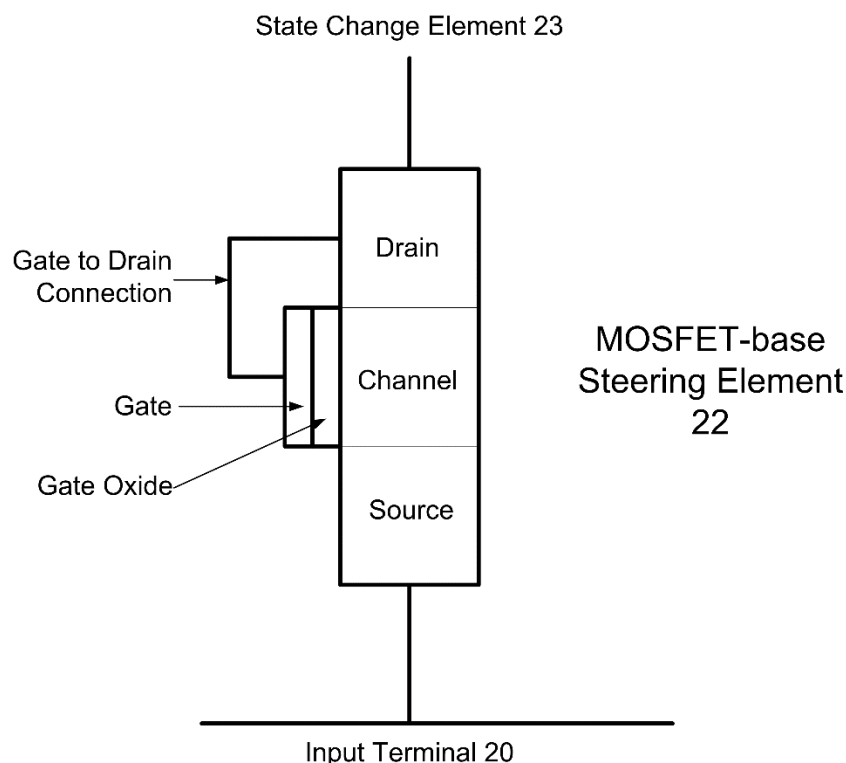
183. Unlike the steering elements of Figure 6(a), this hypothetical steering element has vertically oriented features within the pillar, not just on the exterior surface of the pillar. These would require dramatically different processing steps than any disclosed in Johnson. Further, even if a POSITA could figure out how to accomplish these vertical features without significantly impacting the yield of the memory array overall, these features would make the pillars thicker than those of Johnson's Figures 4, 6, 7, and 8, for example. Thus, changing the steering element from a simple PN junction diode or a Schottky diode to a JFET would decrease the memory cell density of the memory array, something that directly contradicts the

primary objective of Johnson. Ex. 1010 (Johnson), Abstract, 1:57-61, 2:16-20, 3:6-12.

184. The goal of providing high density field programmable memory is much more challenging using a JFET transistor instead of PN junction or Schottky diode because Johnson's fabrication method relies heavily on self-alignment to create steering elements and state change elements that have the same cross-sectional area and that perfectly and naturally aligned with each other and with the input and output terminals. The self-alignment aspect makes use of each level in the stack as a mask for the etching of the previous element, in a lower level of the 3D structure. Ex. 1010 (Johnson), 12:42-13:9, 13:64-14:27. This self-alignment technique is an essential aspect by which Johnson minimizes the distances between the pillars and thus maximizes the density of the memory array. Ex. 1010 (Johnson), 18:54-19:4. This self-alignment technique would not be possible without uniform pillar dimensions. Any additional thickness in the pillars in the steering element due to the existence of the JFET gates and their interconnection would make the coupling between Johnson's circuit and physical designs impossible and would have profound consequences on the effectiveness of the overall design. A POSITA, with his/her limited experience with complex, 3D circuit structures and without guidance from Johnson or any other references pointed to by Petitioner on how to do this would not be able to create such structures without undue experimentation, nor would the

POSITA have any expectation of success in changing the steering element from a simple vertically oriented PN junction diode or a Schottky diode to a diode-connected JFET.

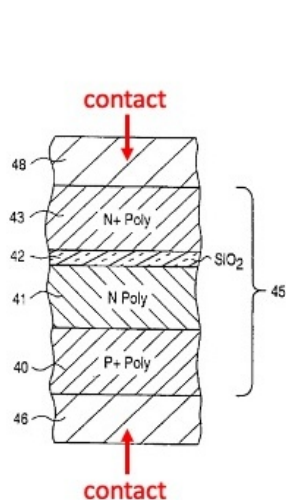
185. This same observation is true of the other transistor-based steering element proposed in Johnson (Ex. 1010 (Johnson)) at 7:67-8:1. A vertically-oriented diode connected MOSFET would also necessarily have gate oxide, gates, and gate to drain connections constructed on at least one side of each pillar:



186. For the same reasons articulated above with respect to the fabrication of a JFET-based steering element, a POSITA would not be able to create such structures without undue experimentation nor would the POSITA have any

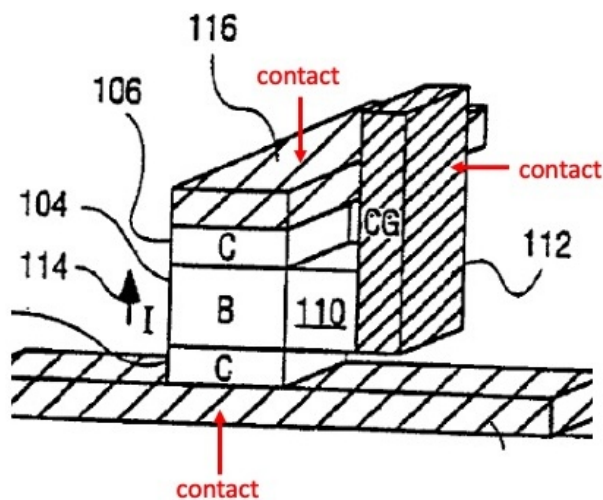
expectation of success in transforming the disclosure of Johnson from a PN junction diode or a Schottky barrier diode steering element 22 into a diode-connected or floating gate MOSFET-based design at all or without dramatically and adversely impacting the density of the resulting memory array.

187. Indeed, as shown in Figure 6(a), one of Johnson’s pillars had contacts 46 and 48 on the bottom and top of its pillar to “form a PN junction diode (the steering element)” and an “antifuse.” Ex. 1010 (Johnson), 12:1-12. As illustrated below, compared with Lee’s transistor, Johnson’s Figure 6(a) did not show gates or additional contacts that would be needed to create a 3-terminal transistor-based steering element and to interconnect it into the memory cell. Ex. 1010 (Johnson), 12:1-41.



Johnson's diode

Fig. 6(a) (excerpted, annotated)



Lee's transistor

Fig. 1A (excerpted, annotated)

Ex. 1010 (Johnson), Figure 6(a), excerpted and annotated; Ex. 1007 (Lee), Figure 1A, excerpted and annotated.

188. As evident from Johnson’s disclosure, Johnson’s design is built with a two terminal pillar with minimal top-and-bottom contacts. Ex. 1010 (Johnson), 11:22-67. To simplify deposition and increase density, Johnson deliberately disclosed diodes without gates or wiring alongside its pillars. Ex. 1010 (Johnson), 11:22-25, Figures 4(a), 6(g). In Johnson, the contacts were used to self-align and etch the pillar underneath to “make[] stacking especially simple and flexible.” Ex. 1010 (Johnson), 11:22-25, Figures 6(a)-6(g). Johnson fabricates its pillar structure that way, as shown, for example, in Figure 6(g) below.

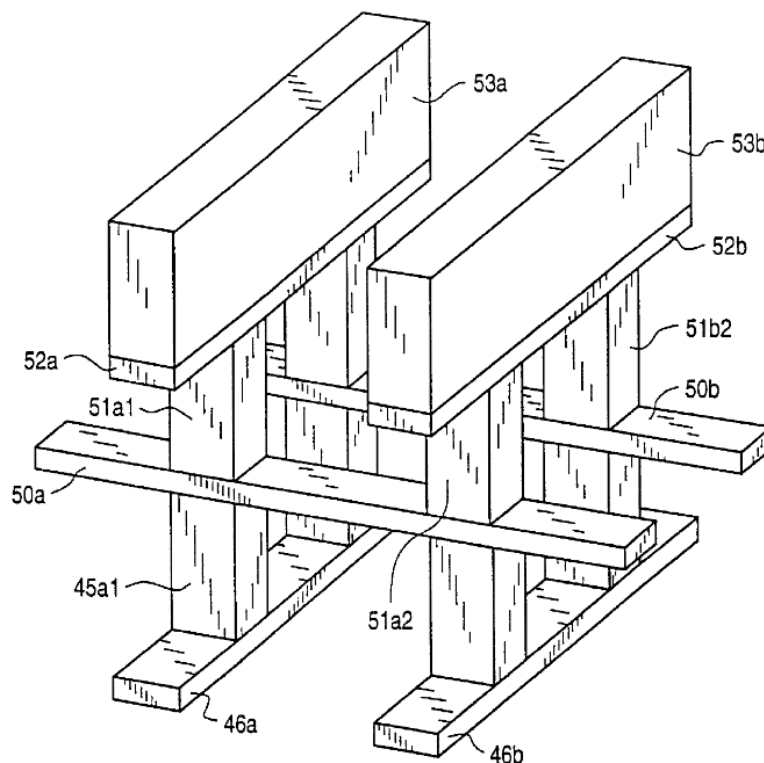


FIG. 6(g)

Ex. 1010 (Johnson), Figure 6(g).

189. For these reasons, a POSITA would not have been able to use Johnson's design with transistors without undue experimentation and likely not at all. And a POSITA would not be motivated to replace Johnson's simple diodes with transistors, and would not have had a reasonable expectation of success in making such a transformation. Without any motivation or an expectation of success, Petitioner's implicit obviousness combination of the disclosure of 7:65-8:1 of Johnson (Ex. 1010) with the multiple embodiments based on a PN junction diode or a Schottky barrier diode fail. Without a valid combination of this sort, the disclosure of Johnson

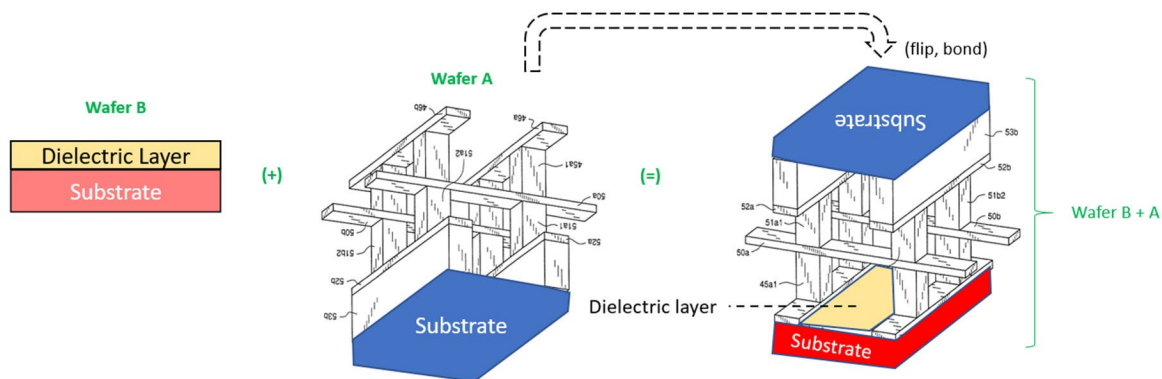
is limited to implementations with diodes for the steering elements and fails to disclose any memory cells with transistors.

H. Ground 2B: Obviousness over Johnson and Kim (Claim 13)

190. In Ground 2B, the Petition asserts obviousness of Claim 13 based on the combination of Johnson and Kim. Petition, pp. 3, 74. I disagree.

191. Petitioner asserts in Ground 2B that a POSITA, under the “proper” construction of stackable add-on layer, would have found Claim 13 obvious over Johnson and Kim. Petition, p. 74. For the most part, Petitioner relies on the recitation of Ground 2A (Claim 13 is obvious over Johnson alone). Accordingly, for at least the same reasons explained above in Section XI.G, for Ground 2A—including Johnson’s failure to show obviousness of “nonvolatile memory cells having at least one transistor” in Claim 13—Ground 2B fails as well.

192. In addition, with respect to element 13(c), Petitioner states in Ground 2B that the combination of Johnson and Kim together teaches this element. Petitioner admits that “Johnson discloses a series of deposition and etching steps as discussed in Section VII.G” of the Petition. Petition, p. 74. The Petition’s proposal for Johnson and Kim is shown below. Petitioner proposes fabricating Johnson’s substrate on Wafer B, and building Johnson’s pillars upside down on Wafer A, and then flipping them over and using wafer bonding.



Petition, p. 75.

193. The fabrication sequence taught by Johnson is very specific. The self-alignment feature described above with respect to Ground 2A uses the strips at each level to mask the etching of the previous level to form the pillars at the previous level. In Figure 6(g) of Johnson used in this alleged combination, strips 53a and 53b are on top and have just been used to mask the etching of the second level and the formation of pillars 51a1, 51a2, 51b2, and the other pillars on that level. Ex. 1010 (Johnson), 13:58-14:27. In the inverted version shown in the Petition, strips 53a and 53b have no purpose. It would make no sense to deposit layer 53 on top of the blue substrate, deposit metal layer 52 on top of it and then etch both into strips. The strips provide no function and the step required to deposit layer 53 merely adds cost and diminishes yield. A POSITA would understand that these structures serve no purpose and would bring into question the combination being proposed and the method proposed by Petitioner. A POSITA's expectation of success in recreating the

structure depicted in the Petition would be substantially diminished by this incongruity.

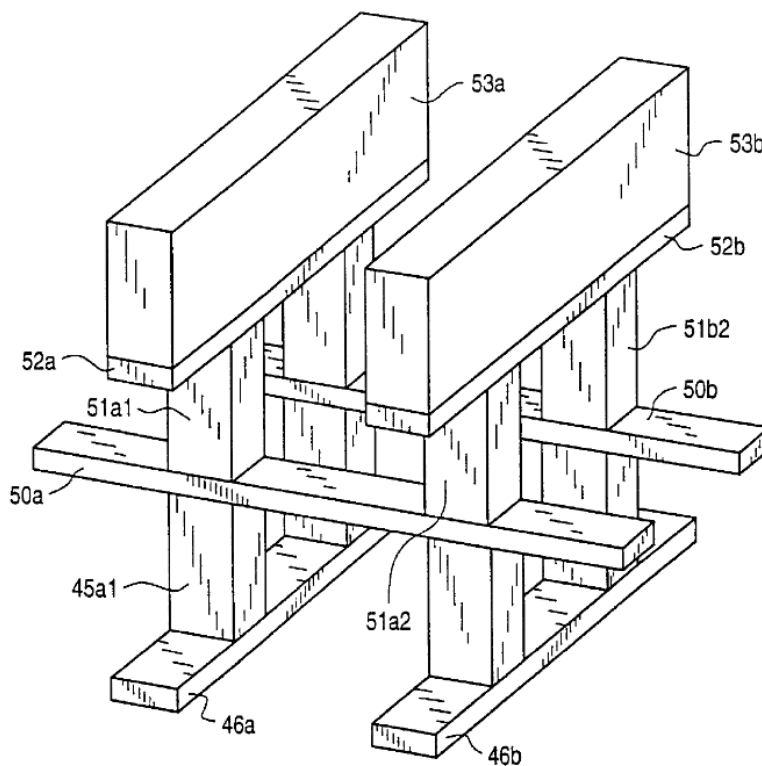


FIG. 6(g)

Ex. 1010 (Johnson), Figure 6(g).

194. To justify the combination of Johnson and Kim in this particular way, Petitioner make several incorrect statements. First Petitioner claims, that a POSITA would have “recognized that using wafer-bonding to bond Johnson’s layer of memory cells (‘stackable add-on layer’) to its insulating layer (‘dielectric layer’) would have been a predictable way to non-monolithically build Johnson’s 3D structure.” Petition, p. 75. On the contrary, this proposed hypothetical process would

not have been a predictable way to build Johnson’s 3D structure. This is because 1) Johnson’s 3D structure includes the possibility of more—perhaps many more—layers of memory cells, but Petitioner only describes a structure with two layers of memory cells, and 2) Petitioner specifically refers to Johnson’s CMOS transistors, but as explained above in Section XI.G for Ground 2A, Johnson’s process does not translate to the use of JFETs or CMOS transistors. Petition, p. 75.

195. Petitioner also says, “this modification consists of nothing more than using a known technique (Kim’s wafer bonding) to improve a similar known device (Johnson’s structure) in the same way (logic/memory stacking using a wafer bonding process).” Petition, pp. 75-76. But indeed, there is no improvement. In fact the alternative non-monolithic method of constructing Johnson’s memory device is inferior to the original because 1) it has unnecessary steps and elements, and 2) it, as described, does not allow for additional layers of memory cells. Petitioner also never explains how Kim’s stacking method, which brings with it issues of alignment, would mesh with Johnson’s specific method of fabricating a densely-packed and self-aligned memory cell array using deposition. Johnson specifically teaches away from prior art in which misalignment issues mandate a reduction in the resulting memory density.

196. Further, Petitioner’s resort to Figure 6(g) in its proposed combination is also problematic. Figure 6, including Figure 6(g), shows intermediate steps in

Johnson’s “fabrication sequence,” Ex. 1010 (Johnson), 12:42-43, and a POSITA would have understood that they were incomplete and unworkable by themselves. I understand that at his deposition, Dr. Sechen admitted he would need to refer to Aspar to achieve the combination of Johnson and Kim. Ex. 2039 (Sechen Deposition), 105:14-107:17 (“Q. Okay. So you meant to refer to Aspar there? A. Yes.”). Dr. Sechen’s admission confirms that a POSITA would have needed more than the teachings of Johnson and Kim to arrive at the claimed invention.

197. Finally, Petitioner says “this modification consists of nothing more than using a known technique (Kim’s wafer bonding) to improve a similar known device (Johnson’s structure) in the same way (logic/memory stacking using a wafer bonding process)” because quality control (which Petitioner specifies as looking for shorts) could be performed on the memory cells prior to bonding. Petition, pp. 75-76. This testing for shorts in the layer or pairs of layers would not generally lead to actionable data that would reduce the cost of the final result or reduce the amount of waste along the way. As also explained above for Ground 1C, wafer bonding would not provide quality control improvement over the testing that semiconductor fabs already perform, and Petitioner cannot credibly claim “less potential waste” when Kim involves discarding almost an entire wafer after each bonding. Indeed, as I explained in Section XI.C above, Petitioner provided no data to support its claim of better “quality control” or “less potential waste,” Petition, p. 76, and Dr. Sechen even

testified at his deposition that Johnson disclosed no access points to test for shorts, Ex. 2039 (Sechen Deposition), 107:18-112:4.

I. Ground 2C: Obviousness over Johnson and Aspar (Claim 13)

198. In Ground 2C, the Petition asserts obviousness of Claim 13 based on the combination of Johnson and Aspar. Petition, pp. 3, 77. I disagree.

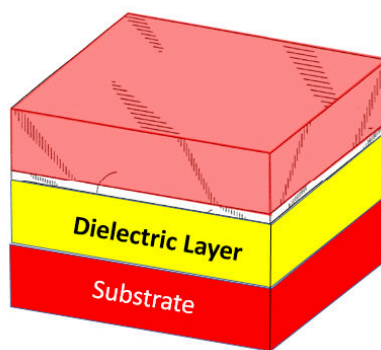
199. Ground 2C is similar to Ground 2B except that Aspar is used as the source of the wafer bonding technology instead of Kim. This method also involves constructing some of Johnson’s device upside down and in reverse order on a (blue) substrate prior to flipping one wafer on top of the other and then cleaving off the bulk of the carrier substrate (wafer A). Petition, pp. 78-80.

200. The flaws with this technique are similar to those outlined above with respect to Ground 1C (Lee/Aspar) and Ground 2B (Johnson/Kim). The motivations to combine outlined in the Petition are also essentially identical to those offered with respect to those other grounds. These motivations to combine are also flawed in the same ways as outlined above with respect to those other two grounds.

201. The net result is that a POSITA would not have had a reasonable expectation of success of building Johnson’s memory device in a non-monolithic way using the teaching of Aspar because the resulting device would be inferior and/or more expensive and/or not less wasteful.

202. For example, the Petition repeats the same better “quality control” and “minimizes waste” rationales from Ground 1E. Petition, p. 81. These rationales are again deficient. Because Wafer A is just an unpatterned doped stack from Johnson’s Figure 6(a) with no diodes formed yet, there is nothing to test, and Johnson did not disclose any access points for testing for shorts. Not surprisingly, Petitioner provided no data supporting its quality control claim. Aspar’s high-temperature annealing, which risked exceeding the thermal budget of Johnson’s device, would result in only more waste.

203. As explained for the Lee/Aspar combination in Ground 1E, Aspar’s high-temperature (1100°C) annealing after its splitting step eviscerates any motivation to use Aspar’s Smart-Cut process. Here, in Ground 2C, Petitioner asserts that the combined Wafer B+A shown below contains “Johnson’s ‘CMOS transistor[]’” control circuitry (red) and diode “doped stack” (pink). Petition, p. 78.

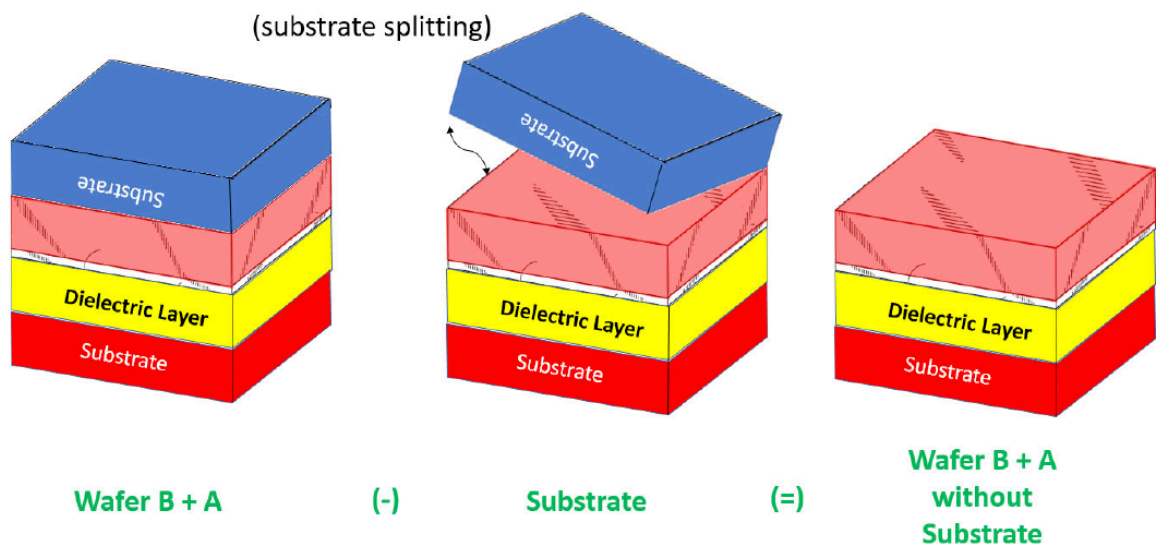


**Wafer B + A
without
Substrate**

Petition, p. 80. A POSITA would have known better than to expose the combined Wafer B+A to high temperature which risks exceeding the thermal budget of and damaging the device, as I explained for Ground IE above. *See* Section XI.E.

204. Petitioner also again distorts Johnson’s manufacturing process and proposes fabricating Figure 6(a) diode pillar upside down, Petition, p. 79 (“FIG 6(b) (inverted)”), even though a POSITA would have known that would only increase cost and lower yields, as explained for Ground 2B above. *See* Section XI.H. As also explained in Section XI.H above, Petitioner doesn’t show how Johnson’s self-aligned deposition process could be replaced with a stacking-based process, or how it would overcome the issues of alignment that Johnson’s method was meant to avoid.

205. Finally, as explained in Section XI.E above for Ground 1E involving Lee and Aspar, Petitioner does not explain how to use Aspar to transfer layers with devices, or how to get a clean cut in the right spot using Smart-Cut. Shown below is a segment of the Petition’s proposal for the Johnson/Aspar combination.



Petition, p. 80.

206. Petitioner again shows a thin film remaining, and Dr. Sechen agrees the thin silicon layer would be present after polishing. Ex. 2039 (Sechen Deposition), 68:19-73:21 (“you get a thin silicon layer on top of the oxide” remaining after splitting and polishing). Petitioner never explains how Aspar’s Smart-Cut can be used without leaving a thin layer of monocrystalline silicon that would obstruct Johnson’s upper metal contact (for example, conductors 26 in Johnson’s Figure 5 below).

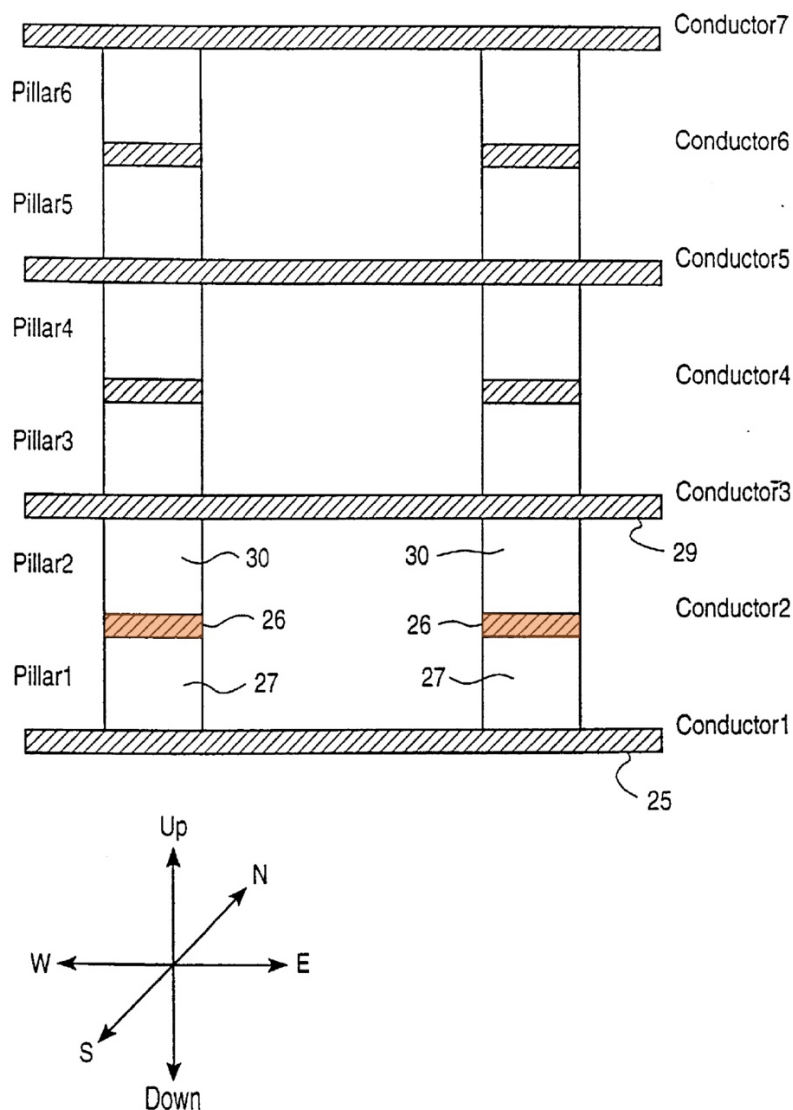


FIG. 5

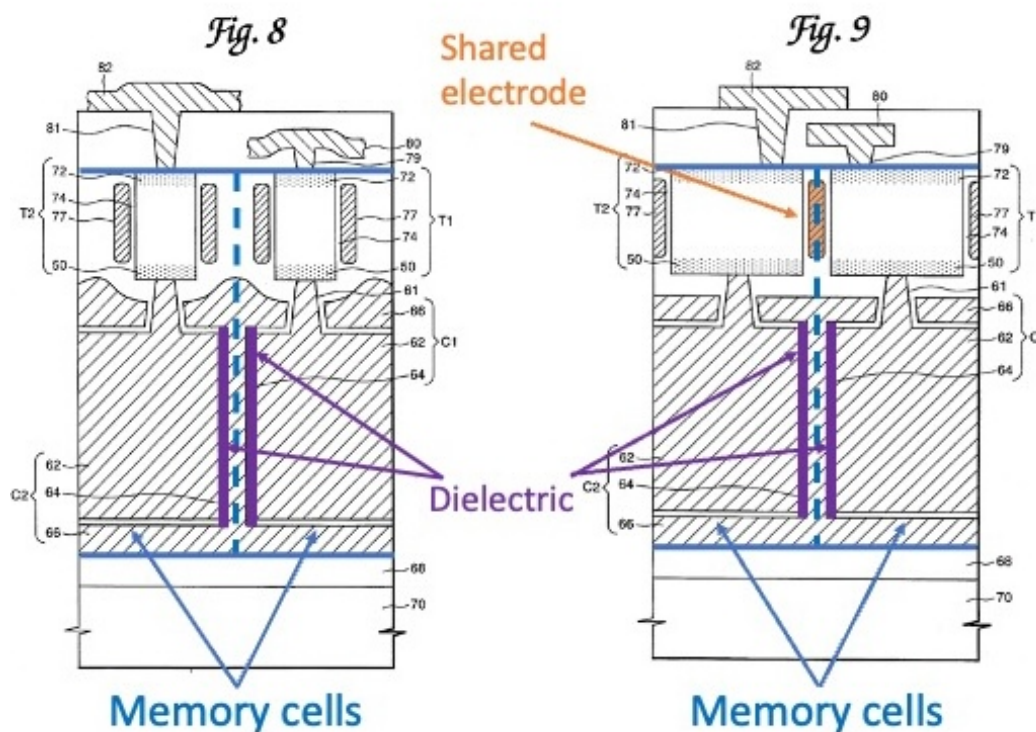
Ex. 1010 (Johnson), Figure 5, annotated.

J. Ground 3: Obviousness over Park and Kim (Claim 1)

207. In Ground 3, the Petition asserts obviousness of Claim 1 based on the combination of Park and Kim. Petition, pp. 3, 82. I disagree.

208. Claim 1 is the only challenged claim in the Petition that relates to volatile memory devices, in particular DRAM, instead of non-volatile memories. Petition, pp. vi-vii.

209. Element 1[b] requires in part that “the plurality of vertically oriented semiconductor memory cells [be] separated from each other by dielectric material.” Ex. 1001 (’702 Patent), 10:55-57. Petitioner and Dr. Sechen point to item 64 shown in Figures 8 and 9 of Park as allegedly disclosing this element. Petition, pp. 88-89; Ex. 1011 (Park), Figures 8-9.



Ex. 1011 (Park), Figures 8-9, annotated.

210. Item 64 in Figures 8 and 9 is the dielectric separating the storage electrode 62 of the DRAM storage capacitor and the plate electrode 66. Ex. 1011 (Park), 5:41-43 (“A plate electrode 66 surrounds the entire surface of the storage electrode 62, with a dielectric film 64 interposed therebetween.”). Each of the pair of items 64 indicated in Figures 8 and 9 is an integral part of the capacitor of each individual memory cell, *not* separating Park’s two memory cells. Items 64 do not separate the two memory cells shown in Figures 8 and 9 from each other. For example, as shown in Figures 8 and 9, in the bottom half of the figures, the plate electrode 66 is continuous across the memory cells, and no dielectric separates the memory cells in this portion of the physical structure being disclosed.

211. Moreover, Park explained that its transistors are only “isolated by an insulating material between the gate electrodes 33 in the bitline direction (see FIG. 8)” but “they share a gate electrode 77 in ... the wordline direction (see FIG. 9).” Ex. 1011 (Park), 5:49-53. This is shown, for example, in Figure 9 and also in Figure 7, which is a plan view of Figures 8-9. Ex. 1011 (Park), Figures 7, 9. Thus, rather than disclosing memory cells separated from each other by dielectric, Park disclosed transistors that are *electrically connected* via gate electrode 77 as shown in Figure 9.

XII. CONCLUSION

212. Based on the foregoing analysis, it is my opinion that Petitioner has failed to establish by a preponderance of the evidence that the Challenged Claims of the '702 Patent are unpatentable over the cited references.

213. In signing this Declaration, I recognize that the Declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be called upon to testify in deposition or before the Patent Trial and Appeal Board. If called upon to testify, I would testify truthfully and competently to all matters stated in this Declaration.

214. I reserve the right to supplement my opinions in the future to respond to any arguments that Petitioner raises and to take into account new information as it becomes available to me.

215. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true and that such statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: March 13, 2024

A handwritten signature in black ink, appearing to read 'Steven A. Przybylski', written over a horizontal line.

Steven A. Przybylski