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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

BESANG INC.,

Patent Owner.

Case No. IPR2023-00991

U.S. Patent No. 7,378,702

REMOTE VIDEOTAPED DEPOSITION

OF CARL SECHEN, Ph.D.,

February 27, 2024

9:00 a.m.

Reported By:

Randi J. Garcia, RPR

DIGITAL EVIDENCE GROUP

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1 Transcript of the deposition of
2 CARL SECHEN, Ph.D., called for Oral
3 Examination in the above-captioned matter,
4 said Deposition being taken pursuant to
5 Federal Rules of Civil Procedure by and
6 before RANDI J. GARCIA, Registered
7 Professional Reporter, and Notary Public, on
8 Tuesday, February 27, 2024, commencing at
9 approximately 9:00 a.m.

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18

19

20 Also Present:

21 Henry Marte, Videographer

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I N D E X

WITNESS: CARL SECHEN, Ph.D.

EXAMINATION

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1 THE VIDEOGRAPHER: We are now on the
2 record. My name is Henry Marte,
3 videographer on behalf of Digital Evidence
4 Group. Today's date is February 27, 2024.
5 And the time is 9:00 a.m.

6 This deposition is being held in the
7 matter of Intel Corp versus BeSang, Inc.
8 The deponent today is Dr. Carl Sechen.

9 All parties to this deposition are
10 appearing remotely and have agreed to the
11 witness being sworn in remotely.

12 Counsel please identify themselves
13 for the record, after which the court
14 reporter will administer the oath to the
15 witness.

16 MR. WILSON: Douglas Wilson of Armond
17 Wilson LLP for the patent owner Besang,
18 and with me is Josepher Li and Xu Zhou.

19 MR. BOWEN: Tyler Bowen of Perkins
20 Coie on behalf of petitioner Intel
21 Corporation. With me is Phil Morin.

22

1 C A R L S E C H E N, Ph.D., after having
2 been first duly sworn, was examined and
3 testified as follows:

4 EXAMINATION

5 BY MR. WILSON:

6 Q. Good morning, Dr. Sechen.

7 A. Good morning.

8 Q. Can you please state your name for
9 the record, your full name.

10 A. Yes. Carl Sechen.

11 Q. Where are you located today?

12 A. I'm in Dallas, Texas.

13 Q. And are you in the offices of a law
14 firm?

15 A. Yes. The Perkins Coie office.

16 Q. Okay. And where do you reside?

17 A. In Allen, Texas.

18 Q. Okay. You've been deposed before;
19 correct?

20 A. Yes.

21 Q. Approximately how many times?

22 A. Something over 25.

1 Q. Okay. So you understand the basic
2 ground rules of a deposition; correct?

3 A. Yes.

4 Q. All right. You understand that
5 you're under oath today; correct?

6 A. Yes.

7 Q. Okay. Is there any reason, as you
8 sit here this morning, that you cannot testify
9 fully, truthfully and accurately?

10 A. No.

11 Q. Okay. If you don't understand one of
12 my questions, I'll ask that you ask for
13 clarification. If you answer, I'll assume that
14 you understood. Okay?

15 A. Yes.

16 Q. Okay. We'll try to take breaks every
17 hour. If you need a break other than that,
18 just -- just ask. As long as a question is not
19 pending, we'll take a break.

20 You also understand that you are not
21 entitled to discuss your -- the testimony today
22 until I'm done with my direct examination?

1 Do you understand that?

2 A. Yes, I do.

3 Q. Okay. And you have a number of
4 people in the room there with you; correct?

5 A. Yes. There are two others.

6 Q. Who are they?

7 A. Tyler and Phil Morin.

8 Q. Okay. Do you have any access to any
9 communication device by which you might
10 communicate with anyone else?

11 A. No.

12 Q. Now, Mr. Bowen told me that you have
13 some exhibits already present there in front of
14 you.

15 A. Yes, I do. I believe there are four
16 of them. Exhibit 1003, which is my
17 declaration. Exhibit 1004, which is my CV.
18 Exhibit 1001, which is the '702 patent. And
19 Exhibit -- let's see. This one is not marked
20 but it's the '941 patent. Oh, there it is.
21 Exhibit 1005, the '941 patent.

22 Q. Okay. Do any of those exhibits that

1 you have there in front of you have any
2 markings, notes, any other -- anything other
3 than as they were originally produced to
4 BeSang?

5 A. No.

6 Q. Okay. Do you have any other notes or
7 documents available to you?

8 A. I do not.

9 Q. Okay. You have Exhibit 1003 there in
10 front of you. I'm happy to give you an
11 electronic copy on the computer as well,
12 whichever you prefer. But if you would like, I
13 can propagate that to you or -- or you can use
14 your paper copy. Up to you.

15 A. I think I'll -- I'd use my paper
16 copy.

17 Q. Okay.

18 MR. BOWEN: I'm sorry, Doug, would
19 you mind just putting it on anyway so --

20 MR. WILSON: Oh, sure, sure. So
21 let's -- let's post Exhibit 1003.

22 THE VIDEOGRAPHER: Yes. And let me

1 know when you're ready, when you want me
2 to bring it up on the screen, but it's
3 already in the box.

4 MR. WILSON: Okay.

5 (Thereupon, Exhibit 1003 was marked for
6 identification.)

7 BY MR. WILSON:

8 Q. Okay. Dr. Sechen, can you turn to
9 last page of Exhibit 1003.

10 A. Okay. Yes.

11 Q. Okay. Is that your signature?

12 A. Yes, it is.

13 Q. Okay. It's dated June 1st, 2023;
14 correct?

15 A. Yes.

16 Q. Okay. Exhibit 1003 is a complete
17 statement of your opinions offered in this
18 case; correct?

19 MR. BOWEN: Objection, form.

20 THE WITNESS: Well, that may be --
21 there may be a legal element to that
22 question, but certainly with respect to

1 the information put forth to me, it
2 certainly is a summary of my opinions
3 that -- as of June 2023.

4 BY MR. WILSON:

5 Q. Okay. You don't have any opinions
6 that you hold with respect to this IPR that are
7 not expressed in Exhibit 1003, do you?

8 MR. BOWEN: Objection, form.

9 THE WITNESS: I'm not sure exactly
10 how to answer. I -- certainly one's
11 knowledge refines over time regarding most
12 subjects, so...

13 BY MR. WILSON:

14 Q. Well, let me -- let me strike that
15 and then ask a more precise question.

16 You didn't have any opinions as of
17 June 1st, 2023 that are not expressed in
18 Exhibit 1003, with respect to this IPR, did
19 you?

20 MR. BOWEN: Objection, form.

21 THE WITNESS: I -- I believe that
22 summarizes my opinions as of June 1st,

1 2023.

2 BY MR. WILSON:

3 Q. Okay. You reviewed Exhibit 1003
4 prior to your deposition today; correct?

5 A. Yes.

6 Q. Did you find any mistakes or errors
7 that you wanted to correct?

8 A. Not that I recall.

9 Q. All right. So as you sit here today,
10 you are confident in the opinions you expressed
11 in Exhibit 1003?

12 MR. BOWEN: Objection, form.

13 THE WITNESS: Yeah. I would need to
14 know which opinions you're talking about,
15 actually, to -- to make a global
16 statement, but -- but nothing comes to
17 mind right away.

18 BY MR. WILSON:

19 Q. Okay. So as you sit here this
20 morning, you're not aware of any opinions in
21 which you are not confident in Exhibit 1003;
22 correct?

1 A. I think that's true.

2 Q. Now, you worked with the law firm of
3 Arnold & Porter in preparing your declaration
4 that is Exhibit 1003; correct?

5 A. I believe so. Yes.

6 Q. And you worked with Jessica Kaiser?

7 A. Yes.

8 Q. Okay. And she has subsequently moved
9 to the firm Perkins Coie?

10 A. I believe so.

11 Q. Okay. Did you work with anyone else
12 in preparing your declaration in this case?

13 A. There may have been other attorneys
14 involved. Frankly, I don't remember who they
15 were.

16 Q. Did -- did you work with anyone at
17 Intel in preparing your declaration?

18 A. No.

19 Q. You didn't speak to anyone at Intel
20 about the contents of your declaration?

21 MR. BOWEN: Objection, form.

22 THE WITNESS: I don't think so. I

1 don't recall any.

2 BY MR. WILSON:

3 Q. Do you know if anyone at Intel
4 reviewed your declaration before it was
5 submitted in this IPR?

6 A. I wouldn't know that.

7 Q. Okay. Let's turn to paragraph 18 of
8 your declaration.

9 A. Okay, I'm there.

10 Q. Now, paragraph 18 lists the materials
11 that you considered in preparing the opinions
12 expressed in your declaration; correct?

13 A. Yes.

14 Q. And that's a complete list of the
15 materials you considered in forming your
16 opinions expressed in your declaration;
17 correct?

18 MR. BOWEN: Objection, form.

19 THE WITNESS: In terms of outside
20 materials, I believe that's true. You
21 know, of course, I also rely on my own
22 experience as well. But in terms of

1 outside material, that's probably true.

2 BY MR. WILSON:

3 Q. Okay. Did you review any of these
4 documents in preparing for your deposition
5 today?

6 A. Yes.

7 Q. Did you review any other materials
8 outside of the documents in paragraph 18 in
9 preparing for your deposition today?

10 A. I did some online searches.

11 Q. Okay. Did you review the deposition
12 transcript of Dr. Lee from the Micron IPR?

13 A. I did not.

14 Q. Okay. Okay. Let's turn to
15 paragraph 84 of your declaration.

16 A. All right, I'm there.

17 Q. Okay. In paragraph 84 you state that
18 you were "asked to assume that the patent owner
19 may argue that 'the stackable add-on layer is
20 being bonded,' encompasses any layer that is
21 directly or indirectly adhered to the recited
22 layer of the substrate."

1 Did I read that correctly?

2 A. I think so.

3 Q. So you haven't seen any evidence that
4 patent owner takes that position; correct?

5 MR. BOWEN: Objection, form.

6 THE WITNESS: I -- as I wrote here, I
7 was simply asked to assume that the patent
8 owner may make that argument.

9 BY MR. WILSON:

10 Q. Okay. And in your opinion that
11 argument, if patent owner were to make it,
12 would be incorrect; correct?

13 A. Yes.

14 Q. Now, take a look at paragraph 91.

15 A. Okay.

16 Q. And there you assert that in your
17 opinion SOI pillar "requires a pillar-shaped
18 doped stack structure formed in a stackable
19 add-on layer added using SOI technology;"
20 correct?

21 A. Yes.

22 Q. What is a pillar-shaped structure?

1 A. Well, let's see, it's a pillar-shaped
2 doped stacked structure in particular. And --
3 and so it's constructed by having a stackable
4 add-on layer that's doped. And then you etch
5 away some portion of it and what you're left
6 with is called a pillar-shaped doped stacked
7 structure.

8 Q. Okay. How do I know if I have
9 something that is pillar-shaped?

10 A. Basically the '702 patent and the Lee
11 reference both demonstrate that once you have
12 etched away the -- the non-desired doped
13 portions of these stackable add-on layer, what
14 you're left with is a pillar-shaped doped stack
15 structure. And that's how they define it.

16 Q. Okay. So what is a pillar shape?

17 MR. BOWEN: Objection, form.

18 THE WITNESS: Well, I mean, this is
19 now going outside the scope of -- of the
20 '702 patent and the '941 patent. And, you
21 know, do -- do we really want to go there?
22

1 BY MR. WILSON:

2 Q. I -- I would like to.

3 A. All right. So if we're not talking
4 about this case at all, what is a pillar-shaped
5 object? You know, you might see these in front
6 of buildings for protection nowadays so that
7 vehicles can't drive too close. So they're
8 made of concrete, they have a certain height,
9 certain width, for example.

10 I -- I honestly haven't looked at a
11 dictionary to come up with something because
12 I -- I've just been studying the patent and the
13 specifics of this case up to now.

14 Q. So pillar-shaped might mean taller
15 than it is wide, for example; correct?

16 MR. BOWEN: Objection, form.

17 THE WITNESS: I don't really know
18 that. I -- I haven't seen the '702 patent
19 indicate that.

20 BY MR. WILSON:

21 Q. I -- I'm just asking you for the
22 plain and ordinary meaning of the term

1 "pillar."

2 MR. BOWEN: Objection, form.

3 THE WITNESS: I have not attempted a
4 definition of that, so I -- I don't
5 really -- I'm not prepared to answer it.

6 BY MR. WILSON:

7 Q. So as you sit here today, you don't
8 know what the plain and ordinary meaning of the
9 term "pillar" is; correct?

10 MR. BOWEN: Objection, form.

11 THE WITNESS: Well, I gave you an
12 example of what a -- an example of a
13 pillar. But -- but if -- so we're talking
14 outside the scope of this case, I -- I'm
15 not -- yeah. Again, I haven't studied
16 dictionaries. I'm not sure -- you know,
17 typically in such cases if you want a
18 plain and ordinary meaning outside the
19 scope of a case, you would look up five
20 dictionaries and see what the majority say
21 or something. But I haven't done that
22 task. So I don't really know.

1 BY MR. WILSON:

2 Q. So -- so you would agree, then, you
3 know, in the dictionary, for example, the term
4 "pillar" has plain and ordinary meaning;
5 correct?

6 MR. BOWEN: Objection, form.

7 THE WITNESS: Yeah, outside the scope
8 of what we're doing here in this case,
9 there -- there's some plain and ordinary
10 meanings. I'm sure they exist. And, of
11 course, those would most likely be at odds
12 with what a patent writer in this case had
13 in mind. But nonetheless, there may be
14 some plain and ordinary meanings there.

15 BY MR. WILSON:

16 Q. Okay. But you haven't researched
17 those, and as you sit here today, you don't
18 know what that would be, the plain and ordinary
19 meaning of "pillar"; correct?

20 MR. BOWEN: Objection, form.

21 THE WITNESS: I have not searched the
22 dictionaries to see what various meanings

1 it might have that are, of course, outside
2 the scope of this case.

3 BY MR. WILSON:

4 Q. Okay. Let's look at paragraph 92 of
5 your declaration.

6 A. Yes.

7 Q. There you say you've "been asked to
8 assume that the patent owner may argue that
9 'SOI pillar' encompasses any pillar-shaped
10 structure with insulating material below it."
11 Correct?

12 Did I read that correctly?

13 A. Yes.

14 Q. And it's also correct that you have
15 not seen any evidence that patent owner has
16 taken that position; correct?

17 A. That's true.

18 Q. Now, you also offer the opinion here
19 that if patent owner were to take that position
20 you believe it would be incorrect; right?

21 A. Yes. That's -- that's correct.

22 Q. All right. And let's take a look at

1 paragraph 93.

2 A. Okay.

3 Q. Paragraph 93 begins your discussion
4 of ground 1A; correct?

5 A. Yes.

6 Q. And that's where you assert that in
7 your opinion, Claims 13 through 17 of the '702
8 patent would have been obvious over Lee;
9 correct?

10 A. Yes.

11 Q. Now, in paragraph 93, you again
12 assert for addressing these claims, 13 through
13 17, that you've been asked to assume that
14 patent owner would argue certain constructions
15 of stackable add-on layer being bonded and SOI
16 pillar; correct?

17 A. Yes.

18 Q. And in the last sentence of
19 paragraph 93, you say, "Under these
20 constructions, Claims 13 through 17 would have
21 been obvious over Lee for the reasons I
22 discussed below." Correct?

1 A. Yes.

2 Q. So in offering your opinions that
3 Claims 13 through 17 would have been obvious
4 over Lee, in ground 1A, you are basing those
5 opinions on constructions that you believe are
6 incorrect; right?

7 A. Yes.

8 Q. Now, you do not offer the opinion
9 that Claims 13 through 17 would have been
10 obvious over Lee if stackable add-on layer
11 being bonded and SOI pillar were construed in
12 the manner you believe is correct; right?

13 A. I -- not -- yeah. Not in this
14 section here, yes. That's true.

15 Q. Well, not anywhere in Exhibit 1003;
16 correct?

17 A. Yeah. Not Lee standing alone.

18 Q. What is the plain and ordinary
19 meaning of the term "wafer" to a person of
20 ordinary skill in the art of the '702 patent?

21 MR. BOWEN: Objection, form.

22 THE WITNESS: Can we look at a

1 specific place? Let's see. Is there a
2 certain claim that you have in mind or --

3 BY MR. WILSON:

4 Q. No. I'm just asking in general. In
5 the subject matter of the '702 patent, what
6 does the term "wafer" mean?

7 MR. BOWEN: Objection, form.

8 BY MR. WILSON:

9 Q. I can point you to examples of usage.
10 For example, paragraph 61 of your declaration
11 you reference two wafers from the '941 patent.

12 A. Generally, a wafer is the piece of
13 material that a -- that is subject to a
14 sequence of processing steps. So it could
15 often be silicon, for example, but it doesn't
16 have to be.

17 But in the context of silicon, it
18 would be the fundamental piece of silicon that
19 is subject to a sequence of processing steps.
20 And nowadays, they might be as large as
21 300 millimeters in diameter.

22 Q. Okay. Is there any particular level

1 of processing that has to have occurred to have
2 a wafer?

3 MR. BOWEN: Objection, form.

4 THE WITNESS: Outside the scope of
5 this case, no.

6 BY MR. WILSON:

7 Q. So a wafer, for example, could just
8 be a layer of raw silicon?

9 A. It -- it could be. It could be that.
10 Again, outside the scope of this case, that's
11 true.

12 Q. Okay. What is the plain and ordinary
13 meaning of the term "chip" to a person of
14 ordinary skill in the art of the '702 patent?

15 MR. BOWEN: Objection, form.

16 THE WITNESS: Well, again, I -- I
17 don't want to -- just to -- say, to a
18 person of ordinary skill outside the scope
19 of this case, a -- a chip would be the
20 portion of a wafer that would
21 potentially -- would potentially be
22 packaged and used as a separate device

1 possibly on a printed circuit board or the
2 like.

3 BY MR. WILSON:

4 Q. Okay. Is there any particular level
5 of processing that has to have occurred to have
6 a chip?

7 MR. BOWEN: Objection, form.

8 THE WITNESS: Again, we're talking
9 outside the scope of this case, because
10 I'd need to look at the specific patents,
11 but -- but yeah. Not necessarily. It
12 wouldn't have to be at any particular
13 stage in the processing.

14 BY MR. WILSON:

15 Q. Well, for example, a -- a raw piece
16 of silicon wouldn't be a chip, would it?

17 MR. BOWEN: Objection, form.

18 THE WITNESS: I -- I -- yeah.
19 It's -- the term -- again, outside the
20 scope of this case, the term is most
21 commonly used to refer to a completely
22 processed piece of silicone or portion of

1 a wafer, but -- but you certainly have
2 seen the term used when it's not complete
3 either. So it can go either way.

4 BY MR. WILSON:

5 Q. Okay. But it wouldn't be used to
6 refer to a raw piece of silicon that was
7 completely unprocessed; correct?

8 MR. BOWEN: Objection, form.

9 THE WITNESS: Yeah. Normally it's
10 a -- a -- a chip would be a diced off
11 portion of the wafer so it -- or at least
12 an intended piece, an intended area on
13 that wafer that would -- would be
14 ultimately diced off.

15 So, you know, by visually inspecting
16 it under a microscope you could see where
17 the intended chips are, if there's been at
18 least some processing.

19 BY MR. WILSON:

20 Q. Well, for it to be a chip, there
21 would have been some processing; correct?

22 MR. BOWEN: Objection, form.

1 THE WITNESS: Possibly. But again,
2 I'd need to see the scope that we're
3 talking about. But in general, like I
4 said, it could be just an intended region
5 on a wafer that -- that would be the chip,
6 so I'm not sure how to answer that.

7 BY MR. WILSON:

8 Q. Can you think of an example where
9 someone would refer to a raw piece of silicon
10 as a chip?

11 MR. BOWEN: Objection, form.

12 THE WITNESS: Very possibly in
13 context of bonding, you might talk -- you
14 know, you might have a chip and you might
15 bond to it another chip that's not yet
16 processed, so in that context, I could see
17 that term being used.

18 BY MR. WILSON:

19 Q. Let's take a look at paragraph 121 of
20 your declaration.

21 Okay. In paragraph 121 you state
22 that, "In my opinion, Lee discloses or suggests

1 limitation 13(b) to the extent that a
2 'stackable add-on layer' encompasses any type
3 of layer that is directly or indirectly adhered
4 to the 'dielectric layer.'"

5 Did I read that correctly?

6 A. Yes.

7 Q. In paragraph 122 you state, "I note
8 that 'stackable add-on layer' is not so broad,
9 and further discuss in my opinions below how
10 13(b) is taught by the prior art under the
11 proper construction." Correct?

12 A. Yes.

13 Q. So in your opinion, Lee does not
14 disclose a stackable add-on layer; correct?

15 MR. BOWEN: Objection, form.

16 THE WITNESS: I wouldn't put it that
17 way. You know, it -- it doesn't teach the
18 stackable add-on layer under the patent
19 owner's apparent construction. But
20 under -- that's really what -- what's
21 being said there.

22

1 BY MR. WILSON:

2 Q. Well, in your opinion, Lee does not
3 teach a stackable add-on layer under the
4 construction that you believe is correct;
5 right?

6 A. I don't necessarily -- yeah. I don't
7 necessarily agree with that.

8 Q. Okay.

9 A. I don't -- I don't agree with that.

10 Q. You don't offer the opinion in
11 Exhibit 1003 that Lee teaches a stackable
12 add-on layer under the construction that you
13 believe is correct; right?

14 A. I -- I believe I do point to portions
15 of Lee that do describe that it -- it does
16 teach the possibility of a stackable add-on
17 layer in accordance with my construction.

18 Q. And where do you point to that?

19 A. There's, I think, roughly three
20 paragraphs that mention that. As I recall,
21 it's like 107 and 208 and 294.

22 Q. Okay. Let's take a look at

1 paragraph 107 of your declaration.

2 A. Sorry, of -- of Lee. I don't have
3 that here, do I?

4 Q. Did you refer to that in your
5 declaration?

6 A. I -- I do believe it's mentioned
7 in -- let's see, one or more of those
8 paragraphs of Lee that I just mentioned is in
9 my declaration.

10 It would be more much more efficient
11 to search on the computer to find where, but...

12 Q. So I -- I can tell you. I mean,
13 paragraph 124 you mentioned paragraph 107 of
14 Lee. Paragraph 132. Paragraph 178.
15 Paragraph 191 and 192. Paragraph 204. And
16 that is it. Those are all the places in your
17 declaration that you mention paragraph 107 of
18 Lee.

19 So let's just start there. Do any of
20 those paragraphs, 124, 132, 178, 191, 192, and
21 204 of your declaration mention a stackable
22 add-on layer?

1 MR. BOWEN: Objection, form.

2 THE WITNESS: I think 124 would.

3 (Clarification by the reporter.)

4 BY MR. WILSON:

5 Q. Okay. Let's look at paragraph 124 of
6 your declaration. Can you point me to the
7 words "stackable add-on layer"?

8 MR. BOWEN: Objection, form.

9 THE WITNESS: I mean, that's
10 basically what Lee in 107 is proposing.
11 And what I'm saying here is that each
12 level of 3104 could be a 2D array of
13 thin-film transistor EEPROMs.

14 BY MR. WILSON:

15 Q. Okay. You don't use the words
16 "stackable add-on layer" in paragraph 24 of
17 your declaration; correct?

18 MR. BOWEN: Objection, form.

19 THE WITNESS: In this case I use the
20 meaning of it, but not the words.

21 BY MR. WILSON:

22 Q. Okay. So is it your opinion that Lee

1 discloses a stackable add-on layer in Figure 35
2 under your understanding of the term "stackable
3 add-on layer"?

4 A. When I read Lee's paragraphs 107, 208
5 and 294, I do come to that opinion.

6 Q. Okay. You don't express that opinion
7 anywhere in Exhibit 1003; correct?

8 MR. BOWEN: Objection, form.

9 THE WITNESS: Well, I -- I think one
10 or both of those other paragraphs are
11 cited, and I believe paragraph 124 clearly
12 suggests that because it says each level
13 is a separate array of thin-film
14 transistor EEPROMs.

15 BY MR. WILSON:

16 Q. So let's look at paragraph 121. In
17 the first sentence of paragraph 121 you say,
18 "In my opinion Lee discloses or suggests
19 limitation 13(b) to the extent that a
20 'stackable add-on layer' encompasses any type
21 of layer there is directly or indirectly
22 adhered to the 'dielectric layer.'" Correct?

1 A. Yes.

2 Q. Now, in paragraph 122 you say, "I
3 note that 'stackable add-on layer' is not so
4 broad, and further discuss in my opinions below
5 how 13(b) is taught by the prior art under the
6 proper construction." Correct?

7 A. Right.

8 Q. So when you get to paragraph 124, are
9 you describing how Lee discloses limitation
10 13(b) under patent owner's construction that
11 you anticipate or under your own opinion as to
12 the definition of a stackable add-on layer?

13 A. I -- I believe it does both.

14 Q. Okay. You don't say that in
15 paragraph 124; correct?

16 MR. BOWEN: Objection, form.

17 THE WITNESS: I mean, Lee suggests it
18 and I just go with what Lee suggests here.

19 BY MR. WILSON:

20 Q. Okay. So you can't point me to
21 anywhere where you've expressed the opinion
22 that Lee discloses limitation 13(b) under your

1 understanding of that term in Exhibit 1003;

2 correct?

3 MR. BOWEN: Objection, form.

4 THE WITNESS: Well, I -- I do believe

5 a person reading -- a -- a POSITA reading

6 my report, for example, and -- and having

7 Lee would come to realize that it -- it

8 would -- would also have a stackable

9 add-on layer in accordance with my

10 definition.

11 BY MR. WILSON:

12 Q. Okay. So the answer to my question

13 is no?

14 MR. BOWEN: Objection, form.

15 THE WITNESS: I'm not sure. I have

16 to see where the -- those other two

17 paragraphs may be cited, but certainly,

18 maybe I could have expressed it more

19 clearly, but it clearly -- if you read

20 124, it's pretty clear that Lee is -- and

21 you specifically read paragraph 107 of

22 Lee, you can see that stacking 2D arrays

1 of thin-film transistor EEPROMs is one of
2 the things it teaches.

3 BY MR. WILSON:

4 Q. Okay. We'll take a look at
5 paragraph 107 of Lee in a minute.

6 So let's take a look at paragraph 140
7 of your declaration. Now, paragraph 140 you
8 say, "Patent owner may argue 'SOI pillar'
9 encompasses any pillar-shaped structure with
10 insulating material below it." Correct?

11 A. Yes.

12 Q. And then you say Lee discloses or
13 suggests this limitation under such a
14 construction; correct?

15 A. Yes.

16 Q. Now, in the middle of the sentence in
17 paragraph 140 you say, "In my opinion such a
18 construction is incorrect because it is
19 inconsistent with the intrinsic evidence."
20 Correct?

21 A. Yes.

22 Q. So you do not believe that Lee

1 discloses an SOI Pillar under the proper
2 construction as you see it of SOI pillar;
3 correct?

4 A. Well, if you ignore paragraphs 107,
5 208 and 294 of Lee, one may come to that
6 conclusion.

7 Q. Well, one may come to that conclusion
8 based on what you wrote there in paragraph 140;
9 correct?

10 MR. BOWEN: Objection, form.

11 THE WITNESS: Right. So in -- in
12 writing that paragraph I did not consider
13 the teachings of paragraphs 20 -- 107, 208
14 and 294.

15 BY MR. WILSON:

16 Q. Okay. Let's take a look at
17 paragraph 156 of your declaration.

18 Do you have paragraph 156?

19 A. Yes.

20 Q. Okay. In paragraph 156 you describe
21 a further etched process by which the level 2
22 pillar strips in Figure 25A will be made into

1 pillars; correct?

2 A. I believe that's right. Okay --
3 something, but it sounds right.

4 Q. It's -- it's summarizing basically.
5 And in that same paragraph you opine that Lee
6 describes an iterative process occurring in
7 Figures 13 through 28 to -- to create a
8 complete structure; correct?

9 MR. BOWEN: Objection, form.

10 THE WITNESS: Which part are you
11 referring to?

12 BY MR. WILSON:

13 Q. Right in the middle of the paragraph,
14 it says, "Lee discloses an iterative process
15 for fully fabricating its levels including
16 level 2 and there you cite Figures 13 through
17 28." Correct?

18 A. Yeah. Okay. "Lee discloses an
19 iterative process for fully fabricating its
20 levels, including level 2." Yes.

21 Q. Okay. So let's --

22 MR. WILSON: Henry, can you propagate

1 Exhibit 1007.

2 Let's take a look at Lee.

3 THE VIDEOGRAPHER: The document is
4 up. Make sure you refresh the page on the
5 box.

6 THE WITNESS: Oh, okay.

7 All right.

8 (Thereupon, Exhibit 1007 was marked for
9 identification.)

10 BY MR. WILSON:

11 Q. Okay. Let's look at -- so -- so you
12 have in front of you Exhibit 1007, which is the
13 Lee reference we've been discussing; correct?

14 A. Yes.

15 Q. And you've reviewed Lee and are
16 familiar with it; correct?

17 A. Yes.

18 Q. Okay. Take a look at -- and I'll
19 just tell you it's PDF page 101, but I want to
20 look at paragraph 161. It's on the bottom
21 right of that page.

22 A. Lost the -- okay. Here we go.

1 Was it page 161 or -- or did I get
2 that mixed up?

3 Q. It's page 101, 1-0-1.

4 A. All right.

5 Q. And paragraph 161 in the lower right?

6 A. Okay.

7 Q. So this paragraph is in the midst of
8 that string of Figures 13 through 28 where you
9 described forming -- let's see. Fully
10 fabricating its levels; correct?

11 A. Yeah. It says here, an iterative --
12 iterative process for fully fabricating its
13 levels, yes.

14 Q. Paragraph 161 begins, "Once the
15 second pillar film stack 1338 and second
16 conductor 1336 have been patterned by etching
17 into a strip 1340, the etch is continued to
18 remove the portion 1341 of the first pillar
19 strips 1318 not covered or masked by the second
20 pillar strips 1340 as shown in Figures 23A and
21 23B." Correct?

22 A. Yes.

1 Q. So at this point, the second pillar
2 film stack level 2 has been added as shown in
3 Figures 23A and 23B; correct?

4 A. Okay. Any way to get a paper copy of
5 this because I need to see the figure at the
6 same time as the text somehow?

7 Q. You -- you can probably open a new
8 window --

9 A. Okay.

10 Q. -- PDF viewer and just pop up, you
11 know, the text and the figure side by side.

12 A. Let's see.

13 THE VIDEOGRAPHER: I can also bring
14 it up to the screen. It's up to you,
15 guys.

16 MR. WILSON: Yeah. If you could do
17 that and just pull up the -- Figure 23A
18 side by side with the text we're
19 referencing.

20 BY MR. WILSON:

21 Q. All right. Dr. Sechen, can you see
22 that now?

1 A. Yes.

2 Q. Okay. So -- so the level 2 pillar
3 strips are shown there labeled as 1340 and
4 Figure 23A; correct?

5 A. Yes.

6 Q. Okay. And then the level 1 pillars
7 that were created are shown there as 1342;
8 correct?

9 A. Yes.

10 Q. Now, they were created -- or sorry,
11 let me strike that.

12 The level 2 pillar strips are used as
13 a mask to etch the level 1 pillars 1342;
14 correct?

15 A. Yes. I believe that's right.

16 Q. Okay. Let's -- let's go back to your
17 declaration, paragraph 156. You have that in
18 front of you, Dr. Sechen?

19 A. Yeah, I do.

20 Q. Okay. So middle of that
21 paragraph 156, right after the reference to
22 Figures 13 through 28, you say, "Based on the

1 disclosed fabrication process, in my opinion, a
2 POSITA would have understood after the
3 subsequent etch step I discuss about, level 2
4 would be pillars (not pillar strips) and have
5 the same cross section depicted in Figure 25A
6 (as I have reproduced and annotated above)."

7 Did I read that correctly?

8 A. Yes.

9 Q. Okay. So what you're describing is
10 using level 3 pillar strips as a mask to create
11 level 2 pillars; correct?

12 A. Or is it level 2 to create level 1?
13 I -- I don't recall any discussion of level 3
14 in what we've been looking at, but...

15 Q. Well, level 2, as shown in Figure
16 25A, are pillar strips; correct?

17 MR. BOWEN: Objection to form.

18 THE WITNESS: Well, I call them
19 pillars.

20 BY MR. WILSON:

21 Q. You see right above paragraph the
22 middle of the paragraph 156, you say, "Although

1 level 2 of Lee's Figure 25A remains in pillar
2 strip form"?

3 A. Oh, yes. That's right. That -- that
4 is correct. That's an intermediate form before
5 it's converted to actual pillars, yes.

6 Q. So the way that level 2 is converted
7 into pillars is by using level 3 as a mask;
8 correct?

9 MR. BOWEN: Objection, form.

10 THE WITNESS: I believe that is
11 stated in Lee somewhere that that's the
12 case.

13 BY MR. WILSON:

14 Q. We can look again at Lee, if -- if
15 you need to refer to it.

16 A. Yeah. I -- I seem to recall that
17 that's correct.

18 Q. Now, you can see that in Figure 25A
19 as you've shown it there, levels 1 and 2 share
20 a common control gate; correct?

21 MR. BOWEN: Objection, form.

22 THE WITNESS: That appears to be the

1 case. I don't -- this may be an
2 intermediate step in the fabrication, but
3 that appears to be the case.

4 BY MR. WILSON:

5 Q. Okay. When level 3 is added, and
6 used to pattern the level 2 pillars, levels 2
7 and 3 will also share a common control gate;
8 correct?

9 MR. BOWEN: Objection, form.

10 THE WITNESS: Well, we should look at
11 Figure 27A because the situation changes
12 considerably.

13 BY MR. WILSON:

14 Q. Okay. Let's look at Figure 27A.
15 You have Lee; correct?

16 A. Yeah. And so you can see now that
17 level 1 and level 2 do not share a common gate
18 at this stage in the processing.

19 Q. Really. So in your opinion in
20 Figure 27A, level 1 and level 2 no longer share
21 a common control gate?

22 A. I don't believe it makes sense to

1 have a common control gate.

2 Q. Okay. So if Lee disclosed it, they
3 shared a common control gate at the stage in
4 Figure 27A, that wouldn't make sense?

5 MR. BOWEN: Objection, form.

6 THE WITNESS: I said this is an
7 intermediate processing step. You know,
8 it's like a -- a car, if you half built
9 it, it doesn't run. And you get all
10 frustrated, but you've only half built it.

11 Same thing here, if you look at
12 something half baked, it's not what you
13 expect, you know, the final product would
14 be.

15 BY MR. WILSON:

16 Q. Okay. So I don't understand what
17 you're referring to as half baked. But what --
18 what do you mean by that with reference to
19 Figure 27A?

20 A. Well, 27A shows further fabrication
21 steps, where -- whereby there's a separate
22 control gate for the level 1 transistors.

1 Q. Okay. So do you believe that in
2 forming Figure 27A, the common control gate's
3 between levels 1 and 2 in Figure 25A were
4 removed?

5 A. That's my understanding.

6 Q. Okay. Now, let's take a look at
7 Figure 1A of Lee.

8 Now, in Figure 1A of Lee, items 103
9 and 116 are conductors; correct?

10 A. Could you repeat that. I'm sorry.

11 Q. Yeah. Figure 1A of Lee, items 103
12 and 116, are conductors; correct?

13 A. 103 and 116 are conductors, yes.

14 Q. As shown in Figure 1A, 103 extends
15 along the X axis and 116 extends along the
16 Y axis; correct?

17 A. Yes.

18 MR. WILSON: Okay. Henry, can we
19 mark Tab 1 as Exhibit 2023.

20 (Thereupon, Exhibit 2023 was marked for
21 identification.)

22 MR. BOWEN: Doug, we've been going

1 about an hour. Are you getting to a spot
2 where we could take a break?

3 MR. WILSON: Sure. Right after this
4 exhibit.

5 BY MR. WILSON:

6 Q. So, Dr. Sechen, the top figure
7 labeled "Series Circuit," do you agree that the
8 two light bulbs there are connected in series?

9 A. Yeah. Sure.

10 Q. And let's look at the bottom figure
11 labeled parallel circuit. Do you agree that
12 the two light bulbs in this circuit are in
13 parallel?

14 A. Yeah. I -- I think a better example
15 would have been resistors instead of light
16 bulbs, but that -- this works, essentially.

17 Q. Okay. Do you also agree that the two
18 light bulbs in this circuit are not connected
19 in series?

20 MR. BOWEN: Objection, form.

21 THE WITNESS: You can say these two
22 light bulbs are not connected in series

1 with the battery. That's what you can
2 say. You know, you -- if you take the
3 battery away, then you can say that these
4 two light bulbs are in series with each
5 other.

6 MR. WILSON: Okay. Okay. We can
7 take a break now.

8 MR. BOWEN: Sounds good. Maybe about
9 10 minutes, does that work?

10 THE VIDEOGRAPHER: One second,
11 please.

12 The time is 10:01 a.m. We're going
13 off the record.

14 (Thereupon, a brief recess was taken.)

15 THE VIDEOGRAPHER: The time is
16 10:11 a.m. Back on the record.

17 MR. WILSON: Okay. Henry, let's mark
18 Tab 3 as Exhibit 2024.

19 (Thereupon, Exhibit 2024 was marked for
20 identification.)

21 BY MR. WILSON:

22 Q. Now, Dr. Sechen, Exhibit 2024 are

1 excerpts from a book entitled VLSI Memory Chip
2 Design.

3 Have you ever seen this book before?

4 A. Yeah. At some point I have, but it's
5 been quite a while since I've looked at that.

6 Q. Okay. I want to look at page 39 of
7 Exhibit 2024, that's PDF page 49.

8 Now, you see Figure 1.33 there at the
9 top?

10 A. Yes.

11 Q. Now, that shows a circuit in three
12 different states; correct?

13 A. Let's see. Yeah, I do see the --
14 certainly the -- the arrays for A and the
15 writing for B and then reading for C. I do see
16 that.

17 Q. Okay. I'm referring specifically to
18 the arrays on the right side of Figure 1.33,
19 the circuit schematics there.

20 Do you see those?

21 A. Yes.

22 Q. All right. Are any two transistors

1 in that circuit in series?

2 MR. BOWEN: Objection, form.

3 THE WITNESS: Let's see. I -- let's
4 see. I may have to review this section of
5 the book a bit, because I -- I'm not sure
6 exactly the architecture they have in mind
7 here for this flash memory.

8 BY MR. WILSON:

9 Q. So you -- you -- do you have an
10 electronic copy there of Exhibit 2024?

11 A. Well, let me see.

12 THE VIDEOGRAPHER: Refresh the box.

13 BY MR. WILSON:

14 Q. If you need to review it, you can
15 start on page 38 of Exhibit 2024 under the
16 heading "The NOR Cell."

17 A. I'm sorry, what page did you --

18 Q. Page 38. So it's PDF page 48, but
19 page 38 of the book.

20 A. Oh, okay.

21 Q. Where it begins the discussion of
22 "The NOR Cell."

1 A. Okay. I see. Okay. I think I
2 follow that architecture.

3 Q. Okay. So I -- I want to go back,
4 then, to my question before. Any two
5 transistors in Figure 1.33 of Exhibit 2024
6 connected in series?

7 MR. BOWEN: Objection, form.

8 THE WITNESS: Well, how do we want to
9 define "series"? These are three terminal
10 devices, so we need to define how we mean
11 that.

12 BY MR. WILSON:

13 Q. How would you define it?

14 A. Well, I suppose you could go, you
15 know, like source drain -- source drain type
16 series, I suppose. You -- you could do that, I
17 guess.

18 Q. Okay. Under that definition, are any
19 two transistors in Figure 1.33 of Exhibit 2024
20 connected in series?

21 MR. BOWEN: Objection, form.

22 THE WITNESS: Apparently not.

1 BY MR. WILSON:

2 Q. Okay. You would agree that in
3 Figure 1.33 there is a data line between each
4 pair of transistors; correct?

5 MR. BOWEN: Objection, form.

6 THE WITNESS: Let's see. Yeah, the
7 vertical line?

8 BY MR. WILSON:

9 Q. Yes.

10 A. Okay.

11 Q. And you would agree that there is a
12 data line connected between each pair of
13 transistors in Figure 1.33; correct?

14 MR. BOWEN: Objection, form.

15 THE WITNESS: Well, the -- the data
16 line is connected to the two transistors
17 to the immediate left of the data line.

18 BY MR. WILSON:

19 Q. Right. And so -- and you see the --
20 the middle of Figure 1.33 where the transistors
21 are labeled A, B, C and D?

22 A. Yes.

1 Q. Okay. There is a data line connected
2 between transistors A and C, and a data line
3 connected between transistors B and D; correct?

4 A. Yes.

5 Q. Okay. Now, let's switch to
6 Figure 1.35 on the top of page 42 of the same
7 exhibit. Sorry, that's PDF page 52.

8 A. Yep.

9 Q. And I want to focus on the circuit
10 schematic shown in the top right of that
11 figure. Data line at the top, source at the
12 bottom.

13 Do you see that, Dr. Sechen?

14 A. Yeah.

15 Q. And here we have a circuit that has
16 10 transistors in it; correct?

17 A. Yes.

18 Q. And in that circuit the transistors
19 are all connected in series; correct?

20 A. Yeah, drain -- drain source series
21 array. That's a NAND flash structure, yes.

22 Q. Okay. We can put that exhibit away.

1 Let's turn to Johnson Exhibit 1010.

2 MR. WILSON: So, Henry, if you could
3 propagate that exhibit.

4 (Thereupon, Exhibit 1010 was marked for
5 identification.)

6 BY MR. WILSON:

7 Q. Now, Dr. Sechen, you've seen
8 Exhibit 1010 Johnson before; correct?

9 A. Yes.

10 Q. You studied this exhibit, you're
11 familiar with it; correct?

12 A. Right.

13 Q. All right. Let's look at Figure 10A.
14 Now, are the memory cells shown here in
15 Figure 10A, are they connected in series?

16 A. What are those memory cells? I
17 forgot. But I...

18 Q. So if you take a look, let's just --
19 let's just run through a quick refresher.
20 Let's look at Figure 4(a).

21 Okay. You can see Figure 4(a)
22 references a state change element 23 and a

1 steering element 22.

2 Do you recall that?

3 A. Yes.

4 Q. Okay. Now, if we go down to the
5 text, column 7, line 58, do you recall this
6 paragraph, "The steering element is a
7 semiconductor element" -- and it goes on to
8 describe it?

9 A. I do.

10 Q. Okay. So there -- some possible
11 implementations are listed there, you see that?

12 A. Could be a diode --

13 Q. Okay. Does that refresh your
14 recollection?

15 A. Yes.

16 Q. Okay. So let's go back to Figure
17 10A. Now, are the memory cells in Figure 10A
18 connected in series?

19 A. It would suggest that.

20 Q. Okay. There's a data line between
21 each pair of memory cells in Figure 10A;
22 correct?

1 A. Yeah. Those are the vertical lines,
2 yeah, bitlines. Yeah. After every pair,
3 right?

4 Q. Okay. But in your opinion, the
5 memory cells shown in Figure 10A are connected
6 in series; correct?

7 A. Yeah.

8 Q. Okay. Let's go back to Lee. And
9 let's look at Figure 25A.

10 Now, in Figure 25A, do you see the
11 conductor that's labeled M2 in between level 1
12 and level 2?

13 A. I do.

14 Q. Okay. Now, let's go back to
15 Figure 22. Figure 22 -- sorry, Figure 20A.
16 You can see that conductor when it's first laid
17 down here in Figure 20A that's labeled M2 is
18 also labeled 1336?

19 A. Yes.

20 Q. All right. Now let's take a look at
21 paragraph 157 in Lee. That's on PDF page 101.
22 And you can see there it says, "As shown in

1 Figures 20A and 20B, a second conductor layer
2 1336 is blanket deposited over and in contact
3 with the top source/drain region (N+
4 source/drain region 1316) as well as over and
5 on to ILD 1334."

6 Did I read that correctly?

7 A. Yes.

8 Q. It says -- it goes on to say, "The
9 second conductive layer 1336 will be used to
10 form a second input/output (for example, a
11 bitline or a wordline) for the first level of
12 memory devices and will be used to form a first
13 input/output (for example, a wordline or
14 bitline) for the second level of memory
15 devices." Correct?

16 A. Yes.

17 Q. Going back to Figure 25A. The M2
18 conductor in the middle in between the level 1
19 and level 2 transistors here, is a bitline or
20 wordline; correct?

21 MR. BOWEN: Objection, form.

22 THE WITNESS: Well, I mean using

1 conventional memory terminology, it would
2 be a bitline.

3 BY MR. WILSON:

4 Q. Okay. And Figure 25A is showing a
5 NOR configuration of memory cells; correct?

6 A. Yeah. That would be an implication
7 here, yes.

8 Q. Okay. Let's look take a look at
9 paragraph 107 of Lee. That's on PDF page 94.

10 Okay. And earlier you referred to
11 this paragraph. Do you recall that?

12 A. Yes.

13 Q. Okay. The first sentence of
14 paragraph 107 says, "One method of improving
15 device density is arrange the devices in a
16 monolithic three-dimensional array of charge
17 storage devices comprising the plurality of
18 device levels."

19 Did I read that correctly?

20 A. Yes.

21 Q. Okay. Lee goes on to define the term
22 "monolithic" in the next sentence; correct?

1 A. Yes.

2 Q. He says, "The term 'monolithic' means
3 that layers of each level of the array were
4 directly deposited on the layers of each
5 underlying level of the array." Correct?

6 A. Right.

7 Q. Now, Lee specifically states that
8 using monolithic three-dimensional arrays
9 improves device density; correct?

10 A. It says that that's one of the two
11 ways it identifies to improve device density.

12 Q. Now, the term "monolithic," as Lee
13 has defined it, would not include creating a
14 separate layer and attaching it to the top of a
15 wafer using the techniques of Aspar or Kim;
16 correct?

17 MR. BOWEN: Objection, form.

18 THE WITNESS: Well, this
19 paragraph points out that there's two ways
20 to improve device density. One is
21 monolithic and the other is
22 non-monolithic. And Lee is teaching both.

1 BY MR. WILSON:

2 Q. So you would agree that the
3 techniques of Aspar and Kim are non-monolithic
4 techniques; correct?

5 MR. BOWEN: Objection, form.

6 THE WITNESS: It -- it depends as to
7 how much of -- of a fabrication is
8 monolithic versus non-monolithic. You
9 know, you can have a -- a stackable add-on
10 layer comprised of some monolithic layers.
11 And then there's another stackable add-on
12 layer that's another set of monolithic
13 layers, but the two might be bonded
14 together and in a non-monolithic way.

15 So you really need to direct
16 attention to which layers are being
17 fabricated and whether they're monolithic
18 or not.

19 BY MR. WILSON:

20 Q. So let's look at paragraph 192 of
21 your declaration. Exhibit 1003.

22 A. Okay.

1 Q. Now, in paragraph 192 you assert that
2 in your opinion, "a person of ordinary skill in
3 the art would have looked to other art, such as
4 Kim, for details about attaching bottom level
5 3104 to insulating layer 3102." Correct?

6 A. Yes.

7 Q. And you say, "A person of ordinary
8 skill in the art looking to separately form
9 Lee's memory device and 'package [it] together'
10 with Lee's substrate 3105 having driver circuit
11 3103 formed therein and insulating layer 3102
12 on top 'to form a non-monolithic memory device'
13 would have looked to the teachings of Kim."
14 Correct?

15 A. Yes.

16 Q. So you characterize Kim's teachings
17 as forming a non-monolithic memory device;
18 correct?

19 A. Well, that's a bit over the top in
20 that, you know, it's non-monolithic because
21 you've got two pieces. You have the section
22 3101 and then you have the other section 3102,

1 3105, and those two pieces are non-monolithic,
2 but the individual pieces, 3101, may be
3 monolithic, and 3102, 3105 could be monolithic.

4 Q. Okay. So you would agree, then, as
5 well that Aspar, to the extent it involves
6 attaching a separate wafer, via wafer bonding,
7 is a non-monolithic process; correct?

8 A. Well, again, it depends just what
9 you -- if you say any portion of layer, a layer
10 or layers are non-monolithically bonded, then
11 the whole thing is non-monolithic. If you're
12 using that definition, then I would agree.

13 Q. Okay. I'm just saying to the extent
14 that Kim -- sorry. Let me strike that.

15 I'm just saying to the extent that
16 Aspar involves the use of attaching a separate
17 wafer via wafer bonding, to that extent Aspar's
18 Smart-Cut process is a non-monolithic process;
19 correct?

20 A. Well, bonding one wafer to another is
21 a non-monolithic processing step. And Aspar
22 may indeed use such a bonding step.

1 Q. Well, Aspar necessarily uses such a
2 bonding step; correct?

3 A. Yeah, it generally does comprise
4 bonding steps, yes.

5 Q. Let's go back to Johnson
6 Exhibit 1010. Let's look at Figure 6(b).

7 Now, Figure 6(b) shows layer 45 on
8 top of layer 46; correct?

9 A. Yes.

10 Q. Let's look at Johnson at column 13,
11 lines 26 through 35.

12 Okay. You can see there it says --
13 you can see toward the end of this paragraph
14 that it's referencing Figure 6(b).

15 Do you see that?

16 A. Yes.

17 Q. The figure we just looked at;
18 correct?

19 A. Yes.

20 Q. Now, the first sentence says, "The
21 processing may begin with a wafer." Correct?

22 A. Okay. "That may have received prior

1 processing steps." Yes.

2 Q. Okay. The next sentence begins with
3 the phrase, "An insulator then is deposited."

4 Do you see that?

5 A. Yes.

6 Q. Okay. Then in the third sentence it
7 says, "The first conductor layer is deposited
8 such as layer 46 of Figure 6(b) and then the
9 first layer stack 45 is deposited."

10 Did I read that correctly?

11 A. Yes.

12 Q. Then it says, "Figure 6(b) shows the
13 wafer at this stage." Correct?

14 A. Yes.

15 Q. So the layer 46 and the first layer
16 stack 45 are deposited after the insulator;
17 correct?

18 A. That's right, 46 is on top of the
19 insulator.

20 Q. Okay. Layers 46 and 45 are not
21 themselves insulators; correct?

22 A. Well, 46 for sure is not. 45 may

1 have some insulator intermediate step in
2 processing.

3 Q. Okay. Let's back up to column 12
4 line 1. You see where it says, "In this
5 embodiment, a pillar contains four layers of
6 material in a layer stack deposited
7 sequentially as shown in Figure 6(a)"?

8 A. Yes.

9 Q. Are any of those layers an insulator?

10 A. Well, number 3 is for sure.

11 Q. Okay.

12 A. And some portion of 41 to 43 as well.
13 Probably. Guessing 42 -- we should look at the
14 figure though to be sure.

15 Q. Okay. Let's look at Figure 6(a).

16 A. Yeah, so 402 is definitely a
17 insulator. I can say that for sure.

18 Q. Anything else?

19 A. Well, I forgot what it called 406 and
20 408, but -- so we may have to go back to the
21 text -- or if you can put that up as well, that
22 would work. Numbering system is different

1 there.

2 Q. Yeah. I think if you look at the
3 portion of Figure 6(a) that's in the upper
4 left, the numbering system will match.

5 A. Oh, okay. Yeah, could -- if we can
6 go to the upper left of the --

7 Q. There you go.

8 A. So 46 and 48 are conductors. Yeah.
9 So the only nonconducting layer is the SO --
10 SIO2 layer 42 or 420 or 402 depending on which
11 portion of that Figure 1 is looking at.

12 Q. Okay. All right. Let's take a
13 look -- let's go back to your declaration.
14 Paragraph 206.

15 MR. WILSON: Paragraph 206.

16 THE VIDEOGRAPHER: Sorry about that.

17 MR. WILSON: No worries.

18 BY MR. WILSON:

19 Q. Okay. Paragraph 206 of your
20 declaration you began discussion of the Aspar
21 Smart-Cut process; correct?

22 A. Yes.

1 Q. And you say it's shown there in Aspar
2 Figure 1; correct?

3 A. Yeah, the basic idea is -- is shown
4 there. Yes.

5 Q. Okay. And Figure 1 shows four steps
6 in the Smart-Cut process; correct?

7 A. Yeah. You could say that.

8 (Thereupon, Exhibit 1009 was marked for
9 identification.)

10 Q. Okay. Let's pull up Aspar, which is
11 Exhibit 1009. Those four steps are described
12 there on the first Page of Exhibit 1009, which
13 is Aspar; correct?

14 A. Yes. That's -- that's right.

15 Q. Okay. In the first step it says,
16 "Hydrogen is implanted in a substrate A. This
17 step induces formation of an in-depth weakened
18 layer."

19 Did I read that correctly?

20 A. Right. That would be the dashed line
21 in step one of that Figure 1.

22 Q. Okay. So Aspar teaches using

1 hydrogen implantation to drive the protons just
2 a little bit into the substrate A; correct?

3 MR. BOWEN: Objection, form.

4 THE WITNESS: Let's see. You
5 introduced the word "protons" and I'm not
6 100 percent sure that that is what I
7 recall, but it certainly -- you know,
8 certainly hydrogen.

9 BY MR. WILSON:

10 Q. Well, in particular it's -- it's H+;
11 correct? It's -- it's individual hydrogen
12 atoms or protons; correct?

13 MR. BOWEN: Objection, form.

14 THE WITNESS: Does -- does hydrogen
15 have a neutron? I want to think it does,
16 but any -- why don't we just stick with
17 hydrogen.

18 BY MR. WILSON

19 Q. Okay. Yeah, that's fine. Let's just
20 stick with hydrogen. Okay. So -- so let me --
21 strike that. I'll ask it again.

22 So Aspar taught using hydrogen

1 implantation to drive the hydrogen just a
2 little bit into the substrate A; correct?

3 MR. BOWEN: Objection, form.

4 THE WITNESS: Right. Into a certain
5 depth, that's -- it is -- yeah, it does
6 implant that at a certain depth, right.

7 BY MR. WILSON:

8 Q. Okay. And implanting the hydrogen
9 creates a weakened layer at the boundary
10 between the substrate A and the wafer A oxide
11 layer; correct?

12 A. No. It's inside -- it's past the
13 oxide layer and it -- I mean, there could even
14 be pattern circuitry in that silicon portion of
15 wafer A as well, but it's -- there's just this
16 implanted hydrogen at some depth that they can
17 control.

18 Q. Okay. So -- so there's a -- there's
19 a thin layer of -- of silicon, at the -- left
20 with the oxide; correct?

21 A. Yes.

22 Q. Okay. And the second step, substrate

1 A, is bonded to a support B by wafer bonding;
2 correct?

3 A. Yes.

4 Q. Okay. And then Aspar says, "A
5 splitting step, which takes place along the
6 in-depth weakened layer, gives rise to transfer
7 of a thin layer from the substrate A onto the
8 support B."

9 Did I read that correctly?

10 A. Yes.

11 Q. Okay. Now let's take a look at that
12 third step in Figure 1.

13 MR. WILSON: Which, Henry, it's just
14 the top of the next page.

15 BY MR. WILSON:

16 Q. Okay. There you can see the
17 splitting step; correct?

18 A. Yes.

19 Q. Okay. A layer of substrate A is
20 removed in the splitting step 3; correct?

21 A. Yeah. That's right. Typically a
22 thicker part is removed.

1 Q. Okay. And as shown in Figure 1,
2 after that third step, after the splitting
3 step, a thin layer of substrate remains above
4 the oxide layer; correct?

5 A. That's right. The -- you get a thin
6 silicon layer on top of the oxide.

7 Q. Okay. In step 4, back to the first
8 page, it says, "A final treatment can be
9 performed to remove the rough surface left
10 after splitting."

11 Did I read that correctly?

12 A. Yes.

13 Q. Okay. Now go back to Figure 1.

14 There in step 4 of Figure 1, after
15 this polishing step, thin substrate layer
16 remains above the oxide; correct?

17 A. Yes.

18 Q. Okay. And that's the thin top layer
19 shown there in Figure 4; correct? Or sorry
20 item 4 in Figure 1; correct?

21 A. Yes.

22 MR. WILSON: Now, let's take a look

1 at the first page of Aspar, back to the
2 first page. Okay. Second column. Yeah,
3 just below item 4 there. Where it says
4 "this process." Yeah.

5 BY MR. WILSON:

6 Q. Okay. So just after that first
7 sentence, you see where it starts "among
8 these"?

9 A. Right. Yes.

10 Q. So first it says -- Aspar says this
11 process has several advantages; correct?

12 A. Yes.

13 Q. And it says, "Among these, the
14 possibility of transferring thin layers of very
15 good thickness homogeneity and with a high
16 crystalline quality onto different materials
17 deserves to be highlighted."

18 Did I read that correctly?

19 A. Yes. And they do highlight
20 additional advantages on the last page. That's
21 right.

22 Q. Okay. So -- so one of the advantages

1 that Aspar references is the transfer of thin
2 layers of very good thickness homogeneity and
3 with a high crystalline quality; correct?

4 A. That's one of the advantages, yes.

5 Q. Okay. And that's referring to that
6 thin layer of silicon that we just looked at in
7 step four of Figure 1 at the top; correct?

8 A. That's one of the ways it -- Aspar
9 can be used, and -- and it does have that good
10 property.

11 Q. Okay. And this reference, Aspar,
12 Exhibit 1009, is describing transferring layers
13 of unpatterned silicon; correct?

14 MR. BOWEN: Objection, form.

15 THE WITNESS: No. It's certainly not
16 limited to that. It -- it discusses
17 other -- other approaches as well.

18 BY MR. WILSON:

19 Q. Okay. Let's -- let's look at the --
20 page 6 of Aspar. And I want to look at the
21 lower right. Sorry, I guess this is page 839,
22 depending on which set of page numbers you use.

1 Under "Conclusions," the last sentence of that
2 first paragraph you see there it says, "In this
3 paper, we focused essentially on homogenous
4 thin film transfer."

5 Did I read that correctly?

6 A. Yes.

7 Q. Homogenous thin film transfer is
8 unpatterned; correct?

9 A. Well, but the rest of the sentence
10 says that previous studies have shown that this
11 process is also compatible with patterned
12 layers and not just homogenous thin film
13 transfers, so one certainly shouldn't just look
14 at half of a sentence of teaching.

15 Q. Well, but I want to focus on what is
16 meant by the term "homogenous thin film
17 transfer." That is a reference to unpatterned
18 films; correct?

19 MR. BOWEN: Objection, form.

20 THE WITNESS: That portion of that
21 sentence likely does refer to that, yes.

22 (Thereupon, Exhibit 1016 was marked for

1 identification.)

2 BY MR. WILSON:

3 Q. Okay. Okay. Now I want to turn to
4 Exhibit 1016 for Fung.

5 And, Dr. Sechen, the reproduction
6 gear appears to have some little artifacts in a
7 the way it's showing up. I think it's fine, I
8 think you can still read it, I think it's still
9 legible, but -- but I will note that it does
10 seem to, you know, fill in some holes and some
11 letters for whatever reason.

12 But please let me know if for some
13 reason you can't discern the meaning of this
14 particular reference, Fung.

15 You've seen Exhibit 1016, Fung,
16 before; correct?

17 A. Yes.

18 Q. You've studied it and you're familiar
19 with it; correct?

20 A. Yes.

21 Q. Okay. I want to turn to column 4,
22 lines 30 through 33. There Fung says, "In

1 order to properly stack all the chips as
2 described, a precise alignment between all the
3 chips forming the stack is required to maintain
4 good mechanical and thermal integrity."

5 Did I read that correctly?

6 A. Yes.

7 Q. So when creating stackable chips,
8 alignment is a critical step; correct?

9 MR. BOWEN: Objection, form.

10 THE WITNESS: Well, that's -- you --
11 you certainly want to maintain good
12 alignment, that's -- that's true, and
13 that's standard practice.

14 BY MR. WILSON:

15 Q. Okay. Let's go back to column 1 and
16 let's start at line 42.

17 And, Dr. Sechen, feel free to read as
18 much or as little of this as you need to to
19 gain context here. I want to start at line --
20 I guess let's back up to line 40.

21 You see there it says, "Nowadays,
22 almost all lithographic processes use steppers.

1 The stepper only aligns and exposes one die at
2 a time."

3 Did I read that correctly?

4 A. Right.

5 Q. It goes on to say, "Thus, images in
6 different die areas do not aligned" -- which I
7 assume is a typo and -- and meant are not
8 aligned -- "as a result of which it is a common
9 occurrence that the two wafers end up
10 misaligned."

11 So did I read that correctly and do
12 you agree with my correction?

13 A. Yes.

14 Q. Okay. Now, Fung goes on to say, "To
15 solve this problem, the feature size of the
16 interconnect required for stacking needs to be
17 very large, which, in turn, degrades the
18 density and performance of the 3D-IC."

19 Did I read that correctly?

20 A. Yes.

21 Q. Okay. Now let's look at column 5, I
22 want to start at line 36. Actually, let's --

1 let's just look at the beginning of this
2 paragraph. It says, "The preferred method of
3 aligning a chip is by way of optical means."

4 Do you see that?

5 A. Yes.

6 MR. WILSON: We're in the wrong place
7 here. So this is like 528.

8 There we go.

9 BY MR. WILSON:

10 Q. So, Dr. Sechen, you see that first
11 sentence?

12 A. Yes.

13 Q. Okay. Now looking down at line 36,
14 thereabouts, you see the sentence that begins,
15 "If the number of feedthroughs"?

16 A. Yes.

17 Q. It says, "If the number of
18 feedthroughs between stacking chips is small
19 (for example, less than 1000), the alignment
20 accuracy remains at an acceptable level,
21 particularly since the joint structure is
22 typically quite large (for example, greater

1 than 10 microns)."

2 Did I read that correctly?

3 A. Yes.

4 Q. So according to Fung, the typical
5 joint structure to ensure proper alignment is
6 greater than 10 microns; correct?

7 MR. BOWEN: Objection, form.

8 THE WITNESS: Well, he's not
9 advocating the use of that, certainly.

10 BY MR. WILSON:

11 Q. But he says that's what's typical;
12 correct?

13 MR. BOWEN: Objection, form.

14 THE WITNESS: Well, he's teaching
15 something completely different than that.
16 So certainly this reference is not used
17 for such things as joint structures.

18 BY MR. WILSON:

19 Q. But that's what Fung says is typical
20 for alignment purposes; correct?

21 MR. BOWEN: Objection, form.

22 THE WITNESS: But it's not what he is

1 teaching or using.

2 BY MR. WILSON:

3 Q. Okay. I -- I don't think you're
4 answering my question. I think it's a pretty
5 straightforward question.

6 He says the -- the joint structure is
7 typically quite large, greater than 10 microns;
8 correct?

9 A. That's not what he is advocating the
10 use of.

11 Q. Okay. But he says that's what's
12 typical --

13 A. -- not use Fung's teaching, then
14 that's what you would encounter.

15 Q. Okay. Okay. Now, let's go back to
16 column 1, line 48.

17 So here Fung describes testing chips
18 to screen out defective ones before you stack
19 them; correct?

20 A. Yes.

21 Q. And he says, in -- so, sorry, let's
22 go down to line 52. Do you see where it says

1 "in as much"?

2 A. Yes.

3 Q. He says, "In as much as one or more
4 chips need to be aligned at any one time, the
5 alignment tolerance is significantly superior
6 than stacking wafers on top of one another."

7 Did I read that correctly?

8 A. Yes.

9 Q. He concludes with, "Hence, stacking
10 chips is definitely the preferred approach for
11 attaining 3D-IC."

12 Did I read that correctly?

13 A. Yes.

14 Q. So Fung advocates stacking chips as
15 opposed to wafers; correct?

16 MR. BOWEN: Objection, form.

17 THE WITNESS: Well, he's pointing out
18 that for certain types of chips and
19 technologies that stacking chips is --
20 results in a better yield, for example.

21 BY MR. WILSON:

22 Q. Thus, he recommends stacking chips as

1 the preferred approach for building 3D
2 integrated circuits; correct?

3 MR. BOWEN: Objection, form.

4 THE WITNESS: Bonding chips, for
5 example, in this manner, is -- my
6 experience is that when you see the term
7 "wafer bonding" it could be chip to chip,
8 it could be to chip to wafer, it could be
9 wafer to wafer, because in all cases,
10 you're plucking chips from a wafer in one
11 form or another and bonding them to
12 another chip that is plucked from a wafer,
13 so the persons of ordinary skill in the
14 art would understand that all those three
15 techniques are known as wafer bonding.

16 BY MR. WILSON:

17 Q. But Fung here is specifically
18 recommending stacking chips as opposed to
19 stacking wafers; correct?

20 MR. BOWEN: Objection, form.

21 THE WITNESS: When you have fully
22 formed or somewhat formed chips, that is

1 what Fung is recommending.

2 BY MR. WILSON:

3 Q. Okay. Let's take a look at your
4 declaration, paragraph 116.

5 MR. WILSON: Actually, so we've been
6 going for about an hour. If you guys are
7 ready to take a break, we can take a break
8 now or we can keep going. Up to you.

9 MR. BOWEN: Do you have a preference,
10 Dr. Sechen?

11 THE WITNESS: We can do it now.

12 MR. BOWEN: All right. Why don't we
13 take a break now. Thank you.

14 THE VIDEOGRAPHER: The time is
15 11:07 a.m. Going off the record.
16 (Thereupon, a brief recess was taken.)

17 THE VIDEOGRAPHER: The time is
18 11:18 a.m. We are back on the record.

19 BY MR. WILSON:

20 Q. Okay. Let's -- I think right before
21 the break we had already turned to
22 Exhibit 1003, your declaration. And I want to

1 look at paragraph 116.

2 A. Yes.

3 Q. Okay. In paragraph 116 you might
4 have to look at the top of the next page. You
5 show an annotated Figure 35 from Lee; correct?

6 A. Yes.

7 Q. Okay. So Lee disclosed an insulating
8 layer 3102.

9 Do you see that?

10 A. Yes.

11 Q. That's annotated in yellow in your
12 figure there?

13 A. Yes.

14 Q. And Lee also disclosed driver
15 circuits 3103, which you've annotated in green;
16 correct?

17 A. Yes.

18 Q. And Lee's Figure 35 shows the yellow
19 insulating layer disposed above the upper
20 surfaces of the driver circuits 3103; correct?

21 A. Yes.

22 Q. Now, in paragraph 118 you opine that

1 Lee disclosed "a dielectric layer disposed
2 above the electrical devices"; correct?

3 A. That's -- yeah. The first sentence
4 of 118 says that, yeah.

5 Q. Okay. And that's because Lee's
6 Figure 35 shows the yellow insulating layer
7 3102 disposed the upper -- above the upper
8 surfaces of the driver circuits 3103; correct?

9 A. Yeah, in 3105 in general that's
10 right.

11 Q. Okay. Now, let's look at
12 paragraph 103 of your declaration. Let's go
13 backwards a little bit. You see there in the
14 first sentence you say, "Lee additionally
15 discloses a method of integrating its pillar
16 memory device into 'a multilevel array of
17 storage cells,' i.e., array 3101 of Figure 35."

18 Did I read that correctly?

19 A. Yes.

20 Q. And you can see that you cite Lee
21 paragraph 147 there for that proposition;
22 correct?

1 A. Yes.

2 Q. Okay. Let's take a look at Lee,
3 Exhibit 1007, paragraph 147. And it's,
4 unfortunately, split on pages and columns here.
5 But do you see that it says, the first sentence
6 of paragraph 147 says, "A method of integrating
7 the pillar memory device of the present
8 invention into a multilevel array of storage
9 cells will now be described"?

10 A. Yes.

11 Q. Okay. And this is the passage that
12 you were referring to as an example of
13 integrating the pillar memory device into the
14 multilevel array of storage cells shown in
15 Figure 35; correct?

16 MR. BOWEN: Objection, form.

17 THE WITNESS: Yeah. That first
18 sentence of 103 in my report is in
19 reference to this paragraph 147, yes.

20 BY MR. WILSON:

21 Q. Okay. And then Lee from here starts
22 with Figure 13 and runs through Figure 28

1 describing a detailed example of how to
2 fabricate this device; correct?

3 A. Well, it talk -- it does talk about,
4 yeah, various options and how -- yes, how
5 certain potential fabrication steps could --
6 could be performed.

7 Q. Okay. Let's go back to paragraph 116
8 of your declaration. Okay.

9 MR. WILSON: Sorry. I'm at page 116.

10 THE VIDEOGRAPHER: You mean PDF 116
11 or --

12 MR. WILSON: Yeah. PDF 123,
13 page 116. Yeah. You're in the right
14 place. Okay.

15 MR. BOWEN: Paragraph 201, Doug?

16 MR. WILSON: I'm sorry?

17 MR. BOWEN: Paragraph 201?

18 MR. WILSON: Yes, you're right.

19 Really I'm looking at subsection E there,
20 ground 1E.

21 BY MR. WILSON:

22 Q. So, Dr. Sechen, beginning here on

1 page 116, you assert the obviousness of Claims
2 13 through 17 over Lee in view of Aspar;
3 correct?

4 A. Yes.

5 Q. And Aspar discloses the Smart-Cut
6 process; correct?

7 A. Yeah, var- -- all various aspects
8 associated with the Smart-Cut process, yes.

9 Q. Okay. If we fast-forward to
10 page 120, there at the bottom of paragraph 209
11 you show a figure representing your proposed
12 combination of Lee's Figure 9A with Figure 35;
13 correct?

14 A. Yes.

15 Q. Okay. In the transfer that you're
16 proposing here of Lee's Figure 9A, Figure 9A is
17 an unpatterned wafer; correct?

18 A. That's -- well, yeah, it's a
19 stackable add-on layer with three doped
20 regions.

21 Q. Okay. And in paragraph 211, the top
22 of the next page, you say, "After bonding, the

1 individual memory cells in level 3104 would be
2 fabricated from the transferred thin layer in
3 the same way they are fabricated in Lee."

4 Did I read that correctly?

5 A. Yes.

6 Q. So when this layer in Figure 9A is
7 transferred and attached to the substrate in
8 Figure 35, there are no memory devices in that
9 layer; correct?

10 MR. BOWEN: Objection, form.

11 THE WITNESS: What you -- yeah, what
12 you get is three pure single crystalline
13 layers, doped layers, N+ P- N+ and -- into
14 which you will form the devices for memory
15 cells.

16 BY MR. WILSON:

17 Q. Okay. Now, I want to look forward
18 just a bit, paragraph 213.

19 So in paragraph 213 -- sorry, I'll
20 wait. Yeah, there we go.

21 Beginning in paragraph 213 you're
22 describing why you believe a person of ordinary

1 skill in the art would have recognized benefits
2 in Aspar's Smart-Cut process; correct?

3 A. 213, 213 does talk about the benefits
4 of using Aspar's Smart-Cut process together
5 with Lee, for example.

6 Q. Okay. And toward the end of that
7 paragraph, the last sentence, I believe, begins
8 "in addition."

9 Do you see that?

10 It's on the top of page 123?

11 A. Yes.

12 Q. Okay. That sentence says, "In
13 addition, a POSITA would have recognized that
14 forming electrical devices on one substrate
15 separately from the memory devices on another
16 substrate would have allowed optimization of
17 the respective processes rather than forcing
18 the memory devices to be formed with a
19 suboptimal process tailored to preserving the
20 electrical devices formed on the single wafer
21 on the monolithic process."

22 Did I read that correctly?

1 A. Yes.

2 Q. So you talk about a suboptimal
3 process tailored to preserving the electrical
4 devices formed on the single wafer in the
5 monolithic process; correct?

6 A. There is that language.

7 Q. But you did not elaborate on what was
8 suboptimal about the monolithic process
9 regarding preserving the electrical devices,
10 did you?

11 A. Well, Aspar goes into great length as
12 to what that means, and I believe also Fung
13 does as well. You know, for example, you need
14 an extremely high frequency device and so you
15 couldn't use silicon for your substrate for the
16 logic circuitry and the processing, you would
17 need to use gallium arsenide or indium
18 phosphide, but -- but you would like to have
19 silicon memory devices because they're better
20 performing in terms of memory devices.

21 And so using Aspar allows you to
22 combine those two rather than forcing the

1 substrate to be using a suboptimal process for
2 it.

3 Q. So what are you concerned about in
4 the process, the monolithic formation process,
5 that might not preserve the electrical devices
6 formed on the single wafer?

7 MR. BOWEN: Objection, form.

8 THE WITNESS: The idea is, is that,
9 you know, you would like to use, for
10 example, single crystalline silicon for
11 forming your memory devices, but this --
12 silicon is not going to give you
13 acceptable electrical devices formed in
14 the substrate portion.

15 And so you don't want to have to live
16 with a suboptimal process. And so you'd
17 like to use, for example, gallium arsenide
18 or indium phosphite, whatever, to give you
19 appropriate performance you -- your --
20 your application demands. And -- and
21 Aspar enables that.

22

1 BY MR. WILSON:

2 Q. So -- so why can't you use single
3 crystal silicon memory devices in the
4 substrate?

5 A. In the substrate?

6 Q. Yes.

7 A. Well, then the whole chip is just
8 memory, there's no logic, there's no -- there's
9 no row decoders, there's no column decoders,
10 there's just memory cells that you can't access
11 or write to.

12 Q. So I -- I guess I'm not understanding
13 your concern here. So what -- what are you
14 concerned about? What would not preserve the
15 electrical devices formed on the single wafer
16 in the monolithic process?

17 A. Well, you also -- I mean, there's
18 various things that -- that you worry about
19 when you have lots of layers. Like, you know,
20 a later processing step can cause perturbations
21 of previous processing steps, so that's always
22 something you worry about so --

1 (Clarification by the reporter.)

2 THE WITNESS: Perturbations with
3 previously fabricated layers. And -- and
4 that's always a concern you have when
5 you're attempting to do a monolithic
6 design, that subsequent steps can perturb
7 earlier steps.

8 And by using a wafer bonding
9 approach, you can always reduce the
10 possibility of that happening, because the
11 processing of the upper layers is done on
12 a different substrate than what you're
13 going to ultimately put it on.

14 BY MR. WILSON:

15 Q. Okay. In -- in what ways can
16 subsequent processing steps perturb earlier
17 layers when doing monolithic processing?

18 A. It can be as simple as ions, for
19 example, passing through layers, it can be --
20 the heat can cause metal to deform possibly
21 creating opens or shorts. There's a number of
22 things that that can happen, so you would

1 prefer to -- to build the pieces and then you
2 can, of course, check the pieces, that they're
3 working before you bond them together which
4 helps your yield dramatically.

5 So and -- so that -- that's the basic
6 idea, but the -- another important thing that
7 Aspar points out on its last page is that you
8 would like to, in many applications, want to be
9 able to combine pure crystalline silicon for,
10 for example, memory devices with a different
11 type of technology for your logic circuitry.

12 Q. Okay. Earlier you referred to ions
13 moving due to subsequent processing steps.
14 What might cause ions to move in prior
15 circuitry?

16 MR. BOWEN: Objection, form.

17 THE WITNESS: Well, I mean, there are
18 ion implantation steps, for example,
19 but -- but certainly just the temperature
20 can give particles energy and they can
21 move. All these things can happen. So it
22 just -- this sentence particularly that's

1 highlighted is -- is really referring to
2 the advantages of having a different
3 process, fab process used for the
4 substrate versus the memory devices.

5 But -- but I've also been discussing
6 advantages of even if you're going to use
7 silicon for all of the processing that
8 subsequent fabrication steps can and do
9 perturb earlier fabrication steps.

10 BY MR. WILSON:

11 Q. So --

12 A. Now, the degree is not severe, but it
13 can happen.

14 Q. Okay. So have -- have you heard of
15 something called a thermal budget?

16 A. Yeah. There's things like that.

17 Q. Okay. So when you lay down an
18 original layer of electrical devices in a
19 substrate, they would be subject to a thermal
20 budget; correct?

21 A. Well, I think we should look into
22 some documentation on that to just see what all

1 the parameters are there. But, you know, how
2 do you know the -- the fab is going to
3 literally meet that for every chip on the
4 wafer?

5 But again, this sentence, by the way,
6 we're -- we're diverting from it, it shouldn't
7 be highlighted because we're not talking about
8 it. This is talking about two different types
9 of semiconductor materials being used for the
10 substrate versus the upper layers which are
11 memory cells for devices.

12 Q. Okay. Are you familiar with the
13 concept of a thermal budget in semiconducting
14 manufacturing?

15 A. I have heard of that, yes.

16 Q. Okay. And -- and you understand that
17 according to the concept of the thermal budget
18 that electrical devices, once they're created,
19 in a particular silicon layer are subject to a
20 thermal budget that if exceeded can cause, for
21 example, things like dope and ions to diffuse
22 into different areas rendering the device

1 potentially out of spec; correct?

2 MR. BOWEN: Objection, form.

3 THE WITNESS: That, you know,
4 certainly makes sense. It's consistent
5 with what I'm aware of.

6 BY MR. WILSON:

7 Q. Okay. You would agree that a person
8 of ordinary skill in the art in 2004 would have
9 been aware of a thermal budget as I've just
10 described it; correct?

11 A. Well --

12 MR. BOWEN: Objection, form.

13 THE WITNESS: -- what you're missing
14 here is the -- who enforces the -- the
15 budget. How do you guarantee that every
16 chip on the wafer has met that budget.
17 And that's a much more complicated problem
18 than just identifying a budget.

19 It's like you have a speed limit on a
20 highway, oh, 70. Well, how do you know
21 that everybody is going to stay under 70?

22

1 BY MR. WILSON:

2 Q. So I don't think you answered my
3 question.

4 You would agree that a person of
5 ordinary skill in the art, in 2004, would have
6 been aware of the thermal budget as I just
7 described it; correct?

8 MR. BOWEN: Objection, form.

9 THE WITNESS: Well, I don't see how
10 that solves any issues, because the
11 enforcement of the thermal budget is the
12 critical part, which is not being
13 discussed.

14 BY MR. WILSON:

15 Q. Okay. I'm going to object to your
16 answer as nonresponsive and move to strike it.

17 Whether it resolves any problems or
18 not is beyond the scope of my question. My
19 question is simply whether a person of ordinary
20 skill in the art, in 2004, would have been
21 aware of the concept of thermal budget as I
22 just described it?

1 A. But that budget describes if you
2 violate it, what happens and ions escape from
3 diffusions and so forth and cause problems.
4 And that's exactly what I'm saying, that --
5 that potential source of error is removed by
6 wafer bonding.

7 Q. So would adherence to the thermal
8 budget have been a reason that a person of
9 ordinary skill in the art, in 2004, would have
10 been motivated to use wafer bonding?

11 A. Yes, I believe so.

12 Q. Okay. And that's because a person of
13 ordinary skill in the art, in 2004, would have
14 been aware of the thermal budget issue as I
15 described it; correct?

16 A. Certainly POSITAs would have been
17 aware of, yeah, temperatures at which metal
18 might start to migrate forming opens or shorts,
19 or -- or at which ions may diffuse where you
20 don't want them to go.

21 They would certainly be aware of such
22 temperatures and the need to stay -- try to

1 stay below those temperatures. But all you can
2 do is try. You can't literally guarantee it
3 for every chip on the wafer.

4 Q. Okay. Let's look at paragraph 241 of
5 your declaration.

6 Okay. And I believe we referred to
7 this paragraph a little bit earlier from
8 Johnson. This is -- in paragraph 241 you quote
9 Johnson column 7, line 61 to column 8, line 5;
10 correct?

11 A. Yes.

12 Q. Okay. And here you specifically
13 emphasize item (iii) in that quote, which is "a
14 junction field-effect transistor with gate
15 connected to source (or to drain)." Correct?

16 A. Yes.

17 Q. And you also emphasize item (iv),
18 which is "a MOSFET," M-O-S-F-E-T, "with gate
19 either floating or connected to source or
20 connected to drain." Correct?

21 A. Yes.

22 Q. Now, Johnson does not disclose how to

1 make either of those examples; correct?

2 MR. BOWEN: Objection, form.

3 THE WITNESS: I -- I would not

4 have -- understand how you would come up

5 with that conclusion because this is text

6 from Johnson, no?

7 BY MR. WILSON:

8 Q. Yes. This is a quote from Johnson.

9 My question is whether Johnson shows how you

10 would make either one of these examples?

11 A. Well --

12 MR. BOWEN: Objection, form.

13 THE WITNESS: -- a -- a POSITA knows

14 how to make diodes out of transistors.

15 And Johnson does. Clearly he mentions the

16 obvious approaches.

17 BY MR. WILSON:

18 Q. Okay. So aside from the mentions

19 here in this passage that you quoted, Johnson

20 does not disclose how to make example (iii) or

21 example (iv) in this quote; correct?

22 MR. BOWEN: Objection, form.

1 THE WITNESS: Well, I totally
2 disagree with that, because a POSITA knows
3 how to do it and Johnson knows how to do
4 it as well.

5 BY MR. WILSON:

6 Q. Okay. But Johnson doesn't disclose
7 anything with respect to the item (iii) or
8 item (iv) embodiment, other than the language
9 here on this page; correct?

10 MR. BOWEN: Objection, form.

11 THE WITNESS: Because that's common
12 knowledge to a POSITA.

13 BY MR. WILSON:

14 Q. Okay. Now, let's look at
15 paragraph 247 of your declaration.

16 Now, here you're describing applying
17 Kim's teachings to Johnson; correct?

18 A. Yes.

19 Q. And here you show a combination
20 involving Johnson's memory arrays built on a
21 substrate blue being combined with Johnson's
22 peripheral circuitry built in the substrate at

1 wafer B; correct?

2 A. That's right.

3 Q. Okay. And in your opinion, you're
4 making this combination based on the teachings
5 of Kim; correct?

6 A. That's true, yes.

7 Q. Now, in the wafer A that you show
8 here, you have two layers of Johnson's memory
9 cells built on the blue substrate; correct?

10 A. Yes.

11 Q. Now, in your opinion, would Kim teach
12 that you could again add additional layers of
13 blue substrate and additional layers of
14 Johnson's memory cells?

15 MR. BOWEN: Objection, form.

16 THE WITNESS: Let's see. I don't see
17 why that -- that couldn't be done.

18 BY MR. WILSON:

19 Q. Okay. But you didn't describe such
20 an embodiment or how a person of ordinary skill
21 in the art would go about doing that; correct?

22 MR. BOWEN: Objection, form.

1 THE WITNESS: Well, I mean, you --
2 you can certainly see that from Aspar.
3 There's other -- yeah. Any of those --
4 either of those would teach that. I mean,
5 you basically would identify a wafer B as
6 your -- your new stack, B plus A, and do
7 the process again.

8 BY MR. WILSON:

9 Q. Okay. You just referred to Aspar,
10 but I think you meant Kim; correct?

11 A. No. I said that Aspar also teaches
12 repeated applications of bonding, and to the
13 extent that Kim doesn't completely illustrate
14 that.

15 Q. Okay. So you meant to refer to Aspar
16 there?

17 A. Yes.

18 Q. Okay. All right. Now, let's look at
19 paragraph 250 of your declaration.

20 MR. WILSON: I want to look at the
21 passage that kind of spans the page break
22 there. Yeah. There we go.

1 BY MR. WILSON:

2 Q. There you say that a person of
3 ordinary skill in the art would -- would be
4 able to test the memory cells that are built on
5 the blue substrate before bonding them to wafer
6 B; correct?

7 A. Yes.

8 Q. Okay. And you specifically point
9 out, for example, testing for shorts; correct?

10 A. Let's see. I think testing in
11 general, you know, you could test for
12 functionality.

13 Q. Right. But the specific example you
14 provide is testing --

15 A. Yeah. All right. I see, yeah.
16 Right. That's one example, yes.

17 Q. Okay. What kind of shorts are you
18 referring to here?

19 A. Well, in -- in general, you could
20 test for any number of things. One example is
21 shorts, but there's what's called stuck at
22 testing, stuck at zero, stuck at one. There's

1 also just simple testing of memory cells, you
2 know, can -- can you write a one -- for
3 example, can you write a zero, can you read the
4 corresponding value. There's different things
5 you can do to test.

6 Q. Okay. But I want to focus on your
7 example that you provided, which is testing for
8 shorts. What specific types of shorts can you
9 test for?

10 A. Certainly whether two transistors are
11 shorted together that aren't intended to. And,
12 let's see, this is -- yeah, Johnson's device.
13 So, for example, if between two conductors like
14 that steering device and the -- the other
15 one -- I forgot the name of it. Let's see if I
16 can come up with that.

17 Yeah. The steering element and the
18 state charge element, if they're -- if there's
19 a short there, or if you can't switch the state
20 of it due to a short in the steering element or
21 the state charge element, either one of them,
22 those -- those are examples of tests you would

1 do.

2 Q. So like, for example, looking back at
3 your example figure, and I don't know whether
4 this is big enough for you to read or not. In
5 paragraph 247, you might test, for example, for
6 a short between the conductors 50A and 52A.
7 You can see those in that middle figure there.

8 You see those?

9 A. Let's see. I guess we could look on
10 the right because they're not upside down.

11 Q. Sure. Yeah. You see the two
12 conductors, 50A and 52A?

13 A. Yes. Right. And there should be --
14 yeah. Certain memory devices between there and
15 you could, yeah, see if those two layers are --
16 are shorted, because, you know, the etch.
17 It's -- like, for example, if it's -- if
18 they're not supposed to be conducting, you
19 could -- obviously if there's a short there's a
20 problem.

21 Q. Okay. But Johnson doesn't disclose
22 any access point for use for testing for

1 shorts, does it?

2 MR. BOWEN: Objection, form.

3 THE WITNESS: Well, a POSITA would
4 know that -- when you're fabricating
5 structures that you want to be able to do
6 a wafer test on -- you just don't want to
7 bond something on to another wafer without
8 knowing that -- that that's working.

9 And -- and that -- that testing,
10 wafer testing, is always done. Even if
11 you're not bonding anything, you're still
12 going to test whether that -- that chip is
13 working so that you don't bother to
14 package it and so forth.

15 And so since you're going to do that
16 test anyway, why not do it for both chips
17 that you're going to bond together.

18 BY MR. WILSON:

19 Q. Okay. So you're saying that the --
20 the device that Johnson's describes would
21 already have this test functionality built into
22 the -- the chip?

1 MR. BOWEN: Objection, form.

2 THE WITNESS: Basically that's
3 correct. Yes. You would want means to
4 test it.

5 BY MR. WILSON:

6 Q. Okay. So if you were to find a short
7 between conductor 52A and 50A, for example, in
8 one memory array of one die in a wafer on the
9 blue substrate, what would you do?

10 A. Well, you have various options.
11 In -- in most cases as -- as Fung teaches, for
12 example, when you're talking wafer bonding it's
13 chip to chip, you know, you're plucking chips
14 off wafers, gluing -- gluing them together,
15 bonding them.

16 And so if -- if you would only bond
17 known working die in -- another thing you could
18 do is if you insist on bonding a whole wafer to
19 another whole wafer, because in some sense if
20 you do that willy-nilly without analyzing
21 functionality, you could get a very -- a very
22 low yield. It will be essentially the product

1 of the individual yields and depending -- and
2 then depending how many wafers you -- you bond
3 together, that product gets lower and lower.
4 So --

5 Now, you could do some sort of
6 analysis and only bond a wafer that has good
7 dies in certain locations that are similar to
8 good dies on the other wafer, but as -- but as
9 Fung explains, it's best to bond known good die
10 from one wafer to a -- to the known good die on
11 another wafer.

12 Q. So if -- if there's a -- a number of
13 shorts or a pervasive short across a wafer you
14 might discard the whole wafer; correct?

15 A. You see, that's very unlikely to ever
16 happen because the chips are individualized.
17 So in other words, it's -- in -- in most
18 applications -- there are exceptions, like with
19 some Internet of Things or other things using
20 older processes where certain sensor
21 applications where you're -- the part you're
22 selling is from an entire wafer.

1 In that case, if there's error, yeah,
2 you have to throw away the wafer. But if you
3 think of a processor with memory, for example,
4 you surely don't want to throw away a whole
5 wafer because it has a bad die.

6 So what your -- and -- and the memory
7 chips are -- the memory for one processor that
8 you would bond to -- that memory to a processor
9 chip, that is isolated on the wafer. It's --
10 it's unlikely to -- an error in it is -- well,
11 will not impact another chip, another memory
12 chip, because they're dielectrically isolated
13 --

14 Q. Okay. Is it your understanding that
15 in a typical chip fabrication process each
16 deposited layer is visually or electrically
17 tested for massive defects or out of spec
18 processing?

19 MR. BOWEN: Objection, form.

20 THE WITNESS: I -- I would say -- I
21 don't believe that they test -- again, it
22 depends which fab line you're talking

1 about and what products they're producing,
2 but, you know, if it's microprocessors,
3 it's likely that they pay very close
4 attention early in the development of a
5 processor and a fab.

6 And then as the yield goes up and up,
7 at some point their testing may be just
8 one portion of the wafer, for each layer,
9 possibly. And knowing that if that's
10 correct, it's very likely correct
11 everywhere. But the -- but the real test
12 is once you're done processing the wafer,
13 does that portion of the -- does an
14 individual chip work and is it worthy of
15 being bonded to, for example, a memory.

16 BY MR. WILSON:

17 Q. So the -- the processing that I just
18 described, which occurs in -- in -- you agree
19 it occurs in some chip fabrication facilities
20 would likely catch the shorts you're looking
21 for in this passage of your declaration;
22 correct?

1 MR. BOWEN: Objection, form.

2 THE WITNESS: I think it would be
3 reasonable to finish processing the memory
4 portion and then you would have your
5 requisite -- most likely have your
6 requisite inputs and outputs for testing
7 also created, and then you could test that
8 memory portion for shorts or opens or
9 whatever stuck out.

10 BY MR. WILSON:

11 Q. Okay. So you think whatever gets by
12 that sort of routine testing in a chip fab
13 would motivate a person of ordinary skill in
14 the art to adopt the approach of not using
15 standard photolithography, but to build the
16 wafer in two parts and then try to bond them
17 together?

18 MR. BOWEN: Objection, form.

19 THE WITNESS: Oh, that's a long one.
20 I -- I think in many cases the wafer
21 bonding approach is superior, you know,
22 both for yield and -- well, particularly

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1 for yield and, therefore, cost. And --
2 but again, it depends, on to some extent,
3 whose -- whose fab are you talking and,
4 you know --

5 (Clarification by the reporter.)

6 THE WITNESS: Whose fab or -- which
7 is -- F-A-B, which is short of fabrication
8 well, fabrication line or fabrication --
9 what should we say? It -- it's basically
10 a fabrication -- I'm not sure what term
11 they use -- like it -- it -- because it
12 involves a company that has equipment that
13 produces chips. And that's -- and the
14 process is called fabrication and so they
15 refer to it as a fab these days.

16 BY MR. WILSON:

17 Q. Okay. Let's look at paragraph 46 of
18 your declaration.

19 A. 46?

20 Q. Yes.

21 MR. WILSON: Yeah. Yeah. There you
22 go.

1 BY MR. WILSON:

2 Q. Okay. Do you have that, Dr. Sechen?

3 A. Yes.

4 Q. Okay. Here you describe the
5 Smart-Cut process by reference to Exhibit 1015
6 and specifically Figure 1124; correct?

7 A. Yes.

8 (Thereupon, Exhibit 1015 was marked for
9 identification.)

10 Q. Okay. So let's pull up Exhibit 1015.
11 And you've seen Exhibit 1015 before;
12 correct?

13 A. Yes.

14 Q. All right. So I want to go
15 specifically to page 60. Actually -- so --
16 yeah. Page 61, actually, which I believe is
17 where that figure actually comes from.

18 A. Yeah. This figure is entirely
19 consistent, if not outright the same as
20 Aspar's.

21 Q. Okay. So Exhibit 1015 is here
22 describing the same process you're referencing

1 in Aspar; correct?

2 A. Yes.

3 Q. Okay. So let's go down to the top of
4 the next page, the text there. And I'm just
5 going to kind of summarize here that this top
6 paragraph describes the process, first bonding,
7 then second annealing to grow the cut, and then
8 third delamination.

9 Do you see that?

10 A. Yes.

11 Q. Okay. Now, I want to start -- you
12 see where it refers to both wafers, after
13 describing the delamination? Middle of the
14 paragraph.

15 A. Yes.

16 Q. Wafers.

17 So it says, "Both wafers are then
18 annealed at 1100 degrees Celsius to remove
19 defects."

20 You see that?

21 A. Yes.

22 Q. What defects is it describing here?

1 A. Well, it would be along the cut
2 basically.

3 Q. So the defects that are being
4 described here are due to the hydrogen
5 implantation; correct?

6 MR. BOWEN: Objection, form.

7 THE WITNESS: Well, that and -- and
8 the delamination process in general.

9 BY MR. WILSON:

10 Q. Okay. And the annealing step here is
11 a step to repair the silicon due to the
12 hydrogen implantation; correct?

13 MR. BOWEN: Objection, form.

14 THE WITNESS: Well, due to the
15 delamination the -- the wafers, according
16 to this author or article, suggests that
17 that should be annealed.

18 Q. Okay. And it specifically suggests
19 that it should be annealed at 1100-degree
20 Celsius to correct those defects; correct?

21 A. That is this one article's opinion,
22 yes.

1 Q. Okay. And then Figure 1124 up there
2 shows -- it's step six on the previous page --
3 the annealing at 1100 degrees C; correct?

4 MR. WILSON: Henry, can we turn back
5 to the previous page of that figure.

6 THE WITNESS: Okay.

7 BY MR. WILSON:

8 Q. So Figure 1124, which you put in your
9 declaration shows that annealing step at
10 1100 degrees Celsius; correct?

11 A. Yes.

12 Q. Now, let's look at -- let's go back
13 to paragraph 247 of your declaration. So back
14 to the Johnson/Kim embodiment. So the figure
15 that you've applied here, you -- you say it's
16 Johnson's Figure 6(e), but I believe it is
17 Johnson's Figure 6(g). We can look at Johnson
18 and confirm that.

19 A. Okay.

20 MR. WILSON: So can we pull up
21 Johnson Figure 6(g). Well, first let's
22 look at Figure 6(e).

1 BY MR. WILSON:

2 Q. Okay. You would agree that's not the
3 figure you used; correct?

4 A. Yeah, that's correct. Sorry.

5 Q. Okay. So let's look at Figure 6(g).
6 This is in fact, the figure you used;
7 correct?

8 A. Yes.

9 Q. Okay. So back to your declaration
10 and that paragraph 247. And if we can, let's
11 blow this up a little bit. Maybe best seen on
12 the right, the figure on the right, yeah. So
13 you can see the vertical strips there. You see
14 53B is labeled, and the actual Figure 53A is
15 labeled as well but it's been blocked out by
16 the blue substrate here.

17 Do you see that? Do you see strips
18 53A and 53B?

19 A. 53B, yes. I don't know what happened
20 to 53A.

21 Q. Yeah. We can go back to Johnson
22 Figure 6(g) so you can see where 53A is

1 labeled.

2 You see it up there at the top?

3 A. In which case I see it.

4 Q. Okay. So these layers 53A and 53B,
5 you see them in your proposed combination;
6 correct?

7 A. Yes.

8 Q. What purpose do those serve in the
9 combination?

10 MR. BOWEN: Objection, form.

11 THE WITNESS: Let's go back to
12 Johnson. I should have a copy that;
13 right?

14 BY MR. WILSON:

15 Q. Yeah, you should.

16 A. This is slow. I don't have a paper
17 copy of this. I mean, it's definitely a --
18 could be another layer in the memory or it
19 could function as the substrate, too, for
20 purposes of bonding, you know, something that
21 would be cleaved off.

22 Q. So as it -- as it stands in your

1 proposed figure, those are unpatterned memory
2 cells; correct?

3 A. Right.

4 Q. Okay. Let's take a look at
5 paragraph 173 of your declaration.

6 Okay. And I want to look at the
7 figures from Endoh that you got here, 1171 and
8 1172 that you labeled.

9 You see those?

10 A. Yes.

11 Q. Okay. You annotated versions of
12 Endoh's Figures 1171 and 1172; correct?

13 A. Yes.

14 Q. So you're familiar with these
15 examples; correct?

16 A. Yes.

17 Q. Are these figures showing a NAND
18 memory configuration?

19 A. Yes.

20 Q. I don't have any further questions.

21 Well, actually, I do have one further question.

22 Dr. Sechen, during the course of your

1 deposition today, have you spoken to anyone
2 about the substance of your testimony or
3 prospective testimony?

4 A. No.

5 MR. WILSON: No further questions.

6 MR. BOWEN: So we have some food here
7 that we'd like to eat for lunch and come
8 back. Would that work?

9 MR. WILSON: That's fine with me,
10 yeah.

11 MR. BOWEN: Dr. Sechen, how long
12 would you like?

13 THE VIDEOGRAPHER: Can I -- can I get
14 us off the record first; is that okay?

15 MR. WILSON: Yeah, sure. Go ahead.

16 THE VIDEOGRAPHER: The time is
17 12:15 p.m. Going off the record.

18 (Thereupon, a lunch recess was taken.)

19 THE VIDEOGRAPHER: Time is 1:24 p.m.
20 Back on record.

21 MR. BOWEN: I have no questions for
22 the witness.

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1 MR. WILSON: Nothing further from us.

2 THE VIDEOGRAPHER: Okay. Stand by.

3 This marks the end of today's deposition.

4 The time is 12:46 p.m.

5 (Time Noted: 12:46 p.m.)

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I, the undersigned authority, hereby
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I further certify that I am not of
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IN WITNESS WHEREOF I hereunto set my
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