

Novel Ultrahigh-Density Flash Memory With a Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell

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Abstract—In order to overcome the limitation of cell area of $4F^2$ per bit in conventional NAND Flash memory cells, stacked-surrounding gate transistor (S-SGT) structured cell is proposed. This newly structured cell achieves a cell area of $4F^2/N$ per bit, where N is the number of stacked memory cells in one silicon pillar, without using multibit per memory cell technology. The S-SGT structured cell consisting of two stacked memory cells in one silicon pillar achieves a cell area per bit of less than 50% of the smallest reported NAND structured cell. The novel S-SGT structured cells are fabricated by vertical self-aligned processes using a $0.2\text{ }\mu\text{m}$ design rule. The S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of Fowler–Nordheim (F–N) tunneling electrons over the whole channel area of the memory cell, respectively, which is the same program and erase mechanism as in conventional NAND structured cell. This high performance S-SGT structured cell is applicable to high-density non-volatile memories for 16 G/64 G bit Flash memories and beyond.

Index Terms—Flash memory, SGT, S-SGT, 3-D device.

I. INTRODUCTION

WITH the development of ULSI technologies, bit density of nonvolatile memories, especially Flash memory, is undergoing revolutionary growth. Recently, high-density Flash memories realizing high-speed programming and low-power consumption are attracting much interest as mass storage media in portable computers and battery-powered systems. In these applications, Flash memories are used to store personal data. Offering high-speed programming and low-power consumption, bipolarity program and erase operation [1] is well suited for these portable applications [2]. Also, the amount of data to be stored is on an upward trend.

To realize over Gigabit density memories for the above applications, current Flash memories have been simply shrunk by introducing self-aligned floating gate structure, self-aligned STI structure, and scaled dielectrics. However, current Flash memory cell units are now beginning to reach its limitations in scaling, because it is hard to reduce memory cell area

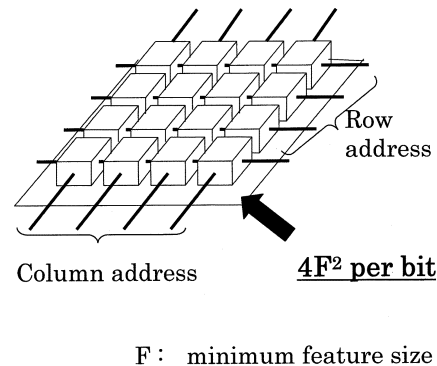


Fig. 1. Conventional 2-D cell array.

per bit itself, spacing between neighboring memory cells, spacing between gate electrode and drain contact hole, contact hole size, and source line. Therefore, NAND structured Flash memories were proposed [3], [4]. By using NAND structured Flash memory technology, a high-density Flash memory with a cell size of $4.4F^2$ (F : feature size) was reported [5]. However, further scaling of Flash memory cells in planar technology is becoming increasingly difficult because of concerns relating to punch through, reliability, process windows, read current, and isolation requirements between neighboring cells. To overcome above scaling issues in planar technology, a three-dimensional (3-D) structured Flash memory cell, 3-D Programmable Erasable Nonvolatile Cylindrical (PENCIL) Flash EPROM cell [6] and a Floating Channel type Surrounding Gate Transistor (FC-SGT) Flash memory were proposed [7], [8].

However, conventional Flash memory is based on a two-dimensional (2-D) memory array architecture as shown in Fig. 1. This 2-D memory array architecture does not use 3-D space efficiency. Moreover, these conventional Flash memories have a cell area limitation of $4F^2$ per bit, where F is a minimum feature size.

In this paper, stacked-surrounding gate transistor (S-SGT) structured cell [9] is proposed, in order to overcome the limitation of cell area of $4F^2$ per bit in conventional NAND Flash memory cells. The S-SGT structured cell will be able to use to a newly 3-D memory array architecture. Fig. 2 schematically shows an example of the 3-D memory Array Architecture.

In Section II, the concept of the S-SGT structured Flash memory and its structure is described. Moreover, it is shown

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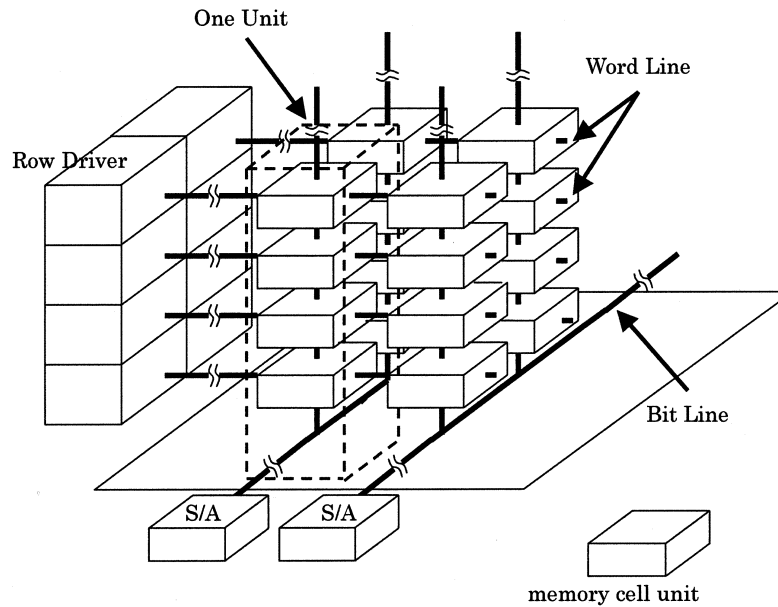


Fig. 2. New 3-D memory array architecture.

that the S-SGT structured cell consisting of two stacked memory cells in one silicon pillar as described in this paper achieves a cell area per bit of less than 50% of the smallest reported NAND structured cell [5]. In Section III, the fabrication process of the S-SGT structured Flash memory is outlined. Especially, vertical self-aligned process is explained. It is shown that the novel S-SGT structured cells can be fabricated by vertical self-aligned processes using a $0.2\text{-}\mu\text{m}$ design rule. In Section IV, measured results of the fabricated S-SGT structured Flash memory cell are explained. It is shown that the S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of Fowler–Nordheim (F–N) tunneling electrons over the whole channel area of the memory cell, respectively, which is the same program and erase mechanism as in conventional NAND structured Flash memory cells. Finally, in Section V, conclusions are given.

II. CONCEPT OF S-SGT STRUCTURED FLASH MEMORY

A. Cell Structure

The structure of the proposed S-SGT structured Flash memory cell arranges bit line contact, first select gate, two SGT type memory cells, second select gate and source line in series vertically in one silicon pillar, as shown in Fig. 3. Fig. 3(a) shows bird's view of S-SGT structured cell. Fig. 3(b) and (c) shows cross-sectional view along (B1)–(B2) and cross-sectional view along (C1)–(C2) of S-SGT structured cell, respectively. The SGT type memory cell is structured that floating gate and control gate surround the silicon pillar [7] and gates, source, and drain are arranged on a silicon pillar vertically. All devices for the proposed cell are vertically stacked in one silicon pillar. Therefore, the S-SGT structured cell does not need additional area such as bit line contacts, the

two select gates and the source line, while conventional NAND structured cell needs this additional area [3].

The newly structured cell achieves a cell area of $4F^2/N$ per bit, where N is the number of stacked memory cells in one silicon pillar, without using multibit per memory cell technology. The S-SGT structured cell consisting of two stacked memory cells occupies only an area of $4F^2$ and achieves a cell area of $2F^2$ per bit as shown in Fig. 3(c). In comparison, conventional NAND structured cell requires a cell area of $8F^2$ per bit as shown in Fig. 3(d). As shown in Fig. 3(e), the equivalent circuit of S-SGT structured cell is the same as that of a conventional NAND structured cell.

B. Occupied Cell Area per Bit

The occupied area per bit of the S-SGT structured Flash memory cell is discussed. Fig. 4 shows the occupied area per bit of the S-SGT structured Flash memory cell in comparison with the smallest reported NAND structured cell. X -axis is the number (N) of stacked memory cells in one silicon pillar. Y -axis is ratio of occupied area per bit as a function of the number (N) of stacked memory cells in one silicon pillar in comparison with the smallest reported cell area per bit of conventional NAND structured cell. As the number (N) of stacked memory cells in one silicon pillar increases, the S-SGT structured cell can reduce to cell area per bit in proportion to $1/N$. As a result, the S-SGT structured cell can realize a drastically smaller cell area per bit than the smallest reported NAND structured cell.

According to Fig. 4, the S-SGT structured cell consisting of two stacked memory cells in one silicon pillar described in this paper achieves a cell area per bit of less than 45% of the smallest reported NAND structured cell. Moreover, a S-SGT structured cell consisting of four stacked memory cells in one silicon pillar

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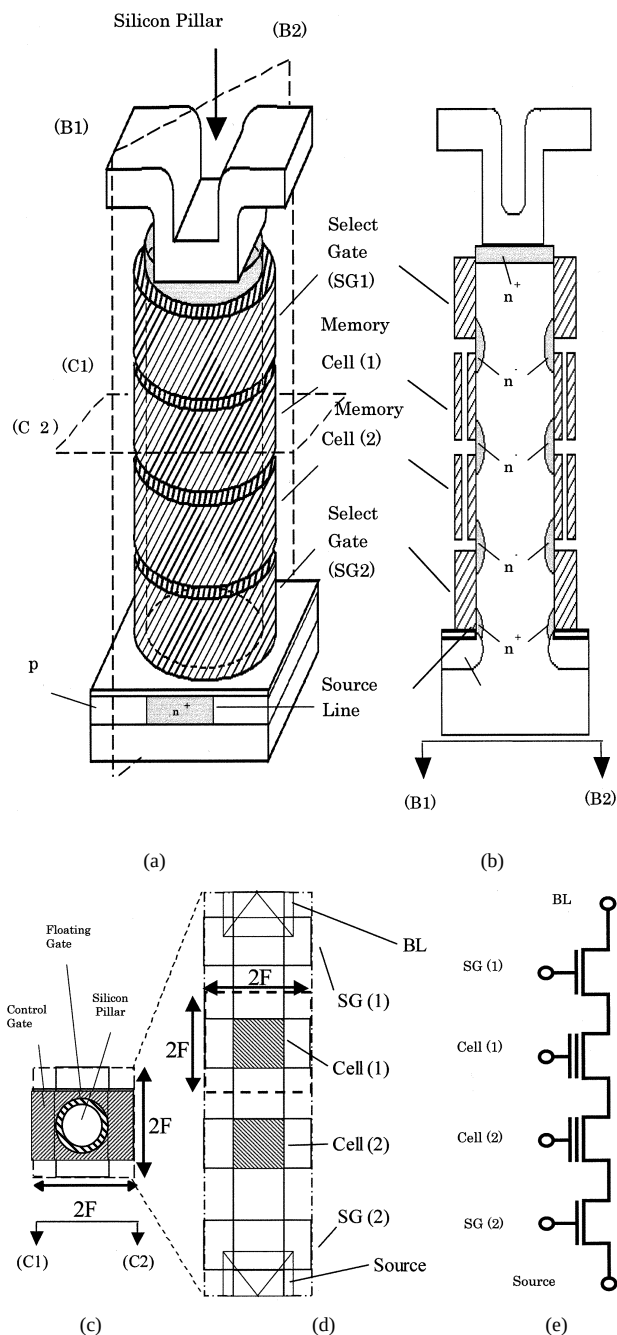


Fig. 3. Concept of S-SGT structured cell. (a) Bird's view of S-SGT structured cell. (b) Cross-sectional view along (B1)–(B2) of S-SGT structured cell. (c) Cross-sectional view along (C1)–(C2) of S-SGT structured cell. (d) Top view of NAND structured cell. (e) Equivalent circuit of S-SGT structured cell and NAND structured cell.

achieves a cell area per bit of less than 22% of the smallest reported NAND structured cell.

From above all, the S-SGT structured Flash memory drastically reduces cell area per bit without using multibit per memory cell technology, and can overcome the limitation of cell area of $4F^2$ per bit in conventional Flash memory.

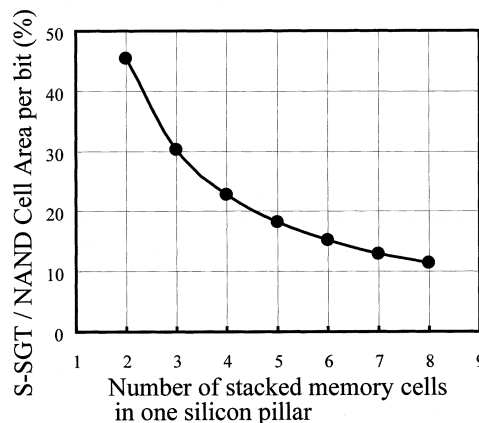


Fig. 4. Ratio of occupied area per bit as function of number of stacked memory cells in one silicon pillar in comparison with the smallest reported cell area per bit of conventional NAND structured cell.

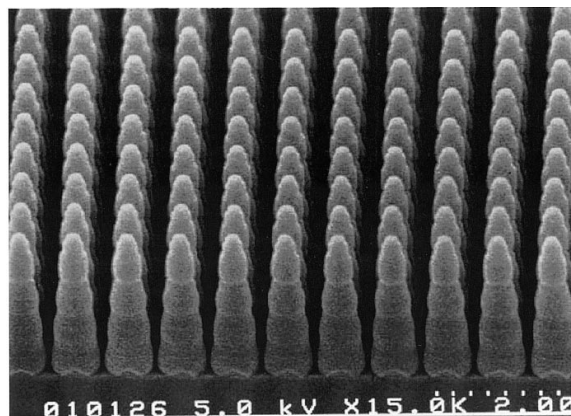


Fig. 5. SEM photograph of S-SGT structured cell.

III. FABRICATION PROCESS

The S-SGT structured cell consisting of two stacked memory cells is fabricated using a $0.2 \mu\text{m}$ process as shown in Fig. 3. A first select gate transistor, two SGT type memory cells, and a second select transistor are fabricated in series vertically in one silicon pillar.

The SEM photograph of the S-SGT structured cell is shown in Fig. 5 and the fabrication sequence for the proposed cell is shown in Fig. 6(a)–(e). The fabrication sequence for the proposed cell is explained as follows. A sidewall mask is formed after first silicon etching as shown in Fig. 6(a). By this first silicon etching, the first select gate transistor region is formed. Then, the first memory cell region is formed by a second silicon-etching step. Then, a sidewall mask for the third silicon etching is formed as shown in Fig. 6(b). This sequence of silicon etching after forming a sidewall mask is additionally two more times repeated for forming a second memory cell region and a second select transistor region. By above process sequence, silicon pillars having two select gate transistor regions and two memory cells regions are fabricated.

After removing all sidewall masks, the gate polysilicon is deposited following gate oxidation. Two select gates and two floating gates are vertically isolated from each other at the steps

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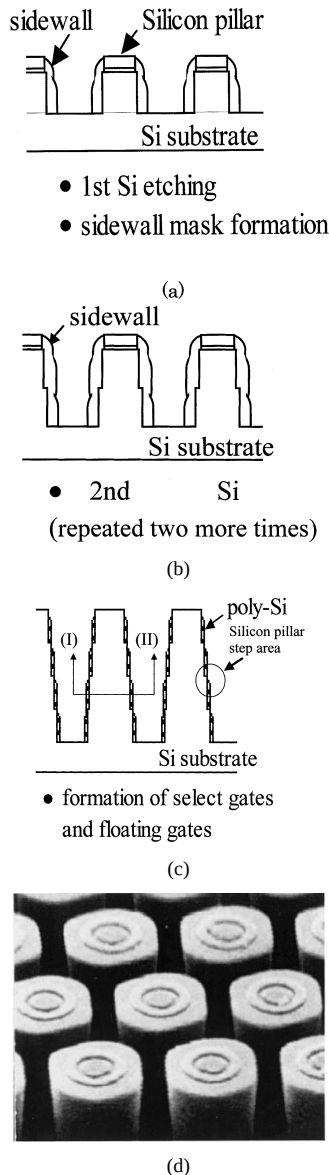


Fig. 6. S-SGT structured cell fabrication sequence.

of the silicon pillar by vertical self-aligned processes with an etch back process for polysilicon as shown in Fig. 6(c)–(e). Fig. 6(c) shows the cross-sectional schematic view of fabricated structure until this process sequence. Fig. 6(d) shows a SEM photograph of a fabricated structure until this process sequence along (I)–(II) as shown in Fig. 6(c). As shown in this SEM photograph, tunnel oxide and floating gate surround the silicon pillar successfully. Fig. 6(e) shows a SEM photograph of a fabricated structure until this process sequence at the steps of the silicon pillar as shown in Fig. 6(c). As shown in this SEM photograph, each gate is vertically isolated from its neighbor gate at the steps of the silicon pillar by vertical self-aligned processes successfully.

Next, phosphorus (P^+) is implanted to form the source and drain diffusion regions. After formation of the interpoly-silicon insulator, which consists of a composite layer of SiO_2/Si_3

N_4/SiO_2 (ONO), second polysilicon is deposited and etched back similar to the first polysilicon etch back process. Control gates are vertically isolated from its neighbors control gate at the steps of the silicon pillar as shown in Fig. 6(f)–(g). Fig. 6(f) shows the cross-sectional schematic view of fabricated structure until this process sequence. Fig. 6(g) shows a SEM photograph of the silicon pillar step region as shown in Fig. 6(f), which is the fabricated structure until above process sequence at the steps of the silicon pillar. As shown in this SEM photograph, both floating gates and control gates are vertically isolated from each other at the steps of the silicon pillar by vertical self-aligned processes successfully.

Finally, bit lines, select gates and word lines are formed. A final cross-sectional view of the S-SGT structured cell is shown in Fig. 6(h). The equivalent oxide thickness of tunnel oxide and ONO are 9.8 and 16 nm, respectively.

IV. MEASURED RESULTS

The program, erase and read characteristics of the S-SGT structured Flash memory cell are discussed.

Fig. 7 shows the program and erase characteristics of the fabricated memory cells. In this figure, the threshold voltage (V_t) of the memory cell is plotted as a function of program time and erase time, respectively. During erase operation, -30 V is applied to all control gates, while keeping the bit line, source line and substrate grounded. Therefore, the threshold voltage (V_t) for all memory cells becomes negative. During write operation, $+20$ V is applied to the selected control gate, while keeping the bit line, source line and substrate grounded. Therefore, the threshold voltage (V_t) of the selected memory cell becomes positive. As a result, programming and erasing of the S-SGT structured cell can be accomplished by uniform injection and uniform emission of F–N tunneling electrons over the whole channel area of the memory cell, respectively, a so-called bipolarity F–N tunneling write/erase technology.

Fig. 8 shows the threshold voltage shifts of the selected memory cell and the unselected one. In this figure, threshold voltage (V_t) of memory cell is shown as a function of programming time. Initial condition is that all memory cells in the S-SGT structured cell is in erased state. $+20$ V and $+10$ V are applied to the control gate of the selected memory cell and that of the unselected memory cell, respectively, while keeping bit line, source line and substrate grounded. The selected memory cell is programmed and the unselected memory cell is not programmed. Therefore, S-SGT structured memory cell can be programmed selectively.

The read characteristics of the S-SGT structured memory cell are shown in Fig. 9. In read operation, 0 V is applied to the control gate of the selected memory cell, while 3.3 V is applied to the control gate of the unselected memory cell and both select gates as shown in Fig. 9(a). Characteristics of drain current versus control gate voltage after erase operation and after program operation are shown in Fig. 9(b). A drain current flows when the selected memory cell is in its erased state, while the drain current does not flow at all when the selected memory cell is in its programmed state.

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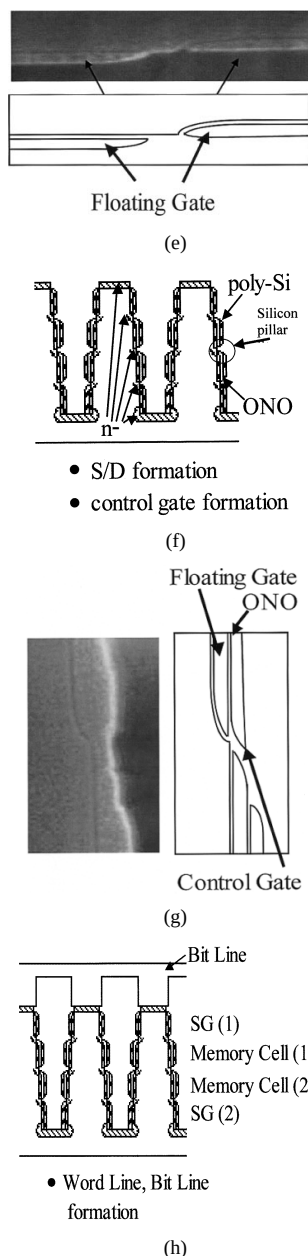


Fig. 6. (Continued.) S-SGT structured cell fabrication sequence.

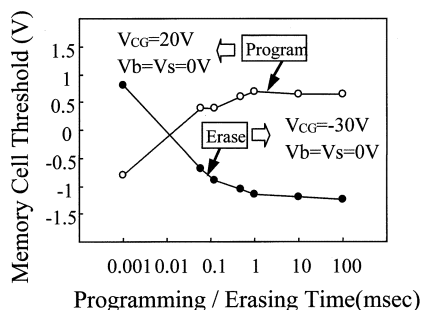


Fig. 7. Cell threshold voltages as a function of programming time and erasing time in the S-SGT structured cell.

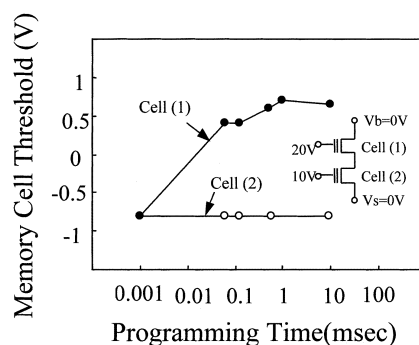


Fig. 8. Cell threshold voltages shifts of the selected memory cell and the unselected one as a function of programming time in the S-SGT structured cell.

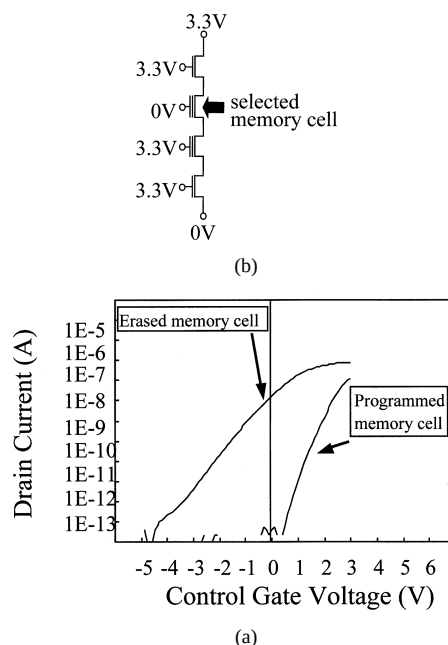


Fig. 9. Drain current versus control gate voltage characteristics after erasing and after programming of the S-SGT structured cell.

From all of the aforementioned, it is demonstrated that the S-SGT structured Flash memory cell is programmed and erased by uniform injection and uniform emission of F-N tunneling electrons over the whole channel area of the memory cell, respectively, so called a bipolarity F-N tunneling write/erase technology. Moreover, it is shown that the S-SGT structured Flash memory cell is programmed and read selectively.

Next, S-SGT structured Flash memory cell's potential is discussed by comparing with conventional NAND Flash memory cell. Equivalent circuit of S-SGT structured Flash memory cell is the same as that of conventional NAND Flash memory cell. Moreover, program, erase, and read operation methods of S-SGT structured Flash memory cell are the same as that of conventional NAND Flash memory cell. While conventional NAND Flash memory cells have the limitation of cell area of $4F^2$ per bit, S-SGT structured cell achieves a cell area of $4F^2/N$ per bit, where N is the number of stacked memory cells in one silicon pillar, without using multibit per memory cell technology. The S-SGT structured cell consisting of two

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stacked memory cells in one silicon pillar achieves a cell area per bit of less than 50% of the smallest reported NAND structured cell. By the reduction of a cell area per bit, bit line length and word line length of S-SGT structured Flash memory cell become to be shorter than that of conventional NAND Flash memory cell at the same memory array size. Therefore, S-SGT structured Flash memory cell is expected to achieve faster program and read operation speed in comparison with conventional NAND Flash memory cell. From above all, S-SGT structured Flash memory cell has potential achieving to smaller cell area per bit and faster program and read operation speed in comparison with conventional NAND Flash memory cell. Therefore, this proposed S-SGT structured Flash memory cell is suitable for future ultrahigh-density Flash memory.

V. CONCLUSION

A novel Flash memory with S-SGT structured cell has been developed. The proposed cell achieves a cell area of $4F^2/N$ per bit without multibit per memory cell technology. The fabricated novel S-SGT structured cell consisting of two stacked memory cells achieves a smaller cell area per bit of less than 50% of a conventional NAND structured cell.

The novel S-SGT structured cells are fabricated by vertical self-aligned processes using a 0.2- μm design rule. The S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of F-N tunneling electrons over the whole channel area of the memory cell, respectively, the same as conventional NAND structured cell.

The S-SGT structured cell can be successfully applied to 16 G/64 G bit Flash memory and beyond.

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REFERENCES

- [1] T. Endoh, R. Shiota, S. Aritome, and F. Masuoka, "A study of high-performance NAND structured EEPROMs," *IEICE Trans. Electron.*, vol. E75-2, pp. 1351–1357, Nov. 1992.
- [2] K. Imamiya, Y. Sugiura, H. Nakamura, T. Himeno, K. Takeuchi, T. Ikehashi, K. Kanda, K. Hosono, R. Shiota, S. Aritome, K. Shimizu, K. Hatakeyama, and K. Sakui, "A 130-mm², 256-Mbit NAND flash with shallow trench isolation technology," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1536–1543, Nov. 1999.
- [3] F. Masuoka, M. Momodomi, Y. Iwata, and R. Shiota, "New ultra high density EPROM and flash EEPROM with NAND structure cell," in *IEDM Tech. Dig.*, 1987, pp. 552–555.
- [4] M. Momodomi, R. Kirisawa, R. Nakayama, S. Aritome, T. Endoh, Y. Itoh, Y. Iwata, H. Oodaira, T. Tanaka, M. Chiba, R. Shiota, and F. Masuoka, "New device technologies for 5V-only 4Mb EEPROM with NAND structured cell," in *IEDM Tech. Dig.*, 1988, pp. 412–415.
- [5] A. Goda, W. Moriyama, H. Hazama, H. Iizuka, K. Shimizu, S. Aritome, and R. Shiota *et al.*, "A novel surface-oxidized barrier-SiN cell technology to improve endurance and read-disturb characteristics for gigabit NAND flash memories," in *IEDM Tech. Dig.*, 2000, pp. 772–775.
- [6] H. Pein and J. D. Plummer, "Performance of the 3D PENCIL flash EPROM cell and memory array," *IEEE Trans. Electron Devices*, vol. 42, pp. 1982–1991, Nov. 1995.
- [7] T. Endoh, M. Hioki, H. Sakuraba, M. Lenski, and F. Masuoka, "Floating channel type SGT flash memory," in *Meeting Abst. 1999 Joint Int. Meeting (196th Meeting of the Electrochemical Society, 1999 Fall Meeting of the Electrochemical Society of Japan With Technical Cosponsorship of the Jpn. Soc. Applied Physics)*, vol. 99-2, HI, Oct. 17–22, 1999, Abst. 1323.
- [8] M. Hioki, T. Endoh, H. Sakuraba, M. Lenski, and F. Masuoka, "An analysis of program and erase operation for FC-SGT flash memory cells," in *Proc. Int. Conf. Simulat. Semicond. Processes Devices*, 2000, pp. 116–117.
- [9] T. Endoh, K. Kinoshita, T. Tanigami, Y. Wada, K. Sato, K. Yamada, T. Yokoyama, N. Takeuchi, K. Tanaka, N. Awaya, K. Sakiyama, and F. Masuoka, "Novel ultra high density flash memory with a Stacked-Surrounding Gate Transistor (S-SGT) structured cell," in *IEDM Tech. Dig.*, 2001, pp. 33–36.



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memory cell with double poly-Si structure. In 1977, he moved to Toshiba Semiconductor Business Division, where he developed 1 Mbit DRAM and, in 1980, he applied for the Flash memory patent for the first time. In 1984, he presented Flash memory for the first time at the IEDM, and, in 1985, at ISSCC. In 1987, he returned to Toshiba Research And Development Center, where he began to develop NAND-structured Flash memory, which was presented in 1987 at IEDM. He moved to Tohoku University as a Professor in 1994. He has 170 registered patents in the USA, Germany, France, and Great Britain, 100 registered patents in Japan, and 71 pending patents. He authored and coauthored approximately 150 papers.

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