

New Three-Dimensional High-Density Stacked-Surrounding Gate Transistor (S-SGT) Flash Memory Architecture Using Self-Aligned Interconnection Fabrication Technology without Photolithography Process for Tera-Bits and Beyond

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New three-dimensional Stacked-Surrounding Gate Transistor (S-SGT) flash memory architecture can achieve the cell area of $3.88F^2$ per bit using the $0.2\mu\text{m}$ design rule. The new architecture is realized by stacking two select transistors and two memory cells vertically on each pillar located in a two-dimensional array matrix. Each gate and each interconnection of this new architecture are fabricated by the vertical self-alignment process and horizontal self-alignment process simultaneously using HTO conformal deposition and reactive ion etching (RIE) without using the photolithography process. The new three-dimensional S-SGT flash memory architecture is applicable to high-density nonvolatile memories as large as tera-bits and beyond. [DOI: 10.1143/JJAP.43.2217]

KEYWORDS: flash memory, stacked-surrounding gate transistor (S-SGT) flash memory, self-aligned interconnection fabrication technology

1. Introduction

The surrounding gate transistor (SGT) was proposed in order to achieve future VLSI devices with high packing density,¹⁾ and an SGT dynamic random access memory (DRAM) cell was also proposed.²⁾ In order to overcome the limitation of $4F^2$ per bit in conventional NAND flash memory cells³⁾ without using multi bit per memory cell technology, a stacked-SGT (S-SGT) structured cell was proposed.⁴⁾ However, the method of fabricating interconnections between each of the memory cells in order to form a two-dimensional memory array matrix using S-SGT structured cell was not presented.

In this paper, self-aligned interconnection fabrication technology is proposed, in order to realize new three-dimensional high-density S-SGT flash memory architecture. The new architecture is realized by stacking two select transistors and two memory cells vertically on each pillar located in a two-dimensional array matrix. Each gate and each interconnection of this new architecture are fabricated by the vertical self-alignment process and horizontal self-alignment process simultaneously using HTO conformal deposition and RIE without using the photolithography process. This new three-dimensional S-SGT flash memory architecture can achieve the cell area of $3.88F^2$ per bit using the $0.2\mu\text{m}$ design rule. In this paper we describe the memory array architecture, fabrication process and operation principle of the new three-dimensional high-density S-SGT flash memory architecture.

2. Memory Architecture

The new three-dimensional high-density S-SGT flash memory is fabricated by arraying S-SGT pillars. Figure 1 shows the architecture and the equivalent circuit of the new three-dimensional high-density S-SGT flash memory. In one pillar, source line, first select gate transistor (SG1), first flash memory cell (MC1), second flash memory cell (MC2), second select gate transistor (SG2) and bit line are stacked in series, vertically.³⁾ The gates of SG1 are interconnected by

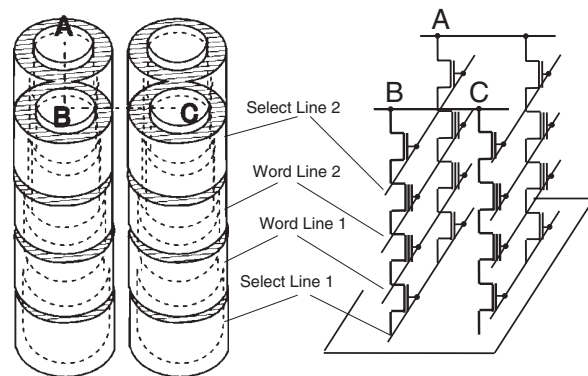


Fig. 1. Bird's eye view of the new three-dimensional high-density S-SGT flash memory and its equivalent circuit.

the select-line 1 (SL1) along the row direction and separated along the column direction. The control gates of MC1 are interconnected by the word-line 1 (WL1) along the row direction and separated along the column direction. Similarly, MC2 and SG2 are interconnected by word-line 2 (WL2) and select-line 2 (SL2), respectively.

3. Fabrication Process

The new three-dimensional high-density S-SGT flash memory is fabricated using a $0.2\mu\text{m}$ process. The concept of self-aligned interconnection fabrication technology is as follows. Figure 2 shows the top view of a silicon pillar array after HTO conformal deposition, following polysilicon deposition. The distance between the silicon pillar along the row direction d_{row} is designed to be sufficiently narrower than two times the sum of the thickness of the polysilicon and that of HTO. Figure 3 shows the self aligned interconnection fabrication sequence by using the cross-sectional view of A-B-C in Fig. 2. As shown in the figure, HTO can bury the space between the pillars along the row direction which is designed to be narrower than twofold the

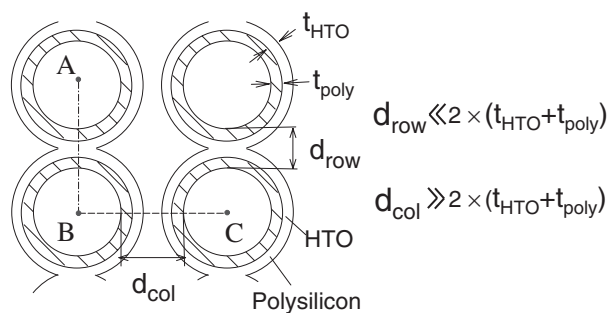


Fig. 2. Top view of pillar array after HTO conformal deposition, following polysilicon deposition.

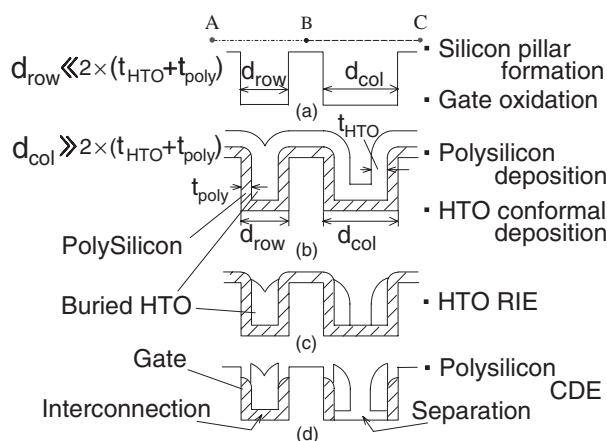


Fig. 3. Self-aligned interconnection fabrication sequence.

deposited HTO thickness. On the other hand, HTO cannot bury the space between silicon pillars along the column direction which is designed to be wider than twofold the HTO thickness. After CDE of polysilicon followed by RIE of HTO, the polysilicon in the narrower space remains and that in the wider space is etched away. Using this concept, a new three-dimensional high-density S-SGT flash memory architecture is formed as shown in Fig. 4. Firstly, the silicon pillar is formed and gate oxidation is carried out followed by polysilicon deposition. Then HTO conformal deposition is carried out. The bottom region between silicon pillars along the row direction is buried with HTO, because this region is narrower than twofold the HTO thickness. On the other hand, the bottom region between the pillars along the column direction is not buried with HTO, because this region is wider than twofold the HTO thickness. According to the concept shown in Fig. 3, RIE of HTO (Step B), RIE of Polysilicon and removal of HTO are carried out sequentially to form SL1 and select gate 1 (the gate of SG1). Simultaneously, the floating gate of MC1 and the floating gate of MC2 are formed. By repeating these processes, the control gate of MC1 and the WL1 are formed simultaneously. Similarly, the control gate of MC2 and WL2 are formed simultaneously. The gate of SG2 and SL2 are formed simultaneously. Through these fabrication processes described, high-density S-SGT and the stacked interconnection lines are formed by a vertical self-alignment process and by a horizontal self-alignment process simultaneously without

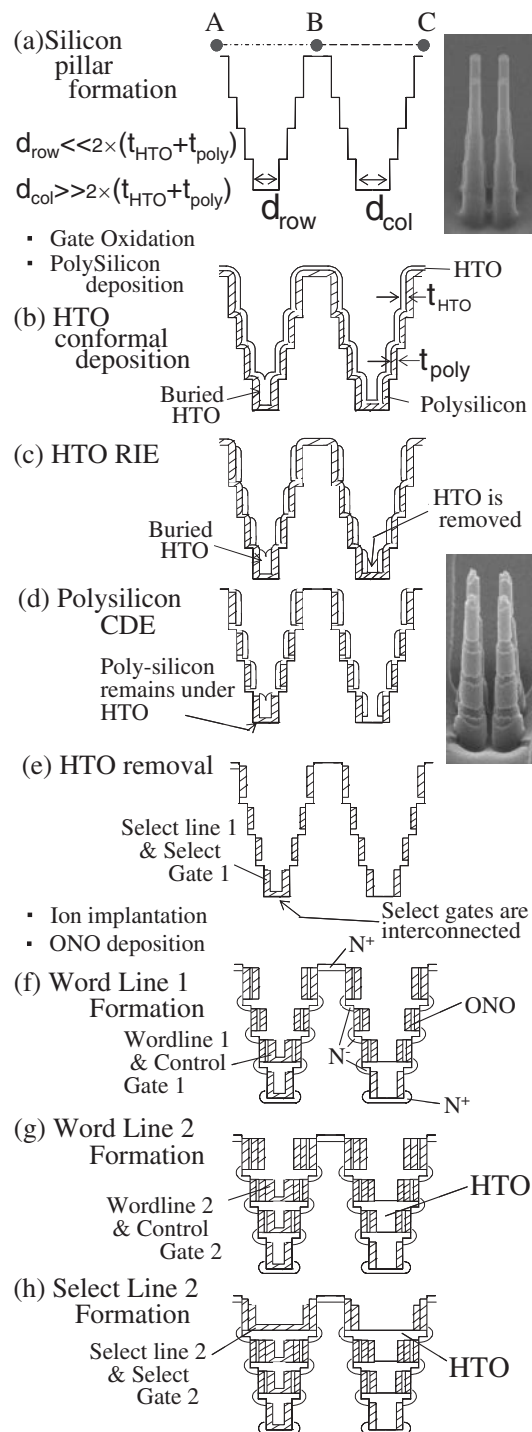


Fig. 4. New three-dimensional high-density S-SGT flash memory fabrication sequence.

using the photolithography process. By using the 0.2 μm process and by selecting suitable thicknesses of polysilicon and HTO, a new three-dimensional flash memory architecture can be achieved with 3.88F^2 per bit. The International Technology Roadmap for Semiconductors (ITRS) 2002 update predicts that the minimum feature size F will be 22 nm and the chip size will be over 200 mm^2 in 2016. The minimum cell area per bit is 4F^2 as far as current planar technology is used. Accordingly, in 2016 the total bit density will be approximately 100 Gbits and is not attainable to 1 Terabit by the extension of current planar technology. The

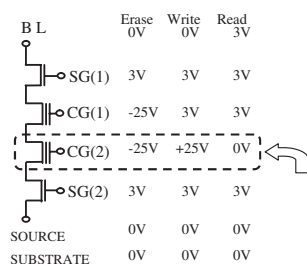


Fig. 5. Equivalent circuit and operating voltages of the S-SGT structured cell.

new three-dimensional high-density S-SGT flash memory technology can achieve the cell area of $4F^2/N$, where N is the number of stacked memory cells. Applying the optimum number of N , tera-bit flash memory will be realized earlier than that predicted in the ITRS 2002 update without using multi bit per memory cell technology.

4. Cell Operation

Figure 5 shows an equivalent circuit and operation voltage. In the erase operation, -25 V is applied to all control gates, while keeping the bit line, source line and substrate grounded, and applying $+3\text{ V}$ to all select gates. Therefore, the threshold voltage (V_t) for all memory cells becomes negative. In the write operation, $+25\text{ V}$ is applied to the selected control gate, while keeping the bit line, source line and substrate grounded, and applying $+3\text{ V}$ to the unselected control gate and all select gates. Therefore, the threshold voltage (V_t) of the selected memory cell becomes positive. As a result, the S-SGT structured cell can be programmed and erased by uniform injection and uniform emission of Fowler-Nordheim (F-N) tunneling electrons over the whole channel area of the memory cell, respectively, the so called bi-polarity F-N tunneling write/erase technology. In the read operation, 0 V is applied to the selected control gate, source line and substrate, and $+3\text{ V}$ is applied to the unselected control gates, the bit line and all select gates. The endurance characteristic of S-SGT structured flash memory cell is shown in Fig. 6. The excellent endurance characteristics of the new three-dimensional S-SGT structured flash memory cell is due to the bi-polarity F-N tunneling write/erase technology. The bi-polarity F-N tunneling write/erase technology leads to low degradation of the tunneling oxide and excellent retention characteristics.⁵⁾

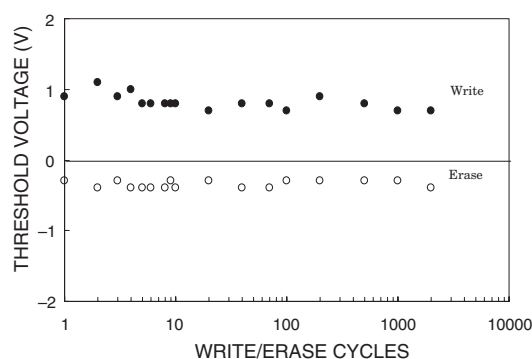


Fig. 6. Endurance characteristics of the S-SGT structured cell.

Therefore this endurance characteristic of the S-SGT structured flash memory cell is the most suitable for the tera-bit flash memories.

5. Conclusion

New three-dimensional S-SGT flash memory architecture can achieve the cell area of $3.88F^2$ per bit using the $0.2\text{ }\mu\text{m}$ design rule. Each gate and each interconnection of the S-SGT flash memory architecture are fabricated using the vertical self-alignment process and horizontal self-alignment process simultaneously using HTO conformal deposition and RIE without using the photolithography process. Moreover, a highly reliable S-SGT structured flash memory has been successfully developed by using a bi-polarity F-N tunneling write/erase technology. The new three-dimensional S-SGT flash memory architecture is applicable to high-density nonvolatile memories such as tera-bit flash memory and beyond.

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