



Current Sources & Voltage References

Linden T. Harrison



CURRENT SOURCES & VOLTAGE REFERENCES

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Using JFETs and CRDs to Create Current Sources

6.1 The JFET paved the way

Just as BJTs can be used to create current sources, so too can field-effect transistors. The designer can readily utilize *junction* FETs (JFETs) and complementary metal oxide semiconductor (CMOS) FETs in low current-source applications. Alternately, one can use double-diffused MOS (DMOS) FETs for higher current requirements. However, these types of devices are often overlooked by the OEM board-level designer, because of their somewhat unfamiliar terminology, as opposed to the wide-scale popularity of the bipolar junction transistor (BJT). Actually, use of the FET can often render a simpler and less costly circuit, if one understands some of the critical parameters involved, rather than using more expensive solutions. These might include using op amps with voltage references or matched bipolar transistors, as discussed previously. Although it is a little more complex than is depicted here, because of process differences (e.g., silicon gate, metal gate, vertical, double-diffused), the basic FET family tree is shown in Figure 6.1. Not all FET versions are available or easy to manufacture. For example, you can see from the diagram that JFETs only function in the depletion mode, and P-channel depletion-mode MOSFETs are unavailable.

The basic theoretical principles of the FET were outlined in various papers published in the late 1920s by a German-born physicist, Dr. Julius E. Lilienfeld. He was granted a patent by the U.S. Patent Office in 1930. Some 17 years later, Dr. Shockley and his colleagues at AT&T's Bell Labs further theorized on this device (the unipolar transistor, as it was originally called), and in the course of their research with the FET, won the Nobel Prize for Physics in 1956, for inventing the bipolar transistor. After patenting the BJT, Dr. Shockley went on to publish various theoretical papers on other semiconductor devices, and in 1952 he invented and patented the JFET, although he did not actually make one. It had been some 22 years since Dr. Lilienfeld first theorized on an FET-like device.

For several years after, the FET languished only as a lab curiosity, during which time the epitaxial process was developed by Dr. Ross's group at Bell Labs. Then in 1959, Dr. Jean Hoerni, a co-founder of Fairchild Semiconductor, developed and patented the semiconductor industry's planar process and designed the first modern-day planar epitaxial JFETs. (Dr. Hoerni subsequently went on to co-found Teledyne Amelco, which also became a major source of JFETs, then later he co-founded Intersil, a major

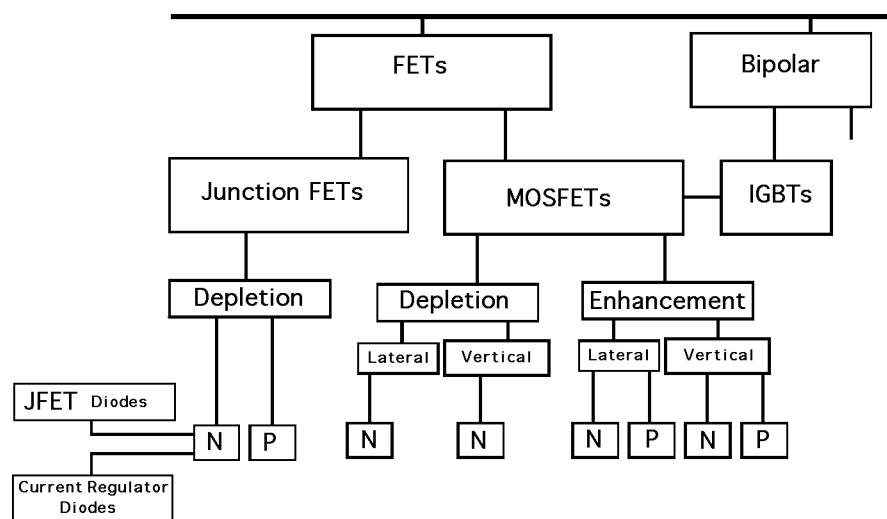


Figure 6.1. The FET family tree.

analog CMOS pioneer.) In the early 1960s, Siliconix, Amelco, and Crystalonics were some of the first companies in the world to specialize and manufacture JFETs in volume. One of Siliconix's co-founders, Bernie Murphy, was a former Bell Labs researcher who had invented the important "buried collector" structure, which has been indispensable to manufacturing analog ICs.

Besides Fairchild Semiconductor, Siliconix, Crystalonics, and Teledyne Amelco, other notable JFET pioneers included National Semiconductor, Solitron Devices, Motorola Semiconductor, Texas Instruments, Philips Semiconductor, and Union Carbide. Some of these companies no longer make discretes or JFETs; only a few of these original pioneers are still even selling FETs. They should all be congratulated, though, because without their bold efforts we would not have CMOS, DMOS, gallium-arsenide FETs, silicon power MOSFETs, or IGBTs, all of which now dominate in various market segments of present-day electronics. By today's standards these early devices were fairly raw, but the limitations on these pioneers was only in the available technology of their time—namely in processing, precision lithography, and diffusion techniques.

Although both BJTs and FETs are used as switches, amplifiers, and current sources, the JFET can also be used in its simplest form as a voltage-controlled resistor. The JFET has many diverse applications (see Figure 6.2), which exploit its various characteristics, when compared with the BJT. Besides voltage-controlled resistors, they include low-noise, differential, and high input-impedance (Z_{in}) amplifiers, audio and AGC amplifiers, video and RF amplifiers, analog switches, RF mixers, H-F oscillators, and current sources. In the design of many of today's analog ICs, JFETs are commonly used for circuit start-up, biasing, and front-ends in bipolar-FET op amps.

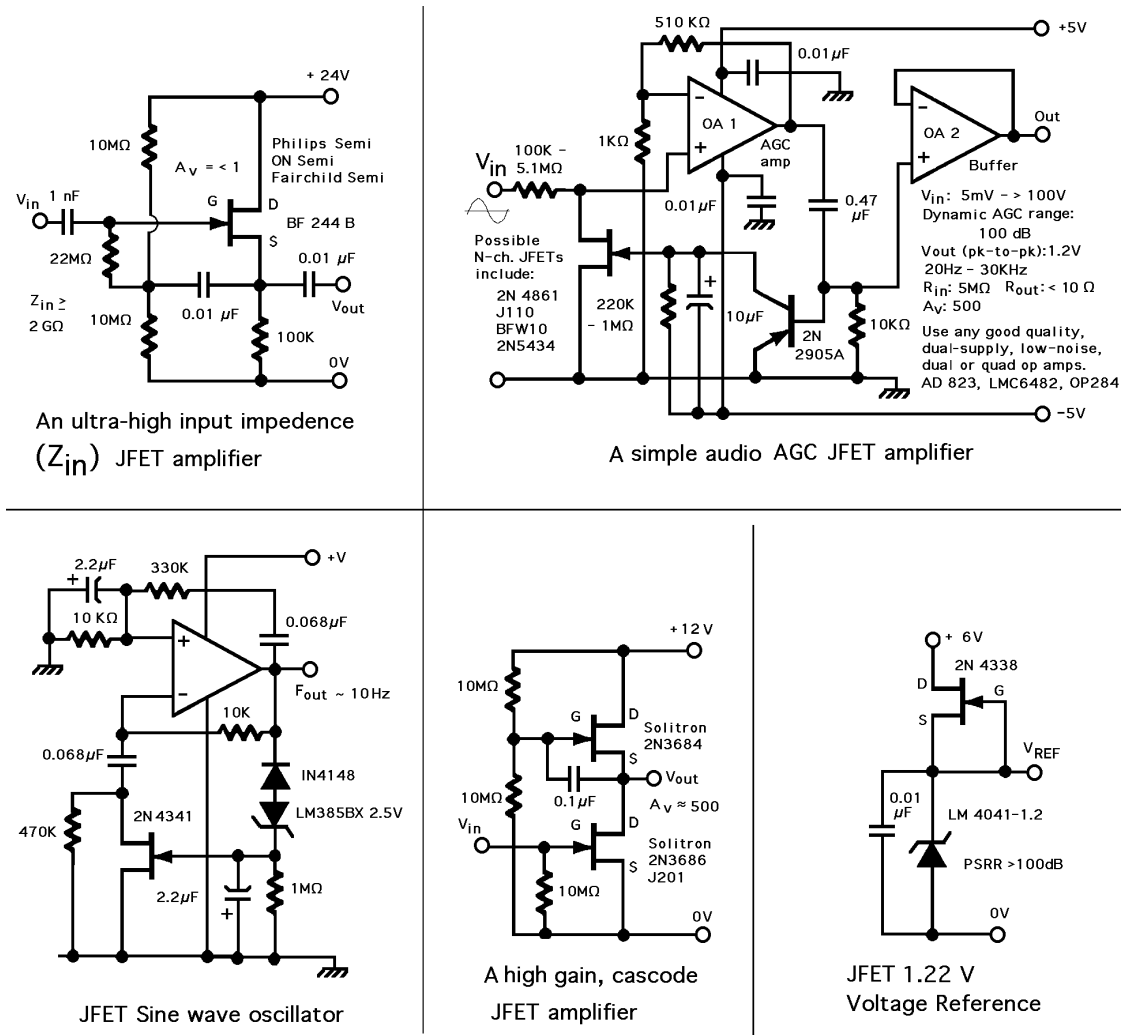


Figure 6.2. Common JFET applications.

In the United States, the following semiconductor manufacturers make silicon JFETs:

- Calogic
- Central Semiconductor
- Crystalonics
- Fairchild Semiconductor
- InterFET

- Linear Integrated Systems
- Microsemi
- ON Semiconductor
- Philips Semiconductors
- Solitron Devices
- Vishay-Siliconix

It's a tribute to those many researchers and JFET engineers from the 1960s and '70s that many of the products they created and modeled are still available today, nearly 40 years later, and still finding new applications.

6.2 Characteristics of the JFET

Even though the silicon junction FET is made similarly to a diode or bipolar transistor (by the planar, epitaxial process), it has some unique characteristics of its own, not shared by the others. However, because the JFET is also a junction device, it inherently has some of the same characteristics as both the diode and BJT. The FET is a unipolar device using only one type of current carrier to support conduction, unlike the BJT, which utilizes both electrons and holes to support conduction. In the case of N-channel FETs, they utilize free electrons, which are negative carriers, whereas P-channel FETs use holes, which are positive carriers. As discussed previously, because electrons have a higher mobility than holes, they tend to move through the semiconductor crystal material faster. This higher-speed capability translates into the fact that N-channel FETs of all types, not just JFETs, are more popular and available than P-channel FETs; N-channel devices are invariably faster.

Advances over the past two decades, however, have closed the gap considerably between P-types and N-types, so that their speeds are now much closer. As a rule of thumb, the smaller the FET chip, the lower capacitance and the faster, though less powerful, it will be. Large chips, as used in MOSFETs, have a lower "on" resistance $R_{DS(on)}$, thereby a higher current capability, $I_{D(on)}$, and are geared for power switching. They tend to have higher input and output capacitance and are therefore slower. A JFET's input capacitance (C_{iss}) is typically less than 10 pF and remains constant up to about 1 GHz. For a small MOSFET, this may be more than 30 pF, but with a power MOSFET, it can be more than 1000 pF. The output capacitance (C_{oss}) for the JFET and small MOSFET are typically less than 30 pF, while that of the power device may be 10 or 20 times higher. As a result, JFETs and small DMOS FETs are usually much faster than power MOSFETs. Varactor FETs exploit the device's unique capacitance characteristics, have two separate gates, and are used for RF applications.

Individual JFETs are typically three-terminal devices like BJTs, with the *gate*, *drain*, and *source* corresponding to the BJT's base, collector, and emitter (see Figure 6.3).

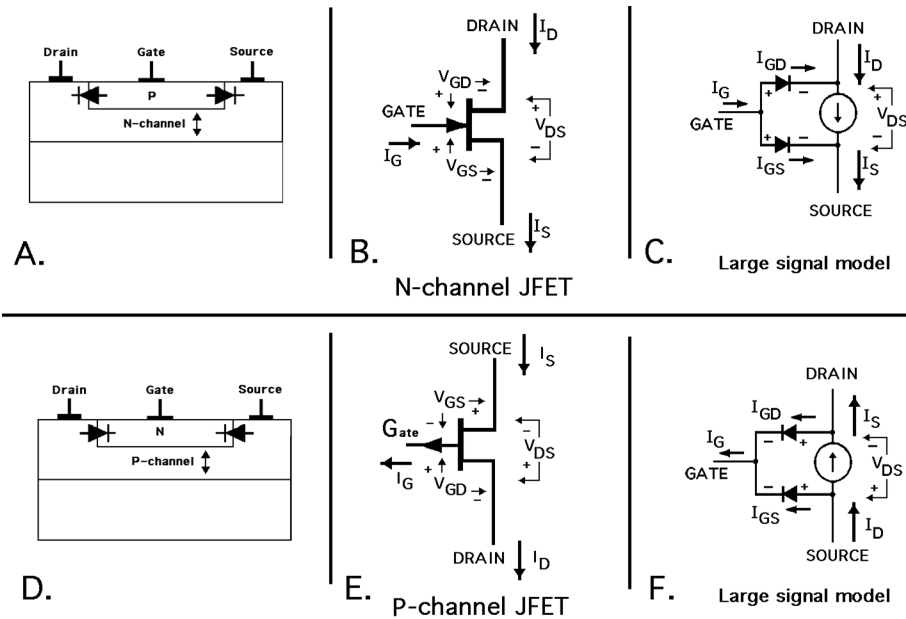


Figure 6.3. Showing the structure of the JFET, as well as its various voltages, currents, and polarities. Notice the two-channel diodes that provide forward and reverse bias.

Besides individual discretes, some FETs are also available as matched-pairs, duals, and arrays, in standard metal, plastic, and surface-mount packages.

Another unique characteristic of the FET is that it is voltage-controlled, whereas the bipolar transistor is current-controlled. To control current passing through any type of FET, one uses a voltage at its gate, whereas with the bipolar transistor a combination of base voltage and current is used. The N-channel JFET is a *normally-on* device, until the gate-to-source voltage (V_{GS}) becomes negative enough to reverse-bias the gate channel diode, and so turn it off. The point where this occurs is known as $V_{GS(off)}$, which we will look at in more detail shortly. The P-channel JFET is also a *normally-on* device, until the gate voltage becomes positive enough to reverse-bias the gate channel diode, and thereby turn it off. In contrast, the bipolar transistor (both NPN and PNP) is a normally-off device until sufficient voltage (V_{BE}) and base current (I_B) are provided to turn it on.

N- and P-channel JFETs work only in the *depletion mode* (as shown in Figure 6.3A and D). Other types of FETs can operate in either the depletion mode or the enhancement mode, which we will cover in a later chapter. The depletion mode operates by a gate voltage depleting or shutting off the majority current carriers in the channel. It

does this by changing the size of the depletion region within the junction area, thus increasing the resistance and reducing the current flow. It requires virtually no gate current to function. The cross-sectional area ($L \times W$) of the JFET's channel is fixed by the device geometry. However, the thickness and position of the channel is controlled by a combination of the gate-to-source voltage (V_{GS}) and the drain-to-source voltage (V_{DS}). These effectively change the resistance in the channel, allowing full, partial, or no conduction.

Because there is virtually no gate current, the JFET has an extremely high *input impedance* (Z_{in}), typically more than $100\text{ M}\Omega$ (more than 1×10^8). To illustrate this point, consider an N-channel JFET amplifier having a gate voltage of -2.5 volt and a gate current of 25 nA . Ohm's law shows us that:

$$R = \frac{2.5V}{25nA} = 100M\Omega \quad (\text{Eq.6.1})$$

This very high impedance applies at low frequencies, because the input impedance of the FET's gate is caused by its inherent channel diode—in effect a reverse-biased diode. At RF frequencies, however, the input impedance drops proportionally to the square of the input frequency. This means that while the input impedance may be several hundred $M\Omega$ at audio frequencies, the impedance at say 100 MHz will probably drop several orders of magnitude, to less than $50\text{ K}\Omega$. Input impedance also depends on the value of any external gate-source resistance used in the gate circuit (which is usual when using the JFET as an amplifier). The lower the value of this external resistor, the higher the JFET's frequency response will be, and vice versa. This resistor (often labeled R_G) is usually found between the gate and the source in JFET amplifier circuits. Its function is to set a predetermined input impedance to match the signal source and to ensure that the JFET's gate is at 0 volts with no input signal present. The output impedance of the JFET depends on its gain, frequency, internal source resistance, and the value of the external source load resistor. It can range from a few ohms to more than $1\text{ M}\Omega$. Higher current JFETs, such as many analog switches, have a much lower drain-to-source resistance, $R_{DS(on)}$, a lower internal source resistance, and so a very low output impedance.

Because JFETs are voltage-controlled, they have much lower equivalent *noise characteristics* (nV/Hz) than do most bipolars, which explains their popularity as low-level preamplifiers, as well as being used for the same reasons as op amp input stages. JFETs are also well suited to *high-frequency* operation, including RF/VHF/UHF, and have much better linearity than BJTs. Although JFETs have a comparatively lower voltage gain than bipolars, they have a much higher dynamic range than bipolars (typically better than 100 dB), so they can amplify smaller signals with lower noise or amplify large signals without introducing distortion.

Discrete JFET amplifiers fall into one of several different types: *high-frequency*, *low-leakage*, *low-noise*, and *general-purpose*. High-frequency types typically have very

low capacitance and a high transconductance (g_{fs}), and often sacrifice other characteristics like gate leakage current and breakdown voltage for high frequency. Low-leakage types offer low capacitance, low transconductance, and leakage currents of less than 1 pA. Low-noise types also offer a low conductance (g_{os}), as well as reasonable breakdown voltages, leakage currents, and transconductance. General-purpose types offer many of the good characteristics of the other three types and usually have higher values of transconductance and noise than, say, low-leakage types. All four types have devices that are suitable as current sources, but the most suitable JFETs come from the low-noise amplifier variety.

A typical set of curves for an N-channel JFET showing drain current, drain-source voltage, various gate-source voltages, and other characteristics is shown in Figure 6.4. Notice first that three regions govern the JFET's operation: (1) the *ohmic* or *linear* region, (2) the *saturation* region, and (3) the *breakdown* region. The ohmic or linear region occurs at low drain currents and low drain-source voltages, below the point shown as " V_p " in Figure 6.4.

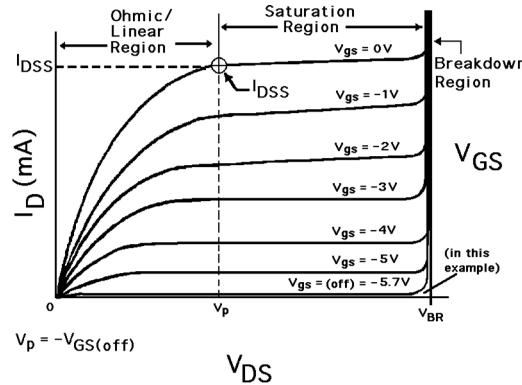


Figure 6.4. A typical set of output characteristic curves for an N-channel JFET.

This region, to the left of V_p , is utilized for creating voltage-controlled resistance (VCR), where the drain-source channel conductance is a near-linear function of the gate-source voltage. This subject is beyond the scope of this book, but it may be expressed as follows:

$$I_D = \frac{2I_{DSS}}{V_{GS(off)}} V_{DS} \left(V_{GS} - V_{GS(off)} - \frac{V_{DS}}{2} \right) \quad (\text{Eq. 6.2})$$

With a JFET amplifier, its DC performance depends on its optimum bias point (Q-point) within the particular circuit, and it must be correctly biased with respect to the

supply voltages (see Figure 6.5). As mentioned, the JFET is composed of two junctions, as shown previously in Figure 6.3A and D. In the N-channel JFET, both are forward-biased junctions, which are similar in many respects to the diode we looked at in a previous chapter. In actual use, though, the polarity of the voltage at the gate reverse-biases these two junctions, in that the V_{GS} ranges from full conduction ($V_{GS} = 0$ volt) to some negative amount of several volts to turn it off— $V_{GS(off)}$. With the P-channel JFET, the gate voltage must become positive enough to reverse-bias the gate channel diode, and thereby turn it off. Again, turning the P-channel JFET full on and conducting occurs at $V_{GS} = 0$ volt. Thus the voltage at the gate of the P-channel device typically ranges from 0 volt to a more positive level of several volts.

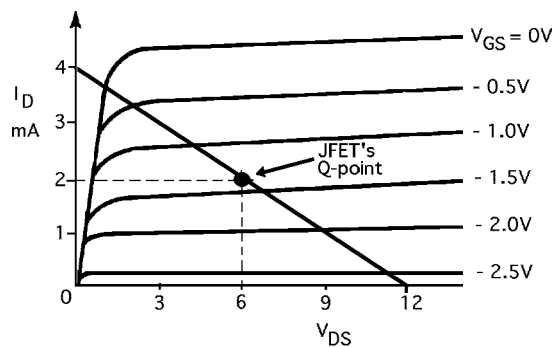


Figure 6.5. The Q-point for a typical N-channel JFET amplifier, operating at 12 volts at 4 mA.

The JFET, being a three-lead device, is capable of three distinct modes of operation: *common gate* (CG), *common drain* (CD), and the most familiar—*common source* (CS). In addition, the JFET has some unique subscript notations that reference either the connection, current flow, or test condition used. In some situations there may be one, two, or three subscript letters used. For example, I_G refers to gate current, while C_{GD} refers to the capacitance between gate and drain. The term I_{DSS} refers to the drain-to-source current, with the gate shorted to the source. The last letter (“S”) refers to the condition of the remaining terminal, in this case the gate, which is designated as being shorted to the common terminal (always the middle of the three subscript letters). Thus, I_{GSS} refers to the gate-to-source current, with the drain shorted to the source. The abbreviation g_{fs} refers to transconductance (g), in this case forward transconductance, designated by “f,” in common source mode, designated by the “s.” Although not a complete study, some relevant JFET equations and models are given in Appendix A. Here we look at some of the JFET’s more important and relevant characteristics as regards potential current sources.

One important JFET characteristic is the gate-to-source breakdown voltage, $V_{(BR)GSS}$. This is measured with the JFET’s drain shorted to the source, at a specified gate current. This parameter is invariably specified at the beginning of a JFET’s data sheet. In

normal operation, though, the V_{GD} is much higher than the V_{GS} . However, JFETs are manufactured according to a particular process, much of which dictates the breakdown voltage of the device. As a result, JFETs normally use the *same value for both* $V_{(BR)GSS}$ and $V_{(BR)GDS}$, although the latter is not usually specified other than in the absolute maximum ratings for V_{GD} . Actually, this gate-to-drain voltage is responsible for most of a JFET's tiny leakage current (I_{GD}), which like any P-N junction increases with either increased voltage or temperature.

Although the JFET is controlled by a voltage at its gate, there is actually a tiny current involved called the *gate operating current* (I_G) typically in the range of 1–100 pA, at room temperature. This current applies when the drain current is flowing and rises rapidly with an increase in either temperature or V_{DG} . As the V_{DG} is increased, typically upwards of about 20 volts, the gate current rises exponentially, caused by a type of avalanche breakdown at the junction. This is often referred to as the gate current's *breakpoint*. Another current referred to in many course books and texts is the *gate-to-source reverse leakage current* (I_{GSS}). It is also specified on many JFET data sheets. The last letter indicates that the drain is shorted to the source. It is a very small leakage current usually measured in pico-amps, which applies at a specified gate-to-source voltage. It is composed of two currents: the gate-to-source (I_{GS}) and the gate-to-drain (I_{GD}) currents. This I_{GSS} leakage current approximately doubles for every 10°C rise in temperature, as shown in Figure 6.6.

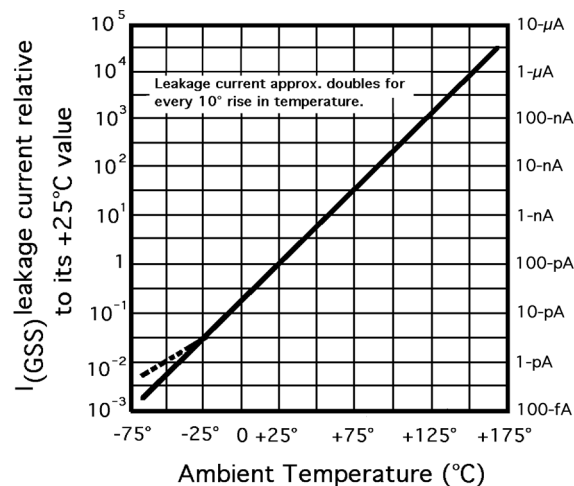


Figure 6.6. Example of a JFET's junction leakage current, as a function of temperature.

With a JFET, the maximum limiting current that can flow between the drain and source is known as the *drain saturation current* (I_{DSS}). This occurs at a particular V_{DS} , when the V_{GS} is at zero. It is clearly seen in Figure 6.4, where the drain current increases linearly, then begins to be pinched off or limited at the knee of the curve. This particular

set of curves, which displays the drain current (I_D) versus the V_{DS} , with applied V_{GS} , is normally referred to as a JFET's *output characteristic*. It is depicted in most JFET data sheets and can be easily measured, using the circuit shown in Figure 6.7. With a JFET, this current is typically less than 50 mA, although some devices are capable of higher current.

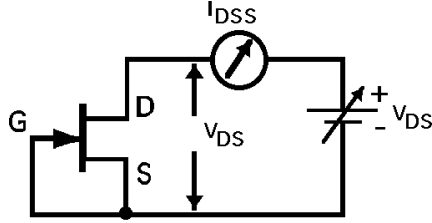


Figure 6.7. I_{DSS} measurement for an N-channel JFET.

At the low end of the I_{DSS} scale, some JFETs can only work below 1 milliamp. In any event, I_{DSS} may typically range over 3:1 for similar devices, so it is important that one considers both the minimum and maximum ratings/curves in the range. I_{DSS} is also temperature sensitive and has a small negative temperature coefficient of approximately $-0.5\%/^{\circ}\text{C}$.

Some manufacturers occasionally specify $I_{D(off)}$ and/or $I_{D(on)}$ in their JFET product data sheets. $I_{D(off)}$ is the drain cutoff current, which is the amount of leakage between the drain and source. It is usually specified at a particular V_{DS} and V_{GS} . $I_{D(off)}$ is usually shown on a data sheet in nano-amps (nA), at both room temperature and at elevated temperatures. $I_{D(on)}$ is a specific level of I_D where the V_{DS} is greater than the pinch-off voltage (V_p). Once one has specific data for a particular JFET's $V_{GS(off)}$ and I_{DSS} , its drain current (I_D) can be calculated by:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 \quad (\text{Eq.6.3})$$

As an example, let's confirm that the JFET is in the saturation region and at full conduction, where I_{DSS} is at its maximum. Let's assume for this example that the JFET's I_{DSS} equals 3.6 mA, its $V_{GS(off)}$ equals -2.65 volts, its V_{GS} equals 0 volt, the test circuit is as shown in Figure 6.7, and this test is conducted at room temperature.

$$I_D = 0.0036 \left(1 - \frac{0V}{2.65V} \right)^2 = 3.6\text{mA, ie. } I_{DSS} \text{ value} \quad (\text{Eq.6.4})$$

Seeing as the key parameter V_{GS} equals 0 volt, this confirms that the JFET is at full conduction.

Another important characteristic is $V_{GS(off)}$, the *gate-to-source cutoff voltage* necessary to turn the FET off. The V_{GS} for an N-channel JFET ranges from 0 volt for full conduction to some negative amount of typically several volts to turn the device off. This is shown in Figure 6.4, and we just saw it used in equation 6.4. Some JFETs have a remarkably low $V_{GS(off)}$ value. For example, a 2N4338 has a maximum $-1 V_{GS(off)}$, while a J202 has a maximum $V_{GS(off)}$ of -1.5 volt. At the other end of the scale, the popular Vishay-Siliconix general-purpose 2N3819 JFET has a maximum $-8 V_{GS(off)}$, while a Crystallonics high-voltage (300 V_{DGO}) 2N5543 has a $-15 V_{GS(off)}$. For some applications, where high supply voltages are involved (more than 20 to 90 volts), higher $V_{GS(off)}$ devices like these can be indispensable.

For a P-channel JFET, $V_{GS(off)}$ ranges from 0 volt for full conduction to some positive amount of several volts. For example, a J176 has a $V_{GS(off)}$ of $+4$ volt (remember it's a P-channel device, so it has a positive gate-to-source bias). With either type, this occurs when the V_{DS} is equal to or greater than the pinch-off voltage (V_p), so that only V_{GS} controls conduction through the channel. So with an N-channel JFET, while the value of V_p is some relatively low positive value, the value of $V_{GS(off)}$ will be the same value, but of opposite polarity. Today most manufacturers and circuit designers prefer using the term $V_{GS(off)}$ rather than V_p , and this is reflected in most JFET product data sheets. It is important for the circuit designer to know the knee of the curve and the minimum V_{DS} necessary to reach the pinch-off point. The graph shown in Figure 6.4 clearly shows the complete I_D versus V_{GS} curves (transfer curves), from V_{GS} equals 0 through $V_{GS(off)}$, for a typical N-channel JFET. However, the data sheet for your chosen device may not necessarily portray the data in exactly the same manner, and you might have to resort to measuring devices and plotting your own curves. These transfer curves are depicted in most JFET data sheets, and the circuit shown in Figure 6.8 shows how this is measured.

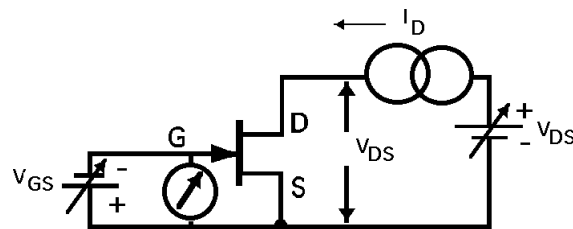


Figure 6.8. $V_{GS(off)}$ measurement for an N-channel JFET.

As you can see in Figure 6.9, I_{DSS} and $V_{GS(off)}$ both shift with temperature. Actually, $V_{GS(off)}$ has a negative temperature coefficient of approximately $-2 \text{ mV}/^\circ\text{C}$.

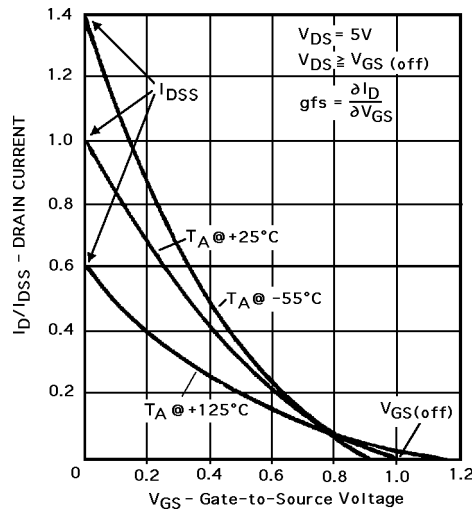


Figure 6.9. Typical JFET transfer versus temperature curves.

Most JFET data sheets specify $V_{GS(off)}$ with typical and maximum values, at a particular V_{DS} and drain current. Some devices also have a minimum value of $V_{GS(off)}$ specified. For example, the popular 2N4416A is specified with a V_{DS} equals 15 volts and I_D equals 1 nA, and has a typical $V_{GS(off)}$ of -3 volts, a minimum of -2.5 volts, and a maximum of -6 volts. In some JFET circuits, particularly when two devices are used together, such as in a cascode circuit, one FET may need to have a higher $V_{GS(off)}$ than the other. Because $V_{GS(off)}$ can typically range over 3:1 or 4:1 for similar devices, it is important that one considers both its minimum and maximum ratings in the range for your application.

Another important characteristic of the JFET is its *transconductance/forward conductance* (g_{fs}) or small-signal common-source forward transconductance (g_m or Y_{fs}). G_{fs} measures the effect of a change in drain current (I_D), for a specific change in gate voltage (V_{GS}), referenced to common-source mode. The input voltage and the output current are related by the transconductance, because the gate voltage is *transferred* to the source current and because g_{fs} (or g_m) applies to *conductance*. Thus,

$$I_D = -g_{fs} V_{gs} \quad (\text{Eq.6.5})$$

You probably recognize this from the JFET's small-signal model, part of which is shown here in Figure 6.10, and more fully in Appendix A7.

The transconductance value can be found by either of the following equations:

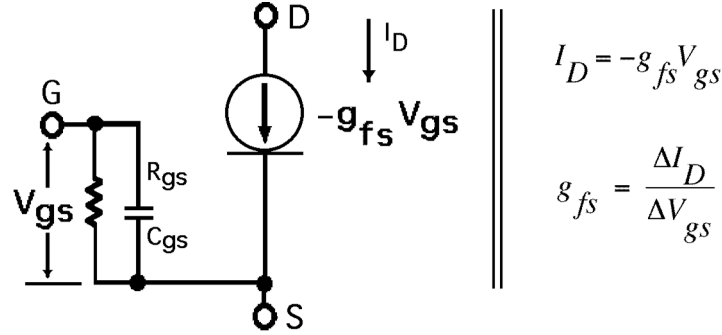


Figure 6.10. The JFET's small-signal transconductance model.

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{gs}} \bigg|_{V_{DS} = \text{constant}} \quad (\text{Eq.6.6})$$

$$g_{fs} = \frac{2I_{DSS}}{V_{GS(off)}} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right) \quad (\text{Eq.6.7})$$

In practical terms, transconductance is a measure of the JFET's gain, or ability to amplify, and is a figure of merit. On a graph it appears as a steep or shallow slope, as shown in Figure 6.11, and is usually referred to in milli-Siemens (mS). The old value was measured in μmhos (ohms reversed), but most JFET manufacturers now specify g_{fs} in mS or μS as standard. g_{fs} is usually measured as milliamps per volt (mA/V). In the example shown in Figure 6.11, the JFET's V_{DS} is held constant at 5 volts, while the I_D current's slope is measured between 5 and 8 mA, and 1 to 2 V_{GS} . This results in a g_{fs} of 3 mA/V or 3 mS. While transconductance depends on both the V_{DS} and the V_{GS} , it mostly depends on the latter. It is highest when V_{GS} equals 0, where I_{DSS} will be at its maximum, and lowest when V_{GS} equals $V_{GS(off)}$ and I_{DSS} equals 0. It also depends on chip area and gate oxide thickness. g_{fs} is specified on some data sheets with a minimum or maximum value; others specify only a typical value. Be aware how it is measured though. The g_{fs} value given in most manufacturers' data sheets is measured at full conduction (I_{DSS}), where g_{fs} is at maximum. Others also specify it with a particular V_{DS} and at a 1-KHz frequency.

Yet another important characteristic of the JFET is its *output impedance* (Z_{OUT}), which can range from a few ohms to more than a Meg ohm. This depends on the JFET's

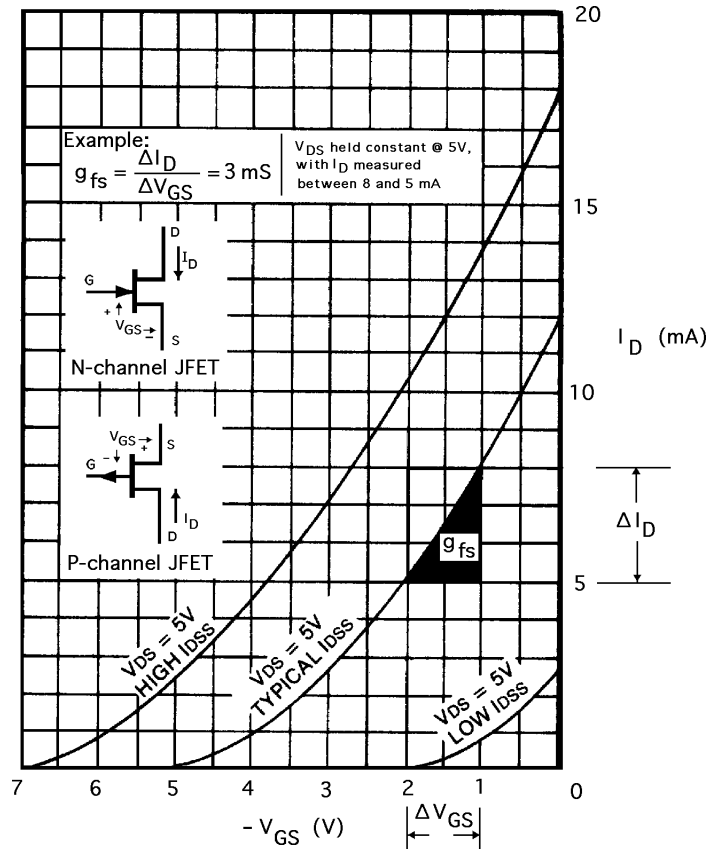


Figure 6.11. A JFET's transconductance (g_{fs}) characteristics.

gain (g_{fs}), input frequency, internal source resistance, and the value of the external source load resistor. This often just approximates to the value of its internal source resistance (r_s), compared with the value of the external source resistor (R_s), which is usually much larger. This internal source resistance forms a voltage divider with any external source load, such that:

$$r_s = \frac{1}{g_{fs}} \quad (\text{Eq.6.8})$$

and the output impedance is given by:

$$Z_{out} = \frac{r_s R_s}{r_s + R_s} \quad (\text{Eq.6.9})$$

where r_s is the JFET's internal source resistance; g_{fs} is the transconductance or gain; Z_{OUT} is the output impedance in ohms; and R_s is the value of the external source resistor. As an example, let's obtain an approximate value of output impedance for several popular N-channel JFETs, all with the same source resistance of 2.2 K Ω (Figure 6.12). Their typical g_{fs} specs are as follows:

$$2N\ 5434 = 17\ \text{mS}$$

$$2N\ 4867A = 1\ \text{mS}$$

$$2N\ 3819 = 5\ \text{mS}$$

$$2N\ 4416A = 6.5\ \text{mS}$$

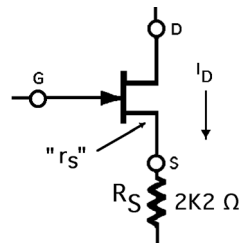


Figure 6.12. Example N-channel JFET used to calculate $Z_{(out)}$, the output impedance.

Using equations 6.8 and 6.9, the results are:

$$2N\ 5434 \quad r_s = 58.82\ \Omega; \quad Z_{OUT} = 57.5\ \Omega$$

$$2N\ 4867A \quad r_s = 1\ \text{K}\Omega; \quad Z_{OUT} = 688\ \Omega$$

$$2N\ 3819 \quad r_s = 200\ \Omega; \quad Z_{OUT} = 183\ \Omega$$

$$2N\ 4416A \quad r_s = 154\ \Omega; \quad Z_{OUT} = 143\ \Omega$$

As you can see, the output impedance is fairly close to the value of the internal source resistance, which in turn depends on the transconductance. We are going to cover two more important characteristics of the JFET shortly. These are the *output conductance* and the zero temperature coefficient. For now, though, we have probably covered the most important JFET basics.

6.3 Using the JFET as a current source

Another unique characteristic of JFETs, particularly in relation to current sources, is the extremely low output conductance (g_{os} , y_{os} , and $\text{Re}_{(y_{fs})}$) of some low-noise JFET

amplifiers, when operating in their saturation regions. Besides low-noise JFETs, other potential devices exist from the different types of JFET amplifiers and switches. This is shown in a table later in this chapter. Although most JFETs do not make good current sources, those with low conductance usually do. This applies equally to both N- or P-channel devices, although N-channel devices predominate. Conductance is a DC characteristic and the reciprocal of resistance where:

$$R = \frac{1}{G} \quad \text{and} \quad G = \frac{1}{R} \quad (\text{Eq.6.10})$$

(Ohms) (Siemens / mhos)

It follows then that a 100-Ω resistor has a conductance of 1/100th or 10 mS, while a 100-KΩ resistor has a conductance of 1/100th K or 10 μS.

In summary, the saturation region is the V_{DS} just above the pinch-off voltage (V_p), extending horizontally to just below the maximum voltage rating of the device, $V_{(BR)DSS}$, and vertically between the V_{GS} equals 0 and $V_{GS (off)}$ limits. Whenever the JFET is operated in this region, its output conductance is low (see Figure 6.13).

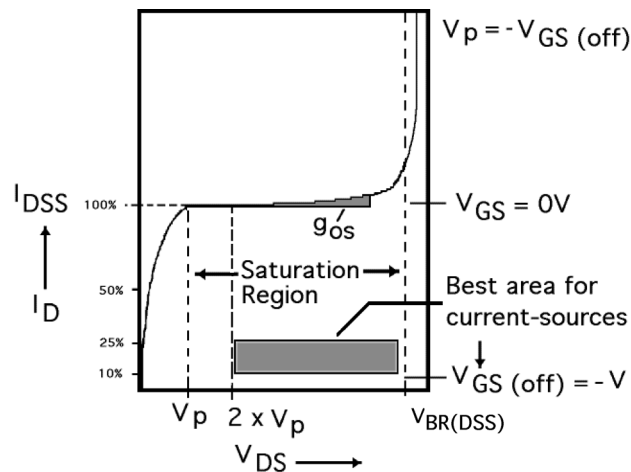


Figure 6.13. N-channel JFET output conductance (g_{0s}) characteristics.

The quality of the current regulation is strongly dependent on output conductance, though, which is in turn closely related to the drain current (I_D). The lower the drain current, the lower the conductance, and the better the regulation will be. Some JFETs have extremely low values of output conductance, often less than 10 μS (micro-Siemens), which make them excellent candidates as current sources (i.e., 2N 4338 = N-channel: $g_{0s} = 5 \mu S$ max, $V_{GS (off)} = -1 V$, $I_{DSS} = 0.6 mA$; 2N 4867 = N-channel: $g_{0s} = 1.5 \mu S$ max, $V_{GS (off)} = -2V$, $I_{DSS} = 1.2 mA$). Others have output conductance values in the

hundreds of micro-Siemens and higher, making them mostly unsuitable for use as current sources.

As previously stated, the JFET's maximum limiting current (I_{DSS}) occurs when the V_{GS} is at 0 volts, at a particular V_{DS} . Under these conditions, the output conductance will be at its maximum ($g_o = g_{os}$ at I_{DSS}). The simplest current source therefore can be made with the JFET's gate tied directly to its source, as shown in Figure 6.14. The circuit's output conductance (g_o) will be approximately equal to the g_{os} specs for that particular JFET. However, the overall performance using this configuration is poor, because the drain current will be at full conduction and will be whatever the I_{DSS} value of this particular JFET happens to be. This is not a very good solution, but analog IC makers often use this same configuration as part of their start-up bias circuitry, where only a current limit (rather than a current source or sink) is needed. So really this I_{DSS} configuration need only be considered here as a starting point.

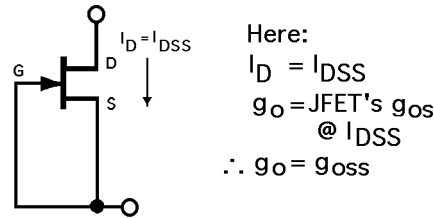


Figure 6.14. The simplest JFET current source uses the I_{DSS} value.

Actually the best regulation performance is obtained when using a JFET that is biased well below its I_{DSS} , at between say 5% to 33% of I_{DSS} . To accomplish that, a resistor is inserted into the source connection, to provide the necessary V_{GS} biasing (see Figure 6.15). At first glance this looks similar to a JFET source-follower circuit, but the gate is tied to the bottom end of the resistor (R_S), so that a feedback voltage controls the gate and establishes a state of equilibrium, keeping the current constant despite changes in drain voltage. The output conductance (g_{os}), which is a function of the operating point of the JFET, decreases linearly with I_D , because the JFET is biased closer to $V_{GS(off)}$. As a result, the circuit's output conductance (g_o) can be found by either of the following equations:

$$g_o = \frac{g_{os}^2}{1 + R_S(g_{os} + g_{fs})} \quad (\text{Eq.6.11})$$

$$g_o \approx \frac{g_{os}}{1 + R_S g_{fs}} \quad (\text{Eq.6.12})$$

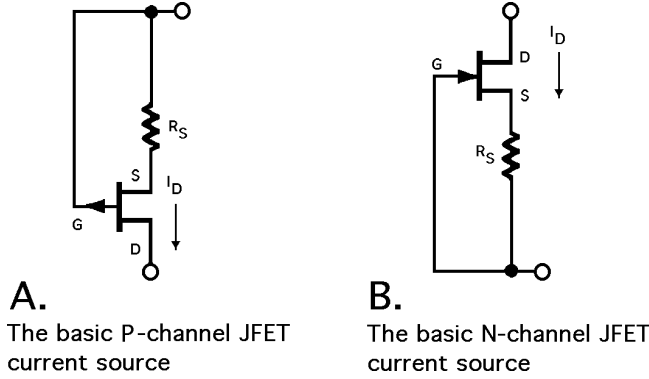


Figure 6.15. Basic Wilson current mirrors.

where g_{os} is the JFET's output conductance; g_{fs} is the value of its transconductance, and R_S is the value of the external source resistor.

Although the JFET may be self-biased to operate as a constant current source at any level below its saturation current (I_{DSS}), the lower the drain current, the tighter the regulation will be. The JFET will operate as a good current source whenever the V_{DS} is twice or more the value of the $V_{GS(off)}$. For values below two times $V_{GS(off)}$, conductance will be significantly higher and regulation will be degraded. Where $V_{GS(off)}$ and I_{DSS} are both known, then the approximate V_{GS} bias voltage for a particular drain current (I_D) can be found by the following:

$$V_{GS} = V_{GS(off)} \left(1 - \sqrt{\frac{I_D}{I_{DSS}}} \right) \quad (\text{Eq.6.13})$$

and also :

$$I_D = I_{DSS} \left[1 - \left(\frac{V_{GS}}{V_{GS(off)}} \right) \right]^2 \quad (\text{Eq.6.14})$$

The bias resistor (R_S) required between the gate and the source can be found by applying Ohm's law, so that:

$$R_S = \frac{V_{GS}}{I_D} \quad (\text{Eq.6.15})$$

As an example, if we assume these values:

$$I_D = 100 \mu\text{A}$$

$$I_{DSS} = 2.5 \text{ mA}$$

$$V_{GS} = -4 \text{ volt}$$

Then the value of R_S would be 40 K Ω .

A change in either the supply voltage or the load impedance will cause only a small change in current as a result of a low output conductance (g_{os}), and is shown by:

$$\Delta I_D = \Delta V_{DS} g_{os} \quad (\text{Eq.6.16})$$

In our example, if the particular JFET device had a g_{os} value of 50 μS , and a change in V_{DS} of 25 mV occurred, then the output current would change by 1.25 μA (1.25%). If we chose another device, having a significantly lower value of g_{os} (i.e., 5 μS), the same 25-mV change in V_{DS} would yield a change of only 0.125 μA (0.12%). In practical terms, because g_{os} can range from less than 1 μS to more than 500 μS , according to the JFET type, the dynamic impedance can be more than 1 M Ω to less than 2 K Ω , which corresponds to a current stability range of less than 1 $\mu\text{A/V}$ to more than 1 mA/V. In this example, the dynamic impedance is more than 200 K Ω .

In many current source applications, it may be necessary to bias the JFET at or near its *zero temperature coefficient point* (zero TC, TC0, or zero tempco). This is a unique point at which the drain current varies least (I_{DZ}), with changes in temperature (either large or small ΔT), and which provides added thermal and circuit stability. You can see an example of the zero TC point in Figure 6.16. Actually, I_{DZ} will change slightly from one device to another, because each device will have a slightly different value of saturation current (I_{DSS}), and I_{DZ} will change proportionally to that. The theoretical value of I_{DZ} can be found by:

$$I_{DZ} \cong I_{DSS} \left(\frac{0.63}{V_{GS(off)}} \right)^2 \quad (\text{Eq.6.17})$$

The necessary gate-to-source bias voltage for zero TC would then be:

$$V_{GS(0TC)} \cong V_{GS(off)} - 0.63V \quad (\text{Eq.6.18})$$

One will also need to determine the value of the JFET's source resistance (R_S), and one can do that by drawing a load-line from a convenient fixed reference point (i.e., 1 V and 1 mA = 1 K Ω), so that the load-line intersects as closely as possible with or near

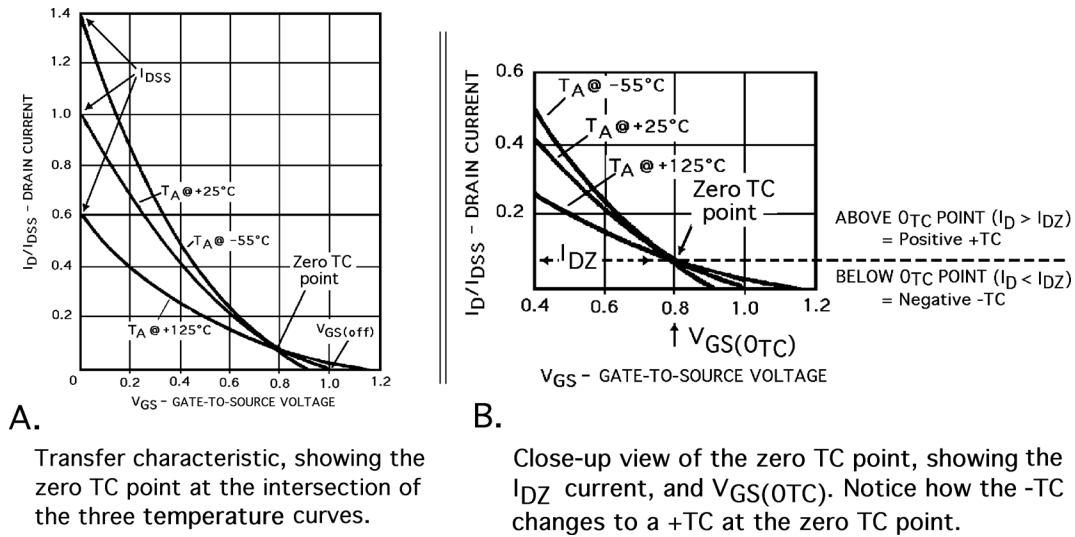


Figure 6.16. Examples of a JFET's Z_{TC} point.

the zero TC point, then back to the origin at 0. Where it intersects with the curves will determine the V_{GS} and I_D .

$$R_S(0TC) = \frac{V_{GS(0TC)}}{I_{DZ}} \quad (\text{Eq. 6.19})$$

Knowing where the zero TC point is allows one to tailor the circuit to have a positive tempco, by operating the drain current *above* I_{DZ} , or to have a negative tempco, by operating the drain current *below* I_{DZ} (see Figure 6.16B). Normally one will have to build a circuit, then test it under extended temperature conditions (in an accurate oven), logging the results on a graph. Once you have some data recorded and graphed, you can then compare it with your initial design calculations. This is not the kind of project one can do using SPICE models, which for JFETs are usually approximations at best.

As a design example, we will first determine the zero TC point for a 2N 4340 (a low-noise N-channel JFET), and then establish what the appropriate load resistor would be to keep the FET current source at that zero TC point. In this example, the JFET has a $V_{GS(off)}$ equals -1.5 volt, an I_{DSS} minimum equals 1.2 mA, and it is operated from a V_{DS} equals 10 volts. Looking at its transfer characteristic graph (Figure 6.17), we can visually confirm that the intersection of the three temperature curves (the zero TC point) occurs at approximately 0.84 volt and 0.2 mA. Using equations 6.17, 6.18, and

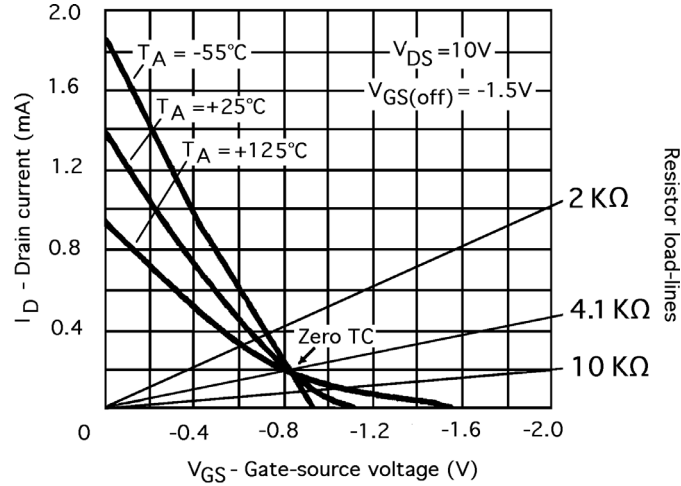


Figure 6.17. Example showing 2N4340 N-channel JFET's zero TC point and three load-lines.

6.19, we can determine from the $V_{GS(off)}$, I_{DSS} , and V_{DS} values given what the zero TC values for V_{GS} , I_{DZ} , and R_S are:

$$V_{GS(0TC)} \cong 1.5 - 0.63 = 0.87 \text{ V} \quad (\text{Eq.6.20})$$

$$I_{DZ} \cong 0.0012 \left(\frac{0.63\text{V}}{1.5\text{V}} \right)^2 = 212 \mu\text{A} \quad (\text{Eq.6.21})$$

$$R_{S(0TC)} = \frac{0.87\text{V}}{212 \mu\text{A}} = 4.1 \text{ K}\Omega \quad (\text{Eq.6.22})$$

Comparing the graph with the calculations, you will see that this is fairly close, although one should remember that $V_{GS(0TC)}$ and I_{DZ} are both *theoretical* (approximate) values, much as the reverse saturation current (I_S) is with the P-N junction. Looking at the three load-lines shown in Figure 6.17, the 2-K Ω load-line is too high and is above the zero TC point, thereby having a negative TC. It has an approximately 45-degree slope as it intersects with the three temperature curves and would drift about 80 μA over the temperature range, which is unacceptable. The 10-K Ω load-line is on the low side and is below the zero TC point, thereby having a positive TC. Although it has a more shallow slope, it would still drift about 25 μA . The 4.1-K Ω load-line intersects exactly at the zero TC point (4.1 K Ω) and would drift less than 5 μA , over the full military temperature range. We can also determine from the data sheet the approximate output conductance from the device's "Output Conductance vs. Drain Current" graph. This shows that for a drain current of approximately 0.2 mA (with V_{GS}

(off) equals -1.5V , I_{DSS} minimum equals 1.2 mA , and V_{DS} equals 10 volts), over the military temperature range the output conductance varies between 0.3 and $0.4\text{ }\mu\text{S}$. This would give a dynamic impedance of more than $2.5\text{ M}\Omega$. From an adjacent data sheet graph for the 2N 4340, we can see that the noise voltage is in fact greater than $8\text{ nV}/\text{Hz}$ at 1 KHz .

All of this is based on creating a current source whose output current is at the zero TC point. This should illustrate, however, that in choosing a JFET and knowing the desired output current, it is most helpful in the design process to visually determine where the zero TC point is. It helps further if you look at devices that are fully characterized and with supporting graphs. This way you will not waste time looking at unsuitable devices. Unfortunately, that is not always possible, so the following reference charts (see Tables 6.1 and 6.2) have been compiled as a further aid to you.

V_{GS(off)}: (V)	1V	1.25V	1.5V	2V	2.5V	3V	3.5V	4V	4.5V	5V	6V	8V	10V
IDSS: (mA) 0.1	0.37V 39 μA	0.62V 25 μA	0.87V 17.6 μA	1.37V 10 μA	1.87V 6.35 μA	2.37V 4.4 μA	2.87V 3.2 μA	3.37V 2.5 μA	3.87V 1.96 μA	4.37V 1.58 μA	5.37V 1.1 μA	7.37V 0.62 μA	9.37V 0.39 μA
0.5	0.37V 200 μA	0.62V 127 μA	0.87V 88 μA	1.37V 50 μA	1.87V 32 μA	2.37V 22 μA	2.87V 16.2 μA	3.37V 12.4 μA	3.87V 9.8 μA	4.37V 7.9 μA	5.37V 5.5 μA	7.37V 3.1 μA	9.37V 1.98 μA
1	0.37V 400 μA	0.62V 254 μA	0.87V 176 μA	1.37V 99 μA	1.87V 63 μA	2.37V 44 μA	2.87V 32.4 μA	3.37V 25 μA	3.87V 19.6 μA	4.37V 15.8 μA	5.37V 11 μA	7.37V 6.2 μA	9.37V 3.96 μA
2	0.37V 793 μA	0.62V 508 μA	0.87V 352 μA	1.37V 198 μA	1.87V 127 μA	2.37V 88 μA	2.87V 64 μA	3.37V 50 μA	3.87V 39 μA	4.37V 31.7 μA	5.37V 22 μA	7.37V 12.4 μA	9.37V 7.93 μA
2.5	0.37V 992 μA	0.62V 635 μA	0.87V 441 μA	1.37V 249 μA	1.87V 158 μA	2.37V 110 μA	2.87V 81 μA	3.37V 62 μA	3.87V 49 μA	4.37V 39.6 μA	5.37V 27.5 μA	7.37V 15.5 μA	9.37V 9.92 μA
3	0.37V 1.2 mA	0.62V 762 μA	0.87V 529 μA	1.37V 298 μA	1.87V 191 μA	2.37V 132 μA	2.87V 97 μA	3.37V 74.4 μA	3.87V 58.8 μA	4.37V 47.6 μA	5.37V 33 μA	7.37V 18.6 μA	9.37V 11.9 μA
4	0.37V 1.58 mA	0.62V 1.01 mA	0.87V 705 μA	1.37V 397 μA	1.87V 254 μA	2.37V 176 μA	2.87V 129 μA	3.37V 99 μA	3.87V 78 μA	4.37V 63.5 μA	5.37V 44 μA	7.37V 24.8 μA	9.37V 15.8 μA
5	0.37V 2 mA	0.62V 1.27 mA	0.87V 882 μA	1.37V 496 μA	1.87V 317 μA	2.37V 220 μA	2.87V 162 μA	3.37V 124 μA	3.87V 98 μA	4.37V 79 μA	5.37V 55 μA	7.37V 31 μA	9.37V 19.8 μA
10	0.37V 4 mA	0.62V 2.54 mA	0.87V 1.76 mA	1.37V 1 mA	1.87V 635 μA	2.37V 441 μA	2.87V 324 μA	3.37V 248 μA	3.87V 196 μA	4.37V 159 μA	5.37V 110 μA	7.37V 62 μA	9.37V 39.6 μA
25	0.37V 10 mA	0.62V 6.35 mA	0.87V 4.41 mA	1.37V 2.48 mA	1.87V 1.58 mA	2.37V 1.1 mA	2.87V 810 μA	3.37V 620 μA	3.87V 490 μA	4.37V 397 μA	5.37V 275 μA	7.37V 155 μA	9.37V 99 μA
50	0.37V 20 mA	0.62V 12.7 mA	0.87V 8.82 mA	1.37V 4.96 mA	1.87V 3.17 mA	2.37V 2.2 mA	2.87V 1.62 mA	3.37V 1.24 mA	3.87V 980 μA	4.37V 794 μA	5.37V 551 μA	7.37V 310 μA	9.37V 198 μA
75	0.37V 29.7 mA	0.62V 19 mA	0.87V 13.2 mA	1.37V 7.44 mA	1.87V 4.76 mA	2.37V 3.3 mA	2.87V 2.43 mA	3.37V 1.86 mA	3.87V 1.47 mA	4.37V 1.19 mA	5.37V 826 μA	7.37V 465 μA	9.37V 297 μA
100	0.37V 39.7 mA	0.62V 25.4 mA	0.87V 17.6 mA	1.37V 9.92 mA	1.87V 6.35 mA	2.37V 4.4 mA	2.87V 3.24 mA	3.37V 2.48 mA	3.87V 1.96 mA	4.37V 1.58 mA	5.37V 1.1 mA	7.37V 620 μA	9.37V 397 μA

NOTES:

1. Select the nearest $V_{GS(off)}$ for your JFET along the top horizontal axis, then select the nearest $IDSS$, from the left vertical axis. Where that column and row intersect, read off the resulting $V_{GS(OTC)}$ and IDZ values.
2. Alternatively, select the nearest $V_{GS(OTC)}$ and IDZ combination from within the cells, then read the corresponding vertical $V_{GS(off)}$ and horizontal $IDSS$ values.
3. These values are approximate only.

Table 6.1 $V_{GS(OTC)}$ and IDZ calculator

Table 6.1 allows you to quickly determine the corresponding $V_{GS(OTC)}$ and I_{DZ} values for many combinations of $V_{GS(off)}$ and I_{DSS} . You can also use this in reverse, so that you can find the corresponding $V_{GS(off)}$ and I_{DSS} values for various combinations of $V_{GS(OTC)}$ and I_{DZ} . Remember these are approximate values only, but they should be close enough.

Table 6.2 allows you to quickly determine a suitable device and includes the most important characteristics as far as potential JFET current sources are concerned. This table lists various N-channel devices with a $V_{GS(off)}$ value of less than -3.6 volts and P-channel devices with a $V_{GS(off)}$ value of less than $+4.1$ volts. These are mostly low-noise devices from 10 different manufacturers, and all with low values of output conductance (g_{os} less than $80 \mu S$). Both tables are easy to use and should save you some time, by revealing either the approximate values or a commonly available device you may need in your design.

Manufacturers and circuit designers commonly portray a product's characteristics by using the temperature coefficient as either a percentage or in parts per million. In relation to a current source, the temperature coefficient of the output current ($\alpha I_{O(TC)}$) is the ratio of change in output current to the change in temperature (e.g., $20^\circ C$ to $85^\circ C$). This is usually expressed as a *percentage* (%) of the output current (i.e., 0.0015%), and is the average value for the total temperature change. You can determine the tempco from your data by the formula in equation 6.23:

$$\alpha I_{O(TC)} = \pm \left(\frac{I_o @ T_2 - I_o @ T_1}{I_o @ 25^\circ C} \right) \left(\frac{100\%}{T_2 - T_1} \right) \quad \text{Eq.6.23}$$

For example, some current measurements gave us the following results: I_o at $25^\circ C = 502 \mu A$; I_o at $20^\circ C = 500 \mu A$; I_o at $85^\circ C = 512 \mu A$. The temperature range of interest is $+20^\circ C$ to $+85^\circ C$. Using equation 6.23 would yield:

$$\left(\frac{512 \mu A - 500 \mu A}{502 \mu A} \right) \left(\frac{100}{65} \right) = 0.03677\% \quad \text{Eq.6.24}$$

You can also express the tempco as a value in *parts per million per degree Celsius* (ppm/ $^\circ C$), by using the formula in equation 6.25:

$$\alpha I_{O(TC)} = \left(\frac{I_o @ T_2 - I_o @ T_1}{I_o @ 25^\circ C} \right) \left(\frac{1 \times 10^6}{T_2 - T_1} \right) \quad \text{Eq.6.25}$$

In the previous example, the output current's tempco could also be expressed as $368 \text{ ppm}/^\circ C$, suggesting an accurate current source.

Part #:	N / P type:	V _{gs(off)} max: V	V _{BR(gss)} min: V	I _{ds} mA min:	G _{os} typ μ S:	G _{fs} typ mS:	Typ. equiv. noise: nV/Hz	Pkg:	Manufacturers:
2N 3574	P	2	25	-0.15	10	0.2		TO-72	Sol
2N 3575	P	4	25	< -1	20	0.3		TO-72	Sol
2N 3578	P	4	20	-1	15	1.2		TO-18	Sol
2N 3685/A	N	- 3.5	-50	1	25	2		TO-72	Sol
2N 3686/A	N	- 2	-50	0.4	10	1.5		TO-72	Sol
2N 3687/A	N	- 1.2	-50	1.2	5	1		TO-72	Sol
2N/MPF 3821	N	- 2	- 50	0.5	10	3	100	TO-72	IF, ON
2N/PN/FN/SST/LS/MMBF 4117/A	N	- 1.8	- 40	0.09 mA	3 μ S	0.08 mS	1.5 nV	TO-18/TO-72/SOT-23	C, F, IF, LIS, Sol, VS
2N/PN/FN/SST/LS/MMBF 4118/A	N	- 3	- 40	0.24 mA	3 μ S	0.15 mS	1.5 nV	TO-18/TO-72/SOT-23	C, F, IF, LIS, Sol, VS
2N 4338	N	- 1	- 30	0.2	5	0.5	6	TO-18/TO-72	C, CS, IF, Sol, VS
2N 4339	N	- 1.8	- 50	0.5	15	2	6	TO-18	C, CS, IF, LIS, Sol, VS
2N 4340	N	- 3	- 50	1.2	30	2.5	6	TO-18	C, CS, IF, Sol, VS
2N/PN/SST 4393	N	- 3	- 40	5 mA	25 μ S	6.0 mS	3.0 nV	TO-18/92/SOT-23	Ph, VS
2N 4867/A	N	- 2	- 40	0.4	1.5	1	3	TO-18/TO-72	IF, Sol, VS
2N 4868/A	N	- 2	- 40	1	1.5	2	6	TO-72	IF, LIS, Sol
2N 5020	P	1.5	25	- 0.3	20	3		TO-18	CS, IF, Sol
2N 5021	P	2.5	25	- 1	20	4		TO-18	IF, Sol
2N 5116	P	4	30	- 5	20	4.5	20	TO-18	CS, Ph, VS
2N 5265	P	3	60	-0.5	75	1		TO-72	Sol
2N 5266	P	3	60	-0.8	75	1.5		TO-72	Sol
2N 5358	N	- 3	- 40	0.5	10	2		TO-72	Sol
2N/SST/MMBF 5484	N	- 3	- 25	1 mA	50 μ S	4.0 mS	10 nV	TO-92/SOT23	C, CS, F, Ph, VS
2N 5716	N	- 3	- 40	0.05	25	1		TO-92	Sol
2N 6451/2	N	- 3.5	- 20	5	50	20	5	TO-72	IF
2N 6550/CM 860	N	- 3	- 20	10	50	40	10	TO-46/TO-72	Cr
CM 697	N	- 3	- 25	30				TO-46	Cr
J 113A	N	- 3	- 35	8	25	6	4	TO-92	F, IF, LIS, ON, Ph, VS
J/MMBFJ/SST 177	P	4	30	-1.5	20	4.5	20	TO-92/SOT-23	C, F, IF, LIS, ON, Ph, Sol, VS
J/SST/MMBF J 201	N	- 1.5	- 40	0.2	1	0.5	6	TO-92/SOT-23	C, F, IF, LIS, ON, Sol, VS
J 230	N	- 3	- 40	0.7	1.5	2	8	TO-92	IF
J305	N	- 3	- 30	1	30	3	10	TO-92	VS
KK 3685	N	- 3.5	-50	1	25	2		TO-92	Sol
KK 3686	N	- 2	-50	0.4	10	1.5		TO-92	Sol
KK 3687	N	- 1.2	-50	0.1	5	1		TO-92	Sol
KK 4304	N	- 1	- 30	0.5	50	1		TO-92	Sol
KK 5033	P	2.5	20	-0.3	20	5		TO-92	Sol

MANUFACTURERS' KEY:

C = Calogic; CS = Central Semi; Cr = Crystallonics; F = Fairchild Semi; IF = InterFet; LIS = Linear Int. Systems; ON = ON Semi; Ph = Philips Semi; Sol = Solitron Devices; VS = Vishay-Siliconix.

* NOTE: Table shows both P-channel, and N-channel JFET devices with low $V_{gs(off)}$. N-ch. are < 3.6V, and P-ch. are < 4.1V. All are low g_{os} < 80 μ S devices.

Table 6.2 Low G_{os} and low $V_{gs(off)}$ single JFETs

In summary, the lower the drain current and the lower the output conductance, then the tighter the regulation will be. The closer the source resistor load-line intersects the zero TC point, the less the current source will drift over the intended temperature range, and the more stable and reliable your circuit will be. You can determine just how accurate your current source is by applying equations 6.23 and 6.25.

As another design example, let's create a simple JFET current source, in some easy steps. We can use the following checklist (see Table 6.3) to aid in our search for the best device(s) for the design. While the column headings are self-explanatory, the one titled "0_{TC} point" allows you to record the approximate $V_{GS(0TC)}$ and I_{DZ} values from the data sheet transfer characteristic graphs.

Manufacturer:	Part No.:	Pkg:	N or P type:	I_{DSS} min/ max: (mA)	$V_{GS(off)}$ min/ max: (V)	$V_{BR(dss)}$ min/ max: (V)	G_{os} typ: (μS)	0 _{TC} point @ V_{GS} and I_{DZ} : (V/mA)

Table 6.3 JFET Current Source Design Check List

1. Determine (1) the desired constant current level, (2) the supply voltage, (3) the load requirements, and (4) current regulation necessary for your circuit, together with the applicable $\pm\%$ tolerances. (Current regulation is usually expressed as a percentage, as in this example: $I_D = 200 \mu A$, tolerance = 1% = $2 \mu A$).

$$\left(\frac{2\mu A}{200\mu A} \right) \times 100\% = 1\% \text{ regulation} \quad (\text{Eq.6.26})$$

2. Does the design involve limited space or other mechanical constraints? This may apply to what kind of JFET package would best suit your design: TO-18, TO-92, SOT-23 (SMD), etc.
3. What polarity of JFET, N-channel, or P-channel will be required?
4. Make the constant current/drain current (I_D) less than 33% of I_{DSS} max. The lower the I_D , the tighter the regulation will be.
5. Either pick a device from the listing in Table 6.2, low G_{OS} and low $V_{GS(off)}$, or look through a JFET catalog. Pick a device with an appropriate I_{DSS} value. Record this data on the checklist.
6. Now choose a device with a $V_{GS(off)}$ that matches your design (negative value $-V_{GS(off)}$ for N-channel devices, or a positive value $+V_{GS(off)}$ for P-channel devices). Record this data also on the checklist.
7. In your circuit, ensure that the JFET's V_{DS} is two times or more the value of the $V_{GS(off)}$, or else if V_{DS} is less than $V_{GS(off)}$, the JFET will fall out of saturation. Determine both the *minimum* and *maximum* supply voltage (V_{DS}) across the JFET. Is the maximum supply voltage less than its breakdown voltage? Remember too that the voltage compliance across the JFET is from $V_{GS(off)}$ to its breakdown voltage $V_{(BR)GSS}$.
8. Next pick a suitable low g_{OS} device (with a low-noise value, e.g., less than 25 nV/Hz) from the listing in Table 6.2 or from a JFET catalog. Record this data on the checklist.
9. You should now have recorded a short list of possible devices.
10. This step involves looking at the graph of the transfer curve (I_D vs. V_{GS}) for each JFET on your checklist. Look at either the printed data sheet graph or the associated PDF file, if downloaded from a Web site. If a chosen device does *not* show a transfer curve, then you should move down the list and find another one that does. As shown previously, the transfer curve is a *very important* element in the design sequence, because it allows one to physically see just how close one's intended design is going to be in relation to the zero TC point. A zero TC means that there will be virtually no change or drift in the current through the JFET, over the intended temperature range. This is an ideal situation and should be one's goal (see Figures 6.16 and 6.17). From the JFET's transfer curve, record the approximate $V_{GS(0TC)}$ and I_{DZ} values in the checklist's right-hand column labeled zero TC point.
11. Relative to the zero TC point, see where your desired current level (in μA or mA) occurs (above it yields a negative TC, while below it yields a positive TC).

12. Draw a resistor load-line on the graph that intersects at the V_{GS} value arrived at in steps 6 and 7, and at your desired current level. Ideally the load-line should be close to or intersect with the zero TC point. If not, try another device where this happens, or consult Table 6.1 for an approximate value of $V_{GS(0TC)}$ and I_{DZ} . If the intersect point is *not* close to the zero TC point, the current source will drift with temperature.
13. Determine the value of the JFET's source resistor (R_S). Make sure that you use a metal-film type, or a precision wirewound resistor, and that its tolerance (e.g., $\pm 0.1\%$, $\pm 0.01\%$), wattage rating ($P_{diss} = V_{drop} \times I_D$), and tempco are all within your design limits. The tempco should be as low as possible, so that it does not degrade your circuit (i.e., $\pm 0.001\% = 10 \text{ ppm}/^\circ\text{C}$), and it should have a low thermal resistance (higher power rating than needed).
14. Build and double-check your circuit's connections, *before* applying power.
15. Now test the circuit, and after some initial evaluation, decide whether you need to adjust the current level, and thereby change the value of R_S . You should test the performance of the circuit by changing the value of V_{DS} and noting any change in drain current (ΔI_D). You will probably need to graph the results. You may decide that over the intended temperature range, the circuit requires a change in its tempco. You can determine what the circuit's tempco is in $\text{ppm}/^\circ\text{C}$ or as a percentage by using equations 6.23 and 6.25. By employing the techniques previously discussed, you can design the circuit to compensate for the load or following circuitry, by having either a positive, a negative, or even a zero tempco.
16. Once you have implemented your modifications, you should retest the circuit over the intended temperature range. Recalculate the new tempco, and see how that has changed.
17. Build a duplicate circuit, but now using the same modifications you made previously. How close is its performance to the prototype built in steps 1 to 17? You may need to average the value of R_S for a mass-production situation.

6.4 The JFET cascode current source

Although performance is good using just one FET, even better regulation can be achieved by using two N-channel JFETs in a *cascode* configuration, as shown in Figure 6.18B. Cascoding improves high-frequency operation, provides even greater output impedance (Z_{out}), increases high-voltage operation and compliance, and reduces output conductance. In this circuit, cascoding buffers the current source Q_1 from the load, by using Q_2 . This means that while the source voltage of Q_2 remains constant, variations in the load voltage are accommodated by Q_2 's drain. As a result, the voltage

drop across the current source remains constant. Here the drain current (I_D) is regulated by Q_1 and R_S , so that effectively V_{DS1} equals $-V_{GS2}$. The current source is set up as previously discussed. Both JFETs must be operated with adequate V_{DG} , so that V_{DG} is ideally more than twice $V_{GS(off)}$, or else the circuit's output conductance will increase significantly. JFET Q_2 needs to have a higher $V_{GS(off)}$ than Q_1 . R_S sets the desired current, as previously discussed, but in early development it could be substituted by a multiturn potentiometer. This would allow easy adjustment of the desired current level and could range from a few μA to several milliamps.

In the cascode circuit shown in Figure 6.18B, it provides an internal circuit impedance of more than $10\text{ M}\Omega$ at current levels less than 1 mA . It can be used equally well in circuits of more than 40 volts or down to about 6 volts , depending on one's exact choice of $V_{GS(off)}$. Capacitor C_1 is just included for circuit stability. This inexpensive four-component circuit can be used as either a precision current source or sink, because the load can be connected to either terminal. Even lower g_{os} for the same current is achieved by the cascode, because of degenerative feedback, and the circuit's lower output conductance (which in turn is caused by the combined forward transconductance). Here the circuit's output conductance (g_o) is much less than the g_{os} of the single JFET circuit (Figure 6.18A)—about a *hundred* times lower. (This is proven by the two equations included in the figure.) You can also expect the cascode circuit's output impedance to be more than $10\text{ M}\Omega$. Regulation is about 100 times better, as shown in Figure 6.18C; notice the really sharp knee versus the softer knee of the single JFET's curve.

Using JFETs such as 2N4340/41 in the cascode circuit guarantees extremely low noise, typically less than $10\text{ nV}/\text{Hz}$. For low-voltage and low-current applications, consider using these N-channel devices: 2N4118 ($V_{GS(off)max}$ equals -1.8 volt and I_{DSSmax} equals 0.09 mA); 2N4119 ($-3\text{ volt}/0.24\text{ mA}$); 2N4338 ($-1\text{ volt}/1.5\text{ mA}$); 2N4339 ($-1.8\text{ volt}/0.6\text{ mA}$); 2N4867 ($-2\text{ volt}/3\text{ mA}$); J202 ($-1.5\text{ volt}/1\text{ mA}$). For low voltages around, say, 3.6 volts , one could probably use a combination of 2N4338 and 4339, and below that, around, say, 2.25 volts , a single current source using a 2N4338 can provide a good solution. Selecting devices might be necessary in certain situations, where a lower actual $V_{GS(off)}$ might be required, thus leading to lower voltage operation down to about 1.5 volts . A few low-voltage P-type devices also exist that include J201 ($2.25\text{ volt}/20\text{ mA}$), 2N3574 ($2\text{ volt}/0.38\text{ mA}$), 2N5265 ($3\text{ volt}/1\text{ mA}$), 2N5266 ($3\text{ volt}/1.6\text{ mA}$), and KK5053 ($2.5\text{ volt}/3.5\text{ mA}$), although none provide as low a voltage as the N-channel JFETs previously noted.

In some instances, you may be tempted to use a JFET *matched-pair* instead. However, monolithic matched-pairs are only available as N-channel devices and are usually more expensive. Although thermal tracking is excellent (because both devices share the same substrate), in most cases overall performance is *not* as good as when using two discrete N-channel devices. One should definitely *avoid* monolithic pairs, in which two intrinsic diodes are formed in manufacture (such as U401, U421, 2N3598, 2N5196, SST440/1), because some biasing schemes may inadvertently forward-bias

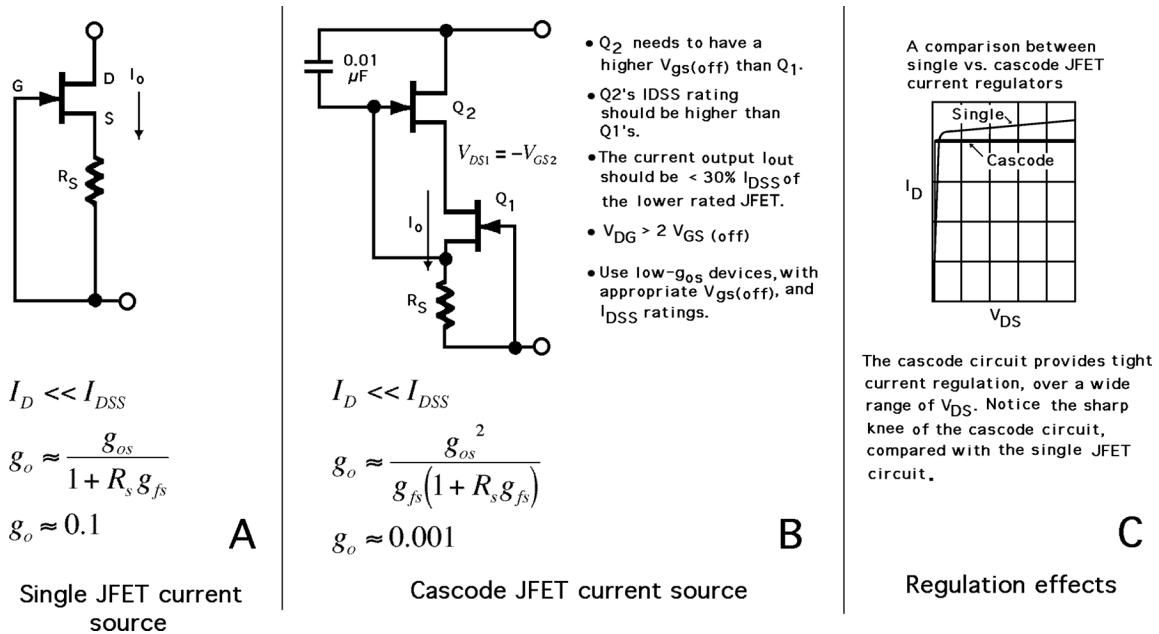


Figure 6.18. Comparing the single and cascode JFET current source.

one of these diodes. You may even be tempted to use a two-chip *matched-pair*, such as U440/1 (V_{GS (off)} equals 6 volts, I_{DSS} equals 30 mA); 2N5564/5/6 (−3 volts/30 mA); 2N5911/2 (−5 volts/40 mA). However, you should consider that both JFETs will have very close specs, because they were designed for differential-pair/front-end amplifier tasks (as shown later in Figure 6.29). This would not work well for a JFET cascode current source, because the upper device—the cascode—needs both a higher V_{GS (off)} and a higher I_{DSS} than the lower one—the current regulator.

Alternately, they may have too close a V_{GS (off)}, which could also cause circuit problems. Even if you hand-selected devices for your lab prototypes or preproduction circuits, if the devices were unwittingly reversed during assembly at the circuit board level, it could prevent proper current regulation and your overall circuit from functioning properly. Using *two* separate devices will always yield the best performance, and these are easily implemented in either through-hole or surface-mount devices. Even a single JFET current source will be a better, safer, more reliable current source than a *mis-matched* matched-pair. In fact, the only time to consider a dual or matched-pair would be if you needed *two* separate, *single* JFET current sources in the same circuit. Each would work equally well as any of the single JFET current sources described.

Some circuit examples of discrete JFETs being used as current sources are shown in Figure 6.19. Circuit A shows a pair of JFET current sources: one N-channel, the other

P-channel. The N-channel example is adjustable over a 500- μ A range. However, while convenient, the tempco of the potentiometer will degrade the overall performance. Once the desired setting has been determined, one should replace the potentiometer with a good-quality, low-tempco, low-tolerance (0.1%) metal-film resistor. The P-channel JFET provides a fixed current with good performance, using just two parts, which could both be tiny surface-mount components.

Circuit B shows a fixed 2-mA cascode current source, which can provide better than 300-ppm regulation, with an output impedance of more than 5 M Ω . The circuit shown uses two Crystallonics TO-46 metal-can devices. The circuit's output conductance is probably lower than 1 μ S.

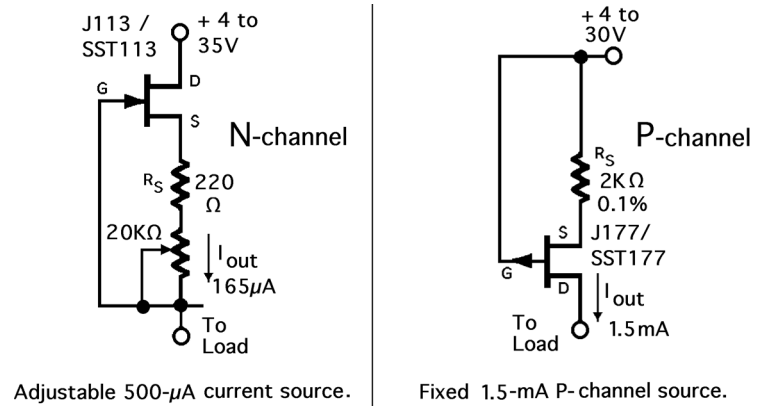
Circuit C combines a JFET cascode together with a high-quality monolithic precision voltage reference. The reference IC keeps Q_1 's V_{GS} constant over a wide temperature span, to create a high-quality current source with less than 50-ppm regulation. The output current is set by the reference voltage output divided by the value of the precision resistor (a 0.1% or better tolerance and less than 50-ppm metal-film type). The addition of the voltage reference also improves overall temperature stability and boosts output impedance to about 1 G Ω .

One or two additional JFET current source circuits are shown in this book, which may be helpful in your designs. One example is the JFET-DMOS cascode current source circuit shown in Chapter 7's Figure 7.11, which allows a much higher voltage range (5–450 volts) than an all-JFET cascode. Another can be seen in Figure 15.35 of chapter 15, which shows some ultra high-precision current sources using Intersil's state-of-art FGA™ voltage references.

6.5 JFET current regulator diodes

The current regulator diode (CRD) is equivalent to the single JFET current source, as depicted in Figure 6.20, but it is fully monolithic, with its geometry specially designed and enhanced for precise current regulation. The electronic symbol for the JFET CRD is shown on the right.

JFET current regulators were first introduced in the late 1960s, and they have been popular and readily available ever since. Major vendors at the time included Siliconix, Motorola Semiconductors, Teledyne-Crystallonics, and Fairchild Semiconductor. Many of the devices were granted MIL-classification (JAN, JAN-TX, etc.) and were part of a vendor's MIL product portfolio. However, in the late '80s and early '90s, there were numerous cuts in U.S. military programs, and as a result some vendors either sold off parts of their MIL business or discontinued manufacture of many discrete MIL product lines. For that reason, neither Fairchild Semiconductor nor ON Semiconductor (formerly Motorola's discretes division) makes CRDs today, although they pioneered them long ago. CRDs are still popular and readily available in the United States from the following major sources:



A. Single JFET current sources.

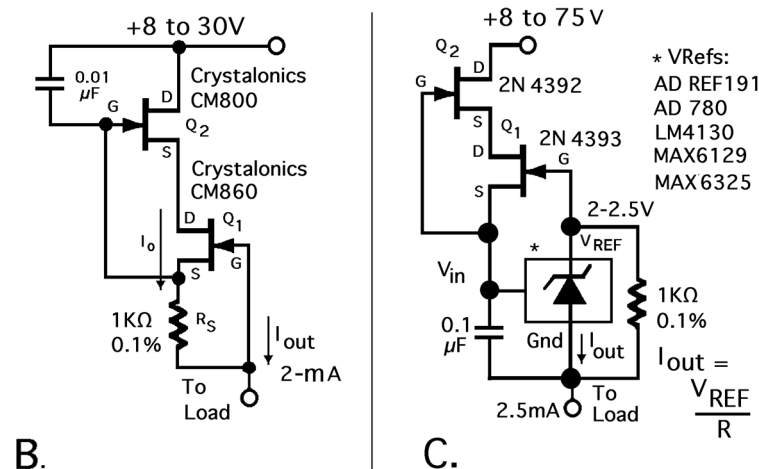


Figure 6.19. Examples of JFET current sources.

- Calogic
- Central Semiconductor
- Crystalonics
- InterFET
- Linear Integrated Systems
- Microsemi
- Solitron Devices
- Vishay-Siliconix

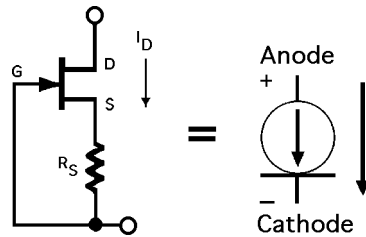


Figure 6.20. JFET current regulator diode: its symbol and equivalent circuit.

6.5.1 Characteristics of the CRD

JFET CRDs do not generally reflect as high a degree of accuracy or regulation as the JFET cascode circuit looked at previously. However, CRDs do remain attractive solutions to many current source applications. This is particularly true where volume production or limited circuit board space is involved. Being a single-component solution, the CRD saves design and purchasing time, incoming Q&A, inspection, and part-by-part selection, as well as having to manage and inventory several different components.

Besides being a low-cost item, a CRD has a fixed current level, a high output impedance, and low noise. Two other important benefits include a small two-lead package and a specified low temperature coefficient. The latter is a major advantage over the single or cascode JFET current sources that we looked at previously, because there one has to spend a significant amount of design time in determining the magnitude and polarity of the tempco and other drift characteristics, in relation to the JFET's zero TC point. Additionally, CRDs usually have a higher voltage rating than most JFETs, in many cases more than 100-volt rating. (Note: An average of the $V_{(BR)GSS}$ voltage rating of the many low- g_{OS} devices listed in Table 6.2 was approximately 38 volts.) Determining exactly which CRD to use is much the same procedure as when designing in and specifying a zener diode or a resistor. Once you have determined the necessary wattage and the current value with its associated tempco, you are ready to order the part(s). Each CRD has an assigned part number, like a zener diode, so it is easy to use. A drop-in replacement will function almost identically (remember that each CRD has a $\pm$ tolerance on its current rating).

CRDs are monolithic two-terminal devices, specially designed for precise current regulation. This is achieved by modifying their internal structure, thus creating the equivalent of an internal resistor at the JFET's source (see Figure 6.21A). This internal bulk-source resistance sets the output current. The gate and source are connected together by metallization. The structure's equivalent can be described by either one of two models. The more popular model (Figure 6.21B) is a current generator in series with the parallel combination of an impedance and a capacitance. The second model (Figure 6.21C) is an older model and is of a current generator in parallel with a capacitance and a conductance. Some devices are further enhanced for higher voltage or

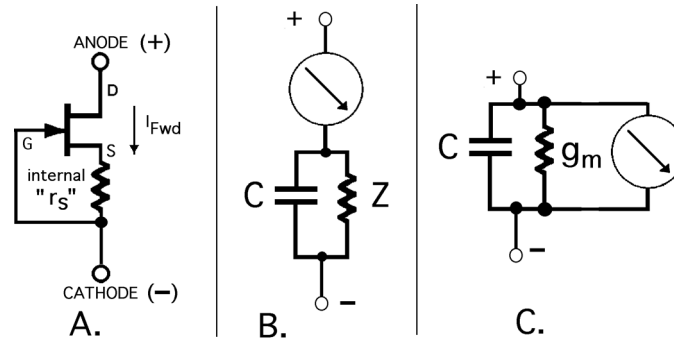


Figure 6.21. CRD equivalent circuits.

higher current operation (like some Crystallonics products, which can provide up to 50-mA constant current). Others are able to provide precise current regulation at very low voltages.

In fact, a somewhat overlooked feature of some of these devices is their ability to work down to approximately 1 volt. In Figure 6.22, you will notice that there are several devices in this example, which operate around the 1 volt at 1 mA level or less (there are others too not shown). In today's world, where an increasingly mobile society requires cell phones, digital cameras, MP-3 music players, pods, handheld PCs, and laptops, this unique low-voltage feature is attractive to manufacturers of battery-powered equipment, consumer items, and portable instrumentation.

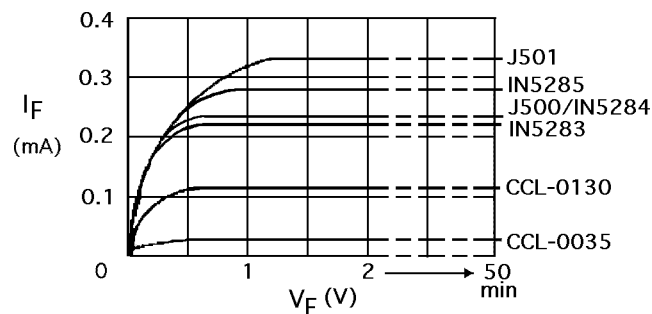


Figure 6.22. Ultra-low-voltage operation with current regulator diodes.

Being a two-electrode device, the CRD meets the industry standard for being a type of diode; in fact, the JEDEC prefix of "1N" confirms that (e.g., 1N5290). As a result, JFET terminology no longer applies, and diode terminology is used instead. Examples include *anode* instead of *drain*, *cathode* instead of *source*, *peak operating voltage*

instead of $V_{(BR)GSS}$, *forward current* (I_F) instead of drain current (I_D), and so on. We will briefly review some of the CRD's characteristics here, many of which are shown in Figure 6.23.

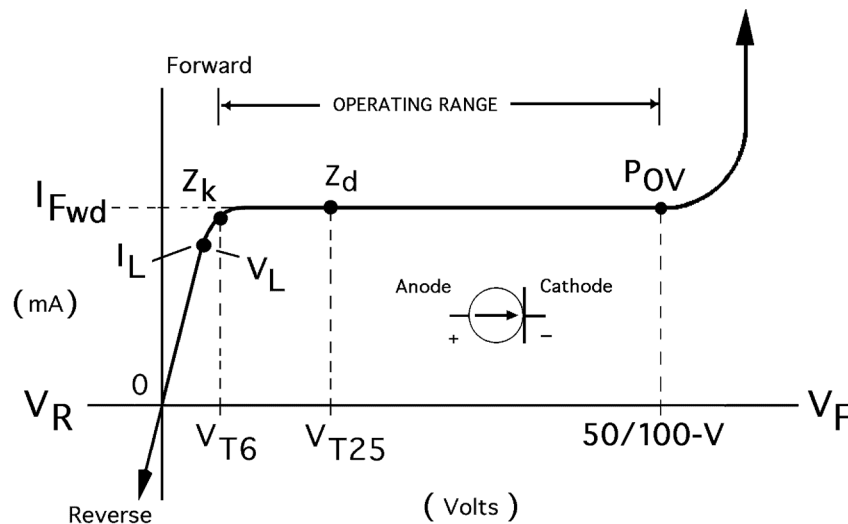


Figure 6.23. The current regulator diode's V-I characteristic curve.

The *peak operating voltage* (POV) simply refers to the maximum voltage that can be applied to the CRD, at 25°C room temperature. The POV is shown in Figure 6.23, and for many devices is 50 volts; others are rated at 100 volts. (Some very-high-current devices have a low POV, less than 30 volts.) Above the POV limit lies the uncharted and potentially dangerous breakdown region (i.e., the CRD might work fine, or it might self-destruct). The POV is usually specified at the maximum regulated current, with an added 10% higher safety margin. Manufacturers additionally specify a *typical* value of POV, which is often 50% higher, but this value is neither guaranteed nor tested. To be safe you should use the minimum POV value, which is guaranteed. In high-voltage applications, it is common to connect two or more CRDs in series, where the combined POV value of each makes up the total effective POV (as shown in Figure 6.24). In some applications, it may be necessary to include voltage-balancing resistors. Their values should be high (more than 100 K Ω each), because they effectively shunt the output resistance. Each CRD should be paralleled by a resistor, as shown in Figure 6.24. A similar technique, known as *current balancing*, is sometimes used when paralleling zener diodes.

Manufacturers refer to the minimum operating voltage as the *limiting voltage* (V_L); this is the *minimum* forward voltage (V_{Fwd}), required to ensure just 80% of the *minimum*

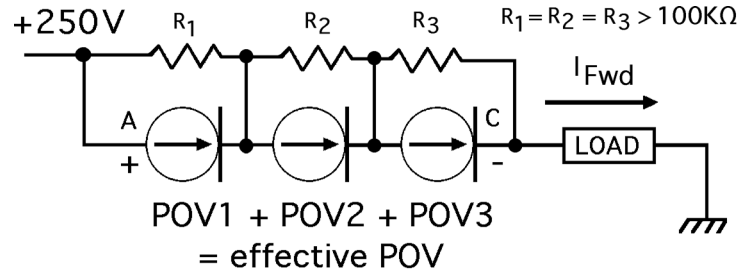


Figure 6.24. Combining CRDs in series for high-voltage applications.

forward current (I_{Fwd}). Some low-current CRDs have a very low limiting voltage of less than 1 volt, such as those devices shown in Figure 6.22.

Some data sheets refer to a reverse voltage (V_R), which is simply the value of a *reverse-bias* voltage that the device can withstand (with the cathode positive and the anode negative). It is usually measured at a low reverse current (I_R) of 1 mA and is approximately a diode drop of 0.7 to 0.8 volt. This is shown in Figure 6.25 and can be considered equivalent to the JFET's gate-drain channel diode. Exceeding the specified absolute maximum rating on the data sheet for reverse current may destroy the CRD. For example, J-500, SST-500, CR, and CRR series all have a 50-mA limit (assume that all other types are lower unless you confirm differently from the manufacturer).

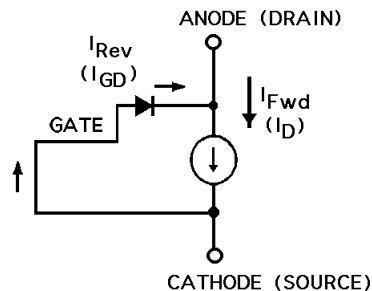


Figure 6.25. Reverse-bias equivalent of the current regulator diode.

In some designs, you may need to insert a protective diode in series with the anode or cathode, so that it is forward-biased in the same direction as the CRD's I_{Fwd} , if there is a possibility that the CRD may be inadvertently reversed. Doing so, however, could alter your circuit's temperature coefficient, because the diode's forward voltage (V_{fwd}) has a negative temperature coefficient of 2.2 mV/°C. You may need to choose another CRD with a different current value and associated tempco to compensate. In some

cases where an AC voltage is applied, two CRDs can be connected in a series-opposing manner. This way one can provide a bidirectional current regulator. During the period of the AC waveform when one device is conducting, the other one is simply a forward-biased diode, as shown in Figure 6.25. The difference between the DC mode mentioned previously and the AC mode of operation is that the AC forward-biased diode is now safely current-limited by the second device.

The CRD's *most important* specification is its forward current (I_F) or regulating current. Some manufacturers still refer to it by its old name of pinch-off current (I_p). This is the current you are essentially designing around. In the data sheet it is specified at a particular test voltage (usually 25 volts), at room temperature. It is shown in Figure 6.23 as " VT_{25} ," meaning at a test voltage of 25 volts. Manufacturers usually measure the forward current using a pulsed test, lasting a few milliseconds. As with most other semiconductors (e.g., MOSFETs, SCRs, diodes, BJTs), using a pulsed test lends itself well to automated test systems. The alternative is a slow (more than 60 seconds per device) steady-state method, which must use a large heatsink. The manufacturer usually specifies a typical value for I_F as well as a minimum and a maximum. For premium-grade devices, the forward current is usually $\pm 10\%$, and for lower-grade devices it is $\pm 20\%$. Because CRDs are available in relatively low current values (from 35 to 50 mA), they can be easily paralleled for increased current operation, as shown in Figure 6.26.

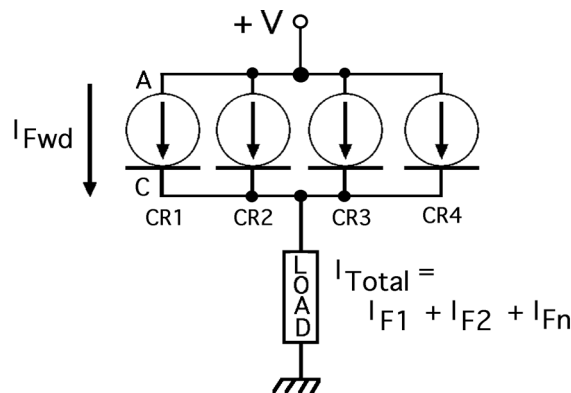


Figure 6.26. Combining CRDs in parallel for higher current operation.

At the other end of the current scale is the *limiting current* (I_L). This is the 80% point of the *minimum* forward current (I_{Fwd}), required to sustain the limiting voltage (V_L). Both the I_L and V_L points are shown in Figure 6.23 for your reference.

Another important CRD characteristic is the *knee impedance* (Z_K). This point is also shown in Figure 6.23 and indicates where the knee of the curve is located. (With a regular JFET the drain current increases linearly, then begins to be pinched off or lim-

ited at the knee of the curve. The curves that display the drain current versus the V_{DS} constitute a JFET's *output characteristics*.) With the CRD, the knee impedance should be as high as possible, to provide the most constant current for the CRD. In the diagram it is associated with " VT_6 " (the knee impedance test voltage), meaning at a test voltage of 6 volts. The knee impedance is specified in $M\Omega$, and as a *minimum* value. Low current values typically yield a high value of Z_K , while high current levels provide lower values of Z_K . This varies, however, from one CRD family to another, as shown in Table 6.4.

Series:	Nominal Current (mA):	Dynamic impedance - Z_d MIN: ($M\Omega$)	Knee impedance - Z_k: ($M\Omega$)
J-505	1.0-mA	0.5- $M\Omega$	0.4- $M\Omega$ typ
IN 5297	1.0-mA	0.8- $M\Omega$	0.205- $M\Omega$ min
CCL-1000	1.1-mA	0.65- $M\Omega$	0.10- $M\Omega$ min
CRR-1250	1.25-mA	0.5- $M\Omega$	0.8- $M\Omega$ typ
CR-100	1.0-mA	0.8- $M\Omega$	0.205- $M\Omega$ min

Table 6.4 Comparison of different CRD Series: Z_d and Z_k values

Another impedance specified for CRDs is the *dynamic impedance* (Z_D). This point is also shown in Figure 6.23 and indicates what the minimum impedance is at full conduction and at a reasonable supply voltage. The dynamic impedance should also be as high as possible, to aid in providing the most constant current for the CRD. In the diagram it is associated with " VT_{25} " (the dynamic impedance test voltage), specified as mentioned at 25 volts. The dynamic impedance is also specified in $M\Omega$, and again as a *minimum* value. CRDs with low current values yield a high value of Z_D (typically more than 5 $M\Omega$), while high current devices provide lower values of Z_D (typically less than 0.5 $M\Omega$). Again, this varies from one CRD family to another, as shown in Table 6.4.

While not usually specified on a data sheet, the CRD has a forward capacitance (C_F), which varies with the applied voltage and the particular device geometry. Its value is highest at low voltages (typically less than 20 pF at 6 volts), but falls with increasing voltage. At above 10 volts and at 1-MHz frequency, the forward capacitance is typically less than 10 pF, and it remains at this low level up to the POV limit of the device.

As mentioned previously, associated with each device's nominal current value is a defined *temperature coefficient* (TC, tempco). Some devices have a positive tempco, whereas others have a negative tempco. It is usually measured over a narrow portion of the device's total operating temperature range, such as $+20^{\circ}\text{C}$ to $+50^{\circ}\text{C}$, of a total -55°C to $+200^{\circ}\text{C}$, in order to determine the slope of the TC (i.e., either positive, negative, or flat). Depending on the application and circuit arrangements, a positive or a negative tempco can be used to compensate for subsequent circuit stages in one's design. A few devices have a zero (or close to zero) TC (i.e., CR047, CR240, J502, 1N5290, CCLM0750). For many CRDs, the temperature coefficient is better than $0.15\%/^{\circ}\text{C}$ (1500 ppm).

Some manufacturers publish the TC values in their data sheets, but not all do. If the TC is important in your application, you are recommended to contact technical support at the manufacturer in question. Remember also that with higher current devices, the tempco will be larger because of higher power dissipation and self-heating. If you are unable to determine the tempco from the data sheet, you should carefully measure the current output over the temperature range of interest. You should also test the performance of the circuit by changing the value of V_{DS} and noting any change in output current. You will need to graph the results. You can determine what the circuit's tempco is in ppm/ $^{\circ}\text{C}$ or as a percentage by using equations 6.23 and 6.25 shown earlier in this chapter.

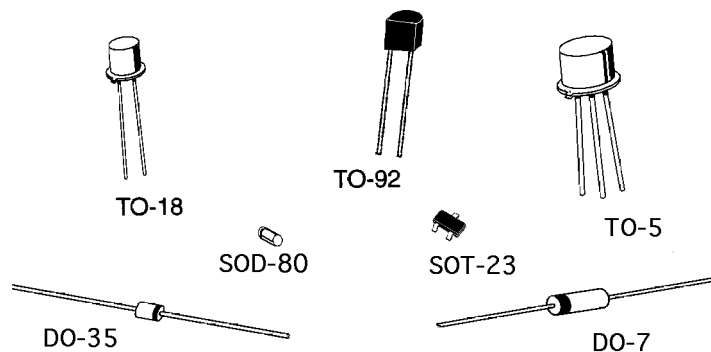


Figure 6.27. Current regulator diodes are available in various popular packages.

Generally, CRDs are available in various glass, metal, plastic, and surface-mount packages (see Figure 6.27). In any design scenario, you should consult the manufacturer or visit its Web site for up-to-date availability on the various package options. Product lines change and grow, and so does a manufacturer's packaging capability. While a couple of years ago a manufacturer may have only offered a few different package options, today it probably has most of the product line available in various packages. In one case, Crystalonics makes a high-current family of CRD devices (CIL-350 series) with currents up to 50 mA, and which are provided in a TO-5 metal

can. Although some devices are proprietary to a manufacturer, many are JEDEC-registered and are available from multiple sources.

Whatever the package type of the CRD of your choice, there will be wattage and *thermal characteristics* associated with it. As with every other type of semiconductor device, the CRD's particular type of package will have a wattage rating and a derating factor. For example, an 1N5283 is provided in a glass DO-7 diode-type package. This is rated at a maximum 600 mW and has a derating factor of 4.8 mW/°C, above 75°C lead temperature. This particular package usually has its temperature measured and referenced 3/8 inch (9.525 mm), from the glass envelope. The cathode lead of the device (the end with the colored band) is where most of the heat is conducted away from the junction. Other popular package types, such as the TO-92 plastic transistor-type package, will have a different wattage rating. In this case, it is typically 350 mW, with a derating factor of 2.8 mW/°C above 25°C, room temperature. You should ensure that the package type(s) you are using in your design is operating well within the manufacturer's recommended thermal rating to ensure a long and reliable life.

6.5.2 A design guide

First establish the load, supply voltage, and constant current requirements for your circuit, along with the $\pm\%$ tolerances for each. This will help determine the necessary wattage required for the CRD. Next, choose a suitable device from Table 6.5 or from a product catalog. Remember that Table 6.5 is only a summary and does *not* include the temperature coefficients that may be necessary for your design. You should make a list of suitable devices. Obtain the device(s), and then build and evaluate the circuit.

Test the performance of the circuit by varying the value of the supply voltage and load impedance. Note and record any change in output current (I_D). You may decide that over the intended temperature range, the circuit requires a change in its current/temperature coefficient to compensate. If you have to implement any changes, such as using a different CRD with a different current value and associated tempco, you should test and graph the circuit again, over the intended temperature range.

Build another circuit using the same modifications you made previously. Recalculate the new tempco, and see how that has changed from the original design. You may have to use a CRD with a current value that is an average of some of your previous tests, for a mass-production situation. Lastly, evaluate your design again, so that it is ready for preproduction stage. You may have to average your results to be more easily mass-produced. If you are involved in a design for a mass-production job (i.e., thousands of devices), you should contact the manufacturer directly and have a certain current value selected for you. To the best of the author's knowledge, the CRD manufacturers listed in this chapter will be happy to work with you in that type of situation.

6.5.3 An overview of various popular CRD families

The following is a brief summary of most of the popular CRD families in the United States. Table 6.5 briefly summarizes these for you with relevant design information.

However, you are advised to obtain more complete product literature from the manufacturer or its Web site before getting too far along in your design.

- *The CIL series* are a high current family, made exclusively by Crystalonics. They include 16 different values, subdivided into two ranges. The CIL-250 to 257 group ranges from 5.1 mA to 10 mA. The CIL-350/A to 366/A group ranges from 11 mA to 51 mA. Both groups have a guaranteed $\pm 10\%$ tolerance on any particular current value. The minimum peak operating voltage is 50 volts DC for CIL-250 to 257 and more than 27 volts for CIL-350/A to 366/A. Both groups operate over an extended temperature range of -55°C to $+150^{\circ}\text{C}$. The CIL-250 to 257 series are available in a DO-7 glass package and are rated at 600 mW. The CIL-350/A to 366/A series are available in a TO-5 metal transistor-type package, rated at 1.5 Watts.
- *The 1N 5283 series* are prime-grade devices, which include 32 different values ranging from 0.22 mA to 4.7 mA, with a guaranteed $\pm 10\%$ tolerance on the specific current value. The peak operating voltage is 100 volts DC, and the series is typically available in a DO-7 glass diode-type package; however, Central Semiconductor makes this in a newer, more efficient DO-35 package. Either package type is rated at 600 mW. The series is specified for operation over an extended temperature range of -55°C to $+200^{\circ}\text{C}$. Crystalonics also makes this available in military-grade JAN, JTX, and JTXV devices.
- *The CR series* are prime-grade devices, which include 32 different values ranging from 0.22 mA to 5.3 mA, with a guaranteed $\pm 10\%$ tolerance on the specific current value. They are available in a two-lead modified TO-18 metal-can package and operate over an extended temperature range of -55°C to $+150^{\circ}\text{C}$. The CR series is rated at 1.25 Watts. Originally introduced by Siliconix, the range is now made by Linear Integrated Systems. Vishay-Siliconix makes CR-160 and above.
- *The CRR series* are prime-grade devices, which include eight different values ranging from 0.24 mA to 4.3 mA, with a guaranteed $\pm 25\%$ tolerance on the specific current value. They are available in a two-lead modified TO-18 metal-can package and operate over an extended temperature range of -55°C to $+150^{\circ}\text{C}$. The CRR series is rated at 1.25 Watts. Originally introduced by Siliconix, the range is now made exclusively by Linear Integrated Systems.
- *The J500 series* are a lower-cost family, which include 12 different values, ranging from 0.24 mA to 4.5 mA. These devices have a guaranteed $\pm 20\%$ tolerance on any particular current value. The minimum peak operating voltage is 50 volts DC, and they are rated at 360 mW. The J500 series are available in a two-lead modified TO-92 plastic package (TO-226AA) and operate over an extended temperature range of -55°C to $+150^{\circ}\text{C}$.

- *The SST500 series* are available in 12 different values, ranging from 0.24 mA to 4.7 mA. These devices have a guaranteed $\pm 20\%$ tolerance on any particular current value. They are basically the popular J-500 series, but in an SOT-23 surface-mount package. The SST500 series have a minimum peak operating voltage of 50 volts DC and are rated at 360 mW. They operate over an extended temperature range of -55°C to $+150^{\circ}\text{C}$.
- *The J552 series* are a low-cost family, which include six different values, ranging from 0.25 mA to 4.5 mA. These devices have a guaranteed $\pm 20\%$ tolerance on any particular current value. The minimum peak operating voltage is 50 volts DC, and they are rated at more than 350 mW. The J552 series are available in a two-lead modified TO-92 plastic package (TO-226AA) and operate over an extended temperature range of -55°C to $+135^{\circ}\text{C}$.
- *The U553 series* are available in six different values, ranging from 0.50 mA to 4.5 mA. These devices are now exclusive to InterFET and have a guaranteed $\pm 20\%$ tolerance on any particular current value. The minimum peak operating voltage is 50 volts DC, and they are rated at 360 mW. The U553 series are available in a modified TO-18 metal can and operate over an extended temperature range of -65°C to $+150^{\circ}\text{C}$.
- *The CCL0035 series* is a low-cost family exclusively from Central Semiconductor, which includes 12 different values, ranging from $35\ \mu\text{A}$ to 5.75 mA. These devices have a guaranteed $\pm 16\%$ tolerance on any particular current value. The minimum peak operating voltage is 100 volts DC, and they are rated at 600 mW. The series is available in a small but rugged DO-35 diode package. It operates over an extended temperature range of -65°C to $+200^{\circ}\text{C}$.
- *The CCLM0035 series* is another low-cost family exclusively from Central Semiconductor, which includes 12 different values, ranging from $35\ \mu\text{A}$ to 5.75 mA. These devices have a guaranteed $\pm 16\%$ tolerance on any particular current value. The minimum peak operating voltage is 100 volts DC, and they are rated at 800 mW. The series is available in a small but rugged SOD-80 surface-mount package. It operates over an extended temperature range of -65°C to $+200^{\circ}\text{C}$.
- *The CCLH080 series* is a low-cost family exclusively from Central Semiconductor, which includes four different values, ranging from 8.2 mA to 15 mA. These devices have a guaranteed $\pm 20\%$ tolerance on each particular current value. The minimum peak operating voltage is 50 volts DC, and they are rated at 600 mW. The series is available in a small but rugged DO-35 diode package. It operates over an extended temperature range of -65°C to $+200^{\circ}\text{C}$.
- *The CCLHM080 series* is a low-cost family exclusively from Central Semiconductor, which includes four different values, ranging from 8.2 mA to 15 mA. These devices have a guaranteed $\pm 20\%$ tolerance on each

particular current value. The minimum peak operating voltage is 50 volts DC, and they are rated at 800 mW. The series is available in a small but rugged SOD-80 surface-mount package that operates over an extended temperature range of -65°C to $+200^{\circ}\text{C}$.

In summary, Linear Integrated Systems and Central Semiconductor offer the most products, followed by Crystalonics. Central Semiconductor offers the lowest-current devices (CCL-0035 and CCLM-0035 families), with current levels down to $35\ \mu\text{A}$, while Crystalonics offers the highest-current devices (CIL-250 and CIL-350 families), with currents up to 51 mA. The most second-sourced family of CRDs is the J-500 family, which is available from four different manufacturers, and in some cases is also available in surface-mount versions. Another is the 1N5283 family, which is an older device, but also available from four different manufacturers. At the time of this writing, the manufacturer with the most devices available in surface-mount packages was Central Semiconductor. Most manufacturers have now included surface-mount packages in their product offerings, but you should check to see whether package options other than those listed in Table 6.5 are available.

Some circuit examples using CRDs are shown in Figure 6.28.

Circuit A shows a typical NPN differential amplifier. Replacing the normal emitter bias resistor with a CRD significantly improves the amplifier's common-mode rejection ratio (CMRR). The CRD can boost the normal common-emitter impedance (less than $1\ \text{K}\Omega$), anywhere from 20 to 60 dB, and also improves the temperature stability of the circuit.

Circuit B shows how to provide a stable, low-voltage reference (0.25 volt) by combining a CRD with a precision resistor. The voltage level is set by applying Ohm's law. Normally, Zener diodes and monolithic voltage references cannot provide voltages this low.

Circuit C combines a Crystalonics CIL-254 (medium-power CRD) with a Central Semiconductor 1N829A (temperature-compensated) selected zener diode, to create a two-component voltage reference. This circuit will provide a stable output for an input voltage range of approximately 8 volts to the POV rating of the CRD (in this case, 60 volts), and over a temperature range of -25°C to more than 100°C . Using a 1N5290 CRD with a (hard-to-find) 1N4569 TC zener instead provides a much lower-power alternative, with an even wider V_{in} .

Table 6.5 US Manufacturers of Current Regulator Diodes

In Circuit D, replacing a BJT's normal emitter load resistor with a CRD increases the gain of the amplifier stage, as well as increasing its input impedance.

Mfr:	Series:	Current Range (mA):	POV max (volts):	Limiting Voltage range:	Temp. range: °C	Wattage rating max	Package:
Calogic:	J-500 - J-511 (12-devices)	0.24 thru' 4.7 ± 20%	50 V	0.4 - 2.1 typ.	- 55° to + 150°	350 mW	TO-92
	SST-500 - 511 (12-devices)	0.24 thru' 4.7 ± 20%	50 V	0.4 - 2.1 typ.	- 55° to + 150°	360 mW	SOT-23
Central Semiconductor	IN 5283 - 5314 + JAN (32-devices)	0.22 thru' 4.7 ± 10%	100 V	1 - 2.9 max	- 65° to + 200°	600 mW	DO-35
	CCL-0035 thru 5750 (12-devices)	0.035 thru 5.75 ± 16%	100 V	0.4 - 4.5 max	- 65° to + 200°	600 mW	DO-35
	CCLM-0035 thru 5750 (12-devices)	0.035 thru 5.75 ± 16%	100 V	0.4 - 4.5 max	- 65° to + 200°	800 mW	SOD-80
	CCLH-080 thru 150 (4-devices)	8.2 thru' 15 ± 20%	50 V	3.1 - 4.3 max	- 65° to + 200°	600 mW	DO-35
	CCLHM-080 thru 150 (4-devices)	8.2 thru' 15 ± 20%	50 V	3.1 - 4.3 max	- 65° to + 200°	800 mW	SOD-80
	IN 5283 - 5314 + JAN (32-devices)	0.22 thru' 4.7 ± 10%	100 V	1 - 2.9 max	- 55° to + 200°	600 mW	DO-7
Crystalonics	CIL-250 to 257 (8-devices)	5.1 thru' 10 ± 10%	> 50 V	3.67 -7.2 max	- 55° to + 150°	600 mW	DO-7
	CIL-350/A to 366/A (8-devices)	11 thru' 51 ± 10%	> 27 V	6.0 max	- 55° to + 150°	1.5W	TO-5
	J-500 - J-511 (12-devices)	0.24 thru' 4.7 ± 20%	50 V	0.4 - 2.1 typ.	- 55° to + 150°	350 mW	TO-92
InterFET:	J-553 - 557 (5-devices)	0.5 thru' 4.5 ± 20%	50 V	0.75 - 1.3 typ	- 55° to + 150°	360 mW	TO-92
	U-553 - 557 (5-devices)	0.5 thru' 4.5 ± 20%	50 V	0.75 - 1.5 typ.	- 65° to + 150°	360 mW	TO-18
	J-500 - J-511 (12-devices)	0.24 thru' 4.7 ± 20%	50 V	0.4 - 2.1 typ.	- 55° to + 150°	350 mW	TO-92
Linear Integrated	SST-500 - 511 (12-devices)	0.24 thru' 4.7 ± 20%	50 V	0.4 - 2.1 typ.	- 55° to + 150°	360 mW	SOT-23
	J-552 - 557 (6-devices)	0.5 thru' 4.5 ± 20%	> 50 V	1 - 2.1 typ.	- 55° to + 135°	350 mW	TO-92
	LSCR022 - 470 (32-devices)	0.243 thru 5.83 ± 10%	100 V	0.4 -1.4 typ	- 55° to + 150°	1.25W	TO-18
	LSCRR0240 - 4300	3 thru 5.4 ± 25%	100 V	0.5 - 1.45 typ.	- 55° to + 150°	1.25W	TO-18
	IN 5283 - 5314 + JAN (32-devices)	0.22 thru' 4.7 ± 10%	100 V	1 - 2.9 max	- 65° to + 200°	600 mW	DO-7
Solitron Devices	IN 5283 - 5314 + JAN (32-devices)	0.22 thru' 4.7 ± 10%	100 V	1 - 2.9 max	- 65° to + 200°	600 mW	DO-7/TO-92 /TO-18
Vishay - Siliconix	CR-160 - 470 (12-devices)	1.6 thru' 4.7 ± 10%	100 V	0.7 - 2.9 typ.	- 55° to + 200°	300 mW	TO-18
	J-500 - J-511 (12-devices)	0.24 thru' 4.7 ± 20%	50 V	0.4 - 2.1 typ.	- 55° to + 150°	350 mW	TO-92

NOTE: Check with manufacturer for latest device package availability.

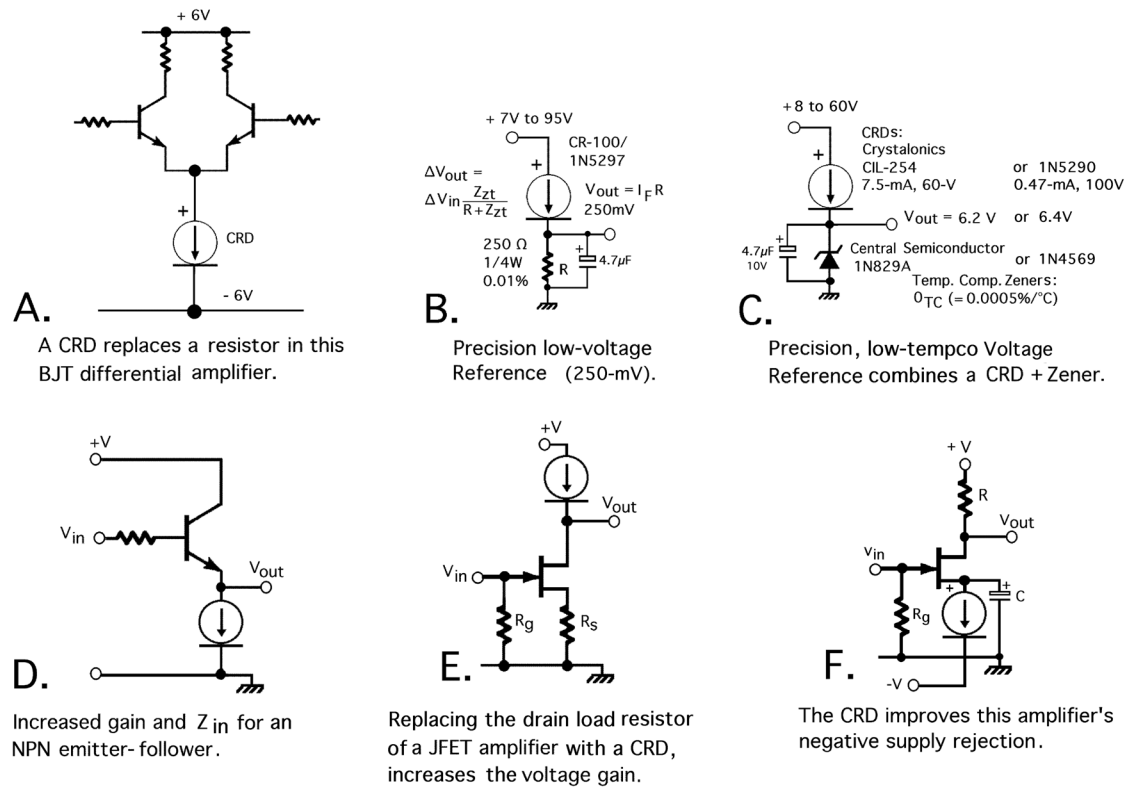


Figure 6.28. Some typical CRD applications.

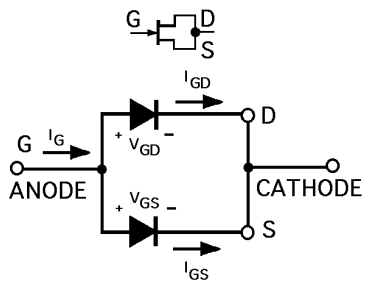
Circuit E shows how using a CRD instead of the normal drain resistor can increase the voltage gain for this JFET amplifier. The CRD's high output impedance is the difference here.

In Circuit F, a CRD replaces the normal source resistor, thereby increasing the JFET amplifier's negative supply rejection.

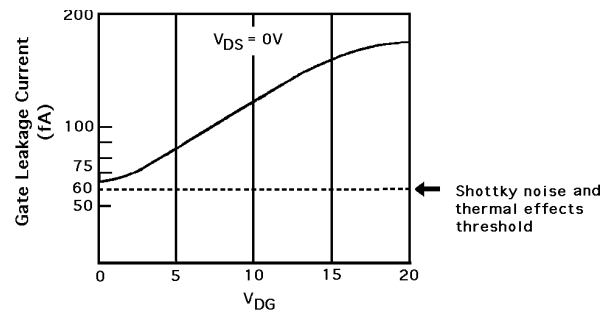
6.6 Using JFETs to create ultra-low-leakage diodes

Dedicated low-leakage diodes typically have leakage currents in the low nano-amp range, which in some situations can actually degrade a precision measurement circuit. For example, the very-low-input bias-currents of some precision op amps are in the pico-amp range. Using a typical low-leakage diode with this type of op amp can significantly degrade the measurement capabilities of the circuit. As mentioned elsewhere in this book, JFETs can be used to create *ultra-low-leakage* diodes, which can also be of use when creating current sources or voltage references. Normally, when the JFET

has its drain and source shorted together (see Figure 6.29), it provides an ultra-low-leakage diode (known as a *pico-amp diode*, PAD), with extraordinary low-leakage currents. In some conditions, such diode-connected JFETs can attain leakage-current levels that are below 200 femto-amps (2×10^{-13} A) at V_{DG} at 20 volts or less than 100 fA at V_{DG} at 5 volts—and almost immeasurable. Particular JFETs, such as these listed as follows, can attain less than 10 pA at 25° C.



The N-channel JFET equivalent when used as a very low-leakage diode.



Notice the ultra-low leakage currents at low drain voltages for 2N4117A.

Figure 6.29. JFET Pico Amp diodes.

TO-72, four-pin metal package:

2N4117	2N4117A
2N4118	2N4118A
2N4119	2N4119A

TO-92, three-pin plastic package:

PN4117	PN4117A
PN4118	PN4118A
PN4119	PN4119A

SOT-23, three-pin surface-mount package:

SST4117

SST4118

SST4119

In addition, dedicated discrete JFET ultra-low-leakage pico-amp diodes, such as the PAD, JPAD, or SSTPAD (SOT-23) series, can attain less than 5 pA. Dual versions are also available in the form of the DPAD and SSTDPAD families. This type of device is made by many JFET and CRD manufacturers, which include Calogic, Central Semiconductor, InterFET, Linear Integrated Systems, Philips Semiconductors, and Vishay-Siliconix. Some examples of JFET diode applications are shown in Figure 6.30.

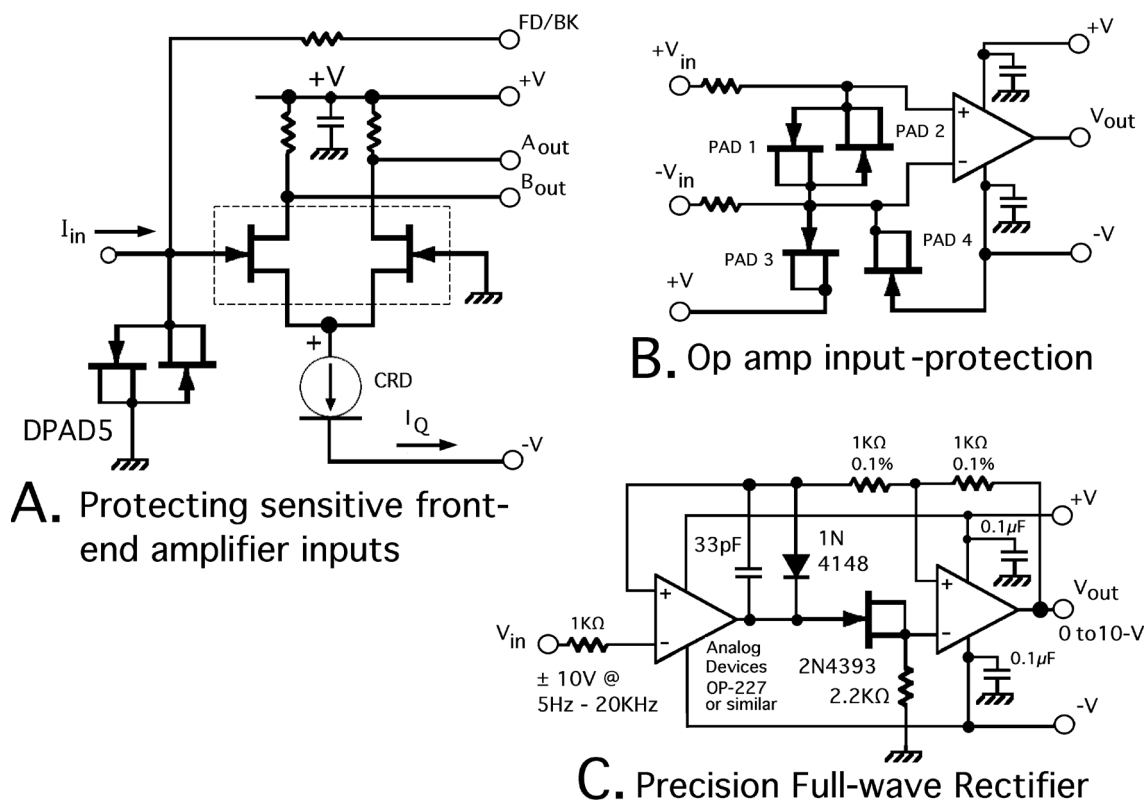


Figure 6.30. JFET/pico-amp diode (PAD) applications.

In Circuits A and B, JFET diodes protect the inputs to very-low-level amplifiers. Normally, the JFET diodes have reverse leakage currents in the low pA range, which is less than the very-low-input bias currents of most amplifiers, either discrete or monolithic. The JFET diodes will clamp the input to approximately 0.7 volt in case a potential dangerous and costly voltage spike occurs. In Circuit B, the op amp's input differential voltage is limited to typically 0.8 volt by the JFET diodes, PADs 1 and 2, while the common-mode input voltage is limited by PADs 3 and 4, to the amount of the supply rails. Using dual PADs (DPADs) would save space.

In Circuit C, a JFET diode/PAD is used in a precision rectifier design. For best results, the op amp should have a very high CMRR value, a high gain, and a low TC V_{OS} , in which case errors will be extremely small (i.e., less than 10 ppm). Anyhow, it's worth remembering the next time you need an ultra-low-leakage diode, that the JFET can do that too.

When you consider what a simple JFET can do, it has to be one of the most useful semiconductor devices ever invented, and certainly an essential building block in analog electronics. It has come a long way since Dr. Lilienfeld first theorized on a FET-like device and Dr. Shockley subsequently invented it in the early 1950s. No doubt the JFET will be a part of our design arsenal for decades still to come.