WAFER BONDING FOR THREE DIMENSIONAL (3D) INTEGRATION

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CONTENTS

LIST OF TABLES vi

LIST OF FIGURES vii

ACKNOWLEDGMENTS xv

ABSTRACT xvi

1. **INTRODUCTION** 1
   - 1.1. Motivation of Wafer Bonding 1
   - 1.2. Motivation of 3D IC Integration 2
   - 1.3. Thesis Organization 5
2. **TECHNICAL BACKGROUND** 7
   - 2.1. Overview 7
   - 2.2. Applications for Wafer Bonding/Attachment 8
     - 2.2.1. Bond and Etch-Back SOI 8
     - 2.2.2. Three-Dimensional (3D) ICs 12
   - 2.3. 3D ICs using Dielectric Glues and Damascene Inter-Wafer Interconnects ..19
   - 2.4. Wafer Bonding Technologies 23
     - 2.4.1. Direct Wafer Bonding (DWB) 23
     - 2.4.2. Plasma Activated Bonding (PAB) 25
     - 2.4.3. Anodic Bonding 27
     - 2.4.4. Metal-to-Metal Bonding 28
     - 2.4.5. Dielectric Glue Bonding 28
   - 2.5. Low-k Polymeric Glue Alternatives 31
     - 2.5.1. MSSQ (Methyl Silsesquioxane) 31
     - 2.5.2. Parylene-N 32
     - 2.5.3. Flare (Poly Arylene Ether) 34
     - 2.5.4. BCB (Benzocyclobutene) 34
   - 2.6. Theory of Bond Strength 35
   - 2.7. Summary 39
3. **EXPERIMENTAL PROCEDURES** 40
   - 3.1. Overview 40

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3.2. Wafer Bonding Equipment and Procedures....40
3.2.1. Deposition and Bake of Polymeric Glues....41
3.2.2. Bonding Equipment and Processing Capabilities....45
3.3. Bond Characterization Techniques....48
3.3.1. Characterization of Bond Strength....49
3.3.1.1.Four Point Bending Technique....49
3.3.1.2.Procedure of Beam Specimen Preparation....50
3.3.1.3.Mean Critical Adhesion Energy and Standard Deviation for Two Types of Results....53
3.3.1.4.Reproducibility Tests by Different Operators....57
3.3.2. Wafer Curvature and Built-In Stress....58
3.4. Material Characterization Techniques....61
3.4.1. Fourier Transform Infrared (FTIR) Spectroscopy....61
3.4.2. Spectroscopic Ellipsometry....62
3.5. Summary....63
4. **POLYMERIC GLUE SCREENING**....64
4.1. Overview....64
4.2. Optical Inspection with Transparent Wafers....65
4.2.1. Initial Screening Results....65
4.2.2. Comparison of Flare and BCB....68
4.3. Chemical Analysis of Flare and BCB using FTIR....70
4.4. Bond Strength Comparison between BCB and Flare....72
4.5. Summary....74
5. **QUANTITATIVE EVALUATION OF BCB BOND STRENGTH**....75
5.1. Overview....75
5.2. Adhesion Promoter Effects....75
5.3. BCB Thickness Effects....79
5.4. Substrate Effects....87
5.5. Baseline Process Parameters....94
5.6. Summary....95

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6. **THERMAL CYCLING EVALUATION OF BOND STRENGTH AND RESIDUAL STRESS** 97
6.1. Overview 97
6.2. Experimental Procedures 98
6.3. Bond Strength Dependence of Number of Thermal Cycles 100
6.4. Bond Strength Dependence of Peak Temperature 105
6.5. Effect of Stress Release of PECVD Oxide on Thermal Cycling 109
6.6. Effect of Thermal Cycling on BCB Thermal Stability 112
6.7. Summary 116
7. **BONDING INTEGRITY OF PATTERNED WAFERS** 119
7.1. Overview 119
7.2. Patterned Wafer Results 119
7.3. Mechanical Evaluation of Bonding Integrity 124
7.4. Electrical Evaluation of Bonding Integrity 126
7.5. Summary 128
8. **SUMMARY, CONCLUSIONS AND FUTURE WORK** 130
8.1. Summary and Conclusions 130
8.2. Future work 134
9. **REFERENCES** 139

APPENDICES

A. **Basic Concepts of Statistical Analysis** 148
B. **Library of Bonded Wafer** 151
C. **Publications from Research Program** 156
Wafer Bonding Highlighted 156
3D IC Highlighted 157

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LIST OF TABLES

2.1 Physical properties of polymer glue candidates. 31

3.1 Sequences of spin dry cleaning process. 41

3.2 Coat and bake programs of adhesion promoter and BCB resin 42

3.3 Coat and bake programs of Flare resin 43

3.4 Coat and bake programs of MSSQ resin. 44

4.1 Peak position and peak assignments of Flare 71

4.2 Peak position and peak assignments of BCB 72

5.1 Four point bending results of four types of bonded wafer pairs 76

5.2 Four point bending results in different BCB thicknesses 80

5.3 Relationship between G_{tip} and $G_{plastic}$ in different bonded interfaces 87

5.4 Chemical components of PG&O 1737 glass wafer [107] 89

5.5 Bond strength of various diatomic molecules of glass wafer [108] 89

6.1 Bond strength dependence of number of cycles at peak temperature of 400 °C for Si/PECVD SiO_2/AP/BCB/AP/PECVD SiO_2/Si (structure depicted in Figure 6.1) 101

6.2 Bond strength dependence of number of cycles at peak temperature of 350 °C for Si/PECVD SiO_2/AP/BCB/AP/PECVD SiO_2/Si 106

6.3 Bond strength dependence of number of cycles at peak temperature of 450 °C for Si/PECVD SiO_2/AP/BCB/AP/PECVD SiO_2/Si 107

7.1 RIE ashing parameters for BCB 123

7.2 Four point bending results of two bonded wafer pairs including the patterned wafers 125

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LIST OF FIGURES

1.1 3D platform for ICs and heterogeneous systems. 3

2.1 Bonded SOI wafer process flow including grinding and polishing methods [28] 9

2.2 Schematic of process flow of the Smart Cut® technique [28] 12

2.3 Schematic of process flow for 3D image sensor fabrication. Adapted from [29]. 15

2.4 Inter-wafer interconnect structure and SEM image of the 3D image sensor. Adapted from [29] 16

2.5 Schematic of process flow of 3D IC structure [30] 17

2.6 Conceptual configuration of 3D image sensor chip with 3D structure. Adapted from [35] 17

2.7 Schematic of process flow of parallel 3D image-processing. Adapted from [35] 18

2.8 Schematic of a test vehicle using wafer bonding, showing bonding interface, vertical inter-chip vias (plug- and bridge-type), and "face-to-face" and "face-to-back" bonding [32] 20

2.9 Inter-wafer interconnect process flow for via-chain structure fabrication [37] 21

2.10 200 mm wafer-to-wafer alignment accuracy with via-chain test structures, indicating 1 μm alignment can be achieved [37] 21

2.11 Top view of the via-chain structure for inter-wafer via sizes of nominal 8 μm (top image) and 2 μm (bottom image), showing wafer-to-wafer misalignment of ~1μm. Vertical via connects bottom (M1) and top (M2) metals [37]. 22

2.12 Via-chain resistance vs. via-chain length (via number): for nominal via size of 8 μm (left), for nominal via size of 2, 3, 4 μm. The nominal via landing pad is 12x12 μm^2 for 8 μm via chain (right) [37]. 23

2.13 Saturation values of bond strength as a function of temperature after long-term heat treatments. Adapted from [38] 25

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2.14 Chemical structure of polymer backbone of MSSQ. Adapted from [56]....32
2.15 3D (cage) structure of MSSQ....32
2.16 Process flow of the polymerization of the parylene-N group [57]....33
2.17 Anticipated cure reaction of flare polymeric glue [60]....35
2.18 Crosslinking schematics of BCB resin and chemical structure of BCB monomer [60]....35
2.19 Beam specimen geometry for four point bending experiments....37
3.1 EVG EV 501 bonder and structure inside the bonder [52]....45
3.2 Schematic of theoretical cure reaction in wafer to wafer bonding process: (a) Before heating and pressurization, (b) Start of polymeric glue cure reaction, pressurization is needed to promote out-of-plane (glue to glue) inter-diffusion, (c) End of polymeric glue cure reaction, inter-diffusion and cross-linking is completed....48
3.3 Fixture for four point bending experiments....49
3.4 Schematic of four point bending specimen before and after bending....50
3.5 Typical four-point bending result; a load-displacement curve for measuring saturation load value....51
3.6 Two types of load vs. displacement curve: (a) type 1consists of linear elastic I, load plateau, and linear elastic II regions, and (b) type 2 consists of linear elastic, load plateau, and sample breakage regions....54
3.7 Examination of load plateau region and saturation load using normalized standard deviation λ: (a) Refused test: calculated λ value of 0.042 is higher than standard λ value of 0.02. (b) Accepted test: calculated λ value of 0.002 is lower than standard λ value of 0.02. 55
3.8 Determination of mean critical adhesion energy, G_c and standard deviation (S.D.) values using "residual analysis" method: (a) Si/ thermal SiO_2 (2 μm)/ BCB (2.6 μm)/ thermal SiO_2 (2 μm)/ Si structure. After analyzing using "Residual analysis", 2 specimens, which are deviated from +/- 2 σ, are discarded (outliers). Mean Gc is 34 J/m^2 with S.D. of 2.2 J/m^2. (b) Si/ PECVD SiO_2 (1 μm)/ BCB (2.6

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μm)/ PECVD SiO_2 (1 μm)/ Si structure. After analyzing, 2 specimens are discarded (outliers). Mean Gc is 31 J/m^2 with S.D. of 1.7 J/m^2. 56

3.9 Reproducible test by different operators for obtaining critical adhesion energy. Mean G_c obtained by operator A is 22 J/m^2 with S.D. of 1.8 J/m^2, and mean G_c obtained by operator B is 23 J/m^2 with S.D. of 2 J/m^2. 57

3.10 Geometric structure for calculating the film stress using Stoney's equation.....58

3.11 Geometric structure for calculating the wafer bow using Stoney's equation.....61

3.12 Wafer bow versus wafer radial distance curve for 200 mm wafers 61

4.1 Wafer bonding result using MSSQ. Bonded wafer pair (200mm): P (100) prime wafer and Corning 7740 glass wafer. 66

4.2 Wafer bonding result using MSSQ. Bonded wafer pair (200mm): P (100) prime wafer and Corning 7740 glass wafer. 66

4.3 Oxygenation reaction of free radical center, which is the main reason of oxidative chain scissions [87].....67

4.4 The rupture reaction resulted from oxygen radical [87]. 67

4.5 Wafer bonding result using Flare. Bonded wafer pair consists of (200mm): P (100) wafer and Corning glass wafer.....68

4.6 Wafer bonding result using BCB. Bonded wafer pair consists of (200mm): P (100) wafer and Corning glass wafer.....68

4.7 Wafer bonding result using BCB. Bonded wafer pair consists of patterned wafer (sent from SEMATECH) and Corning glass wafer. 69

4.8 FTIR spectra of Flare for the samples as spun, after bake (up to 250°C) and after cure reaction (one hour at 400°C). 70

4.9 FTIR spectra of BCB for the samples before and after bonding/curing (one hour at 250°C).....71

4.10 Geometrical configurations of bonded wafer pairs using BCB and Flare. 72

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4.11 Critical adhesion energies of bonded wafer pairs using BCB and Flare. Bond strength of bonded wafer using BCB is 9 J/m^2 with standard deviation of 0.9 J/m^2 and bond strength of bonded wafer using Flare is 18 J/m^2 with standard deviation of 2.2 J/m^2. 73

5.1 Beam specimen configurations and critical adhesion energies of bonded wafer pairs including double layer BCB with or without adhesion promoter. 76

5.2 Beam specimen configurations and critical adhesion energies of bonded wafer pairs including one layer BCB with or without adhesion promoter.....77

5.3 Chemical structure of adhesion promoter, AP3000. The adhesion promoter consists of silane based molecules (triacetoxysilane, $Si(OCOCH_3)_3$) and vinyl functional group. 78

5.4 The bonding mechanism across BCB to oxide layer using adhesion promoter. 78

5.5 Beam specimen configurations and critical adhesion energies in different BCB thicknesses. BCB is sandwiched by PECVD oxide deposited silicon wafers 79

5.6 Beam specimen configurations and critical adhesion energies in different BCB thicknesses. BCB is sandwiched by thermal oxide deposited silicon wafers 81

5.7 Critical adhesion energies dependence on BCB thickness. BCB is sandwiched by one silicon wafer and one glass wafer. 81

5.8 The molecular morphology in a craze. The molecules are heavily aligned in the form of fabrils (the dark areas) in the craze. This craze also contains voids. These are more predominant in the craze center. The voided areas assume the characteristics of a crack as the craze spreads laterally [108] 82

5.9 The biaxial loading yield loci for shear yielding and crazing. Crazing is important in quadrant I ($\sigma_1, \sigma_2 > 0$). Adapted from [108] 83

5.10 Schematic depicting critical adhesion energy dependence on structure consisting of ductile and elastic materials....83

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5.11 The geometrical configuration of beam specimen consisting of two elastic substrates and a BCB layer 84

5.12 Measured critical adhesion energies for various types of oxide layers. 88

5.13 Anticipated bond structure in between glass wafer and adhesion promoter and in between oxide deposited silicon wafer and adhesion promoter 90

5.14 General failure mechanism at the interface between BCB and substrate: (a) For short BCB chain, no effective entanglements are formed and chain pull-out effect occurring at the interface between adhesion promoter and substrate is dominant failure mode. (b) For long BCB chain, the interface is connected with entanglement between BCB as well as chemical interactions at the interface. Each BCB resin is entangled and the maximum bond density achievable is similar to that of (a). The scission of the interfacial chains should occur for bond failure. However, due to entangled BCB chain, the interfacial chains are not pulled out, and chain scission does not occur well. (c) For very long BCB chain, although each BCB resin is well entangled, the maximum bond density achievable (number of chemical bonds at the interface) is very low and such an interface fails easily by scission of bond groups at the interface [116] 91

5.15 The relationship among G_{tip}, polymer chain length, polymer bond density and the extent of physical entanglement of BCB chains 92

5.16 The relationship between G_{tip} and bond density of BCB at the interfaces between oxide deposited silicon wafer and BCB and between glass wafer and BCB 94

6.1 Beam specimen configurations and critical adhesion energy at 1, 5, and 10 thermal cycles at peak cycle temperature of 400 °C. BCB layer is sandwiched by PECVD oxide deposited silicon wafers. 101

6.2 Geometry of stacked layers and temperature dependence of residual stress on the stacked layers after the first and second thermal cycling at peak temperature of 400 °C. 102

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6.3 Geometry of PECVD oxide on silicon wafer and temperature dependence of residual stress on PECVD oxide on silicon wafer after the first and second thermal cycling at peak temperature of 400 °C.....104
6.4 Geometry of BCB on silicon wafer and temperature dependence of residual stress on BCB on silicon wafer after the first and second thermal cycling at peak temperature of 400 °C.....104
6.5 Critical adhesion energy in different peak cycle temperatures. Used number of thermal cycles is 1-, 5-, and 10-times at each peak temperature. BCB layer is sandwiched by PECVD oxide deposited silicon wafers.....106
6.6 Geometry of stacked layers and temperature dependence of residual stress on the stacked layers after the first and second thermal cycling at peak temperature of 350 °C.....108
6.7 Geometry of PECVD oxide on silicon wafer and temperature dependence of residual stress on PECVD oxide on silicon wafer after the first and second thermal cycling at peak temperature of 350 °C.....108
6.8 Geometry of BCB on silicon wafer and temperature dependence of residual stress on BCB on silicon wafer after the first and second thermal cycling at peak temperature of 350 °C.....109
6.9 Schematic diagrams showing stress state and change of chemical structure related with condensation reaction of neighborhood silanol groups. (a) Basic tetrahedral siloxane (Si-O-Si) configuration. (b) After deposition, the Si-to-Si distance is too close for the double OH inclusion, leading to compression. (c) After thermal cycling, the Si-to-Si distance is long compared to the basis Si-O-Si configurations, leading to tension [123].....111
6.10 Cure % dependence of glass transition temperature (Adapted from Dow Chemical Inc. [126]).....113
6.11 Temperature dependence of residual stress for BCB layer on silicon wafer after multiple thermal cycle tests. Peak temperature of 350 °C is used for these cycling tests.....114

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6.12 Temperature dependence of residual stress for BCB layer on silicon wafer after multiple thermal cycle tests. Peak temperature of 400 °C is used for these cycling tests.....114

6.13 Temperature dependence of residual stress for BCB layer on silicon wafer after multiple thermal cycle tests. Peak temperature of 450 °C is used for these cycling tests.....115

7.1 Preliminary procedure for evaluation of wafer bonding and thinning.....120

7.2 Wafer bonding/thinning result for a processed wafer with two-level Cu/oxide interconnects (provided by International SEMATECH) bonded on a glass wafer. Right side: surface profile showing a step height of 900 nm across the Al pads. 121

7.3 Photo image of a Cu/oxide interconnect structures after bonding to a glass wafer using BCB and complete removal of the Si by grinding, polishing and TMAH etching [24,26].....122

7.4 Process flow of a typical double bonding/thinning procedure, permitting bonding and thinning integrity evaluation without inter-wafer interconnect processing [24,104]. 122

7.5 Wafer edge chipping after grinding/polishing of the top processed wafer to ~50 μm. Top wafer was bonded to a Si wafer with the baseline BCB bonding process [26,104].....125

7.6 The beam specimen configurations of the two types of processed wafers: (a) bonded wafer pair including Cu/low-k interconnects; (b) bonded wafer pair including Cu/oxide interconnects 125

7.7 Critical adhesion energies of fully processed Cu/low-k and Cu/oxide wafer: each processed wafers has different pre-cracked surfaces.....125

7.8 Optical images of weak interfaces of the two types of processed wafers: (a) bonded wafer pair including Cu/low-k interconnects; (b) bonded wafer pair including Cu/oxide interconnects. 126

7.9 Electrical tests of processed wafer before and after wafer bonding, thinning, and BCB removal processes. (a) Probability chart of 360k 0.25 μm via chain resistance. (b) Probability chart of comb-to-comb

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bridging current at 5V. Data provided by International SEMATECH [104] 127

7.10 Electrical tests of processed wafer before and after double bonding and thinning, and then BCB removal processes. (a) Probability chart of 360k 0.25 μm via chain resistance. (b) Probability chart of comb-to-comb bridging current at 5V. Data provided by International SEMATECH [104]. 128

8.1 The process flow of the bonding of wafers including via patterns and its beam specimen preparation 135

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ABSTRACT

Wafer-scale three-dimensional (3D) integration is recognized as an emerging technology to increase the performance and functionality of integrated circuits (ICs). When bonding with fully processed ICs, the back end bonding process must be fully compatible with IC back-end processing and IC packaging constraints. In particular, wafers must be bonded with temperatures less than 450 °C and with low pressure.

Bonded wafers should have high bond strength and low residual stress to be compatible with subsequent processing steps such as mechanical thinning, chemical-mechanical planarization (CMP), and thermal cycling. Several low-k dielectric polymers have been evaluated as potential bonding glues and baseline-bonding processes have been established. The fraction of bonded area has been examined by optical inspection after bonding silicon wafers to coefficient of thermal expansion (CTE)-matched glass wafers. Benzocylcobutene (BCB) was selected the baseline glue after achieving complete and reproducible void-free bonding with 200 mm diameter wafers.

Bond strength at the glue interface of bonded wafers with blanket films and bond strength of patterned structures including multi-level copper interconnect test wafers were quantified by four-point bending. Using four point bending, the following chemical and mechanical effects of BCB on the bonding integrity were evaluated; (1) BCB thickness, (2) BCB film preparation (*e.g.*, employment of adhesion promoter) and (3) material stack (*e.g.*, different types of silicon oxides and glasses).

The adhesion promoter recommended by the manufacturer increases adhesion energy by more than a factor of two for the baseline 2.6 μm thickness investigated with a Plasma enhanced chemical vapor deposition (PECVD) oxide interface. An adhesion energy of 31 J/m^2 with standard deviation of 2.7 J/m^2 is obtained with the adhesion promoter and 13 J/m^2 with standard deviation of 0.5 J/m^2 without the adhesion promoter. The increased adhesion energy with the adhesion promoter is attributed to reactions like strong covalent bond between adhesion promoter and BCB resin and siloxane bonds between adhesion promoter and oxide layer.

While the bond strength increases with glue thickness, thicker glue layers lead to higher aspect ratio inter-wafer interconnects. A BCB thickness of ~1 μm is promising in

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terms of both bond strength and the required aspect ratio of inter-wafer interconnects. A BCB thickness of 0.4 μm has a critical adhesion energy of 19 J/m^2 with standard deviation of 0.7 J/m^2 for bonded wafers that are coated with PECVD oxide, less than 31 J/m^2 obtained with 2.6 μm BCB, but still significantly greater than bonded SOI wafers (< 5 J/m^2).

The delamination in all oxide and glass wafer bonding occurs at the interface between the BCB and the oxide (or glass). The cohesion strength of BCB is the highest (> 34 J/m^2), and the BCB-to-glass adhesion energy is the lowest (9 J/m^2) even though the adhesion promoter certainly increases the adhesion between BCB and oxide (or glass).

Weak interfaces of the patterned wafers with copper interconnects and either an oxide ILD or a porous low-k ILD bonded onto 2 μm thermal oxide wafers are identified and bond strengths are quantified. The bond strength measured at the weak interface is 6 J/m^2 with standard deviation of 0.5 J/m^2 for porous low-k ILD wafer and 21 J/m^2 with standard deviation of 1.9 J/m^2 for oxide ILD wafer. The critical adhesion energy does not depend appreciably on which side of the wafer beam (either blanket silicon wafer or processed wafer) is pre-cracked. In addition, electrical properties of the patterned wafers are preserved after wafer bonding process.

The effect of thermal cycling on adhesion energy and residual stress is evaluated for the bonded wafer pairs that consist of a stacked layer including BCB and PECVD oxide buffer layer. The dominant stress release of the stacked layer after the "first cycle effect" is mainly due to the stress release of PECVD oxide layer. An optimization procedure for the thermal stability of BCB through thermal cycling is established. Decrease of stress hysteresis in the stacked layer of a PECVD oxide layer and a BCB of 88 % initial cure during the first thermal cycling is observed and leads to the increase of critical adhesion energy. To reach steady state, seven thermal cycles are required with 350 °C peak temperature resulting in 94 % BCB cure, while four thermal cycles with 400 °C peak temperature result in more than 95 % BCB cure. The result implies that four cycles at 400 °C peak temperature is the optimal point for the stabilization of BCB under the given thermal cycling conditions.

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CHAPTER 1
INTRODUCTION

1.1. Motivation of Wafer Bonding

The scaling of planar complementary metal-oxide-silicon (CMOS) integrated circuits (ICs) combined with chip-scale packaging continues to drive enhancements of productivity in integrated electronics. However, scaling beyond the 40 nm technology node is projected to be very expensive [1-4]. Furthermore, even the most innovative first-level single chip and multiple chip packaging approaches can limit IC performance capabilities and increase product cost [1,4]. Wafer-level 3D (three dimensional) monolithic processing is expected to help by reducing interconnect parasitics and lowering the interconnectivity cost [3]. The advantages of 3D processing are driving the current interest in wafer-level 3D ICs, bond/etch-back silicon-on-insulator (SOI), and wafer-level packaging (WLP) [2-4].

Wafer-to-wafer bonding is one of the key technologies to perform wafer-level 3D applications. Wafer-level bonding technologies are basically classified into two categories: fusion bonding and intermediate bonding.

Fusion bonding: This category is divided into two sub-bonding categories, direct wafer bonding (DWB) and plasma-activated bonding (PAB). During the DWB process, two silicon or silicon dioxide wafers are brought directly into close contact at room temperature and bonded. After the contact has been made, the weakly bonded wafer pair is heated to achieve high bond strength through the formation of covalent bonds. Alternatively, PAB uses plasma to increase the bonding surface area through the intentional roughening of the relevant surface(s) and creating reactive dangling bonds. Using PAB, moderate bond strength (< 5 J/m^2) can be obtained at low processing temperature (around 400 °C) [4].

Intermediate bonding: Unlike fusion bonding, this technology involves the insertion of material between two substrates, followed by heating and compression of the bonding pair. Three types of materials are often used as intermediate materials: metals with low eutectic temperatures, glasses with low melting temperature, and polymers. Essentially,

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there is metal-to-metal bonding for metals with low eutectic temperature, anodic bonding for melted glass, and glue bonding for polymeric materials.

Intermediate bonding usually involves lower operational temperature range than fusion bonding. Wafers bonded through an intermediate routinely show a larger fraction of bonded area and higher bond strength than wafers bonded using fusion bonding. In addition, glue bonding using polymers has the ability to accommodate wafer-level non-planarity (*e.g.*, wafer bow) and particulates at the bonding interfaces. Polymeric glue bonding is emerging as an enabling technique critical to the manufacturing of 3D ICs. Chapter 2 provides a detailed description of these bonding techniques.

1.2. Motivation of 3D IC Integration

Interconnect delays are becoming a bottleneck for IC performance due to an increase in chip size and a reduction in the minimum feature size. Although silicon BEOL interconnect technology has advanced with the advent of copper/low-k damascene patterning, interconnect delay is expected to be serious below the 130 nm technology node, limiting chip performance [4-7]. It is therefore critical to find alternate technologies to overcome this problem.

Several analyses have demonstrated that a large number of the long horizontal interconnects commonly used in 2D structures can be replaced by short vertical interconnects through 3D-chip integration [4,7]. Moreover, a 3D architecture can accomplish increased functionality and offer extra flexibility in system design, while maintaining the cost advantage of monolithically fabricated interconnects [6,8-10]. For example, logic gates can be located close to each other with multiple active layers. This can give rise to considerable reduction in *RC* delay and enhancement in performance of logic circuits [4].

This 3D IC technology can also be used to establish systems on a chip (SOC), by placing circuits with different voltages and performance requirements in different layers. For example, circuits that have logic structures in the first silicon layer and memory circuits in the second layer might be attractive [4]. Figure 1.1 is a simplified application-oriented drawing of the 3D platform for heterogeneous system applications. The only

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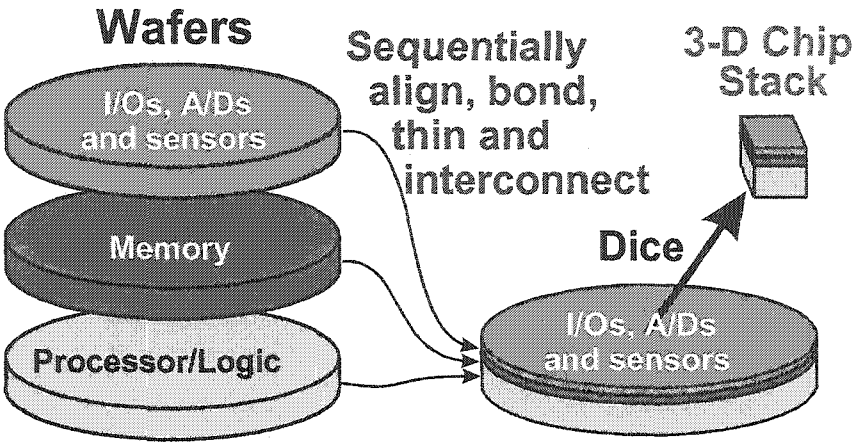


Figure 1.1: 3D platform for ICs and heterogeneous systems.

requirements are that the wafers are of the same diameter and have the same die size to realize the inter-wafer interconnection scheme [6].

Although the concept of 3D integration was suggested by Lee *et al.* in 1979 [11], it remained as a need for the future, because IC performance was device limited [4]. However, with the growing importance of *RC* delay, this technology is regarded as an alternative that cannot only maintain chip performance well beyond the 130 nm node. It will also inspire a new generation of circuit design concepts. There are several possible fabrication technologies that can be used to realize multiple device layers separated by interlayer dielectrics (ILDs) for 3D circuit processing. The choice of a particular technology for fabricating 3D circuits will depend on the requirements of the system, because circuit performance is strongly affected by the electrical and thermomechanical characteristics of the fabricated structures. Process compatibility with conventional 2D technology will also be a major consideration. A brief description of these alternative methods follows:

Processed wafer bonding: This method includes wafer scale bonding between two fully processed wafers, on which chips are fabricated on the surface. Within this scheme, the chips (die) are completely stacked after wafer-to-wafer alignment. To bond the two wafers, Gutmann *et al.* [12] use polymeric glue, Rahman *et al.* [8] use metal-to-metal bonding with copper, and Guarini *et al.* [14] use direct wafer-to-wafer bonding. The backside of the bonded pair is thinned to allow further processing such as vertical via interconnect and/or bonding of more wafers. Some advantages of this technology are:

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1. Electrical properties of devices on all active layers can have similar performance, for products where this may be desirable.
2. Device processing temperature does not influence other device layers, as the wafers are fabricated separately.
3. Processing for each wafer can be optimized for the technology on that wafer.

The major limitation of this technique is any lack of precision during the aligning process, which constrains the inter-chip connection to be global metal lines [4]. As an alternative way to alleviate this aligning problem, chip-to-wafer scale 3D integration has been suggested. Bonding for stacking chips on a wafer can be considered in the same class as the processed wafer bonding [20,23].

Recrystallization: Kohno *et al.* [15] and Crowder *et al.* [16] proposed a method for fabricating a second silicon layer on top of an existing substrate that is to deposit polysilicon and to fabricate thin-film transistors (TFTs). To improve the performance of these TFTs, an intense laser or electron beam is used to recrystallize the polysilicon. This technique may not be practical for high performance devices because of the high temperatures applied during melting of the polysilicon and also due to difficulty in controlling the grain sizes. However, high performance TFTs fabricated using low temperature processing, and even low-temperature single-crystal silicon TFTs, have been recently demonstrated that might be employed to fabricate advanced 3D ICs [15-16].

Silicon epitaxial growth: Another method for forming silicon layers is to etch a hole in a passivated wafer and epitaxially grow single crystal silicon through windows opened in the ILD, as initially suggested by Neudeck *et al.* [17]. The silicon crystal grows vertically and then laterally, to cover the ILD. The quality of these fabricated devices can be as good as those fabricated on the wafer surface since the grown layer is single crystal with few defects. However, the high temperatures (1000 °C) involved in this process cause significant degradation in the quality of devices on lower layers and prohibit its use over metallized layers. Low-temperature silicon epitaxy using high vacuum chemical vapor deposition (CVD) has been developed in an attempt to deal with this drawback.

Solid phase crystallization (SPC): As an alternative to high-temperature epitaxial growth, low-temperature deposition and crystallization of amorphous silicon, which passivates the lower active layer devices, can be employed. The amorphous film can be

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randomly crystallized to form a polysilicon film. Eliminating grain boundaries can enhance TFT performance. For this purpose, local crystallization can be induced using low temperature processes. Subramanian *et al.* [18] suggested this method using patterned seeding of germanium, and Lee *et al.* [19] proposed metal-induced lateral crystallization. This technique offers the flexibility to create multiple active layers that are compatible with current processing environments, and recent results prove the feasibility of building high-performance TFTs at low processing temperatures that can be compatible with lower level metallization.

The *International Technology Roadmap for Semiconductors* (ITRS) [1] projects that 2D integration will require more metal levels to build logic megacells that double in size every two years. The number of metal levels predicted for beyond 2005 using a stochastic wiring distribution model [1] reaches unattainable values, such that by 2014 the number of metal levels is almost an order of magnitude larger than what is projected by the ITRS [1]. This result emphasizes that substantial changes in design methodologies, technologies, and architectures are needed to cope with metal wiring requirements. One possible solution to this problem is the 3D-integration of transistors. It has been predicted that interconnect performance is significantly improved by using 3D IC integration [10,14]. Key concerns for the 3D-circuits are power dissipation, associated thermal heat sinking requirements [20], potential new crosstalk issues [21-22], and additional complexity introduced in the fabrication technology [23].

1.3. Thesis Organization

The rest of this thesis is organized as follows. Chapter 2 describes five wafer bonding technologies and low-k polymeric glue alternatives. The 3D IC integration approach being pursued at RPI is also briefly described in this chapter. Chapter 3 reviews the experimental techniques used in the research reported in this thesis; the four point bending technique for quantitative bond strength measurement and the wafer curvature technique for residual stress measurement are introduced. The statistical treatment used for bond strength data is presented, and some with key results are outlined. Material characterization techniques used to evaluate changes in chemical structure of glue and measure the glue thickness are also introduced. The baseline wafer bonding procedure

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using polymeric glue is described in this chapter as well. Chapter 4 presents the procedures used to screen glues.

Chapter 5 presents quantitative evaluation of BCB bond strength using four-point bending. In particular, the dependences of bond strength on using an adhesion promoter with BCB, on BCB thickness, and on the material stack of BCB are investigated, and the results are explained. Baseline process parameters that affect bond strength are also presented. Chapter 6 describes the effects of thermal cycling on bond strength and residual stress of BCB bonded wafer pairs with PECVD oxide layers. Chapter 7 addresses the evaluation of bond strength for bonded patterned wafers and the identification of the weak interface of these patterned wafer stacks. In addition, electrical properties of the patterned wafers are investigated after the wafer bonding process, and the results are presented. Chapter 8 provides a summary of this thesis, presents conclusions drawn from this study, and suggests future directions for polymer based wafer bonding research.

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CHAPTER 2
TECHNICAL BACKGROUND

2.1. Overview

Applications such as monolithic wafer-scale 3D ICs, WLP and bond/etch-back SOI (silicon on insulator) require bonding of processed wafers. Wafer bonding is one of the processes that distinguishes 3D processing from conventional planar ICs and packaging of chips [1,4,7]. This chapter presents several applications of 3D integration and bonding technologies. Particular focus is placed on monolithic wafer-scale 3D ICs, which are being pursued at RPI; *i.e.*, wafer bonding with dielectric glues, a three-step thinning process of grinding, polishing and etching, and inter-wafer interconnection using copper damascene patterning [24-26]. The features of dielectric glue bonding technology and chemical, mechanical and thermal properties of four low-k polymeric glue alternatives are also presented. The importance of bonding glue characteristics in obtaining high bond strength and void-free bonding, and to relaxing pre-bonding wafer planarization requirements is a key to process compatibility with standard IC processes [3].

In this chapter, applications for wafer bonding such as bond/etch-back SOI and 3D ICs are introduced. Wafer scale 3D IC processing using dielectric glues and copper damascene inter-wafer interconnects, as pursued at RPI, is emphasized. Additionally, commonly used bonding techniques are listed and their features are introduced. This material provides a context for the research into dielectric glue bonding with low-k materials.

The advantages and features of low-k polymeric glue alternatives are highlighted, and the chemical and physical properties of the alternatives are addressed. These properties are used in subsequent chapters to help explain experimental results. Finally, the beam bending theory based on fracture mechanics is introduced. This beam bending theory is used to evaluate the bond strength at the interface containing the bonding glue, a key characterization procedure implemented in this thesis research.

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2.2. Applications for Wafer Bonding/Attachment

In this section, applications for wafer bonding/attachment are introduced. In particular, "bond and etch-back" SOI and Micro-Electro-Mechanical Systems (MEMS) are the current main applications using wafer-bonding technologies [27-28]. First, the bond and etch-back SOI and the Smart Cut® technologies are introduced along with fusion bonding technology [28]. Various 3D IC integrations are next described with the use of both fusion bonding and intermediate bonding technologies. Applications in MEMS are not discussed. Applications in 3D IC and heterogeneous integration are discussed [29-30,32,35].

2.2.1. Bond and Etch-Back SOI

The bond and etch-back technique used to form SOI is based on bonding two silicon wafers, which are either a hydrophobic Si wafer and a hydrophilic SiO_2 wafer, or two hydrophilic SiO_2 wafers. Figure 2.1 shows the process flow to obtain a bonded SOI wafer, including thinning of the device wafer. Fabrication of an SOI wafer consists of three main processes: (1) initial bonding, (2) annealing, and (3) thinning of one of the wafers [27-28]. The two silicon wafers are bonded with a SiO_2 layer that serves as the buried insulator in the SOI, and is called a buried oxide (BOX). Thereafter annealing takes place at high temperatures (1100 °C and above). After contact and annealing, one of the wafers is etched to a thickness suitable for SOI applications [28]. A typical SOI structure made by this method is an active SOI layer which is a few tenths of a micron thick on top of a BOX layer whose thickness is on the order of 1 μm [1].

Initial bonding and annealing: When two flat, hydrophilic surfaces such as oxidized silicon wafers are placed one against the other, bonding occurs naturally, even at room temperature. The contacting forces are believed to be caused by the attraction of the hydroxyl groups (OH) absorbed on the two surfaces [38-39]. This attraction can cause spontaneous formation of hydrogen bonds across the gap between the two wafers and propagates from a first site of contact across the whole wafer in the form of a "contacting wave" [28].

After the wafers are bonded at room temperature, it is customary to anneal the structure to strengthen the bond [27,38], whose strength increases with annealing

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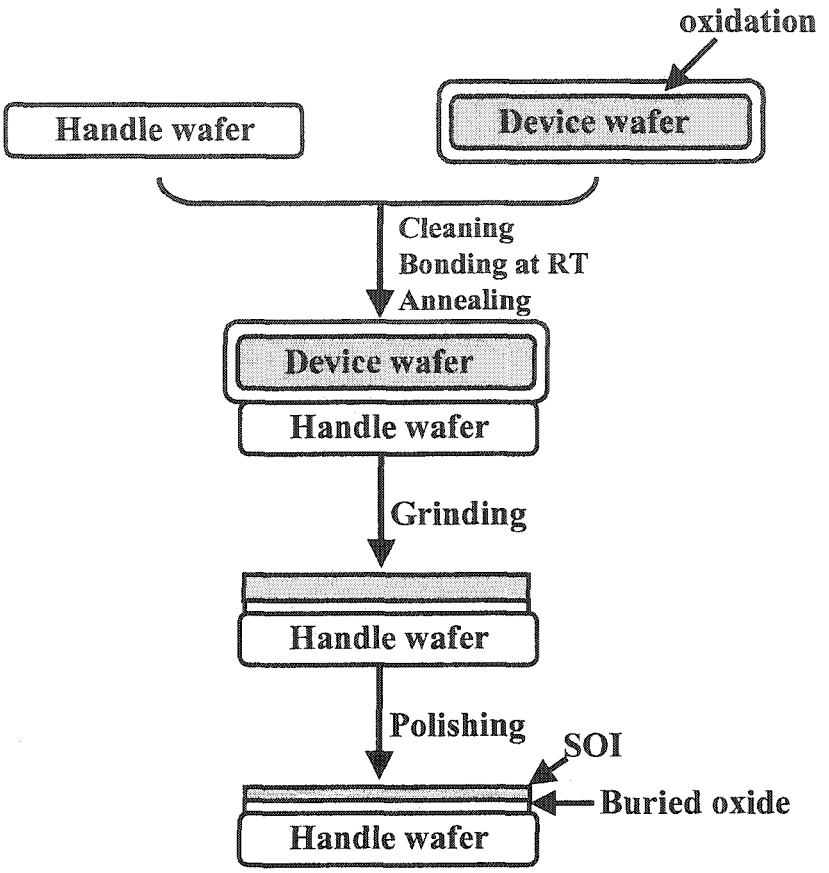


Figure 2.1: Bonded SOI wafer process flow including grinding and polishing [28].

temperature. The annealing steps for bond strengthening that occur at different temperatures can be distinguished. The first step starts around 300 °C and the bonds between hydroxyl groups are replaced by Si-O-Si bonds. At higher temperatures (1100 °C and above), viscous flow of the oxide layer allows for complete "welding" of the wafers. The quality of bonding depends on the roughness of the surfaces in contact as well as on the bond reaction(s) [28,38].

When the wafers are annealed at 300 °C and above, the following reaction takes place: Si-OH + OH-Si → Si-O-Si + H_2O. As a result of water vapor formation during the reaction, voids appear between the bonded wafers. These voids are called "intrinsic voids" and they disappear at higher temperatures, as the water reacts and oxidizes the silicon (as in a thermal wet oxidation process). The hydrogen produced by the latter reaction diffuses out of the wafers [27-28].

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Another type of void, called "extrinsic voids" is caused by the presence of particulates between the wafers. Voids with a diameter of several millimeters are readily created by particles of 1 μm or less in size [27]. The extrinsic voids are not completely eliminated by high-temperature annealing. The only way to obtain void-free bonding is to clean the wafers with ultra-pure chemicals and water and to carry out all bonding operations in a clean environment. Practically, besides cleaning, the length of time during which the cleaned wafers are left in a clean environment before bonding significantly influences the surface quality. Not only particles but also other contaminants are absorbed on cleaned wafers. For example, the creation of voids caused by hydrocarbons is increased when wafers are left for a long time after cleaning. The amount of contaminants, such as boron present at the bonding interface, increases monotonically when wafers are left sitting after the cleaning process [27].

Etch-back thinning: After bonding and annealing of the wafers, the top wafer is thinned down from a thickness of over 700 μm (200 mm diameter wafer) to a few micrometers or less in order to be useful for SOI device applications [28]. Grinding followed by polishing or plasma assisted chemical etching is used for the thinning. Currently, Smart Cut® is also used as a thinning technique, and it provides a way of getting a crystalline film on a non-crystalline support [27].

In the etch-back process using grinding and polishing, the total thickness of the bonded wafer pair is controlled through the backside of the bonded wafer that acts as a reference plane. The SOI thickness uniformity strongly depends on the total thickness variation (TTV) of both the handle wafer before bonding and the thinned SOI after bonding [27]. Additional thinning is applied after grinding because the SOI uniformity should be better than 0.5 μm, which is total thickness of SOI after the additional thinning, and the mechanical damage to the surface should be minimized [28]. Surface polishing or etching is desired for the additional back-etch technique to reduce TTV and mechanical damage [28].

Polishing is generally performed by chemical mechanical planarization (CMP) [27], and after the damage is removed from the surface, it looks like a mirror with a surface roughness that can be as little as 1 Å RMS (root mean square) [28]. Basically, the same method for bulk wafer polishing is applied to SOI polishing, but there are still two

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difficulties that have to be overcome. One is the control of the depth of SOI layer removal in order to reach the required SOI thickness. The other is the minimization of SOI thickness non-uniformity. Modifying the polishing process so that the thickness of the SOI layer can be measured while the wafers are still on the polishing plate can solve the first problem. This modification allows the polishing and thickness measurements to be repeated several times. It improves not only the film thickness itself but also the uniformity of SOI wafers [28]. The second difficulty concerning thickness uniformity can be improved by placing an SOI wafer in the center of a polishing plate with dummy oxidized wafers in the surrounding area. The application of a single wafer polisher also has the same effect. The obtainable uniformity is expected to improve continuously, corresponding to the development of processes such as grinding and polishing [27-28].

Unlike the polishing method, the plasma-assisted chemical etching technology uses chemical gas as etchant. This method is used to improve the thickness uniformity of bonded SOI wafers that have been thinned to 1~5 μm by conventional methods [28]. SF_6 is used as a reactive gas, and is activated when plasma reaches the area. After this process, SOI layers obtained have an average thickness of 0.1 μm with a standard deviation of 3 nm [28].

The wafer bonding allows different materials to be connected and can provide a way of getting a crystalline film on a non-crystalline support. However, obtaining precise thin films is still the main difficulty in this application. The Smart Cut® technology enables thin crystalline layers to be placed on any kind of substrate. This technology is based on implantation and wafer bonding [28]. Ion implantation using H_2 or He gas induces formation of a weakened layer located at the mean ion penetration depth and results in delamination of a thin film from a thick substrate. Wafer bonding and layer transfer enable different materials to be associated to form multi-layer substrates. This Smart Cut® process, first developed to obtain SOI materials, is now used as an industrial process that provides high quality materials in large quantities [28].

Figure 2.2 shows the process flow of the Smart Cut® technology [28]. This process flow includes: (1) hydrogen implantation into substrate A, which forms a weakened layer, (2) bonding of substrate A to a support B, (3) splitting occurs along the weakened layer,

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which induces the transfer of a thin layer from the substrate A onto the support B, and (4) a final treatment to remove the surface roughness left after splitting [28].

This process has several advantages from both technical and economical perspectives. Among these advantages, the possibility of transferring a thin layer of good thickness homogeneity with a high crystalline quality onto different materials deserves to be highlighted. The possibility of reusing the remainder of the implanted substrate may be key to drastic cost reduction compared to other bonding techniques [27].

2.2.2. Three-Dimensional (3D) ICs

3D IC approaches based on wafer bonding and inter-wafer interconnects are expected to provide high performance interconnects and/or to enable high density multi-functional integration [3,5]. They generally involve several major processing steps, including wafer-to-wafer alignment, wafer-to-wafer bonding, wafer thinning, and inter-wafer interconnection [4]. In terms of wafer bonding, three major approaches are under investigation: (1) direct wafer bonding, (2) metal-to-metal bonding, and (3) dielectric

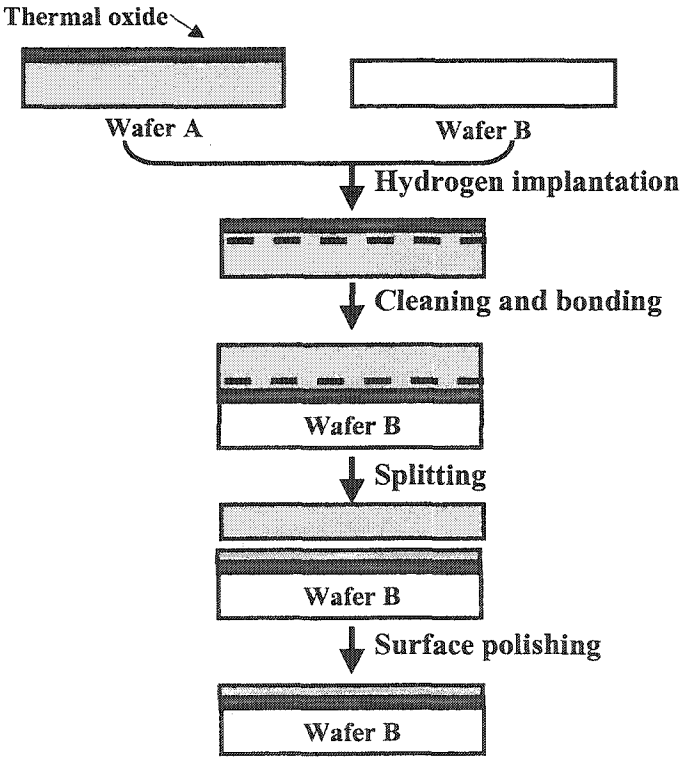


Figure 2.2: Schematic of process flow of the Smart Cut® technique [28].

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glue bonding. Wafer alignment and thinning techniques vary from one 3D IC approach to another [9,32-33] and are also application specific.

Direct wafer bonding for 3D IC applications requires a process compatible with semiconductor BEOL protocols, such as low bonding temperature, low bonding pressure and damage-free atomic level surface planarization and passivation [3,39]. In metal-to-metal bonding, metal bonds can also serve as inter-wafer interconnects. The bonding material candidates include copper [33], solder [34] or micro-bump [9] with underfill. This approach is generally suitable for two-wafer level 3D ICs. In dielectric glue bonding, inter-wafer interconnects are formed by high aspect vias through the thinned top wafer, through the bonding glue, and into the top of the multilevel on-chip interconnect of the bottom wafer. These glues can be curable polymers such as BCB, polyimide or other adhesives [9,32,34].

Inter-wafer interconnection approaches include copper damascene patterning [32], tungsten fill and etch-back [29], and through wafer fill (either poly-Si [9] or metal [33]). Tungsten fill and etch-back inter-wafer interconnection were used by Fraunhofer Institute in 1995 [23,36]. Since tungsten was used as via filling material in this application, the etching process after filling of vertical vias was easy to carry out (no need of CMP). However, since the resistivity of tungsten is higher than that of copper, its electrical properties including RC delay was poorer than those of copper. Compared to the tungsten fill process, copper damascene process is an advanced approach because this patterning technique is compatible with horizontal Cu/low-k ILD interconnect schemes and improves electrical performance of the vertical interconnects. Unlike the tungsten fill approach, in the copper damascene process, wafers are bonded and etched back first, and the etching/filling process of vertical vias is carried out later.

There are several ongoing 3D IC approaches using the above-mentioned unit processes such as wafer-level bonding, etch-back and vertical interconnections. Guarini *et al.* [14] presented a 3D IC technology that utilizes SOI wafers, glue bonding for stacking a handling wafer, and direct wafer bonding for stacking multiple circuit layers. The 3D IC process starts after conventional SOI FEOL device and BEOL metallization processes. The processed SOI wafer is bonded to a glass-handling wafer using polymeric glue. The original silicon substrate is then thinned by grinding and etching to the buried

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oxide (BOX) layer, which is used as an etch stop. Aligning with other circuit layers is facilitated because the stacked wafer pairs are transparent. After the device wafer is bonded to another device wafer or a growing stack of device wafers, the glass-handling wafer is released by laser ablation, and vertical interconnect vias are drilled/filled with metal interconnects to connect the two circuit wafers.

Guarini *et al.* [14] evaluated the electrical integrity in three main stages: (1) after CMOS fabrication, (2) after a "simulated" lamination process, in which pressure and temperature required to adhere the processed wafer to glass are applied without actually completing adhesion, and (3) after a full attachment to glass and an anneal to simulate the thermal processing required for the second bonding step. A linear relationship between drain current and threshold voltage of long channel *n*FETs indicate that these processes do not influence the channel mobility. They also measure electrical characteristics like ring oscillators and via chain test structures. Ring oscillator results show a slight increase in stage delay after processing with high circuit yield. Via chain test structures are used to evaluate the effects of processing steps on back-end characteristics. The results show higher resistivity for metal lines that go through the glass release step, which may result from an incomplete adhesive strip [14].

Burns *et al.* [29] proposed 3D image sensor technology that utilizes SOI wafers and glue bonding to stack multiple circuit layers. The 3D image sensor consists of glue bonding between an SOI wafer with imaging circuits and an SOI wafer with pixel-parallel A/D converter circuits with vertical interconnects between them. Figure 2.3 shows a schematic of the process flow for 3D image sensor fabrication and Figure 2.4 illustrates the inter-wafer interconnect structure and SEM image of the image sensor. The image circuits are fabricated in a 10-μm epitaxial layer on a 0.3 μm SOI layer with 1 μm BOX (SOI buried oxide). The epi thickness was chosen to maximize optical performance in the visible spectrum. A/D circuits are fabricated in a 1 μm SOI layer with a 1 μm BOX. Both wafers are processed with the same two-level metal, 0.8-μm CMOS process.

Prior to CMOS fabrication, silicon trenches are etched through the SOI layer of the A/D wafer and filled with TEOS oxide to form channels through which 3D vias are etched to interconnect the two active layers. Following fabrication, the A/D wafer is inverted, aligned with imager wafer, and bonded with a 3 μm thick layer of glue. Then

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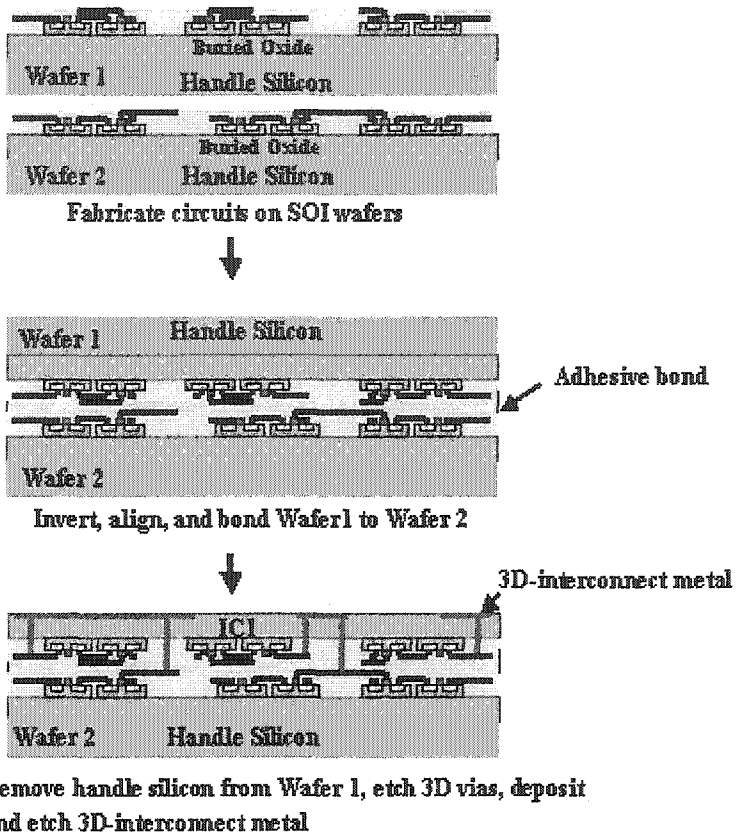


Figure 2.3: Schematic of process flow for 3D image sensor fabrication. Adapted from [29].

the bulk silicon of the A/D wafer is removed, using the BOX layer as an etch stop to produce a thin uniform active layer. A set of vertical interconnect vias is etched through the BOX, trench, and deposited oxides of the A/D wafer to expose metal pads on the first metal layer of the A/D wafer. Next a deep set of vias is patterned and etched fully through the A/D wafer and polymeric glue to expose metal pads on the second metal layer of the imager wafer, and the via is filled with metal.

The 3D circuit is inverted and bonded to an oxidized silicon wafer for mechanical support, and the bulk silicon is thinned from the imager wafer to expose the epi layer for backside imaging. Bond pads are patterned and etched through the BOX and 10-μm silicon layers to expose pads on the first metal layer of the imager wafer. The 3D via size is 6-μm square and is 2.7 and 7.5-μm deep for the shallow and deep vias, respectively. An aluminum alloy is deposited and patterned to connect the metal pads of the two wafers.

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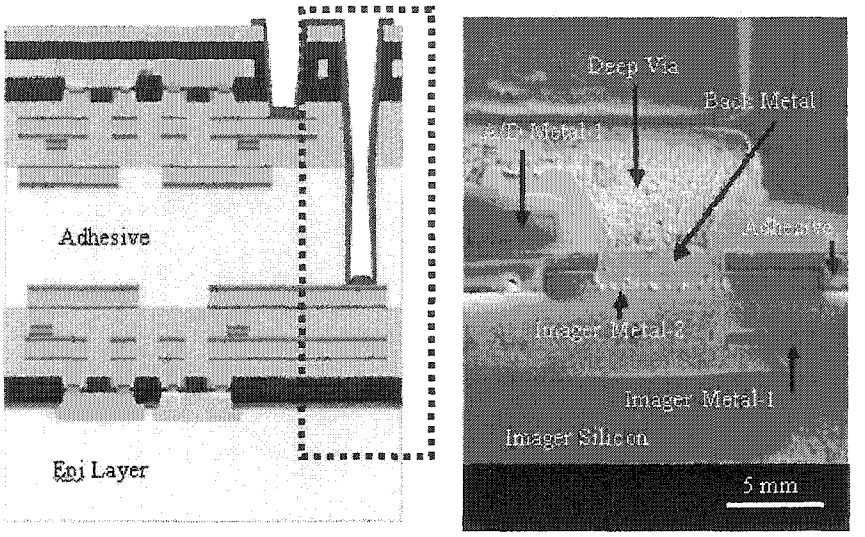


Figure 2.4: Inter-wafer interconnect structure and SEM image of the 3D image sensor. Adapted from [29].

After processing, the contact resistances of shallow and deep via chains were measure and ring oscillators were characterized. The resistance results showed that via etching through the polymeric glue did not degrade the contact either by undercutting the polymeric glue or by contaminating the metal pad. 3D ring oscillators constructed by coupling of an inverter in the imager wafer with an inverter in the A/D wafer with 6-μm 3D vias showed "delay per stage" performance better than that of 2D oscillators [29].

Reif *et al.* [8,13,30] proposed a 3D IC integration process using an SOI wafer and a metal thermo-compression technique to bond two processed wafers. Figure 2.5 shows a schematic process flow for this approach. As an initial process, copper patterning of an SOI device wafer is performed. To facilitate subsequent processing of the wafer, a handling wafer is bonded with the copper patterned SOI wafer. After the handling wafer is bonded, the silicon on the back of the SOI wafer is removed to the BOX layer, followed by via etching and filling processes. Via filling consists of: (1) oxide spacer that may be deposited using O_3/TEOS plasma enhanced chemical vapor deposition (PECVD) method, (2) CVD TiN for metal liner, and (3) CVD W for via fill. Subsequently, the copper is patterned, and the two patterned wafers are aligned and bonded. Alignment accuracy is +/- 3 μm. After the bonding process, the handling wafer is released. Laser ablation or grinding/polishing is generally used for releasing handling wafer [30].

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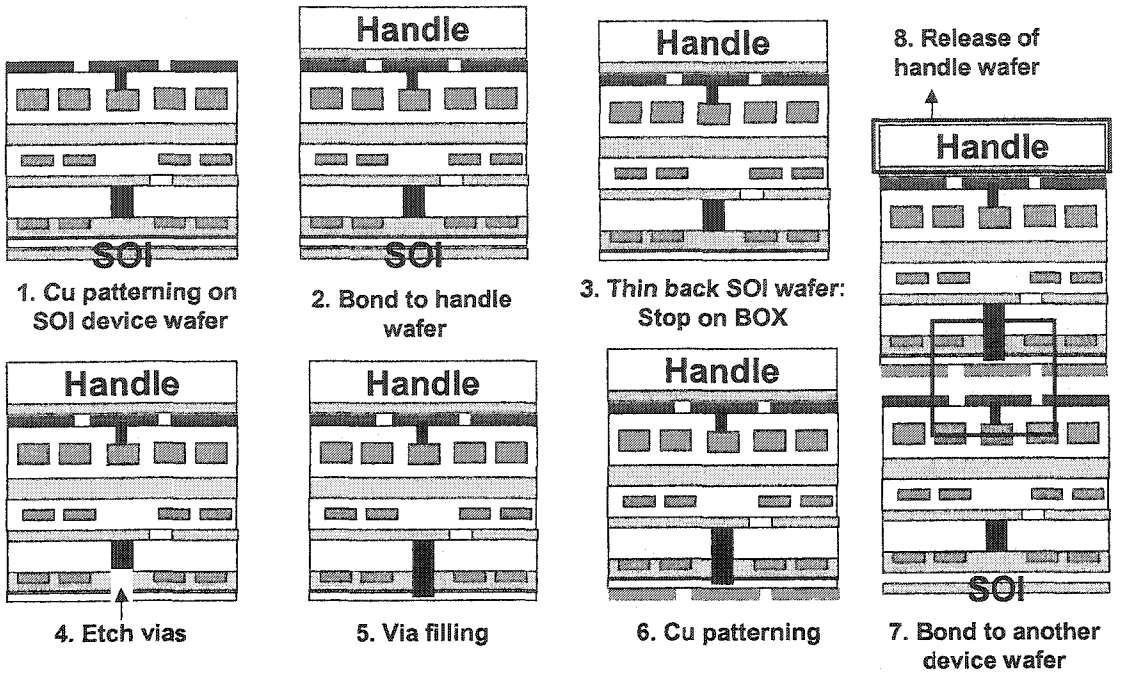


Figure 2.5: Schematics of process flow of 3D IC structure [30].

Lee *et al.* [9,35] reported a parallel 3D image-processing IC, whose conceptual configuration is shown in Figure 2.6. The 3D structure consists of four main layers: (1) an image sensor array layer, (2) an amplifier and A/D converter array layer, (3) a data latch (register) and masking circuit layer, and (4) a processor array and output circuit layer. These four layers are connected vertically, and 2D image signals are transferred in the vertical direction and within each layer in parallel.

Figure 2.7 is a schematic of the process flow. The device wafer with buried

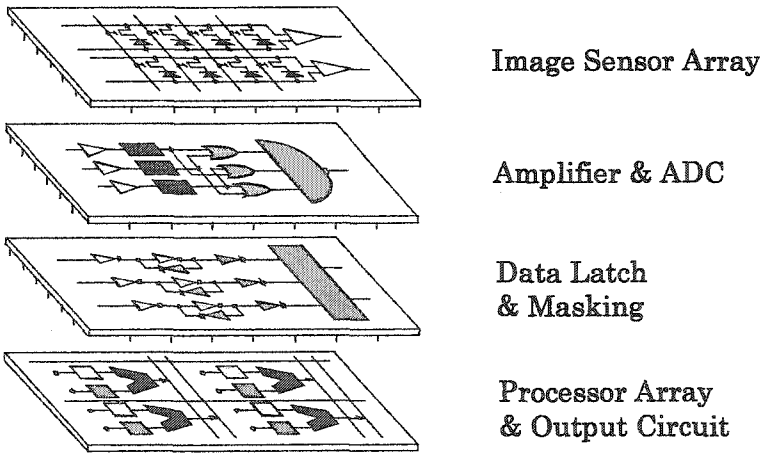


Figure 2.6: Conceptual configuration of 3D image sensor chip with 3D structure. Adapted from [35].

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interconnections is bonded to a quartz glass handling wafer using epoxy, and the backside of the bulk silicon wafer is thinned to about 30 μm by mechanical polishing and CMP. After thinning, silicon dioxide is deposited using PECVD at a low temperature and is patterned by reactive ion etching (RIE) to form contact holes for back-surface microbumps. Subsequently, the thinned wafer is aligned/bonded with another wafer. By repeating this sequence, a multilevel 3D wafer stack is achieved. Key processes of their 3D structure are microbump formation, wafer alignment, wafer bonding, and wafer thinning [35].

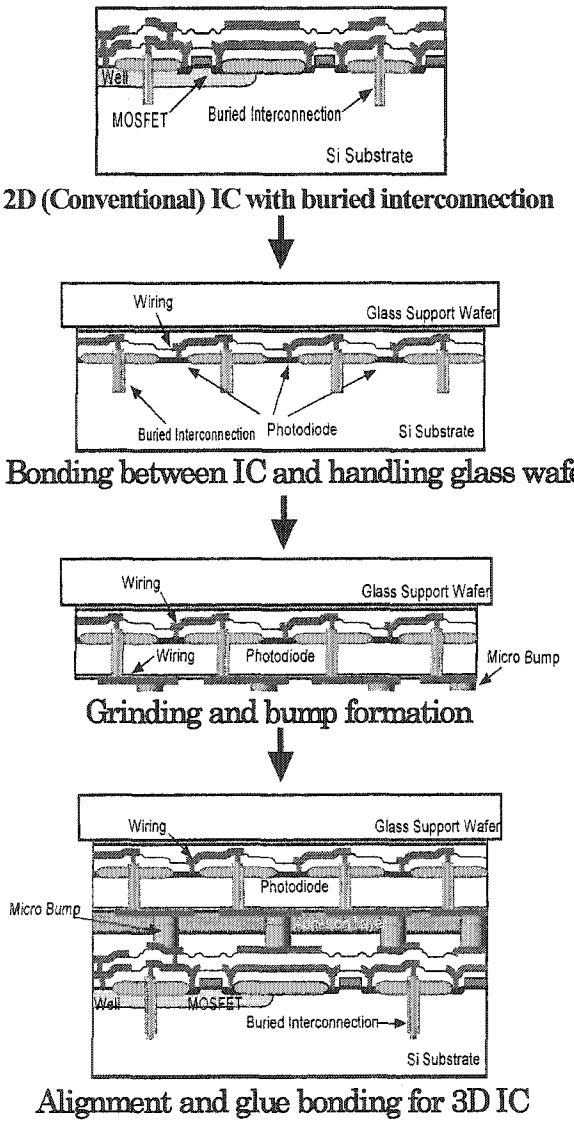


Figure 2.7: Schematic of process flow of parallel 3D image processing. Adapted from [35].

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One of the challenges is to etch deep vias in order to form vertical interconnects with buried active layers. The high aspect ratio vertical vias (2.5 μm wide and 60 μm deep) are etched by inductively coupled plasma (ICP) etching. After etching, the silicon trench is oxidized, then filled with polysilicon using low-pressure chemical vapor deposition (LPCVD) [35].

Microbumps acting as electrical connections between the two wafers are constructed on the surface using lift-off. Then, the thinned wafer is aligned with the bottom wafer with an alignment tolerance of 1μm. This aligner also acts as a bonder by providing a uniform compression for aligned wafers, and the temperature can be raised to approximately 200 °C using an UV lamp [35].

Two wafers are bonded using an epoxy adhesive layer. The electrical connection between the upper and lower wafers is achieved through the buried interconnections and metal microbumps. Electrical contact resistance of the microbumps is measured when they are formed on Al wiring. They also measured the device characteristics of NMOS transistor and there was no significant change in device performance, which means no notable degradation of active layers between "after NMOS fabrication" and "after full attachment" including inter-wafer interconnects. After chip processing, this 3D image processor showed faster clock frequency than conventional 2D IC based imagers [9].

2.3. 3D ICs using Dielectric Glues and Damascene Inter-Wafer Interconnection

Gutmann *et al.* [12] and Lu *et al.* [5,37] proposed a 3D IC integration approach that uses thermo-compression bonding with low-k polymers to bond two processed wafers, and copper damascene to create inter-wafer interconnects. A schematic of the resulting structure is depicted in Figure 2.8. In this approach, fully processed wafers with multilevel interconnects are aligned and bonded using a dielectric glue, followed by thinning the top-wafer to < 10 μm using grinding, CMP, and wet etching. Subsequently, inter-wafer interconnects are formed using a copper damascene patterning process, including high aspect ratio via etching, copper/barrier deposition and CMP of copper/barrier metal layer.

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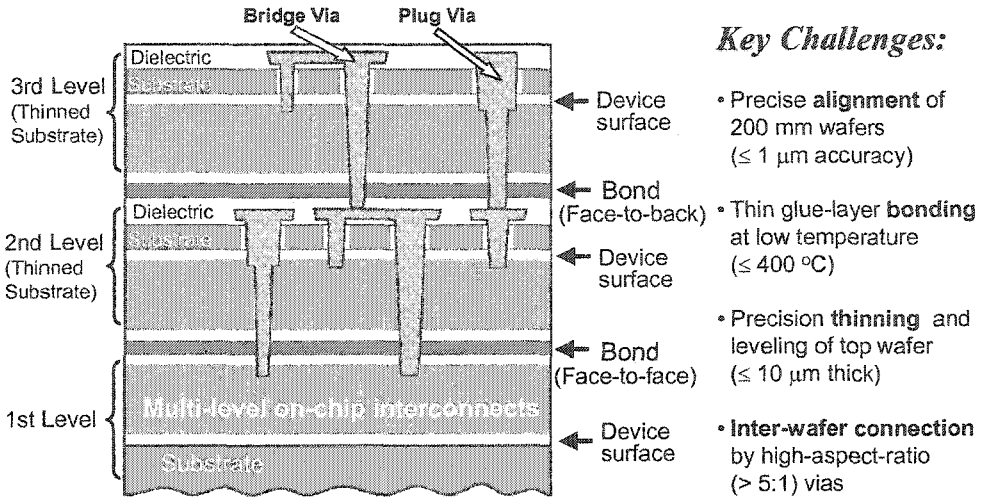


Figure 2.8: Schematic of a test vehicle using wafer bonding, showing bonding interface, vertical inter-chip vias (plug- and bridge-type), and "face-to-face" and "face-to-back" bonding [32].

This approach, compared to other bonding techniques, presents three key advantages; (1) the ability of the dielectric glue to accommodate wafer-level non-planarity and particulates at the bonding interfaces, (2) there is no handling wafer, *i.e.,* the thinned silicon is not transferred as is the case in other wafer-scale 3D approaches, and (3) the same basic approach can be used with multiple wafer stacks (more than 2 wafers).

Figure 2.8 lists four key processing challenges; (1) wafer-scale alignment accuracy, (2) highly reliable bonding, (3) wafer thinning and leveling control, and (4) inter-wafer via formation. Each of these processes should be compatible with semiconductor processing constraints, because an IC BEOL compatible baseline process is critical for a successful 3D IC fabrication technology [5,36].

In order to evaluate the processing feasibility and to establish design rules for inter-wafer interconnect technology, a four-layer mask set of via-chain test structures was developed, with features for evaluating both "bridge" and "plug" types of vias. Figure 2.9 illustrates the process flow of the inter-wafer interconnect fabrication, showing plug- and bridge-type vias. BCB (Benzocyclobutene) is used as polymeric glue due to its reproducible void-free bonding, low temperature processing, and the ability to deposit thin films by spin-on. Subsequent to wafer bonding, the backside of the top silicon is completely removed to simplify the interconnect process. Damascene BEOL processes are used for Cu metallization on the bottom wafer (Metal-1) and the top wafer (Metal-2).

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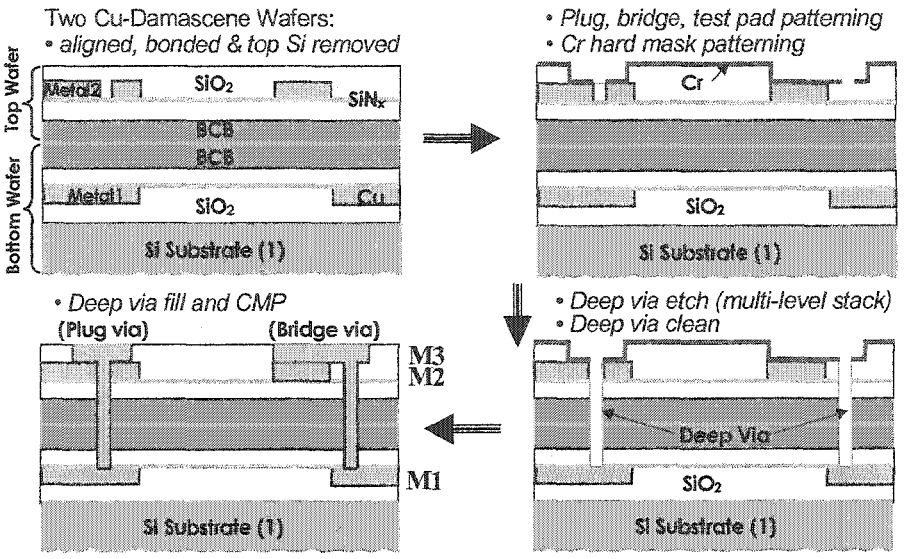


Figure 2.9: Inter-wafer interconnect process flow for via-chain structure fabrication [37].

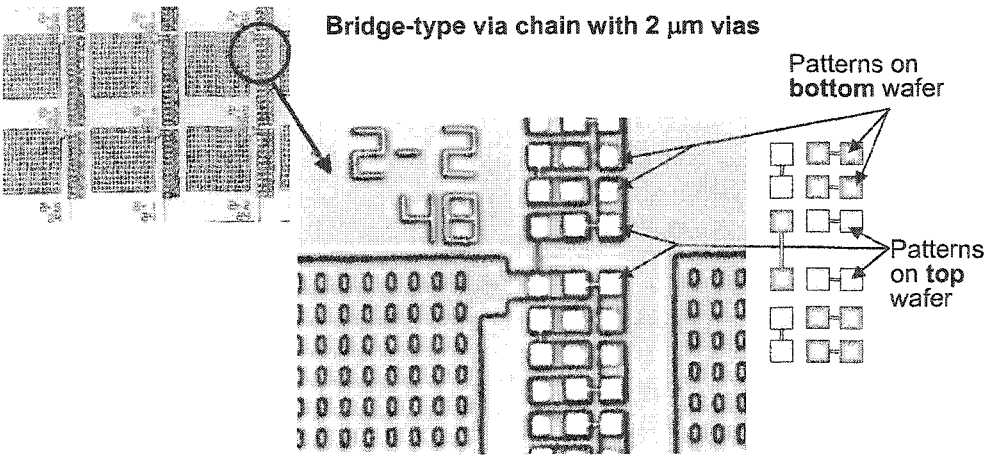


Figure 2.10: 200 mm wafer-to-wafer alignment accuracy with via-chain test structures, indicating 1 μm alignment can be achieved [37].

The bridge metal (M3) and the inter-wafer via are fabricated using an "inter-wafer interconnect damascene process". Photos in Figure 2.10 show bridge-type via-chain patterns for a two-micron via with different landing pads and chain lengths, prior to deep via processing. These photographs were taken on a pair of Cu-damascene wafers after alignment, bonding, top wafer thinning and patterning of bridge lines, plug pads and test pads patterning [37].

Inter-wafer interconnect formation for this via chain demonstration requires etching vias on the order of 10 μm deep, through a multi-level/multi-material stack (*e.g.*, SiO_2,

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silicon nitride, and polymeric glue layers). Control of the sidewall profile when etching a variety of materials is challenging, and the etch rate is not uniform due to different via-sizes and loading effects. For this test vehicle, a 0.2 μm chromium layer is used as the hard mask for the deep via etching. A design-of-experiment (DoE) procedure was used to study the deep via etch through various materials on either blanket films or multi-material structures through the use of an inductively coupled plasma (ICP) reactor [37].

Prior to via filling after etching, the vias are cleaned using a wet-clean and a plasma dry-clean. For via filling, a low temperature (< 300 °C) TaN CVD liner process is performed. The Cu CVD fill is performed in a modified Tokyo Electronic (TEL) Phoenix wafer cluster tool. After metallization, CMP of the structure completes the copper damascene process (colleagues at SUNY-Albany performed via etching and filling processes) [3].

Figure 2.11 shows top views of the bridge via-chain structures fabricated using the process discussed above. From Figure 2.12, it is observed that the bridge via-chain

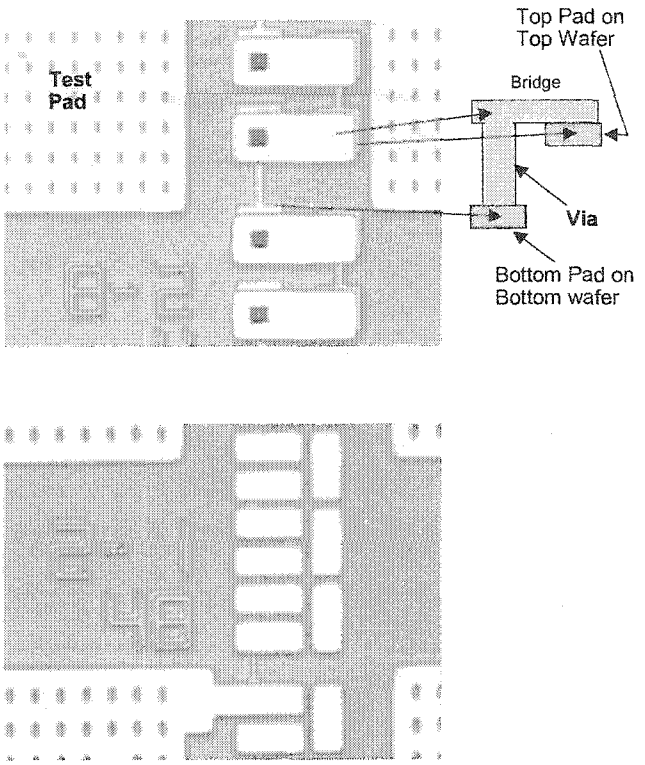


Figure 2.11: Top view of the via-chain structure for inter-wafer via sizes of nominal 8 μm (top image) and 2 μm (bottom image), showing wafer-to-wafer misalignment of ~1μm. Vertical vias connect bottom (M1) and top (M2) metals [37].

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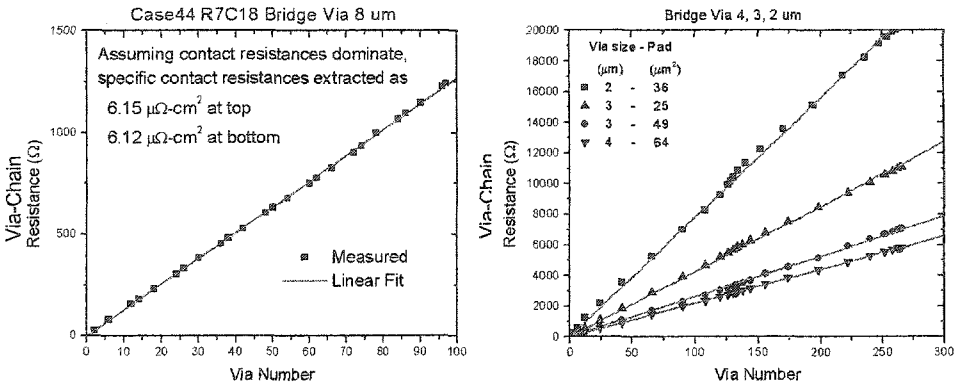


Figure 2.12: Via-chain resistance vs. via-chain length (via number): for nominal via size of 8 μm (left), for nominal via size of 2, 3, 4 μm. The nominal via landing pad is 12x12 μm² for 8 μm via chain (right) [37].

resistance depends on chain length (via number), via size and via landing pad areas. Though the via-chain specific contact resistance of ~6 μΩ-cm² is much larger than expected, the linear relationship between the chain resistance and chain length indicates the continuous and uniform 3D via-chain are demonstrated [37].

2.4. Wafer Bonding Technologies

In this section, wafer-bonding technologies along with their applications and characterization are introduced. Direct wafer bonding and plasma activated bonding techniques without the insertion of intermediate glue material are delineated [38-41]. Their merits and drawbacks and quantitative bond strength values are also presented. Among the intermediate bonding technologies, anodic bonding [47], metal-to-metal bonding [8,13,33] and dielectric glue bonding technologies [26] are mainly described. 3D applications using copper-to-copper bonding and low-k dielectric glue bonding are introduced and their characterization results for bond strength are described.

2.4.1. Direct Wafer Bonding (DWB)

Direct wafer bonding technology, used to bond two silicon wafers or two SiO_2 wafers together, is a sub class of fusion bonding and requires clean and mirror-polished surfaces [38]. When two clean silicon wafers are bonded, hydrophobic surfaces of the wafers are used for the bonding. On the other hand, when two SiO_2 wafers are bonded, hydrophilic surfaces of the SiO_2 wafers are used [28,39]. Cleaning by dipping in a HF solution to

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remove the native oxide layer is done to obtain hydrophobic surfaces, which consist of hydrogen saturated silicon surfaces [28,38]. After cleaning, the wafer surfaces are hydrophilic. In bonding using hydrophilic surfaces, oxide layers are grown on both the top and bottom wafers. Water molecules are then attached through intermediate OH groups such as silanol [38].

The two wafers first contact at room temperature in atmosphere. In order to minimize the number of particles between the wafers, the bonding process should be performed in a clean environment. While the wafers contact, bonding starts from the local contact point, which is ideally in the center of the wafer. The bonded area then spreads over the whole wafer within a short time. The speed of lateral spreading of the bonded area is independent of the wafer thickness and the distance to the wafer rim [39]. Also, the speed increases when bonding in a vacuum. In room temperature bonding, Van der Waals and hydrogen bonding interactions induce adhesion at the surfaces of bonded wafers. These interactions produce lower bonding energies than those associated with covalent bonding. Due to this lower energy, wafer bonding at room temperature is not strong [38].

Enhancement of bonding strength is achieved by a subsequent heating step, during which covalent bonds are formed. A suitable final temperature is around 1100 °C in the case of silicon-to-silicon wafer bonding [38,39]. With hydrophobic wafers, the heating process leads to a dehydrogenation reaction and silicon-silicon covalent bonding across the interface [39].

$$\equiv Si - H + H - Si \equiv\rightarrow \equiv Si - Si \equiv + H_2 \qquad (2.1)$$

At temperatures up to 600 °C, hydrogen diffuses along the bonding interface rather than into the silicon. Bonding of two hydrophilic wafers is similar to bonding of hydrophobic wafers, but there is an intermediate step involved. At the interface, initially there are water molecules adsorbed on hydrophilic oxides, these hydroxyl groups react with each other to form water molecules, viz.

$$\equiv Si - OH + HO - Si \equiv\rightarrow \equiv Si - O - Si \equiv + H_2O \qquad (2.2)$$

From this reaction, strong covalent bonds (siloxane bonds) start to form across the bonding interface at temperatures above 120 °C (see Figure 2.13) [38]. The water

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molecules produced oxidize the surrounding crystalline silicon and produce hydrogen molecules.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \quad (2.3)$$

In spite of advantages such as the use of no electric biases and ease of operation, this bonding approach has two main drawbacks [28,38]. First, since the deposition of on-wafer interconnects is performed before wafer bonding, the interconnects will undergo the high bonding temperatures. The conventional materials used for interconnects are aluminum and copper, and the metals can't maintain the interconnect structure stable at process temperatures over 500 °C. The adoption of silicides can be considered, but it requires another process step like deposition of a silicide layer. In addition, bonding strength is much lower than those of other bonding techniques. As seen in Figure 2.13, the bond strength for hydrophobic bonding is less than ~3 J/m^2 at 700 °C, as measured using a quantitative razor blade method, and the bonding strength of hydrophilic bonding is around ~2.5 J/m^2 at 900 °C, using the razor blade method [39].

2.4.2. Plasma Activated Bonding (PAB)

DWB is commonly used to fabricate silicon-based MEMS devices. However, as

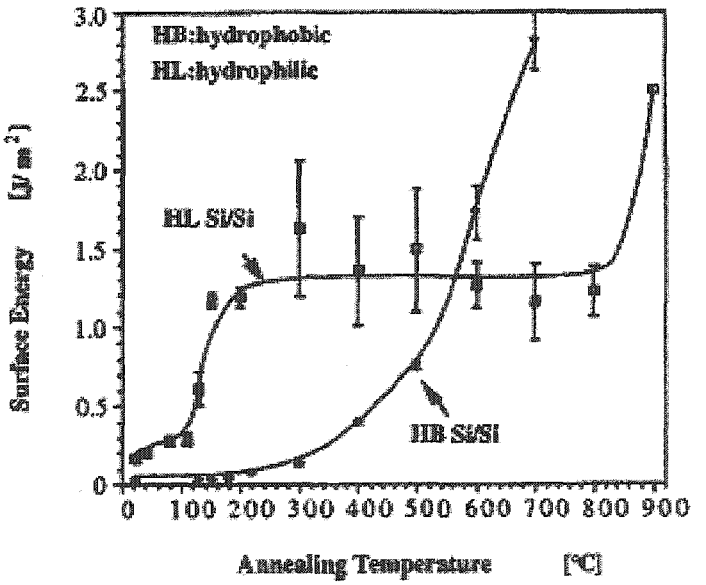


Figure 2.13: Saturation values of bond strength as a function of temperature after long-term heat treatments. Adapted from [38].

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mentioned in Section 2.2.1, high temperature anneals of up to 1100 °C have to be applied to reach a bond strength of ~3 J/m^2 [39]. Since the high annealing temperature does not fit with applications such as 3D ICs, low-temperature processing (below 400 °C) techniques compatible with BEOL, should be developed. One promising method to increase bond strength at moderate temperature is to use plasma treatment prior to bonding. Plasma activated bonding (PAB) is a chemical free process for wafer bonding, and bonded interfaces are shown to form hermetic seals. Successful PAB has been reported using O_2, N_2, NH_3 and Ar plasmas, but the bonding mechanism is under debate [40-41]. Plasma exposure affects a silicon or silicon dioxide wafer surface in different ways. Chemical reactions may take place, charges may be injected into the surface, and plasma bombardment may cause structural changes. Essentially, it is speculated that the oxygen plasma gives rise to chemical reactions with the silicon component, and the wafer surface is oxidized [41].

PAB using O_2 plasma has shown good bonding with high bond strength. Several groups have studied the surface of O_2 plasma activated wafers, and there is a general agreement that plasma activation may lead to a highly disordered surface structure, which enhances the hydrophilicity of the surface. Suni *et al.* [42] suggested that the hydrophilicity is caused by an enhanced number of OH-groups at the surface, whose accommodation is made possible by the increased surface porosity and surface area. Takagi *et al.* [43] speculated that the porous structure increased water diffusivity. Amirfeiz *et al.* [41] additionally proposed that the porous oxide layer has cavities lined with OH-groups or hydride groups and filled with water.

PAB bonding is being used commercially in the fabrication of SOI wafers by the Genesis Process™ [44]. One research report has demonstrated that the process is a promising method for bonding of dissimilar materials [44]. The process is also interesting for the bonding of wafers with temperature sensitive structures such as diffused layers and metal patterns that cannot sustain the high annealing temperatures of DWB.

If PAB is used for low-temperature WLP, damage caused by the plasma activation must be minimized. The question of plasma-induced damage is particularly important for silicon dioxide, *e.g.*, for the gate oxide of MOS (metal-oxide-semiconductor) devices. Henriksen *et al.* [45] suggested that plasma activation increases oxide charge.

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Furthermore, they found that plasma activation applied during SOI wafer fabrication was deleterious to BJT (bipolar junction transistor) fabricated on those SOI wafers. Therefore, an accurate assessment of the damage induced in the oxide by plasma activation is important. To mitigate the damage, a forming gas annealing process has been reported to be effective [45].

2.4.3. Anodic Bonding

Anodic bonding or field assisted bonding was originally developed for the bonding of metal to glass [46], with a glass-to-silicon process established later [47]. This bonding uses charge migration for wafer bonding. For example, a silicon wafer and a glass wafer with a high content of alkali metal oxide such as sodium oxide (Na_2O) are used as a bonded wafer pair. The glass wafer is biased as the cathode, and the silicon wafer as the anode. While the two wafers are in contact, heating to 300~400 ^{o}C with electric bias is applied [46].

Wallis *et al.* [47] described the anodic bonding theory extensively, summarizing that the anodic bonding spreads from initial one contact point to the entire wafer. According to their explanation, the contact point of two wafers (glass and silicon wafers) is polarized by the depletion of positive ions on applying voltage. Where the glass wafer is not in contact with the silicon wafer, less polarization occurs and most of the voltage is accumulated by the gap between glass and silicon wafers. In the gap, the resulting electric field becomes the largest at the contact point. Since the bonding force between glass and silicon is proportional to the square of the electric field, the region around the contact point will be well bonded. This region in turn polarizes and its boundary has the maximum electric field. The bonded region spreads outward from the initial contact point to the entire interface in this way. Contact by electrostatic force is not feasible in conductor-conductor combination, since the electric field in the gap disappears as soon as the parts between upper and lower silicon contacts each other. Instead, this bonding method is applied to insulator-insulator combinations [48].

The primary variables that control this process are temperature, pressure and voltage (electrical bias). The introduction of electrical bias makes this bonding incompatible with active devices due to electrical damage. Therefore, this bond is usually used for pressure sensor, solar cell and piezoelectric applications and packaging.

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2.4.4. Metal-to-Metal Bonding

In metal-to-metal bonding, intermediate metal films are deposited prior to the bonding process. When a two-component phase diagram that consists of deposited metal and substrate materials is evaluated, there is a point that shows the composition of a "liquid-phase" in invariant equilibrium with the "solid phase" of each metal and substrate [46]. This point is called the eutectic point, and the point indicates the lowest melting point of the corresponding metal [48]. The alloy between metal and substrate is formed by solid-liquid inter-diffusion at the interface, followed by solidification on cooling. In the case of gold and silicon, this point is 363 ^{o}C and corresponds to a eutectic composition of 2.85 % Si and 97.1 % Au by weight [46].

Eutectic bonding also strongly depends on the cleanliness of the wafer surfaces. Thus, it is important to remove silicon dioxide and organic contaminants during pre-cleaning. Silicon dioxide precludes the diffusion of gold into silicon and organic contaminants hamper good surface contact [48].

For the removal of silicon dioxide, wafers are dipped into HF, and for the removal of organic contaminants, exposure to UV light or a piranha clean is used [46,50]. Similar to anodic bonding, pressure is applied while the wafers are maintained at the appropriate temperature. The low bonding (eutectic) temperature makes this technique attractive [49-50]. For example, Tadepalli and Thompson [50] reported quantitative characterization and process optimization for copper-to-copper bonding that is used for wafer stacking and layer-to-layer interconnects in 3D IC integration. In their research, bonding temperature and pre-clean method are the key parameters used to affect bond quality. A bond strength of 17 J/m^2 was obtained at a low bonding temperature of 300 ^{o}C. For the pre-cleaning of copper, glacial acetic acid was suggested to remove the surface oxide and organic contaminants on copper [50].

2.4.5. Dielectric Glue Bonding

Glue bonding is an intermediate bonding technology that is popular for 3D ICs and bond/etch-back SOI technology due to the following reasons:

1. There are many polymeric glue candidates for bonding [51,60]. Examples include hybrid materials such as MSSQ, HOSP and BCB. Organic materials include Flare, SiLK^{TM} and polyimide. Hybrid materials used as bonding glue are again categorized

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into two groups: 1) materials with an inorganic backbone (MSSQ and HOSP) and 2) materials that contain inorganic constituents (BCB). The inorganic components (mostly silicon) of the hybrid materials adhere well with those of silicon oxide and silicon nitride layers that are commonly found in adjacent layers. Since organic polymer materials usually consist of long and rigid aromatic groups, their glass transition temperatures are high (T_g> 350 °C) and they can offer high thermal stability.

2. Bonding temperature is generally lower than other bonding methods; in particular, they are often compatible with BEOL processes. The bonding temperature ranges from 250 °C (BCB) to less than 400 °C (Flare and Parylene-N) [52-53].
3. Electrical biases are not introduced during the bonding process. Since electrical biases may induce electrical degradation of the circuit device, the use of electric biases is not desirable [26].
4. Glue bonding can induce high bond strength at the interface compared to other bonding technologies. In case of direct wafer bonding, the bond strength at room temperature without annealing is ~0.2 J/m^2 (see Figure 2.13) [38], and less than ~3 J/m^2 even after annealing up to 900 °C [39]. The bond strength of oxygen plasma based PAB is above 1.2 J/m^2 [54]. In copper-to-copper bonding, the bond strength of a bond formed at 300 °C is 17 J/m^2 [50]. Compared to these, the bond strength of bonding using BCB is more than 30 J/m^2 for bonds formed at 250 °C [26].
5. Cross-linking and inter-diffusion properties of polymeric glues and many reactive functional groups of polymeric glues make possible well-sealed and well-adhered bonding interface without a seam. It also accommodates wafer-level non-planarity [3,52-53]. Compared to glue bonding, surfaces for metal-to-metal bonding and fusion bonding require improved planarity.
6. Compatibility of many polymers with standard cleanroom processes [51]. In particular, spin-on polymer materials are easy to apply compared to other bonding methods. The tolerance of glue bonding to particles is higher than that of other bonding methods.

Dielectric bonding consists of three main steps [52]; (1) preparation of the glue layers, (2) wafer contact, and (3) wafer bonding. For spin on polymer materials, the glue

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layers are prepared by spin dispensing of the polymer resin and carrier solvent. This is followed by a pre-bake to remove the carrier solvent, volatile impurities and water vapor due to the condensation reaction, and to improve the degree of surface planarization, and/or to harden the glue surface. On the other hand, vapor deposited polymers are deposited in a vacuum without carrier solvent; therefore, a relatively clean and uniform film can be obtained [52]. The polymer thin films used in wafer bonding should have a uniform thickness over the wafer surface and properties compatible with subsequent processes such as thinning and via interconnection as well as conventional BEOL processes. The desired properties of polymeric glues include the following [51,53,55]:

1. Good adhesion between the glue and its adjacent layer (substrate) as well as good cohesion within the glue to prevent interfacial delamination and decohesion failure
2. No outgassing and by-product generation during bonding process to avoid void formation
3. Modest processing temperature and modest bonding pressure, compatible with BEOL processes to minimize degradation of the chip performance and to maintain mechanical stability
4. No electric biases to minimize degradation of the chip performance and to maintain mechanical stability
5. Thermal and mechanical stability including high glass transition temperature overall range of BEOL to maintain the rigid structure after bonding and to survive subsequent processes
6. CTE (Coefficient of Thermal Extension) well-matched to that of other layers to prevent interfacial delamination and to minimize shift of alignment mark for patterning process caused by stress induced wafer bowing
7. Low moisture uptake and high solvent resistance to reduce the stress corrosion, which weakens the bonding between substrate and glue.

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Table 2.1, Physical properties of polymeric glue candidates [55-63]

Property	Unit	MSSQ	Parylene-N	Flare	BCB
Glass Transition Temperature	°C	>400	13	>400	> 350
Melting temperature	°C	-	420	-	-
Coefficient of Thermal Expansion	ppm/°C	-	6.9	61	52
Thermal Conductivity	W/(mK)	-	0.012	-	2.1
Tensile Modulus	GPa	-	2.4	4.9	2.9
Tensile Stress	MPa	50	45	60	87
Elongation to break	%	12	30		8
Poisson's ratio		-		0.3	0.34
Dielectric Constant	KHz	2.7	2.65	2.85	2.65
Water Absorption	%	-	<0.1	-	-
EBR Solvent		IPA	-	Anisole	Mesitylene

2.5. Low-k Polymeric Glue Alternatives

There are various low-k dielectric polymers that are used as glue candidates currently. In this research four polymers were selected as glue candidates: (1) Methyl silsesquioxane (MSSQ) as a representative silsesquioxanes; (2) Parylene-N as a representative semicrystalline polymer; (3) Flare as a representative organic polymer; and (4) BCB as a hybrid polymer. All materials have been investigated as potential low-k ILDs and are compatible in varying degrees with on-chip interconnection and first-level packaging requirements. The physical properties of these materials are listed in Table 2.1.

2.5.1. MSSQ (Methyl silsesquioxane)

MSSQ (Methyl silsesquioxane) polymer, $CH_3SiO_{1.5}$, is a spin-on-polymer formed from condensation polymerization of silicon diols and triols obtained by the hydrolysis of organo-silicon chloride. This silicone polymer contains an inorganic backbone of alternating silicon and oxygen atoms as shown in Figure 2.14 [55-56]. Cross-linking of the polymer chains reduces the flexibility of the chains, and the resulting polymers are viscous liquids.

This polymer also contains the minimum amount of carbon and hydrogen, and no carbon-carbon bonds preventing charring at high temperature. The high decomposition

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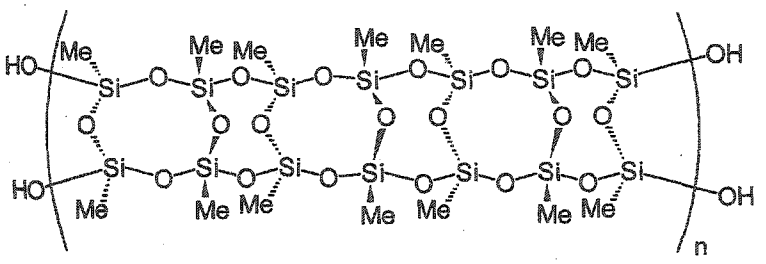


Figure 2.14: Chemical structure of polymer backbone of MSSQ. Adapted from [56].

temperature of silicon–carbon bonds (of siloxane and methyl groups) maintains this polymer resin thermally stable till about 500 °C and the silicon-carbon structures make the surface energy of bulk MSSQ high due to their high bond strength.

A typical three-dimensional structural formula of MSSQ is shown in Figure 2.15. This organosilicon group is a subset of polysiloxane and distinguishes itself as a mono-substituted silicon-oxygen polymer. In MSSQ, there are eight silicon atoms within the "cage" structure. Each silicon atom is attached to a methyl group. There is one and half (sesqui) oxygen atoms bonded to each silicon atom, resulting in an empirical formula of $CH_3SiO_{1.5}$ for MSSQ [56].

2.5.2. Parylene-N

Parylene-N is a vapor deposited polymer (VDP) deposited with the monomer, *p*-xylylene (PX). The monomer exists in the gaseous state at low pressure, and on condensation spontaneously polymerizes to produce linear poly (*p*-xylylene) (PPX), a high molecular weight coating. The Gorham process [57] is generally used to polymerize

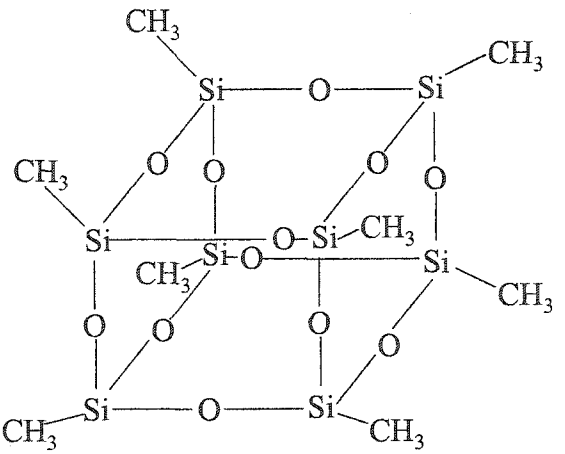


Figure 2.15: 3D (cage) structure of MSSQ.

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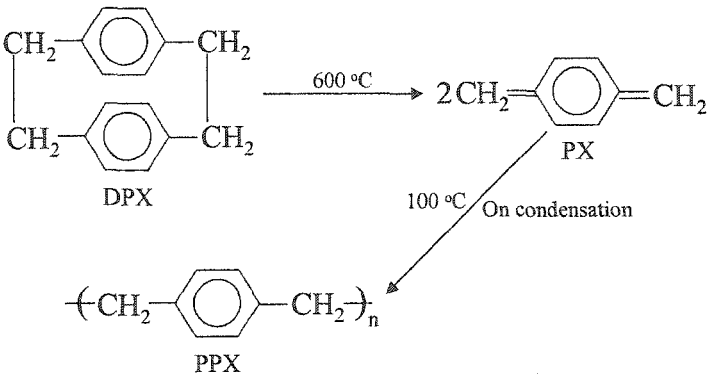


Figure 2.16: Process flow of polymerization of the parylene-N group [57].

such monomers. According to this process, the reactive PX is generated by the thermal cleavage of its stable dimer, di-*p*-xylylene (DPX), a [2,2] paracyclophane. Substituents on the PX nucleus are carried unchanged through to the polymeric repeat unit. The process flow for the polymerization is shown in Figure 2.16.

The p-xylylene polymers (PPXs) are referred to as parylene. Parylene can be categorized into parylene-N, parylene-C, parylene-D, parylene-E, parylene-F. Parylene-N, which has been used as a glue material, is a crystalline polymer, and retains its useful physical integrity to the crystalline melting point, 420 °C [58]. However, since the glass transition temperature is below room temperature (T_g~13 °C), resins of the Parylene-N do not move until reaching the melting temperature (T_m~420 °C). Due to the stiffness of resins after T_g, chemical reactions do not occur actively in between room temperature and 420 °C. This feature distinguishes Parylene-N from other polymer glue candidates. Namely, in the case of other glue alternatives such as BCB, Flare and MSSQ, crosslinking reactions start at the glass transition temperature. However, the reaction of Parylene-N starts at the melting temperature. As temperature increases, the crystallinity of the parylene-N increases and the increased crystallinity results in a decrease in elongation and an increase of modulus. Such a rigid structure remains up to the melting point. This material also exhibits anisotropy due to alignment of the chains parallel to the substrate during deposition. Crystalline phase changes (accompanied by shifts in film stress) may affect parylene reliability at BEOL process temperatures.

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2.5.3. Flare (Poly Arylene Ether)

Flare belongs to the poly arylene ether group and consists of many aromatic groups separated by oxygen atoms. The polymeric glue is synthesized by the reaction of activated difunctionalized aromatic precursor with bis-phenol. Since Flare consists of aryl rings leading to a stiff backbone, its thermal and mechanical stabilities are very high (>550 °C) [59]. Other attractive properties of Flare include: (1) isotropic, electrical and mechanical properties, (2) low moisture uptake caused by the use of ether linkages, as opposed to the carbonyl linkages utilized in other polymers [59], (3) high glass transition temperature caused by the lack of hydrocarbon groups [60], (4) high bond strength and crack resistance, and (5) both thin and thick films can be deposited. Since Flare resin does not have an inorganic component such as silicon, via poisoning residue caused by silanol (Si-OH) after etch or thermal processing, is not a major concern [60]. It is believed that Flare has a bis phenyl ethynyl group as the main group on the polymer backbone [59]. At high processing temperatures (over 350 °C), the ethynyl group forms free radicals, and the free radicals react with other ethynyl group, and the polyene and phenylethynyl are cross-linked [60-61]. The cure reaction of Flare is shown in Figure 2.17.

2.5.4. BCB (Benzocyclobutene)

BCB (Benzocyclobutene) consists of molecules that contain a benzocyclobutene functionality as the main crosslinkable site. Polymers of this type are polymerized by the interaction of thermally activated benzocyclobutene. The thermally activated polymerization is performed by an initial Diels-Alder reaction of two o-quinodimethanes, one of the two becomes a diene and the other becomes a dienophile.

The formed dimer then fragments to give a benzylic diradical species. This diradical may undergo intermolecular coupling, and the crosslinking structure is completed. The crosslinking schematic and chemical structure of BCB monomer are presented in Figure 2.18 [60,62]. BCB can be reflowed due to extensive crosslinking features of oligomer into a three-dimensional structure, and is rigid because of the many rings incorporated into the structure. The excellent reflow property of BCB increases the contact area with substrates, and results in a high fraction of covered area [51]. Although the exact glass

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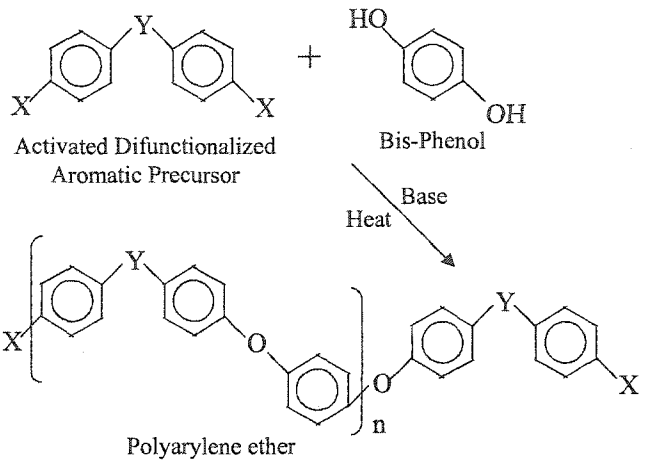
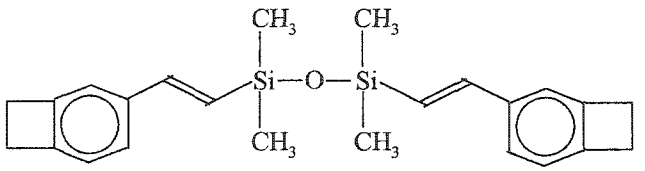


Figure 2.17: Anticipated cure reaction of Flare [60].

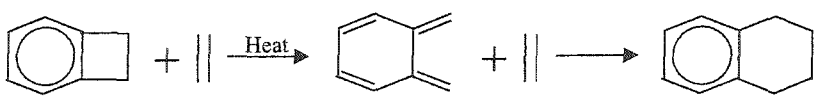
transition temperature is not well established, the limited thermal stability of Si-C bonds at the six-member ring causes decomposition of the polymer over 350 °C [63].

2.6. Theory of Bond Strength

As interest and demand about applications using 3D integration increase, the necessity of mechanical evaluation of bonding integrity also increases. Through characterization of bond strength of the relevant interfaces and evaluation of bonding integrity, potential problems such as interfacial adhesion failure and delamination between polymeric glue and adjacent layers may be explained. Such an evaluation provides quantitative data that can establish a threshold value for maintaining bonding integrity. To evaluate the causes of these potential problems properly and to minimize the occurrence of problems, interfacial bond strength must be evaluated quantitatively.



BCB monomer



BCB Diels-Alder (cycloaddition) reaction

Figure 2.18: Crosslinking schematics of BCB resin and chemical structure of BCB monomer [60].

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Traditionally, mechanical methods for measuring bond strength of stacked layers including polymer thin films (ductile materials) such as the scratch, peel, and stud pull tests suffer from critical limitations due to plastic deformation of the films and unpredicted relaxation of residual film stresses. These both lead to a lack of reproducibility [64]. Since plastic energy dissipation in polymer films is large, the measured results depend more often on the plastic properties of the film than on the interfacial properties. Classical thermodynamic approaches that relate bond strength to interface surface energies using the contact angle method may produce bond strength values that are an order of magnitude less than the actual energy required to separate the interface. That is, this method just considers the surface coverage at the interface, not plastic dissipation energy of the bulk polymer layer [65].

The four point bending method using both peel and shear stress modes is used to measure adhesion energy. Since a 3D IC structure mostly consists of polymeric glue in between top and bottom elastic substrates (*e.g.,* silicon, silicon oxide, silicon nitride and glass), deformation by plastic flow can be significantly reduced during the tests. Four point bending is used to measure the bond strength of different bonding structures quantitatively and it is used as a method for obtaining optimal interfacial chemistry and bonding process condition for 3D integration applications. Four point bending is based on fracture mechanics, where delamination is modeled as a crack propagating along the interface between two materials [65]. This method was first proposed by Charalambides *et al.* [66-67] and then Suo *et al.* [68-69], Cao *et al.* [70], Hu *et al.* [71], Hutchinson *et al.* [72], Ma [73] and Dauskardt *et al.* [74] reported advanced theories and applications.

The effect of several important parameters including interfacial chemistry, plasticity and residual stress on bond strength has also been studied by many research groups. Snodgrass *et al.* [75] and Hohlfelder *et al.* [64] reported the effect of the interfacial chemistry of the polymer material on bond strength. Kook *et al.* [76], Lane *et al.* [77] and Im *et al.* [78] have proposed a plastic effect of metal and polymer materials on bond strength. Jiao *et al.* [79] reported residual stress effect of polymer material on bond strength. In this thesis, the methodology proposed by Charalambides *et al.* [66-67] is used to obtain critical adhesion energy.

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Figure 2.19 schematically shows the sample configuration in four point bending. During the experiment, the load required to achieve a given displacement in the sample ends is measured. For most specimens, load vs. displacement curve has two distinct regions: a linear elastic region and a load plateau region (constant load region). The linear elastic region represents the behavior of vertical pre-crack from top surface to the interface. In this region, as the load is applied, the beam specimen is bent and the pre-crack tip dos not move notably and thus elastic energy is stored. Up to the end of linear elastic region, the pre-crack tip stores elastic energy continuously, with the yielding point reached at the end of the linear elastic region. At the yielding point, the stored elastic energy is released, and the released elastic energy acts as a driving force for crack propagation. The crack tip moves into the interface and along the interface. In the load plateau region, released strain energy is mainly divided into fracture energy and plastic dissipation energy. The fracture energy is consumed to extend crack length by breaking of atomic bonds at the interface, and the plastic dissipation energy is consumed to deform the ductile material such as polymeric glue.

Critical adhesion energy is obtained under the condition that the strain energy release rate must be at quasi-steady state, at least when the crack length of the interface exceeds the thickness difference between pre-crack tip and interface. As noted, Charalambides *et al.* determined the critical adhesion energy under the steady state condition as the difference in strain energy between the pre-cracked upper beam and un-cracked bottom beam of the specimen. The upper beam has negligible strain energy, so the strain energy of the entire beam can be taken as the energy in the un-cracked section. Figure 2.19 represents the beam structure; these energies are represented in terms of the applied

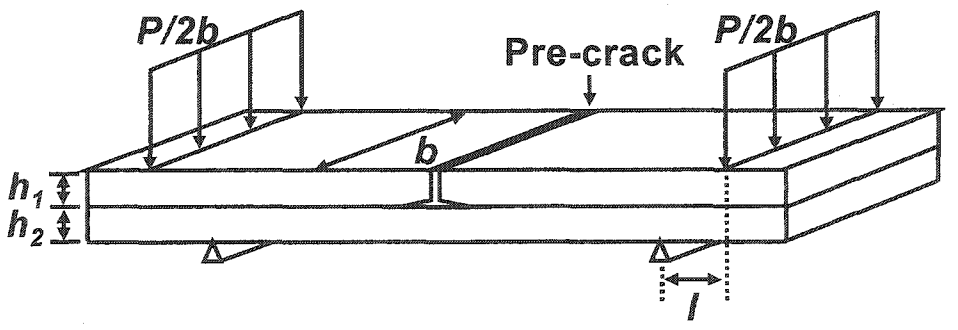


Figure 2.19: Beam specimen geometry for four point bending experiments.

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moment M and inertia I [66-67].

$$G = \frac{(1-\nu_2^2)M^2}{2E_2}\left(\frac{1}{I_2} - \frac{\lambda}{I_c}\right) \tag{2.4}$$

where G is the strain energy per unit area and I_2, I_c are the second inertia of area per unit width of un-cracked beam substrate and composite beam (cracked substrate and glue), λ is the effective modulus described as $\lambda = \frac{E_2(1-\nu_1^2)}{E_1(1-\nu_2^2)}$, and M is the moment per unit width to be described as $M = {}^{pl}/_{2b}$, where p is the total load, l is the spacing between inner and outer loading pins, and b is the specimen width. Since the thickness of glue layer is far thinner than that of upper and lower beams, the effect of glue thickness is neglected. The second inertia terms are represented as

$$I_c = {}^{h_1^3}/_{12} + {}^{\lambda h_2^3}/_{12} + {}^{\lambda h_1 h_2 (h_1+h_2)^2}/_{4(h_1+\lambda h_2)} \tag{2.5}$$

$$I_2 = {}^{h_2^3}/_{12} \tag{2.6}$$

From Equation 2.4 to Equation 2.6, the strain energy of the entire beam is

$$G = \frac{3(1-\nu_2^2)p^2l^2}{2E_2b^2h^3}\left(\frac{1}{\eta_2^3} - \frac{\lambda}{\eta_1^3 + \lambda\eta_2^3 + 3\lambda\frac{\eta_1\eta_2}{\eta_1+\lambda\eta_2}}\right) \tag{2.7}$$

where $\eta_i = {}^{h_i}/_{h}$ $(i = 1,2)$. This governing equation for the strain energy release rate is used to evaluate the critical adhesion energy of beam specimens.

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2.7. Summary

Various approaches for bond/etch-back SOI and 3D IC integration schemes are outlined with a focus on the RPI 3D IC approach; *i.e.*, dielectric glue bonding and inter-wafer interconnection using copper damascene patterning. Issues and advantages associated with the bond/etch-back SOI and 3D ICs are also discussed. Wafer bonding technology, which is a key process for all these applications, is introduced. Fusion bonding, anodic bonding, metal-to-metal bonding and dielectric glue bonding are examined. Among the bonding technologies discussed, dielectric glue bonding and four glue alternatives are mainly presented. Dielectric glue is used as bonding intermediate in this research due to the advantages, which are good adhesion, no outgassing, bonding at moderate temperature and pressure conditions, no electrical bias, and good thermo-mechanical properties.

MSSQ, Parylene-N, Flare and BCB have been considered as glue candidates, and they represent silsesquioxanes, semicrystalline polymers, organic polymers, and hybrid polymers respectively. These materials have been investigated as potential low-k ILDs and properties of these materials are compatible with on-chip interconnection and first-level packaging requirements. Advantages and features of low-k polymeric glue alternatives are highlighted, and the chemical and physical properties of the alternatives are described. Beam bending theory relevant to four point bending characterization of bonded substrates is introduced. The theory is used to evaluate the bond strength at the interface. This evaluation is a key characterization procedure implemented in this research.

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CHAPTER 3
EXPERIMENTAL PROCEDURES

3.1. Overview

This chapter provides brief descriptions of the experimental techniques used in the research reported in this thesis. For each technique, the theoretical background and the specific conditions used are presented. Wafer bonding equipment and procedures are covered first. Sequences of polymeric glue bonding, bonder structure, and parameters affecting glue bonding are also included in this section.

The experimental method used to measure bond strength, four point bending, is established as a part of this thesis. For this method, bonded wafer pairs are diced into beam-shaped specimens, followed by mechanical and chemical treatments. The procedure for beam specimen preparation that was shown to provide reproducible results is also presented. The load plateau and critical adhesion energy values obtained are statistically analyzed using normalized standard deviation and residual analysis using random variable and normal distribution techniques. Reproducibility of results when four point bending is performed by different operators is also addressed.

To measure residual stress of stacked layers, the wafer curvature method is employed. The method is presented, and the measuring instrument (Flexus) is described.

Both Fourier transform infrared spectroscopy (FTIR) and spectroscopic ellipsometry are used to characterize films. FTIR analysis is performed in order to follow chemical changes (*i.e.*, curing reaction) of the polymeric glue materials during bonding. Spectroscopic ellipsometry is used to measure the thickness of polymeric glues.

3.2. Wafer Bonding Equipment and Procedures

In this section, dielectric glue bonding procedures and equipment for wafer bonding are introduced. The baseline processes for spin-on and bake processes for spin-on polymeric glue candidates (BCB, Flare and MSSQ) and vapor deposition polymer (Parylene-N) are also described in detail.

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3.2.1. Deposition and Bake of Polymeric Glues

Prior to depositing polymeric glue candidates (MSSQ, Flare, Parylene-N and BCB) on a substrate, blanket wafers are cleaned by chemical treatment. Piranha cleaning is used first. The wafers are dipped into a sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2) solution of a ratio of 2:1 for 20 min. at room temperature, and are rinsed for 5 min. with DI water and spin-dried in a hot nitrogen (N_2) ambient. The spin dry cleaning process is performed in a FluoroWare (Semitool®, Kalispell, MT) spin drier with the sequence listed in Table 3.1. For patterned wafers, the spin dry cleaning process is conducted without chemical treatment in order to protect the circuit structures. The spin dry cleaning is identical to that used for blanket wafers. After spin dry cleaning, solvent cleaning of both blanket and patterned wafers is conducted in a FlexiFab™ (Machine Technology Inc., Ventura, CA) spin coater to remove particles and to complete the pre-clean process. Acetone, methanol, and isopropanol are generally used as rinsing solvents. All three solvents are sprayed for 20 sec. at 1000 RPM, and the wafers are spin-dried for 40 sec. at 3000 RPM.

Procedures for depositing and baking of the candidate glues are as follows:

Table 3.1: Sequence of spin dry cleaning process

Step	Time (sec.)	Speed (rpm)	Action
1	300	600	Rinse
2	20	1800	N_2 Purge
3	120	1800	Dry 1
4	300	600	Dry 2

BCB deposition: All BCB deposition is conducted on a FlexiFab™ Spin Coater track with sequential deposition and baking procedures outlined in Table 3.2. Before spin-on of the BCB resin, an adhesion promoter strongly recommended by the manufacturer is spun-cast. Dow Chemical AP 3000 is used for this purpose. More information about the structure and function of this adhesion promoter is presented in Chapter 5. After the adhesion promoter is dispensed, Dow Chemical Cyclotene 3022-35 BCB resin is dispensed and baked. A disposable pipette is used to deposit the adhesion promoter and

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BCB resin. So *et al.* [80] used an additional baking process of the adhesion promoter due to the possibility of bubble formation during baking process. However, Snodgrass *et al.* [75] did not observe this phenomenon. The additional adhesion promoter baking process is not used in this research as no bubbles are observed. During the BCB resin spin deposition process, most wafers undergo backside rinse and edge bead removal steps; Mesithylene (Dow Chemical T1100), a rinse solvent for uncured BCB resin, is used.

Backside rinses are performed to remove polymer residues on the wafer backsides. Any remaining polymers are cured during the subsequent bonding process and thus may not etch well during the backside thinning process. After thinning, the backside of a thinned wafer may have height differences due to unetched polymer residues, and the difference may induce breakage of the bonded wafer pair by the compression force applied during the next bonding step. Although the spin process is conducted uniformly, an edge bead is generally formed, requiring an edge bead removal process. The edge bead may induce height difference between edge parts and center parts, and the difference may produce void generation during bonding and edge chipping during backside etching. Hence, these processes are incorporated in the baseline process flow.

After spin coating, the wafer is placed on the hot plate for 2 min. at 170 °C to drive off any volatile solvents of the adhesion promoter and polymer resin, and cooled down

Table 3.2: Coat and bake programs for adhesion promoter and BCB resin

Coat program				
Step	**Time (sec.)**	**Speed (rpm)**	**Ramp (%)**	**Action**
1	5	0	0	AP dispense
2	20	3000	30	
3	5	0	0	BCB dispense
4	5	750	30	
5	30	4000	40	
6	5	1000	10	BR
7	5	1000	10	EBR
8	10	2000	20	
Bake program				
Step	**Time (sec.)**	**Pin Height (in.)**	**Temp. (°C)**	**Action**
1	120	0	170	
2	300	1	170	N_2 Purge

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for 5 min. in a N_2 environment. When BCB is used as a dielectric material, the baking temperature is usually lower than 170 °C [57]. However, such a low baking temperature may result in a low fraction of bonded area after bonding due to void generation by insufficient solvent removal and insufficient BCB flow. During the baking process, the thickness of BCB resin hardly changes. Spectroscopic reflectometry and ellipsometry are used to measure the BCB thickness. After deposition and baking, the BCB has a mean thickness of 1.3 μm, and is very uniformly distributed across 200 mm wafers (less than 2 % standard deviation).

Flare deposition: Flare resin is deposited using a FlexiFab™ Spin Coater track, with deposition and baking procedures outlined in Table 3.3. Unlike BCB, Flare resin does not need a separate adhesion promoter because Flare is believed to have a sufficient density of silanol functional groups to react with dangling bonds of the substrate [81]. A disposable pipette is used to deposit Flare resin (Flare 4k, manufactured by Honeywell). Most wafers undergo backside rinse and edge bead removal steps of Flare resin using anisole, a rinse solvent for uncured Flare resin. After spin coating, the wafer is placed on the hot plate for a multiple step baking process. The determined bake sequence comprises baking at 200, 250 and 300 °C for 2 min. each in a N_2 purge. The sequence was

Table 3.3: Coat and bake programs of Flare resin

Coat program				
Step	**Time (sec.)**	**Speed (rpm)**	**Ramp (%)**	**Action**
1	5	0	0	Flare dispense
2	5	500	5	
3	3	0	0	
4	60	3000	30	
5	5	1500	15	BR
6	5	1500	15	EBR
7	10	3000	30	
Bake program				
Step	**Time (sec.)**	**Pin Height (in.)**	**Temp. (°C)**	**Action**
1	120	0	150	N_2 Purge
2	120	0	200	N_2 Purge
3	120	0	250	N_2 Purge

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developed by the manufacturer to promote solvent removal, avoid oxidation of the resin, and harden the polymer resin [82]. During baking, the thickness of Flare resin hardly changes. After deposition and multi-step baking, the Flare 4k has a mean thickness of 0.32 μm and is very uniformly distributed across 200 mm wafers (less than 1% standard deviation).

MSSQ deposition: MSSQ resin was deposited using a FlexiFab^{TM} Spin Coater track following the deposition and baking programs outlined in Table 3.4. Like Flare resin, MSSQ does not need a separate adhesion promoter. Allied Signal produces the MSSQ resin used with the commercial name of Accuspin T-18 [83]. A disposable pipette is used to deposit the MSSQ resin, and most wafers undergo backside rinse and edge bead removal steps with isopropanol as the rinse solvent. After spin coating, the wafer is baked on a hot plate at 160 °C for 90 sec. with N_2 purge [83]. The sequence was developed by the manufacturer to drive off the solvent and to harden the polymer resin. During the baking process, the thickness of MSSQ resin remains quite constant. After deposition and baking steps, the MSSQ has a mean thickness of ~0.5 μm, and is very uniformly distributed across 200 mm diameter wafers (less than 2 % standard deviation).

Table 3.4: Coat and bake programs of MSSQ resin

Coat program				
Step	**Time (sec.)**	**Speed (rpm)**	**Ramp (%)**	**Action**
1	5	0	0	MSSQ dispense
2	20	3000	30	
3	5	2000	20	BR
4	5	2000	20	EBR
5	10	2000	20	
Bake program				
Step	**Time (sec.)**	**Pin Height (in.)**	**Temp. (°C)**	**Action**
1	60	0	160	N_2 Purge

Parylene-N deposition: Parylene-N is deposited in a Novatran model 1050 Parylene Deposition System (Dow Chemical Inc., Midland, MI) [57,84] using the following sequence. First, the wafers are placed on a rotating sample holder, and a lint-free clean room wipe that has been dipped in adhesion promoter A-174, is placed inside the

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chamber before the chamber is pumped down to 20 mTorr. The deposition pressure is controlled by a feedback loop tied to the vaporizer power. The vaporizer is set to a temperature of 150 °C. At 20 mTorr, the vaporizer valve is opened and, after the pressure reaches < 20 mTorr again, power to the dimer heaters is turned on. At this point, the dimer begins to evaporate and the pyrolysis reaction occurs in chamber for the reaction, where the dimer is split up into monomers. The temperature of the dimer is controlled to keep a constant monomer vapor pressure in the chamber of 55 mTorr. When the pressure set point is reached, the deposition rate is approximately 10 nm/min [57]. Film thickness depends on the amount of dimmer used. With 10 g of dimer, a Parylene-N film thickness of about 1 μm with minimal thickness variation is obtained.

3.2.2. Bonding Equipment and Processing Capabilities

Wafer contact and bonding are conducted using an EVG EV501 wafer bonder (EV Group Inc., Schaerding, Austria) depicted in Figure 3.1. As seen in the Figure 3.1, the bonder chamber consists of a pneumatic cylinder, "uniforce compliant membranes", graphite plate, top and bottom heaters, and bonder chuck. The two wafers being bonded are in the bonder chuck [53]. The pneumatic cylinder moves the piston into the stacked wafers to supply the pre-determined pressure. A uniforce compliant membrane consists of two absorber disks and a quartz plate disk. The purpose of the membranes is to provide

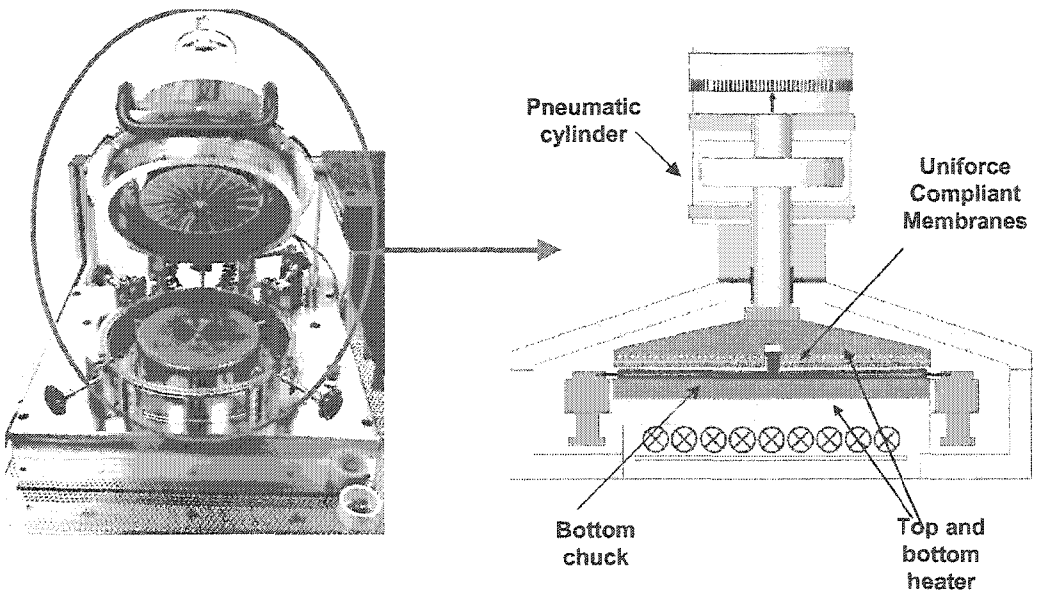


Figure 3.1: EVG EV 501 bonder and structure inside the bonder [52].

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the stacked wafers with even pressure distribution. The graphite plate can be used as an electrode for anodic bonding. However, in this work, the graphite plate is used to absorb the impacts of the sudden pressure changes resulting from "on-and-off" pressure cycles. If such a buffer plate is not used, brittle materials such as the quartz plate and the wafers being bonded may break.

In the 3D integration process developed at RPI, processed wafers are first aligned in a EVG EV640 Smart-View Aligner (EV Group Inc., Schaerding, Austria) prior to loading into the bonder chamber [6,53]. Two wafers are placed in the bonder chuck with their glue layers touching and clamped with two clamps. The bonder-chuck is then loaded into the EV501 bonding chamber, after which the multi-step bonding process is performed. The bonding step sequence involves a pump down, heating, compression, and cooling [52]. Since three spin-on polymeric glue candidates (BCB, Flare and MSSQ) have different chemical structures from Parylene-N, heat treatments of these materials are conducted differently. The procedures are described below.

Bonding of spin-on polymers: When bonding is done using one of the three spin-on glue candidates (BCB, Flare and MSSQ), the bonder is pumped down to 10^{-4} mbar and heated to a pre-determined final heating temperature. Determination of the final heating temperature is associated with the polymer cure temperature, because the cure reaction of the polymers is the key to causing the bonding between glue and its adjacent layer, at the glue-glue interface [52]. For Flare and MSSQ polymers, the final heating temperature is 400 °C, and that of BCB resin is 250 °C. These are compatible with both conventional BEOL processing and 3D integration processing as performed at RPI [32,52].

When the pre-determined temperature is reached, the bond is initiated by pressing in the middle of the top wafer to create an initial point of contact, followed by uniform down pressure over the entire wafer [52-53]. Heating time is determined by the desired extent of curing of the materials. If the heating time is long, stresses in the glue material sandwiched by wafers and compressed by the piston would increase, and this may trigger segregation of small polymer molecules. On the other hand, if the heating time is too short, the glues will not be sufficiently cured, resulting in low bond strength and void generation caused by non-cured small polymer molecules. Furthermore, the glue may

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flow with time due to its viscoelasticity. It is therefore important to select the optimal final heating time and temperature to maximize the bonding result.

After the heating stage of the glue bonding process is completed, pressure is unloaded and the wafers are slowly cooled. A suitable cool-down rate is also important. A fast cool-down rate may result in stress generation by CTE differences between glue and its adjacent layer, and hence weaker bond strength. However, a slow cool-down rate will increase total processing time.

Bonding of vapor deposition polymer: During vapor deposition, parylene-N undergoes a cure reaction. Hence, for bonding of this polymer material, the melting point is used. Parylene-N polymer melts around 400~420 ^{o}C and is known to reflow [57]. After the bond chamber is pumped down (~10^{-4} mbar), the wafers are heated to the melting temperature of the polymer (400 ^{o}C). This is compatible with both conventional BEOL processing and 3D integration processing as developed at RPI [53]. The bond is initiated by pressing in the middle of the top wafer to create an initial point of contact, then uniform down pressure is applied over the entire wafer. After the heating stage, pressure is unloaded and the wafers are slowly cooled.

For all polymers, pressure is applied to remove any gaps between the glue layers on the top and bottom wafers, and to facilitate curing [52-53]. The cure reactions of glues are the defining step in wafer bonding as the adhesion energy between the two wafers is determined by these reactions. The reaction can result in three distinct phenomena; interdiffusion between the two glue surfaces, crosslinking within the glue, and chemical bonding between glue and dangling bonds of the substrate. The interdiffusion reaction occurs in the vicinity of the cure temperature (T_c) and higher. Once this temperature is reached, an interfacial-healing process takes place with the glue-to-glue interface gradually disappearing [85]. One required condition for the interdiffusion reaction is that glue material should be made up of amorphous polymer chains [85-86]. Thus, it is difficult for interdiffusion to occur in Parylene-N because the polymer consists of crystalline polymer chains rather than an amorphous structure.

The cross-linking reaction is often used to explain adhesion within polymeric glues. Prior to pressure loading, spin-cast polymeric glues undergo bake and partial cure step. With proper pressure loading and long enough curing, a gelation reaction occurs through

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the opening of crosslinkable groups such as benzocyclobutene of BCB, and the silanol group of MSSQ, thereby connecting monomers and oligomers of the glue with each other. The connected polymer chains (cross-linked polymer chains) keep the structure rigid until the chains are dissociated at high temperature (over the glass transition temperature) [87-88]. This reaction may make glue flow around the substrate with topological differences. This reflow is called interlocking action, and, especially, BCB shows such a "liquid-like" behavior. A schematic of the general cure reaction, including interdiffusion and crosslinking, is illustrated in Figure 3.2 [89].

Chemical bonding is mainly used to explain the adhesion mechanism between polymeric glue and dangling bonds of substrate [75,85]. The formation of chemical bonds often occurs through thermal treatment. In particular, condensation reaction that replaces weak silanol bonds (Si-OH) with strong siloxane-covalent bonds (Si-O-Si) is often employed to make chemical bonds in the relevant interface [75]. For example, when MSSQ and BCB resins (and its adhesion promoter) are in contact with a silicon oxide layer, silanol groups in the resins react with dangling bonds of the oxide layer to form strong siloxane groups [60,75].

3.3. Bond Characterization Techniques

In this section, the methods used to quantify the bond strength at the glue interface and the residual stresses of glue and bonded wafer pairs are introduced. First, four point

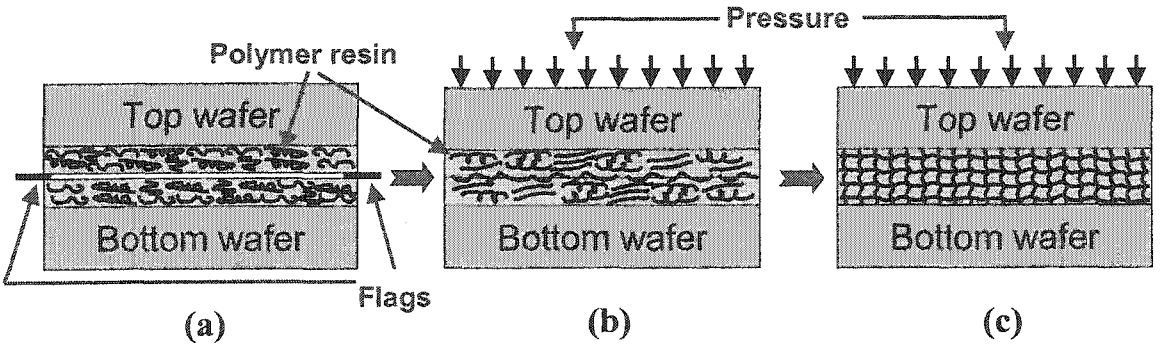


Figure 3.2: Schematic of theoretical cure reaction in wafer to wafer bonding process: (a) Before heating and pressurization, (b) Start of polymeric glue cure reaction, pressurization is needed to promote out-of-plane (glue to glue) inter-diffusion, (c) End of polymeric glue cure reaction, inter-diffusion and cross-linking is completed.

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bending is explained and procedures for beam specimen preparation are described. The wafer curvature method to measure the built-in residual stress and wafer deflection is also described.

3.3.1. Measuring Bond Strength

The four point bending technique is described in this section. The specification of the bending machine used and preparation procedure of beam specimen such as dicing, mechanical polishing, pre-crack making and chemical treatment are also explained. Normalized standard deviation and residual analysis for statistical analyses of the measurements are explained. Results of four point bending tests performed by two different experimenters are presented for inspection of reproducibility.

3.3.1.1. Four Point Bending Technique

Figure 3.3 shows the special fixture used for four point bending (Zwick T1-FR005TN Material Testing Machine, Zwick USA LP, Atlanta, GA). A load cell measures the applied load, and an actuator measures displacement. The reading of the displacement from actuator is verified using a linear variable differential transformer (LVDT) transducer [73]. The load cell has a maximum capacity of 500 N and a resolution of 0.5 N. The minimum displacement rate that is measured is 1 μm/min, and 0.05 μm is the spatial resolution of displacement.

Figure 3.4 shows a schematic of the specimen before and after bending. Initially, the bonded wafer is diced into beam-shaped specimens with nominal dimensions of 40 mm long, 5 mm wide, and 1.5 mm thick. The beam specimen is polished and a pre-crack is

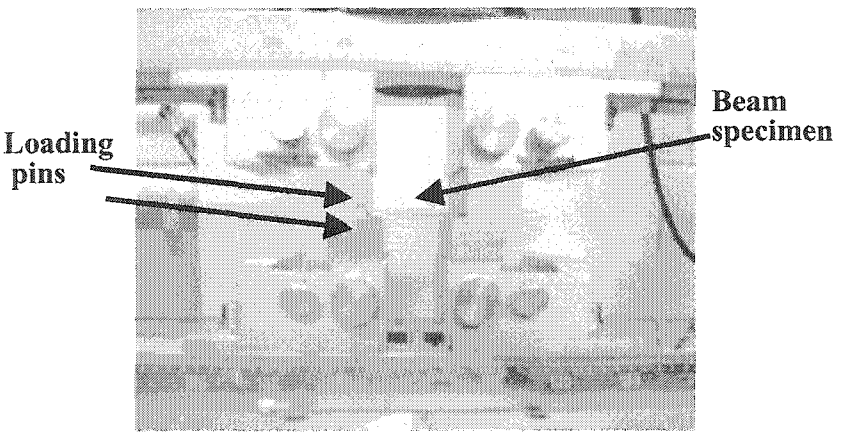


Figure 3.3: Fixture for four point bending experiments.

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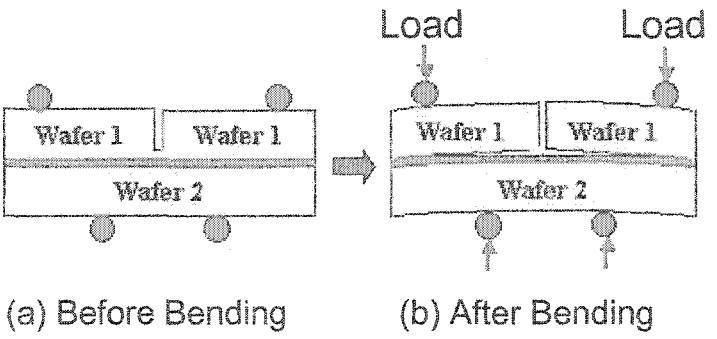


Figure 3.4: Schematic of four point bending specimen before and after bending.

made in its center. Chemical treatment for smoothing "side cracks" and the pre-crack is performed. Details on each of the above mentioned steps are described in Section 3.3.1.2. The beam-shaped specimen is then mounted on the bending machine. The distance between the inner loading pins of the bending machine is 2.4 cm, and that between outer loading pins is 3.4 cm (see Figure 3.4).

As an increasing load is applied, the bending moment in the pre-crack spot increases and the pre-crack propagates vertically into the interface. If the interface between pre-cracked substrate and glue is weaker than un-cracked substrate, the crack deflects into the interface and propagates along it. A typical load vs. displacement curve, reflecting the crack movement in the specimen, is plotted in Figure 3.5. This load vs. displacement curve has four distinct regions. The linear elastic region comes from pure bending of pre-cracked and un-cracked substrates (range 1 of Figure 3.5). The crack kink region occurs due to movement of the initial pre-crack spot into the weak interface (range 2 of Figure 3.5). The plateau load – steady-state crack propagation (range 3 of Figure 3.5) region indicates crack propagation along the bonding interface. The second linear elastic region comes from the bending of un-cracked substrate after plateau load region (range 4 of Figure 3.5). If the pre-crack is in the weak interface, the crack propagates along the weak interface without crack-kink [50,73].

3.3.1.2. Procedure of Beam Specimen Preparation

Beam-shaped specimens prepared for four point bending experiments need to be very carefully prepared in order to acquire consistent and reproducible results. The specimen preparation procedure consists of the following steps: (1) dicing of a bonded wafer pair,

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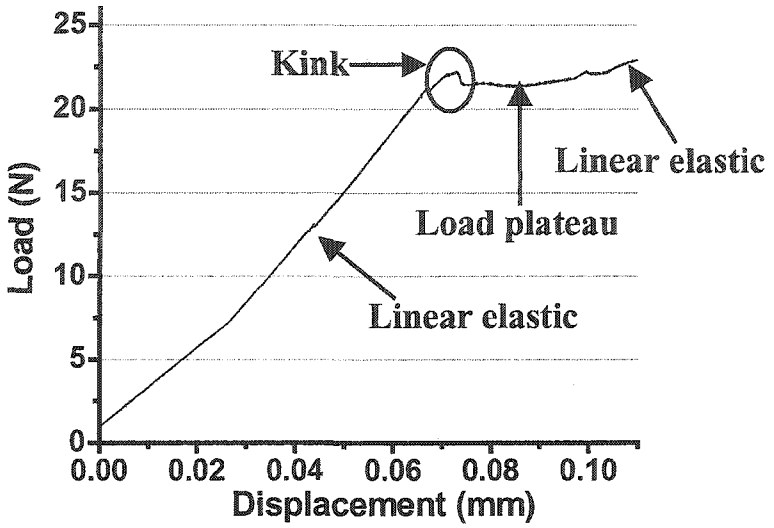


Figure 3.5: Typical four-point bending result; a load-displacement curve for measuring saturation load value.

(2) mechanical polishing, (3) pre-crack making, and (4) chemical treatment to smooth cracks. An explanation of each step follows:

Dicing of bonded wafer: After the wafer bonding process, the bonded wafer pairs are diced to produce the beam specimens. The speed of the dicing saw is 1,000 RPM. After dicing, the nominal dimension of the beam specimens is 40 mm long, 5 mm wide, and 1.5 mm thick.

Mechanical polishing: After the dicing process, the outer sides of the beam specimens are rough and have cracks ranging in size from ten to a hundred microns. It is important to reduce the sizes of these "side cracks", as they may degrade the accuracy of the four point bending test. In particular, when the critical adhesion energy value of the beam specimen is high, it is possible for side cracks of large sizes to trigger crack initiation. The purpose of this polishing step is to reduce the size of side cracks created during the dicing process. SiC and diamond abrasive polishing pads are used for the mechanical polishing. The polishing pads are put on a mechanical polisher, and the polisher is rotated at 250~300 RPM. Water is supplied to alleviate friction between specimen and pad. After polishing using several grits of SiC abrasive polishing pad, followed by polishing with a diamond polishing pad, the size of cracks in the side of the beam specimens are below a micron. This mechanical polishing also diminishes the

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nominal dimensions of the beam specimens to 40 mm long, 4 mm wide, and 1.5 mm thick.

Pre-crack formation: After mechanical polishing, one of two substrates of the bonded wafer pair is pre-cracked at the center of 4 cm length with another dicing saw. Unlike the dicing stage, the process for pre-crack formation is conducted with a slower saw speed for dicing (~500 RPM). This saw speed can reduce breakage rate. When the pre-crack reaches very close to, or a little bit into the bond interface, the dicing process is stopped. Since the interfaces between the glue and cracked substrate are of different colors from the bulk substrate, observation under a microscope is generally used to determine the etch stop.

Chemical treatment: After the pre-crack is formed at the center of each beam specimen, the beam specimens are dipped into wet etchant in order to: (1) smooth damaged and roughened surfaces that are produced during pre-crack formation, and (2) etch the pre-crack more until pre-crack tip reaches the glue interface. In most beam specimens, the pre-crack tip does not reach the weak substrate-glue interface to be studied (called under-diced). In some cases, the crack extends into the glue layer (called over-diced). Both under–dicing and over-dicing may induce breakage of the beam specimen subsequent to four point bending test because stress is concentrated at the inappropriately placed crack tip. The crack propagation along the interface is mainly caused by the shearing action, when the pre-crack tip is placed at the interface, the fraction of shear stress contributing to crack growth is maximized, and thus crack propagation along the interface is promoted without specimen breakage.

When a pre-crack is formed in a silicon wafer, 30 % tetramethylammonium hydroxide (TMAH) solution is used for the dipping etchant (1 hr at 85 °C). When a pre-crack is formed in a glass wafer, BOE (buffered oxide etch) solution (hydrofluoric acid (HF): ammonium fluoride (NH_4F) solution of a ratio of 1:10) is used (several hours at room temperature).

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3.3.1.3. Mean Critical Adhesion Energy and Standard Deviation for Two Types of Results

The measurements from the four-point bending test are analyzed by statistical methods to assess data quality and obtain the saturation load and critical adhesion energy. The two procedures that use statistical analysis are outlined below:

1. Obtaining saturation load values during each bending test.
2. Calculating the mean and standard deviation values of the critical adhesion energy from the saturation loads from several beam specimens taken from a bonded wafer pair, obtained from process 1. Minimum 4 specimens and maximum 8 specimens are used to calculate the mean and standard deviation values of critical adhesion energy.

Normalized standard deviation is used for statistical analysis of process 1 [90-91] and residual analysis is used for statistical analysis of process 2 [90].

Precise determination of the saturation load value in each four point bending test is important because it determines critical adhesion energy. The normalized standard deviation is used to characterize the scatter and deviation from the mean value of saturation load during each beam bending experiment. The normalized standard deviation defined as

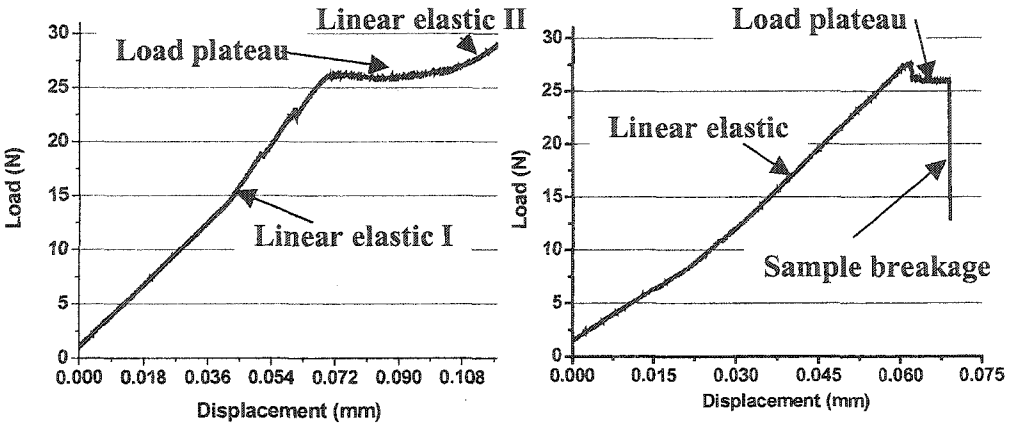
$$\lambda = \frac{\text{standard deviation}}{\text{mean}} = \frac{\sigma}{\mu} \tag{3.5}$$

This normalized value is used as a criterion to determine the acceptance of a saturation load value. Here, mean and standard deviation values are obtained from load plateau of each beam bending experiment. A load vs. displacement curve is usually one of two types (see Figure 3.6):

Type 1 – A linear elastic region I, load plateau region, and linear elastic region II (classical load-plateau shape, type 1)

Type 2 - A linear elastic region, load plateau region, and sample breakage (load-plateau shape deviated from the classical trend, type 2).

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(a) type 1 (b) type 2

Figure 3.6: Two types of load vs. displacement curves: (a) type 1 consists of linear elastic I, load plateau, and linear elastic II regions, and (b) type 2 consists of linear elastic, load plateau, and sample breakage regions.

Although Type 1 load curves are observed in load vs. displacement curves of most bonded wafer pairs, Type 2 is observed occasionally. Load vs. displacement curves shown in Figure 3.6 are obtained from beam specimens of bonded wafers with BCB of 2.6 μm. Both silicon wafers in this bonded wafer pair were thermally oxidized (2 μm thick) prior to bonding (see Section 3.2.2).

The two different load vs. displacement curve types are mainly caused by; (1) different parameters such as surface morphology, specimen geometry, glue thickness, and glue stack material, and (2) local variations of the bonding state. Spatial variations are presumably caused by variations in process conditions (*i.e.*, local curing temperature and applied pressure) and/or uncertainties during the specimen preparation process and four point bending experiment (*i.e.*, humidity, environmental temperature, and vibration) [74].

As an example, in a Type 2 load vs. displacement curve, where the bond strength of relevant interface is high (more than 35 J/m^2), a crack propagates along the interface initially and then stops. In this situation, the crack propagation energy is mostly consumed to break the specimen.

The load plateau region and saturation load value for Type 1 results are determined by measuring normalized standard deviation λ of load plateau looking region. A λ value of 0.02 is selected as a criterion to determine the acceptance of load plateau. That is, when the λ value of the relevant region (load plateau looking area) is lower than 0.02,

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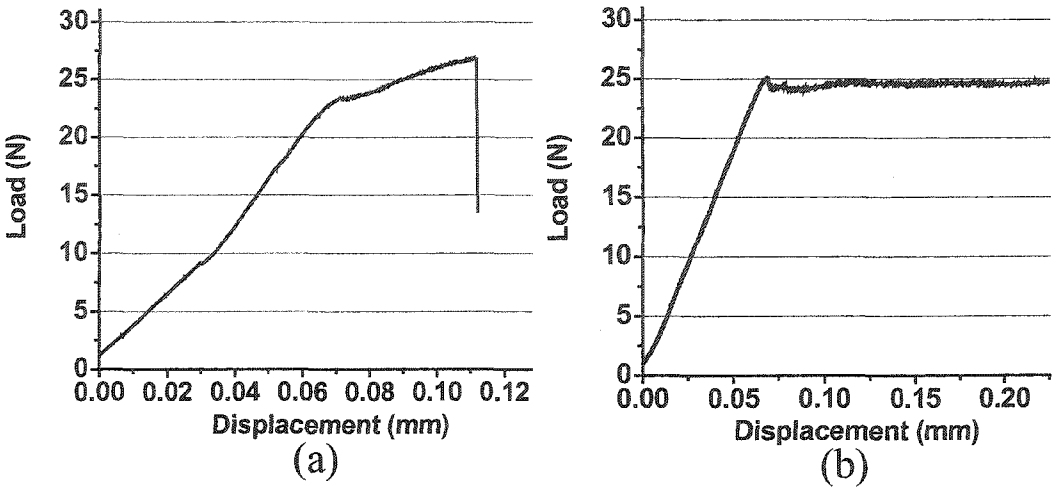


Figure 3.7: Examination of load plateau region and saturation load using normalized standard deviation λ: (a) Refused test: calculated λ value of 0.042 is higher than standard λ value of 0.02. (b) Accepted test: calculated λ value of 0.002 is lower than standard λ value of 0.02.

mean load value of the region is accepted as saturation load, otherwise the region is not a clear load plateau and the test is refused.

In Type 2 results, the load plateau region and saturation load value are determined by measuring λ of load plateau looking region until just before breakage. A λ value of 0.02 is again chosen as a criterion to determine the acceptance of load plateau in the Type 1 case. Figure 3.7 shows examples of accepted load plateau and refused load plateau tests. In this example, the 0.6 μm of BCB is sandwiched between two silicon wafers coated with 1μm PECVD oxide layers (see Section 3.2.2).

After the saturation load value of each beam specimen is determined, the critical adhesion energy, G_c, is calculated using Equation 2.7. Thus saturation load value and geometric parameters are found out from the four point bending test.

To evaluate the critical adhesion energy for each bonded wafer sample, several beam specimens are made and the critical adhesion energies are determined as described above. If the errors are normally distributed, then approximately 95% of the standardized residuals should fall in the interval between -2σ and $+2\sigma$ [90]. Residuals that are far outside this interval are treated as outliers and discarded. This 4σ range standard is used as a criterion to determine whether the relevant value is accepted or refused.

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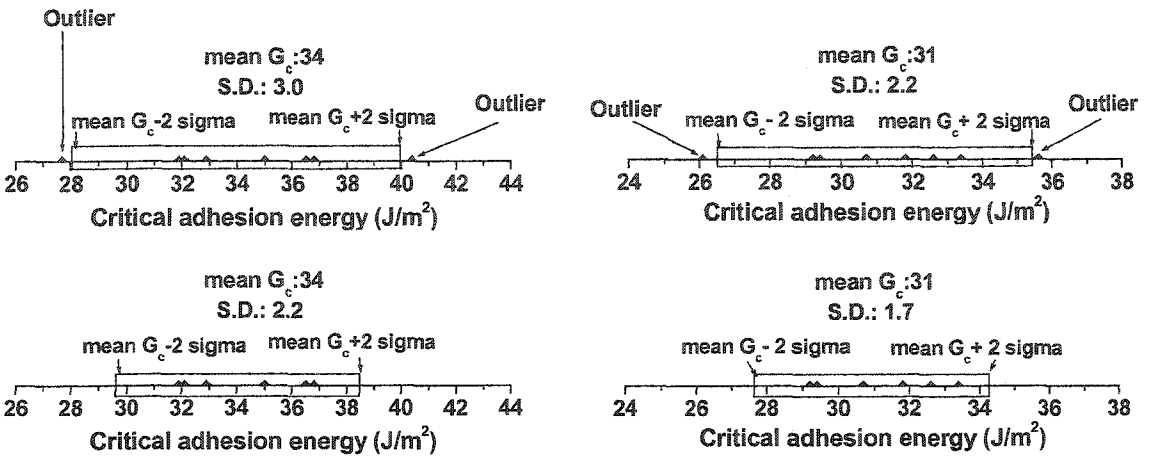


Figure 3.8: Determination of mean critical adhesion energy, G_c and standard deviation (S.D.) values using "residual analysis" method: (a) Si/ thermal SiO_2 (2 μm)/ BCB (2.6 μm)/ thermal SiO_2 (2 μm)/ Si structure. After analyzing using "Residual analysis", 2 specimens, which are deviated from +/- 2 σ, are discarded (outliers). Mean Gc is 34 J/m^2 with S.D. of 2.2 J/m^2. (b) Si/ PECVD SiO_2 (1 μm)/ BCB (2.6 μm)/ PECVD SiO_2 (1 μm)/ Si structure. After analyzing, 2 specimens are discarded (outliers). Mean Gc is 31 J/m^2 with S.D. of 1.7 J/m^2.

Critical adhesion energy values outside between -2σ and $+2\sigma$ are discarded by this "residual" analysis. After eliminating outliers, new mean critical adhesion energy and its standard deviation are calculated and the final values are determined.

Figure 3.8 shows two examples using this residual analysis. Figure 3.8(a) represents an evaluation result of a bonded wafer pair. In this pair, 2.6 μm of BCB is sandwiched between two silicon wafers with 2 μm thermal oxide layers. The initial mean adhesion energy and standard deviation values from the full set of 8 data points are 34 J/m^2 and 3 J/m^2, respectively. Two of the 8 data points are outside the -2σ and $+2\sigma$ range (outliers). After discarding the outliers, the mean adhesion energy and standard deviation value are calculated again. The critical adhesion energy is 34 J/m^2 with a standard deviation of 2.2 J/m^2, and all values are within the -2σ and $+2\sigma$ range.

Figure 3.8(b) shows the results for another bonded wafer pair. In this pair, 2.6 μm of BCB is sandwiched between two silicon wafers with 1 μm PECVD oxide layers. Initial mean adhesion energy and standard deviation values computed using all 8 data points are 31 J/m^2 and 2.2 J/m^2, respectively. Two data points are outside between -2σ and $+2\sigma$ range. After discarding these outliers, the mean adhesion energy and standard deviation

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value are calculated again. Subsequently, the confirmed critical adhesion energy is 31 J/m^2 with a standard deviation of 1.7 J/m^2. For most bonded wafer pairs studied in the research on which this thesis is based, all critical adhesion energy values obtained are within the -2σ and $+2\sigma$ range.

3.3.1.4. Reproducibility Test Between Different Operators

Reproducibility of data by different people is an important measure for the acceptance of experimental results. To evaluate the effect of operator on critical adhesion energy measurements, two operators (A and B) conducted the bending experiments. Beam specimens are prepared by the same person (A) in order to minimize the error caused by differences in sample preparation.

A processed wafer with copper interconnects and oxide inter-level dielectric (ILD) (supplied by SEMATECH, see Section 7.2) was bonded to a silicon wafer with 2 μm thermal oxide layer using 2.6 μm BCB. Figure 3.9 shows the critical adhesion energy results, determined as described above by A and B, respectively. The mean critical adhesion energy of five specimens obtained by A is 22 J/m^2 and its standard deviation is 1.8 J/m^2. The mean critical adhesion energy of four specimens obtained by B is 23 J/m^2 and its standard deviation is 2 J/m^2. Four point bending tests performed by different

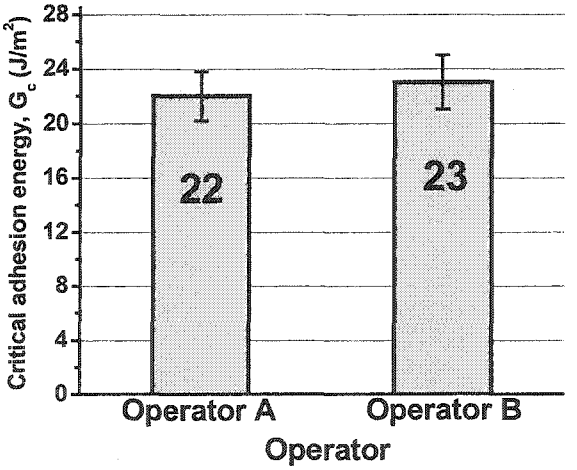


Figure 3.9: Reproducible test by different operators for obtaining critical adhesion energy. Mean G_c obtained by operator A is 22 J/m^2 with S.D. of 1.8 J/m^2, and mean G_c obtained by operator B is 23 J/m^2 with S.D. of 2 J/m^2.

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operators are reproducible.

3.3.2. Wafer Curvature and Built-In Stress

The cantilever beam technique measures the deformation of a substrate by a deposited film. This deformation can be used to calculate the film stress using theory developed by Stoney in 1909. According to this theory, film stress is obtained from the radius of curvature of a substrate with a given thickness, covered with a film [35]. It assumes that all observed curvature is due to stress in the thin film.

Stoney calculated the film stress by equating the forces and the moments of the film and the substrate, assuming that the system is under uniaxial stress. Figure 3.10 shows the geometrical structure for calculating the film stress. Stoney's formula is [92-93]:

$$\sigma = \frac{E_s h^2}{6Rt}\left[\frac{1}{1+\frac{t}{h}\left(1-4\frac{E_f}{E_s}\right)}\right] \tag{3.6}$$

where E_s is Young's modulus of the substrate and E_f is Young's modulus of the thin film (Pa), h is the substrate thickness (m), t is the film thickness (m), R is the radius of curvature (m), and σ is the film stress. In Equation 3.6, $\frac{E_s h^2}{6Rt}$ is the first term and

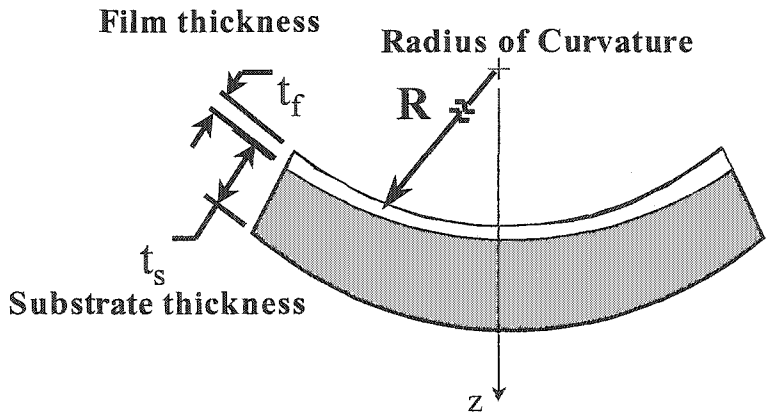


Figure 3.10: Geometric structure for calculating the film stress using Stoney's equation.

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$\frac{1}{1+\frac{t}{h}\left(1-4\frac{E_f}{E_s}\right)}$ is the second term. When the ratio of film thickness to substrate thickness is less than 0.01, the second term can be neglected [92-93].

In reality the stresses are normally biaxial, and thus Young's modulus, E, needs to be replaced by the biaxial modulus $E/(1-\nu)$. Assuming the stress to be isotropic in the plane of the film, Stoney's formula is modified to [92-93]

$$\sigma = \frac{E_s h^2}{6(1-\nu_s)Rt}\left[\frac{1}{1+\frac{t}{h}\left(1-4\frac{E_f(1-\nu_s)}{E_s(1-\nu_f)}\right)}\right] \tag{3.7}$$

This equation shows that film stress is proportional to the substrate curvature, 1/R. In this formula, $\frac{E_s h^2}{6(1-\nu_s)Rt}$ is the first term and $\frac{1}{1+\frac{t}{h}\left(1-4\frac{E_f(1-\nu_s)}{E_s(1-\nu_f)}\right)}$ is the second term. Similar to that in the uniaxial mode, when the ratio of film thickness to substrate thickness is less than 0.01, the second term is neglected. In this thesis work, since the maximum thickness of the thin film layer is 4 μm and the thickness of silicon/glass substrate is 730 μm, the second terms of Equations 3.6 and 3.7 are neglected (the ratio is less than 0.01). Finally, residual stress expressed by Stoney's equation is determined using the following expression:

$$\sigma = \frac{Eh^2}{6(1-\nu)Rt} \tag{3.8}$$

This equation shows that film stress is proportional to the substrate curvature, 1/R.

The measurement of radius of curvature is performed by scanning a laser beam across the substrate and measuring the angle of the reflected beam [94]. The substrate curvature 1/R is obtained by measuring the change of the reflected angle with distance along the

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substrate. From the curvature, the slope of the substrate surface (θ) can be calculated. In general, the curvature of a substrate can be written as,

$$\frac{1}{R} = \frac{\frac{d^2y}{dx^2}}{\left(1+\left(\frac{dy}{dx}\right)^2\right)^{3/2}} \tag{3.9}$$

where, x is the distance along the scan direction and y is the substrate deflection. For small deflections where $(dy/dx)^2$ is much smaller than 1, the curvature can be expressed as,

$$\frac{1}{R} = \frac{d^2y}{dx^2} = \frac{d\left(\frac{dy}{dx}\right)}{dx} = \frac{d\theta}{dx} \tag{3.10}$$

where θ is the substrate surface slope dy/dx, and therefore, the curvature, 1/R, is obtained by linear regression of a graph of θ versus x [94].

As the original bare substrate is rarely flat, to measure the film stress it is necessary to measure the substrate curvature before film deposition, $1/R_1$, as well as the curvature after the deposition, $1/R_2$, and thus, Equation 3.7 becomes,

$$\sigma = \frac{Eh^2}{6(1-\nu)t}\left(\frac{1}{R_2} - \frac{1}{R_1}\right) \tag{3.11}$$

The cantilever beam technique can also be used for measuring wafer bow. Figure 3.11 shows the geometrical structure for measuring wafer bow (or y direction deflection). The radius of curvature is computed for this structure, using the small deflection theory and Taylor series. The radius of curvature is found to be constant everywhere over the entire area. Consequently, the deflection in the y direction can be expressed as

$$y = R - \sqrt{R^2 - r^2} = R\left(1 - \sqrt{1 - \left(\frac{r}{R}\right)^2}\right) = R\left(1 - \left(1 + \frac{1}{2}\left(\frac{r}{R}\right)^2\right)\right) = -\frac{1}{2}\frac{r^2}{R} \tag{3.12}$$

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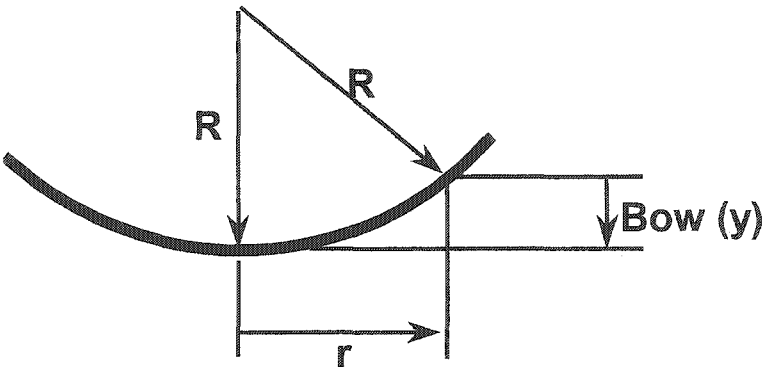


Figure 3.11: Geometric structure for calculating the wafer bow using Stoney's equation.

where r is the radial distance along the curved surface [94]. Figure 3.12 shows y vs. r curve for a 200 mm wafer with a center-down, edge-up (concave up) bow. Wafer bow versus wafer radial distance curve for 200 mm wafers is presented in Figure 3.12.

3.4. Material Characterization Techniques

In this section, FTIR and ellipsometry are introduced. First, the theory and applications for FTIR are described. The characterization is used to evaluate chemical structure changes during bonding process. Ellipsometry, which is used to measure glue thickness, is then described.

3.4.1. Fourier Transform Infrared (FTIR) Spectroscopy

Fourier Transform Infrared (FTIR) spectroscopy uses the infrared region of the

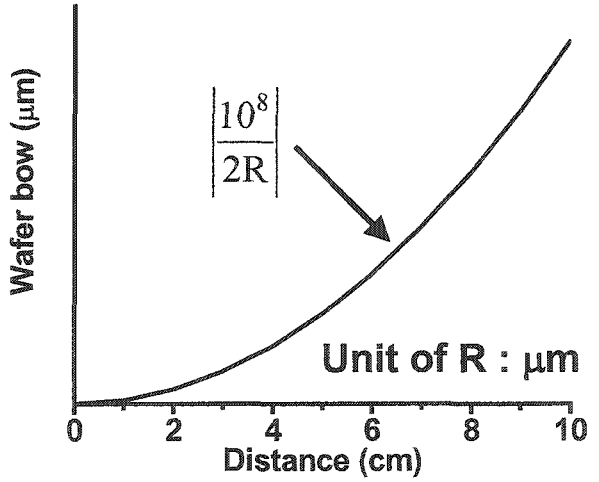


Figure 3.12: Wafer bow versus wafer radial distance curve for 200 mm wafers.

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spectrum for qualitative and quantitative analyses [95]. When infrared radiation interacts with molecules, the molecules may absorb portions of the radiation causing them to change rotational and/or vibrational states. The precise frequency of radiation that the molecule absorbs depends on the functional groups in the molecules of the sample. Molecules that absorb infrared radiation show a characteristic pattern of absorbed frequencies called an absorbance spectrum. The absorbance spectrum is unique to each individual molecule, like a fingerprint, making Infrared spectroscopy a powerful forensic and analytical tool for the identification of compounds in a mixture. The amount of radiation that is absorbed is directly proportional to the amount of the compound present (or the compound's concentration). Therefore, by carefully measuring how much radiation is absorbed when infrared light passes through a mixture of compounds, the concentration of each compound can be determined. IR spectroscopy is a potent tool for simultaneously identifying numerous chemical compounds and their respective concentrations.

The Fourier transforms convert time-based signal data into the frequency domain. In an IR spectrometer, radiation is passed through the sample and measured by a photomultiplier as a timed signal. As the IR beam enters the spectrometer it is split into two separate paths. One path travels to a mirror at a fixed distance, whereas the other beam ventures to a moving mirror whose position varies uniformly with time. The beams reflect back off these mirrored surfaces and recombine. Depending on the position of the moving mirror at the time of the beams' reflections determines the degree of destructive and constructive interference upon recombination. The pattern of this interference, called an interferogram, is a time-based function. The signal that the photomultiplier senses is this interference pattern. Applying the Fourier transform to these data allows us to express the data as a function of frequency producing a pattern of absorbed frequencies.

3.4.2. Spectroscopic Ellipsometry

Ellipsometry measures the change in polarization state of light reflected from the interfaces of a sample. An ellipsometric measurement provides two independent parameters, the change in relative phase (Δ) and the change in relative amplitude (ψ) of the orthogonal electric field components of light upon reflection. The ellipsometric angles

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Δ and ψ are functions of the layer thickness and complex refractive index. Variable Angle Spectroscopic Ellipsometry (VASE) [96-97] measures the quantity ρ (ratio of reflection coefficients) both as a function of wavelength and the angle of incidence. The dependence is expressed as

$$\rho = \tan\Psi \cdot e^{i\Delta} = f(n, k, d) \tag{3.13}$$

where n and k are the real and complex parts of the refractive index (RI), while d is the thickness of substrate. All measurements for the research reported here are made on J. A. Woolam Co., Inc., M-44 spectroscopic ellipsometer (Woolam Co., Lincoln, NE) [96]. The data are gathered at 44 wavelengths from 410 nm to 742 nm for three incident angles, typically 65 °, 70 ° and 75 °. A simple Cauchy model given by

$$n(\lambda) = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4}, \qquad k(\lambda) = 0 \tag{3.14}$$

was fitted to the data. A, B, C are the model fit parameters. Once the Cauchy constants A, B, C are fixed, thickness matched with the constants is determined [96]. The RI values quoted in this thesis are measured at a wavelength of 634.1 nm.

3.5. Summary

The experimental techniques used in this thesis are described in this chapter. First, wafer bonding equipment and dielectric glue bonding procedures are presented. Baseline spin-on, baking and bonding procedures for four glue candidates are described, including the bonder configuration and key process parameters.

Four point bending, used to quantify bond strength at the relevant interface is discussed. The cantilever beam method to measure wafer curvature and estimate residual stress is discussed.

For material characterization, both Fourier transform infrared spectroscopy (FTIR) and spectroscopic ellipsometry are used. Changes in chemical structure such as curing of the glue materials during bonding are evaluated using FTIR. Spectroscopic ellipsometry is used to measure thickness of glues.

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CHAPTER 4
POLYMERIC GLUE SCREENING

4.1. Overview

Evaluation procedures to determine a baseline polymeric glue material and bonding process are described in this chapter. Accurate screening results using all four glue candidates are important because improper wafer-bonding evaluation can lead to subsequent mechanical and electrical degradations in subsequent thinning, thermal cycling and electrical evaluations.

Bonding results can be evaluated by both direct methods, such as optical inspection and image processing, and indirect methods, such as four point bending or residual stress measurement. Direct methods are used to qualitatively inspect; (1) the fraction of bonded area, (2) the number of voids, (3) the size of voids, and (4) the glue thickness variation. Since fast and easy-to-explain results are obtained using this direct method, it is used for initial glue screening purpose.

Indirect methods are used to characterize the quality of bonding result quantitatively. Properties such as bond strength and residual stress at the glue interface are used as criteria to determine bonding quality. The quantitative results of bonded wafer pairs are treated in Chapters 5, 6 and 7.

First we describe glue screening using optical inspection. Candidates showing small fractions of bonded area and low bond strengths are eliminated. Theoretical reasons for the low quality of bonding results are given. FTIR is performed to analyze changes in chemical structure during the bonding process, of the accepted glue materials. Deductions can be made about their cure and bonding mechanisms from the FTIR studies. Finally, four point bending tests are done to quantify the difference in bond strength of bonded wafers using BCB and Flare.

Based on optical inspections and bond strength evaluations, BCB is selected as the baseline bonding glue, due to routinely good void-free bonding results and high bond strength compatible with subsequent BEOL processes.

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4.2. Optical Inspection with Transparent Wafers

In this section, optical inspection results using bonded wafer pairs that include transparent wafers are discussed. From initial screening tests of bonded wafers using four glue candidates, two candidates, MSSQ and Parylene-N are removed due to their low fractions of bonded area and weak bond strengths. When the remaining two candidates, Flare and BCB are compared, wafer bonding using BCB has routinely shown void-free bonding results, and high bond strength using four point bending. Flare is removed due to voidage, although wafer bonding using Flare has shown higher bond strength than that using BCB. These evaluations are described.

4.2.1. Initial Screening Results

After bonding, optical inspection is used to observe the fraction of bonded area. The bond strength is evaluated qualitatively using a razor blade to attempt to separate the wafers. It is found that the fraction of bonded area and the bond strength depend on the material properties, and the applied pressure and loading time during bonding. Particles and defects also influence the bonding results [52-53].

Figure 4.1 shows a photograph of wafers (200-mm Corning 7740 glass wafer to p-type (100) prime silicon wafer) bonded using MSSQ, and Figure 4.2 shows a photograph of a wafer pair (Corning glass to silicon wafer) bonded using parylene-N. In both bonded wafer pairs, the coefficient of thermal expansion (CTE) of Corning glass wafers (3.25 ppm/°C) [98] is well matched with that of silicon wafers (3.2 ppm/°C). The bonding results of both glues by optical inspection show small fractions of bonded area, qualitative razor blade tests of the glues show low bond strength.

In wafer pairs bonded using MSSQ, many voids are observed at the bonding interfaces, resulting in a small fraction of bonded area. It is believed that water created by a condensation reaction during bonding is the main reason for the voids. The cure reaction of MSSQ that occurs during bonding is

$$2\ \text{Si-OH} \rightarrow \text{Si-O-Si} + H_2O \qquad (4.1)$$

Undesirable water vapor along with desirable siloxane bonds are created from this reaction. In particular, it is difficult for the water formed to diffuse to the wafers' edges.

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The water remains at the bond interface or glue-to-glue surface during the bonding process, thereby forming voids [55-56].

The wafer pairs bonded using parylene-N show weak bonding strength through razor blade test. The bonded wafers were fully delaminated by the razor blade test. As shown in Figure 4.2, the fraction of bonded area is small. The natural crystallinity and the possibility of oxidative chain scission during heating step result in weak bonding strength [87-89]. When parylene resins are polymerized, the polymer chains have restricted motion due to the crystallinity [99]. With heating, the polymer chains are readjusted toward the thermodynamically most stable form, increasing crystallinity. As mentioned in Section 3.2, crosslinking and interdiffusion reactions, which are necessary for obtaining strong interfacial adhesion energy, are not generated well in the crystalline state. Oxidative chain scissions occur when hydrogen abstraction by oxygen incorporation is the predominant reaction pathway for parylene-N polymeric, as illustrated in Figure 4.3 [87].

Rupture of chains is another problem for parylene-N. The oxygenation of the free radical center results in one less electron in the highest occupied molecular orbital (this consists of mainly carbon-carbon sigma bond), causing the hydrocarbon backbone to weaken and lead to chain scissions. The ruptured chains (see Figure 4.4) can get charred

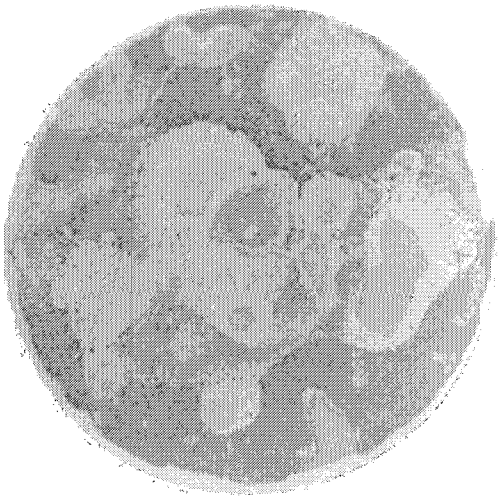


Figure 4.1: Wafer bonding result using MSSQ. Bonded wafer pair (200mm): P (100) prime wafer and Corning 7740 glass wafer.

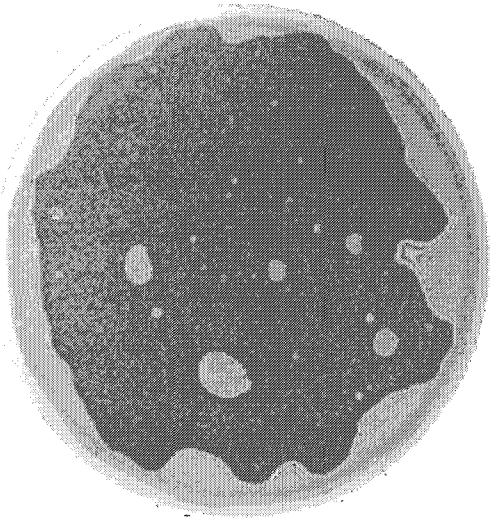


Figure 4.2: Wafer bonding result using Parylene-N. Bonded wafer pair (200mm): P (100) prime wafer and Corning 7740 glass wafer.

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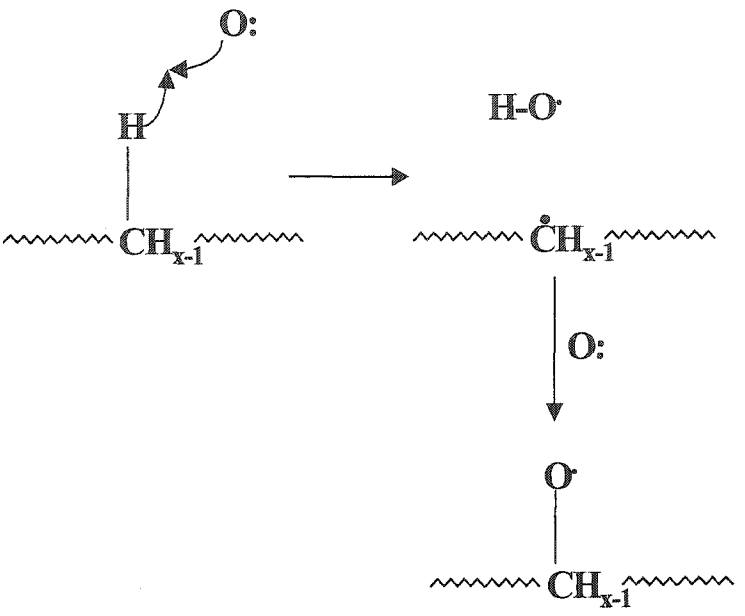
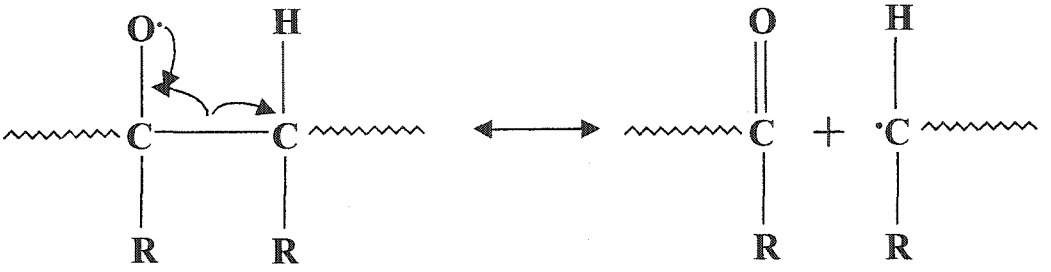


Figure 4.3: Oxygenation reaction of free radical center, which is the main reason of oxidative chain scissions [87].



Where R=H or CH_3

Figure 4.4: The rupture reaction resulting from oxygen radical [87].

at high enough temperatures, and induce outgassing [100-101].

Figure 4.5 shows a photograph of a wafer pair (200-mm Corning 7740 glass wafer to p-type (100) prime silicon wafer) bonded using Flare, and Figure 4.6 shows a photograph of a wafer pair (Corning glass to silicon wafer) bonded using BCB. Compared to the bonding results using MSSQ and parylene-N, the fraction of bonded area using Flare and BCB are much higher. Thus, BCB and Flare were selected in this initial screening procedure.

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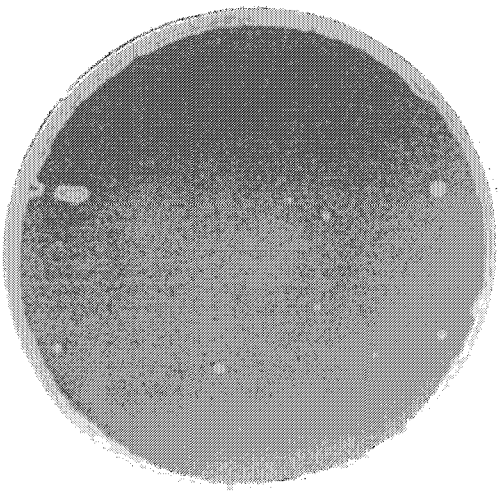


Figure 4.5: Wafer bonding result using Flare. Bonded wafer pair consists of(200mm): P (100) wafer and Corning glass wafer.

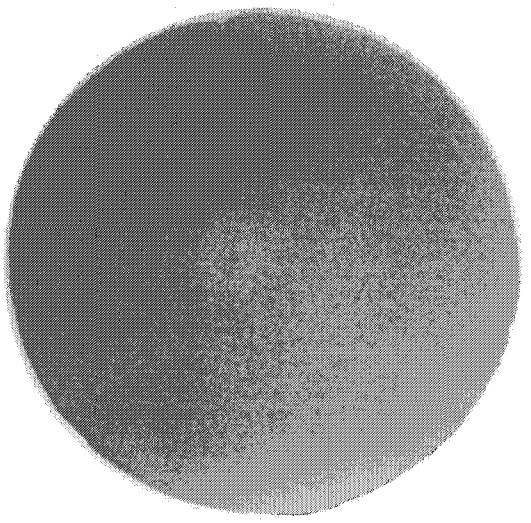


Figure 4.6: Wafer bonding result using BCB. Bonded wafer pair consists of (200mm): P (100) wafer and Corning glass wafer.

4.2.2. Comparison of Flare and BCB

With Flare, the number of visible voids is smaller than that for bonding using MSSQ and parylene-N (comparing Figure 4.5 with Figures 4.1 and 4.2). Since Flare consists of aromatic or bis-phenol precursors that have a rigid structure, and does not have outgassing sources within its chemical structure, by-products or condensates are few generated during bonding process, except for any solvent that remains after heating [59-60]. The solvents remaining even after baking are placed in the entangled polymer resins. Beyond the curing temperature, the entangled polymer resins are disentangled and solvents are exposed, which are then outgassed.

Other positive points of wafer bonding using Flare are high thermal stability and good solvent and moisture resistance. The high thermal stability is caused by the aromatic components of Flare resin, and the good solvent and moisture resistance stems from the hydrophobic property of Flare [59]. However, while wafer pairs bonded using Flare show very large fractions of bonded area, they are not as good as the void-free bonding results obtained with BCB (comparing Figures 4.5 and 4.6).

It is believed that solvent remaining in the Flare resin prevents void-free bonding. Unlike other glue candidates, the glass transition temperature of Flare resin is almost identical to the final bonding temperature (~400 °C). We believe that crosslinked polymer resins of Flare move because the cure temperature is close to glass transition temperature.

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The movement of resins can lead to exposure of the remaining solvents that are within the entangled Flare resins, and the exposed solvents may form the voids [81-82].

The wafer bonding quality using BCB is very good and wafer pairs bonded using BCB routinely show void-free bonding results. The "interlocking action" (due to re-flow) in BCB is the main reason for the void-free bonding result [102]. The polymer resins of BCB are more "liquid-like" than those of other glue candidates because the resins lead to higher crosslinking reaction density; this interlocking action can fill the empty spaces around particles. Proof of the interlocking action is seen in the change of "edge bead removal" area after bonding [52-53]. In the spin-on process, the glue on the wafer edge may be removed to prevent the void generation caused by edge bead formation. The "edge bead removal" area of wafer pairs bonded using Flare hardly changes during the wafer bonding (see Figure 4.5). However, the "edge bead removal" area of wafer pairs bonded using BCB almost disappears, *i.e.*, the BCB interlocking action fills "edge bead removal" area (see Figure 4.6) [52].

Another piece of evidence about this reflow property is the bonding result using a patterned silicon wafer and a blanket glass wafer. While the patterned wafer has a height difference of 0.9 μm across its surface and glass wafer is flat, optical inspection of the bonded pair indicates the absence of voids at the interface (see Figure 4.7). The BCB resins apparently move, squeeze into the channels, and fill the topological gaps among the channels while the curing reaction is done under pressure. More details about patterned wafer bonding using BCB are addressed in Chapter 7.

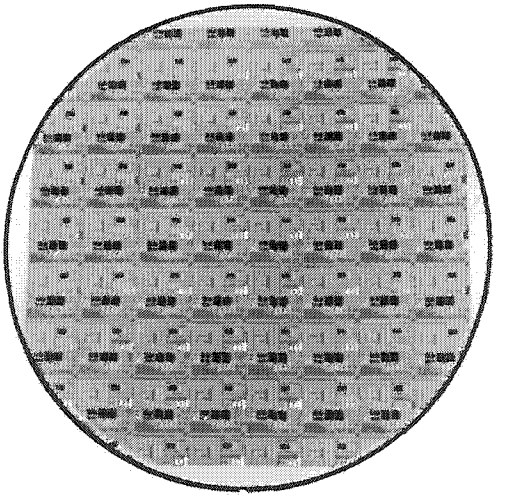


Figure 4.7: Wafer bonding result using BCB. Bonded wafer pair consists of patterned wafer (sent from SEMATECH) and Corning glass wafer.

Although the quality of bonding is quite good, some issues related to BCB bonding still remain. Three specific issues are; 1) void generation due to chemical impurities within polymer, 2) void or bonding defect generation due to particles, and 3) non-uniform thickness variation due to BCB resin reflow during

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bonding.

In summary, BCB and Flare pass optical inspection and the qualitative razor blade test. Bonded wafer pairs using other glue materials such as MSSQ and Parylene-N showed only small fractions of bonded area and/or are delaminated during the razor blade test. Of the Flare and BCB, wafer pairs bonded using BCB routinely show void-free bonding result. Even though Flare has advantages compared to BCB, such as thinner glue thickness and higher thermal stability, voids are usually generated during the bonding process. Based on these screening test results, BCB is chosen as the glue for the baseline process, and for more detailed studies.

4.3. Chemical Analysis of Flare and BCB using FTIR

Fourier Transform Infrared Spectroscopy (FTIR) is used to shed light on details of the bonding mechanism, such as the cure reaction and carrier solvent evaporation. The bonding mechanisms of Flare and BCB are estimated using FTIR [52]. Figure 4.8 shows FTIR spectra for Flare films. The Flare FTIR spectra, (Figure 4.8), indicate that the "as spun" sample has seven main peaks, summarized in Table 4.1.

This spectrum confirms the presence of cyclohexanone solvent in Flare, because the cyclohexanone consists of two C-H groups and a carbonyl group. However, the solvent (cyclohexanone) peaks (C-H and C=O bonds) disappear after thoroughly baking at

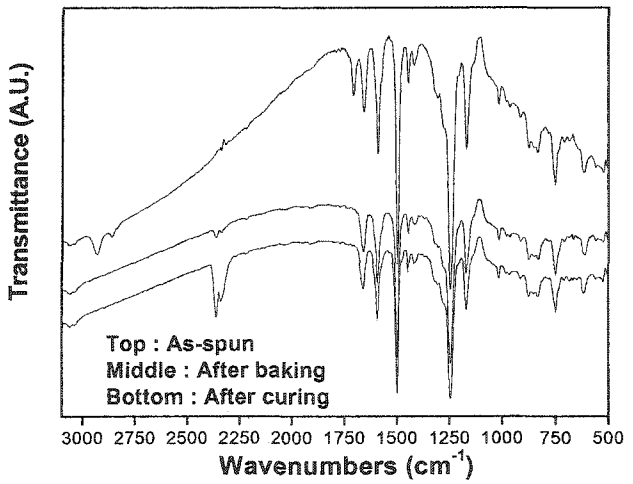


Figure 4.8: FTIR spectra of Flare for the samples as spun, after bake (up to 250°C) and after cure reaction (one hour at 400°C).

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Table 4.1: Peak position and peak assignments of Flare

Peak Position (cm^{-1})	Peak assignment
1240	Symmetric R-O-R (ether) stretching
1500	Asymmetric R-O-R (ether) stretching
1590	Aromatic C=C
1650	C=O stretching of benzophenone moiety
1700	C=O carbonyl
2930	C-H stretching
3050	C-H stretching of phenyl group

250 °C. No difference is observed in the FTIR peaks between after-baking and after-curing of Flare deposited on a prime Si wafer. These results suggest the removal of solvent or by-product caused by reactions after such a bake. Therefore, outgassing does not occur during bonding, and the main source for void formation may be due to particles.

As shown in Figure 4.9, the BCB FTIR spectrum of the sample before bonding shows a typical result for BCB monomer, as summarized in Table 4.2. After the bonding process (one hour at 250 °C), the vinyl stretch and wag peaks and benzene side ring peaks disappear, the tetralin peak (1500 cm^{-1}) is strengthened and an aliphatic C-H peak (3005 and 2925 cm^{-1}) is produced. This result indicates that BCB monomers are crosslinked (cured) during the wafer bonding process.

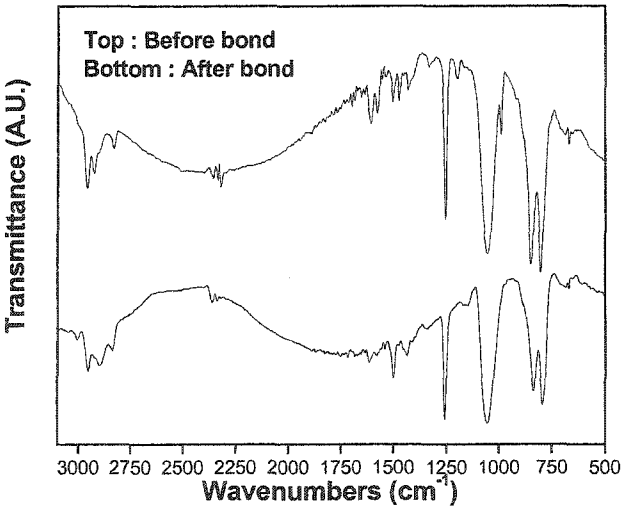


Figure 4.9: FTIR spectra of BCB for the samples before and after bonding/curing (one hour at 250°C).

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Table 4.2: Peak position and peak assignments of BCB

Peak Position (cm^{-1})	Peak assignment
985	Aliphatic C=C wagging
1049	Si-O-Si
1194	Aliphatic C=C wagging
1250	$Si-CH_3$
1473	Benzene side ring stretching
1500	Tetralin
2925	Aliphatic C=C stretching
3005	Aliphatic C-H

4.4. Bond Strength Comparison between BCB and Flare

Wafer pairs bonded using BCB and Flare show large fractions of bonded area and high bond strengths. As a next step, quantitative characterization of bond strength in wafer pairs bonded using both glue materials needs to be done to evaluate the possibility of delamination of glue materials, and to confirm the baseline glue material for wafer bonding. The four point bending method, which is introduced in Section 2.6, is used for the quantitative evaluation of bond strength. Glass to silicon wafer bonding using BCB and Flare are used as geometrical structure.

Figure 4.10 shows the bonded wafer structure using BCB or Flare. The CTE of the glass wafers are well matched with that of the silicon wafers. The thickness of BCB used is 2.6 μm and that of Flare is 0.6 μm. For BCB, an adhesion promoter (AP 3000) is employed to enhance the bond strength. The increase in bond strength by the use of

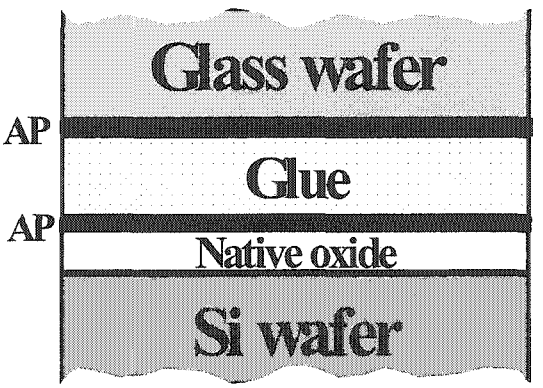


Figure 4.10: Geometrical configuration of bonded wafer pair using BCB and Flare.

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adhesion promoter is attributed to reactions between the adhesion promoter and BCB resin and substrate. Section 5.2 explains the role of adhesion promoter in increasing bond strength.

Figure 4.11 represents the critical adhesion energies of both glue materials. Even though the thickness of Flare is thinner than that of BCB, the critical adhesion energy of Flare is 18 J/m^2 with standard deviation of 2.2 J/m^2, and that of BCB is 9 J/m^2 with standard deviation of 0.9 J/m^2. The critical adhesion energy using Flare is higher by a factor of two over that of BCB, even though the Flare is four times thinner. With both glue materials, the weak interface is in between the glass wafer and the glue layer.

Hydroxyl groups of the Flare resin adhere to silanol groups (Si-OH) of the glass wafer and native oxide layer of the silicon wafer; strong siloxane bond groups (Si-O-Si) are formed by condensation reactions during high temperature processing (400 °C). In bonding using BCB, one end of the adhesion promoter forms siloxane bond groups with glass wafer and native oxide layer of silicon wafer, and the other side forms covalent bond with BCB resins [75,78]. It is believed that the density of reactive groups in Flare is higher than that of BCB, and the difference of density leads to the critical adhesion energy difference.

However, the critical adhesion energy of BCB is high enough to resist delamination

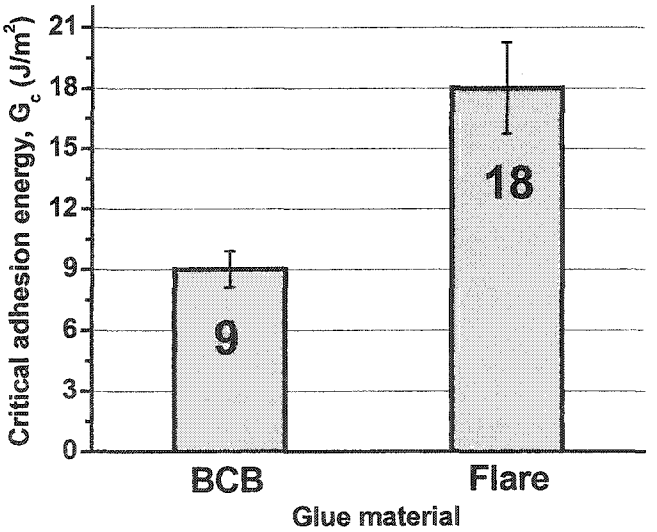


Figure 4.11: Critical adhesion energies of bonded wafer pairs using BCB and Flare. Bond strength of bonded wafer using BCB is 9 J/m^2 with S.D. of 0.9 J/m^2 and that using Flare is 18 J/m^2 with S.D. of 2.2 J/m^2.

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during subsequent processing (these evaluations are addressed in chapters 5, 6 and 7). Furthermore, as has been noted, since the fraction of bonded area using BCB is higher than that using Flare, BCB is finally determined as baseline bonding glue material.

4.5. Summary

Evaluation procedures to determine a baseline polymeric glue material and bonding process are presented. Direct optical inspection was mainly used to screen glue materials. MSSQ and Parylene-N candidates were eliminated by this evaluation due to their small fraction of bonded area, as well as their low qualitative bond strength (razor blade test). BCB and Flare show large fractions of bonded area and high bond strength, although BCB routinely shows void-free bonding.

Solvent evaporation during baking for Flare and curing reaction during bonding process for BCB have been analyzed by FTIR. Bond strengths and weak interfaces of wafers bonded using BCB and Flare, when sandwiched between a glass wafer and a silicon wafer, have been measured and identified. Based on these optical inspection and bond strength evaluations, BCB is selected as the baseline bonding glue.

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CHAPTER 5
QUANTITATIVE EVALUATION OF BCB BOND STRENGTH

5.1. Overview

Maintaining excellent bonding integrity after the bonding process, both during subsequent processing and during operation, is critical for 3D ICs and other wafer bonding applications. Bonded wafer pairs usually experience thermal and mechanical loads during subsequent processing steps, *e.g.*, mechanical thinning and grinding, chemical mechanical planarization (CMP), as well as thermal shocks due to deposition, etch and other processing steps. Bonded wafer pairs should have high bond strengths to minimize problems such as interfacial adhesive failure, glue delamination, or edge chipping. Four-point bending measurements of critical adhesion energy (bond strength), performed as described in Chapter 2.6, are used as the starting point for quantifying bonding integrity. Designing for bonding integrity can involve trade-offs with other design issues. For example, in 3D IC integration it may be desirable to keep the glue layer as thin as possible in order to maintain the aspect ratios of vertical inter-wafer interconnect vias reasonably low [101-102]. However, bonding integrity may decrease when using too thin a glue layer, leading to adhesive failure.

We consider BCB to be the baseline glue material for 3D integration, based on results of glue screening tests presented in Chapter 4 [52-53]. In this chapter, bonding quality and integrity of the BCB are evaluated under different chemical and structural conditions. We evaluate conditions that influence bonding quality and integrity, namely glue layer preparation (*e.g.*, adhesion promoter and surface treatment), glue layer thickness, and identity of material on the substrate surfaces (*e.g.*, silicon, silicon oxides, glass and metal). Parameters for a baseline process using BCB as a bonding glue are also presented.

5.2. Adhesion Promoter Effects

Dow Chemical Company, the manufacturer of BCB, recommends the use of their AP3000 as an adhesion promoter. We evaluate the effect of this adhesion promoter on bond strength by four-point bending. Four different bonded wafer pairs are prepared as

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Table 5.1: Four point bending results of four types of bonded wafer pairs

Geometric configuration of beam specimen	BCB thickness	Load-plateau	n	Mean G_c (J/m^2)	S.D. (J/m^2)
$Si/SiO_2/AP/BCB/AP/SiO_2/Si$	2.6 μm (double layer)	Type 1	6	31	1.7
$Si/SiO_2/BCB/SiO_2/Si$	2.6 μm (double layer)	Type 1	6	13	0.5
$Si/SiO_2/AP/BCB/AP/SiO_2/Si$	0.4 μm (single layer)	Type 1	7	19	0.7
$Si/SiO_2/BCB/AP/SiO_2/Si$	0.4 μm (single layer)	Type 1	6	10	0.4

shown in the first two columns of Table 5.1. Several beam samples were prepared for each bonded wafer pair (n in Table 5.1), in order to estimate the standard deviation of the measured adhesion energy.

A 1.3 μm thickness of BCB is spun on both wafers for a total of 2.6 μm in the first two ("baseline-thickness BCB") wafer pairs of the four bonded wafer pairs. In the first baseline-thickness BCB wafer pair, both wafers are coated by adhesion promoter and BCB. The adhesion promoter used (AP3000, Dow Chemical Company) consists of silane-based molecules and a vinyl reactive functional group. In the second baseline-thickness BCB wafer pair, both wafers are coated by BCB without the use of adhesion promoter. In these bonded wafers pairs, the BCB layer is sandwiched between two silicon wafers covered with 1 μm PECVD oxide layers.

Figure 5.1 shows the beam specimen configurations and critical adhesion energies of the two baseline-thickness BCB bonded wafer pairs. The critical adhesion energy

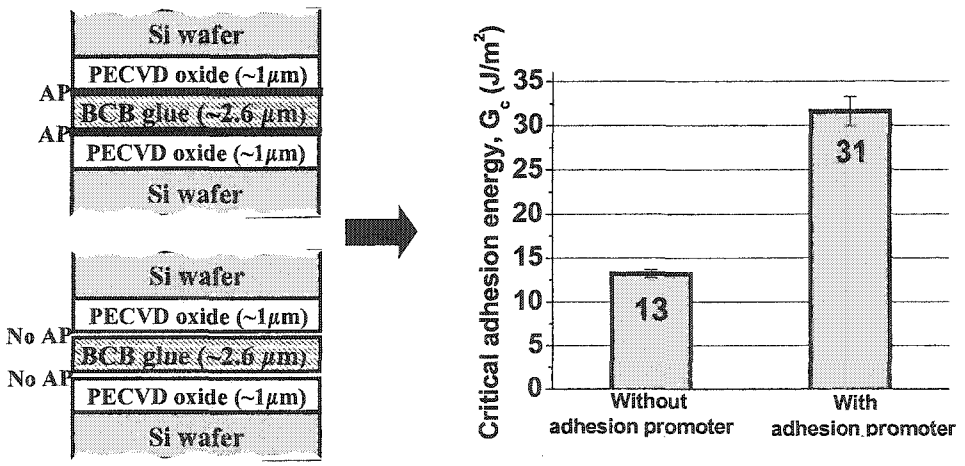


Figure 5.1: Beam specimen configurations and critical adhesion energies of bonded wafer pairs including double layer BCB with and without adhesion promoter.

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measured in the specimens prepared from the pair with adhesion promoter (31 J/m^2) is more than twice of those from wafers bonded without adhesion promoter (13 J/m^2). (See Table 5.1). A "Type 1" (see Section 3.3.1.3) load vs. displacement curve (linear elastic→load plateau→linear elastic) is apparent in the four point bending tests with both baseline-thickness BCB bonded wafer pairs.

A single layer of BCB of 0.4 μm thickness is spun on the other two ("thin BCB") bonded wafer pairs. In the first thin BCB wafer pair, adhesion promoter and BCB are deposited on the top wafer and only adhesion promoter is deposited on the bottom wafer. After the adhesion promoter and BCB layers are spun on, baseline baking and bonding processes are conducted (see Section 3.2 for baseline bonding process). In the other thin BCB bonded wafer pair, adhesion promoter and BCB are deposited on the top wafer, and the bottom wafer is left bare. These two wafers are also baked and bonded using the baseline processes. In these thin BCB bonded wafers, the BCB layer is sandwiched between two silicon wafers with 1 μm PECVD oxide layers. Figure 5.2 shows the beam specimen configurations and critical adhesion energies of the two bonded wafer pairs. The critical adhesion energy measured in the specimens prepared from the pair with adhesion promoter (19 J/m^2) is almost a factor of two higher than those from the pair without adhesion promoter (10 J/m^2) (see Table 5.1). Load vs. displacement curves show "Type 1" behavior in both thin BCB bonded wafers pairs.

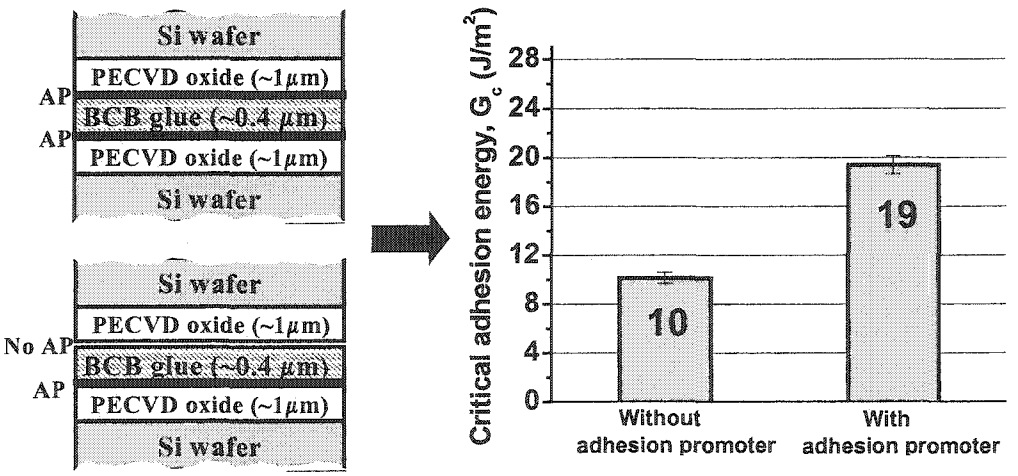


Figure 5.2: Beam specimen configurations and critical adhesion energies of bonded wafer pairs including one layer BCB with or without adhesion promoter.

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The increase in critical adhesion energy due to the use of adhesion promoter is attributed to reactions between the adhesion promoter, BCB resin, and PECVD oxide. Figure 5.3 shows the chemical structure of the adhesion promoter, AP3000 [73, 103] and Figure 5.4 represents the bonding mechanism of the adhesion promoter across the interface between the BCB resin and PECVD oxide. The vinyl end group of AP3000 reacts with the vinyl group of the BCB resin and forms strong covalent bonds. Silane-based molecules (triacetoxysilane, $Si(OCOCH_3)_3$) in the AP3000 react with dangling hydroxyl groups (Si-OH) on the surface of the oxide layer to create strong siloxane bonds (Si-O-Si). The presence of these strong bridging bonds lead to increased interfacial

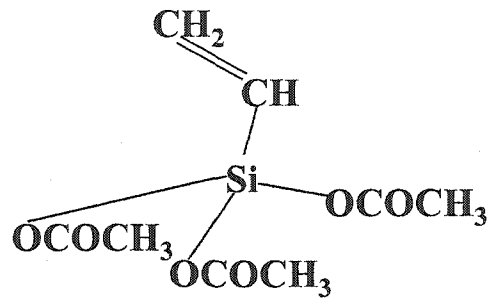


Figure 5.3: Chemical structure of adhesion promoter, AP3000. The adhesion promoter consists of silane based molecules (triacetoxysilane, $Si(OCOCH_3)_3$) and vinyl functional group.

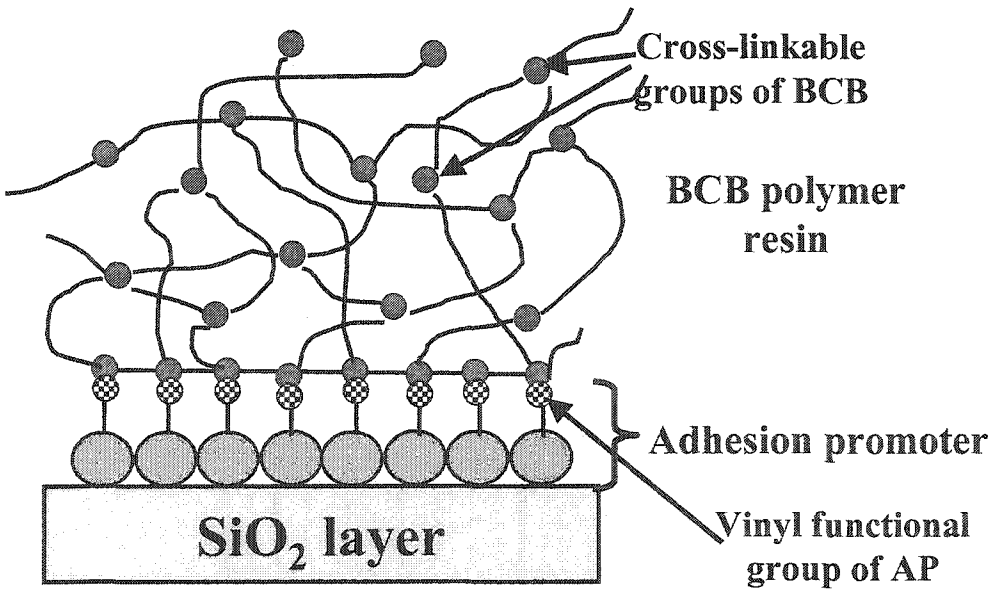


Figure 5.4: The bonding mechanism across BCB to oxide layer using adhesion promoter.

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strength. When no adhesion promoter is employed, the BCB resin and oxide layer are in direct contact, and these strong covalent bonds are not present [101].

It is worth noting that the 0.4 μm thick BCB layers, when used with the adhesion promoter, have a critical adhesion energy of 19 J/m^2 for bonded wafers that are coated with PECVD oxide. This critical adhesion energy is still higher than reported values of fusion bonded wafers (~5 J/m^2) [50].

5.3. BCB Thickness Effects

The BCB thickness affects both the required length of vertical inter-wafer interconnects in 3D IC structures and the bond strength of the glue layer, as discussed in Section 5.1. Since thin glue layers are generally preferred for 3D ICs, but bond strength decreases with decreasing glue thickness, quantification of the bond strength to determine a threshold glue thickness is highly desirable. Other issues such as wafer surface topology and contamination need to be considered as well, particularly, as the BCB thickness is reduced below ~2 μm.

Beam specimens prepared with different BCB thicknesses and different substrate surface layers are used to evaluate the effect of BCB thickness on bond strength. Deposited BCB thickness is varied from 7 μm to 0.4 μm. In one set of three bonded wafer pairs (samples 1, 2 and 3 in Table 5.2), the glue layer is sandwiched between two silicon wafers coated with 1 μm PECVD oxide layers. The thickness of BCB varies from 2.6 μm to 0.4 μm. Figure 5.5 shows the geometric configuration of these bonded wafer

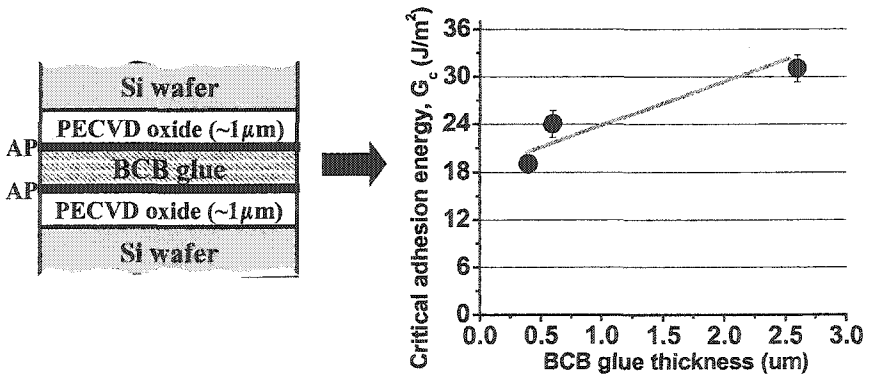


Figure 5.5: Beam specimen configurations and critical adhesion energies in different BCB thicknesses. BCB layer is sandwiched by PECVD oxide deposited silicon wafers.

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pairs and bond strengths for different BCB layer thicknesses (see Table 5.2 for results). In all of these evaluations, adhesive failure is observed at the BCB to substrate (oxide surface) interface. Load vs. displacement curves show "Type 1" behavior in all three wafer pairs.

In a second set of two wafer pairs (samples 4 and 5 in Table 5.2), the glue layer is sandwiched between two silicon wafers coated with 2 μm thermally grown oxide layers, and the thicknesses of BCB are 2.6 μm and 0.6 μm. Figure 5.6 shows the geometric configuration and the bond strength results (also see Table 5.2). Even in these bonded wafer pairs, adhesive failures are observed at the BCB interface. Load vs. displacement curves show "Type 1" behavior in both wafer pairs.

In a third set, the glue layer is sandwiched between a silicon wafer with a native oxide layer of 1.4 nm thickness and a glass wafer (samples 7, 8, 9 and 10 in Table 5.2). The CTE of the glass wafer is well matched to that of silicon. The thickness of BCB is varied

Table 5.2: Four point bending results in different BCB thicknesses

Sample #	Geometric configuration of beam specimen	BCB thickness	Load-plateau	n	Mean G_c (J/m^2)	S.D. (J/m^2)
1	Si/PECVD SiO_2/AP/BCB /AP/ PECVD SiO_2/Si	2.6 μm (double layer)	Type 1	6	31	1.7
2	Si/PECVD SiO_2/AP/BCB /AP/ PECVD SiO_2/Si	0.6 μm (double layer)	Type 1	5	24	1.7
3	Si/PECVD SiO_2/AP/BCB /AP/ PECVD SiO_2/Si	0.4 μm (single layer)	Type 1	7	19	0.7
4	Si/Thermal SiO_2/AP/BCB /AP/ Thermal SiO_2 /Si	2.6 μm (double layer)	Type 1	6	34	2.2
5	Si/Thermal SiO_2/AP/BCB /AP/ Thermal SiO_2 /Si	0.6 μm (double layer)	Type 1	6	25	2.3
6	Si/Native SiO_2/AP/BCB /AP/Native SiO_2/Si	2.6 μm (double layer)	Type 1	6	30	1.4
7	Glass/AP/BCB/AP/Si	7 μm (double layer)	Type 1	7	17	0.6
8	Glass/AP/BCB/AP/Si	4.8 μm (double layer)	Type 1	7	14	1.2
9	Glass/AP/BCB/AP/Si	2.6 μm (double layer)	Type 1	7	9	0.9
10	Glass/AP/BCB/AP/Si	1.3 μm (single layer)	Type 1	7	7	0.1

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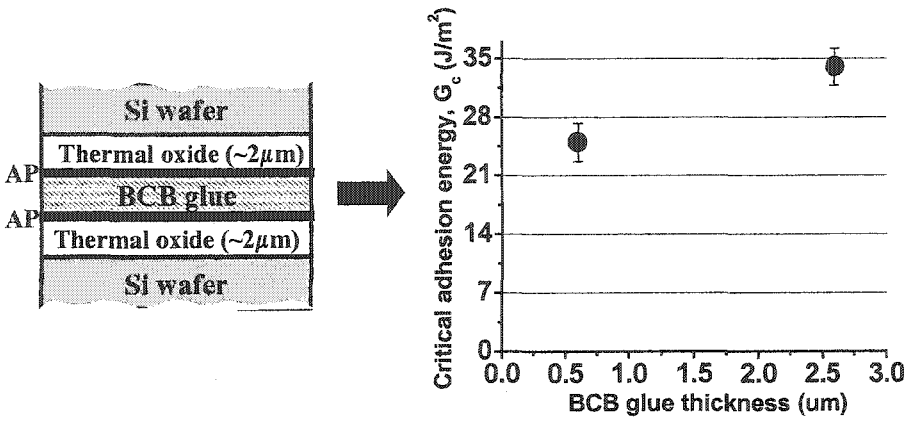


Figure 5.6: Beam specimen configurations and critical adhesion energies in different BCB thicknesses. BCB layer is sandwiched by thermal oxide deposited silicon wafers.

from 7 μm to 1.3 μm. Figure 5.7 shows the geometric configurations and the bond strengths in different BCB layer thicknesses. Load vs. displacement curves show "Type 1" behavior in these bonded wafer pairs.

As BCB thickness decreases within a given wafer set, the critical adhesion energy decreases monotonically for the bonded wafer pairs. The likely cause of this is a decrease in the plastic deformation of the polymeric glue. The critical adhesion energy, G_c may be partitioned into the energy used to break atomic bonds, G_{tip}, and the energy dissipated plastically in the glue material, $G_{plastic}$ [72,75-77]. Deformation energy by the residual stress, $G_{residual}$ can be also considered as a part of critical adhesion energy although as a fraction of the total adhesion energy, it is not large [76,106-107].

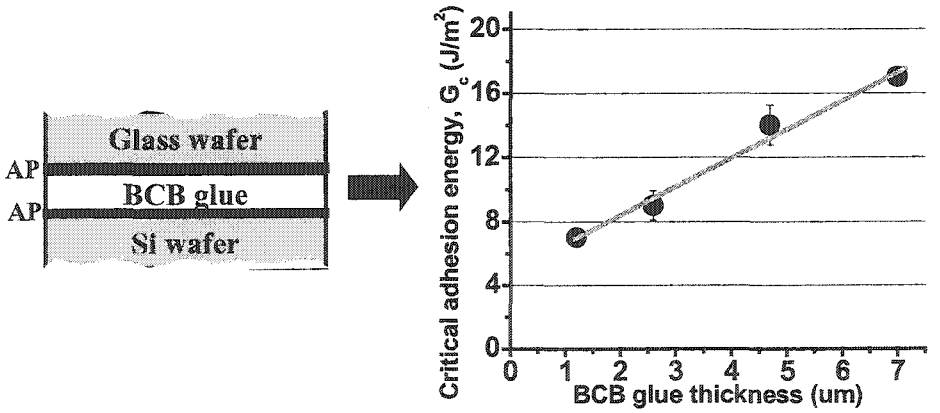


Figure 5.7: Critical adhesion energy dependence on BCB thickness. BCB is sandwiched by one silicon wafer and one glass wafer.

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In an amorphous polymer such as BCB, the phenomenon of "crazing" also occurs before breaking of atomic bonds and properly belongs to $G_{plastic}$ [77,93,108]. Crazing is the mode of plastic deformation in which very localized voids are created, bridged by bundles of polymer fibers called "fabrils". Although these fabrils are quite strong, the overall density of these crazed regions is significantly lower than the uncrazed regions, leading to concentrations of stress and, ultimately, to the rupture of the fabrils [108]. A schematic of craze micromorphology is shown in Figure 5.8.

Crazing becomes important when the film is under tensile stress (both σ_1 and σ_2 greater than zero). This is shown graphically in Figure 5.9. The reduced ductility accompanying craze formation results in a decreased toughness of the BCB layer than if it were to deform solely through shear yielding. However, the localized plastic deformation accompanying crazing is significant and gives a higher toughness than that of materials such as silicate glasses, which fracture prior to even local plastic deformation [77]. Thus, crazing leads to an increase in $G_{plastic}$ and hence an increase in G_c [93].

Figure 5.10 shows a schematic depicting the dependence of critical adhesion energy on structures that consist of ductile and elastic materials which exhibit crazing of a glue layer. When these stacked layers are compared with those of the 3D IC structures pursued

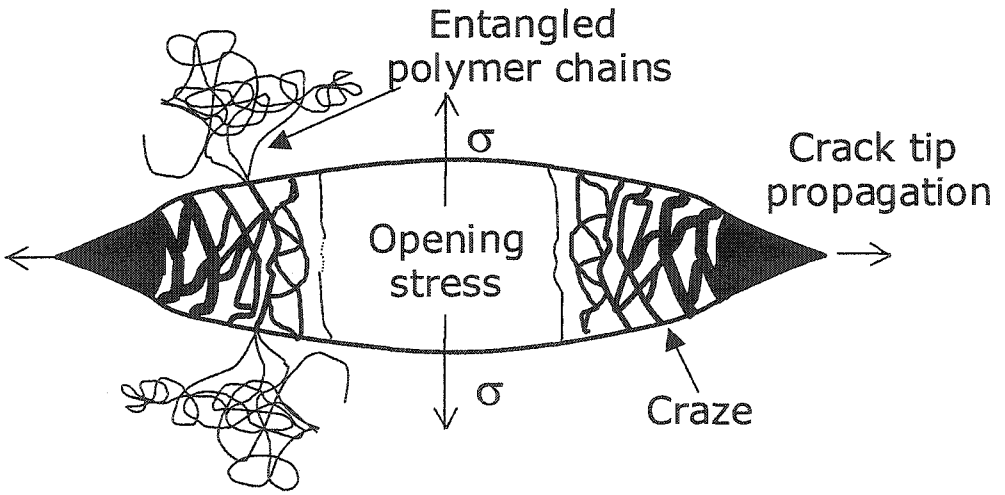


Figure 5.8: The molecular morphology in a craze. The molecules are heavily aligned in the form of fabrils (the dark lines) in the craze. A craze also contains voids between the fabrils. The voided areas assume the characteristics of a crack as the craze spreads laterally. Figure adapted from [108].

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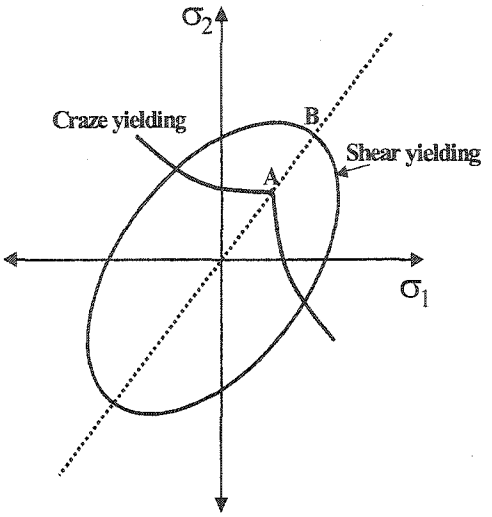


Figure 5.9: The biaxial loading yield loci for shear yielding and crazing. Crazing is important in quadrant I (σ_1, $\sigma_2 > 0$). Adapted from [108].

at RPI, BCB acts as the ductile material, and oxide buffer layer and glass and/or silicon wafers fill the role of the elastic materials.

The critical adhesion energy may be thought of as a sum of the breaking energy of atomic bonds and plastic dissipation energy in this situation [72,74-76,93]. It is believed that the contribution of deformation energy due to residual stress to critical adhesion energy is quite low [72,76]. To evaluate the size of the contribution of deformation energy on the critical adhesion energy, the deformation energy obtained by calculating strain energy in pure beam bending consisting of composite materials is compared with

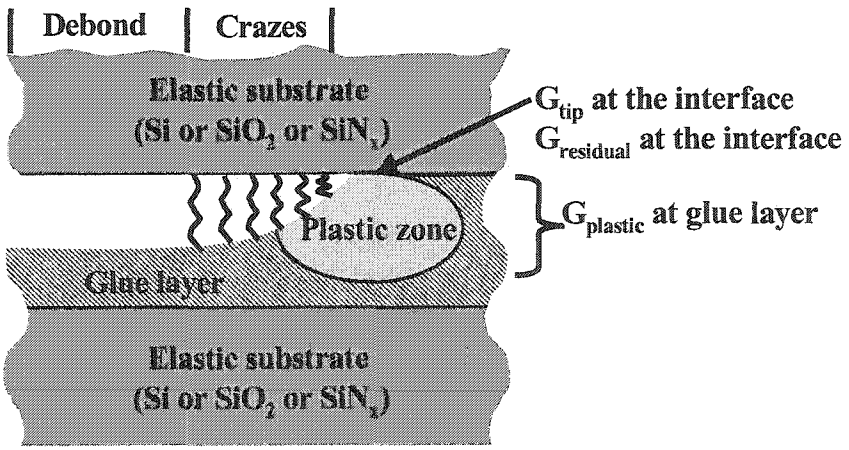


Figure 5.10: Schematic depicting critical adhesion energy dependence on structure consisting of ductile and elastic materials.

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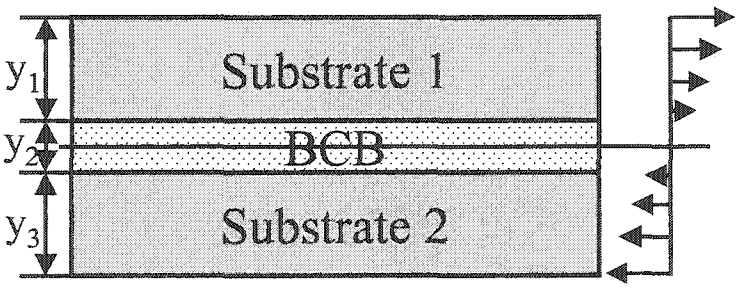


Figure 5.11: The geometrical configuration of beam specimen consisting of two elastic substrates and a BCB layer.

critical adhesion energy [78,93,106,109]. Figure 5.11 shows the geometrical configuration of beam specimen consisting of two elastic substrates and a BCB layer [93,109]. The expression for the elastic strain energy, $G_{residual}$ in a composite beam is as follows:

$$\begin{aligned} G_{residual} &= \int_{(y_2/2+y_3)}^{-y_2/2} \frac{\sigma_3^2}{2E_3}dy + \int_{y_2/2}^{y_2/2} \frac{\sigma_2^2}{2E_2}dy + \int_{y_2/2}^{(y_2/2+y_1)} \frac{\sigma_1^2}{2E_1}dy \\ &= \int_{(y_2/2+y_3)}^{-y_2/2} \frac{1}{2E_3}\left(-\frac{E_3M_3y}{(EI)^*}\right)dy + \int_{y_2/2}^{y_2/2} \frac{1}{2E_2}\left(-\frac{E_2M_2y}{(EI)^*}\right)dy \\ &+ \int_{y_2/2}^{(y_2/2+y_1)} \frac{1}{2E_1}\left(-\frac{E_1M_1y}{(EI)^*}\right)dy \end{aligned} \quad (5.1)$$

where σ_i is stress occurring in the BCB layer and the two substrates, M_i and E_i are the bending moment and Young's modulus of each component respectively, y_i is thickness of each component and $(EI)^*$ is defined as the integral value in the middle of the composite material [109]. For small deflections, the bending moment is expressed as a function of the radius of curvature term.

$$M_i = \frac{(EI)^*}{\rho} \quad i = 1,2,3 \quad (5.2)$$

where ρ is the radius of curvature. When Equation 5.2 is substituted into Equation 5.1, deformation energy is given by the following equation.

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$$
\begin{aligned}
G_{residual} &= \int_{(y_2/2+y_3)}^{y_2/2} \frac{E_3}{2\rho^2}\cdot y^2\cdot dy + \int_{y_2/2}^{y_2/2} \frac{E_2}{2\rho^2}\cdot y^2\, dy + \int_{y_2/2}^{(y_2/2+y_1)} \frac{E_1}{2\rho^2}\cdot y^2\, dy \\
&= \frac{E_3}{6\rho^2}\left[\left(\frac{y_2}{2}+y_3\right)^3-\left(\frac{y_2}{2}\right)^3\right]+\frac{E_2}{6\rho^2}\left[\left(\frac{y_2}{2}\right)^3+\left(\frac{y_2}{2}\right)^3\right] \\
&+\frac{E_1}{6\rho^2}\left[\left(\frac{y_2}{2}+y_1\right)^3-\left(\frac{y_2}{2}\right)^3\right] \\
&= \frac{E_3}{3\rho^2}\left[\left(\frac{y_2}{2}+y_3\right)^3-\left(\frac{y_2}{2}\right)^3\right]+\frac{E_2}{3\rho^2}\left(\frac{y_2}{2}\right)^3
\end{aligned}
\tag{5.3}
$$

When BCB is sandwiched with two silicon wafers, BCB is component 2 and two silicon wafers are components 1 and 3. The radius of curvature of BCB on silicon wafer obtained from the wafer curvature method described in Section 3.3.2 is about 27 m, y_1 and y_3 are 730 μm, y_2 is 2.6 μm. E_1 and E_3 (Young's modulus of silicon) are 131 GPa, E_2 (Young's modulus of BCB) is 2.9 Gpa [62-63]. As a result, the calculated $G_{residual}$ value is less than 0.5 J/m^2 and the measured critical adhesion energy, G_c under the same beam specimen geometry is 30 J/m^2. $G_{residual}$ value is much smaller than G_c. Thus, $G_{residual}$ can be neglected for these types of structures without significant error.

Because of this independence of the critical adhesion energy from deformation energy contributions, we may express G_c as a sum of the breaking energy of atomic bonds and plastic dissipation energy in the following manner [72,74-76,93].

$$G_c = G_{tip} + G_{plastic} = G_{tip}\,(1+ G_{plastic} / G_{tip}) \tag{5.4}$$

It is known that plastic dissipation energy is affected by the BCB thickness, *t*, and by the breaking energy of atomic bonds, G_{tip} [72,76].

$$G_{plastic} = f\,(G_{tip}, t) \tag{5.5}$$

Since this plastic dissipation energy is proportional to the plastic zone height of the glue and the plastic zone height is proportional to the BCB thickness within this BCB thickness range, BCB thickness affects the critical adhesion energy through the plastic dissipation energy. The effect of BCB thickness on plastic zone range is determined by the chemical structure of the relevant material [110].

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In bonded wafer pairs consisting of the glue layer sandwiched between two silicon wafers with 1 μm PECVD oxide layer, the relation between critical adhesion energy and BCB thickness is expressed as

$$G_c(J/m^2) = 18 + 5.5 \cdot t \approx 18(1 + 0.3 \cdot t) \quad 0.4\mu m \le t \le 2.6\mu m \tag{5.6}$$

which is obtained from Figure 5.5. In bonded wafer pairs consisting of the glue layer sandwiched between one glass wafer and one silicon wafer, the relation between critical adhesion energy and BCB thickness is expressed as

$$G_c(J/m^2) = 5 + 1.7 \cdot t \approx 5(1 + 0.3 \cdot t) \quad 1.3\mu m \le t \le 7\mu m \tag{5.7}$$

which is obtained from Figure 5.7. In both cases, the mean critical adhesion energy is linearly proportional to BCB thickness. When Equation 5.4 is compared with Equations 5.6 and 5.7, there are several points to be considered. The first is the analogy between the equations. $\frac{G_{plastic}}{G_{tip}}$ of Equation 5.4 corresponds to 0.3t of Equations 5.6 and 5.7. This correspondence is expressed as

$$G_{plastic} \approx 0.3 \cdot G_{tip} \cdot t \quad 0.4\mu m \le t \le 7\mu m \tag{5.8}$$

While such a linear relationship is less apparent in Figure 5.6, with only two data points, a similar fitting approach yields

$$G_c(J/m^2) \approx 22(1 + 0.3 \cdot t) \quad 0.6\mu m \le t \le 2.6\mu m \tag{5.9}$$

When Equation 5.9 is combined with Equations 5.6 and 5.7 using the critical adhesion energy formulation of Equation 5.4, the values given in Table 5.3 are obtained.

The different values of G_{tip} and $G_{plastic}$ indicate the critical adhesion energy dependence on the material stack materials, which is discussed further in Section 5.4. From Equation 5.8, the plastic dissipation energy is represented as a function of bond breaking energy and BCB thickness. This result corresponds to Equation 5.5 and is in good agreement with results published by Hutchinson and Evans [74] and Kook and

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Dauskardt [76]. The second thing to notice about Equations 5.5 and 5.8 is the quantitative relationship between plastic dissipation energy, $G_{plastic}$, and breaking energy of atomic bonds, G_{tip}. The G_{tip} is a typical energy in a relevant interface and depends on interfacial chemistry and surface morphology. However, these surface properties also affect the plastic energy of ductile material such as BCB. Based on Equation 5.8, critical adhesion energy as well as plastic dissipation energy in different glue thicknesses can be estimated.

Table 5.3: Relationship between G_{tip} and $G_{plastic}$ in different bonded interfaces

Bonded interfaces	G_{tip} (J/m^2)	$G_{plastic}$ (J/m^2) with t in μm
PECVD oxide and BCB (Figure 5.5)	18	5.4 t
Thermal oxide and BCB (Figure 5.6)	21	6.6 t
Glass and BCB (Figure 5.7)	5	1.5 t

5.4. Substrate Effects

BCB may be used to glue different materials, depending upon the desired application. For optical inspection of wafer pairs bonded for screening glues, the glue is used to bond glass substrates. In the 3D IC via chain test vehicle, the BCB is sandwiched between two silicon wafers covered with 1 μm PECVD oxide layers. For double bonding/thinning processes used to inspect bonding and thinning integrities, the BCB is adjacent to 2 μm or 0.3 μm thermal oxide layers on silicon wafers. In other applications, glue is in contact with native oxide [75], silicon nitride [64] and/or metal [111-112]. The bond strength values are expected to be different for each case, and the differences can be used to judge the compatibility with BEOL processes.

Since BCB is stacked with different oxide layers in research focusing on RPI's 3D technology platform, the effect of different oxide types on bond strength needs to be evaluated. Native oxide, PECVD silicon oxide, thermal oxide and glass are the oxide layers considered here. The bond strengths for the different oxide types are shown in Table 5.2.

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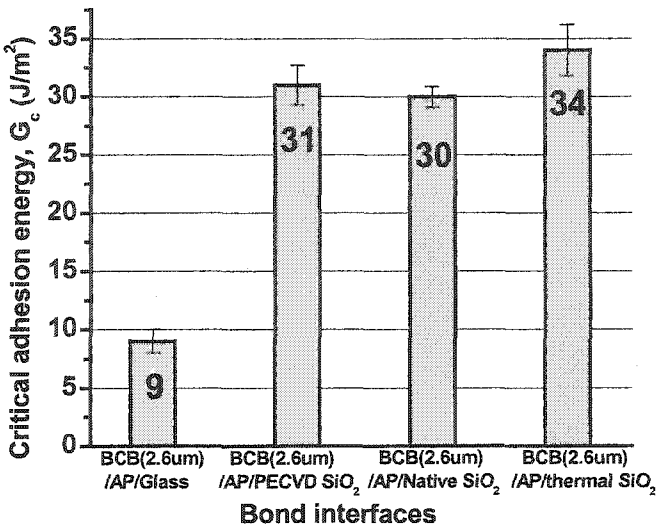


Figure 5.12: Measured critical adhesion energies for various types of oxide layers.

Figure 5.12 represents measured critical adhesion energies for different types of oxide layers (samples 1, 4, 6, and 9 in Table 5.2). In all cases, Dow AP3000 is used as adhesion promoter, and the BCB thickness is 2.6 μm. The thickness of native oxide is 1.4 nm, that of PECVD silicon oxide is 1 μm, and that of thermal oxide is 2 μm. The glass wafer is approximately 730 μm thick. Since these materials are elastic, the difference in oxide thickness should not affect the bond strength (no plastic dissipation).

The bond strength at the interface between thermal oxide and BCB is the highest and that at the interface between a glass wafer and BCB is the lowest. This difference in bond strength, G_c, is caused by different breaking energy of atomic bonds, G_{tip}, of the BCB stack materials. The difference in G_{tip} results from the different surface chemical compositions and surface morphologies [76]. Plastic dissipation energy, $G_{plastic}$, another key component of bond strength, also depends on G_{tip} and BCB thickness as described in Equation 5.8 ($G_{plastic} \approx 0.3 \cdot G_{tip} \cdot t$). Since the bonded wafer pairs mentioned above have the same glue thickness, bond strength mostly relies on the breaking energy of atomic bonds. In these material stacks, the glass substrate is a PG&O 1737 aluminosilicate wafer, and Table 5.4 shows its chemical composition [113]. Both the bulk and surface of the glass wafer mainly consist of SiO_2 (69 %) and Al_2O_3 (11.5 %), while the surfaces of oxide coated silicon substrates mostly consist of SiO_2. The two kinds of wafers are bonded with AP 3000 adhesion promoter.

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Table 5.4: Chemical components of PG&O 1737 glass wafer [113]

Components	Mole fraction (%)
SiO_2	69
Al_2O_3	11.5
CaO	7.3
B_2O_3	5
BaO	4.4
MgO	1.4
SrO	1.2
As_2O_3	0.2

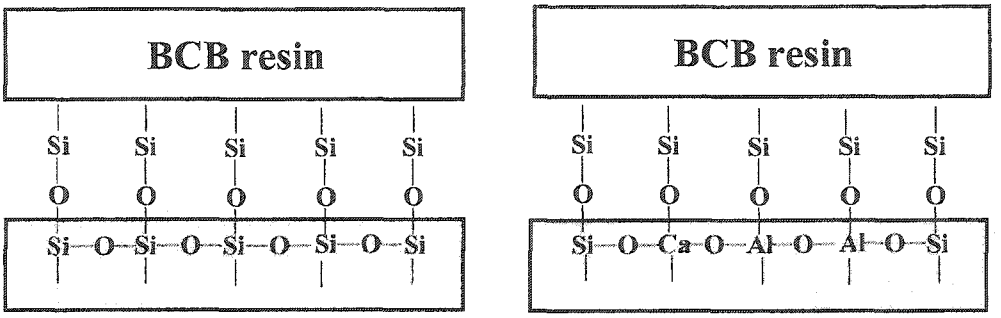
Table 5.5: Bond strength of various atomic pairs found on a glass wafer [114]

Molecule	Bond strength (kJ/mol)
Si-O	800
Al-O	511
B-O	808
Ca-O	402
Ba-O	561
Mg-O	363
As-O	481

As shown in Figure 5.3, silane-based molecules of the adhesion promoter react with dangling bonds on the surface of each wafer. In bonded wafer pairs that include a glass wafer, the silane-based molecules react with different types of dangling bonds to form Si-O-Si, Al-O-Si, B-O-Si, and Ca-O-Si, etc. [113]. In bonded wafer pairs that include an oxide covered silicon wafer, the molecules react with silanol dangling bonds, Si-OH to form siloxane, Si-O-Si, bonds. Table 5.5 reports bond strengths for various elemental pairs. Figure 5.13 shows anticipated bond structure between a glass wafer and adhesion promoter, and between an oxide covered silicon wafer and adhesion promoter [114].

The bond strength between oxide covered wafer and adhesion promoter should be higher than that between a glass wafer and adhesion promoter due to the high bond strength of Si-O. The bond-breaking energy, G_{tip}, between an oxide covered wafer and adhesion promoter is far higher than that between a glass wafer and adhesion promoter. Hence, the bond strength, G_c, of wafers bonded between oxide deposited silicon wafer and BCB is higher than that bonded between glass wafer and BCB because G_c strongly depends on G_{tip}.

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(a) Oxide deposited Silicon wafer

(b) Glass wafer

Figure 5.13: Anticipated bond structure in between glass wafer and adhesion promoter and in between oxide deposited silicon wafer and adhesion promoter.

The bond breaking energy G_{tip} values at the interfaces between oxide deposited silicon wafer and BCB and between glass wafer and BCB can be qualitatively evaluated as functions of bond density (number of polymer bonds between adhesion promoter and BCB neighboring material per unit area) and BCB chain length and the extent of BCB chain entanglement [106,115-116]. The chemical interactions to determine bond density occur at the interface between reactive functional groups of adhesion promoter, triacetoxysilane and the dangling bond groups of BCB neighboring material (*i.e.*, silicon dioxide or glass). Before explaining the adhesive failure occurring at both relevant interfaces, the general failure mechanism is described at Figure 5.14.

When lengths of BCB chains are short (see Figure 5.14a), no effective entanglements can be formed between BCB chains, and adhesion failure occurs at the interface between two ends groups of adhesion promoter and BCB-adjacent material. This failure is caused by the scissions of bond groups at the interface (chain pull out effect) [115]. When lengths of BCB chains are a bit longer, as shown in Figure 5.14b, the interface is connected with physical entanglement between BCB resins as well as chemical interactions between two ends groups of adhesion promoter and BCB-adjacent material. Each BCB resin is entangled and the maximum bond density achievable is similar to that of Figure 5.14a.

For bond failure, scission of the interfacial chains must occur. However, due to the tightness of entangled BCB chain, the interfacial chains are not easily pulled out, and chain scission occurs only with difficulty.

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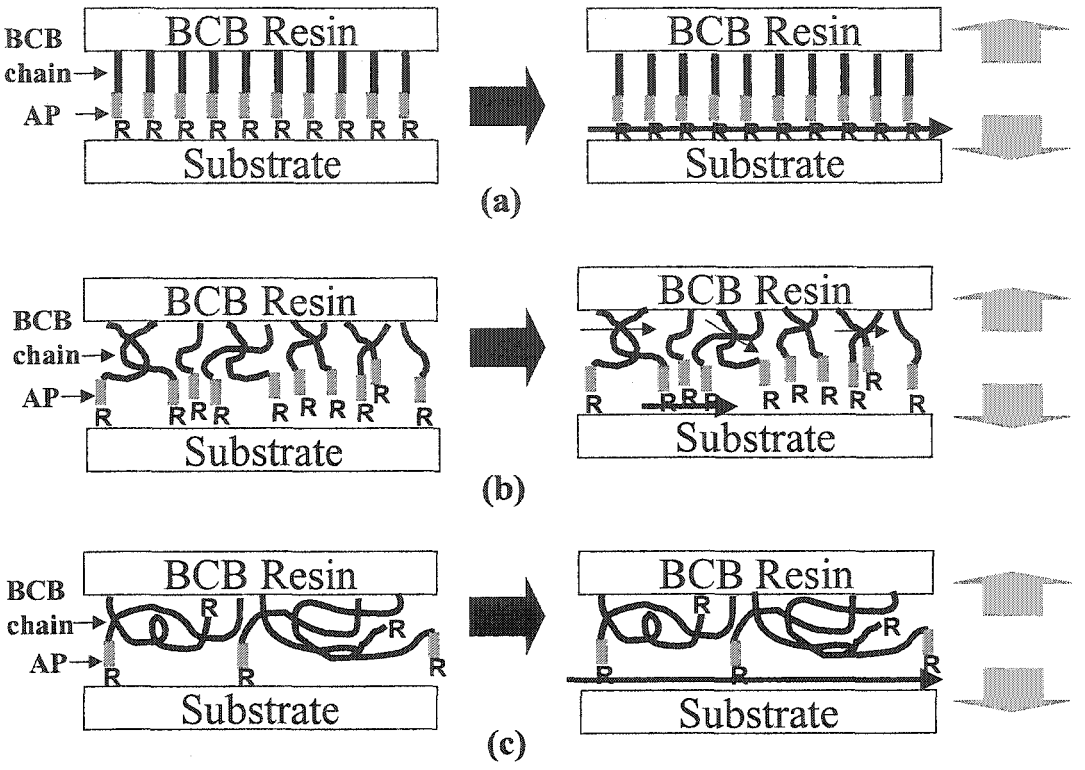


Figure 5.14: General failure mechanism at the interface between BCB and substrate: (a) For short BCB chain, no effective entanglements are formed and chain pull-out effect occurring at the interface between adhesion promoter and substrate is dominant failure mode. (b) For long BCB chain, the interface is connected with entanglement between BCB as well as chemical interactions at the interface. Each BCB resin is entangled and the maximum bond density achievable is similar to that of (a). The scission of the interfacial chains should occur for bond failure. However, due to entangled BCB chain, the interfacial chains are not pulled out, and chain scission does not occur well. (c) For very long BCB chain, although each BCB resin is well entangled, the maximum bond density achievable (number of chemical bonds at the interface) is very low and such an interface fails easily by scission of bond groups at the interface [116].

Hence, G_{tip} for these longer chained structures is much higher than that for the short-chained structures of Figure 5.14a. When lengths of BCB chains are yet longer, a shown in Figure 5.14c, even though each BCB resin is well entangled, the maximum bond density achievable is very low and such an interface fails easily by scission of bond groups at the interface. Consequently, G_{tip} is lower than for the structures of Figures 5.14a and 5.14b [106,116].

The largest values of G_{tip} are generally observed at intermediate chain lengths (such as shown in Figure 5.14b) where effective entanglement can be formed and a high bond

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density can be achieved. Under these conditions, the interface fails initially due to the formation of crazes at the interface and the subsequent breakdown of these crazes. As bond density increases, the mechanism of interface failure undergoes a transition from scission of the bridging chains before craze formation to a mechanism where crazing occurs and is followed by craze failure. The maximum bond density achievable is generally observed to decrease linearly with increasing polymer chain length, on the other hand, the maximum chain entanglement is observed to increase linearly with increasing the polymer chain length. The maximum G_{tip} is obtained at the crossing point of these two dependencies. Figure 5.15 shows the relationship among G_{tip}, polymer chain length, polymer bond density and the extent of physical entanglement of BCB chains [116].

It is believed that the extent of physical entanglement of BCB chains and BCB chain length at the interface between oxide deposited silicon wafer and BCB are the same as those at the interface between a glass wafer and BCB. However, polymer bond density is different in both interfaces due to difference in the chemical components between oxide layer and glass. Based on the data described in Figure 5.13 and Tables 5.4 and 5.5, the relationships between G_{tip} and bond density at the interfaces between oxide covered silicon wafer and BCB adhesion promoter and between glass wafer and BCB adhesion promoter are evaluated in the following expressions:

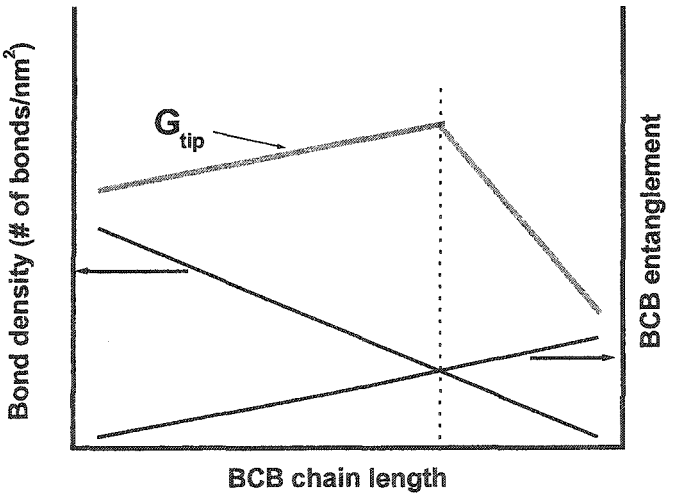


Figure 5.15: The relationship among G_{tip}, polymer chain length, polymer bond density and the extent of physical entanglement of BCB chains [116].

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Expected G_{tip} at the interface between oxide covered silicon wafer and BCB adhesion promoter (chemical compositions at the interface: Si-O-Si bond structure of 100 %):

$$800(\text{Si}-\text{O bonds})\frac{\text{kJ}}{\text{mol}}\cdot\frac{\text{mol}}{6.023\cdot10^{23}\text{atoms}}\cdot\frac{\text{X atoms}}{(1\text{nm})^2}=1.4\cdot\text{X}\cdot\frac{\text{J}}{\text{m}^2} \qquad (5.10)$$

Expected G_{tip} at the interface between glass wafer and BCB adhesion promoter (chemical compositions at the interface: Si-O-Si bond structure of 69 %, Al-O-Si bond structure of 11.5 etc):

$$\begin{aligned}&0.69\cdot800(\text{Si}-\text{O bonds})\frac{\text{kJ}}{\text{mol}}\cdot\frac{\text{mol}}{6.023\cdot10^{23}\text{atoms}}\cdot\frac{\text{X atoms}}{(1\text{nm})^2}+\\&0.115\cdot511(\text{Al}-\text{O bonds})\frac{\text{kJ}}{\text{mol}}\cdot\frac{\text{mol}}{6.023\cdot10^{23}\text{atoms}}\cdot\frac{\text{X}_1\text{ atoms}}{(1\text{nm})^2}+\\&+\text{etc.}\approx0.9\cdot\text{X}+0.1\cdot\text{X}_1\frac{\text{J}}{\text{m}^2}\end{aligned} \qquad (5.11)$$

Based on the results in Equations 5.10 and 5.11, the relationship between G_{tip} and bond density of BCB at the interfaces between oxide deposited silicon wafer and BCB and between glass wafer and BCB is expressed in Figure 5.16. At the interface between oxide deposited silicon wafer and BCB, an interfacial bond density of 13 bonds/nm^2 is required to obtaining the G_{tip} of 18 J/m^2 reported in Figure 5.5 and Equation 5.3. On the other hand, at the interface between glass wafer and BCB, a bond density of 5-6 bonds/nm^2 is required to obtain the G_{tip} of 5 J/m^2 as reported in Figure 5.7 and Equation 5.4.

The bond strengths observed for the three different types of oxide layers and BCB are comparable, because the bond-breaking energies, G_{tip} in different types of oxide layers are comparable. For example, G_{tip}, at the interface between thermal oxide and BCB (21 J/m^2) is higher than that at the interface between PECVD oxide and BCB (18 J/m^2) by ~10 %, as reported in Table 5.3. Bond strength at the interface between thermal oxide and BCB (34 J/m^2) is also higher than that at the interface between PECVD oxide and BCB (31 J/m^2) by ~10 %, as reported in Table 5.2.

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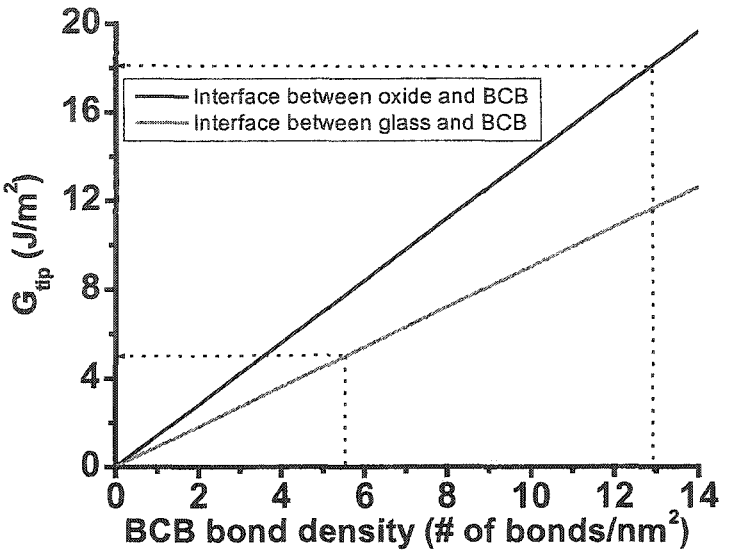


Figure 5.16: The relationship between G_{tip} and bond density of BCB at the interfaces between oxide deposited silicon wafer and BCB and between glass wafer and BCB [116].

5.5. Baseline Process Parameters

BCB is the baseline bonding glue due to reproducible, void-free bonding and high bond strength. Optical inspection and FTIR were also used to help select the baseline glue. Four-point bending has been used to quantify the bond strength and identify the weak interface.

The following is the baseline bonding process for optical inspection of bonding during glue screening. A 2.6 μm layer of BCB is sandwiched between one glass wafer and one silicon wafer. The CTE of the glass wafer used is well matched with that of silicon wafer. The critical adhesion energy and the weak interface are also determined. Load vs. displacement curves obtained during four-point bending experiments show Type 1 behavior in general. The mean critical adhesion energy of 9 J/m^2 is obtained as described in Table 5.2, and debonding occurs at the interface between the glass wafer and BCB. This baseline process has been established through these evaluations for bonding quality.

For 3D IC integration, BCB of 2.6 μm thickness is sandwiched between two silicon wafers covered with 1 μm PECVD oxide layers. After bonding, critical adhesion energy

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is measured, and the weak interface is identified to evaluate the bonding quality. Load vs. displacement curves show Type 1 behavior. The mean critical adhesion energy of 31 J/m^2 is obtained, as listed in Table 5.2. Debonding occurs at the interface between PECVD oxide layer and BCB.

For 3D applications, the BCB layer should be as thin as possible in order to reduce aspect ratios of vertical inter-wafer interconnect vias. However, bonding integrity may decrease when using thin glue layers, and adhesive failure may occur. To evaluate the possibility of adhesive failure when using thin BCB layers, experiments were done. In one experiment, the BCB thickness used to bond a glass wafer and a silicon wafer was decreased to 1.3 μm. In another experiment, the BCB thickness used to bond two silicon wafers was reduced to 0.4 μm. In both cases, load vs. displacement curves show Type 1 behavior, similar to the baseline processes. For glass-to-silicon wafer pairs bonded with 1.3 μm BCB, a critical adhesion energy of 7 J/m^2 is obtained, and the interface between the glass wafer and BCB is weakest. For two silicon-to-silicon wafer pairs bonded with 0.4 μm BCB, the critical adhesion energy is 13 J/m^2, and the weak interface is between the PECVD oxide layer and BCB. These critical adhesion energy values are still higher than that of fusion bonding and are attractive for 3D applications.

5.6. Summary

In summary, wafer bonding using BCB is evaluated quantitatively using four-point bending. To determine proper baseline-bonding parameters for 3D applications, the following chemical and geometrical effects on critical adhesion energy have been investigated: Using of an adhesion promoter, BCB layer thickness, and different substrate materials and structures on the wafer(s).

Adhesion promoter increases the critical adhesion energy. When the adhesion promoter is used, bond strength increases to approximately a factor of two for both the thick BCB and thin BCB wafer sets. The "baseline BCB" wafer set, consisted of 2.6 μm of BCB in a double layer and the "thin BCB" wafer set consisted of 0.4 μm of BCB in a single layer, both between silicon wafers covered with PECVD oxide. Using 2.6 μm of BCB, an adhesion energy of 31 J/m^2 is obtained with the adhesion promoter, and 13 J/m^2

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without the adhesion promoter. Using 0.4 μm of BCB, an adhesion energy of 19 J/m^2 is obtained with the adhesion promoter and 10 J/m^2 without the adhesion promoter.

BCB thickness affects the bond strength at the glue interface. BCB thickness of 0.4 μm led to a measured critical adhesion energy of 19 J/m^2 for bonded wafers coated with PECVD oxide, significantly less than 31 J/m^2 obtained with 2.6 μm BCB. Even with as little as 0.4 μm BCB, the critical adhesion energy is very attractive for 3D applications. The decrease in adhesion energy observed for thin BCB is apparently due to a decrease in plastic dissipation energy, because the plastic dissipation energy is proportional to BCB thickness as well as bond breaking energy. In both bonded wafer pairs that include a PECVD oxide deposited silicon wafer and a glass wafer, the critical adhesion energies are linearly proportional to BCB thickness within the pre-determined BCB thickness range. Based on these results, the relationship between plastic energy dissipation, $G_{plastic}$, and bond breaking energy, G_{tip}, and BCB thickness, t is observed to be $G_{plastic} \approx 0.3 \cdot G_{tip} \cdot t$ for t measured in micrometers.

Substrate material affects bond strength. Bonding using a BCB thickness of 2.6 μm leads to a critical adhesion energy of 31 J/m^2 for silicon wafers that are coated with PECVD oxide, 34 J/m^2 for silicon wafers that are coated with thermal oxide, 30 J/m^2 for silicon wafers that are coated with native oxide, and 9 J/m^2 for bonds between silicon and glass wafers. The large difference in bond strengths of bonded wafer pair between a glass wafer and a silicon wafer coated with oxide layer using 2.6 μm of BCB thickness, and that between two silicon wafers coated with oxide layers using 2.6 μm of BCB thickness mainly results from the difference in bond breaking energy, G_{tip}, of in these two material stacks. The difference in the bond breaking energy is caused by the different surface chemical compositions and their bond densities. Plastic dissipation energy including crazing, $G_{plastic}$, another key component of bond strength, also depends on G_{tip} and BCB thickness as a form of $G_{plastic} \approx 0.3 \cdot G_{tip} \cdot t$. Since the bonded wafer pairs mentioned above have the same glue thickness, bond strength mostly relies on the breaking energy of atomic bonds.

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CHAPTER 6
THERMAL CYCLING EVALUATION OF BOND STRENGTH AND RESIDUAL STRESS

6.1. Overview

Within the 3D IC integration scheme pursued at RPI, the bonded wafer stack may undergo thermal excursions after the initial BCB curing step. These excursions may occur during such processes as etching of inter-wafer vias and deposition of copper used to form the inter-wafer interconnections. Copper damascene processing may involve deposition temperatures up to 350 °C and annealing temperatures up to 400 °C, although lower temperature processes are more common [117-120]. Another, perhaps more extreme, thermal excursion to be considered is that experienced by the bonded wafer stack during curing of subsequent BCB layers when adding another wafer to the stack. During the bonding of a wafer to an existing wafer stack, BCB used in the earlier bonds goes through the thermal excursions associated with the curing cycle.

It is important to determine how such thermal cycling of cured BCB layers can change the BCB layer. Some possible ways in which the layer might be affected during thermal cycling include an increase in bond strength due to stress relaxation, adhesive failure at the interface between BCB and PECVD oxide, and cohesive failure within the BCB layer. Although BCB has been used in microelectronic applications, the effects of high-temperature (over 350 °C) thermal cycling on bond strength/residual stresses at bonding interfaces and on the physical stability of BCB are not well understood. Most published studies consider the effects of thermal cycling of BCB in a low temperature range (-55 °C~150 °C) [121-122], and the bond strengths at the interface between BCB and wafers has mostly been evaluated qualitatively using stud pull and tape tests [102,122]. Hence, evaluations of both bonding integrity at the interfaces of the stacked layers and stability of the BCB layer during the specified thermal cycling schemes are important. The results obtained through these evaluations allow us to evaluate criteria on the reliability of the bonded wafer stacks and to establish a thermal cycling process that yields stable BCB layers without degrading already deposited BCB layers.

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The key goals of the research discussed in this chapter are; a) to quantify changes in bond strength at the interfaces of the bonded wafer stacks that result from thermal cycling, and b) to measure residual stresses in stacked layers consisting of BCB and PECVD oxide on silicon wafers. Thermal cycling tests performed in the temperature range of 350 to 450 °C in nitrogen ambient are used to evaluate the thermal stability of the BCB. The focus of this part of the work is on bonding of wafers covered by PECVD oxide layers, which represent wafers processed through MLM or BEOL. The thermal cycling process may affect the mechanical stability of stacked layers consisting of BCB and PECVD oxide. For example, stability may increase due to residual stress relaxation at the interface between the BCB and wafer, or it may decrease due to thermal fatigue. Based on these results, bond strength dependence on residual stress is determined.

In this research, bond strengths are determined using four-point bending and residual stresses are determined using wafer curvature, as described in Sections 2.6 and 3.3.2, respectively. Stress analyses of PECVD oxide layers using this wafer curvature method have been performed by Thurn and Cook [123], Chen *et al.* [124], Haque *et al.* [125], and Zhang *et al.* [126]. In this thesis, mainly the theory proposed by Thurn and Cook is used to understand stress release effect of PECVD oxide layer.

6.2. Experimental Procedures

Thermal cycling tests are performed with four different 200 mm wafers/wafer stacks:

1. Silicon wafer covered with 1 μm PECVD oxide
2. Silicon wafer coated with 3 μm BCB
3. Silicon wafer covered with 1 μm PECVD oxide followed by 3 μm BCB
4. A bonded wafer pair consisting of a 2.6 μm thick BCB layer sandwiched between two silicon wafers each covered with 1 μm PECVD oxide layer.

The PECVD oxide layers are deposited using SiH_4 and N_2O at 300 °C in a Plasmatherm 73 (Plasma-Therm Inc., Voorhees, NJ) with a chamber pressure of 0.9 Torr and radio frequency power of 25 W, using 200 mm silicon wafers. During deposition, the desirable reaction is

$$SiH_4 + 2N_2O \rightarrow SiO_2\,(s) + 2H_2 + 2N_2 \qquad (6.1)$$

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The thickness of PECVD oxide layers is measured using spectroscopic reflectometry and ellipsometry. The standard deviation of the measured thickness across the wafer is less than 5%.

For measurement of residual stress, 3 μm of BCB resin (Cyclotene 3022-45, Dow Chemical) is spin-cast in a FlexiFab^{TM} on AP3000 adhesion promoter (Dow Chemical). The BCB is applied to wafers (2) and (3) listed above after pre-cleaning with a solution of sulfuric acid and hydrogen peroxide (piranha clean) and after spin-dry cleaning. The spun-on BCB is baked at 170 °C for 2 min. and cooled for 5 min. in a nitrogen environment. The standard deviation of BCB thickness (measured using spectroscopic reflectometry and ellipsometry) is less than 1%. After baking, the curing process is performed in the EVG bonder using the same conditions that are used for the baseline bonding process, but without pressurization.

For four-point bending measurements, each (beam) specimen is prepared by cutting out a piece of the bonded wafer pair. The nominal dimensions of the specimen are 40 mm long, 4 mm wide, and 1.5 mm thick. The beam specimen is then mounted in the bending fixture, and the bending tests are conducted as described in Section 3.3.1.

Residual stress is determined by measuring the deformation of a substrate by a deposited film using: [92]

$$\sigma = \frac{E_s}{1-\nu_s}\frac{t_s^2}{6t_f}\left(\frac{1}{R}-\frac{1}{R_0}\right) \tag{6.2}$$

where E_s and ν_s are Young's modulus and Poisson's ratio for the substrate, t_s and t_f are the substrate and film thickness, and R and R_0 are the radii of curvature before film deposition (pure silicon wafer) and after film deposition, respectively. A KLA-Tencor^{TM} FLX-2320 system (Tencor Instruments, Mountain View, CA) is used for curvature measurements.

The thermal cycling tests are performed on pieces cut from the wafers and bonded wafer pairs. The pieces studied are rectangular shapes (nominal dimensions are 40 mm x 30 mm); the four rough edges of the rectangular shapes are polished mechanically. After thermal cycling, each rectangular shape is diced again into beam specimens, and four-point bending tests are performed.

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Several variables can be changed for thermal cycling tests. These include number of cycles, peak cycle temperature, nominal ramp rate, dwell time at the highest temperature, and the atmosphere during thermal cycling. Of these, the effects of the number of cycles and peak cycle temperature on bond strength and residual stress are investigated in this work, because they are often considered to be the key variables affecting the bond strength and residual stress [121-123]. One, five and ten thermal cycles (1-, 5- and 10-cycle) were chosen since preliminary experiments indicated that the residual stress and bond strength both reached a saturation point in less that 10 cycles. Peak cycle temperatures of 350, 400, and 450 °C were chosen after considering subsequent 3D IC processes (such as deep via etching and barrier metal/copper filling for vertical inter-wafer interconnect process) and thermal stability results of BCB described in the literature [63,121-122]. Also, it is reported that the glass transition temperature (T_g) of BCB after curing is above 350 °C [122,127].

A nitrogen atmosphere is used during the thermal cycling to prevent oxidation of BCB in all thermal cycling tests reported in this chapter. A ramp rate (both ramp up and cool down) of 25 °C/min was used with a dwell time of 20 min. at the peak temperature.

6.3. Bond Strength Dependence on Number of Thermal Cycles

Four-point bending tests were performed after 1, 5, and 10 thermal cycles. Figure 6.1 shows beam specimen configurations of Si/PECVD SiO_2/BCB/PECVD SiO_2/Si structure and represents the effect of number of thermal cycles on bond strength at the interface between PECVD oxide and BCB layers. A double layer BCB of 2.6 μm thickness is sandwiched between two silicon wafers with 1 μm of PECVD oxide.

A "first cycle effect" is observed, with the bond strength showing a substantial increase after the first thermal cycle and then remaining relatively unchanged thereafter, as seen by measurements in the fifth thermal cycle. Table 6.1 summarizes bond strength measurements for numbers of cycles and a peak temperature of 400 °C. In all four-point bending measurements, adhesive failure occurred at the interface between PECVD oxide and BCB layers. Load vs. displacement curves from four-point bending tests show "Type 2" pattern (linear elastic→load plateau→specimen breakage). It is believed that the presence of a tough interface in the sample may induce beam specimen breakage

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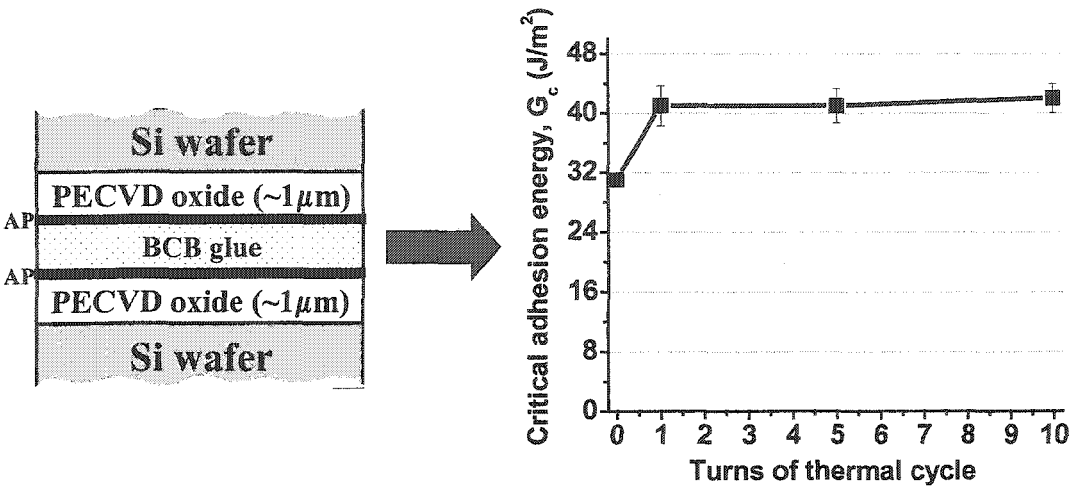


Figure 6.1: Beam specimen configurations and critical adhesion energy for 1, 5, and 10 thermal cycles at peak cycle temperature of 400 °C. BCB layer is sandwiched by PECVD oxide coated silicon wafers.

while at the load plateau (more than 35 J/m^2). The crack propagates along the interface initially and then stops extending due to the toughness of the interface. The beam specimen may then break because the crack propagation energy is diverted into breaking the specimen, as described in Section 3.1.1.3.

Residual stress at the interface between BCB and PECVD oxide of stacked layers consisting of PECVD oxide and BCB on a silicon wafer is first measured to evaluate the effect of residual stress on bond strength. The same deposition procedures are used for the PECVD oxide and BCB layer in this test structure as used for wafer bonding. Figure 6.2 shows the geometry of the stacked layers deposited on a silicon wafer, and

Table 6.1: Bond strength dependence of number of cycles at peak temperature of 400 °C for Si/PECVD SiO_2/AP/BCB /AP/PECVD SiO_2/Si (structure depicted in Figure 6.1)

Number of cycles	Load-plateau	n	Mean G_c (J/m^2)	S.D. (J/m^2)
0	Type 1	6	31	1.7
1	Type 2	4	41	2.7
5	Type 2	4	41	2.3
10	Type 2	4	42	2

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temperature dependence of residual stress of the stacked layers during the first and second thermal cycles with the peak temperature fixed at 400 °C. The BCB and PECVD oxide layers are overall in compressive stress, and the compressive stress is rapidly released during the first thermal cycle (first cycle effect). The stress trajectory during cycling shows plastic behavior from 300 °C to 400 °C (observation of stress hysteresis). However, during the second thermal cycle, stress hysteresis of the compressive stress on the layers was not observed.

This result is important in understanding the increase of bond strength at the interface between BCB and PECVD oxide layers after the first thermal cycle. The plastic behavior occurring at high temperatures (over 300 °C) during the first thermal cycle is compatible with the plastic behavior of PECVD oxide layer under similar conditions. The plastic behavior of PECVD oxide layers is discussed in Section 6.5. The bond strength mainly consists of the energy required to break atomic bonds, G_{tip}, and the plastic dissipation energy of the ductile polymeric glue, $G_{plastic}$. However, deformation energy due to residual stress, $G_{residual}$, can change the bond strength [110]. From Figures 6.2, which shows a large hysteresis in residual stress, it can be inferred that the bond strength increase after 1-cycle, shown in Figure 6.1, is at least partially caused by stress relaxation at the relevant interface ($G_{residual}$ contribution). Were G_{tip} and $G_{plastic}$ to change during further thermal cycling, bond strength at the relevant interface after a 5-cycle would have a different value from that after 1-cycle. However, this is not observed, with the bond strength measured after 5-cycle being the same as that measured after 1-cycle. This close

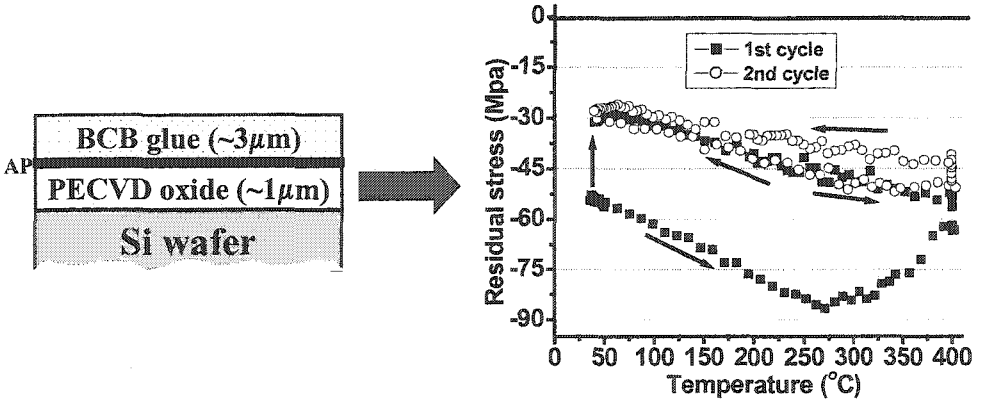


Figure 6.2: Geometry of stacked layers and temperature dependence of residual stress on the stacked layers after the first and second thermal cycling at peak temperature of 400 °C.

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tracking of the trend in bond strength with the trend in residual stress indicates a significant likelihood that the bond strength at the interface between BCB and its adjacent layer depends mainly on changes in $G_{residual}$ during thermal processing.

A first order model has been developed to describe the stress release at the interface between BCB and PECVD oxide layer of the stacked layer during the first thermal cycle and the small change in residual stress after the first thermal cycle. The force occurring at the interface between BCB and PECVD oxide layer is approximated by the sum of forces of from both the BCB and PECVD oxide layers as described in Equation 6.3 [128].

$$\sigma_{total}\, t_{total} = \sigma_{oxide}\, t_{oxide} + \sigma_{BCB}\, t_{BCB} \tag{6.3}$$

Here, σ_{oxide} and σ_{BCB} are residual stresses in the oxide and BCB layer respectively and σ_{total} is residual stress at the interface between BCB and PECVD oxide layer; t_{oxide} and t_{BCB} are thicknesses of the oxide and BCB layer respectively, and t_{total} is the total thickness of the stacked layer consisting of BCB and PECVD oxide layers. From Equation 6.3, the residual stress at the interface between BCB and PECVD oxide layer is related with that of the PECVD oxide layer and that of the BCB. Hence, the temperature dependence of residual stress of the PECVD oxide layer and the BCB layer should be examined individually to evaluate the temperature dependence of residual stress at the interface between BCB and PECVD oxide layer of stacked layers.

We made a test structure consisting of PECVD oxide layer on a silicon wafer. The configuration of this structure and the temperature dependence of residual stress of the oxide layer after a first and second thermal cycles are shown in Figure 6.3. For a peak cycle temperature of 400 °C, the compressive stress in the PECVD oxide layer is considerably released during the first thermal cycle. This stress relaxation is caused by the change in chemical composition by condensation reaction of silanol groups within PECVD oxide layer [123-124]. The change in chemical composition leads to densification of the chemical structure of the PECVD oxide layer. As seen in Figure 6.3, during the second cycle, little hysteresis in residual stress is observed, presumably because the condensation reaction in the oxide layer neared completion during the first cycle. This stress relaxation mechanism within the PECVD oxide layer is described in detail in Section 6.5.

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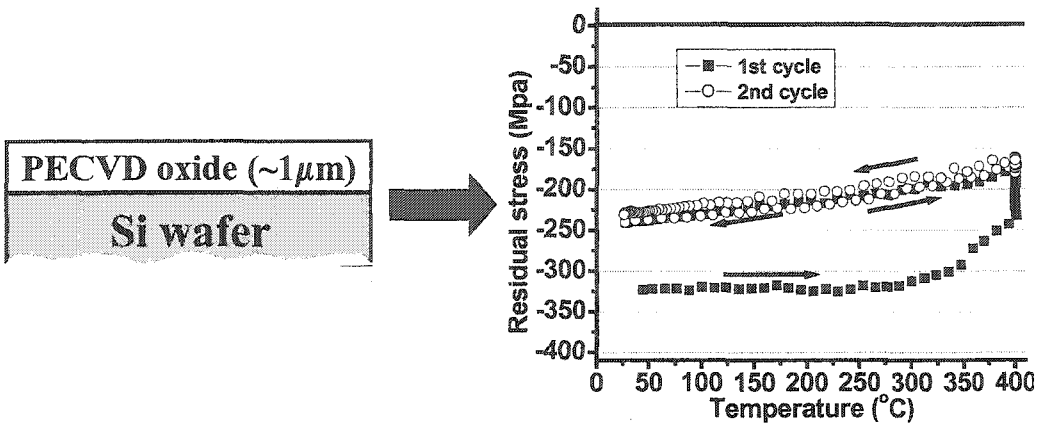


Figure 6.3: Geometry of PECVD oxide on silicon wafer and temperature dependence of residual stress on PECVD oxide on silicon wafer after the first and second thermal cycling at peak temperature of 400 °C.

Figure 6.4 shows the geometric configuration of BCB on a silicon wafer and the temperature dependence of residual stress during a first and second thermal cycle. Before thermal cycling, BCB is cured as in the baseline-bonding process (250 °C at 1 hr). For a peak cycle temperature of 400 °C, tensile stress in the BCB was exhibited during the thermal cycle. The residual tensile stress of BCB is thermal stress caused by the large CTE difference with between BCB and silicon. During the first heating cycle, BCB becomes plastic above ~300 °C, and the stress is relaxed. At the peak temperature of 400 °C, BCB is further cured (12 % of BCB monomers is not cured yet as addressed in Section 6.6) and the residual stress is reset to zero at the glass transition temperature

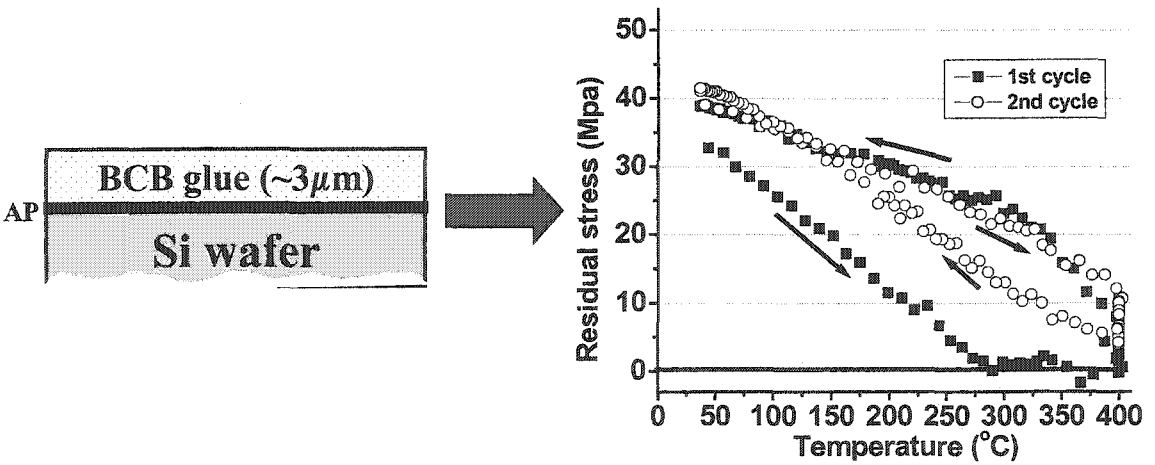


Figure 6.4: Geometry of BCB on silicon wafer and temperature dependence of residual stress on BCB on silicon wafer after the first and second thermal cycling at peak temperature of 400 °C.

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corresponding to the increased BCB cure. The stress then increases during the cooling process. During the second thermal cycling, changes in the residual stress are small, meaning that the BCB has been stabilized and further curing has slowed or stopped completely. Since the magnitude of residual stress change in BCB (tensile stress) is much smaller than that in a PECVD oxide layer (compressive stress), the residual stress at the interface between BCB and PECVD oxide layer is dominated by stress in the PECVD oxide layer and hence is in compression (see Equation 6.3).

In summary, residual stress existing at the interface between BCB and PECVD oxide layers of the stacked layers deposited on a silicon wafer is released during the first thermal cycle due to the stress relaxation within the PECVD oxide layer. Since the residual stress at the interface between BCB and PECVD oxide layers is released, deformation energy due to residual stress, $G_{residual}$, decreases and the total bond strength, G_c at the interface increases ("first cycle effect"). The plastic behavior of residual stress occurring at the interface between 300 °C and 400 °C is dominated by the residual stress within PECVD oxide that comes from structural changes caused by condensation reactions. After the first thermal cycle, the stress of PECVD oxide layer has stabilized and accordingly, total residual stress and bond strength at the interface between BCB and PECVD oxide layers is also stabilized.

6.4. Bond Strength Dependence on Peak Temperature

The effect of "peak temperature" on bond strength is evaluated using thermal cycle conditions similar to those in Section 6.3: nominal ramp rate (25 °C/min.), dwell time at the peak temperature (20 min.), and a nitrogen atmosphere. The variables considered are peak cycle temperature and number of thermal cycles. Peak temperatures of 350, 400, and 450 °C are used; and 1, 5, and 10 thermal cycles are used.

Beam specimens that consist of Si/PECVD SiO_2/BCB/PECVD SiO_2/Si are prepared to evaluate bond strength of the wafer pairs bonded under different thermal cycling conditions, with the baseline BCB thickness of 2.6 μm.

The effect of the peak temperature on bond strength is shown in Figure 6.5, and the bond strength dependences on the number of thermal cycles at peak temperatures of 350 °C and 450 °C are shown in Table 6.2 and Table 6.3, respectively (the comparable

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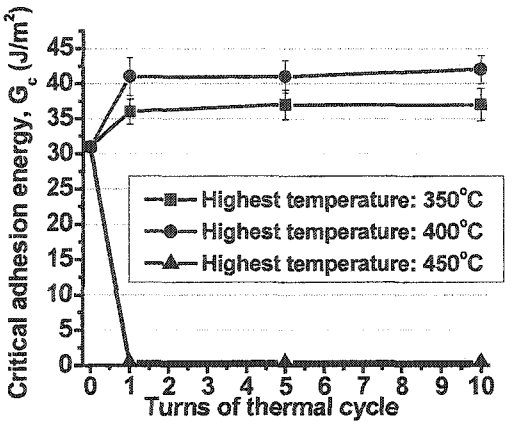


Figure 6.5: Critical adhesion energy in different peak cycle temperatures. Used number of thermal cycles is 1-, 5-, and 10-times at each peak temperature. BCB layer is sandwiched by PECVD oxide deposited silicon wafers.

table for the 400 °C peak temperature results is given as Table 6.1 in Section 6.3). In all evaluations performed for a peak temperature of 350 °C, adhesive failure occurs at the interface between PECVD oxide and BCB layers. During the four-point bending tests, load vs. displacement curves show "Type 2" patterns, as described in Table 6.2.

In thermal cycle tests performed with a peak temperature of 450 °C, bond strengths are very low (less than 0.5 J/m^2), irrespective of number of cycles, as described in Table 6.3. Cohesive failure of BCB is observed in these samples. Clearly 450 °C is beyond the acceptable range for thermal cycling of BCB.

In summary, several phenomena are observed through these bond strength evaluations:

Table 6.2: Bond strength dependence of number of cycles at peak temperature of 350 °C for Si/PECVD SiO_2/AP/BCB /AP/PECVD SiO_2/Si

Number of cycles	Load-plateau	n	Mean G_c (J/m^2)	S.D. (J/m^2)
1	Type 2	4	36	1.8
5	Type 2	4	37	2.1
10	Type 2	4	37	2.3

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Table 6.3: Bond strength dependence of number of cycles at peak temperature of 450 °C for Si/PECVD SiO_2/AP/BCB /AP/PECVD SiO_2/Si

Number of cycles	n	Mean G_c (J/m^2)
1	3	>0.5
5	3	>0.5
10	3	>0.5

1. When the peak cycle temperature is 350 or 400 °C, bond strength at the interface between BCB and PECVD oxide layers of a stacked structure consisting of PECVD oxide and BCB on a silicon wafer increases rapidly during the first thermal cycle. The bond strength is relatively unchanged in further cycling (five and ten thermal cycles).
2. The magnitude of the stable bond strength for a peak cycle temperature of 350 °C (35~37 J/m^2) is ~10% lower than that for a peak cycle temperature of 400 °C (41~42 J/m^2).
3. At the peak cycle temperature of 450 °C, bond strength is very low (less than 0.5 J/m^2). In thermal cycling performed at this temperature, de-cohesive failure within BCB occurs.

For peak temperatures not exhibiting cohesive failure (*i.e.*, 350 °C and 400 °C), the residual stress at the interface between BCB and PECVD oxide layers is measured to evaluate the effect of the residual stress on bond strength during thermal cycles. The first cycle effect is observed and caused by a decrease of $G_{residual}$, as described in Section 6.3.

Figure 6.6 shows the temperature dependence of residual stress in the PECVD oxide/BCB layers of a stack after the first and second thermal cycles, when the peak cycling temperature is 350 °C. Figure 6.2 of Section 6.3 shows the temperature dependence of residual stress for a peak temperature condition of 400 °C for a similar stack. In both cases, the observed compressive stress is released rapidly during the first thermal cycle.

Figure 6.7 shows the temperature dependence of residual stress after the first and second thermal cycle for a PECVD oxide layer on a silicon wafer for a peak cycle temperature of 350 °C. Figure 6.3 of Section 6.3 shows the temperature dependence of residual stress for a similar stack after the first and second thermal cycle for a peak

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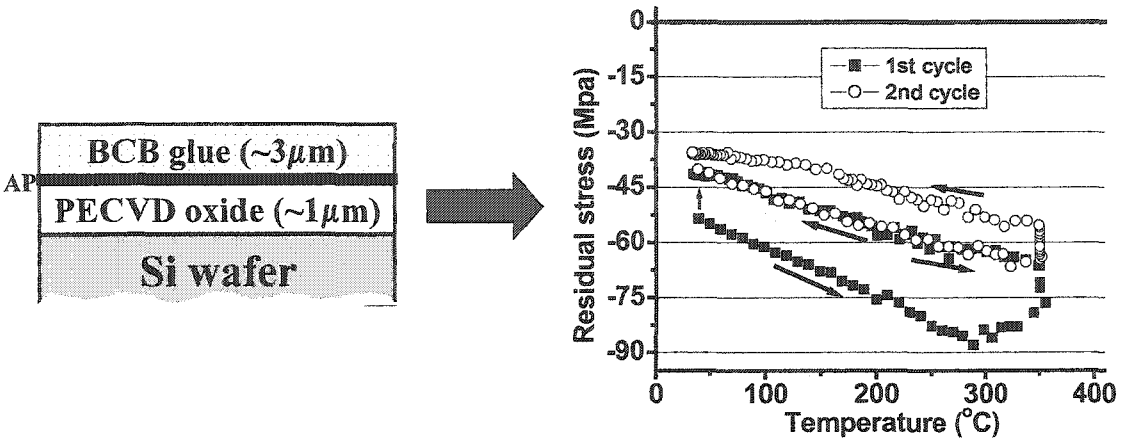


Figure 6.6: Geometry of stacked layers and temperature dependence of residual stress on the stacked layers after the first and second thermal cycling at peak temperature of 350 °C.

temperature is 400 °C (-320 MPa→-230 MPa). For a peak temperature of 350 °C, compressive stress in the PECVD oxide layer is released during the first thermal cycle (-320 MPa→-280 MPa). The magnitude of stress released at 400 °C peak temperature is about twice that released at 350 °C peak temperature. This difference can be attributed to increased condensation reaction produced in PECVD oxide layer at the higher peak temperature.

Figure 6.8 shows the temperature dependence of the residual stress for BCB on silicon after the first and second thermal cycles when the peak temperature is 350 °C. Before thermal cycling, BCB is cured using the baseline-bonding process. During the first heating cycle, BCB is in tension. As thermal cycle proceeds, changes in the residual

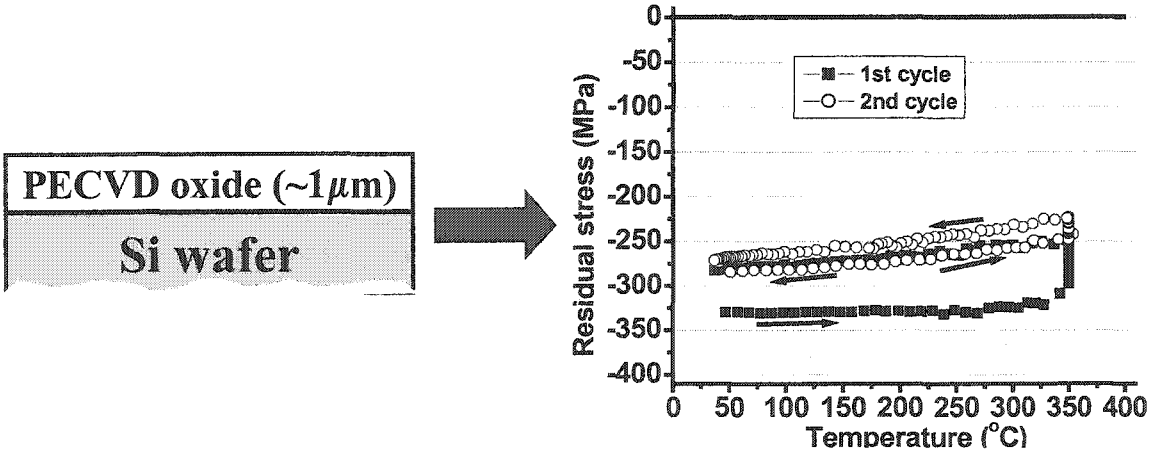


Figure 6.7: Geometry of PECVD oxide on silicon wafer and temperature dependence of residual stress on PECVD oxide on silicon wafer after the first and second thermal cycling at peak temperature of 350 °C.

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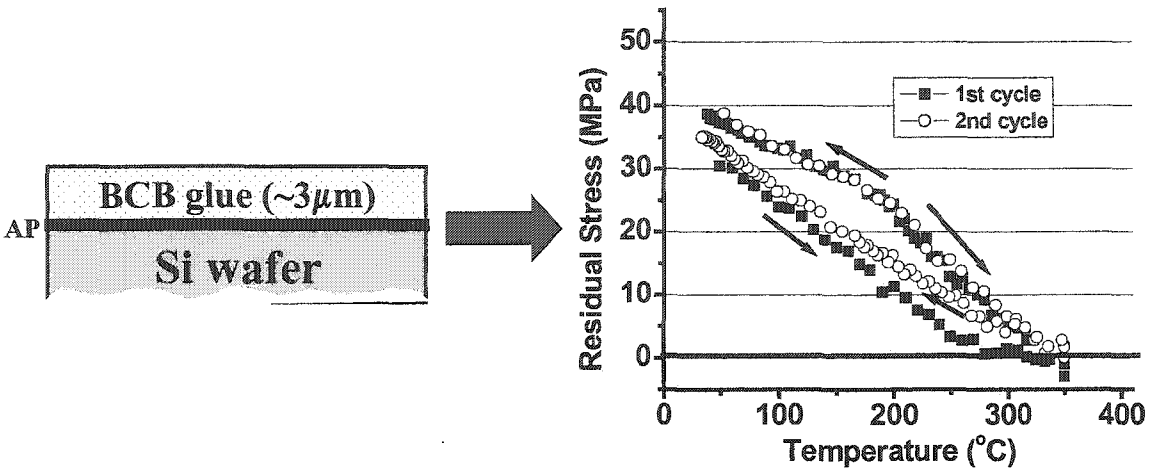


Figure 6.8: Geometry of BCB on silicon wafer and temperature dependence of residual stress on BCB on silicon wafer after the first and second thermal cycling at peak temperature of 350 °C.

stress are small, meaning that the BCB has been stabilized. The magnitude of residual stress change in BCB is far smaller than that in a PECVD oxide layer, and thus the total change in residual stress of the stacked layers is dominated by stress release in the PECVD oxide layer as described in Equation 6.3.

When the peak cycle temperature is 450 °C, cohesive failure within BCB after only one thermal cycle, caused by the degradation of BCB during the cycling process. The weak bond strength (less than 0.5 J/m^2) is evidence of BCB degradation as described in Figure 6.5. The dissociation of Si-C bonds in cured BCB resin at such an elevated temperature is the main reason for the degradation [63].

6.5. Effect of Stress Release of PECVD Oxide on Thermal cycling

The increase of bond strength in a wafer pair that consists of two PECVD oxide-deposited silicon wafers bonded with 2.6 μm of BCB thickness during thermal cycling depends on stress relaxation of the PECVD oxide layer that occurs during the first thermal cycle, as described earlier. The PECVD oxide layer undergoes a plastic deformation with permanent changes in intrinsic stress under temperatures that may be used during BEOL processing steps.

Of special interest is a large decrease in the intrinsic stress of PECVD oxide layer during thermal cycling, from huge compressive stresses after curing (-330 MPa) to smaller compressive stress after thermal cycling (-230 MPa at the peak temperature of

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400 °C and -280 MPa at the peak temperature of 350 °C). These stress changes are the result of the chemical reaction of the PECVD oxide layer. High concentrations of hydrogen and silane component are incorporated into these plasma-deposited oxide films, in the form of silanol bonds (Si-OH) [129]. The incorporation of silanols into the film is described by Equation 6.1, which is repeated here:

$$SiH_4 + 2N_2O \rightarrow SiO_2\,(s) + 2H_2 + 2N_2 \qquad (6.1)$$

According to Thurn and Cook [123], a modified reaction can occur in the presence of excess N_2O through the replacement one of the bridging –O- atoms from SiO_2(s) with a terminating –OH to form a silanol:

$$2SiH_4 + 5N_2O \rightarrow 2SiO_{3/2}\,(s) + 3H_2 + 5N_2 \qquad (6.4)$$

Combining Equations 6.1 and 6.4 leads to a joint reaction [130]

$$2SiH_4 + (4+x)N_2O \rightarrow 2[(1-x)SiO_2 + xSiO_{3/2}OH] + (4-x)H_2 + (4+x)N_2 \qquad (6.5)$$

where x ranges between zero or one ($0< x <1$). When x is zero, Equation 6.5 becomes Equation 6.1, and when x is one, Equation 6.5 becomes Equation 6.4.

The isolated silanol groups resulting from Equation 6.1 do not easily undergo a condensation reaction due to the chemically stable structure (Si-O-Si). However, two adjacent silanols resulting from Equation 6.4 can interact with each other through the following condensation reaction:

$$2SiO_{3/2}OH \rightarrow 2SiO_2 + H_2O \qquad (6.6)$$

During deposition of the oxide layer, two chemical structures are produced. One is the desirable siloxane (Si-O-Si) structure as shown in Equation 6.1 and Figure 6.9(a), and the other structure consists of two adjacent terminating silanol (Si-OH) groups produced by incomplete oxidation of silane (SiH_4) as shown in Equation 6.4 and Figure 6.9(b). The volume occupied by the –OH groups in the second structure (Figure 6.9(b)) is greater than that occupied by a bridging -O- atom, leading to compression at this site. At the elevated temperatures of a thermal cycle, two such silanol species may undergo a

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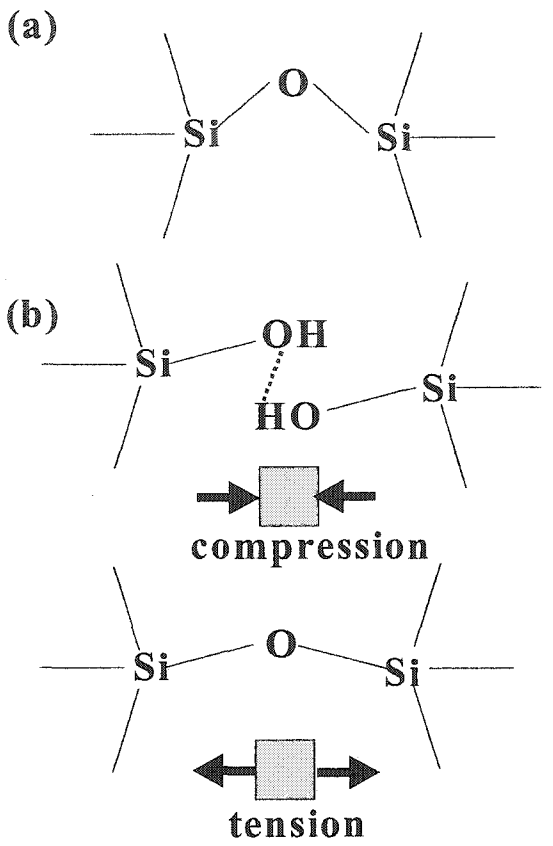


Figure 6.9: Schematic diagrams showing stress state and change of chemical structure related with condensation reaction of neighborhood silanol groups. (a) Basic tetrahedral siloxane (Si-O-Si) configuration. (b) After deposition, the Si-to-Si distance is too close for the double OH inclusion, leading to compression. (c) After thermal cycling, the Si-to-Si distance is long compared to the basis Si-O-Si configuration, leading to tension [123].

condensation reaction, leading to a bridging siloxane linkage. The distance between Si and Si across this linkage is longer than that for a normal linkage, leading to tension at this stage [123].

The above reactions and the associated volume changes induce changes in residual stress of the oxide layer. The formation of silanol sites by Equation 6.4 leads to substituting the strong siloxane bonds with comparatively weak hydrogen bond interactions between two –OH groups, giving rise to decreased structural integrity and decreased resistance to deformation. As-deposited film also exhibits decreased modulus and hardness relative to thermal oxide or bulk SiO_2 due to the hydrogen bonds caused by Equation 6.4 [123]. The large compressive deposition stresses that release somewhat

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during thermal cycling to become smaller compressive stresses are consistent with the reactions of Equations 6.4 and 6.5.

6.6. Effect of Thermal Cycling on BCB Thermal Stability

The build up of residual stresses in BCB during cooling after curing (or after any thermal excursion during processing) is mainly caused by the change in thermal stress through CTE mismatch between the glue and its adjacent layer, and differences between cure temperature and reference temperature (or between peak cycle temperature and reference temperature) *viz.*

$$\sigma_{BCB} = \frac{E_{BCB}}{1-\nu_{BCB}}(\alpha_{BCB} - \alpha_{substrate})(T_{process} - T_{reference}) \tag{6.7}$$

where E_{BCB}, ν_{BCB} are BCB modulus and Poisson's ratio, α_{BCB} and $\alpha_{substrate}$ are CTE of BCB and substrate, and $T_{process}$ and $T_{reference}$ indicate the process and environment temperature, respectively.

Liquid–like BCB resin may be considered to be in the zero stress state until the curing starts and BCB solidifies. When the solidified BCB cools, it contracts more than the adjacent PECVD oxide layer or silicon substrate due to the higher CTE (CTE of BCB is ~52 ppm/°C, CTE of PECVD SiO_2 is ~0.5 ppm/°C, and CTE of silicon substrate is ~3.2 ppm/°C) [131]. This CTE difference induces tensile stress in the BCB layer during cooling.

In the baseline bonding process, the cure temperature is 250 °C and dwell time at that temperature is 1 hr. in order to achieve void-free bonding results. BCB's residual stress and glass transition temperature, T_g can be examined by subsequent thermal cycling. Based on T_g, the cure percentage is estimated with T_g vs. cure percentage curve, as shown in Figure 6.10 [134].

During thermal cycling, BCB may be stabilized because additional curing (crosslinking) may occur during the process. On the other hand, BCB may be degraded because connections of weak bonds can be broken at high temperatures. In either case, the glass transition temperature and the residual stress of BCB are affected by thermal cycling. Evaluation of the effects of thermal cycling on residual stress, glass transition

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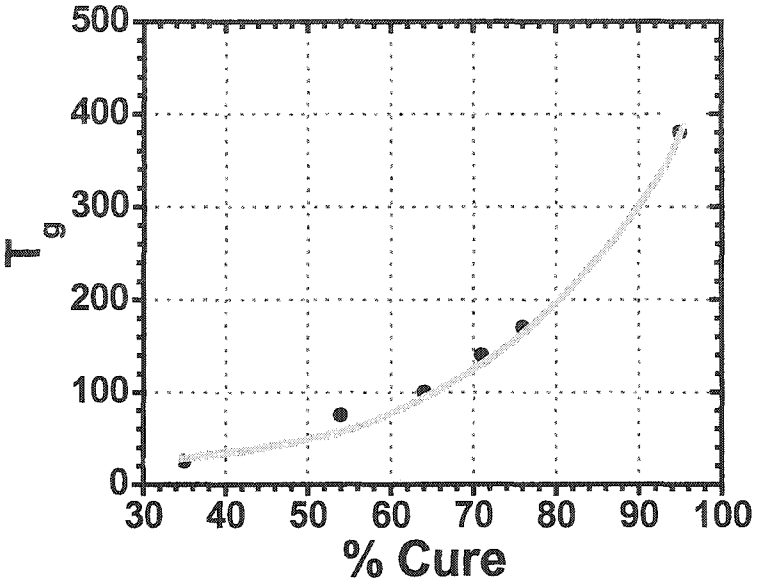


Figure 6.10: Cure % dependence of glass transition temperature (Adapted from Dow Chemical Inc. [134]).

temperature and cure percentage are useful to establish a stabilized BCB state and to delineate the key parameters needed for the increase of bond strength at the glue interface. The thermal stability of BCB is evaluated at three different temperatures (350, 400, and 450 °C) using stress measurements to help determine whether BCB is compatible with 3D applications.

For each thermal cycle, the nominal ramp rate is 25 °C/min., the dwell time at the peak temperature is 20 min., and nitrogen environment is used. The peak cycle temperature and number of cycles are varied.

The BCB cure process and BCB thermal cycle tests at three temperatures were performed to determine the temperature dependence of residual stress of the BCB layer on the silicon wafer after multiple thermal cycle tests:

1. *After BCB cure* – The BCB cure process is the same as the baseline bonding process, but without application of pressure. After the cure reaction, glass transition temperature and cure percentage are examined for subsequent thermal cycles. Figures 6.11, 6.12 and 6.13 show temperature dependences of BCB stress after multiple thermal cycles. During the heating step of the first cycle, a residual stress of 35 MPa is observed. As the temperature increases, the residual stress decreases and becomes zero at 300 °C. Since the glass transition temperature is defined as the temperature at

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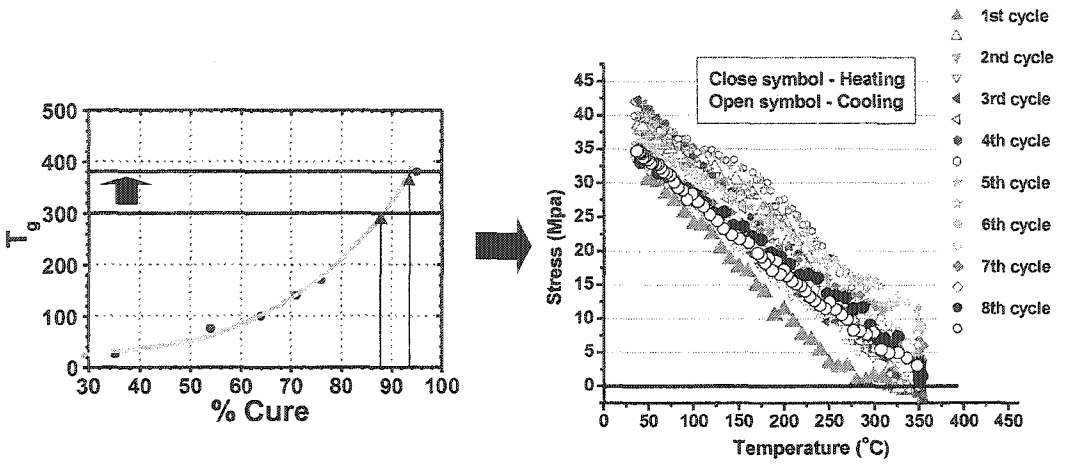


Figure 6.11: Temperature dependence of residual stress for BCB layer on silicon wafer after multiple thermal cycle tests. Peak temperature of 350 °C is used for these cycling tests.

which the stress is zero, 300 °C is the glass transition temperature of the BCB after curing. As shown in Figure 6.10, the corresponding cure percentage of BCB is ~88%.

2. *Thermal cycles to a peak temperature of 350 °C* – Figure 6.11 shows the temperature dependence of BCB residual stress after multiple thermal cycles at a peak temperature of 350 °C. As thermal cycling proceeds from the first to the seventh thermal cycle, the magnitude of stress hysteresis between heating and cooling step is reduced. We conclude that the chemical structure of bulk BCB is being stabilized (becoming more cured). At the eighth cycle, the stress hysteresis is almost zero, meaning that BCB is mostly stabilized. When the glass transition temperature induced in the stabilized state of Figure 6.11 is compared with glass transition temperature vs. cure percentage

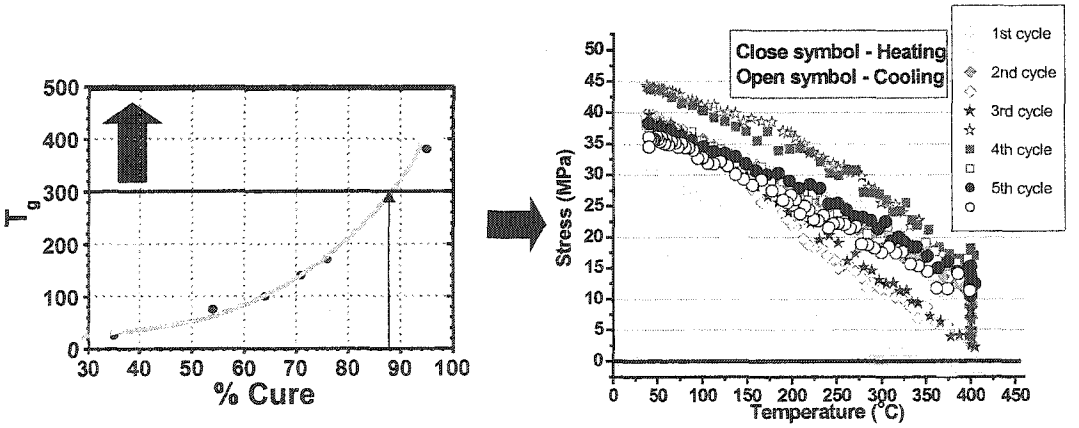


Figure 6.12: Temperature dependence of residual stress for BCB layer on silicon wafer after multiple thermal cycle tests. Peak temperature of 400 °C is used for these cycling tests.

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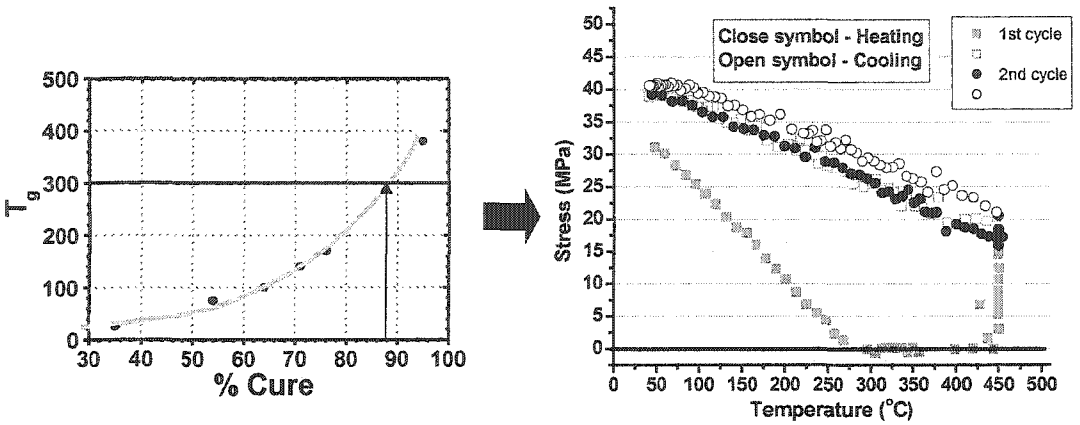


Figure 6.13: Temperature dependence of residual stress for BCB layer on silicon wafer after multiple thermal cycle tests. Peak temperature of 450 °C is used for these cycling tests.

curve of Figure 6.10, the cure percentage of stabilized BCB is ~94 %.

3. *Thermal cycles to a peak temperature of 400 °C* – Figure 6.12 shows the temperature dependence of BCB residual stress after multiple thermal cycles performed to a peak temperature of 400 °C. Proceeding from the first to the fourth thermal cycling, the magnitude of stress hysteresis between heating and cooling step is reduced. From the fifth cycle, the stress hysteresis is almost zero, meaning that BCB is stabilized. When the glass transition temperature induced in the stabilized state of Figure 6.12 is compared with cure percentage vs. glass transition temperature curve of Figure 6.10, the cure percentage of stabilized BCB is more than 95 %.
4. *Thermal cycles to a peak temperature of 450 °C* – Figure 6.13 shows temperature dependence of stress for BCB after multiple cycles at a peak temperature of 450 °C. From the second thermal cycle, the stress hysteresis between heating and cooling step is almost zero. This phenomenon has significantly different characteristics from those for cycling at peak temperatures of 350 and 400 °C. It is believed that BCB is damaged and becomes brittle due to excessive thermal decomposition during this high peak temperature thermal cycling. However, the bulky structure of BCB prevents complete disintegration of BCB and maintains the structure of an unstable solid state, (*i.e.*, although degraded, BCB does not become viscous). Hence, the structure easily collapses under small external impacts. Low critical adhesion energy value (< 0.5 J/m^2) obtained after this process is compatible with the above explanation.

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Several conclusions have been drawn from this evaluation of the effect of cycling temperature on thermal stability of BCB. When thermal cycling performed at a peak temperature of 400 °C is compared with cycling performed at 350 °C, the number of cycles needed for reaching a stabilized BCB state is reduced (the 400 °C process needs 5 cycles, while the 350 °C process needs 8 cycles.) and cure percentage at the stabilized state increased (the 400 °C process reaches more than 95 % cure, while the 350 °C process reaches ~94 % cure.)

The second is that BCB degrades during thermal cycling up to 450 °C. The chemical structure of BCB is damaged, presumably through the dissociation of Si-C bonds within BCB [63]. Due to the change in material property, cohesive failure is observed by four-point bending for this temperature process.

6.7. Summary

The effects of thermal cycling on bond strength and residual stress at the interface between BCB and PECVD oxide coated wafer and the thermal stability of BCB were evaluated by four-point bending and wafer curvature method. The results obtained through these evaluations permit; a) applying reliability criteria to the bonding integrity of the bonded wafer stacks and b) establishing a thermal cycling that yields stable BCB layers.

A peak cycle temperature and the number of thermal cycle are the key variables to affect bond strength and residual stress during thermal cycle process. Quantitative evaluations of the effect of these variables on bond strength and residual stress are important because high temperature processes (over 350 °C) and multiple thermal excursions are generally used in BEOL and 3D integration processes. In spite of these usages, effects of the high temperature processes and the multiple thermal excursions on bond strength/residual stress at the interface between BCB and PECVD oxide, and the thermal stability of BCB are not well understood.

In thermal cycling performed at peak temperatures of 350 and 400 °C, relaxation of residual stress in the PECVD oxide layer by condensation reaction occurring during the first thermal cycle dominates the increase of bond strength at the interface between BCB and PECVD oxide ("first cycle effect"), meaning that stress relaxation of PECVD oxide

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layer leads to the decrease in deformation energy by residual stress, $G_{residual}$ and the increase in bond strength, G_c at the interface between BCB and PECVD oxide layers of a bonded wafer stack.

After the first thermal cycle, stress hysteresis of the PECVD oxide layer is not observed because the condensation reaction affecting the relaxation of residual stress was driven to completion. Little if any stress release is seen in the second thermal cycle, which leads to a stable bond strength at the interface between BCB and PECVD oxide layers after the first thermal cycle.

In peak cycle temperature, the magnitude of residual stress change of PECVD oxide layer released in the 400 °C process is about twice that released during the 350 °C process. Accordingly, the magnitudes of the bond strength increase and the residual stress release during the 400 °C thermal cycle process are higher than those during the 350 °C thermal cycle process. This difference is caused by different amounts of condensation reaction occurring in the PECVD oxide layer during thermal cycling. When the peak temperature is 400 °C, the condensation of silanol in the PECVD oxide layer occurs more vigorously than that at 350 °C.

Another set of thermal cycle tests was performed at 350, 400 and 450 °C peak temperatures in order to evaluate BCB thermal stability. BCB was first cured using the baseline process. During the first heating cycle, BCB becomes plastic at ~300 °C and residual stress is relaxed. At the peak temperatures of 350 and 400 °C, BCB is more cured and the residual stress is reset at a new glass transition temperature corresponding to the increased BCB cure conversion. The reset stress increases during the cooling process. As more thermal cycles are performed, stress hysteresis of BCB becomes less, as the BCB is being stabilized. After a small number of thermal cycles (<10), BCB reaches a steady state (no hysteresis of residual stress).

When the peak cycle temperature is 350 °C, BCB reaches steady state from the eighth thermal cycle, and cure percentage at the steady state is ~94%. On the other hand, when the peak cycle temperature is 400 °C, BCB reaches steady state from the fifth thermal cycle, and cure percentage at the steady state is more than 95%. The BCB process for wafer-to-wafer bonding applications is mostly stabilized after four cycles at a peak temperature of 400 °C.

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Thermal cycle process performed at a peak temperature of 450 °C gives rise to cohesive failure within BCB layer with very low critical adhesion energy (< 0.5 J/m^2). The low critical adhesion energy value is evidence for the limited thermal stability of BCB. The chemical structure of the BCB is damaged through the dissociation of Si-C bonds within BCB during thermal cycling performed at a peak temperature of 450 °C.

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CHAPTER 7
BONDING INTEGRITY OF PATTERNED WAFERS

7.1. Overview

One of the critical issues in 3D IC implementations consisting of wafers that have been processed through the BEOL is compatibility with advanced semiconductor processing protocols [3-5,24,26]. Procedures to evaluate the impact of the wafer bonding process on the performance and yield of wafers without requiring inter-wafer interconnects processing are presented here. Wafers with two-level back-end copper interconnect test structures including two types of inter-level dielectrics (ILDs) (both oxide and porous low-k) are considered, and mechanical and electrical bonding integrities are evaluated through the procedures. International SEMATECH provided both Cu/ILD patterned wafers.

Although various procedures can be applied to evaluate bonding integrity, three procedures are mainly discussed [24]; (1) optical inspection of the bonding interface (void/defects/uniformity) using TCE-matched glass wafers, (2) four-point bending to quantify bond strength and identify the weak bond interface, and (3) electrical tests of the patterned wafers using additional bonding, thinning and dielectric glue ashing.

In this chapter, optical inspections of patterned wafers with oxide and porous low-k ILDs are discussed first. Then, the four point bending determinations of the weak interface of each patterned wafer and its critical adhesion energy is discussed. Finally, test results of electrical bonding integrity through the measurements of via contact resistance and comb-to-comb leakage current are described.

7.2. Patterned Wafer Results

The wafers considered are "interconnect test structure wafers" supplied by SEMATECH. One important feature of these wafers is that they have 900 nm topological features (Al test pads) across their surfaces. Figure 7.1 shows the initial flow used to evaluate the bonding and thinning processes [26,104]. Each wafer is bonded onto a TCE-matched glass wafer using BCB (2.6 μm thick, baseline bonding process). The use of

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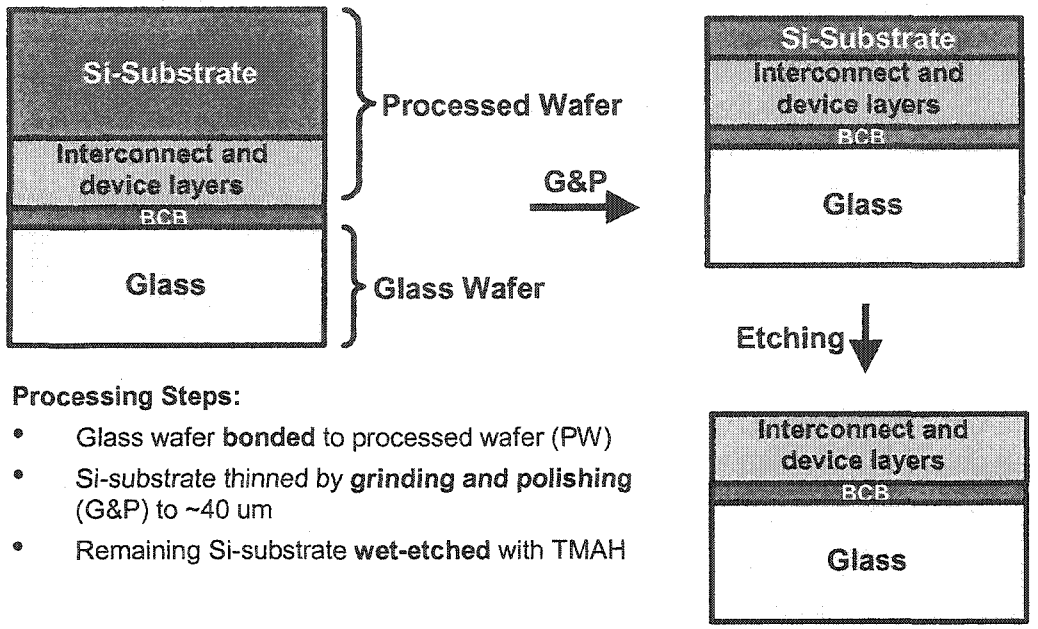


Figure 7.1: Preliminary procedure for evaluation of wafer bonding and thinning.

TCE matched glass allows visual inspection of the bonding (and thinning) integrity through the glass wafer.

After bonding, the silicon substrate is removed by a three-step thinning process: grinding, polishing and tetramethyl-ammonium hydroxide (TMAH) wet etching [5,26-27]. First, the backside silicon of a bonded wafer pair (a processed silicon wafer and a glass wafer in this case) is thinned to ~40 μm by grinding and polishing, and visually inspected with respect to changes at the interface. Finally, the remaining silicon is completely wet etched using TMAH, and again inspected for defects. After Si removal, transparent interconnect structures remain bonded to the glass wafer. This procedure permits bonding and thinning integrity evaluation without requiring inter-wafer interconnect processing [104].

Figure 7.2 shows a photo of a 200 mm processed Si wafer after bonding to a glass wafer, thinning the silicon substrate of the processed wafer using grinding and polishing processes (No wet etching). Though the surface profile result shows a step height of ~900 nm across the Al pads on the patterned wafers (as shown in Figure 7.2), void-free bonding is obtained and maintained after wafer thinning. No changes in the patterns can be visually observed after wafer bonding and thinning processes. Moreover, bonding integrity with such wafers is maintained even if the silicon is completely removed on part

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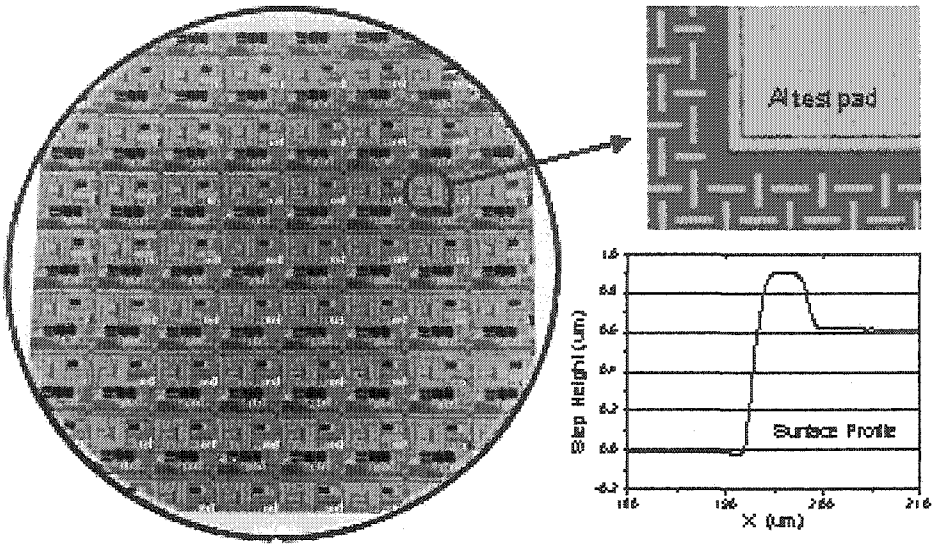


Figure 7.2: Wafer bonding/thinning result for a processed wafer with two-level Cu/oxide interconnects (provided by International SEMATECH) bonded on a glass wafer. Right side: surface profile showing a step height of 900 nm across the Al pads.

of the wafer, *i.e.*, the silicon is "punched through" in some part of the wafer due to the non-uniformity in mechanical grinding/polishing process. In these cases, the remaining silicon layer (very thin) is still bonded well to the bottom wafer, with no visible changes at the bonding interface [104].

The backside silicon of the wafer shown in Figure 7.2 is then completely removed by the TMAH wet etching step with the oxide acting as the etch-stop. As shown in Figure 7.3, a quasi-transparent wafer with Cu/oxide interconnect test structures bonded to the glass wafer is obtained [24,104]. Detailed microscopy inspection indicates a defect-free bonding interface with damage-free interconnect patterns. A similar study was carried out on SOI wafers (with passive and active devices) where the buried oxide (BOX) layer acts as an etch-stop for TMAH etching. Similar quasi-transparent wafers with device layers on glass wafers are obtained [5,24].

A more aggressive evaluation procedure using a double bonding and thinning process is performed for the evaluation of bonding/thinning integrity, as shown in Figure 7.4. Wafer Si-I and/or Si-II can be either a prime silicon wafer with or without an oxide layer, a prime SOI wafer, or a TCE-matched glass wafer. If the processed wafer is an SOI wafer, the thinned substrate can be the BOX layer in step (b) of Figure 7.4. The Si substrate of the processed wafer can be completely wet-etched (the etch stops on the

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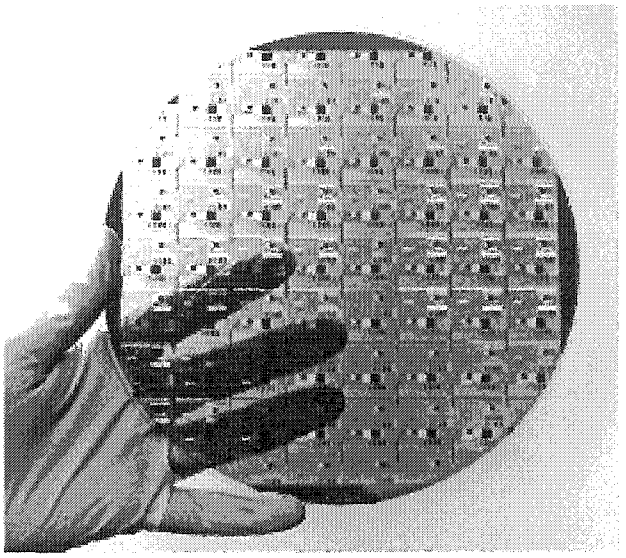


Figure 7.3: Photo image of a Cu/oxide interconnect structures after bonding to a glass wafer using BCB and complete removal of the Si by grinding, polishing and TMAH etching [24,26].

BOX) after backside grinding/polishing due to the high etch selectivity of TMAH [24,26,104].

The common processing steps for this evaluation procedure include additional

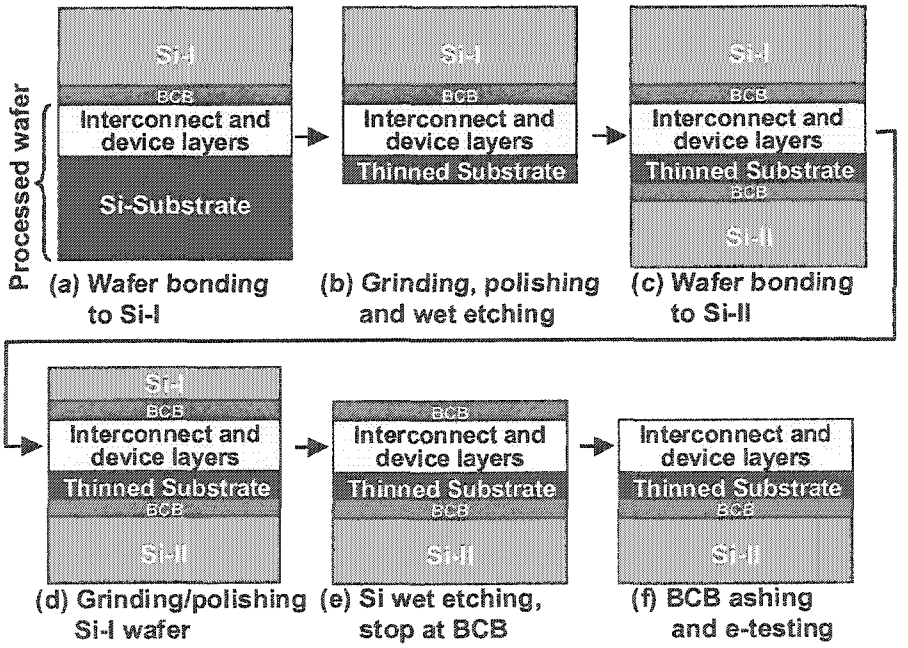


Figure 7.4: Process flow of a typical double bonding/thinning procedure, permitting bonding and thinning integrity evaluation without inter-wafer interconnect processing [24,104].

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bonding and thinning along with BCB ashing to expose the previously tested interconnect structures. The interconnect test wafers with Cu/ILD interconnect structures experience two bonding and thinning processes, plus a top silicon (Si-I) removal (wet-etch) and a BCB RIE ashing in order to re-expose the Al test pads for electrical testing. Table 7.1 shows process conditions for the BCB ashing. A void-free bonding interface and damage-free patterns are visually observed after this procedure. This result with a bonded structure of three wafers (three-wafer level bonding) demonstrates that the wafer bonding process for 3D integration can preserve the mechanical integrity of the Cu/ILD interconnect structures even after double bonding/thinning.

One concern during the evaluation of integrity of the wafer bonding and thinning processes is wafer breakage and edge chipping. These phenomena have been observed and were reported in literatures [132-133]. Most thinning processes rely heavily on backside grinding, which results in the formation of sharp wafer edges. Such edges combined with damage induced during the grinding lead to edge chipping and/or wafer breakage. Edge chipping has a deleterious effect on the useful wafer real estate and post-thinning processing. Post-grinding techniques such as polishing [132] and wet or dry chemical etching [133] have been shown to significantly improve the edge quality and increase the wafer survival probability after thinning. To reduce the damage induced during grinding, polishing is used. A small amount of wafer edge chipping (<1 mm), as shown in Figure 7.5, has been observed in the single bonding/thinning process after polishing.

Another possible reason for edge chipping is locally concentrated stresses during the thinning process. In particular, it is believed that normal forces generated by "peeling stress" initiates the crack from the edge area, and shear forces generated by shear stress propagate the initiated crack along the interface [91,93].

Table 7.1: RIE ashing parameters for BCB glue

RF power (13.56 MHz)	250 W
Total pressure	30 mTorr
Flow rate of O_2 gas	80 sccm
Flow rate of CF_4 gas	20 sccm

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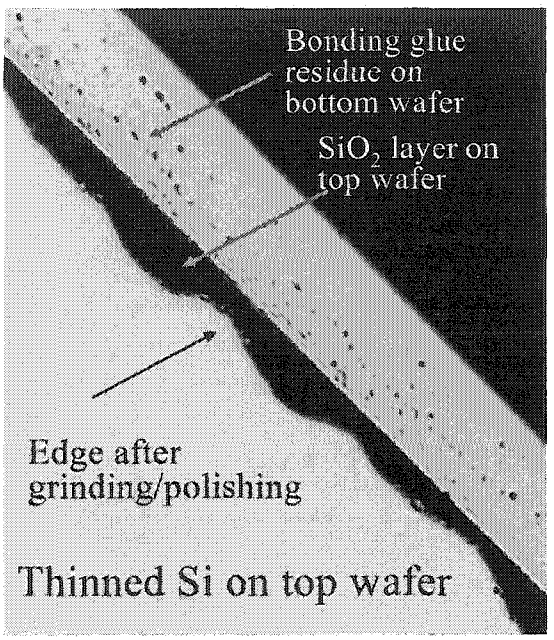


Figure 7.5: Wafer edge chipping after grinding/polishing of the top processed wafer to ~50 μm. Top wafer was bonded to a Si wafer with the baseline BCB bonding process [26,104].

7.3. Mechanical Evaluation of Bonding Integrity

Four point bending is used to characterize mechanical aspects of the bonded two level Cu/ILD interconnect structures [13] with either a oxide inter-level dielectric (ILD) or a porous low-k ILD. Each wafer is bonded onto a silicon wafer with a 2 μm thermal oxide layer, using 2.6 μm BCB (baseline bonding process). Table 7.2 indicates the important four point bending results for the two bonded wafer pairs. Figure 7.6 shows the beam

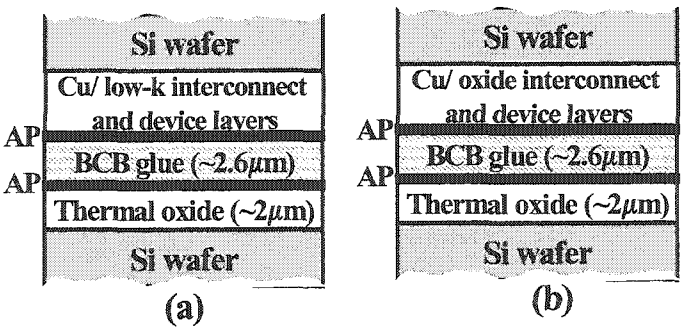


Figure 7.6: The beam specimen configurations of the two types of patterned wafers: (a) bonded wafer pair including Cu/low-k interconnects; (b) bonded wafer pair including Cu/oxide interconnects.

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specimen configurations of the two bonded wafer pairs, and Figure 7.7 shows evaluation results of critical adhesion energies on the bonded wafer pairs. In both bonded wafer pairs, the critical adhesion energies don't depend appreciably on which side the beam (either blanket silicon wafer or processed wafer) is pre-cracked (see Table 7.2).

Table 7.2: Four point bending results of two bonded wafer pairs including the patterned wafers

Geometric configuration of beam specimen	BCB thickness	Load-plateau	n	Mean G_c (J/m^2)	S.D. (J/m^2)
Pre-crack of oxide wafer					
Cu/oxide ILD/AP/BCB/AP/SiO_2/Si	2.6 μm (double layer)	Type 1	5	21	1.9
Cu/low-k ILD/AP/BCB/AP/SiO_2/Si	2.6 μm (double layer)	Type 1	5	6	0.6
Pre-crack of the patterned wafer					
Cu/oxide ILD/AP/BCB/AP/SiO_2/Si	2.6 μm (double layer)	Type 1	5	22	1.7
Cu/low-k ILD/AP/BCB/AP/SiO_2/Si	2.6 μm (double layer)	Type 1	5	6	0.5

Figure 7.8 shows optical images of the weak (fracture) interfaces of the two processed wafers after four point bending. Debonding occurs in the interconnect structures on both

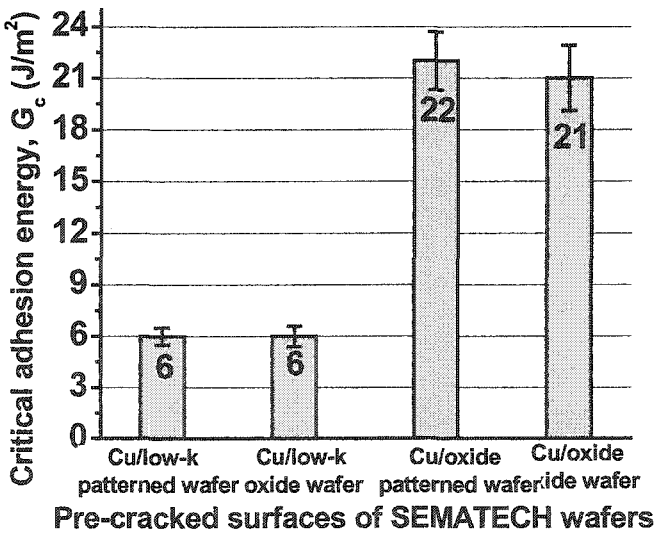


Figure 7.7: Critical adhesion energies of fully processed Cu/low-k and Cu/oxide wafer: each processed wafers has different pre-cracked surfaces.

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processed wafers, rather than at a BCB interface. This result also shows that bond strength between BCB and thermal oxide (34 J/m^2 with adhesion promoter; see Figure 5.6) is larger than that of the Cu/ILD interconnect structures. Load vs. displacement curves from the four point bending experiments are "Type 1" for both bonded wafer pairs.

7.4. Electrical Evaluation of Bonded Wafers

Electrical characteristics of the two level Cu/ILD interconnect structures are

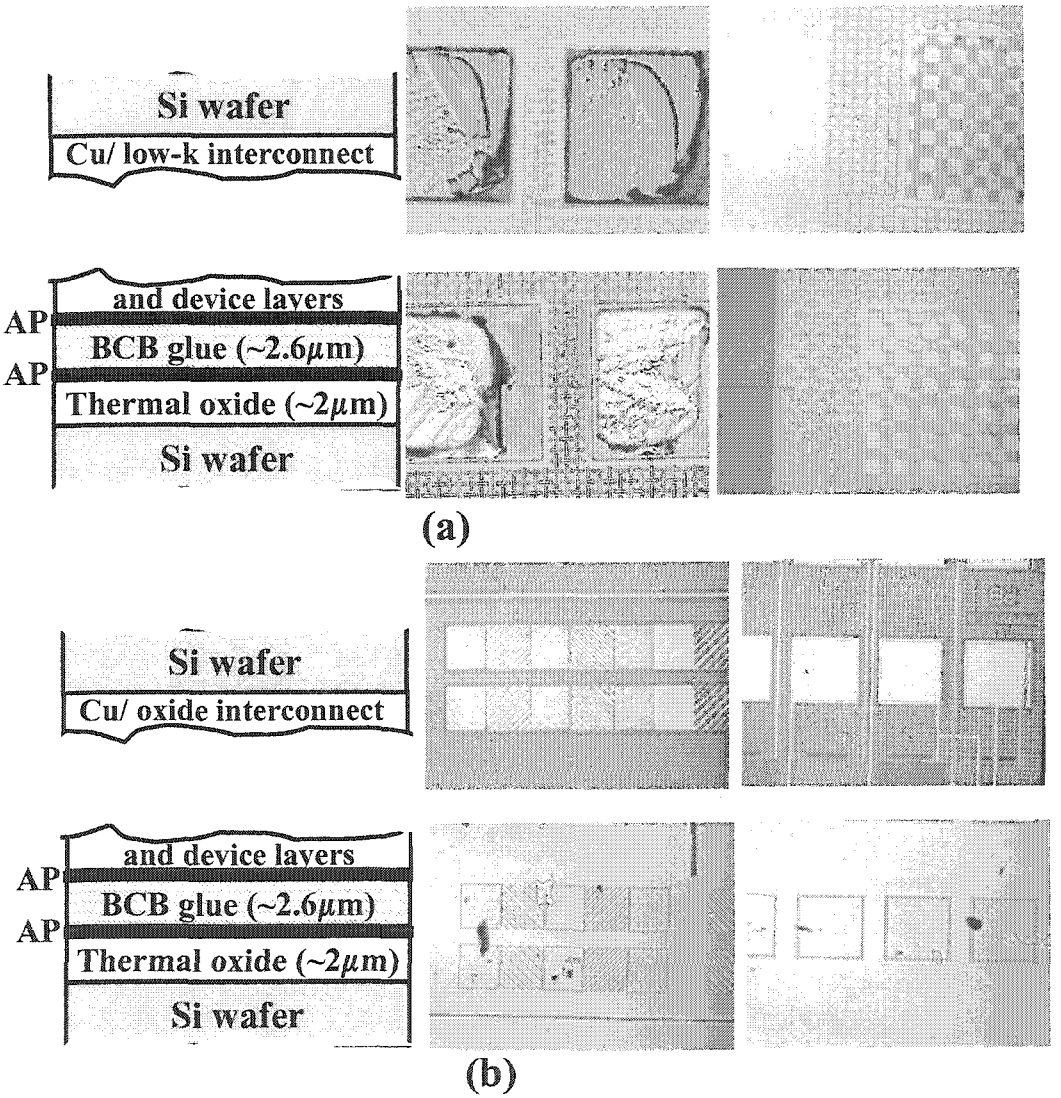


Figure 7.8: Optical images of weak interfaces of the two types of processed wafers: (a) bonded wafer pair including Cu/low-k interconnects; (b) bonded wafer pair including Cu/oxide interconnects.

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measured before and after bonding to a blanket silicon wafer using BCB and complete removal of the bonded silicon wafer using our baseline process [11-12].

Figure 7.9 shows the electrical test results of patterned wafers before and after the bonding and thinning [104]. In addition, the patterned wafers experience BCB ashing to re-expose the Al test pads for electrical testing. A slight change in the via-chain resistance and an order of magnitude change in the comb-to-comb resistance are observed after this processing. Both changes are within acceptable limits. These results demonstrate that electrical characteristics of the processed wafers are maintained after bonding and thinning processing. One difference is that the bonded blanket silicon wafer was completely removed by thinning for the case shown in Figure 7.9, instead of the silicon substrate of the processed wafer as shown in Figures 7.2 and 7.3. Similar to the case of a single bonding/thinning process, the via-chain resistance did not change after the double bonding/thinning and BCB ashing processes. The change in the comb-to-comb leakage current after the double bonding/thinning process is comparable to that of a single bonding/thinning process (see Figure 7.10) [24,104].

It is interesting to note that excellent electrical characteristics are maintained even after bonding and thinning, which are thermally and mechanically aggressive processes. Results with processed wafer with Cu/low-k interconnect structures are also promising,

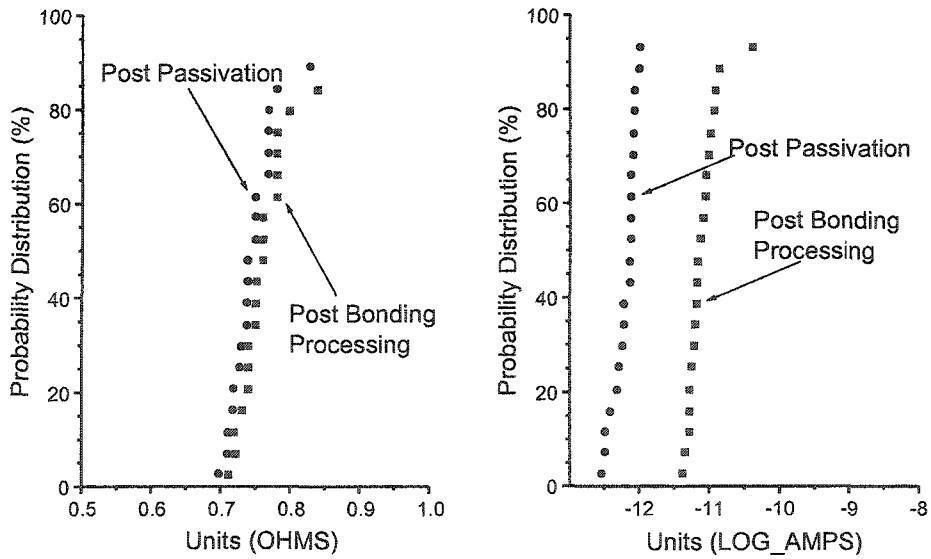


Figure 7.9: Electrical tests of processed wafer before and after wafer bonding, thinning, and BCB removal processes. (a) Probability chart of 360k 0.25 μm via chain resistance. (b) Probability chart of comb-to-comb bridging current at 5V. Data provided by International SEMATECH [104].

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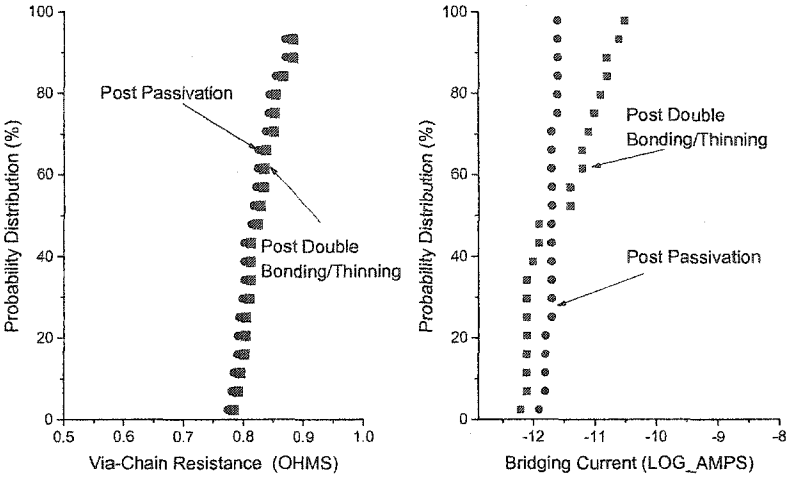


Figure 7.10: Electrical tests of processed wafer before and after double bonding and thinning, and then BCB removal processes. (a) Probability chart of 360k 0.25 μm via chain resistance. (b) Probability chart of comb-to-comb bridging current at 5V. Data provided by International SEMATECH [104].

although issues with low-k mechanical integrity have been observed as described elsewhere [24,104].

7.5. Summary

Procedures to evaluate the mechanical and electrical impacts of wafer bonding and thinning processes required for 3D integration applications (focusing on 3D IC fabrication) are discussed. Wafers with two-level back-end copper interconnect test structures including two types of inter-level dielectrics (ILDs) (one is oxide ILD and the other is porous low-k ILD) have been used for the purpose. The electrical results indicate the viability of the bonding techniques described in this research for 3D IC applications.

Four-point bending has been used to evaluate mechanical bonding integrity of the bonded wafer pairs; each consisting of a patterned wafer bonded onto a silicon wafer. For the bonded wafer pair containing the Cu/porous low-k ILD wafer, the critical adhesion energy measured at the weak interface is 6 J/m^2, and in the bonded wafer pair including Cu/oxide ILD wafer, the critical adhesion energy measured at the weak interface is 21 J/m^2. Optical images indicated that the debonding occurred in the interconnect structures on both processed wafers rather than at the BCB interface.

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Electrical testing (via-chain resistance and comb-structure leakage current) of the patterned wafer interconnect structures using both single and double bonding and thinning procedures shows that critical parameters remain within acceptable ranges.

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CHAPTER 8
SUMMARY, CONCLUSIONS AND FUTURE WORK

8.1. Summary and Conclusions

Silicon back-end-of-the-line (BEOL) technology has advanced significantly in the last decade with the advent of copper/low-k damascene patterning technology, which postpones the interconnect bottleneck by approximately three generations of scaling [4-7]. However, as minimum feature size goes deeper into sub-micron regime, even global interconnects with damascene-patterned copper/low-k technology will limit the performance of gigascale integrated devices [1]. Moreover, even the most innovative first-level single chip and multiple chip packaging approaches can limit IC performance [4,7]. 3D integration approaches, including 3D ICs and bond/etch-back SOI, have been considered to overcome these problems [4-5]. Several analyses have been used to demonstrate that this 3D integration can reduce the RC delays of global interconnects and accomplish increased functionality over conventional planar ICs, while maintaining the cost advantage [4,7].

In one 3D IC integration approach, fully processed wafers (with multilevel on-chip interconnects) are aligned and bonded with dielectric glue, followed by "top-wafer" thinning using backside-grinding and polishing. After top wafer thinning, inter-wafer interconnects are formed using copper damascene patterning. Four key challenges in this approach are; 1) achieving needed wafer level alignment accuracy, 2) reliably bonding the wafer, 3) thinning wafer accurately and without damage, and 4) interconnecting the wafer stack [3,5-6].

One of the fundamental requirements for 3D IC implementation is that the processing steps must be compatible with advanced semiconductor processing protocols. Process conditions during the bonding step, among other 3D process steps, must remain within certain windows as not to be detrimental to the processed wafers making up the bonded stack. Additionally, the wafer bond itself must be able to withstand conventional BEOL processes, particularly those BEOL processes involving harsh thermal and/or mechanical conditions such as wafer thinning, CMP and thermal cycling [26].

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Bonding methods may be classified into two categories: fusion bonding and intermediate bonding. In this thesis, the focus is on intermediate bonding technology using low-k dielectric polymers as glues. Such bonds routinely show a larger fraction of bonded area, and higher bond strengths than those using other bonding methods [38-39,50]. Several low-k dielectric polymers (MSSQ, Parylene-N, Flare and BCB) were used as bonding glues. The fractions of bonded area were determined by optical inspection after bonding silicon wafers to CTE-matched glass wafers. Based on these glue-screening tests, BCB was selected as the baseline glue material for the 3D program at RPI, due to its complete, reproducible, and void-free bonding results.

The bond strength of wafer pairs bonded using BCB is measured using four-point bending. Using the four-point bending technique allows us to examine bonding integrity of the BCB for 3D applications in a quantitative way. The effect of the following chemical and geometric variables on bond strength have been investigated; (1) glue film preparation (*e.g.*, adhesion promoter), (2) BCB thickness, and (3) identity of material on the substrate surfaces (*e.g.*, silicon, silicon oxides and glass).

We find that BCB adhesion promoter influences the glue interfacial chemistry and bond strength. When the adhesion promoter is used, bond strength increases by about a factor of two for both "baseline BCB" bonds (2.6 μm of BCB applied in two layers then bonded) and "thin BCB" bonds (0.4 μm of BCB applied in one layer). In case of two wafers covered with PECVD oxide that are bonded using 2.6 μm of BCB, an adhesion energy of 31 J/m^2 is obtained when using the adhesion promoter and 13 J/m^2 without the adhesion promoter. For a similar wafer pair bonded using 0.4 μm of BCB, an adhesion energy of 19 J/m^2 is obtained when using the adhesion promoter and 10 J/m^2 without the adhesion promoter.

These results also demonstrate that BCB thickness affects the bond strength at the glue interface with thicker glue layers corresponding to higher bond strengths. The decrease in bond strength observed for thin BCB is apparently due to a decrease in the contribution of plastic dissipation energy, which is proportional to BCB thickness. In both bonded wafer pairs that include a PECVD oxide deposited silicon wafer and a glass wafer, the critical adhesion energies are linearly proportional to BCB thickness within the pre-determined BCB thickness range. Based on these results, the relationship between

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plastic energy dissipation, $G_{plastic}$, and bond breaking energy, G_{tip}, and BCB thickness, t is observed to be $G_{plastic} \approx 0.3 \cdot G_{tip} \cdot t$ (see Section 5.3).

The choice of materials (substrates) in contact with BCB also affects the bond strength. A wafer pair, each with PECVD oxide layers, bonded with a 2.6 μm thick BCB layer had a critical adhesion energy of 31 J/m^2. Wafers with thermal oxide bonded in the same way had a critical adhesion energy of 34 J/m^2, and bonded wafers with native oxides had a critical adhesion energy of 30 J/m^2. All of these oxide-BCB bond strengths are almost identical within measurement error (see Table 5.2). However, a silicon wafer bonded to a CTE-matched glass wafer had a critical adhesion energy of 9 J/m^2. It is believed that the difference in chemical composition between the glass wafer and the oxide layer on the silicon wafer is the reason for this dramatic difference in bond strength.

The effects of thermal cycling on bond strength and residual stress at the interface between BCB and a PECVD oxide coated wafer, and the thermal stability of BCB were evaluated by four point bending and by wafer curvature measurements. The results obtained through these measurements help establish; a) criteria to evaluate the bonding integrity of the bonded wafer stacks, and b) a thermal cycling process that yields stable BCB layers.

Quantitative evaluations of the effects of thermal cycling on bond strength and residual stress are important because high temperature processes (over 350 °C) and multiple thermal excursions are generally used in BEOL and 3D integration processes. During thermal cycling, peak cycle temperature and the number of thermal cycles are key variables that affect bond strength.

Stress relaxation of the PECVD oxide layer during thermal cycling can lead to a decrease in the deformation energy due to residual stress, $G_{residual}$, and consequently to an increase in bond strength, G_c. In thermal cycling performed at peak temperatures of 350 and 400 °C, there is a relaxation of residual stress in the PECVD oxide layer by condensation reactions that change the chemical structure of the film. This release of stress increases the bond strength at the interface between BCB and PECVD oxide. It is observed that the relaxation of residual stress occurs predominantly during the first thermal cycle ("first cycle effect"). In thermal cycles after the first one, stress hysteresis,

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(*i.e.*, relaxation of residual stress) of the PECVD oxide layer is not seen, presumably because the condensation reaction does not progress significantly beyond the point reached in the first cycle. Thus little change in bond strength at the interface between BCB and PECVD oxide layers is seen after the initial increase seen in the first cycle.

The magnitude of the residual stress change in the PECVD oxide layer during the 400 °C process is about twice that released during the 350 °C process. Accordingly, the bond strength increase during the 400 °C thermal cycle process is higher than that during the 350 °C thermal cycle process. The likely cause of this increase in stress release, and corresponding increase in bond strength, at higher peak temperature is an increase in the extent of the condensation reaction produced in the PECVD oxide layer at the higher temperature. At a peak temperature of 400 °C, the condensation reaction in the PECVD oxide layer occurs more vigorously than at 350 °C.

Thermal cycle tests were performed at 350, 400 and 450 °C peak temperatures in order to evaluate BCB thermal stability. BCB was first cured using the baseline process. During the first heating cycle, BCB becomes plastic at ~300 °C and residual stress is relaxed. At peak temperatures of 350 and 400 °C, BCB is more cured and the residual stress is reset at new glass transition temperatures corresponding to the increased BCB cure conversions. The reset stress increases during the cooling process. As more thermal cycles are performed, stress hysteresis in the BCB layer gets smaller, as the BCB is being stabilized. After a small number of thermal cycles, BCB reaches steady state (*i.e.*, exhibits no hysteresis of residual stress). When the peak cycle temperature is 350 °C, BCB reaches steady state from the eighth thermal cycle with a cure percentage at steady state of ~94 %. On the other hand, when the peak cycle temperature is 400 °C, BCB reaches steady state from the fifth thermal cycle with a cure percentage at steady state of more than 95 %. The BCB process for wafer-to-wafer bonding applications is mostly stabilized after four cycles at a peak temperature of 400 °C.

Thermal cycling performed at a peak temperature of 450 °C gives rise to cohesive failure within the BCB layer, with very low critical adhesion energy (< 0.5 J/m^2). The low critical adhesion energy value is evidence that 450 °C is beyond the thermal stability temperature of BCB. The chemical structure of the BCB is damaged through the

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dissociation of Si-C bonds within BCB during thermal cycling performed at a peak temperature of 450 °C [63,90].

Procedures to evaluate the mechanical and electrical impacts of wafer bonding and thinning processes required for 3D integration applications (focusing on 3D IC fabrication) are discussed in this thesis. Wafers with two-level back-end copper interconnect test structures including two types of inter-level dielectrics (ILDs) (one is oxide ILD and the other is porous low-k ILD) have been used for the purpose. Electrical results performed by International SEMATECH indicate the viability of the bonding techniques described in this research for 3D silicon ICs [24,104].

Four-point bending has been used to evaluate mechanical bonding integrity stacks including patterned wafers. For a bonded wafer pair containing a Cu/porous low-k ILD wafer, the critical adhesion energy measured at the weak interface is 6 J/m^2, and in a bonded wafer pair including Cu/oxide ILD wafer, the critical adhesion energy measured at the weak interface is 21 J/m^2. Optical images indicate that debonding occurred in the interconnect structures on both processed wafers rather than at the BCB interface.

Electrical testing of the patterned wafers, subjected to single-bonding, double bonding and thinning procedures, shows that critical parameters remain within acceptable ranges (see Section 7.4).

8.2. Future Work

Based on this thesis, some suggestions are made about work relating to BCB based bonding that can be pursued:

1. Evaluation of the effect of via pattern density on bond strength
2. Improving the CTE of BCB through the inclusion of solids
3. Evaluation of the bond strength obtained by other bonding technologies
4. Evaluation of the bond strength after bonding silicon to non-CTE matched wafers
5. Surface analyses of the fractured surfaces
6. Evaluation of the effect of surface morphology of the glue-adjacent layer on bond strength.

Brief descriptions of each of these topics follow:

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Evaluation of the effect of via pattern density on bond strength: The bonded wafer pairs used for evaluations of the bond strength did not have any inter-wafer vias (metal interconnects between two wafers) although the inter-wafer vias are required for fabricating 3D integrated devices. The inter-wafer vias may be weakened during harsh processes and fail because of the occurrence of cracks and the excessive stresses beyond the yield point. Furthermore, different pattern densities and aspect ratios of inter-wafer vias may accelerate or decelerate the adhesion failure. It is therefore needed to evaluate the effects of pattern density and aspect ratio of the inter-wafer vias on bond strength. The bond strength of wafer pairs bonded for this purpose is measured by four point bending. Figure 8.1 illustrates the process flow for bonding wafers with via patterns and the beam specimen preparation of such structures. Test patterns of vias can be created through a lithographic process. After lithographic patterning of a sacrificial oxide layer, BCB is spun-on, baked and cured. Then, to expose the buried silicon oxide layer, BCB is dry-etched. When the silicon oxide layer is exposed, BOE etching is performed to remove the silicon oxide layer. In the next step, Ta barrier layers and Cu interconnects (vias) are deposited and CMP is conducted to planarize the surface. This wafer including via patterns is bonded with another wafer using BCB and the baseline bonding process.

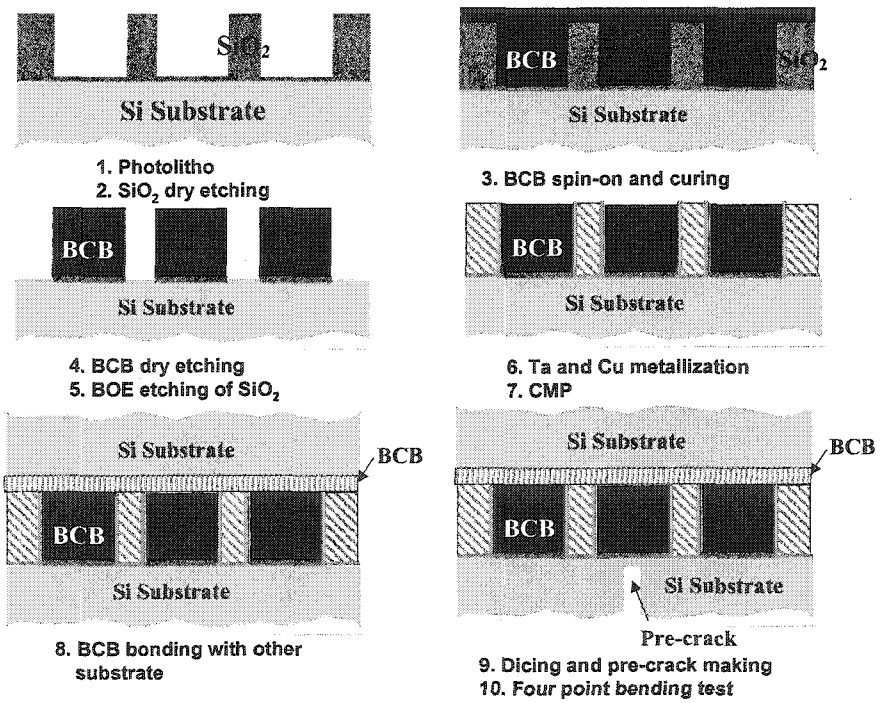


Figure 8.1: The process flow of the bonding of wafers including via patterns and its beam specimen preparation.

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The bonded wafer pair is diced into beam shapes and pre-cracks are made as described in Section 3.3 before four point bending testing is performed. Using these results, limits on pattern density and aspect ratio of inter-wafer vias can be determined that will keep bonding integrity within a required window.

Improving the CTE of BCB through the inclusion of solids: Upon curing, BCB "thermosets," become amorphous and highly cross-linked. This microstructure results in many useful properties for structural engineering applications, such as high modulus, high failure strength, low creep rates, and good performance at elevated temperatures [135]. However, the structure of such thermosetting polymers often leads to high CTE values. Subsequently, the large CTE mismatch between BCB and substrate can induce large thermal residual stresses at the bond interface. As a result, adhesion failure or glue delamination may occur during harsh processes. To make the CTE of BCB (52 ppm/°C) comparable with those of other substrates; *e.g.*, silicon (3.2 ppm/°C) and silicon dioxide (0.5 ppm/°C), loading of nanometer or micron-sized solids into bulk BCB can be considered [135]. For example, the silica beads can be loaded into BCB resins during BCB spin-on process and subsequent curing will result in significant variation of CTE in silica beads loaded BCB [72,136-137]. As the ratio of beads to resins increases, the CTE of BCB will decrease due to the lower CTE of the silica beads. The extent of CTE decrease is closely related to the extent of loading of silica beads (weight % of silica beads in combination of BCB resin and silica beads) [136]. As the bead size decreases at a constant volume fraction loading, the CTE of BCB decreases. This CTE decrease can be explained by considering the total surface area of the bead particles [136]. With the inclusion of silica beads, the expansion of the BCB resin at the interface between silica beads and BCB resin is constricted during thermal processes. As the surface area of the beads increases due to the decrease in bead size, constriction of the BCB resin increases and CTE of the BCB decreases [72,137]. When large sized beads and small sized beads are mixed with the proportions varying from 100% large sized beads to 100% small sized beads, CTE values of BCB resin decrease due to the increase of surface area. However, the presence of beads in the liquid BCB results in an increase in viscosity. A higher viscosity and subsequent decrease in flow rate may lead to a non-uniform deposition of BCB. When the thickness uniformity of BCB is poor, bond quality will be lowered due to

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the generation of voids during bonding process. Therefore, it is important to determine how to achieve a low CTE while keeping a low enough viscosity that uniformity is not severely impacted.

Evaluation of the bond strength of other bonding technologies: Bond strength of other wafer bonding techniques, particularly direct wafer bonding (*i.e.*, SOI wafer) can be evaluated and compared with that of BCB bonding. Four-point bending can be used to quantify the bond strengths. Changes in bond strength occurring due to thermal cycling performed at high temperatures (above 350 °C) can be monitored and the possibility of adhesive failure can be diagnosed as described in Chapter 6.

Evaluation of the bond strength after bonding silicon to non-CTE matched wafers: Bond strength can be measured by four point bending, after bonding silicon wafers to non-CTE matched wafers (*e.g.*, non-CTE matched glass wafers and sapphire wafers) to evaluate the effect of bond strength on thermo-mechanical stability in heterogeneous 3D applications such as silicon-on-sapphire (SOS) process. Since large CTE differences between the substrate and the glue and between the two substrates lead to increases in residual thermal stress during bonding and thermal cycling processes, the bond strength may be negatively impacted. This effect can be evaluated and bond strength/CTE-mismatch relationships can be established.

Surface analyses of the fractured surfaces: The bond-breaking energy at the interface strongly affects the bond strength, as mentioned in chapter 5. To evaluate the effects of chemical bond structure and surface morphology on bond strength, quantitative surface analysis of the delaminated (fractured) surfaces after four-point bending tests may be helpful. X-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM) can be used to examine chemical compositions and surface roughness of the delaminated surfaces. These results can be compared with surfaces before wafer bonding to find the key parameters affecting bond strength due to changes in interfacial chemistry and surface morphology.

For example, in wafer pairs bonded using BCB, XPS scans are made on mating fracture surfaces of the failed specimens. To identify the debonding path, a broad XPS scan can be made of each mating fracture surface. Detailed scans are then made in regions of the spectra containing peaks of interest. In case of BCB, O, C, Si and N peaks

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can be examined for this purpose [75]. AFM scans can be used to examine average topographic profiles for the mating delaminated surfaces [75].

Evaluation of the effect of surface morphology of the glue-adjacent layer on bond strength: Change in surface morphology of the BCB-adjacent layers (substrates) will lead to change in the contact area and the extent of interlocking at the BCB interface and consequently, change in the bond strength of the BCB interface. It is important to evaluate the effect of surface morphology of glue-adjacent layer on bond strength because optimal surface morphology conditions for bonding process can be determined by these evaluations. Plasma treatment can generally be used to change the surface morphology [138-139]. For instance, plasma treatment of PECVD oxide layers bonded with BCB in the 3D IC integration process will change their surface. The plasma conditions, such as source power, flow of inlet gases and pressure, are key parameters to affect change in surface morphology. After changing the surface morphology, BCB can be bonded with the oxide layer and four point bending can be performed to evaluate the dependence of bond strength on surface morphology. Subsequently, optimal surface morphology conditions to maximize bond strength can be determined.

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APPENDIX A

Basic Concepts of Statistical Analysis

Data summary is often important to transform measured data into useful information. Furthermore, the conclusions about the corresponding process that created the data are important; that is, we might want to draw some conclusions about the long-term performance of a process based on only a relatively small number of sample data. Since only small number of samples are used to draw the conclusion, there is some uncertainty about that. However, when a probability model is specified for the sample analysis, the extent of uncertainty can be quantified and sample size can be selected or modified to achieve a tolerable level of uncertainty [89]. During the four point bending tests, there are two processes that need the data summary procedure.

(1) How to obtain precise saturation load value in load plateau region after each bending test.
(2) How to calculate the mean and standard deviation values about critical adhesion energy from the saturation load obtained from process 1.

Normalized standard deviation function is used for evaluating adequacy of the regression model as the statistics for process 1[89-90]. Residual analysis is used for evaluating adequacy of the regression model as the statistics for process 2 [89]. In this section, basic concepts for precise data summary are introduced and then in chapter 3.3.1.4, procedures for data acquisitions about process 1 and process 2 are explained.

Random Variables: in an experiment, a measurement is usually denoted by a variable such as X. In a random experiment, a variable whose measured value can change (from one replicate of the experiment to another) is referred to as a random variable [89]. In our experimental set, X is the critical adhesion energy measurement. The term "random" is to indicate that noise disturbances can change its measured value.

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When the interesting measurement is assumed to be a real number, it is possible for arbitrary precision in the measurement to be determined. In practice, it may be round off to the nearest tenth or hundredth of a unit. The random variable that represents this measurement is named as continuous random variable; on the other hand, whenever the measurement is limited to discrete points on the real line, the random variable is named as a discrete random variable. In some cases, the random variable X is actually discrete but, because the range of possible values is so large, it may be more convenient to analyze X as continuous random variables.

Normal Distribution: the most widely used model for distribution of a random variable is a normal distribution. Whenever a random experiment is replicated, the random variable that equals the average (or total) result over the replicates tends to have a normal distribution as the number of replicates becomes large. De Moivre first presented this result in 1733. But, his work was forgotten for some time, and Gauss independently developed a normal distribution nearly 100 year later. Although De Moivre was later credited with the deviation, a normal distribution is usually referred to as a Gaussian distribution [89].

The theoretical basis of a normal distribution is to justify the somewhat complex form of the probability density function and to calculate probabilities for a normal random variable. Random variables with different means and variances can be modeled by normal probability density function with appropriate choices of the center and width of the curve. The value $E(X)=\mu$ determines the center of the probability density function and the value of $V(X)= \sigma^2$ determines the width. The following definition provides the formula for normal probability density functions. From the definition, a random variable X with probability density function is expressed as:

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{\frac{-(x-\mu)^2}{2\sigma^2}} \qquad \text{for } -\infty < x < \infty \qquad \text{(A.1)}$$

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This is also called a normal distribution (normal random variable) with parameters μ and σ, where $-\infty<x<\infty$, and $\sigma>0$ under the condition $E(X)=\mu$ and $V(X)= \sigma^2$. The notation $N(\mu,\sigma^2)$ is often used to denote a normal distribution with mean μ and variance σ^2.

Some useful results concerning a normal distribution are described in Equations A.2, A.3 and A.4.

$$P(\mu-\sigma<x<\mu+\sigma)=0.6827 \quad (A.2)$$

$$P(\mu-2\sigma<x<\mu+2\sigma)=0.9545 \quad (A.3)$$

$$P(\mu-3\sigma<x<\mu+3\sigma)=0.9973 \quad (A.4)$$

By the symmetric feature of f(x), $P(x<\mu)$ is equal to $P(x>\mu)$ and the two probabilities have the same value of 0.5. Because f(x) is positive for all x, this model assigns some probability to each interval of the real line. However, probability density function decreases as x moves farther from μ. Consequently, the probability that a measurement falls far from μ is small, and at some distance from μ, the probability of an interval can be approximated zero. The area under a normal probability density function beyond 3σ from the mean is quite small. This fact is convenient for quick and rough sketches of a normal probability density function. The sketches help us determine probabilities. Because more than the probability of 0.9973 of a normal distribution is within the interval $(\mu-3\sigma, \mu+3\sigma)$, 6σ is referred to as the width of a normal distribution. Numerical integration can be used to show that the area under the normal probability density function from $-\infty < x < \infty$ is 1.

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APPENDIX B

Library of Bonded Wafer

[1] Si/Thermal SiO_2/AP/BCB (2.6 μm)/AP/Thermal SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 34 +/- 2.2, 6
- Load-plateau type: classical load-plateau shape, type 1
- Double layer BCB of baseline process thickness
- BCB and thermal oxide thicknesses: 2.6 μm and 2 μm
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  30th September 2002 ~ 13th October 2002.

[2] Si/Thermal SiO_2/AP/BCB (0.6 μm)/AP/Thermal SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 25 +/- 2.3, 6
- Load-plateau type: classical load-plateau shape, type 1
- Double layer of thin BCB
- BCB and thermal oxide thicknesses: 0.6 μm and 2 μm
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  30th September, 2002 ~ 13th October, 2002

[3] Si/PECVD SiO_2/AP/BCB (2.6 μm)/AP/PECVD SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 31 +/- 1.7, 6
- Load-plateau type: classical load-plateau shape, type
- Double layer BCB of baseline process thickness
- BCB and PECVD oxide thicknesses: 2.6 μm and 1 μm
- Thermal cycling: Yes (see the Tables 6.1, 6.2, and 6.3)
- Date for four point bending (w/o thermal cycle):
  15th September, 2002 ~ 29th September, 2002
- Date for four point bending (w thermal cycle):

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29th January, 2003 ~ 27th February, 2003

[4] Si/PECVD SiO_2/AP/BCB (0.6 μm)/AP/PECVD SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 24 +/- 1.7, 5
- Load-plateau type: classical load-plateau shape, type1
- Double layer of thin BCB
- BCB and PECVD oxide thicknesses: 2.6 μm and 1 μm
- Thermal cycling: Yes
- Date for four point bending (w/o thermal cycle):
  15th September, 2002 ~ 1st October, 2002
- Date for four point bending (w thermal cycle):
  29th January, 2003 ~ 12th February, 2003

[5] Si/PECVD SiO_2/AP/BCB (0.4 μm)/AP/PECVD SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 19 +/- 0.7, 7
- Load-plateau type: classical load-plateau shape, type1
- Single layer of thin BCB
- BCB and PECVD oxide thicknesses: 2.6 μm and 1 μm
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  17th October, 2002 ~ 3rd November, 2002

[6] Si/Native SiO_2/AP/BCB (2.6 μm)/AP/Native SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 30 +/- 1.4, 6
- Load-plateau type: classical load-plateau shape, type1
- Double layer BCB of baseline process thickness
- BCB and native oxide thicknesses: 2.6 μm and 1.4 nm
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  21th November, 2002 ~ 5th December, 2002

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[7] Glass/AP/BCB (7 μm)/AP/Native SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 17 +/- 0.6, 7
- Load-plateau type: classical load-plateau shape, type1
- Double layer of thick BCB
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  5th July, 2002 ~ 20th July, 2002

[8] Glass/AP/BCB (4.8 μm)/AP/Native SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 14 +/- 1.2, 7
- Load-plateau type: classical load-plateau shape, type1
- One thick BCB and one baseline thickness BCB
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  14th June, 2002 ~ 28th June, 2002

[8] Glass/AP/BCB (2.6 μm)/AP/Native SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 9 +/- 0.9, 7
- Load-plateau type: classical load-plateau shape, type1
- Double layer BCB of baseline process thickness
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  4th June, 2002 ~ 24th June, 2002

[9] Glass/AP/BCB (1.3 μm)/AP/Native SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 7 +/- 0.1, 7
- Load-plateau type: classical load-plateau shape, type1
- Single layer of BCB
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  10th June, 2002 ~ 24th June, 2002

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[10] Glass/AP/Flare (0.6 μm)/AP/Native SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 18 +/- 2.2, 5
- Load-plateau type: classical load-plateau shape, type1
- Double layer Flare of baseline process thickness
- Remaining rectangular samples (without notches): No
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  5th July, 2002 ~ 20th July, 2002

[11] Si/PECVD SiO_2/BCB (2.6 μm)/PECVD SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 13 +/- 0.5, 6
- Load-plateau type: classical load-plateau shape, type1
- Double layer BCB of baseline process thickness
- BCB and PECVD oxide thicknesses: 2.6 μm and 1 μm
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  17th October 2002 ~ 2nd November 2002.

[12] Si/PECVD SiO_2/BCB (0.4 μm)/AP/PECVD SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 10 +/- 0.4, 6
- Load-plateau type: classical load-plateau shape, type1
- Single layer of thin BCB
- BCB and PECVD oxide thicknesses: 2.6 μm and 1 μm
- Remaining rectangular samples (without notches): No
- Thermal cycling: No
- Date for four point bending (w/o thermal cycle):
  17th October 2002 ~ 3rd November 2002.

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[14] Cu/Oxide ILD/AP/BCB (2.6 μm)/ /Thermal SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 21+/- 1.9, 5
- Load-plateau type: classical load-plateau shape, type1
- Double layer BCB of baseline process thickness
- BCB and thermal oxide thicknesses: 2.6 μm and 2 μm
- Thermal cycling: Yes
- Date for four point bending (w/o thermal cycle):
  15th December, 2002 ~ 9th January, 2003
- Date for four point bending (w thermal cycle):
  8th January, 2003 ~ 23rd January, 2003

[15] Cu/Low-k ILD/AP/BCB (2.6 μm)/ /Thermal SiO_2/Si

- Critical adhesion energy (J/m^2) and number of samples: 6+/- 0.6, 5
- Load-plateau type: classical load-plateau shape, type1
- Double layer BCB of baseline process thickness
- BCB and thermal oxide thicknesses: 2.6 μm and 2 μm
- Thermal cycling: Yes
- Date for four point bending (w/o thermal cycle):
  15th December, 2002 ~ 9th January, 2003
- Date for four point bending (w thermal cycle):
  5th January, 2003 ~ 23rd January, 2003

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APPENDIX C

Publications from Research Program

Wafer Bonding Highlighted

1. "Wafer Bonding Using Low-K Dielectrics as Bonding Glues in Three-Dimensional Integration", Y. Kwon, J.-Q. Lu, R. J. Gutmann, R. P. Kraft , J. F. McDonald and T. S. Cale, in Semiconductor Wafer Bonding Science: Technology and Applications, H. Baumgart, C. E. Hunt S. Bengtsson, T. Abe, eds., ECS, PV 2001-27, 2001, pp. 145-154.

2. "Wafer Bonding Using Dielectric Polymer Thin Film in 3D Integration", Y. Kwon, J.-Q. Lu, R.P. Kraft, J.F. McDonald, R.J. Gutmann and T.S. Cale, in *"Polymer Interfaces and Thin Films"*, Ed. C.W. Frank, in MRS Symp. Proc. Vol. 710, pp. DD12.18.1-DD12.18.6, 2002.

3. "Evaluation of Wafer Bonding and Thinning for 3D-IC Fabrication", Y. Kwon, A. Jindal, J. J. McMahon, J.-Q. Lu, T.S. Cale, and R.J. Gutmann, in *4th International Conference on Microelectronics and Interfaces (ICMI'03)*, March 3-6, Santa Clara convention Center, Santa Clara, CA, March 3-6, 2003.

4. "Evaluation of Dielectric-Glue Wafer-Bonding for Three-Dimensional Integrated Circuits using Four-Point Bending Technique", Y. Kwon, J.-Q. Lu, R.J. Gutmann, T.S. Cale, in *Proceedings of MRS Spring Meeting*, San Francisco, CA, April, 2003.

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3D IC Highlighted

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