

**Semiconductor Wafer Bonding:
Science, Technology, and Applications VI**



**Edited by
H. Baumgart
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PV 2001-27

Semiconductor Wafer Bonding: Science, Technology, and Applications VI

Proceedings of the International Symposium

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Sponsoring Division:
Electronics

Proceedings Volume 2001-27



THE ELECTROCHEMICAL SOCIETY, INC.
65 South Main St., Pennington, NJ 08534-2839, USA

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Published by:

The Electrochemical Society, Inc.
65 South Main Street
Pennington, New Jersey 08534-2839, USA

Telephone 609.737.1902
Fax 609.737.2743
e-mail: ecs@electrochem.org
Web: www.electrochem.org

Library of Congress Catalogue Number: 2002111865

ISBN 1-56677-360-1

Printed in the United States of America

PREFACE

The Sixth International Symposium on Semiconductor Wafer Bonding: Science, Technology and Applications was held in September 2001 in San Francisco as part of the 2001 Fall Meeting of the Electrochemical Society. The tradition of this bi-annual symposium was started at the 1991 ECS Meeting in Phoenix. The lively interest in this field, the on-going research and innovation and a steadily growing number of novel contributions and commercial breakthroughs have sustained the growth of the symposium in 1993 at the ECS meeting in Honolulu, in 1995 in Reno, in 1997 in Paris, in 1999 in Honolulu and in 2001 in San Francisco. As a further sign of recognition and maturity, interest in this field has grown to the extent that we have seen the emergence of several competing conferences devoted to this topic just within the year 2001.

The field of Wafer Bonding originated from Silicon-on-Insulator (SOI) research. Over the years Wafer Bonding has actively contributed to progress in SOI and has also received major impulses from breakthroughs and advances in SOI. The multifaceted possibilities of layer splitting technologies continue to captivate the Bonding Community. Three invited talks were devoted to this topic in the Exfoliation and Layer Transfer Session, and two of them explored non SOI opportunities and non-standard systems, true to the tradition of this symposium. The innovation and technological success of Exfoliation and Layer Transfer Technologies combined with commercial maturity provide testimony of the vitality of this specialty field. It was always a hallmark of Wafer Bonding that the intriguing possibilities of Bonding Technology fostered multiple applications beyond SOI, and enabled the fabrication of novel composite material systems. Such heterostructure composites were unattainable prior to the ascend of Wafer Bonding techniques with their rapidly developing learning curve. This proceedings volume demonstrates again the broad potential of bonding techniques by presenting applications in a range of very diverse fields. At this symposium the questions of plasma treatments prior to bonding and low temperature plasma assisted bonding loomed large in the sessions on Fundamental Wafer Bonding Mechanisms and Low Temperature UHV Bonding. A number of papers were devoted to this issue. The Novel Bonding Sessions had several papers focusing on 3-D integration issues, while the Bonded Heterostructure Session dealt with GaN FETs and opto electronics. Anodic Bonding and Fusion Bonding retains its special value for microelectromechanical systems (MEMS) applications and was well represented in that session. Over the past years Wafer Bonding has passed the important litmus test of producing commercially viable applications. Today bonded wafers and special clean room tools for wafer bonding are commercially available from several manufacturers and we are seeing an increasing number of semiconductor companies designing and fabricating high end products with bonded wafer material.

We would like to acknowledge the Electrochemical Society for providing the organizational support for this symposium. The success of the 6th Semiconductor Wafer Bonding Symposium is due primarily to the participants from the international Wafer Bonding Community. We express our appreciation and special thanks to all the authors presenting novel research results and the invited speakers, who also graciously served as Session Chairmen. We look forward to continue this tradition and anticipate to review the progress in this field at the 7th International Symposium on Semiconductor Wafer Bonding Science, Technology and Applications to be held jointly with the SOI Symposium at the Electrochemical Society Meeting in Paris, France from April 27 to May 2, 2003.

Austin, Texas
Spring 2002

Helmut Baumgart
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Stefan Bengtsson
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The Electrochemical Society (ECS) is an international, nonprofit, scientific, educational organization founded for the advancement of the theory and practice of electrochemistry, electrothermics, electronics, and allied subjects. The Society was founded in Philadelphia in 1902 and incorporated in 1930. There are currently over 7,000 scientists and engineers from more than 70 countries who hold individual membership; the Society is also supported by more than 100 corporations through Contributing Memberships.

The technical activities of the Society are carried on by Divisions and Groups. Sections of the Society have been organized in a number of cities and regions. Major international meetings of the Society are held in the spring and fall of each year. At these meetings, the Divisions and Groups hold general sessions and sponsor symposia on specialized subjects.

The Society has an active publications program that includes the following:

Journal of The Electrochemical Society — The *Journal* is the peer-reviewed leader in the field of electrochemical and solid-state science and technology. Articles are posted online as soon as they become available for publication. This archival journal is also available in a paper edition, published monthly following electronic publication.

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Interface — *Interface* is ECS's quarterly news magazine. It provides a forum for the lively exchange of ideas and news among members of ECS and the international scientific community at large. Published online (with free access to all) and in paper, issues highlight special features on the state of electrochemical and solid-state science and technology. The paper edition is automatically sent to all ECS members.

Meeting Abstracts (formerly *Extended Abstracts*) — Meeting Abstracts of the technical papers presented at the spring and fall Meetings of the Society are published in serialized softbound volumes.

Proceedings Series — Papers presented in symposia at Society and topical meetings are published as serialized Proceedings Volumes. These provide up-to-date views of specialized topics and frequently offer comprehensive treatment of rapidly developing areas.

Monograph Volumes — The Society sponsors the publication of hardbound Monograph Volumes, which provide authoritative accounts of specific topics in electrochemistry, solid-state science, and related disciplines.

For more information on these and other Society activities, visit the ECS website:

www.electrochem.org

WAFER BONDING USING LOW-K DIELECTRICS AS BONDING GLUES IN THREE-DIMENSIONAL INTEGRATION

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ABSTRACT

We discuss 200-mm wafer bonding using polymers as dielectric bonding glue - a critical process for our approach to monolithic wafer-scale 3D integration of chips. After discussing the requirements for polymeric adhesives for this application, some wafer bonding procedures and results are presented for experiments in which silicon wafers are bonded to glass wafers. Compared with other glues, the pairs of wafers bonded using Flare and BCB show a larger fraction of bonded area. Flare also results in higher bond strength, as determined using the razor blade test, and good bonding integrity, as indicated by the results of thermal cycling and backside grinding experiments.

INTRODUCTION

Signal delays caused by interconnect parasitics are becoming more significant in terms of limiting overall circuit speed as faster devices are developed and the system integration scale increases. Statistical models derived for wire length distributions for integrated circuits show that the vast majority of them are quite short. Only a small portion, perhaps 10%, accounts for 90% of the total wire length in the chip. Since these long wires currently limit performance of modern high performance circuits, due to a combination of resistance and capacitance, any approach to reducing interconnect delay must address this long-wire limitation. Several mathematical treatments have been used to demonstrate that 3D chip integration can greatly reduce the length of long wires [1-2]. Approaches to 3D integration at either the chip [3-5] or wafer level [6-12] have been presented. They can be considered as either packaged chip or full wafer approaches (or perhaps hybrids).

Wafer bonding technology using low-k dielectrics as bonding glues is an attractive approach to 3D integration; i.e., bonding more than one processed wafers or IC chips. This 3D technology may alleviate future Cu/low-k interconnect bottlenecks and help overcome fabrication and performance limitations of future generations of planar ICs [7]. In addition, highly integrated systems may be realized utilizing this 3D wafer bonding approach, e.g., hard intellectual property (IP) core-based implementations, high-speed synchronous digital systems such as application specific ICs (ASICs) or system-on-a-chip (SOC), as well as heterogeneous systems, such as microsystems, smart sensors, optoelectronics, and wireless technologies [13].

Figure 1 illustrates in simplified pictorial fashion our concept of 3D chip integration by wafer to wafer bonding [14]. This concept is not only a technique for shortening wires, but also an approach to heterogeneous wafer integration. Wafers combined using this

approach can be fabricated by different processing steps (within the same materials system) or with different wafer materials. In this way, for example, a wafer optimized for DRAM processing could be combined with a wafer optimized for logic, or a wafer that has a heterostructure capable of emitting or detecting light or THz radiation. The only requirement is that the wafers are of the same diameter with the matched inter-wafer interconnection scheme. The 3D integration approach indicated by Fig. 1 does not limit the number or type of wafers that can be stacked together. Wafers (including non-Si wafers) can be attached for the fourth and subsequent levels. Therefore, this scheme offers the benefits of significantly reduced interconnect delays, as well as system integration to increase both the performance and functionality. The use of optimized processing technology on separate wafers for implementations of ASICs/SOCs or heterogeneous systems also offers the potential of reducing processing complexity, increasing the yield and cutting the packaging steps, thus lowering the overall cost.

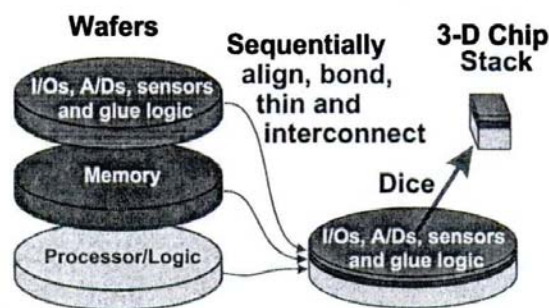


Fig. 1. Three dimensional chip stacking by monolithic wafer bonding and thinning.

The concept presented here is not meant as a replacement for single wafer integration, but as an interface between conventional back-end-of-the-line (BEOL) processing and high-performance first-level packaging. Many fabrication challenges exist in this process flow, and numerous alternative unit process steps are under study [6-18]. A quantitative method for evaluating inter-wafer via design rules, yield, via resistance, and overall reliability and integrity for the structure with these variants is required. In this paper, we discuss our 3D integration efforts that use wafer bonding technology with a dielectric glue as the bonding adhesive. Requirements for polymeric adhesives for this application are described. Results with FlareTM and BCB are presented in detail and serve as a baseline for alternative adhesives.

3D WAFER-SCALE INTEGRATION AND PROCESSING FEASIBILITY

Figure 2 shows a schematic of our 3-D integration concept that uses wafer bonding [6]. It represents three wafers with ICs bonded together, either face-to-face (second to first level) or face-to-back (third to second level). Device surfaces and multilevel interconnects are also depicted in the figure. Dielectric glue layers are used to enhance bonding adhesion. High aspect ratio (HAR) vias (plug- and bridge-type) replace the long distance interconnects found in conventional planar ICs. Initially two wafers are aligned and bonded face-to-face (or interconnect structure-to-interconnect structure). The top wafer is thinned to ~10 μm and planarized, followed by an inter-wafer interconnection using copper damascene patterning including HAR etching and via fill.

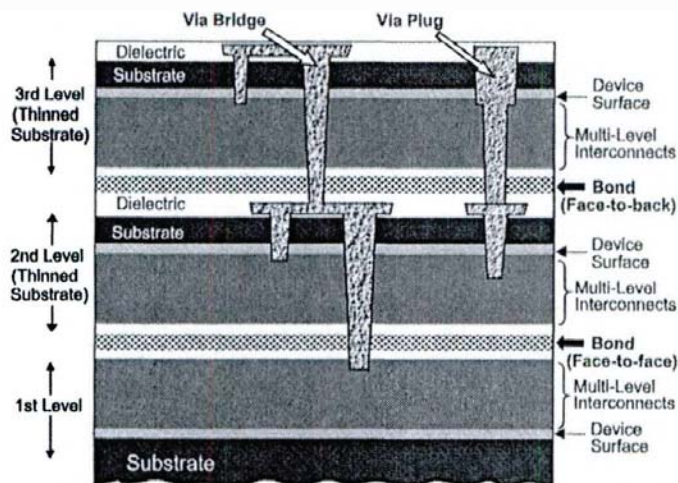


Fig. 2. 3D integration concept using wafer-bonding, showing dielectric glue layers as bonding interface, vertical high-aspect-ratio vias (plug- and bridge-type), and bonding approaches of "face-to-face" and "face-to-back".

Essential for the success of any 3D process will be inter-wafer via yield. A direct way to test this is with via-chain test structures as used in ordinary 2D chips. A via-chain test structure has been designed and is in hot-lot fabrication to demonstrate the technological feasibility and establish design rules for 3D integration. Four key process issues have to be addressed [6]: wafer alignment, bonding, thinning and inter-chip interconnection vias. Each of these four processes must be compatible with conventional BEOL processes and with final packaging processes. Among them, the wafer bonding is one of the key processes and is discussed in next section.

To maximize the potential circuit performance improvements using the 3D approach described, the wafer alignment accuracy must be in the range of the BEOL dimensions (microns). An Electronics Visions Group (EVG) EV640 SmartView™ Aligner is used to provide 1-2 μm alignment accuracy with 200-mm wafers, as has been demonstrated in our laboratory [8]. Inter-chip vias with small diameters and short lengths are also required. Thus, the backside of the top wafer must be thinned to under $\sim 10\ \mu\text{m}$ and leveled subsequent to the wafer bonding. We have thinned to 60 μm with good bonding integrity results, but bonding defects and inter-wafer edge effects presently prevent thinning to the desired 10- μm range. We are exploring several options for wafer thinning [17].

Damascene patterning with HAR via etching, subsequent metallization, and chemical-mechanical planarization (CMP) provide the contact between the ICs on the wafers. Our CMP results satisfy our requirements for the via-chain test structure fabrication, including the flat surface for wafer bonding, although full wafer-scale planarity remains to be evaluated [14, 17]. Our capability for HAR via etch and fill, and for liner fill, using 200-mm wafer tools has been discussed [7,8]. For via-chain test structures the via must penetrate through at least three different materials, some more than once, including Si,

SiO₂ or other low-k dielectric, and the adhesive layer. A collaborative research partner, the Institute for Advanced Materials at the U. at Albany, has demonstrated the RIE capability for Si, SiO₂, Si, SiN_x, and Flare, both in blanket film stacks and in patterned test structures with 200-mm wafers [18].

RESULTS AND DISCUSSIONS OF WAFER BONDING USING DIELECTRICS

While any new integration concept has technological challenges, a key challenge of our wafer-scale monolithic 3D integration is wafer bonding. Wafer bonding of fully processed 200-mm wafer requires intimate contact over the entire wafer, and compatibility with both conventional BEOL processes and subsequent thinning and inter-chip interconnection. Most wafer bonding processes currently involve high temperatures, high voltages and/or high pressures. Therefore, it is especially challenging to directly bond 200-mm wafers, on which ICs with several interconnect metal levels have been fabricated. Our approach to wafer bonding using low-k dielectric polymer glues does not involve very high temperatures, very high pressures or electrical biases; the required processes are compatible with conventional IC fabrication.

The polymeric glue layer must provide a seamless interface and strong adhesion to prevent delamination, be sufficiently thin to minimize the via aspect-ratio, be processed at modest temperatures to avoid any effects on the device wafer performance and reliability, and be thermally and mechanically stable after bonding. The desirable properties of the bonding glue include: (1) good adhesion and cohesion - glue to wafer (adhesion), and glue to glue (cohesion), to prevent delamination; (2) no outgassing during bonding to avoid void formation; (3) high thermal and mechanical stability over the ranges of BEOL and packaging processing conditions; i.e., a high glass transition temperature and rigid structure after bonding; (4) CTE well-matched to that of substrates; (5) low stress relaxation and creep; and (6) low moisture uptake. The candidates for bonding glue currently under evaluation at Rensselaer are spin-on amorphous polymers, such as Flare (Poly aryl ether) [19], methylsilesequioxane (MSSQ) [20], benzocyclobutene (BCB) [21], and hydrogensilsesquioxane (HSQ) [22], as well as a vapor deposited polymer Parylene-N [23]. They can be deposited as thin films, have relatively well-known chemical and physical properties, and are cleanroom process compatible. In addition, these materials meet our bonding requirements to some extent and are compatible with IC processing.

The bonding protocol largely consists of three main steps: preparation of the glue layers, wafer contact and wafer bonding. For spin-on polymer materials (Flare, MSSQ, BCB and HSQ), the glue layers are prepared as follows: (1) spin dispense polymeric material using a FlexiFabTM Coat Bake System and (2) pre-bake to remove solvents, volatile impurities and water vapor due to the condensation reaction, to improve the degree of surface planarization (re-flow, e.g., MSSQ), and/or to harden the glue surface. Parylene-N was deposited using a SCS multi-wafer deposition system (PDS 1050) with a dimer (di-*p*-xylyene). Vapor deposition of Parylene-N is a solvent-free dry process without outgassing, and a very uniform film is obtained.

Wafer contact and bonding are conducted using an EVG EV501 wafer bonder. Two wafers with glue layers are placed glue-to-glue, separated by three "flags", and clamped by two clamps on a bonder chuck, as illustrated in Fig. 3. The bonder-chuck is then loaded into the EV501 bonding chamber, which is pumped down to approximately 10^{-4} mbar. The bonder chuck is heated to a given temperature while the mechanical spacers (flags) keep the wafers physically separated. The bond is started by pressing in the middle of the top wafer to create an initial point of contact, while allowing wafer flags to be removed, a "wafer-bow" process depicted in Fig. 3a. Upon removal of the flags (Fig. 3b), a uniform bonding down pressure is applied over the wafer pair. The wafer pair is then further heated to complete the bonding process. Finally, the wafers are slowly cooled and unloaded. The maximum processing temperature for the wafer bonding is 400 °C, compatible with both conventional BEOL processes and subsequent inter-chip interconnection and packaging processes.

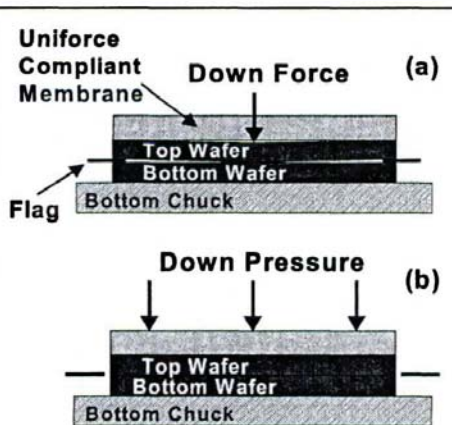


Fig. 3. Schematic of bonding process: a. initial application of down force. b. after flags removed.

In the 3D integration process, the processed wafers are first aligned in the EVG EV640 prior to loading in the bonder chamber. Therefore, the flags are important to separate the two wafers and prevent any gas trapping (e.g., in the rough surface or wafer bow) between the wafers before and during the bonding processes. The down force is applied to remove any gaps between the glue layers on the top and bottom wafers, and to facilitate the cross-link reaction. Curing (the cross-link network formation or the intermixing of polymer chains) is the defining step of wafer bonding, i.e., it provides the bond between the two wafers. A holding time is needed during the bonding process to form a complete cross-linked network. A slow cool down process is crucial to minimize debonding due to stresses generated by CTE differences between polymer and wafers.

After bonding, visual inspection is used to evaluate alternative glues and process conditions. The bond strength is evaluated qualitatively using a razor blade to attempt to separate the wafers. Our experiments show that the fraction of bonded area and the bond strength depend on the process temperature, the applied pressure and the pressure vs. time protocol. Particles and defects also influence the bonding results.

Figure 4 shows a photo of bonded wafers (200-mm Corning 7740 glass wafer to p-type (100) prime silicon wafer) using Flare. Figure 5 shows a photo of a bonded wafer pair (Corning glass to silicon wafer) using BCB. While the quality is quite good, some issues related to the bonding are: (1) void generation due to outgassing of the remaining solvent or by-product created during the curing process; (2) void or bonding defect generation due to particles or polymer structural defects; (3) and wafer bow caused by mechanical stress.

As can be seen from Figs. 4 and 5, large void-free bonded areas are obtained for both Flare and BCB. However, there are some distinct differences. The first difference is the appearance of void or bonding-defect structures. There are at least two possible reasons: glue thickness and reflow performance. Glue films were spun on both wafers of the bonded pair. The glue thickness after final baking was 0.33 μm for Flare film, and 1.43 μm for BCB. Small particles on the wafer surface are more likely to be buried by the thick BCB film than the thinner Flare film. The polymer resins of BCB can reflow more than Flare since the BCB is more crosslinked [19, 21]. Active reflow of the BCB can fill the empty spaces around particles. Proof of the good reflow property of BCB is the change of edge bead area during bonding. In the spin-on process, the glue on the wafer edge-bead was removed. The edge bead of bonded pair using Flare did not change much during wafer bonding (see Fig. 4), but that using BCB almost disappeared during bonding (see Fig. 5). We attribute the post-bonding difference in edge beads, at the same bonding pressure, to better reflow of BCB. Therefore, the bonding defects with Flare in Fig. 4 may be mainly due to particles, but those with BCB in Fig. 5 may be mainly due to polymer structural defects. Further study is needed. Another major difference is the thermal stability temperature of the bonded pair: 350 $^{\circ}\text{C}$ for BCB and greater than 400 $^{\circ}\text{C}$ for Flare, respectively, according to the polymer properties provided by the manufacturers. Therefore, Flare is a more attractive glue for a BEOL-compatible wafer bonding process.

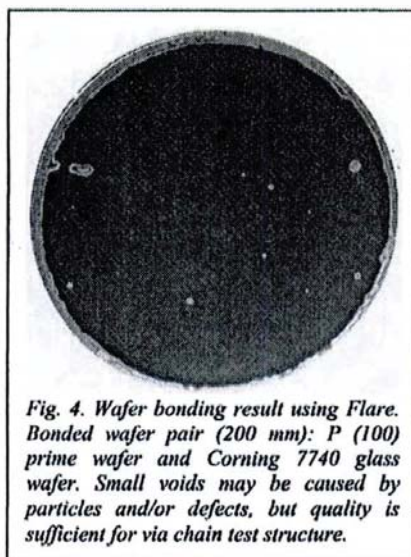


Fig. 4. Wafer bonding result using Flare. Bonded wafer pair (200 mm): P (100) prime wafer and Corning 7740 glass wafer. Small voids may be caused by particles and/or defects, but quality is sufficient for via chain test structure.

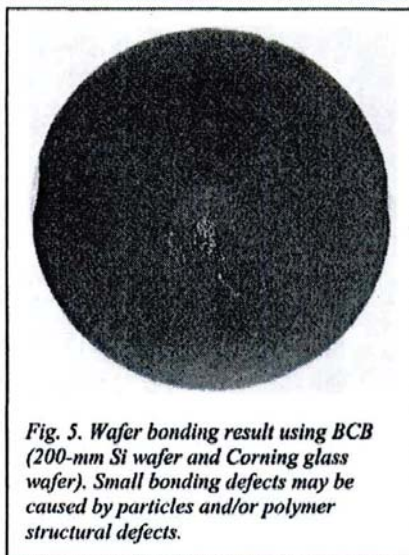


Fig. 5. Wafer bonding result using BCB (200-mm Si wafer and Corning glass wafer). Small bonding defects may be caused by particles and/or polymer structural defects.

Some of the bonded pairs with Flare underwent a thermal cycle test and a mechanical stress test in order to evaluate the bonding integrity. The bonded wafer pairs using Flare show little change in defect structure after thermal cycling to 400 $^{\circ}\text{C}$ or after top-wafer thinning (by grinding and CMP) to 60 μm , as depicted in Fig. 6. Both thermal cycling and thinning to 60 μm have little effect on the structure of the bonding interface.

Flare is a non-fluorinated poly aryl ether, that is manufactured by Honeywell Inc. The high degree of cross-linking during the curing process increases both film rigidity and thermal stability. The cross-link network results in strong adhesion of Flare to itself and to most surfaces of the wafer (e.g., silicon and ILD surfaces). Thus, Flare is an attractive bonding glue that results in a larger fraction of bonded area and higher bond strength

compared to alternative glues tested to date (such as MSSQ and parylene [16]). A remaining concern is outgassing during bonding; therefore, a baking process must be developed to completely remove the solvent or by-product before wafer bonding.

BCB (CYCLOTENE resin) is manufactured by Dow Chemical. It is very rigid due to extensive crosslinking and low water uptake. The crosslinking reaction starts from opening side rings of arylcyclobutenes, the end group of BCB monomer. Opened side rings produce an orthoxylylene moiety as a reactive intermediate, which is a diene structure. Such diene groups react with dienophile like vinyl group thermally in the range of 150-300 °C through Diels-Alder reaction. The main concern is to develop a process to completely cure BCB films.

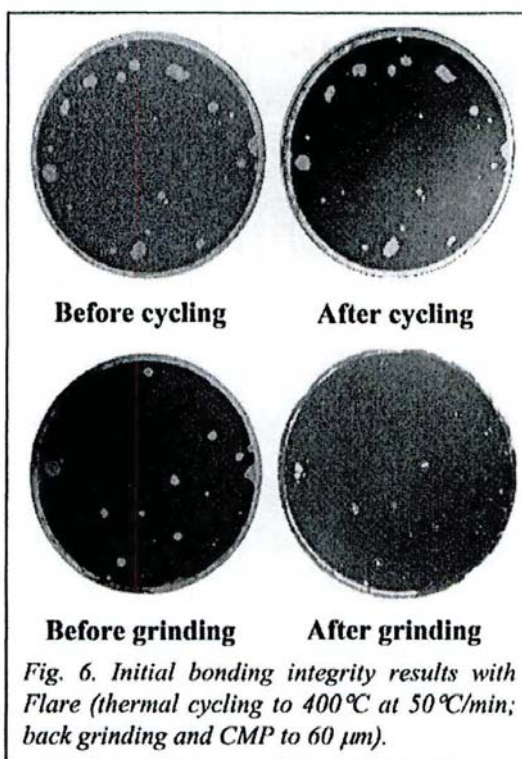


Fig. 6. Initial bonding integrity results with Flare (thermal cycling to 400 °C at 50 °C/min; back grinding and CMP to 60 μm).

In order to understand the bonding mechanism, Fourier Transform Infrared Spectroscopy (FTIR) was used. Figures 7 and 8 show the FTIR spectra for Flare and BCB films on prime silicon wafers, respectively. As shown in Fig. 7, the Flare FTIR spectra indicates that the "as spun" sample has five main peaks at wavenumbers of 3050 cm^{-1} (C-H stretch of phenyl group), 2930 cm^{-1} (C-H stretch), 1700 cm^{-1} (C=O carbonyl group), 1650 cm^{-1} (C=O stretch of benzophenone moiety), 1590 cm^{-1} (aromatic C=C), 1500 cm^{-1} (asymmetric ether stretch) and 1240 cm^{-1} (symmetric ether stretch) [19]. This spectrum confirms the presence of cyclohexanone solvent in Flare, because cyclohexanone consists of two C-H groups and a carbonyl group. However, solvent (cyclohexanone) peaks (C-H and C=O bonds) disappear after proper baking steps up to 250 °C. No difference is observed in the FTIR peaks between after-baking and after-curing of Flare deposited on a prime Si wafer. These results suggest the complete removal of solvent or by-product caused by reactions after such a bake process. Therefore, outgassing should not occur during bonding with this bake process and the main source for the void formation may be attributed to particles.

As shown in Fig. 8, the BCB FTIR spectrum of the sample before bonding shows a typical result for BCB monomer structure [24]: vinyl stretch structure peak (2926 cm^{-1}), vinyl wag structure peaks (1194 and 985 cm^{-1}), benzene side ring stretch peak (1473 cm^{-1}), siloxane group peak (1049 cm^{-1}), and Si-methyl structure peak (1250 cm^{-1}). After the bonding process (one hour at 250 °C), the vinyl stretch and wag groups and benzene side ring peaks disappear, tetralin peak (1500 cm^{-1}) is strengthened and an aliphatic C-H

peak (3005 and 2925 cm^{-1}) is produced. This result indicates that BCB monomers are crosslinked fully (cured completely) during the wafer bonding process.

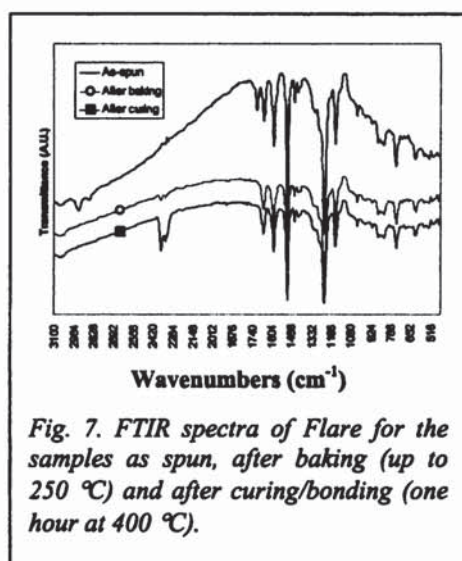


Fig. 7. FTIR spectra of Flare for the samples as spun, after baking (up to 250 °C) and after curing/bonding (one hour at 400 °C).

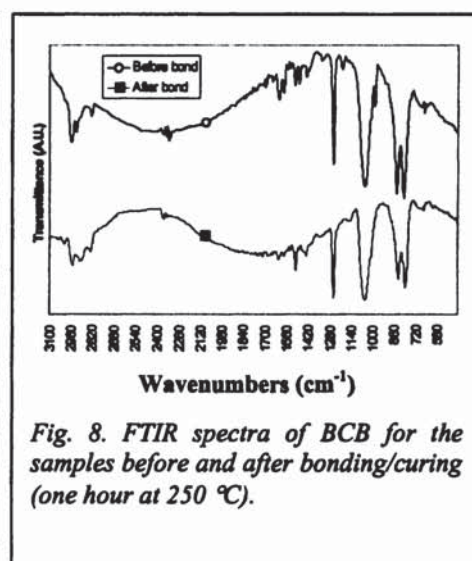


Fig. 8. FTIR spectra of BCB for the samples before and after bonding/curing (one hour at 250 °C).

SUMMARY AND CONCLUSION

Wafer bonding is one of the key processes in our approach to monolithic 3D integration, which offers a novel technology platform for high performance ICs and heterogeneous system integration with the potential of lowering the cost. We demonstrated 200-mm wafer bonding using two polymers for a dielectric bonding glue. This wafer bonding process is compatible with both conventional BEOL processes and subsequent inter-chip interconnection and packaging processes. Compared with other glues, the pairs of wafers bonded using Flare and BCB show a larger fraction of bonded area. Flare also results in higher bond strength as determined using the razor blade test, and good bonding integrity as determined using a thermal cycle test and wafer grinding and CMP (latter tests not completed for BCB at this time). FTIR analyses also provided valuable insight into the bonding mechanism. More detailed thermal, mechanical and spectroscopic analyses of the bonding glue are needed to understand the wafer bonding mechanism using polymeric glues.

ACKNOWLEDGEMENTS

This work is supported by DARPA, MARCO and NYSTAR through the Interconnect Focus Center for Gigascale Integration. We acknowledge the contributions of other 3D program participants at Rensselaer (J. McMahon, G. Rajagopalan, M. Gupta, D.L. Bae, C.K. Hong, and the cleanroom staff) and at the University at Albany (J. Castracane, E.T. Eisenbraun and B. Xu).

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