

Low-Temperature Wafer-Level Transfer Bonding

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Abstract—In this paper, we present a new wafer-level transfer bonding technology. The technology can be used to transfer devices or films from one substrate wafer (sacrificial device wafer) to another substrate wafer (target wafer). The transfer bonding technology includes only low-temperature processes; thus, it is compatible with integrated circuits. The process flow consists of low-temperature adhesive bonding followed by sacrificially thinning of the device wafer. The transferred devices/films can be electrically interconnected to the target wafer (e.g., a CMOS wafer) if required. We present three example devices for which we have used the transfer bonding technology. The examples include two polycrystalline silicon structures and a test device for temperature coefficient of resistance measurements of thin-film materials. One of the main advantages of the new transfer bonding technology is that transducers and integrated circuits can be independently processed and optimized on different wafers before integrating the transducers on the integrated circuit wafer. Thus, the transducers can be made of, e.g., monocrystalline silicon or other high-temperature annealed, high-performance materials. Wafer-level transfer bonding can be a competitive alternative to flip-chip bonding, especially for thin-film devices with small feature sizes and when small electrical interconnections ($< 3 \times 3 \mu\text{m}^2$) between the devices and the target wafer are required. [647]

Index Terms—Adhesive bonding, benzocyclobutene (BCB), device transfer, film transfer, integration, transfer bonding.

I. INTRODUCTION

FOR MANY applications, including sensor and actuator systems, radio-frequency devices, optical transducers, and three-dimensional integrated circuits, transferring devices from the original substrate wafer (sacrificial device wafer) to a new substrate wafer (target wafer) is desired. This can be beneficial, e.g., if devices shall be processed on both the front and back side, if a different substrate material than the original one is needed, or if the devices shall be integrated with integrated circuits (ICs). In the latter case, electrical interconnections between the ICs and the devices must be established.

One of today's standard integration technologies is monolithic integration. This means that the devices are directly processed on the substrate (e.g., a CMOS circuit). Therefore, the processing of the transducers is limited to temperatures below 450 °C and all transducer processing and design must be compatible with the CMOS circuit. Besides leading to more complex processing, many high-performance processes and materials used to fabricate transducers are excluded. Flip-chip bonding is another technology commonly used to integrate transducers and

ICs on chip level [1], [2]. However, flip-chip bonding involves relatively high costs (e.g., due to chip-level integration) and a limited ability to miniaturize the contact bumps and, in turn, the transducer unit. An alternative that is related to flip-chip bonding is wafer-to-wafer transfer of microstructures using gold bump compression bonding [3]. Thin-film layers have been transferred from the original substrate to highly electrically insulating glass substrates by gluing the two substrates together and subsequently thinning the original substrate. These techniques use relatively thick glue layers ($\geq 20 \mu\text{m}$) or glue layers that are supplied in the form of a resin drop, which results in an initially undefined glue layer thickness [4], [5]. Epoxy glues that require ultraviolet light for curing have also been used in these techniques [6], [7]. Thus, one of the two substrates has to be transparent for ultraviolet light. None of the mentioned techniques includes electrical interconnections between the transferred films and the new substrate, as opposed to our technique. A sacrificial wafer bonding technique using negative photoresist has been applied for planarization of deep holes or grooves [8]. A chip-level polyimide bonding technique has been described with which III–V films can be transferred from a GaAs substrate to a CMOS chip for integration of photonic and electronic circuits [9].

This paper describes a new, universal IC-compatible transfer bonding technology. In contrast to most other hybrid integration technologies, transfer bonding can be realized with excellent yield on wafer level, which makes it a cost-effective process. A wide range of different transparent and nontransparent wafer materials can be used. Unlike competing integration technologies, transfer bonding allows the transfer of completely (or partly) processed thin-film devices with very small feature sizes ($< 2 \mu\text{m}$) and very small electrical interconnections ($< 3 \times 3 \mu\text{m}^2$) between the devices and the target wafer. The main advantage of transfer bonding is that the sacrificial device wafer and the target wafer (e.g., a CMOS wafer) can be processed and optimized in separate processes. In a subsequent integration step, the devices are transferred to the target wafer. Then the devices are electrically interconnected to the target wafer if required. The transfer bonding technology consists of several steps. First, the sacrificial device wafer and the target wafer (e.g., a CMOS wafer) are aligned and bonded to each other with a specially developed high-yield low-temperature adhesive bonding technology [10], [11]. Second, the device wafer is sacrificially etched while the devices remain on the target wafer. If required, electrical interconnections between the devices and the target wafer are processed. For 10-cm-diameter wafers, we have demonstrated a 3- μm bond alignment accuracy. We also have demonstrated the processing of electrical interconnections between devices and the target wafer that are 1.7 μm wide with a contact resistance of about 8 Ω .

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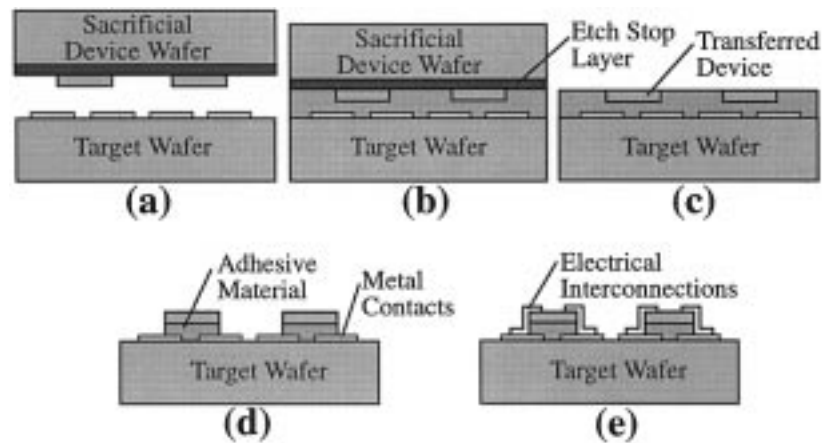


Fig. 1. Process flow for device transfer bonding.

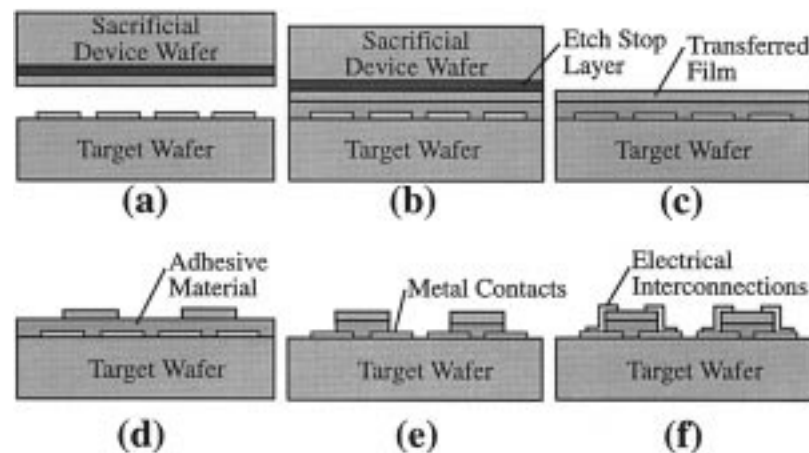


Fig. 2. Process flow for film transfer bonding.

II. TRANSFER BONDING

In this paper, we present device transfer bonding, film transfer bonding, and a combination of device and film transfer bonding. Fig. 1 shows a schematic drawing of the process flow for transfer bonding of devices and Fig. 2 shows a schematic drawing of the process flow for transfer bonding of films, including subsequent processing of the transferred films. It is possible to fabricate electrical interconnections between the transferred devices/films and the target wafer.

For device transfer bonding, the devices are processed on a sacrificial device wafer on top of a film, which acts as an etch-stop layer during sacrificial etching of the wafer (e.g., SiO_2 in the case of Si etching). If the bonding material and the devices themselves can withstand the applied etching procedure, the etch-stop layer is not required. After aligning the sacrificial device wafer and the target wafer (e.g., a CMOS wafer), the two wafers are bonded with a low-temperature polymer bonding technique (see Section II-A). In a next step, the device wafer is sacrificially thinned down to the etch-stop layer (see Section II-B). After removing the etch-stop layer and etching through-holes in the polymer material, electrical interconnections can be processed between the devices and the target wafer (see Section II-C).

For film transfer bonding, a film is deposited on top of an etch-stop layer on a sacrificial device wafer. If the film material can withstand the applied etching procedure used for re-

moving the sacrificial device wafer, the etch-stop layer is not required. The sacrificial device wafer can now be bonded to a target wafer (e.g., a CMOS wafer) with a low-temperature adhesive bonding technique (see Section II-A). In a next step, the sacrificial device wafer is thinned down to the etch-stop layer (see Section II-B). After removing the etch-stop layer, the transferred film can be patterned. Optionally, through-holes can be etched in the polymer material, and electrical interconnections between the target wafer and the film can be processed in a subsequent step (see Section II-C).

To transfer bond more complex devices, it may be advantageous to use a combination of device transfer bonding and film transfer bonding. For example, a sandwich of several patterned and unpatterned materials can be transferred from the sacrificial device wafer to the target wafer (see the example device in Section III-C).

A. Adhesive Wafer Bonding

Adhesive bonding is used for the transfer bonding technique presented in this paper. The advantages of using adhesive bonding are as follows.

- 1) Adhesive bonding is a low-temperature process and thus IC compatible.
- 2) Various wafer substrate materials can be joined.

- 3) Adhesive bonding is capable of bonding wafers with protruding structures.
- 4) Adhesive bonding is fast, low cost, and easy to apply and gives a high yield bond interface.

In this work, we used benzocyclobutene (BCB), a polymer material from Dow Chemical, as the adhesive bonding material. BCB is a standard material in the electronics industry and produces high-quality void-free bonds [10], [11]. Furthermore, it can withstand typical metal wet-etching processes, most organic solvents, and several hours at moderate temperatures in acid and alkaline baths [12]. BCB can withstand temperatures as high as 350 °C. Chemical and thermal stability of the bonding material is important to allow subsequent processing of the transferred films/structures (e.g., lithography, sputtering, etc.). The minimum required curing temperature for BCB is approximately 180 °C, and the thickness of the BCB bonding layer can be chosen to be in the range between 0.8 and 20 μm . Table I shows the material properties of cured BCB films.

Using BCB as the adhesive bonding material results in a high yield transfer process and a very high bond strength between the transferred devices/films and the target wafer [11]. In principle, other adhesives like negative photoresist can also be used as the bonding material for the transfer bonding technology. It is important that the bonding results in void-free and low-stress bond interfaces [11], [13]. A typical bonding procedure using BCB as the adhesive bonding material is given below.

- 1) Rinse and dry the wafers.
- 2) Apply the adhesion promoter AP8000 to both wafers.
- 3) Spin-coat a BCB film on the target wafer.
- 4) Pre-cure the BCB film on a hotplate at 65 °C for 5 min.
- 5) Align the two wafers in a bond aligner and join them in the vacuum environment of a bonder.
- 6) Cure the BCB at 250 °C for 60 min while applying a pressure of 1.7–2 bar using the bond chuck.

Pre-curing is needed to evaporate the solvents from the polymer before the bonding. The bonding time and temperature arise from the curing requirements of the polymer. The bonding pressure is needed to bring the two wafers in close contact and to press the device structures of the sacrificial device wafer into the polymer material. For the alignment and bonding, we have used a commercially available BA6 bond aligner and an SB6 bonder from Karl Suss¹ [14]. The specified alignment accuracy of the equipment is 3 μm for 10-cm-diameter wafers.

B. Sacrificial Wafer Thinning

The thinning of the sacrificial device wafer can be done in several ways. In our investigations, we have used deep reactive ion etching (DRIE) and KOH etching to thin down silicon sacrificial device wafers. As an etch-stop layer, we have used a 2- μm -thick SiO_2 film. After etching the sacrificial device wafer, the SiO_2 film was removed with a buffered hydrofluoric acid (HF) solution. It is also possible to grind down the main part of the sacrificial device wafer before etching the remaining silicon thickness using KOH or DRIE etching. The grinding speed for 10-cm-diameter silicon wafers is typically more than 100 μm

¹Substrate Bonder SB6, 1996.

TABLE I
MATERIAL PROPERTIES OF CURED BCB FILMS

Dielectric Constant (1KHz)	2.65
Dissipation Factor (1KHz)	0.0008
Breakdown Voltage	3x10 ⁶ V/cm
Volume Resistivity	1019 $\Omega\text{-cm}$
Coefficient of Thermal Expansion	52 ppm/°C
Tensile Modulus	2 GPa
Tensile Strength	85 MPa
Poisson's Ratio	0.34

per minute, which can significantly reduce the total required time for removing the sacrificial device wafer.

C. Electrical Interconnections

To process electrical interconnections between the devices and the target wafer, the intermediate bonding material must be removed on the areas where the interconnections shall be processed, as illustrated in Figs. 1(d) and (e) and 2(e) and (f). The etching of the intermediate BCB bonding material was done with reactive ion etching using 90% O_2 and 10% CF_4 as etch gases [15]. Photoresist was used as the mask material.

The deposition of metal for the electrical interconnections between the devices and the target wafer can be realized using sputtering, metal evaporation, electroplating, electroless plating, chemical-vapor deposition (CVD) metalization, etc. Layer interconnections as small as 1–4 μm^2 with aspect ratios of 6:1 have been reported in the literature [16], [17].

We have fabricated simple evaporated titanium/gold (Ti/Au) interconnections between the top metalization of an example device and the bottom metalization of the target wafer. The thickness of the intermediate BCB bonding layer, including the thickness of the device layer (step height), is 2 μm . We have used an evaporation process with a tilting and rotating mechanism for improved step coverage [18]. Then the Ti/Au was patterned using anisotropic wet etching. The resulting interconnections are 1.7 μm wide, and we have measured a contact resistance of approximately 8 Ω .

III. EXAMPLES OF TRANSFER BONDING

The following examples will demonstrate the potential of the transfer bonding technology. We describe three different variations of the transfer bonding technology, namely, device transfer bonding, film transfer bonding, and a combination of both. In all examples, we have used 10-cm-diameter double-sided-polished p-type silicon wafers.

A. Transfer Bonding of Polycrystalline Silicon Structures

To demonstrate device transfer bonding, we have transferred arrays of polycrystalline silicon structures from a sacrificial device wafer to a target wafer. The sacrificial device wafer was 300 μm and the target wafer 500 μm thick. A 2- μm SiO_2 layer was grown on the sacrificial device wafer using wet oxidation at 1100 $^\circ\text{C}$ for 9 h. A 2- μm -thick low-pressure chemical-vapor deposition (LPCVD) polycrystalline silicon layer was deposited on the sacrificial device wafer and patterned using reactive ion etching and a standard photoresist mask. The dimensions of the resulting structures are shown in Figs. 3 and 4. We bonded the sacrificial device wafer to the target wafer according to the previously described bonding procedure. The thickness of the adhesive BCB coating was 7 μm and the bonding pressure was 1.7 bar. After the bonding procedure, the sacrificial device wafer was removed with DRIE. The required etching time was 150 min. The nonuniform DRIE rate across the wafer caused removal of the silicon at the wafer edge after about 110 min of etching, while it took 150 min to completely remove the silicon in the center of the wafer. When 0.6- μm -thick SiO_2 was used as the etch-stop layer, the SiO_2 at the perimeter of the wafer (a 1.5-cm-wide ring) was etched away. This, in turn, caused the etching of the underlying transferred structures on that area. The SiO_2 layer was removed with buffered HF wet etching. Fig. 3 shows a scanning electron micrograph (SEM) image of the transferred polycrystalline silicon structures that are embedded in the 7- μm -thick BCB layer and Fig. 4 shows a cross-sectional SEM image of such a structure. As can be seen in Fig. 4, the dicing resulted in some chipping of the polycrystalline silicon structure. We have performed device transfer bonding on two sets of wafers with about 1.5 million polycrystalline silicon structures per wafer. No visible damage or delamination of any of the transferred structures has been found.

We have previously reported bonding of wafers with 50- μm -deep and 100- μm -wide channels at the wafer surface using a 5- μm -thick intermediate BCB coating [19]. The 5- μm -thick BCB coating at the bond interface was squeezed into the 50- μm -deep and 100- μm -wide channels and completely filled them. This indicates that the BCB material can be used for transfer bonding of structures with greater aspect ratios than the presented ones and that the BCB will still mold around the transferred structures. We also have achieved transfer bonding where the structures are completely embedded in the BCB using extremely short bonding times of 4 min and curing temperatures of 300 $^\circ\text{C}$. These structures had the same dimensions as the previously described structures.

B. Transfer Bonding of a Polycrystalline Silicon Film

For demonstrating film transfer bonding, we have transferred a polycrystalline silicon film from a sacrificial device wafer to a target wafer. The sacrificial device wafer was 300 μm and the target wafer was 500 μm thick. A 2- μm SiO_2 layer was grown on both wafers using wet oxidation at 1100 $^\circ\text{C}$ for 9 h. Then a 0.7- μm -thick LPCVD polycrystalline silicon film was deposited on the sacrificial device wafer. The sacrificial device wafer was bonded to the target wafer according to the previ-

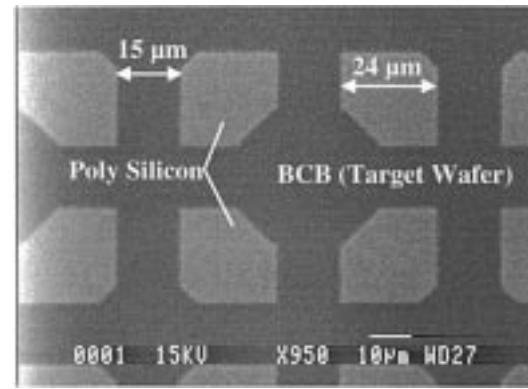


Fig. 3. SEM image of the target wafer with transfer bonded polycrystalline silicon structures.

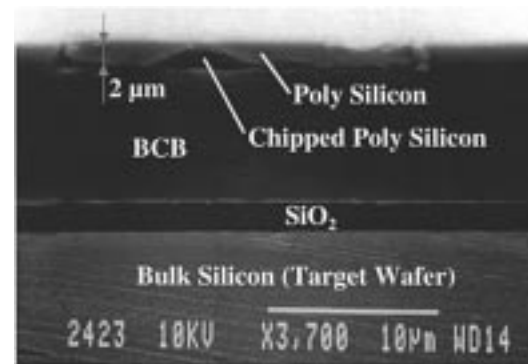


Fig. 4. Cross-sectional SEM image of a transfer bonded polycrystalline silicon structure.

ously described bonding procedure. The thickness of the adhesive BCB coating was 7 μm and the bonding pressure was 2 bar. After the bonding procedure, the sacrificial device wafer was removed using a 30% KOH etch solution at a temperature of 60 $^\circ\text{C}$. The total etching time was approximately 12 h. When a 30% KOH etch solution at a temperature of 80 $^\circ\text{C}$ was used for approximately 3 h and 45 min to remove the sacrificial device wafer, the bond interface at the wafer edge was destroyed. This caused delamination of the transferred film at a ring of about 2 cm around the wafer edge. The SiO_2 etch-stop layer was removed with buffered HF wet etching. Fig. 5 shows the target wafer with the transferred polycrystalline silicon film. Fig. 6 shows a cross-sectional SEM image of the transferred film. We have performed film transfer bonding on three sets of wafers. The transferred film of one of the three wafers was damaged on an area of about 0.4 mm^2 . This was due to a void at the bond interface, which led to local delamination and cracking of the transferred film. On the other two wafers, the transferred polycrystalline silicon films stayed completely intact and crack-free, as can be seen in Fig. 5. The root mean square surface roughness of the transferred polycrystalline silicon films was measured to be $R_q = 0.35$ nm and the average surface roughness was measured to be $R_a = 0.30$ nm. These values are on the same order of magnitude as the surface roughness of standard polished silicon wafers. We have calculated the average intrinsic stress of the 7.7- μm -thick transferred polycrystalline silicon (0.7 μm thick) and BCB (7 μm thick) sandwich layer on two perpendicular axes to be 70 and 72 MPa (compressive stress). Therefore, the

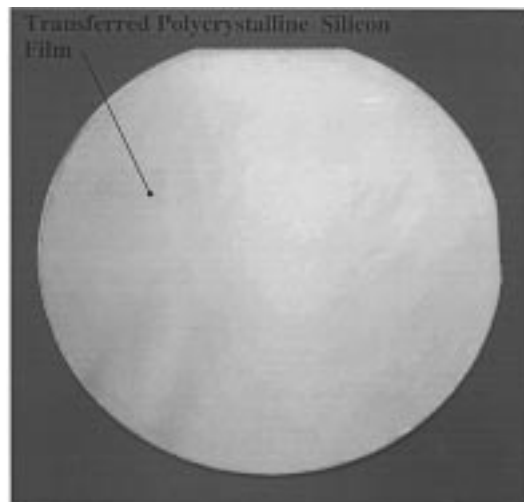


Fig. 5. Target wafer with transfer bonded polycrystalline silicon film without any visible cracks or voids at the bond interface.

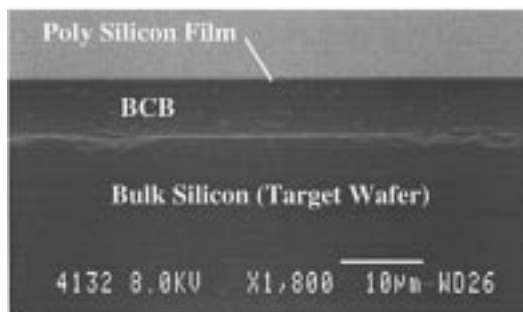


Fig. 6. Cross-sectional SEM image of the transfer bonded polycrystalline silicon film.

bow of the substrate wafer was measured with and without the transferred film sandwich on top. The average stress level has then been calculated using the wafer stress application option of a Tencor P-10 profilometer. In the calculations, we have used $7.7\text{ }\mu\text{m}$ for the film sandwich thickness and $1.805 \times 10^{11}\text{ Pa}$ for the elastic constant of the silicon substrate wafer.

After the film transfer bonding, the polycrystalline silicon film can be processed using a variety of standard IC processes. We have demonstrated the patterning of the polycrystalline silicon film with a photoresist mask and reactive ion etching. Fig. 7 shows a SEM image of the resulting silicon structures on top of the BCB film. No visible damage or delamination of the resulting structures has been found.

C. Transfer Bonding of Test Devices for Temperature Coefficient of Resistance (TCR) Measurements of Thin-Film Materials

In the following section, we describe the transfer bonding of test devices for TCR measurements of thin-film materials. These devices are used for material characterization of thermistor materials, which can be used in uncooled infrared bolometers. The devices are fabricated with the transfer bonding technology because the back sides as well as the front

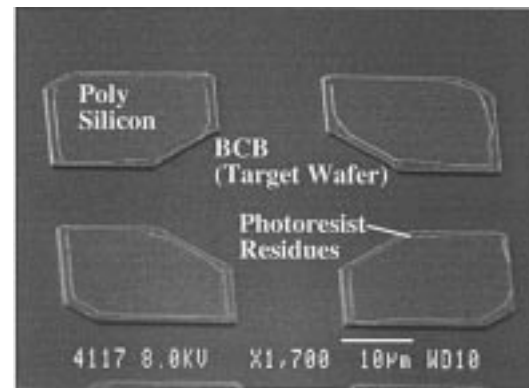


Fig. 7. SEM image of the patterned polycrystalline silicon film.

sides of the devices must be processed. First, two titanium/platinum (Ti/Pt) electrodes are deposited on the front side of the thin-film material. Since a metalization is also needed on the back side of the thin-film material, transfer bonding is needed and allows a molybdenum silicide (MoSi) film to be deposited on the back side of the thin-film material. Thus, the two metal electrodes can be probed and the TCR value of the thin-film material can be measured through the thickness of the thin-film material over the MoSi and back through the thin-film material. To fabricate the devices, we have used a combination of device transfer bonding and film transfer bonding, as illustrated in Fig. 8.

The sacrificial device wafer was $300\text{ }\mu\text{m}$ and the target wafer was $500\text{ }\mu\text{m}$ thick. A $2\text{-}\mu\text{m}$ SiO_2 layer was grown on both wafers using wet oxidation at $1100\text{ }^\circ\text{C}$ for 9 h. A $0.7\text{-}\mu\text{m}$ -thick LPCVD polycrystalline silicon film was deposited on the sacrificial device wafer. Then a $0.01/0.05\text{-}\mu\text{m}$ -thick Ti/Pt film was evaporated on the polycrystalline silicon film and patterned with a standard liftoff process. Finally, the wafer surface was covered with a $0.7\text{-}\mu\text{m}$ -thick plasma-enhanced chemical-vapor-deposited (PECVD) silicon nitride (Si_3N_4) layer. The fully processed sacrificial device wafer consists of silicon bulk material; a SiO_2 etch-stop layer; and a sandwich of a polycrystalline silicon film, patterned Ti/Pt, and a Si_3N_4 film [Fig. 8(a)]. For transfer bonding, the sacrificial device wafer was bonded to the target wafer according to the previously described bonding procedure [Fig. 8(b)]. The thickness of the adhesive BCB coating was $2\text{ }\mu\text{m}$ and the bonding pressure was 2 bar. After the bonding procedure, the sacrificial device wafer was removed using a 30% KOH etch solution at a temperature of $60\text{ }^\circ\text{C}$. The total etching time was approximately 12 h. The SiO_2 etch-stop layer was removed with buffered HF wet etching while the $\text{Si}_3\text{N}_4/\text{Pt}/\text{Ti}/\text{silicon}$ films remained on the target wafer [Fig. 8(c)]. In a subsequent step, we have sputtered a conductive MoSi film onto the top polycrystalline silicon film [Fig. 8(d)]. The resulting film sandwich was patterned with a photoresist mask and reactive ion etching. The patterned Ti/Pt works as a masking material for the underlying Si_3N_4 and BCB films [Fig. 8(e)]. Fig. 9 shows a SEM image of a transfer bonded and fully processed device on the target wafer. We have transfer bonded two sets of wafers containing approximately 260 test devices per wafer. No visible damage or delamination of the devices was found. Thirty devices have been evaluated and all of them were working.

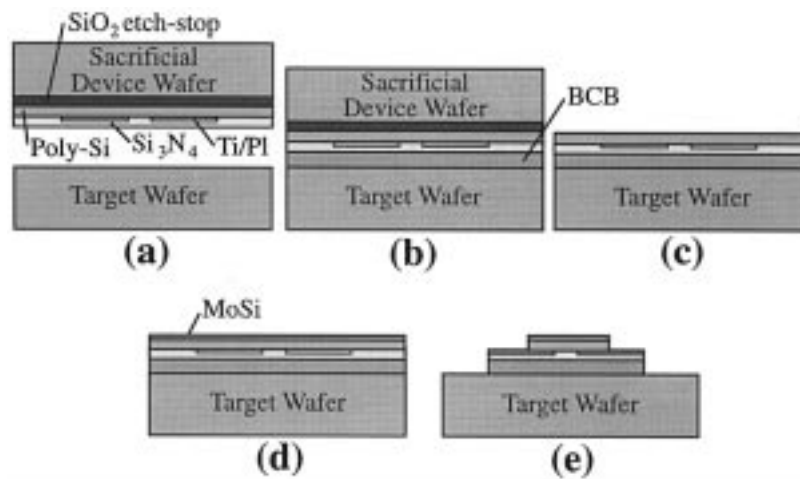


Fig. 8. Process flow for transfer bonding and fabrication of multilayer test devices for TCR measurements of thin-film materials.

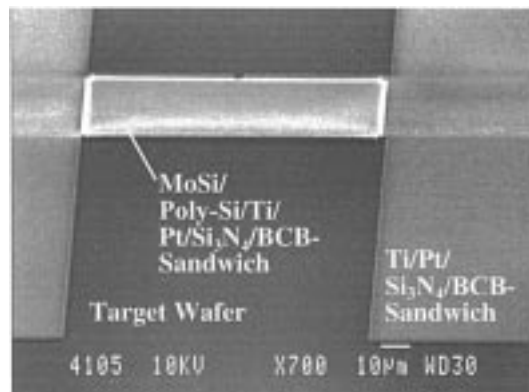


Fig. 9. SEM image of a transfer bonded and etched multilayer test device for TCR measurements of thin film materials as illustrated in Fig. 8(e).

IV. POTENTIALS AND LIMITATIONS OF THE TRANSFER BONDING TECHNOLOGY

Low-temperature transfer bonding opens new opportunities specifically in integrating transducers and ICs. The transducers and the IC fabrication can be optimized independently on different wafers with cost-efficient processes. This allows monocrystalline silicon or other high-temperature annealed, high-performance materials to be used in the transducers. Later, the transducers are transferred and integrated on the IC wafer. The integration is a low-temperature wafer-level process, which only requires standard clean-room equipment (along with a wafer bonder).

For 10-cm-diameter wafers, we have demonstrated a $3\text{-}\mu\text{m}$ bond alignment accuracy between the sacrificial device wafer and the target wafer. For some applications, bond alignment better than $3\text{-}\mu\text{m}$ might be desirable. To date, the alignment accuracy is limited by the bond equipment and the bonding process. Further development of the bond equipment and the bonding process is likely to improve the alignment accuracy in the near future.

The electrical interconnections between the transducers and the target wafer can be below $3 \times 3\text{-}\mu\text{m}^2$. We have achieved a yield of more than 90% for the transfer bonded devices and films. When using BCB as the bonding material, the temperatures for processes after the transfer bonding must not exceed

$350\text{ }^{\circ}\text{C}$. If higher temperatures are needed, an intermediate bonding material, which can withstand these temperatures, must be used. Given the presented specifications, wafer-level transfer bonding can be a competitive alternative to flip-chip bonding, especially for thin-film devices that require small electrical interconnections and have small feature sizes.

V. CONCLUSION

The presented transfer bonding technology is a low-temperature process for transferring devices or films from a sacrificial device wafer to a target wafer. We have demonstrated the transfer bonding technology for different thin-film polycrystalline silicon devices with feature sizes as small as $1.5\text{-}\mu\text{m}$. We have not observed any problems with cracking of the transferred devices/films as reported for other integration technologies [7]. The technology results in excellent yield and is IC compatible. Furthermore, we have demonstrated the processing of simple electrical interconnections between the device metalization and the metalization of the target wafer by using evaporated Ti and Au. The presented wafer-level transfer bonding technology can be a competitive alternative to flip-chip bonding, especially for the integration of thin-film devices with small feature sizes and when small electrical interconnections ($< 3 \times 3\text{-}\mu\text{m}^2$) between the devices and the target wafer are required.

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